Data Sheet

K8T800 Desktop North Bridge

Revision 1.24
September 29, 2004

VIA TECHNOLOGIES, INC.

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Offices:

VIA Technologies Incorporated
USA Office:
940 Mission Court
Fremont, CA 94539
USA
Tel: (510) 683-3300
Fax: (510) 683-3301 or (510) 687-4654
Web: http://www.viatech.com

VIA Technologies Incorporated
Taiwan Office:
1st Floor, No. 531
Chung-Cheng Road, Hsin-Tien
Taipei, Taiwan ROC
Tel: (886-2) 2218-5452
Fax: (886-2) 2218-5453
Web: http://www.via.com.tw

REVISION HISTORY

Document Release	Date	Revision	Initials
1.0	4/23/03	Initial external release (same as internal review release rev 0.71 except for fix of V-Link voltage typographical error in note 2 under "Absolute Max" electrical specs)	DH
1.1	6/9/03	Changed product name to K8T800	DH
1.11	6/30/03	Fixed south bridge strap names in VAD pin definitions Corrected voltages for VCCATX, VCCARX, VCCSUS	DH
1.12	7/9/03	Fixed trademarks list; Fixed MHz, MT/s terminology in feature bullets Fixed missing block diagrams and incorrect document revision in page footers Changed south bridge to VT8237	DH
1.2	10/9/03	Changed cover page and page heading formats Updated feature bullets, overview and block diagram to match Product Brief	AT
1.21	10/28/03	Fixed grammatical and format errors in feature bullets and overview Added system power management support in the feature bullets	AT
1.22	11/20/03	Removed strapping information from the V-Link pin description table Added a strap pins table Updated Function 0 RxB2 [6-5, 2-0]	AT
1.23	2/27/04	Minor updates on product features and overview sections Corrected signal HTSTOP# description in pin description table Updated Strap Pins table Corrected voltages for VCCATX	AT
1.24	9/29/04	Added HyperTransport trademark notice Spelled out corp. to corporation in legal page Renamed HTSTOP# to LDTSTOP# Updated D0 Rx57 register name Added lead-free mechanical package diagram	SV

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K8T800 NORTH BRIDGE

800MHz AMD Opteron / Athlon 64 HyperTransport Interface
533 MB / Sec V-Link Interface
8x / 4x AGP Bus

PRODUCT FEATURES

- **Defines Highly Integrated Solutions for Performance Desktop PC Designs**
  - High performance North Bridge with HyperTransport interface to AMD Opteron / Athlon 64 CPU plus AGP 8x bus to external Graphics Controller and high-speed V-Link interface to South Bridge
  - Combines with VIA VT8235 / VT8237 V-Link South Bridge for integrated 10/100 LAN, Audio, ATA133 IDE, LPC, USB 2.0 ports and Serial ATA (VT8237)
  - 35 x 35 mm BGA package (Ball Grid Array) with 578 balls and 1.27mm ball pitch
  - 2.5V core, 0.22 u process
- **High Performance HyperTransport CPU Interface**
  - Processor interface via HyperTransport interface
  - 800 / 600 / 400 / 200 MHz clock rates with 1600 / 1200 / 800 / 400 MT/s (Mega-Transfers per second) in both directions simultaneously (up to 6.4 GB/sec using 16-bit data transfer mode)
  - 8 or 16-bit control / address / data transfer both directions (transmit and receive may be different widths and / or speeds)
  - Default 8-bit / 200 MHz operation on startup with speedup to dual 16-bit, 800 MHz operation under software control
  - Supports isochronous AGP-to-CPU and PCI-to-CPU transactions
- **Full Featured Accelerated Graphics Port (AGP) Controller**
  - AGP v3.0 compliant 8x / 4x transfer mode with Fast Write support
  - 1.5V AGP I/O interface
  - Pipelined split-transaction long-burst transfers up to 2.1 GB / Sec (4 bytes x 533 MHz)
  - Supports Side Band Addressing (SBA) mode
  - Supports Flush / Fence commands
  - Supports DBI (Dynamic Bus Inversion)
  - Pseudo-synchronous AGP and CPU interfaces with optimal skew control
  - Thirty-two level read and write request queue
  - One-ninety-two level (quadwords) read data FIFO (1,536 bytes)
  - Sixty-four level (quadwords) write data FIFO (512 bytes)
  - Graphics Address Relocation Table (GART)
    - One level TLB structure
    - Sixteen entry fully associative page table
    - LRU replacement scheme
  - VPX-64 / VPX-II support (see separate VIA VT8101 and VT8102 data sheets)

- **High Bandwidth 533 MB/Sec V-Link Host Controller**
  - Supports 66 MHz, 4x and 8x transfer modes, V-Link Host interface with total bandwidth of 533 MB/sec
  - Half duplex transfers with separate command / strobe for 4x8 bit mode and full duplex for 8x4 bit mode
  - Request / Data split transaction
  - Transaction assurance for V-Link Host to Client access eliminates V-Link Host-Client Retry cycles
  - Intelligent V-Link transaction protocol to minimize data wait-state / throttle transfer latency
  - Highly efficient V-Link arbitration with minimum overhead)
- **Advanced System Power Management Support**
  - ACPI 2.0 and PCI Bus Power Management 1.1 compliant
  - Supports LDTSTOP# (HyperTransport Bus Stop) protocol
  - Low-leakage I/O pads

K8T800 SYSTEM OVERVIEW

The K8T800 North Bridge is a high performance, cost-effective and energy efficient North Bridge for the implementation of 64-bit capable server, workstation and desktop personal computer systems based on AMD Opteron / Athlon 64 processors.

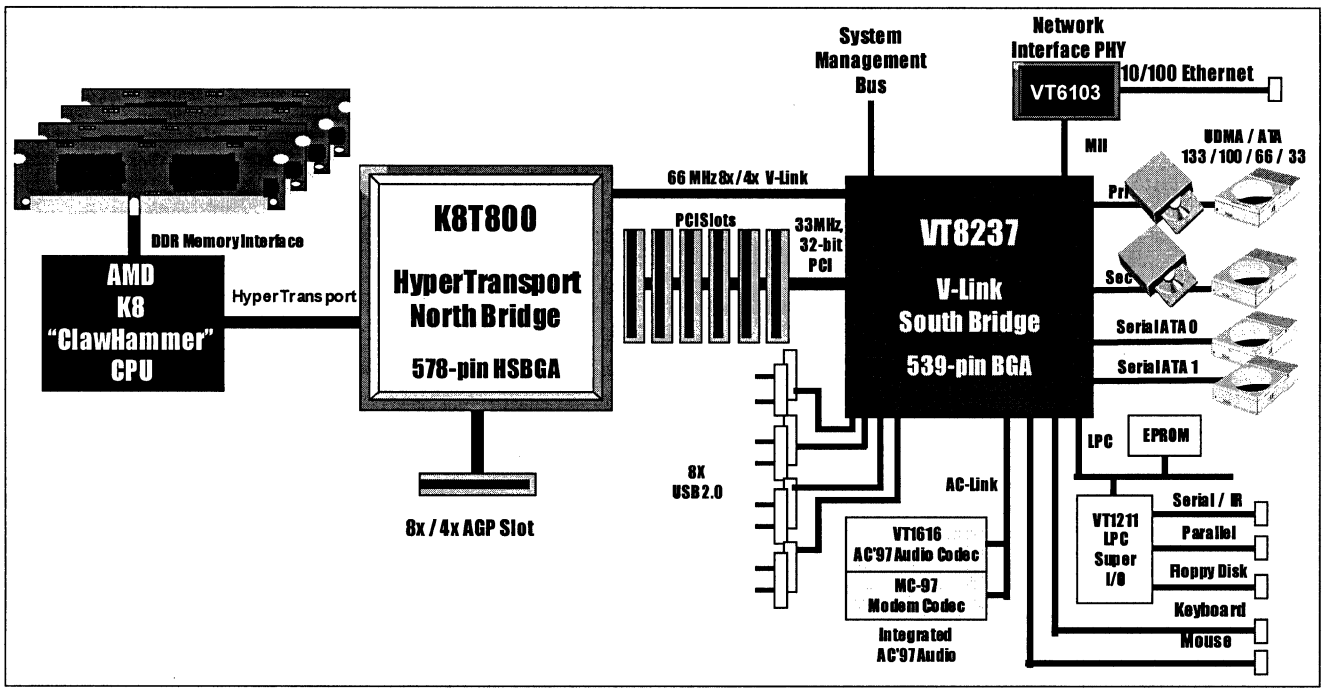


Figure 1. System Block Diagram

A complete 64-bit Opteron / Athlon 64 chip set consists of the K8T800 North Bridge and the VT8237 V-Link South Bridge. The K8T800 provides superior performance between the CPU / HyperTransport, V-Link interface and AGP 8x bus with pipelined, burst and concurrent operation. The VT8237 is a highly integrated peripheral controller, it includes V-Link-to-PCI / V-Link-to-LPC controllers and integrates Serial ATA and Ultra DMA IDE controllers, USB2.0 host controller, 10/100Mb networking MAC, AC97 and system power management controllers. Its internal bus structure is based on a 66 MHz PCI bus that provides 2x bandwidth compared to previous generation PCI bridge chips.

K8T800 Overview

The K8T800 interfaces to the AMD Opteron / Athlon 64 processor via the HyperTransport interface with data transfer rate of 1.6 GT/sec, 1.2 GT/sec, 800 MT/sec or 400 MT/sec each direction (input and output), simultaneously, providing a total maximum data transfer bandwidth of 6.4 GB/sec. Isochronous AGP-to-CPU and PCI Master-to-CPU transactions are supported for time constraint, periodic data transmissions.

The AGP controller is AGP v3.0 compliant with up to 2.1GB/second data transfer rate capability. It supports pseudo-synchronous AGP and HyperTransport interface for optimal system performance. Deep read (1536 bytes) and write (512 bytes) FIFO are integrated for optimal bus utilization and minimum data transfer latency.

The K8T800 North Bridge interfaces to the South Bridge through the high speed 8x 66 MHz (533 MB / Sec) V-Link interface. Deep pre-fetch and post write buffers are included to allow for concurrent CPU and V-Link operation. The combined K8T800 North Bridge and VT8237 South Bridge system supports enhanced PCI bus commands such as "Memory-Read-Line", "Memory-Read-Multiple" and "Memory-Write-Invalid" commands to minimize snoop overhead. In addition, advanced features are supported such as CPU write-back forward to PCI master and CPU write-back merged with PCI post write buffers to minimize

PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

System Power Management

For sophisticated system power management, the K8T800 supports LDTSTOP# (HyperTransport Bus Stop) protocol to minimize power consumption during suspend system states (S1 and S3). Coupled with the VT8237 South Bridge chip, a complete power conscious PC main board can be implemented with no external glue logic.

PINOUTS

Figure 2. Ball Diagram (Top View)

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	NC	NC	NC	NC	NC	NC	NC	GND	VCC HT	VCC HT	G CLK	LDT STOP#	TCAD 1	TCAD 1#	TCAD 3	TCAD 3#	TCAD 4	TCAD 4#	TCAD 6	TCAD 6#	T CTL	T CTL#	GND	VCC HT	VCC HT	VCC HT
B	NC	NC	NC	NC	NC	NC	NC	GND	VCC HT	VCC HT	HT RST#	TCAD 0	GND	TCAD 2	GND	TCLK 0	GND	TCAD 5	GND	TCAD 7	GND	GND	VCC HT	VCC HT	VCC HT	VCC HT
C	NC	NC	NC	NC	NC	NC	NC	GND	VCC HT	VCC HT	VCC HT	TCAD 0#	TCAD 9#	TCAD 2#	TCAD 11#	TCLK 0#	TCAD 12#	TCAD 5#	TCAD 14#	TCAD 7#	GNDA TX	VCCA TX	VCC HT	VCC HT	VCC HT	RT COMP
D	NC	NC	NC	NC	NC	GND	NC	GND	VCC HT	VCC HT	VCC HT	GND	TCAD 9	GND	TCAD 11	GND	TCAD 12	GND	TCAD 14	GND	TCAD 15#	VCC HT	VCC HT	VCC HT	RP COMP	RN COMP
E	NC	NC	NC	NC	GND	GND	NC	GND	VCC HT	VCC HT	VCC HT	TCAD 8	TCAD 8#	TCAD 10	TCAD 10#	TCLK 1	TCLK 1#	TCAD 13	TCAD 13#	TCAD 15	VCC HT	VCC HT	VCC HT	VCC HT	VCCA RX	GNDA RX
F	NC	NC	NC	NC	NC	NC	GND	GND	VCC	VCC HT	VCC HT	GND	GND	GND	VCC HT	VCC HT	GND	GND	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	R CTL	R CTL#	GND
G	GND	NC	NC	NC	NC	G6	G7	G8	9	10	11	12	13	14	15	16	17	18	G19	G20	VCC HT	VCC HT	RCAD 15#	RCAD 15	GND	RCAD 7#
H	GND	GND	NC	NC	NC	H6		VCC	VCC	VCC	VCC	VCC			VCC	VCC				H	VCC HT	RCAD 14#	GND	RCAD 6	RCAD 6#	RCAD 7
J	NC	GND	GND	NC	NC	J		VCC		VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	GND		J	GND	RCAD 14	RCAD 13#	RCAD 13	GND	RCAD 5#
K	NC	NC	NC	GND	NC	K				GND	GND	GND	GND	GND	GND	GND	GND	VCC HT	VCC	K	VCC HT	RCAD 12#	GND	RCAD 4	RCAD 4#	RCAD 5
L	NC	NC	NC	NC	NC	L				GND	GND	GND	GND	GND	GND	GND	GND	VCC HT	VCC	L	VCC HT	RCAD 12	RCLK 1#	RCLK 1	GND	RCLK 0#
M	NC	NC	NC	NC	NC	M		VCC AGP		GND	GND	GND	GND	GND	GND	GND	GND	VCC HT	VCC	M	GND	RCAD 11#	GND	RCAD 3	RCAD 3#	RCLK 0
N	NC	NC	NC	NC	NC	N		VCC AGP		GND	GND	GND	GND	GND	GND	GND	GND	VCC HT		N	VCC HT	RCAD 11	RCAD 10#	RCAD 10	GND	RCAD 2#
P	NC	NC	NC	NC	GND	P		VCC		GND	GND	GND	GND	GND	GND	GND	GND	VCC HT		P	VCC HT	RCAD 9#	GND	RCAD 1	RCAD 1#	RCAD 2
R	GND	GND	GND	GND	GND	R		VCC		GND	GND	GND	GND	GND	GND	GND	GND	VCC HT	VCC	R	GND	RCAD 9	RCAD 8#	RCAD 8	GND	RCAD 0#
T	GND QQ	VCC AGP	VCC AGP	VCC AGP	VCC AGP	T		VCC AGP	VCC AGP	GND	GND	GND	GND	GND	GND	GND	GND	VCC HT	VCC	T	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	RCAD 0
U	VCC QQ	VCC AGP	VCC AGP	VCC AGP	VCC AGP	U		VCC AGP	VCC AGP	GND	GND	GND	GND	GND	GND	GND	GND	VCC HT	VCC	U	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT
V	AGP PCMP	VCC AGP	VCC AGP	VCC AGP	GND	V		VCC AGP	VCC AGP	VCC AGP	VCC AGP	VCC AGP	VCC AGP	VCC VL	VCC VL	VCC VL	VCC VL	VCC	VCC	V	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT
W	AGP NCMP	VCC AGP	VCC AGP	VCC AGP	GND	W6			VCC AGP	VCC	VCC	VCC	VCC	VCC	VCC VL	VCC VL	VCC VL	VCC VL	VCC	W	GND	GND	GND	GND	GND	GND
Y	G REQ	AGP8X DT#	VCC AGP	VCC AGP	VCC AGP	Y6														VCC	VCC	VCC	VCC	VCC	VCC	VCC
AA	ST1	ST0	G GNT	VCC AGP	VCC AGP	AA6	7	8	9	10	11	12	13	14	15	16	17	18	19	AA20	VCC	VCC	VCC	VCC	VCC	VCC
AB	ST2	GND	GND	GND	GND	GND	VCC AGP	VCC AGP	GND	GND	VCC AGP	VCC AGP	VCC AGP	VCC AGP	GND	GND	VCC VL	VCC VL	VCC VL	VCC VL	VCC	VCC	VCC	VCC	VCC	VCC
AC	G WBF	SBA 0#	SBA 1#	G DBIL	G DBIH	AGP VREF	G BE3	GND	G FRM	G IRDY	G DSEL	G STOP	AGP VREF	G TRDY	G SERR	G PAR	DE BUG	VCC VL	VCC VL	VCC VL	VCC VL	GND	GND	GND	VCC SUS	TEST IN
AD	SBA 2#	SBA 3#	SBA 5#	GD31	GD27	G RBF	GD25	GD23	GD19	GD16	G BE2	GD13	GD10	GD9	G BE0	GD5	GD4	GD1	VL PCOMP	VAD 0	VAD 1	DN STB#	DN CMD	VAD 6	RE SET#	SUS ST#
AE	SBSS SBS#	GND	SBA 6#	GD30	GND	GD26	GDS1F GDS1	GND	GD22	GD17	GND	GD15	GD11	GND	GDS0F GDS0	GD6	GND	GD2	VAD 4	GND	V BE#	GND	UP STB	VAD 3	GND	PWR OK
AF	SBSF SBS	SBA 4#	SBA 7#	GD29	GD28	GD24	GDS1S GDS1#	GD21	GD20	GD18	G BE1	GD14	GD12	GD8	GDS0S GDS0#	GD7	GD3	GD0	V PAR	VAD 5	VL VREF	DN STB	UP STB#	VAD 2	VAD 7	UP CMD

Pin Lists

Table 1. Pin List (Numerical Order)

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Names	Pin #		Pin Name
A11	I	GCLK	E12	O	TCAD8	N22	I	RCAD11	AD01	I	SBA2#	AF01	I	SBSF / SBS
A12	I	LDTSTOP#	E13	O	TCAD8#	N23	I	RCAD10#	AD02	I	SBA3#	AF02	I	SBA4#
A13	O	TCAD1	E14	O	TCAD10	N24	I	RCAD10	AD03	I	SBA5#	AF03	I	SBA7#
A14	O	TCAD1#	E15	O	TCAD10#	N26	I	RCAD2#	AD04	IO	GD31	AF04	IO	GD29
A15	O	TCAD3	E16	O	TCLK1	P22	I	RCAD9#	AD05	IO	GD27	AF05	IO	GD28
A16	O	TCAD3#	E17	O	TCLK1#	P24	I	RCAD1	AD06	I	GRBF	AF06	IO	GD24
A17	O	TCAD4	E18	O	TCAD13	P25	I	RCAD1#	AD07	IO	GD25	AF07	IO	GDS1S / GDS1#
A18	O	TCAD4#	E19	O	TCAD13#	P26	I	RCAD2	AD08	IO	GD23	AF08	IO	GD21
A19	O	TCAD6	E20	O	TCAD15	R22	I	RCAD9	AD09	IO	GD19	AF09	IO	GD20
A20	O	TCAD6#	**E25**	**P**	**VCCARX**	R23	I	RCAD8#	AD10	IO	GD16	AF10	IO	GD18
A21	O	TCTL	**E26**	**P**	**GNDARX**	R24	I	RCAD8	AD11	IO	GBE2	AF11	IO	GBE1
A22	O	TCTL#	F24	I	RCTL	R26	I	RCAD0#	AD12	IO	GD13	AF12	IO	GD14
B11	O	HTRST#	F25	I	RCTL#	**T01**	**P**	**GNDQQ**	AD13	IO	GD10	AF13	IO	GD12
B12	O	TCAD0	G23	I	RCAD15#	T26	I	RCAD0	AD14	IO	GD9	AF14	IO	GD8
B14	O	TCAD2	G24	I	RCAD15	**U01**	**P**	**VCCQQ**	AD15	IO	GBE0	AF15	IO	GDS0S / GDS0#
B16	O	TCLK0	G26	I	RCAD7#	V01	AI	AGPPCOMP	AD16	IO	GD5	AF16	IO	GD7
B18	O	TCAD5	H22	I	RCAD14#	W01	AI	AGPNCOMP	AD17	IO	GD4	AF17	IO	GD3
B20	O	TCAD7	H24	I	RCAD6	Y01	I	GREQ	AD18	IO	GD1	AF18	IO	GD0
C12	O	TCAD0#	H25	I	RCAD6#	Y02	I	AGP8XDT#	AD19	AI	VLPCOMP	AF19	IO	VPAR
C13	O	TCAD9#	H26	I	RCAD7	AA01	O	ST1	AD20	IO	VAD0	AF20	IO	VAD5
C14	O	TCAD2#	J22	I	RCAD14	AA02	O	ST0	AD21	IO	VAD1	**AF21**	**P**	**VLVREF**
C15	O	TCAD11#	J23	I	RCAD13#	AA03	O	GGNT	AD22	O	DNSTB#	AF22	O	DNSTB
C16	O	TCLK0#	J24	I	RCAD13	AB01	O	ST2	AD23	O	DNCMD	AF23	I	UPSTB#
C17	O	TCAD12#	J26	I	RCAD5#	AC01	I	GWBF	AD24	IO	VAD6	AF24	IO	VAD2
C18	O	TCAD5#	K22	I	RCAD12#	AC02	I	SBA0#	AD25	I	RESET#	AF25	IO	VAD7
C19	O	TCAD14#	K24	I	RCAD4	AC03	I	SBA1#	AD26	I	SUSST#	AF26	I	UPCMD
C20	O	TCAD7#	K25	I	RCAD4#	AC04	IO	GDBIL	AE01	I	SBSS / SBS#			
C21	**P**	**GNDATX**	K26	I	RCAD5	AC05	IO	GDBIH / GPIPE#	AE03	I	SBA6			
C22	**P**	**VCCATX**	L22	I	RCAD12	**AC06**	**P**	**AGPVREF**	AE04	IO	GD30			
C26	AI	RTCOMP	L23	I	RCLK1#	AC07	IO	GBE3	AE06	IO	GD26			
D13	O	TCAD9	L24	I	RCLK1	AC09	IO	GFRM	AE07	IO	GDS1F / GDS1			
D15	O	TCAD11	L26	I	RCLK0#	AC10	IO	GIRDY	AE09	IO	GD22			
D17	O	TCAD12	M22	I	RCAD11#	AC11	IO	GDSEL	AE10	IO	GD17			
D19	O	TCAD14	M24	I	RCAD3	AC12	IO	GSTOP	AE12	IO	GD15			
D21	O	TCAD15#	M25	I	RCAD3#	**AC13**	**P**	**AGPVREF**	AE13	IO	GD11			
D25	AI	RPCOMP	M26	I	RCLK0	AC14	IO	GTRDY	AE15	IO	GDS0F / GDS0			
D26	AI	RNCOMP				AC15	IO	GSERR	AE16	IO	GD6			
						AC16	IO	GPAR	AE18	IO	GD2			
						AC17		DEBUG	AE19	IO	VAD4			
						AC25	**P**	**VCCSUS**	AE21	IO	VBE#			
						AC26	I	TESTIN	AE23	I	UPSTB			
									AE24	IO	VAD3			
									AE26	I	PWROK			

NC (71 pins): A1-7, B1-7, C1-7, D1-5,7, E1-4,7, F1-6, G2-5, H3-5, J1,4-5, K1-3,5, L1-5, M1-5, N1-5, P1-4

VCCAGP (38 pins): M8, N8, T2-5,8-9, U2-5,8-9, V2-4,8-13, W2-4,9, Y3-5, AA4-5, AB7-8,11-14

VCCVL (16 pins): V14-17, W15-18, AB17-20, AC18-21

VCCHT (79 pins): A9-10,24-26, B9-10,23-26, C9-11,23-25, D9-11,22-24, E9-11,21-24, F10-11,15-16,19-23, G21-22, H21, J10-17, K18,21, L18,21, M18, N18,21, P18,21, R18, T18,21-25, U18,21-26, V21-26

VCC (44 pins): F9, H8-12,15-16, J8, K19, L19, M19, P8, R8,19, T19, U19, V18-19, W10-14,19, Y20-26, AA21-26, AB21-26

GND (147 pins): A8,23, B8,13,15,17,19,21-22, C8, D6,8,12,14,16,18,20, E5-6,8, F7-8,12-14,17-18,26, G1,25, H1-2,23, J2-3,18,21,25, K4,10-17,23, L10-17,25, M10-17,21,23, N10-17,25, P5,10-17,23, R1-5,10-17,21,25, T10-17, U10-17, V5, W5,21-26, AB2-6,9-10,15-16, AC8,22-24, AE2,5,8,11,14,17,20,22,25

Table 2. Pin List (Alphabetical Order)

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Names	Pin #		Pin Name
Y02	I	AGP8XDT#	AF06	IO	GD24	T26	I	RCAD0	AD25	I	RESET#	B12	O	TCAD0	AC26	I	TESTIN
W01	AI	AGPNCOMP	AD07	IO	GD25	R26	I	RCAD0#	D26	AI	RNCOMP	C12	O	TCAD0#	AF26	I	UPCMD
V01	AI	AGPPCOMP	AE06	IO	GD26	P24	I	RCAD1	D25	AI	RPCOMP	A13	O	TCAD1	AE23	I	UPSTB
AC06	**P**	**AGPVREF**	AD05	IO	GD27	P25	I	RCAD1#	C26	AI	RTCOMP	A14	O	TCAD1#	AF23	I	UPSTB#
AC13	**P**	**AGPVREF**	AF05	IO	GD28	P26	I	RCAD2	AC02	I	SBA0#	B14	O	TCAD2	AD20	IO	VAD0
AC17		DEBUG	AF04	IO	GD29	N26	I	RCAD2#	AC03	I	SBA1#	C14	O	TCAD2#	AD21	IO	VAD1
AD23	O	DNCMD	AE04	IO	GD30	M24	I	RCAD3	AD01	I	SBA2#	A15	O	TCAD3	AF24	IO	VAD2
AF22	O	DNSTB	AD04	IO	GD31	M25	I	RCAD3#	AD02	I	SBA3#	A16	O	TCAD3#	AE24	IO	VAD3
AD22	O	DNSTB#	AC05	IO	GDBIH / GPIPE#	K24	I	RCAD4	AF02	I	SBA4#	A17	O	TCAD4	AE19	IO	VAD4
AD15	IO	GBE0	AC04	IO	GDBIL	K25	I	RCAD4#	AD03	I	SBA5#	A18	O	TCAD4#	AF20	IO	VAD5
AF11	IO	GBE1	AE15	IO	GDS0F / GDS0	K26	I	RCAD5	AE03	I	SBA6#	B18	O	TCAD5	AD24	IO	VAD6
AD11	IO	GBE2	AF15	IO	GDS0S / GDS0#	J26	I	RCAD5#	AF03	I	SBA7#	C18	O	TCAD5#	AF25	IO	VAD7
AC07	IO	GBE3	AE07	IO	GDS1F / GDS1	H24	I	RCAD6	AF01	I	SBSF / SBS	A19	O	TCAD6	AE21	IO	VBE#
A11	I	GCLK	AF07	IO	GDS1S / GDS1#	H25	I	RCAD6#	AE01	I	SBSS / SBS#	A20	O	TCAD6#	**E25**	**P**	**VCCARX**
AF18	IO	GD0	AC11	IO	GDSEL	H26	I	RCAD7	AA02	O	ST0	B20	O	TCAD7	**C22**	**P**	**VCCATX**
AD18	IO	GD1	AC09	IO	GFRM	G26	I	RCAD7#	AA01	O	ST1	C20	O	TCAD7#	**U01**	**P**	**VCCQQ**
AE18	IO	GD2	AA03	O	GGNT	R24	I	RCAD8	AB01	O	ST2	E12	O	TCAD8	**AC25**	**P**	**VCCSUS**
AF17	IO	GD3	AC10	IO	GIRDY	R23	I	RCAD8#	AD26	I	SUSST#	E13	O	TCAD8#	AD19	AI	VLPCOMP
AD17	IO	GD4	**E26**	**P**	**GNDARX**	R22	I	RCAD9				D13	O	TCAD9	**AF21**	**P**	**VLVREF**
AD16	IO	GD5	**C21**	**P**	**GNDATX**	P22	I	RCAD9#				C13	O	TCAD9#	AF19	IO	VPAR
AE16	IO	GD6	**T01**	**P**	**GNDQQ**	N24	I	RCAD10				E14	O	TCAD10			
AF16	IO	GD7	AC16	IO	GPAR	N23	I	RCAD10#				E15	O	TCAD10#			
AF14	IO	GD8	AD06	I	GRBF	N22	I	RCAD11				D15	O	TCAD11			
AD14	IO	GD9	Y01	I	GREQ	M22	I	RCAD11#				C15	O	TCAD11#			
AD13	IO	GD10	AC15	IO	GSERR	L22	I	RCAD12				D17	O	TCAD12			
AE13	IO	GD11	AC12	IO	GSTOP	K22	I	RCAD12#				C17	O	TCAD12#			
AF13	IO	GD12	AC14	IO	GTRDY	J24	I	RCAD13				E18	O	TCAD13			
AD12	IO	GD13	AC01	I	GWBF	J23	I	RCAD13#				E19	O	TCAD13#			
AF12	IO	GD14	B11	O	HTRST#	J22	I	RCAD14				D19	O	TCAD14			
AE12	IO	GD15	A12	I	LDTSTOP#	H22	I	RCAD14#				C19	O	TCAD14#			
AD10	IO	GD16	AE26	I	PWROK	G24	I	RCAD15				E20	O	TCAD15			
AE10	IO	GD17				G23	I	RCAD15#				D21	O	TCAD15#			
AF10	IO	GD18				M26	I	RCLK0				B16	O	TCLK0			
AD09	IO	GD19				L26	I	RCLK0#				C16	O	TCLK0#			
AF09	IO	GD20				L24	I	RCLK1				E16	O	TCLK1			
AF08	IO	GD21				L23	I	RCLK1#				E17	O	TCLK1#			
AE09	IO	GD22				F24	I	RCTL				A21	O	TCTL			
AD08	IO	GD23				F25	I	RCTL#				A22	O	TCTL#			

NC (71 pins): A1-7, B1-7, C1-7, D1-5,7, E1-4,7, F1-6, G2-5, H3-5, J1,4-5, K1-3,5, L1-5, M1-5, N1-5, P1-4

VCCAGP (38 pins): M8, N8, T2-5,8-9, U2-5,8-9, V2-4,8-13, W2-4,9, Y3-5, AA4-5, AB7-8,11-14

VCCVL (16 pins): V14-17, W15-18, AB17-20, AC18-21

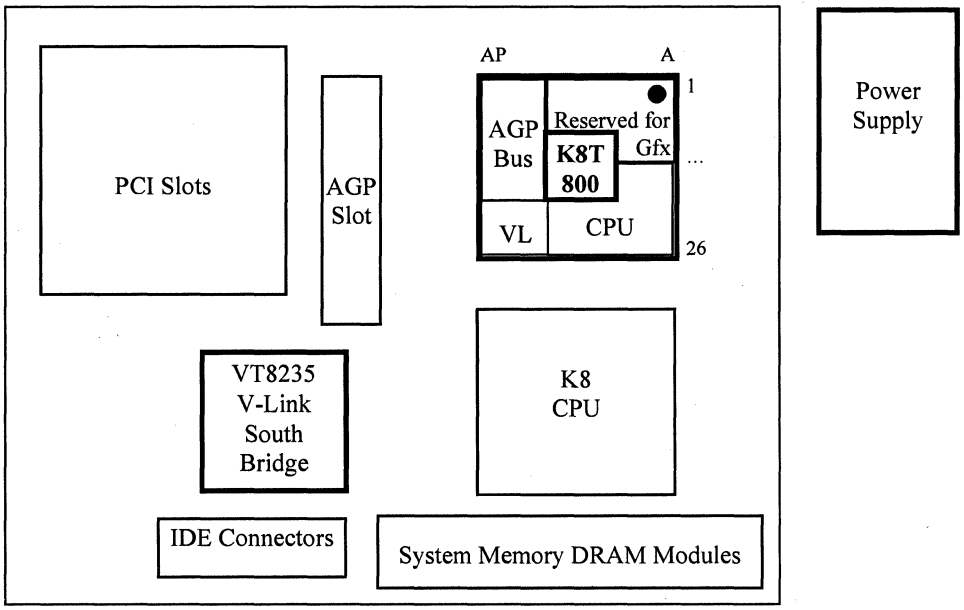
VCCHT (79 pins): A9-10,24-26, B9-10,23-26, C9-11,23-25, D9-11,22-24, E9-11,21-24, F10-11,15-16,19-23, G21-22, H21, J10-17, K18,21, L18,21, M18, N18,21, P18,21, R18, T18,21-25, U18,21-26, V21-26

VCC (44 pins): F9, H8-12,15-16, J8, K19, L19, M19, P8, R8,19, T19, U19, V18-19, W10-14,19, Y20-26, AA21-26, AB21-26

GND (147 pins): A8,23, B8,13,15,17,19,21-22, C8, D6,8,12,14,16,18,20, E5-6,8, F7-8,12-14,17-18,26, G1,25, H1-2,23, J2-3,18,21,25, K4,10-17,23, L10-17,25, M10-17,21,23, N10-17,25, P5,10-17,23, R1-5,10-17,21,25, T10-17, U10-17, V5, W5,21-26, AB2-6,9-10,15-16, AC8,22-24, AE2,5,8,11,14,17,20,22,25

Pin Arrangement

Pinouts for the K8T800 North Bridge chip were defined assuming the ATX PCB layout model shown below (and general pin layout shown) as a guide for PCB component placement. Other PCB layouts (AT, LPX and NLX) were also considered and can typically follow the same general component placement. If desired by the PCB layout engineer, for better routing, the North Bridge chip can be oriented 45 degrees clockwise rotated from the position shown below.



Pin Descriptions

Table 3. Pin Descriptions

Signal Name	Pin #	I/O	Signal Description
"HyperTransport" Transmit Interface			
TCAD15 / TCAD15#	E20, D21	O	**Transmit Differential Control / Address / Data Pair 15.**
TCAD14 / TCAD14#	D19, C19	O	**Transmit Differential Control / Address / Data Pair 14.**
TCAD13 / TCAD13#	E18, E19	O	**Transmit Differential Control / Address / Data Pair 13.**
TCAD12 / TCAD12#	D17, C17	O	**Transmit Differential Control / Address / Data Pair 12.**
TCAD11 / TCAD11#	D15, C15	O	**Transmit Differential Control / Address / Data Pair 11.**
TCAD10 / TCAD10#	E14, E15	O	**Transmit Differential Control / Address / Data Pair 10.**
TCAD9 / TCAD9#	D13, C13	O	**Transmit Differential Control / Address / Data Pair 9.**
TCAD8 / TCAD8#	E12, E13	O	**Transmit Differential Control / Address / Data Pair 8.**
TCAD7 / TCAD7#	B20, C20	O	**Transmit Differential Control / Address / Data Pair 7.**
TCAD6 / TCAD6#	A19, A20	O	**Transmit Differential Control / Address / Data Pair 6.**
TCAD5 / TCAD5#	B18, C18	O	**Transmit Differential Control / Address / Data Pair 5.**
TCAD4 / TCAD4#	A17, A18	O	**Transmit Differential Control / Address / Data Pair 4.**
TCAD3 / TCAD3#	A15, A16	O	**Transmit Differential Control / Address / Data Pair 3.**
TCAD2 / TCAD2#	B14, C14	O	**Transmit Differential Control / Address / Data Pair 2.**
TCAD1 / TCAD1#	A13, A14	O	**Transmit Differential Control / Address / Data Pair 1.**
TCAD0 / TCAD0#	B12, C12	O	**Transmit Differential Control / Address / Data Pair 0.**
TCLK0 / TCLK0#	B16, C16	O	**Transmit Differential Clock Pair 0.** Clock for TCAD 0-7.
TCLK1 / TCLK1#	E16, E17	O	**Transmit Differential Clock Pair 1.** Clock for TCAD 8-15.
TCTL / TCTL#	A21, A22	O	**Transmit Differential Control.**
"HyperTransport" Receive Interface			
RCAD15 / RCAD15#	G24, G23	I	**Receive Differential Control / Address / Data Pair 15.**
RCAD14 / RCAD14#	J22, H22	I	**Receive Differential Control / Address / Data Pair 14.**
RCAD13 / RCAD13#	J24, J23	I	**Receive Differential Control / Address / Data Pair 13.**
RCAD12 / RCAD12#	L22, K22	I	**Receive Differential Control / Address / Data Pair 12.**
RCAD11 / RCAD11#	N22, M22	I	**Receive Differential Control / Address / Data Pair 11.**
RCAD10 / RCAD10#	N24, N23	I	**Receive Differential Control / Address / Data Pair 10.**
RCAD9 / RCAD9#	R22, P22	I	**Receive Differential Control / Address / Data Pair 9.**
RCAD8 / RCAD8#	R24, R23	I	**Receive Differential Control / Address / Data Pair 8.**
RCAD7 / RCAD7#	H26, G26	I	**Receive Differential Control / Address / Data Pair 7.**
RCAD6 / RCAD6#	H24, H25	I	**Receive Differential Control / Address / Data Pair 6.**
RCAD5 / RCAD5#	K26, J26	I	**Receive Differential Control / Address / Data Pair 5.**
RCAD4 / RCAD4#	K24, K25	I	**Receive Differential Control / Address / Data Pair 4.**
RCAD3 / RCAD3#	M24, M25	I	**Receive Differential Control / Address / Data Pair 3.**
RCAD2 / RCAD2#	P26, N26	I	**Receive Differential Control / Address / Data Pair 2.**
RCAD1 / RCAD1#	P24, P25	I	**Receive Differential Control / Address / Data Pair 1.**
RCAD0 / RCAD0#	T26, R26	I	**Receive Differential Control / Address / Data Pair 0.**
RCLK0 / RCLK0#	M26, L26	I	**Receive Differential Clock Pair 0.** Clock for RCAD 0-7.
RCLK1 / RCLK1#	L24, L23	I	**Receive Differential Clock Pair 1.** Clock for RCAD 8-15.
RCTL / RCTL#	F24, F25	I	**Receive Differential Control.**
"HyperTransport" Control			
HTRST#	B11	O	**HyperTransport Reset.** Connect to RESET# pin of K8 CPU. 2.5V swing. Active when the RESET# input is active.
LDTSTOP#	A12	I	**HyperTransport Stop.** Connect to South Bridge SLP# pin.

"Transmit" pins should be connected to the K8 CPU "In" pins. "Receive" pins should be connected to the K8 CPU "Out" pins. See the HyperTransport specs and the specs for the K8 CPU models to be supported for additional information.

AGP Bus Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GD[31:0]	(see pin list)	IO	**Address / Data Bus.** Address is driven with GDS assertion for AGP-style transfers and with GFRM# assertion for PCI-style transfers.
GBE[3:0] (GBE[3:0#] for 4x mode)	AC7 AD11 AF11 AD15	IO	**Command / Byte Enable.** (Interpreted as C/BE# for AGP 2x/4x and C#/BE for 8x). For AGP cycles these pins provide command information (different commands than for PCI) driven by the master (graphics controller) when requests are being enqueued using GPIPE# (2x/4x only as GPIPE# isn't used in 8x mode). These pins provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to "0000" during the return of AGP read data. For PCI cycles, commands are driven with GFRM# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
GPAR	AC16	IO	**AGP Parity.** A single parity bit is provided over GD[31:0] and GBE[3:0].
GDBIH / GPIPE# **GDBIL**	AC5 AC4	IO	**Dynamic Bus Inversion High / Low.** AGP 8x transfer mode only. Driven by the source to indicate whether the corresponding data bit group (GDBIH for GD[31:16] and GDBIL for GD[15:0]) needs to be inverted on the receiving end (1 on GDBIx indicates that the corresponding data bit group should be inverted). Used to limit the number of simultaneously switching outputs to 8 for each 16-pin group. **Pipelined Request.** Not used by AGP 8x. Asserted by the master (external graphics controller) to indicate that a full-width request is to be enqueued by the target (North Bridge). The master enqueues one request each rising edge of GCLK while GPIPE# is asserted. When GPIPE# is deasserted no new requests are enqueued across the AD bus. **Note**: See RxAE[1] for GPIPE# / GDBIH pin function selection.
GDS0F (GDS0 for 4x), **GDS0S** (GDS0# for 4x)	AE15 AF15	IO	**Bus Strobe 0.** Source synchronous strobes for GD[15:0] (the agent that is providing the data drives these signals). GDS0 provides timing for 2x data transfer mode; GDS0 and GDS0# provide timing for 4x mode. For 8x transfer mode, GDS0 is interpreted as GDS0F ("First" strobe) and GDS0# as GDS0S ("Second" strobe).
GDS1F (GDS1 for 4x), **GDS1S** (GDS1# for 4x)	AE7 AF7	IO	**Bus Strobe 1.** Source synchronous strobes for GD[31:16] (i.e., the agent that is providing the data drives these signals). GDS1 provides timing for 2x data transfer mode; GDS1 and GDS1# provide timing for 4x transfer mode. For 8x transfer mode, GDS1 is interpreted as GDS1F ("First" strobe) and GDS1# as GDS1S ("Second" strobe).
GFRM (GFRM# for 4x)	AC9	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator. Interpreted as active high for 8x.
GIRDY (GIRDY# for 4x)	AC10	IO	**Initiator Ready.** (Interpreted as active low for PCI/AGP2x/4x and high for AGP 8x). For AGP write cycles, the assertion of this pin indicates that the master is ready to provide *all* write data for the current transaction. Once this pin is asserted, the master is not allowed to insert wait states. For AGP read cycles, the assertion of this pin indicates that the master is ready to transfer a subsequent block of read data. The master is *never* allowed to insert a wait state during the initial block of a read transaction. However, it may insert wait states after each block transfers. For PCI cycles, asserted when the initiator is ready for data transfer.
GTRDY (GTRDY# for 4x)	AC14	IO	**Target Ready.** (Interpreted as active low for PCI/AGP2x/4x and high for AGP 8x). For AGP cycles, indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfer for both read and write transactions. For PCI cycles, asserted when the target is ready for data transfer.
GDSEL (GDSEL# for 4x mode)	AC11	IO	**Device Select (PCI transactions only).** This signal is driven by the North Bridge when a PCI initiator is attempting to access main memory. It is an input when the chip is acting as PCI initiator. Not used for AGP cycles. Interpreted as active high for AGP 8x.

AGP Bus Interface (continued)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GSTOP (GSTOP# for 4x)	AC12	IO	**Stop (PCI transactions only).** Asserted by the target to request the master to stop the current transaction. Interpreted as active high for AGP 8x.
AGP8XDT#	Y2	I	**AGP 8x Transfer Mode Detect.** Low indicates that the external graphics card can support 8x transfer mode. Value is visible in AGP3.0 Status register Rx84[3].
GRBF (GRBF# for 4x)	AD6	I	**Read Buffer Full.** Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When GRBF# is asserted, the North Bridge will not return low priority read data to the graphics controller.
GWBF (GWBF# for 4x)	AC1	I	**Write Buffer Full.**
SBA[7:0]# (SBA[7:0] for 4x)	(see pin list)	I	**Side Band Address.** Provides an additional bus to pass address and command information from the master (graphics controller) to the target (North Bridge). These pins are ignored until enabled.
SBSF (SBS for 4x), **SBSS** (SBS# for 4x)	AF1 AE1	I	**SideBand Strobe.** Driven by the master to provide timing for SBA[7:0]. SBS is used for AGP 2x while SBS and SBS# are used together for AGP 4x. For 8x mode, the strobe mechanism works differently with SBS interpreted as SBSF ("First" strobe) and SBS# as SBSS ("Second" strobe).
ST[2:0]	AB1 AA1 AA2	O	**Status (AGP only).** Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT# is asserted. 000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller). 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously enqueued write command. 011 Indicates that the master is to provide high priority write data for a previously enqueued write command. 100 Reserved. (arbiter must not issue, may be defined in the future). 101 Reserved. (arbiter must not issue, may be defined in the future). 110 Reserved. (arbiter must not issue, may be defined in the future). 111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. The master may enqueue AGP requests by asserting PIPE# or start a PCI transaction by asserting GFRM#. ST[2:0] are always outputs from the target (North Bridge logic) and inputs to the master (graphics controller).
GREQ (GREQ# for 4x)	Y1	I	**Request.** Master (graphics controller) request for use of the AGP bus.
GGNT (GGNT# for 4x)	AA3	O	**Grant.** Permission is given to the master (graphics controller) to use the AGP bus.
GSERR (GSERR# for 4x)	AC15	IO	**AGP System Error.**

Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA-B#.

Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses)

Note: Two mechanisms are provided by the AGP bus to enqueue master requests: GPIPE# (to send addresses multiplexed on the AD lines) and the SBA port (to send addresses unmultiplexed). AGP masters implement one or the other or select one at initialization time (they are not allowed to change during runtime). Only one of the two will be used; the signals associated with the other will not be used. GRBF# has an internal pullup to maintain it in the de-asserted state in case it is not implemented on the master device. AGP 8x mode allows only SBA (GPIPE# isn't used in 8x mode).

Note: AGP 8x signal levels are 0V and 0.8V. AGP 8x mode maintains most signals at a low level when inactive resulting in no current flow.

V-Link Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VAD[7:0]	(see pin list)	IO	**Address / Data Bus.** Also used to pass strap information from the South Bridge to the North Bridge (the physical strap is not on the North Bridge VAD pin but is on the indicated pin of the South Bridge with the information passed over to the North Bridge at reset time).
VPAR	AF19	IO	**Parity.**
VBE#	AE21	IO	**Byte Enable.**
UPCMD	AF26	I	**Command from Client (South Bridge) to Host (North Bridge).**
UPSTB	AE23	I	**Strobe from Client to Host.**
UPSTB#	AF23	I	**Complement Strobe from Client to Host.**
DNCMD	AD23	O	**Command from Host (North Bridge) to Client (South Bridge).**
DNSTB	AF22	O	**Strobe from Host to Client.**
DNSTB#	AD22	O	**Complement Strobe from Host to Client.**

Clock, Reset, Power Control and Test			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GCLK	A11	I	**AGP Clock.** 66 MHz clock for AGP logic.
RESET#	AD25	I	**Reset.** Input from the South Bridge chip. 3.3V tolerant input. When asserted, this signal resets the chip and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options In addition, HTRST# is driven active to reset the K8 CPU.
PWROK	AE26	I	**Power OK.** Driven by South Bridge PWROK output from the power supply PWRGOOD input to the South Bridge.
SUSST#	AD26	I	**Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pull-up to disable.
TESTIN	AC26	I	**Test In.** This pin is used for testing and must be left unconnected or tied high (4.7K Ω to 2.5V) on all board designs.
DEBUG	AC17		**Debug.**
NC	(see pin list)		**No Connect.** Reserved for graphics functions in pin-compatible "K8M800" chipset North Bridge.

Reference Voltages			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VLVREF	AF21	P	**V-Link Voltage Reference.** 0.625V ±2% derived using a resistive voltage divider (3K Ω to 2.5V and 1K Ω to ground). See Design Guide for details.
AGPVREF	AC6, AC13	P	**AGP Voltage Reference.** 0.5 VCCQQ (0.75V) for AGP 2.0 (4x transfer mode) and 0.23 VCCQQ (0.35V) for AGP 3.0 (8x transfer mode). See the Design Guide for additional information and circuit implementation details..

Compensation			
Signal Name	**Pin #**	**I/O**	**Signal Description**
RPCOMP	D25	AI	**Host CPU P-Channel Compensation.** Connect 50 Ω 1% resistor to GND.
RNCOMP	D26	AI	**Host CPU N-Channel Compensation.** Connect 50 Ω 1% resistor to VCCHT.
RTCOMP	C26	AI	**Host CPU Compensation.** Connect 100 Ω 1% resistor to VCCHT.
VLPCOMP	AD19	AI	**V-Link P-Channel Compensation.** Connect 360 Ω 1% resistor to ground.
AGPNCOMP	W1	AI	**AGP N-Channel Compensation.** Connect 60.4 Ω 1% resistor to VCCAGP.
AGPPCOMP	V1	AI	**AGP P-Channel Compensation.** Connect 60.4 Ω 1% resistor to GND.

Analog Power / Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VCCATX	C22	P	**Analog Power for HT Transmit.** 3.3V ±5%. Connect through a ferrite bead for isolation of digital switching noise.
GNDATX	C21	P	**Analog Ground for HT Transmit.** Connect to main ground plane through a ferrite bead for isolation of digital switching noise.
VCCARX	E25	P	**Analog Power for HT Receive.** 2.5V ±5%. Connect through a ferrite bead for isolation of digital switching noise.
GNDARX	E26	P	**Analog Ground for HT Receive.** Connect to main ground plane through a ferrite bead for isolation of digital switching noise.

Digital Power / Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VCCHT	(see pin lists)	P	**Power** for **HyperTransport I/O Interface Logic.** Voltage is HT Interface dependent (typically 1.2V).
VCCVL	(see pin lists)	P	**Power** for **V-Link I/O Interface Logic.** 2.5V ±5%
VCCAGP	(see pin lists)	P	**Power** for **AGP Bus I/O Interface Logic.** 1.5V ±5%
VCCQQ	U1	P	**AGP Quiet Power.** 1.5V ±5%. Connect to VCCAGP (see Design Guide)
GNDQQ	T1	P	**AGP Quiet Ground.** Connect to main ground plane.
VCCSUS	AC25	P	**Suspend Power.** 2.5V ±5%. Used to sustain the on-chip 256-byte SRAM.
VCC	(see pin lists)	P	**Power** for **All Other Internal Logic.** 2.5V ±5%
GND	(see pin lists)	P	**Digital Ground.** Connect to main ground plane.

Strap Pin Descriptions

Strap Pins (External pullup / pulldown straps are required to select "H" / "L")				
Signal	**Actual Strap Pin**	**Function**	**Description**	**Status Bit**
VAD7	**VT8235-CD:** SDCS3# **VT8235-CE:** SDCS3# **VT8237:** PDCS3#	Test Mode	L: Disable H: Enable Pull down for normal operation. VAD7 is sampled during system initialization; The actual strapping pin is located on the South Bridge chip.	-
VAD6	**VT8235-CD:** SDA2 **VT8235-CE:** SDA2 **VT8237:** PDA2	Auto-Configure	L: Disable H: Enable VAD6 is sampled during system initialization; The actual strapping pin is located on the South Bridge chip.	**Rx51[7]**
VAD5	**VT8235-CD:** SDA1 **VT8235-CE:** SDA1 **VT8237:** PDA1	External Loop Test Mode	L: Disable H: Enable Pull down for normal operation. VAD5 is sampled during system initialization; The actual strapping pin is located on the South Bridge chip.	-
VAD4	**VT8235-CD:** SDA0 **VT8235-CE:** SDA0 **VT8237:** PDA0	-reserved-	-	-
VAD3	**VT8235-CD:** SA19 **VT8235-CE:** Strap_VAD3 **VT8237:** GPIOD	Fast Command	Check Design Guide for details.	**Rx53[7]**
VAD2	**VT8235-CD:** SA18 **VT8235-CE:** Strap_VAD2 **VT8237:** GPIOB	Initial HT Bus Width	L: 8-bit Pull down for normal operation. VAD2 is sampled during system initialization; The actual strapping pin is located on the South Bridge chip.	-
VAD[1:0]	**VT8235-CD:** SA[17:16] **VT8235-CE:** Strap_VAD[1:0] **VT8237:** GPIOA, GPIOC	Initial HT Bus Frequency	LL: 200MHz Pull down for normal operation. VAD[1:0] are sampled during system initialization; The actual strapping pin is located on the South Bridge chip.	-

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO), RWC (or just WC) (Read / Write 1's to Clear individual bits) and W1 (Write Once then Read / Only after that). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions following these tables for details). All offset and default values are shown in hexadecimal unless otherwise indicated.

The graphics registers are described in a separate document.

Table 4. Registers

I/O Ports

Port #	I/O Port	Default	Acc
22	PCI / AGP Arbiter Disable	00	RW
CFB-8	Configuration Address	0000 0000	RW
CFF-C	Configuration Data	0000 0000	RW

Device 0 Registers - Host Bridge

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**3188**	RO
5-4	Command	**0006**	**RW**
7-6	Status	**0210**	**WC**
8	Revision ID	**0n**	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	**06**	RO
C	-reserved-	00	—
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
13-10	Graphics Aperture Base	**0000 0008**	**RW**
14-2B	-reserved-	00	—
2D-2C	Subsystem Vendor ID	0000	**W1**
2F-2E	Subsystem ID	0000	**W1**
30-33	-reserved-	00	—
34	Capability Pointer **AGP 2.0:**	**A0**	RO
	(CAPPTR) **AGP 3.0:**	**80**	RO
35-3F	-reserved-	00	—

Device-Specific Registers

Offset	V-Link Control	Default	Acc
40	V-Link Revision ID	00	**RO**
41	V-Link NB Capability	**19**	**WC**
42	V-Link NB Downlink Command	**88**	RW
43	V-Link NB Uplink Max Req Depth	**80**	RW
44	V-Link NB Uplink Buffer Size	**82**	**RO**
45	V-Link NB Bus Timer	**44**	RW
46	V-Link NB Misc Control	00	RW
47	V-Link Control	00	RW
48	V-Link NB/SB Configuration	**18**	RW
49	V-Link SB Capability	**19**	**WC**
4A	V-Link SB Downlink Status	**88**	**RO**
4B	V-Link SB Uplink Max Req Depth	**80**	RW
4C	V-Link SB Uplink Buffer Size	**82**	RW
4D	V-Link SB Bus Timer	**44**	RW
4E	CCA Master High Priority	00	RW
4F	V-Link SB Miscellaneous Control	00	RW

Device-Specific Registers (continued)

Offset	HyperTransport Host Control	Default	Acc
50	HT Host Control 1	00	RW
51	HT Host Control 2	00	RW
52	256-Byte SRAM Base Address	00	RW
53	HT Initialization 1	00	RW
54	HT Initialization 2	00	RW
55	Arbitration Control 1	**08**	RW
56	Arbitration Control 2	00	RW
57	System Memory Ending Address	**01**	RW

Offset	Interrupt Control & Configuration	Default	Acc
58	Capability ID	**08**	**RO**
59	Next Pointer	**68**	**RO**
5A	Interrupt Register Index	00	RW
5B	Capability Type	**80**	**RO**
5F-5C	Interrupt Register Data	0000 0000	**RO**

Offset	HyperTransport Arbitration Ctrl	Default	Acc
60	HT Arbitration Control	00	RW

Offset	BIOS ROM Control	Default	Acc
61	C-ROM Shadow Control	00	RW
62	D-ROM Shadow Control	00	RW
63	E/F-ROM Shadow, Mem Hole, SMI	00	RW

Offset	HyperTransport Buffer Control	Default	Acc
64	HT Buffer / FIFO Control 1	00	RW
65	HT Buffer / FIFO Control 2	00	RW
66	HT Buffer / FIFO Control 3	00	RW
67	HT Buffer / FIFO Control 4	00	RW

Offset	Extended Power Management Ctrl	Default	Acc
68	Power Management Capability	**01**	**RO**
69	Power Management Next Pointer	00	**RO**
6A	Power Management Capabilities I	**02**	**RO**
6B	Power Management Capabilities II	00	**RO**
6C	Power Management Control/Status	00	RW
6D	Power Management Status	00	**RO**
6E	PCI-to-PCI Bridge Support Extension	00	**RO**
6F	Power Management Data	00	**RO**

Offset	PCI Bus Control	Default	Acc
70	PCI Buffer Control	00	RW
71	CPU to PCI Flow Control	**48**	**WC**
72	-reserved-	00	—
73	PCI Master Control	00	RW
74	-reserved-	00	—
75	PCI Arbitration 1	00	RW
76	PCI Arbitration 2	00	RW
77-7F	-reserved-	00	—

Device 0 Device-Specific Registers (continued)

Offset	AGP 2.0 Control (RxFD[1]=1)	Default	Acc
83-80	AGP 2.0 GART/TLB Control	0000 0000	RW
84	AGP 2.0 Graphics Aperture Size	00	RW
85	AGP Buffer / Packet Control	**01**	RW
86	PCI Master R/W Merge Timers	**4F**	RW
87	-reserved-	00	—
8B-88	AGP 2.0 GART Table Base	0000 0000	RW
8C-9F	-reserved-	00	—
A3-A0	AGP 2.0 Capabilities	**0020 C002**	**RO**
A7-A4	AGP 2.0 Status	**1F00 0201**	**RO**
AB-A8	AGP 2.0 Command	0000 0000	RW

Registers A0-AB in the AGP 2.0 register group in the table above are actually offsets from CAPPTR (Rx34) which (with Rx34 = A0h for AGP 2.0) result in the offsets listed above.

Offset	AGP 3.0 Control (RxFD[1]=0)	Default	Acc
83-80	AGP 3.0 Capabilities	**0033 C002**	**RO**
87-84	AGP 3.0 Status	**1F00 0A03**	**RO**
8B-88	AGP 3.0 Command	**1F00 0000**	RW
8F-8C	AGP 3.0 Isochronous Status	0000 0000	—
93-90	AGP 3.0 GART / TLB Control	0000 0000	RW
97-94	AGP 3.0 Graphics Aperture Size	**0001 0F00**	RW
9B-98	AGP 3.0 GART Table Base Low	0000 0000	RW
9F-9C	AGP 3.0 GART Table Base High	0000 0000	RW
A0-AB	-reserved-	00	—

Registers 80-AB in the AGP 3.0 register group in the table above are actually offsets from CAPPTR (Rx34) which (with Rx34 = 80h for AGP 3.0) result in the offsets listed above.

Offset	AGP 2.0 / 3.0 Control	Default	Acc
AC	AGP Control	00	RW
AD	AGP Latency Timer	**02**	RW
AE	AGP Miscellaneous Control	00	RW
AF	AGP 3.0 Control	00	RW
B0	AGP Pad Control / Status	**8x**	RW
B1	AGP Drive Strength	**63**	RW
B2	AGP Pad Drive / Delay Control	**08**	RW
B3	AGP Strobe Output Drive Control	00	RW

Offset	V-Link Compenation / Drive Ctrl	Default	Acc
B4	V-Link NB Compensation Control	00	RW
B5	V-Link NB Strobe Drive Control	00	RW
B6	V-Link NB Data Drive Control	00	RW
B7	-reserved-	00	—
B8	V-Link SB Compensation Control	00	RW
B9	V-Link SB Strobe Drive Control	00	RW
BA	V-Link SB Data Drive Control	00	RW
BB	-reserved-	00	—

Device 0 Device-Specific Registers (continued)

Offset	Power Management Control	Default	Acc
BC	Power Management Mode	00	RW
BD	-reserved-	00	—
BE	Dynamic Clock Stop	00	RW
BF	-reserved-	00	—

Offset	HyperTransport Control	Default	Acc
C3-C0	Link Command	**0060 5808**	RW
C7-C4	Link Configuration & Control	**xx11 0020**	RW
CB-C8	Link End	**0000 00D0**	**RO**
CF-CC	Link Frequency Capability	**0035 0022**	RW
D3-D0	-reserved-	0000 0000	—
D7-D4	Link Enumeration Scratchpad	0000 0000	RW

Offset	HyperTransport I/O	Default	Acc
D8	Transmit Data Rise / Fall Delay	00	RW
D9	Transmit Clock Rise / Fall Delay	00	RW
DA	Transmit Data Drive Control	00	RW
DB	Transmit Clock Drive Control	00	RW
DC	Transmit Autocomp Result	00	RW
DD	Receive Data / Clock Rise/Fall Delay	00	RW
DE	Receive Terminator Value	**22**	RW
DF	Receive Terminator Autocomp Status	00	RW

Offset	UMA Control (reserved)	Default	Acc
E0-E3	-reserved-	00	—

Offset	DRAM Above 4G Control	Default	Acc
E4	Low Top Address Low	00	RW
E5	Low Top Address High	**FF**	RW
E6	SMM / APIC Decoding	**01**	RW
E7	-reserved-	00	—

Offset	AGP / V-Link Control	Default	Acc
E8	AGP Output Delay	00	RW
E9	AGP / V-Link Receive Strobe Delay	00	RW
EA	V-Link Output Delay	00	RW
EB	AGP SBA Termination Control	00	RW
EC	AGP Isochronous Control 1	00	RW
ED	AGP Isochronous Control 2	00	RW
EE	AGP Master Isoch Read Timer	00	RW
EF	AGP Master Isoch Write Timer	00	RW

Offset	Test, BIOS Scratch, Miscellaneous	Default	Acc
F0-F2	Reserved (Do Not Program)	00	RW
F3-F4	BIOS Scratch Registers	00	RW
F5-FC	Reserved (Do Not Program)	00	RW
FD	AGP 2.0 / 3.0 Select	00	RW
FE-FF	Reserved (Do Not Program)	00	RW

Device 1 Registers - PCI-to-PCI Bridge

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**B188**	RO
5-4	Command	**0007**	**RW**
7-6	Status	**0230**	**WC**
8	Revision ID	**nn**	RO
9	Program Interface	00	RO
A	Sub Class Code	**04**	RO
B	Base Class Code	**06**	RO
C	-reserved-	00	—
D	Latency Timer	00	RO
E	Header Type	**01**	RO
F	-reserved- (Built In Self Test)	00	—
10-17	-reserved-	00	—
18	Primary Bus Number	00	**RW**
19	Secondary Bus Number	00	**RW**
1A	Subordinate Bus Number	00	**RW**
1B	Secondary Latency Timer	00	RO
1C	I/O Base	**F0**	**RW**
1D	I/O Limit	00	**RW**
1F-1E	Secondary Status	0000	RO
21-20	Memory Base	**FFF0**	**RW**
23-22	Memory Limit (Inclusive)	0000	**RW**
25-24	Prefetchable Memory Base	**FFF0**	**RW**
27-26	Prefetchable Memory Limit	0000	**RW**
28-33	-reserved-	00	—
34	Capability Pointer	**80**	RO
35-3D	-reserved-	00	—
3F-3E	PCI-to-PCI Bridge Control	00	**RW**

Device-Specific Registers

Offset	AGP Bus Control	Default	Acc
40	CPU-to-AGP Flow Control 1	00	RW
41	CPU-to-AGP Flow Control 2	**08**	RW
42	AGP Master Control	00	RW
43	AGP Master Latency Timer	**22**	RW
44	Reserved (Do Not Program)	00	RW
45	Fast Write Control	**72**	RW
47-46	PCI-to-PCI Bridge Device ID	0000	RW
48	AGP / PCI2 Error Reporting	00	**WC**
49-7F	-reserved-	00	—

Offset	Power Management	Default	Acc
80	Capability ID	**01**	**RO**
81	Next Pointer	00	**RO**
82	Power Management Capabilities 1	**02**	**RO**
83	Power Management Capabilities 2	00	**RO**
84	Power Management Control / Status	00	RW
85	Power Management Status	00	**RO**
86	PCI-PCI Bridge Support Extensions	00	**RO**
87	Power Management Data	00	**RO**
88-FF	-reserved-	00	—

Miscellaneous I/O

One I/O port is defined (Port 22).

Port 22 – PCI / AGP Arbiter Disable ..... RW

7-2 Reserved ..... always reads 0

1 AGP Arbiter Disable
- 0 Respond to GREQ# signal .....default
- 1 Do not respond to GREQ# signal

0 PCI Arbiter Disable
- 0 Respond to all REQ# signals.....default
- 1 Do not respond to any REQ# signals, including PREQ#

This port can be enabled for read/write access by setting bit-7 of Device 0 Configuration Register 76.

Configuration Space I/O

All on-chip registers (listed above) are addressed via the following configuration mechanism:

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

Port CFB-CF8 - Configuration Address..... RW

31 Configuration Space Enable
- 0 Disabled..... default
- 1 Convert configuration data port writes to configuration cycles on the PCI bus

30-24 Reserved .....always reads 0

23-16 PCI Bus Number
Used to choose a specific PCI bus in the system

15-11 Device Number
Used to choose a specific device in the system (devices 0 and 1 are defined)

10-8 Function Number
Used to choose a specific function if the selected device supports multiple functions (only function 0 is defined).

7-2 Register Number (also called the "Offset")
Used to select a specific DWORD in the configuration space

1-0 Fixed .....always reads 0

Port CFF-CFC - Configuration Data..... RW

Refer to PCI Bus Specification Version 2.2 for further details on operation of the above configuration registers.

Device 0 Register Descriptions

Device 0 Host Bridge Header Registers

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number, function number and device number equal to zero.

Device 0 Offset 1-0 - Vendor ID (1106h) ..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 0 Offset 3-2 - Device ID (3188h) ..... RO

15-0 ID Code ..... reads 3188h to identify the K8T800

Device 0 Offset 5-4 –Command (0006h) ..... RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent ..... default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable ..... RO
- 0 SERR# driver disabled ..... default
- 1 SERR# driver enabled

(SERR# is used to report ECC errors).

7 Address / Data Stepping ..... RO
- 0 Device never does stepping ..... default
- 1 Device always does stepping

6 Parity Error Response ..... RW
- 0 Ignore parity errors & continue ..... default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop ..... RO
- 0 Treat palette accesses normally ..... default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command ..... RO
- 0 Bus masters must use Mem Write ..... default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring ..... RO
- 0 Does not monitor special cycles ..... default
- 1 Monitors special cycles

2 PCI Bus Master ..... RO
- 0 Never behaves as a bus master
- 1 Can behave as a bus master ..... default

1 Memory Space ..... RO
- 0 Does not respond to memory space
- 1 Responds to memory space ..... default

0 I/O Space ..... RO
- 0 Does not respond to I/O space ..... default
- 1 Responds to I/O space

Device 0 Offset 7-6 – Status (0210h) ..... RWC

15 Detected Parity Error
- 0 No parity error detected ..... default
- 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6). ..... write one to clear

14 Signaled System Error (SERR# Asserted) ..... always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master ..... write one to clear

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target ..... write one to clear

11 Signaled Target Abort ..... always reads 0
- 0 Target Abort never signaled

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium ..... always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected
- 0 No data parity error detected ..... default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and this chip was initiator of the operation in which the error occurred..... write one to clear

7 Fast Back-to-Back Capable ..... always reads 0

6 User Definable Features ..... always reads 0

5 66MHz Capable ..... always reads 0

4 Supports New Capability list ..... always reads 1

3-0 Reserved ..... always reads 0

Device 0 Offset 8 - Revision ID (0nh) ..... RO

7-0 Chip Revision Code ..... always reads 0nh

Device 0 Offset 9 - Programming Interface (00h) ..... RO

7-0 Interface Identifier ..... always reads 00h

Device 0 Offset A - Sub Class Code (00h) ..... RO

7-0 Sub Class Code ..... reads 00 to indicate Host Bridge

Device 0 Offset B - Base Class Code (06h) ..... RO

7-0 Base Class Code .. reads 06 to indicate Bridge Device

Device 0 Offset D - Latency Timer (00h) ..... RW

Specifies the latency timer value in PCI bus clocks.

7-3 Guaranteed Time Slice for CPU ..... default=0

2-0 Reserved (fixed granularity of 8 clks) .. always read 0

These bits are writeable but read 0 for PCI specification compatibility. The programmed value may be read back in Rx75[6-4] (PCI Arbitration 1).

Device 0 Host Bridge Header Registers (continued)

Device 0 Offset E - Header Type (00h).....RO

7-0 Header Type Code ..... reads 00: single function

Device 0 Offset F - Built In Self Test (BIST) (00h).....RO

7 BIST Supported .....reads 0: no supported functions

6-0 Reserved ..... always reads 0

Device 0 Offset 13-10 - Graphics Aperture Base (AGP 2.0) (00000008h) .....RW

This register is interpreted per the following definition if RxFD[1]=1 (AGP 2.0 registers enabled).

31-28 Upper Programmable Base Address Bits ..... def=0

27-20 Lower Programmable Base Address Bits ..... def=0

These bits behave as if hardwired to 0 if the corresponding AGP 2.0 Graphics Aperture Size register bit (Device 0 Offset 84h) is 0.

27	26	25	24	23	22	21	20	(Base)
7	6	5	4	3	2	1	0	(Size)
RW	RW	RW	RW	RW	RW	RW	RW	1M
RW	RW	RW	RW	RW	RW	RW	0	2M
RW	RW	RW	RW	RW	RW	0	0	4M
RW	RW	RW	RW	RW	0	0	0	8M
RW	RW	RW	RW	0	0	0	0	16M
RW	RW	RW	0	0	0	0	0	32M
RW	RW	0	0	0	0	0	0	64M
RW	0	0	0	0	0	0	0	128M
0	0	0	0	0	0	0	0	256M

19-4 Reserved ..... always reads 0

3 Prefetchable.....**always reads 1**

Indicates that the locations in the address range defined by this register are prefetchable.

2-1 Type ..... always reads 0

Indicates the address range in the 32-bit address space.

0 Memory Space..... always reads 0

Indicates the address range in the memory address space.

Device 0 Offset 13-10 - Graphics Aperture Base (AGP 3.0) (00000008h) ..... RW

This register is interpreted per the following definition if RxFD[1]=0 (AGP 3.0 registers enabled). This register may only be read if AGP 3.0 register Rx90[8] = 1.

31-22 Programmable Base Address Bits.....def=0

These bits behave as if hardwired to 0 if the corresponding AGP 3.0 Graphics Aperture Size register bit (Device 0 Offset 94h) is 0.

31	30	29	28	-	-	27	26	25	24	23	22	(Base)
11	10	9	8	7	6	5	4	3	2	1	0	(Size)
RW	RW	RW	RW	0	0	RW	RW	RW	RW	RW	RW	4M
RW	RW	RW	RW	0	0	RW	RW	RW	RW	RW	0	8M
RW	RW	RW	RW	0	0	RW	RW	RW	RW	0	0	16M
RW	RW	RW	RW	0	0	RW	RW	RW	0	0	0	32M
RW	RW	RW	RW	0	0	RW	RW	0	0	0	0	64M
RW	RW	RW	RW	0	0	RW	0	0	0	0	0	128M
RW	RW	RW	RW	0	0	0	0	0	0	0	0	256M
RW	RW	RW	0	0	0	0	0	0	0	0	0	512M
RW	RW	0	0	0	0	0	0	0	0	0	0	1G
RW	0	0	0	0	0	0	0	0	0	0	0	2G-max
0	0	0	0	0	0	0	0	0	0	0	0	4G

21-4 Reserved .....always reads 0

3 Prefetchable ..... **always reads 1**

Indicates that the locations in the address range defined by this register are prefetchable.

2-1 Type .....always reads 0

Indicates the address range in the 32-bit address space.

0 Memory Space.....always reads 0

Indicates the address range in the memory address space.

Device 0 Offset 2D-2C – Subsystem Vendor ID..... W1/R

15-0 Subsystem Vendor ID .....default = 0000h

This register may be written once and is then read only.

Device 0 Offset 2F-2E – Subsystem ID W1/R

15-0 Subsystem ID.....default = 0000h

This register may be written once and is then read only.

Device 0 Offset 34 - Capability Pointer (CAPPTR)..... RO

Contains an offset from the start of configuration space.

7-0 AGP Capability List Pointer .....always reads A0h

Device 0 Host Bridge Device-Specific Registers

These registers are normally programmed once at system initialization time.

V-Link Control

Device 0 Offset 40 – V-Link Specification ID (00h).....RO

7-0 Specification Revision..... always reads 00

Device 0 Offset 41 – NB V-Link Capability (19h) .....WC

7 V-Link Parity Error Detected by NB.....WC
- 0 No V-Link Parity Error Detected.....default
- 1 V-Link Parity Error Detected (write 1 to clear)

6 Reserved ..... always reads 0

5 16-bit Bus Width Supported by NB .....RO
- 0 Not Supported.....default
- 1 Supported

4 8-Bit Bus Width Supported by NB.....RO
- 0 Not Supported
- 1 Supported.....**default**

3 4x Rate Supported by NB.....RO
- 0 Not Supported
- 1 Supported.....**default**

2 2x Rate Supported by NB.....RO
- 0 Not Supported.....default
- 1 Supported

1 Reserved ..... always reads 0

0 8x Rate Supported by NB.....RO
- 0 Not Supported
- 1 Supported.....**default**

Device 0 Offset 42 – NB Downlink Command (88h) .....RW

7-4 DnCmd Max Request Depth (0=1 DnCmd).. def = 8

3-0 DnCmd Write Buffer Size (doublewords)..... def = 8

Device 0 Offset 43 – NB Uplink Max Req Depth (80h)...RO

7-4 UpCmd Max Request Depth (0=1 UpCmd).. def = 8
Indicates the maximum allowable number of outstanding UPCMD requests

3-0 Reserved ..... always reads 0

Device 0 Offset 44 – NB Uplink Buffer Size (82h).....RO

7-4 UpCmd P2C Write Buffer Size (max lines).. def = 8

3-0 UpCmd P2P Write Buffer Size (max lines) .. def = 2

Device 0 Offset 45 –NB V-Link Bus Timer (44h)..... RW

7-4 Timer for Normal Priority Requests from SB
- 0000 Immediate
- 0001 1*4 VCLKs
- 0010 2*4 VCLKs
- 0011 3*4 VCLKs
- 0100 4*4 VCLKs..... default
- 0101 5*4 VCLKs
- 0110 6*4 VCLKs
- 0111 7*4 VCLKs
- 1000 8*4 VCLKs
- 1001 16*4 VCLKs
- 1010 32*4 VCLKs
- 1011 64*4 VCLKs
- 11xx Own the bus for as long as there is a request

3-0 Timer for High Priority Requests from SB
- 0000 Immediate
- 0001 1*2 VCLKs
- 0010 2*2 VCLKs
- 0011 3*2 VCLKs
- 0100 4*2 VCLKs..... default
- 0101 5*2 VCLKs
- 0110 6*2 VCLKs
- 0111 7*2 VCLKs
- 1000 8*2 VCLKs
- 1001 16*2 VCLKs
- 1010 32*2 VCLKs
- 1011 64*2 VCLKs
- 11xx Own the bus for as long as there is a request

Device 0 Offset 46 – NB V-Link Misc Control (00h).....RW

7 **Downstream High Priority**
- 0 Disable High Priority Down Commands .....def
- 1 Enable High Priority Down Commands

6 **Downlink Priority**
- 0 Treat Downlink Cycles as Normal Priority .def
- 1 Treat Downlink Cycles as High Priority

5-4 **Combine Multiple STPGNT Cycles Into One V-Link Command**
- 00 Compatible, 1 command per V-Link cmd....def
- 01 2 commands per V-Link command
- 10 3 commands per V-Link command
- 11 4 commands per V-Link command

3-2 **V-Link Master Access Ordering Rules**
- 00 High priority read, pass normal read (not pass write) .....default
- 01 Read (high/normal) pass write (HR>LR>W)
- 1x Read / write in order

1-0 **Reserved** ..... always reads 0

Device 0 Offset 47 – V-Link Control (00h).....RW

7 **Parity Error on SERR# Reported via NMI**
- 0 Disable .....default
- 1 Enable

6 **Parity Error on SERR# Reported to SB via Vlink**
- 0 Disable .....default
- 1 Enable

5-4 **Reserved** ..... always reads 0

3 **Down Strobe Dynamic Stop**
- 0 Disable .....default
- 1 Enable

2 **Auto-Disconnect**
- 0 Disable .....default
- 1 Enable

1 **V-Link Disconnect Sequence for STPGNT cycle**
- 0 Disable .....default
- 1 Enable

0 **V-Link Disconnect Sequence for HALT Cycle**
- 0 Disable .....default
- 1 Enable

Device 0 Offset 48 – NB/SB V-Link Configuration (18h)RW

7 **V-Link Parity Check**
- 0 Disable..... default
- 1 Enable

6 **Rest Bus Width Support**
- 0 Disable..... default
- 1 Enable

5 **16-bit Bus Width**
- 0 Disable..... default
- 1 Enable

4 **8-Bit Bus Width**
- 0 Disable
- 1 Enable..... **default**

3 **4x Rate**
- 0 Disable
- 1 Enable..... **default**

2 **2x Rate**
- 0 Disable..... default
- 1 Enable

1 **Reserved** .....always reads 0

0 **8x Rate**
- 0 Disable..... default
- 1 Enable

Device 0 Offset 49 – SB V-Link Capability (19h) ..... WC

7 **V-Link Parity Error Detected by SB..... WC**
- 0 No parity error detected..... default
- 1 Parity error detected

6 **Reserved** .....always reads 0

5 **16-bit Bus Width Supported by SB..... RO**
- 0 Not Supported..... default
- 1 Supported

4 **8-Bit Bus Width Supported by SB..... RO**
- 0 Not Supported
- 1 Supported ..... **default**

3 **4x Rate Supported by SB..... RO**
- 0 Not Supported
- 1 Supported ..... **default**

2 **2x Rate Supported by SB..... RO**
- 0 Not Supported..... default
- 1 Supported

1 **Reserved** .....always reads 0

0 **8x Rate Supported by SB..... RO**
- 0 Not Supported
- 1 Supported ..... **default**

Device 0 Offset 4A – SB Downlink Status (88h).....RO

7-4 **DnCmd Max Request Depth** (0=1 DnCmd).. def = 8
3-0 **DnCmd Write Buffer Size** (doublewords)..... def = 8

Device 0 Offset 4B – SB Uplink Command (80h).....RW

7-4 **UpCmd Max Request Depth** (0=1 UpCmd).. def = 8
Indicates the maximum allowable number of outstanding UPCMD requests
3-0 **Reserved** ..... always reads 0

Device 0 Offset 4C – SB Uplink Command (82h).....RW

7-4 **UpCmd P2C Write Buffer Size** (max lines).. def = 8
3-0 **UpCmd P2P Write Buffer Size** (max lines).. def = 2

Device 0 Offset 4D – SB V-Link Bus Timer (44h).....RW

7-4 **Timer for Normal Priority Requests from NB**
0000 Immediate
0001 1*4 VCLKs
0010 2*4 VCLKs
0011 3*4 VCLKs
0100 4*4 VCLKs.....default
0101 5*4 VCLKs
0110 6*4 VCLKs
0111 7*4 VCLKs
1000 8*4 VCLKs
1001 16*4 VCLKs
1010 32*4 VCLKs
1011 64*4 VCLKs
11xx Own the bus for as long as there is a request

3-0 **Timer for High Priority Requests from NB**
0000 Immediate
0001 1*2 VCLKs
0010 2*2 VCLKs
0011 3*2 VCLKs
0100 4*2 VCLKs.....default
0101 5*2 VCLKs
0110 6*2 VCLKs
0111 7*2 VCLKs
1000 8*2 VCLKs
1001 16*2 VCLKs
1010 32*2 VCLKs
1011 64*2 VCLKs
11xx Own the bus for as long as there is a request

Device 0 Offset 4E – CCA Master Priority (00h)..... RW

7 **1394 High Priority**
0 Low priority..... default
1 High priority
6 **LAN / NIC High Priority**
0 Low priority..... default
1 High priority
5 **Reserved** .....always reads 0
4 **USB High Priority**
0 Low priority..... default
1 High priority
3 **Reserved** .....always reads 0
2 **IDE High Priority**
0 Low priority..... default
1 High priority
1 **AC97-ISA High Priority**
0 Low priority..... default
1 High priority
0 **PCI High Priority**
0 Low priority..... default
1 High priority

Device 0 Offset 4F – SB V-Link Misc Control (00h)..... RW

7 **Upstream Command High Priority**
0 Disable high priority up commands..... default
1 Enable high priority up commands
6-4 **Reserved** .....always reads 0
3 **Up Strobe Dynamic Stop**
0 Disable..... default
1 Enable
2-1 **Reserved** .....always reads 0
0 **Down Cycle Wait for Up Cycle Write Flush (Except Down Cycle Post Write)**
0 Disable..... default
1 Enable

HyperTransport Host Control

Device 0 Offset 50 - HT Host Control 1 (00h).....RW

7 In-Order Processing CPU-to-PCI / CPU-to-AGP Requests or HyperTransport Ordering Rule
- 0 Disable .....default
- 1 Enable

6 PCI Master Read Ready / PCI Master Write Ready In-Order Response
- 0 Disable .....default
- 1 Enable

5 AGP Master Read Ready / AGP Master Write Ready In-Order Response
- 0 Disable .....default
- 1 Enable

4 AGP Read Outstanding Request Queue Depth
- 0 16-Level .....default
- 1 32-Level

3 EOI Cycle to AGP
- 0 Disable .....default
- 1 Enable

2-0 Number of Outstanding PCI-to-CPU Requests on HyperTransport Bus

Device 0 Offset 51 - HT Host Control 2 (00h) ..... RW

7 ROMSIP Support.....RO from VAD6 Strap
- 0 Disable..... default
- 1 Enable

6 Set Isochronous Request Bit for PCI-to-CPU Requests with PCI MSIO
- 0 Disable..... default
- 1 Enable

5 Set Isochronous Request Bit for AGP-to-CPU Requests with AGP High Priority
- 0 Disable..... default
- 1 Enable

4 Set Isochronous Request Bit for All PCI-to-CPU Requests
- 0 Disable..... default
- 1 Enable

3 Set Isochronous Request Bit for All AGP-to-CPU Requests
- 0 Disable..... default
- 1 Enable

2 Non-Posted CPU-to-PCI Response from PCI Will Wait For Previous PCI-to-CPU Write PCI Write Flush
- 0 Disable..... default
- 1 Enable

1 Non-Posted CPU-to-AGP Response from AGP Will Wait For Previous AGP-to-CPU AGP Write Flush
- 0 Disable..... default
- 1 Enable

0 256-Byte SRAM Access
- 0 Disable..... default
- 1 Enable

Device 0 Offset 52 - SRAM Base Address (00h)..... RW

7-0 256-Byte SRAM Base Address ..... default = 00h

Device 0 Offset 53 - HT Initialization 1 (00h) ..... RW

7 **CPU Fast Command ..... RO**
- 0 Disable ..... **default set per VAD3 strap info**
- 1 Enable

6-4 **HT 400 Init Counter .. default per ROMSIP[57:55]**

3 **AGP Isochronous Read Outstanding Request Queue Depth**
- 0 16-Level ..... default
- 1 32-Level

2-0 **HT 200 Init Counter .. default per ROMSIP[54:52]**

Device 0 Offset 54 - HT Initialization 2 (00h) ..... RW

7 **Set / Clear Isoc Bit For Isoc AGP Request**
- 0 Clear ..... default
- 1 Set

6-4 **HT 800 Init Counter**.....default per ROMSIP[63:61]

3 **Reserved** .....always reads 0

2-0 **HT 600 Init Counter**.....default per ROMSIP[60:58]

Device 0 Offset 55 - Arbitration Control 1 (08h)..... RW

7 **AGP Read Length Can Be 1QW or 8QW (Not 1 / 2 / 4 / 8QW) for AGP Performance**
- 0 Disable .....default
- 1 Enable

6 **AGP Byte Enable Write Type**
- 0 Issue Byte writes for all BE writes.....default
- 1 Issue DW writes for all BE writes

5 **When PCI-to-CPU Write Cycles With All Byte Enables Set, HyperTransport Controller May:**
- 0 Issue Byte Write.....default
- 1 Issue DoubleWord Write

4 **AGP Read 8QW Access from HT**
- 0 Disable .....default
- 1 Enable

3 **Allow CPU CF8 / CFC I/O Cycle**
- 0 Disable (Don't Allow)
- 1 Enable (Allow).....default

2 **PCI Master Access Could Be Bursting**
- 0 Only 1 request before data phase .....default
- 1 Could have 4 request pipeline before data phase

1 **Reduce 1T Latency for AGP Access**
- 0 Disable .....default
- 1 Enable

0 **LDTSTOP# Connection Sequence Change**
- 0 100 usec for PLL lock timer.....default
- 1 1 usec for PLL lock timer

Device 0 Offset 56 - Arbitration Control 2 (00h) ..... RW

7 **Clear CPU-to-PCI Read Response PassPW Bit**
- 0 Disable..... default
- 1 Enable

6 **Set CPU-to-PCI Target Done PassPW Bit**
- 0 Disable..... default
- 1 Enable

5 **Clear CPU-to-PCI Target Done PassPW Bit**
- 0 Disable..... default
- 1 Enable

4 **Legacy NMI Encoding for MT[3]**
- 0 Disable..... default
- 1 Enable

3 **Legacy External Interrupt Encoding for MT[3]**
- 0 Disable..... default
- 1 Enable

2 **Reduce 1T Latency for FW Cycle**
- 0 Disable..... default
- 1 Enable

1 **K8 CRC Error Checking..... W1R†**
- 0 Disable..... default
- 1 Enable

0 **AGP Over 4G Error Checking ..... W1R†**
- 0 Disable..... default
- 1 Enable

† "W1R" indicates "write once, then read only"

Device 0 Offset 57 – System Memory Ending Address (01h)..... RW

6 **System Memory Ending Address (HA[31:24]) ..... default = 01h**

HyperTransport Arbitration Control

Device 0 Offset 60 - HT Arbitration Control (00h) ..... RW

7 PCI Master (PCI1 & PCI2) Requests Can Pass Other Writes If The CPU Write Channel Is Full
- 0 Disable ..... default
- 1 Enable

6 AGP Non-Isoc Requests Can Pass Other Writes If The CPU Write Channel Is Full
- 0 Disable ..... default
- 1 Enable

5 Extend Arbitration Based on PCI Master Request
- 0 Disable ..... default
- 1 Enable

4 Extend Arbitration Based on AGP Non-Isoc Req
- 0 Disable ..... default
- 1 Enable

3 Extend Arbitration Based on AGP Isoc Request
- 0 Disable ..... default
- 1 Enable

2 PCI Master Request Can Be High Priority in Upstream Arbitration
- 0 Disable ..... default
- 1 Enable

1 AGP Non-Isoc Request Can Be High Priority in Upstream Arbitration
- 0 Disable ..... default
- 1 Enable

0 AGP Isoc Request Can Be High Priority in Upstream Arbitration
- 0 Disable ..... default
- 1 Enable

Interrupt Control & Configuration

Device 0 Offset 58 - Capability ID (08h) ..... RO

Device 0 Offset 59 - Next Pointer (68h) ..... RO

Device 0 Offset 5A - Interrupt Register Index (00h) ..... RW

Device 0 Offset 5B - Capability Type (80h) ..... RO

Device 0 Offset 5F-5C - Interrupt Register Data ..... RO

31-24 ..... Always reads 0F8h
23-16 Vector
15-8 Destination
7 Reserved ..... always reads 0
6 Destination Mode
5 Trigger Mode
4-2 MT
1 Interrupt Polarity
0 Interrupt Mask

BIOS ROM & Memory Hole Control

Device 0 Offset 61 - Shadow RAM Control 1 (00h)..... RW

7-6 CC000h-CFFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 C8000h-CBFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 C4000h-C7FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 C0000h-C3FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Device 0 Offset 62 - Shadow RAM Control 2 (00h)..... RW

7-6 DC000h-DFFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 D8000h-DBFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 D4000h-D7FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 D0000h-D3FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Device 0 Offset 63 - Shadow RAM Control 3 (00h)..... RW

7-6 E0000h-EFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 F0000h-FFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 Memory Hole
- 00 None ..... default
- 01 512K-640K
- 10 15M-16M (1M)
- 11 14M-16M (2M)

1 Disable A,BK SMRAM Direct Access

0 Enable A,BK DRAM Access

SMI Mapping Control:

Bits	SMM		Non-SMM	
1-0	Code	Data	Code	Data
00	DRAM	DRAM	PCI	PCI
01	DRAM	DRAM	DRAM	DRAM
10	DRAM	PCI	PCI	PCI
11	DRAM	DRAM	DRAM	DRAM

HyperTransport Buffer / FIFO Control

Device 0 Offset 64 – HT Buffer Control 1 (00h) ..... RW

7-4 **AGP Master Isochronous Request Timer**.... def=0h
(programmed in units of 16 HT clocks)

3-2 **HT Parking Arbitration for PCI / AGP / Isoch AGP Requests**
- 00 Park at Previous Bus .....default
- 01 Park at PCI Master
- 10 Park at AGP Master
- 11 Park at AGP Isoch Request

1 **MG FIFO Data Depth**
- 0 64 QW.....default
- 1 128 QW

0 **FW Data Depth**
- 0 16 QW .....default
- 1 32 QW

Device 0 Offset 65 – HT Buffer Control 2 (00h) ..... RW

7-4 **PCI Master Timer**..... default = 0h
(programmed in units of 16 HT clocks)

3-0 **PCI Master Promotion Timer**..... default = 0h
(programmed in units of 16 HT clocks)

Device 0 Offset 66 – HT Buffer Control 3 (00h) ..... RW

7-4 **AGP Master Timer** ..... default = 0h
(programmed in units of 16 HT clocks)

3-0 **AGP Master Promotion Timer**..... default = 0h
(programmed in units of 16 HT clocks)

Device 0 Offset 67 – HT Buffer Control 4 (00h) ..... RW

7-0 **AGP Master Isoch Request Timer** ..... default = 00h
(programmed in units of 16 HT clocks)

Extended Power Management Control

Device 0 Offset 68 – Power Management Capability ID RO

7-0 **Capability ID** .....always reads 01h

Device 0 Offset 69 – Power Management Next Pointer.. RO

7-0 **Next Pointer**..... always reads 00h ("Null" Pointer)

Device 0 Offset 6A – Power Mgmt Capabilities I ..... RO

7-0 **Power Management Capabilities** ..always reads 02h

Device 0 Offset 6B – Power Mgmt Capabilities II ..... RO

7-0 **Power Management Capabilities** ..always reads 00h

Device 0 Offset 6C – Power Mgmt Control / Status ..... RW

7-2 **Reserved** .....always reads 0

1-0 **Power State**
- 00 D0 ..... default
- 01 -reserved-
- 10 -reserved-
- 11 D3 Hot

Device 0 Offset 6D – Power Management Status..... RO

7-0 **Power Management Status**.....always reads 00h

Device 0 Offset 6E – PCI-to-PCI Bridge Support Ext.... RO

7-0 **P2P Bridge Support Extensions**....always reads 00h

Device 0 Offset 6F – Power Management Data..... RO

7-0 **Power Management Data** .....always reads 00h

PCI Bus Control

These registers are normally programmed once at system initialization time.

Device 0 Offset 70 - PCI Buffer Control (00h)..... RW

- **7 CPU to PCI Post-Write**
  - 0 Disable .....default
  - 1 Enable
- **6 Reserved** ..... always reads 0
- **5-4 PCI Master to DRAM Prefetch**
  - 00 Always prefetch .....default
  - x1 Never prefetch
  - 10 Prefetch only for Enhance command
- **3 Reserved** ..... always reads 0
- **2 PCI Master Read Buffering**
  - 0 Disable .....default
  - 1 Enable
- **1 Delay Transaction**
  - 0 Disable .....default
  - 1 Enable
- **0 Reserved** ..... always reads 0

Device 0 Offset 71 - CPU to PCI Flow Control (48h).. RWC

- **7 Retry Status..... RWC**
  - 0 No retry occurred .....default
  - 1 Retry occurred
- **6 Retry Timeout Action**
  - 0 Retry forever (record status only)
  - 1 Flush buffer or return FFFFFFFFh for reads .....default
- **5-4 Retry Count and Retry Backoff**
  - 00 Retry 2 times, backoff CPU .....default
  - 01 Retry 16 times
  - 10 Retry 4 times
  - 11 Retry 64 times
- **3 PCI Burst**
  - 0 Disable
  - 1 Enable .....default
- **2 Reserved** ..... always reads 0
- **1 Compatible Type#1 Configuration Cycles**
  - 0 Disable (fixed AD31).....default
  - 1 Enable
- **0 IDSEL Control**
  - 0 AD11, AD12 .....default
  - 1 AD30, AD31

Device 0 Offset 73 - PCI Master Control (00h)..... RW

- **7 Reserved** .....always reads 0
- **6 PCI Master 1-Wait-State Write**
  - 0 Zero wait state TRDY# response..... default
  - 1 One wait state TRDY# response
- **5 PCI Master 1-Wait-State Read**
  - 0 Zero wait state TRDY# response..... default
  - 1 One wait state TRDY# response
- **4 WSC#**
  - 0 Disable..... default
  - 1 Enable
- **3-1 Reserved** .....always reads 0
- **0 PCI Master Broken Timer Enable**
  - 0 Disable..... default
  - 1 Enable. Force into arbitration when there is no FRAME# 16 PCICLK's after the grant.

Device 0 Offset 75 - PCI Arbitration 1 (00h) ..... RW

7 **Arbitration Mode**
- 0 REQ-based (arbitrate at end of REQ#) ..default
- 1 Frame-based (arbitrate at FRAME# assertion)

6-4 **Latency Timer**..... read only, reads Rx0D bits 2:0

3 **Reserved** ..... always reads 0

2-0 **PCI Master Bus Time-Out**
(force into arbitration after a period of time)
- 000 Disable .....default
- 001 1x16 PCICLKs
- 010 2x16 PCICLKs
- 011 3x16 PCICLKs
- 100 4x16 PCICLKs
- ... ...
- 111 7x16 PCICLKs

Device 0 Offset 76 - PCI Arbitration 2 (00h)..... RW

7 **I/O Port 22 Access**
- 0 CPU access to I/O address 22h is passed on to the PCI bus ..... default
- 1 CPU access to I/O address 22h is processed internally

6 **Reserved** .....always reads 0

5-4 **Master Priority Rotation Control**
- 00 Disable..... default
- 01 Grant to CPU after every PCI master grant
- 10 Grant to CPU after every 2 PCI master grants
- 11 Grant to CPU after every 3 PCI master grants

Setting 01: the CPU will always be granted access after the current bus master completes, no matter how many PCI masters are requesting.

Setting 10: if other PCI masters are requesting during the current PCI master grant, the highest priority master will get the bus after the current master completes, but the CPU will be guaranteed to get the bus after that master completes.

Setting 11: if other PCI masters are requesting, the highest priority will get the bus next, then the next highest priority will get the bus, then the CPU will get the bus.

In other words, with the above settings, even if multiple PCI masters are continuously requesting the bus, the CPU is guaranteed to get access after every master grant (01), after every other master grant (10) or after every third master grant (11).

3-2 **Select REQn# to REQ4# mapping**
- 00 REQ4#..... default
- 01 REQ0#
- 10 REQ1#
- 11 REQ2#

1 **Reserved** .....always reads 0

0 **REQ4# is High Priority Master**
- 0 Disable..... default
- 1 Enable

GART / Graphics Aperture

The function of the Graphics Address Relocation Table (GART) is to translate virtual 32-bit addresses issued by an AGP device into 4K-page based physical addresses for system memory access. In this translation, the upper 20 bits (A31-A12) are remapped, while the lower 12 address bits (A11-A0) are used unchanged.

A one-level fully associative lookup scheme is used to implement the address translation. In this scheme, the upper 20 bits of the virtual address are used to point to an entry in a page table located in system memory. Each page table entry contains the upper 20 bits of a physical address (a "physical page" address). For simplicity, each page table entry is 4 bytes. The total size of the page table depends on the GART range (called the "aperture size") which is programmable in the K8T800.

This scheme is shown in the figure below.

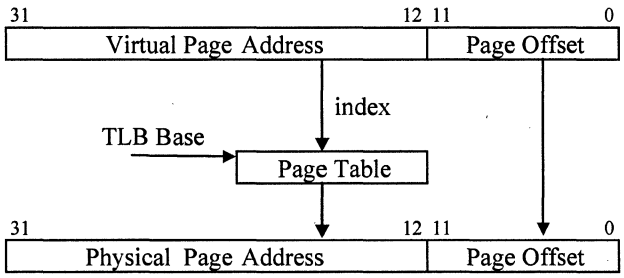


Figure 3. Graphics Aperture Address Translation

Since address translation using the above scheme requires an access to system memory, an on-chip cache (called a "Translation Lookaside Buffer" or TLB) is utilized to enhance performance. The TLB in the K8T800 contains 16 entries. Address "misses" in the TLB require an access of system memory to retrieve translation data. Entries in the TLB are replaced using an LRU (Least Recently Used) algorithm.

Addresses are translated only for accesses within the "Graphics Aperture" (GA). The Graphics Aperture can be any power of two in size from 1MB to 256MB (i.e., 1MB, 2MB, 4MB, 8MB, etc) for AGP 2.0 and 4MB to 2GB for AGP 3.0. The base of the Graphics Aperture can be anywhere in the system virtual address space on an address boundary determined by the aperture size (e.g., if the aperture size is 4MB, the base must be on a 4MB address boundary). The Graphics Aperture Base is defined in register offset 10 of device 0. The Graphics Aperture Size and TLB Table Base are defined in the following register groups (Rx84 and 88 respectively for AGP 2.0 and Rx94 and 98 for AGP 3.0) along with various control bits.

AGP 2.0 Registers

AGP 2.0 registers Rx80-AB are enabled if RxFD[1] = 1 and AGP 3.0 registers Rx80-AB are enabled if RxFD[1] = 0.

Device 0 Offset 83-80 – AGP 2.0 GART/TLB Control... RW

31-16 Reserved ..... always reads 0

15-8 Reserved (test mode status)..... RO

7 Flush Page TLB

0 Disable .....default

1 Enable

6-0 Reserved (always program to 0) ..... RW

Note: For any master access to the Graphics Aperture range, snoop will not be performed.

Device 0 Offset 84 – AGP 2.0 Graphics Aperture Size .. RW

7-0 Graphics Aperture Size

11111111 1M
11111110 2M
11111100 4M
11111000 8M
11110000 16M
11100000 32M
11000000 64M
10000000 128M
00000000 256M

AGPMiscellaneous Control

Offset 85 – AGP Buffer / Packet Control (01h)..... RW

7-6 Delay Read Response Buffer Release

00 No Delay ..... default
01 Delay 1T (2T Rate)
01 Delay 2T (3T Rate)
11 Delay 3T (4T Rate)

5 Sequence ID Value for AGP Isochronous Video Display

0 SeqID = 0 ..... default
1 SeqID = 1

4-3 Reserved .....always reads 0

2 Value of PASSPW Bit in AGP Master Upstream Request Packet

1 Value of Sequence ID in PCI/AGP Master Upstream Request Packet

0 Soc Bit in CPU-to-PCI Response Packet Same as Corresponding Request Packet

0 Always Clear
1 Same ..... default

Offset 86 – PCI Master R/W Merge Timers (4Fh) ..... RW

7 Reserved .....always reads 0

6-4 PCI Master Read Merge Timer

Used for waiting for the next request.

000 Disable
001 1 tick (7.5ns per tick)
010 2 ticks
011 3 ticks
100 4 ticks ..... **default**
101 5 ticks
110 6 ticks
111 7 ticks

3-0 PCI Master Write Merge Timer

Used for waiting for the next request.

0000 Disable
0001 1 tick (each tick = 60 nsec)
0010 2 ticks
0011 3 ticks
... ...
1111 15 ticks ..... **default**

Offset 8B-88 – AGP 2.0 GART Table Base..... RW

31-12 Graphics Aperture Translation Table Base. Pointer to the base of the translation table in system memory used to map addresses in the aperture range (the pointer to the base of the "Directory" table).

11-2 Reserved ..... always reads 0

1 Graphics Aperture
- 0 Disable .....default
- 1 Enable

Note: To disable the Graphics Aperture, set this bit to 0 and set all bits of the Graphics Aperture Size to 0. To enable the Graphics Aperture, set this bit to 1 and program the Graphics Aperture Size to the desired aperture size.

0 Reserved ..... always reads 0

Device 0 Offset A3-A0 - AGP 2.0 Capabilities (0020C002h) .....RO

31-24 Reserved ..... always reads 00

23-20 Major Specification Revision ... always reads 0010b
Major rev # of AGP spec that device conforms to

19-16 Minor Specification Revision ... always reads 0000b
Minor rev # of AGP spec that device conforms to

15-8 Pointer to Next Item ..... always reads C0 (last item)

7-0 AGP Capability ID
(always reads 02 to indicate it is AGP)

Device 0 Offset A7-A4 - AGP 2.0 Status (1F000201h) ....RO

31-24 Maximum AGP Requests..... always reads 1Fh
Max # of AGP requests the device can manage (32)

23-10 Reserved .....always reads 0s

9 Supports SideBand Addressing ..... **always reads 1**

8-6 Reserved .....always reads 0s

5 Addresses Above 4G Supported ..... always reads 0†

4 Fast Write Supported..... always reads 0†

3 Reserved .....always reads 0s

2 4X Rate Supported ..... always reads 0†

1 2X Rate Supported ..... always reads 0†

0 1X Rate Supported ..... **always reads 1**

†Writable if RxFD[0] = 1.

Device 0 Offset AB-A8 - AGP 2.0 Command..... RW

31-24 Request Depth (reserved for target).. always reads 0s

23-10 Reserved ..... always reads 0s

9 SideBand Addressing Enable
- 0 Disable..... default
- 1 Enable

8 AGP Enable
- 0 Disable..... default
- 1 Enable

7-6 Reserved ..... always reads 0s

5 4G Enable
- 0 Disable..... default
- 1 Enable

4 Fast Write Enable
- 0 Disable..... default
- 1 Enable

3 Reserved ..... always reads 0s

2 4X Mode Enable
- 0 Disable..... default
- 1 Enable

1 2X Mode Enable
- 0 Disable..... default
- 1 Enable

0 1X Mode Enable
- 0 Disable..... default
- 1 Enable

AGP 3.0 Registers

AGP 3.0 registers Rx80-AB are enabled if RxFD[1] = 0 and AGP 2.0 registers Rx80-AB are enabled if RxFD[1] = 1.

Device 0 Offset 83-80 - AGP 3.0 Capabilities (0035C002h) ..... RO

- **31-24 Reserved** ..... always reads 0
- **23-20 Major Specification Revision** ... always reads **0011b**
  Major rev # of AGP spec that device conforms to
- **19-16 Minor Specification Revision** ... always reads **0101b**
  Minor rev # of AGP spec that device conforms to
- **15-8 Pointer to Next Item** ..... always reads C0 (last item)
- **7-0 AGP Capability ID**
  (always reads 02 to indicate it is AGP)

Device 0 Offset 87-84 - AGP 3.0 Status (1F000A03h) ..... RO

- **31-24 Maximum AGP Requests** ..... **always reads 1Fh**
  Max # of AGP requests the device can manage (32)
- **23-16 Reserved** ..... always reads 0s†
- **15-13 Optimum Async Request Size** ..... always reads 0s†
  Suggested setting is 010b or 2^(2+4)=64 Bytes for 8QW access
- **12-10 Calibration Cycle Setting**
  - 000 4 ms
  - 001 16 ms
  - 010 64 ms ..... **default†**
  - 011 256 ms
- **9 Supports SideBand Addressing** ..... **always reads 1**
- **8 Reserved** ..... always reads 0†
- **7 64-Bit GART Entries** ..... always reads 0
- **6 CPU GART Translation Supported**. always reads 0
- **5 Addresses Above 4G Supported** ..... always reads 0
- **4 Fast Write Supported** ..... always reads 0
- **3 AGP 8x Detected** ..... Set from AGP8XDT# pin
- **2 4X Rate Supported** ..... Reads 0 if bit-3 = 1
  ..... Reads 1 if bit-3 = 0
- **1 2X Rate Supported** ..... **always reads 1**
- **0 1X Rate Supported** ..... **always reads 1**

†Writable if RxFD[0] = 1.

Device 0 Offset 8B-88 - AGP 3.0 Command ..... RW

- **31-24 Request Depth** (reserved for target) .... always reads 0
- **23-13 Reserved** ..... always reads 0
- **12-10 Calibration Cycle Select** ..... default = 0
- **9 SideBand Addressing**
  - 0 Disable ..... default
  - 1 Enable
- **8 AGP**
  - 0 Disable ..... default
  - 1 Enable
- **7-6 Reserved** ..... always reads 0
- **5 Addresses Over 4G**
  - 0 Disable ..... default
  - 1 Enable
- **4 Fast Write**
  - 0 Disable ..... default
  - 1 Enable
- **3 Reserved** ..... always reads 0
- **2-0 Transfer Mode Select** ..... default = 000b

  Rx84[3] = 0 (8x mode **not detected** via AGP8XDT#)
  - 001 1x data transfer rate
  - 010 2x data transfer rate
  - 100 4x data transfer rate

  Rx84[3] = 1 (8x mode **detected** via AGP8XDT#)
  - 000 -reserved ..... default
  - 001 4x data transfer rate
  - 010 8x data transfer rate

Device 0 Offset 8F-8C - AGP 3.0 Isochronous Status .... RW

- **31-24 Reserved** ..... always reads 0
- **23-16 Max Asynchronous & Isochronous Bandwidth**
  ...default = half of DRAM Bandwidth Backdoor Regs
- **15-8 Maximum Number of Isochronous Transactions in a Single Isochronous Period** ..... default = 0
- **7-6 Isochronous Payload Sizes Supported**
  - 00 256, 128, 64, 32 bytes ..... default
  - 01 256, 128, 64 bytes
  - 10 256, 128 bytes
  - 11 256 bytes
- **5-3 Max Latency for Isochronous Data Transfer**
  (in units of 1 usec) ..... default = 0
- **2 Reserved** ..... always reads 0
- **1-0 Isochronous Error Code**
  - 00 No Error ..... default
  - 01 Isoch Request Overflow
  - 1x -reserved-

Device 0 Offset 93-90 - AGP 3.0 GART / TLB Control.RW

31-10 Reserved .....always reads 0s
9 Calibration Cycle
0 Disable .....default
1 Enable
8 Graphics Aperture Base Register (Rx13-10) Read
0 Disable .....default
1 Enable
7 GART TLB
0 Disable (TLB entries are invalidated)....default
1 Enable
6-0 Reserved .....always reads 0s

Device 0 Offset 97-94 - AGP 3.0 Graphics Aperture SizeRW

31-28 Aperture Page Size Select.....default = 0000b
Only 4K pages are allowed
27 Reserved ..... always reads 0s
26-16 Page Size Supported.....default = 001h
If bit-n of this field is 1, indicates support of 2^(n+12) page size. Must be set to 001h (field bit-0 set) to indicate only 4K pages allowed.
15-12 Reserved ..... always reads 0s
11-0 Aperture Size.....default = 0

111100111111	4MB
111100111110	8MB
111100111100	16MB
111100111000	32MB
111100110000	64MB
111100100000	128MB
111100000000	256MB
111000000000	512MB
110000000000	1GB
100000000000	2GB <= Max supported
000000000000	4GB <= Do not program

Device 0 Offset 9B-98 - AGP 3.0 GART Table Base Lo RW

31-12 GART Base Address [31:12] .....default = 0
11-0 Reserved ..... always reads 0s

Device 0 Offset 9F-9C - AGP 3.0 GART Table Base Hi RW

31-0 GART Base Address [63:32] .....default = 0
This register should be programmed to all zeros since memory over 4GB is not supported.

AGP 2.0 / 3.0 Registers

Device 0 Offset AC - AGP Control (00h) ..... RW

7 **AGP Disable**
- 0 Enable ..... default
- 1 Disable

6 **AGP Read Synchronization**
- 0 Disable ..... default
- 1 Enable

5 **AGP Read Snoop DRAM Post-Write Buffer**
- 0 Disable ..... default
- 1 Enable

4 **GREQ# Priority Becomes Higher When Arbiter is Parked at AGP Master**
- 0 Disable ..... default
- 1 Enable

3 **GGNT Assertion**
- 0 Assert when 1 block of data is back ..... default
- 1 Assert when all data of this request is back

2 **Fence / Flush**
- 0 Disable (low priority reads and writes will be executed out of order) ..... default
- 1 Enable (low priority reads and writes will be executed in order)

1 **AGP Arbitration Parking**
- 0 Disable ..... default
- 1 Enable (GGNT# remains asserted until either GREQ# de-asserts or data phase ready)

0 **AGP to PCI Master or CPU to PCI Turnaround Cycle**
- 0 2T or 3T Timing ..... default
- 1 1T Timing

Device 0 Offset AD – AGP Latency Timer (02h)..... RW

7 **AGP Performance Improvement**
- 0 Disable ..... default
- 1 Enable

6 **Pipe Mode Performance Improvement**
- 0 Disable ..... default
- 1 Enable

5 **AGP Data Input Enable (for Power Saving)**
- 0 AGP data input always enabled ..... default
- 1 AGP data input only enabled when necessary to avoid redundant transitions

4 **AGP Performance Improvement**
- 0 Disable ..... default
- 1 Enable

3-0 **AGP Data Phase Latency Timer** ..... default = 02h

Device 0 Offset AE – AGP Misc Control (00h) ..... RW

7-2 **Reserved** ..... always reads 0

1 **GDBIH / GPIPE# Mux Function**
- 0 From GDBIH (0.95) ..... default
- 1 From GPIPE# (0.9)

0 **CPU GART Read, AGP GART Write Coherency**
- 0 Disable ..... default
- 1 Enable

Device 0 Offset AF – AGP 3.0 Control (00h)..... RW

7 **CPU / PCI Master GART Access**
- 0 Disable ..... default
- 1 Enable

6 **AGP Calibration**
- 0 Disable ..... default
- 1 Enable

5 **Mix Coherent / Non-coherent Accesses**
- 0 Disable ..... default
- 1 Enable

4 **Reserved** ..... always reads 0

3 **DBI Function**
- 0 Disable (DBI input masked and all outputs assume DBI=0) ..... default
- 1 Enable

2 **DBI Output for AGP Transactions**
- 0 Disable ..... default
- 1 Enable

1 **DBI Output for Frame Transactions Including Fast-Write**
- 0 Disable ..... default
- 1 Enable

0 **DBI Output from Frame Transactions**
- 0 Disable ..... default
- 1 Enable

Device 0 Offset B0 – AGP Pad Control / Status (8xh)....RW

7 AGP 4x Strobe VREF Control
- 0 STB VREF is STB# and vice versa
- 1 STB VREF is AGPREF ..... **default**

6 AGP 4x Strobe & GD Pad Drive Strength
- 0 Drive strength set to compensation circuit default ..... default
- 1 Drive strength controlled by RxB1[7-0]

5-3 AGP Compensation Circuit N Control Output.RO

2-0 AGP Compensation Circuit P Control Output.RO

Note: N = low drive, P = high drive

Device 0 Offset B1 – AGP Drive Strength (63h).....RW

7-4 AGP Output Buffer Low Drive Strength..... def=6

3-0 AGP Output Buffer High Drive Strength..... def=3

Device 0 Offset B2 – AGP Pad Drive / Delay (08h)..... RW

7 GD/GBE/GDS, SBA/SBS Control
- 0 SBA/SBS = no cap ..... default
  GD/GBE/GDS = no cap
- 1 SBA/SBS = **cap**
  GD/GBE/GDS = **cap**

6-5 GD / GBE Receive Strobe Delay
- 00 None ..... default
- 01 Delay by 0.15 ns
- 10 Delay by 0.30 ns
- 11 Delay by 0.45 ns

4 GD[31-16] Staggered Delay
- 0 None ..... default
- 1 GD[31:16] delayed by 1 ns

3 AGP Slew Rate Control
- 0 Disable
- 1 Enable..... **default**

2 SBA Receive Strobe Delay
- 0 None ..... default
- 1 Delay by 0.15 ns

1-0 GDS Output Delay
- 00 None ..... default
- 01 Delay by 0.15 ns
- 10 Delay by 0.30 ns
- 11 Delay by 0.45 ns

(GDS1 & GDS1# will be delayed an additional 1ns if bit-4 = 1)

Device 0 Offset B3 – AGP Strobe Drive Strength..... RW

7-4 AGP Strobe Output Low Drive Strength.....def=0

3-0 AGP Strobe Output High Drive Strength .....def=0

V-Link Compensation / Drive Control

Device 0 Offset B4 – V-Link NB Compensation Ctrl (00h)RW

- 7-5 **V-Link Autocomp Output Value – High Drive**. RO
- 4 **Reserved** ..... always reads 0
- 3-1 **V-Link Autocomp Output Value – Low Drive**.. RO
- 0 **Compensation Select**
  - 0 Auto Comp (use values in bits 7-5, 3-1) default
  - 1 Manual Comp (use values in RxB5, B6)

Device 0 Offset B5 – V-Link NB Strobe Drive Ctrl (00h)RW

- 7-5 **V-Link Strobe Pullup Manual Setting (High)**
- 4 **Reserved** ..... always reads 0
- 3-1 **V-Link Strobe Pulldown Manual Setting (Low)**
- 0 **Reserved** ..... always reads 0

Device 0 Offset B6 – V-Link NB Data Drive Ctrl (00h). RW

- 7-5 **V-Link Data Pullup Manual Setting (High)**
- 4 **Reserved** ..... always reads 0
- 3-1 **V-Link Data Pulldown Manual Setting (Low)**
- 0 **Reserved** ..... always reads 0

Device 0 Offset B8 – V-Link SB Compensation Ctrl (00h)RW

- 7-5 **V-Link Autocomp Output Value – High Drive**. RO
- 4 **Reserved** ..... always reads 0
- 3-1 **V-Link Autocomp Output Value – Low Drive**.. RO
- 0 **Compensation Select**
  - 0 Auto Comp (use values in bits 7-5, 3-1) default
  - 1 Manual Comp (use values in RxB9, BA)

Device 0 Offset B9 – V-Link SB Strobe Drive Ctrl (00h)RW

- 7-5 **V-Link Strobe Pullup Manual Setting (High)**
- 4 **Reserved** ..... always reads 0
- 3-1 **V-Link Strobe Pulldown Manual Setting (Low)**
- 0 **Reserved** ..... always reads 0

Device 0 Offset BA – V-Link SB Data Drive Ctrl (00h). RW

- 7-5 **V-Link Data Pullup Manual Setting (High)**
- 4 **Reserved** ..... always reads 0
- 3-1 **V-Link Data Pulldown Manual Setting (Low)**
- 0 **Reserved** ..... always reads 0

Power Management Control

Device 0 Offset BC – Power Management Mode (00h) . RW

- 7 **Dynamic Power Management**
  - 0 Disable..... default
  - 1 Enable
- 6-0 **Reserved** ..... always reads 0

Device 0 Offset BE – Dynamic Clock Stop Control (00h)RW

- 7 **Host Interface Power Management**
  - 0 Disable..... default
  - 1 Enable
- 6 **Reserved** ..... always reads 0
- 5 **V-Link Interface Power Management**
  - 0 Disable..... default
  - 1 Enable
- 4 **AGP Interface Power Management**
  - 0 Disable..... default
  - 1 Enable
- 3 **PCI #2 Interface Power Management**
  - 0 Disable..... default
  - 1 Enable
- 2 **Reserved** ..... always reads 0
- 1 **V-Link Configuration Power Management**
  - 0 Disable..... default
  - 1 Enable
- 0 **Reserved** ..... always reads 0

HyperTransport Control

Device 0 Offset C3-C0 – Link Command (0060 5808h). RW

31-29 Slave / Primary Interface Type..... default = 0, **RO**

28-26 Reserved ..... always reads 0

25-21 Unit ID Count..... **default = 3, RO**
Specifies the number of UnitIDs used by the chip

20-16 Base Unit ID [4:0] ..... default = 0
Specifies the link-protocol base UnitID. Internal logic uses this value to determine the UnitIDs for link requests and response packets. When a new value is written to this field, the response includes a UnitID that is based on the new value.

15-8 Capabilities Pointer ..... **default = 58h, RO**

7-0 Capabilities ID ..... **default = 08h, RO**
Specifies the capabilities ID for the link configuration space

Device 0 Offset C7-C4 – Link Configuration & Control (xx11 0020h).....RW

31 **Reserved** ..... always reads 0

30-28 **Link Width Out**..... default per CPU straps†
Specifies the operating width of the outgoing link.
- 000 8 bits .....default
- 001 16 bits (Device A, 0C4h only)
- 01x -reserved-
- 100 2 bits
- 101 4 bits
- 110 -reserved-
- 111 0 bits (not connected)

27 **Reserved** ..... always reads 0

26-24 **Link Width In** ..... default per CPU straps†
Specifies the operating width of the incoming link.
- 000 8 bits .....default
- 001 16 bits (Device A, 0C4h only)
- 01x -reserved-
- 100 2 bits
- 101 4 bits
- 110 -reserved-
- 111 0 bits (not connected)

† The default values of the above fields depend on the widths of the links of the connecting devices per the HyperTransport link specification. These fields are cleared by PWROK but not by RESET#. After the field is updated, the link width does not change until either RESET# is asserted or a link disconnect sequence occurs via LDTSTOP# (HyperTransport Stop).

23 **Reserved** ..... always reads 0

22-20 **Max Link Width Out**..... **default = 001b, RO**
Specifies the operating width of the outgoing link to be 16 bits wide for side A and 8 bits wide for side B.

19 **Reserved** ..... always reads 0

18-16 **Max Link Width In**..... **default = 001b, RO**
Specifies the operating width of the incoming link to be 16 bits wide for side A and 8 bits wide for side B.

15 **Reserved** ..... always reads 0

14 **Extended Control Time During Initialization‡**
Specifies the time in which HT[B,A]CTL is held asserted during the initialization sequence that follows LDTSTOP# assertion after HT[B,A]CTL is detected asserted.
- 0 At least 16 bit times .....default
- 1 About 50 microseconds

‡This bit is cleared by PWROK but not by RESET#

13 **Link High Impedance Enable‡**
- 0 During the LDTSTOP# disconnect sequence, the link transmit signals are driven but to undefined states and the link receive signals are assumed to be driven. ..... default
- 1 During the LDTSTOP# disconnect sequence, the link transmit signals are set to high impedance states and the link receivers are configured for high impedance inputs (power is cut to the receiver differential amps and it is guaranteed that there are no high-current paths in the receive circuits).

12-10 **Reserved** .....always reads 0

9-8 **CRC Error Detected on Incoming Link‡..... RWC**
Bit-9 applies to the link upper byte (DevA, C4h only)
Bit-8 applies to the link lower byte

7 **Transmitter Off**
- 0 On ..... default
- 1 Off

6 **End of Chain**
- 0 Not EOC..... default
- 1 EOC

5 **Initialization Complete ..... RO**
Set by hardware after low-level link initialization has completed successfully. If there is no device on the other end of the link or the device on the other end is unable to properly perform link initialization, then this bit is not set. This bit is cleared by RESET# or after the link disconnect sequence completes after the assertion of LDTSTOP#.

4 **Link Failure‡..... RWC**
This bit is set by hardware when a CRC error is detected on the link (if enabled by bit-1 below) or if the link is not used in the system.

3 **CRC Error Command**
This bit may be used to check the CRC failure detection logic of the device on the other side of the link.
- 0 Transmitted CRC values match the values calculated per the link specification. ..... default
- 1 Link transmission logic generates erroneous CRC values

2 **Reserved** .....always reads 0

1 **CRC Flood Enable**
- 0 CRC errors do not result in sync packets and do not set the link fail bit..... default
- 1 CRC errors result in sync packets to the outgoing link and set the link fail bit

0 **Reserved** .....always reads 0

‡This bit is cleared by PWROK but not by RESET#

Device 0 Offset CB-C8 – Link End (0000 00D0h) .....RO

31-8 Reserved ..... always reads 0

7 Transmitter Off..... always reads 1
Hardwired high to indicate that there is no subordinate HyperTransport link.

6 End of HyperTransport Chain ..... always reads 1
Hardwired high to indicate that there is no subordinate HyperTransport link.

5 Reserved ..... always reads 0

4 Link Failure..... always reads 1
Hardwired high to indicate that there is no subordinate HyperTransport link.

3-0 Reserved ..... always reads 0

Device 0 Offset CF-CC – Link Frequency Capability (0035 0022h).....RW

31-16 Link Frequency Capability..... def=0035h, RO
These bits indicate that the link supports 200, 400, 600 and 800 MHz link frequencies.

15-12 Reserved ..... always reads 0

11-8 Link Frequency.....RW
Specifies the link frequency. The two msbs of this field default to 00b. The two lsbs of this field are latched from VAD[1:0] on the rising edge of PWROK (but not by RESET#) to set the default value (normally 00b for 200 MHz operation). After this field is updated, the link frequency does not change until either RESET# is asserted or a link disconnect sequence occurs via LDTSTOP# (HyperTransport Stop).
0000 200 MHz **...lsbs default per straps VAD[1:0]**
0010 400 MHz
0100 600 MHz
0101 800 MHz
all other values are reserved

7-5 Link Major Revision..... default = 001b, RO

4-0 Link Minor Revision..... default = 00010b, RO
These fields are hardwired to indicate support of revision 1.02 of the HyperTransport link specification.

Device 0 Offset D7-D4 – Link Enumeration Scratchpad (0000 0000h).....RW

31-16 Reserved .....always reads 0

15-0 Enumeration Scratchpad.....default = 0000h
No internal hardware is controlled by these bits. These bits are cleared by PWROK but not by RESET#.

HyperTransport I/O

Device 0 Offset D8 – Transmit Data Rise / Fall Delay (00h)..... RW

- 7-6 **Positive Data Signal Rising Edge Delay**..... def=0
- 5-4 **Positive Data Signal Falling Edge Delay**..... def=0
- 3-2 **Negative Data Signal Rising Edge Delay**..... def=0
- 1-0 **Negative Data Signal Falling Edge Delay** ..... def=0

Device 0 Offset D9 – Transmit Clock Rise / Fall Delay (00h)..... RW

- 7-6 **Positive Clock Signal Rising Edge Delay** ..... def=0
- 5-4 **Positive Clock Signal Falling Edge Delay** ..... def=0
- 3-2 **Negative Clock Signal Rising Edge Delay**..... def=0
- 1-0 **Negative Clock Signal Falling Edge Delay**..... def=0

Device 0 Offset DA – Transmit Data Drive Ctrl (00h)... RW

- 7 **Data Coarse Delay** ..... default = 0
- 6-4 **Data Pullup Drive Control**..... default = 0
- 3 **Reserved** ..... always reads 0
- 2-0 **Data Pulldown Drive Control**..... default = 0

Device 0 Offset DB – Transmit Clck Drive Ctrl (00h) ... RW

- 7 **Clock Coarse Delay**..... default = 0
- 6-4 **Clock Pullup Drive Control** ..... default = 0
- 3 **Reserved** ..... always reads 0
- 2-0 **Clock Pulldown Drive Control** ..... default = 0

Device 0 Offset DC – Transmit Autocomp Result (00h) RW

- 7 **Transmit Autocomp Select**
  - 0 Manual .....default
  - 1 Automatic
- 6-4 **Transmit Pullup Drive Strength From Autocomp** ..... default = 0
- 3 **Reserved** ..... always reads 0
- 2-0 **Transmit Pulldown Drive Strength From Autocomp** ..... default = 0

Device 0 Offset DD – Receive Data / Clock Rise / Fall Delay (00h) ..... RW

- 7-6 **Data Input Rising Edge Delay**..... default = 0
- 5-4 **Data Input Falling Edge Delay**..... default = 0
- 3-2 **Clock Input Rising Edge Delay** ..... default = 0
- 1-0 **Clock Input Falling Edge Delay** ..... default = 0

Device 0 Offset DE – Receive Terminator Value (22h) . RW

- 7 **Autocomp Termination Value**
  - 0 Manual..... default
  - 1 Automatic
- 6-4 **Data Receive Termination Value**..... **default = 010b**
- 3 **Reserved** ..... always reads 0
- 2-0 **Clock Receive Termination Value** ... **default = 010b**

Device 0 Offset DF – Receive Terminator Autocomp Status (00h)..... RW

- 7 **TCAD / RCAD High / Low Byte Delay Control**
  - 0 Configure / read low byte (TCAD[7:0] / RCAD[7:0]) delay control..... default
  - 1 Configure / read high byte (TCAD[15:8] / RCAD[15:8]) delay control

  The registers include RxD8, D9, DD
- 6-4 **Receive Termination Autocomp Value**... default = 0
- 3-2 **Receive PLL Feedback Delay Fine Tune**
  - 00 Lead 0.1 ns ..... default
  - 01 Aligned
  - 10 Lag 0.1 ns
  - 11 Lag 0.2 ns
- 1-0 **Receive Clock Delay**
  - 00 1T (200 MHz)..... default
  - 01 2T
  - 10 3T
  - 11 Illegal setting - do not use

DRAM Above 4G Control

Device 0 Offset E4 – Low Top Address Low (00h).....RW

7-4 Low Top Address Low ..... default = 0

3-0 DRAM Granularity

0 16M Total DRAM less than 4G.....default
1 32M Total DRAM less than 8G
2 64M Total DRAM less than 16G
3 128M Total DRAM less than 32G
4 256M Total DRAM less than 64G
5-7 -reserved-

Device 0 Offset E5 – Low Top Address High (FFh).....RW

7-0 Low Top Address High.....default = FFh

Device 0 Offset E6 – SMM / APIC Decoding (01h).....RW

7-6 Reserved ..... always reads 0

5 APIC Lowest Interrupt Arbitration

0 Disable .....default
1 Enable

4 I/O APIC Decoding

0 FECxxxxx accesses go to PCI.....default
1 FEC00000 to FEC7FFFF accesses go to PCI
FEC80000 to FECFFFFF accesses go to AGP

3 MSI (Processor Message) Support

0 Disable (master access to FEExxxxx will go to PCI) .....default
1 Enable (master access to FEExxxxx will be passed to host side to do snoop)

2 Top SMM

0 Disable .....default
1 Enable

1 Reserved ..... always reads 0

0 Compatible SMM

0 Disable
1 Enable .....**default**

Table 5. System Memory Map

Space	Start	Size	Address Range	Comment
DOS	0	640K	00000000-0009FFFF	Cacheable
VGA	640K	128K	000A0000-000BFFFF	Used for SMM
BIOS	768K	16K	000C0000-000C3FFF	Shadow Ctrl 1
BIOS	784K	16K	000C4000-000C7FFF	Shadow Ctrl 1
BIOS	800K	16K	000C8000-000CBFFF	Shadow Ctrl 1
BIOS	816K	16K	000CC000-000CFFFF	Shadow Ctrl 1
BIOS	832K	16K	000D0000-000D3FFF	Shadow Ctrl 2
BIOS	848K	16K	000D4000-000D7FFF	Shadow Ctrl 2
BIOS	864K	16K	000D8000-000DBFFF	Shadow Ctrl 2
BIOS	880K	16K	000DC000-000DFFFF	Shadow Ctrl 2
BIOS	896K	64K	000E0000-000EFFFF	Shadow Ctrl 3
BIOS	960K	64K	000F0000-000FFFFF	Shadow Ctrl 3
Sys Bus Init	1MB D Top 4G-64K	— 64K	00100000-DRAM Top DRAM Top-FFFEFFFF FFFEFFFF-FFFFFFFF	Can have hole 000Fxxxx alias

AGP / V-Link Control

Device 0 Offset E8 – AGP Output Delay ..... RW

7-6 AGP Data Output Rise Delay (GD) ..... def=0
5-4 AGP Data Output Fall Delay (GD) ..... def=0
3-2 AGP Data Strobe Output Rise Delay (GDS) . def=0
1-0 AGP Data Strobe Output Fall Delay (GDS) .. def=0

Device 0 Offset E9 – AGP / VL Receive Strobe Delay ... RW

7-6 AGP Strobe Receive Rise Delay (GDS) ..... def=0
5-4 AGP Strobe Receive Fall Delay (GDS) ..... def=0
3-2 V-Link Strobe Receive Rise Delay (UPSTB) . def=0
1-0 V-Link Strobe Receive Fall Delay (UPSTB) .. def=0

Device 0 Offset EA – V-Link Output Delay ..... RW

7-6 V-Link Data Output Rise Delay (VAD) ..... def=0
5-4 V-Link Data Output Fall Delay (VAD) ..... def=0
3-2 V-Link Strobe Output Rise Delay (DNSTB) . def=0
1-0 V-Link Strobe Output Fall Delay (DNSTB) .. def=0

Device 0 Offset EB – AGP SBA Termination Control ... RW

7-3 Reserved ..... always reads 0
2-0 SBA Termination Manual Control ..... default = 0

Device 0 Offset EC – AGP Isochronous Control 1 ..... RW

7-4 Reserved ..... always reads 0
3 Isoch Read Shares Master AGP FIFO When No Asynch Read is Allocated
  0 Disable ..... default
  1 Enable
2 Isoch Read Will Snoop Command FIFO
  0 Disable ..... default
  1 Enable
1 Issue Request to Arbitor for GGNT
  0 When data from entire transaction is rcvd ...def
  1 When 1 block of data is received
0 Reserved ..... always reads 0

Device 0 Offset ED – AGP Isochronous Control 2 ..... RW

7 Reserved ..... always reads 0
6 Hold Last AGP Data (GD Pins)
  0 Disable ..... default
  1 Enable
5-0 Fill Isoch Request Queue by VXD After Checking the Value of Isoch Status Bits for Error Report in the Capability Header (Rx8C[1-0]).

Device 0 Offset EE – AGP Master Isoch Read Timer ... RW

7-0 AGP Master High Priority Counter for Isoch Request to Assert High Priority Signal to DRAM Controller for Isoch Reads

Device 0 Offset EF – AGP Master Isoch Write Timer .. RW

7-0 AGP Master High Priority Counter for Isoch Request to Assert High Priority Signal to DRAM Controller for Isoch Writes

BIOS Scratch

Device 0 Offset F3-F4 – BIOS Scratch Registers ..... RW

7-0 No hardware function ..... default = 0

Miscellaneous Registers

Device 0 Offset FD – AGP 2.0 / 3.0 Select ..... RW

7-3 Reserved ..... always reads 0
2 AGP Capability Pointer (Rx34) Value
  0 Rx34 = A0h (AGP 2.0) ..... default
  1 Rx34 = 80h (AGP 3.0)
1 Compatible Rx80-AF
  0 AGP 3.0 registers at Rx80-B3 ..... default
  1 AGP 2.0 registers at Rx80-B3
0 AGP Status Register Write
  0 Disable (AGP 3.0 Rx84 is RO) ..... default
  1 Enable (AGP 3.0 Rx84 is RW)

Device 1 Register Descriptions

Device 1 PCI-to-PCI Bridge Header Registers

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number of 0 and function number equal to 0 and device number equal to one.

Device 1 Offset 1-0 - Vendor ID (1106h) ..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 1 Offset 3-2 - Device ID (B188h) ..... RO

15-0 ID Code (reads B188h to identify the PCI-to-PCI Bridge device)

Device 1 Offset 5-4 – Command (0007h) ..... RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent ..... default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable ..... RO
- 0 SERR# driver disabled ..... default
- 1 SERR# driver enabled

(SERR# is used to report ECC errors).

7 Address / Data Stepping ..... RO
- 0 Device never does stepping ..... default
- 1 Device always does stepping

6 Parity Error Response ..... RW
- 0 Ignore parity errors & continue ..... default
- 1 Take normal action on detected parity errors

5 Reserved ..... always reads 0

4 Memory Write and Invalidate Command ..... RO
- 0 Bus masters must use Mem Write ..... default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring ..... RO
- 0 Does not monitor special cycles ..... default
- 1 Monitors special cycles

2 Bus Master ..... RW
- 0 Never behaves as a bus master
- 1 Enable to operate as a bus master on the primary interface on behalf of a master on the secondary interface ..... default

1 Memory Space ..... RW
- 0 Does not respond to memory space
- 1 Enable memory space access ..... default

0 I/O Space ..... RW
- 0 Does not respond to I/O space
- 1 Enable I/O space access ..... default

Device 1 Offset 7-6 - Status (Primary Bus) (0230h) .... RWC

15 Detected Parity Error ..... always reads 0

14 Signaled System Error (SERR#) ..... always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master with Master-Abort (except Special Cycles) ..... **write 1 to clear**

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target with Target-Abort ..... **write 1 to clear**

11 Signaled Target Abort ..... always reads 0

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium ..... **always reads 01**
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected ..... always reads 0

7 Fast Back-to-Back Capable ..... always reads 0

6 User Definable Features ..... always reads 0

5 66MHz Capable ..... **always reads 1**

4 Supports New Capability list ..... **always reads 1**

3-0 Reserved ..... always reads 0

Device 1 Offset 8 - Revision ID (00h) ..... RO

7-0 Chip Revision Code (00=First Silicon)

Device 1 Offset 9 - Programming Interface (00h) ..... RO

This register is defined in different ways for each Base/Sub-Class Code value and is undefined for this type of device.

7-0 Interface Identifier ..... always reads 00

Device 1 Offset A - Sub Class Code (04h) ..... RO

7-0 Sub Class Code .reads 04 to indicate PCI-PCI Bridge

Device 1 Offset B - Base Class Code (06h) ..... RO

7-0 Base Class Code.. reads 06 to indicate Bridge Device

Device 1 Offset D - Latency Timer (00h) ..... RO

7-0 Reserved ..... always reads 0

Device 1 Offset E - Header Type (01h) ..... RO

7-0 Header Type Code ..... reads 01: PCI-PCI Bridge

Device 1 Offset 18 - Primary Bus Number (00h).....RW

7-0 Primary Bus Number ..... default = 0

This register is read write, but internally the chip always uses bus 0 as the primary.

Device 1 Offset 19 - Secondary Bus Number (00h).....RW

7-0 Secondary Bus Number..... default = 0

Note: AGP must use these bits to convert Type 1 to Type 0.

Device 1 Offset 1A - Subordinate Bus Number (00h)....RW

7-0 Primary Bus Number ..... default = 0

Note: AGP must use these bits to decide if Type 1 to Type 1 command passing is allowed.

Device 1 Offset 1B – Secondary Latency Timer (00h)....RO

7-0 Reserved ..... always reads 0

Device 1 Offset 1C - I/O Base (F0h).....RW

7-4 I/O Base AD[15:12]..... default = 1111b

3-0 I/O Addressing Capability ..... default = 0

Device 1 Offset 1D - I/O Limit (00h).....RW

7-4 I/O Limit AD[15:12] ..... default = 0

3-0 I/O Addressing Capability ..... default = 0

Device 1 Offset 1F-1E - Secondary Status.....RO

15-0 Secondary Status

Rx44[4] = 0: these bits read back 0000h

Rx44[4] = 1: these bits read back same as Rx7-6

Device 1 Offset 21-20 - Memory Base (FFF0h).....RW

15-4 Memory Base AD[31:20].....default = FFFh

3-0 Reserved ..... always reads 0

Device 1 Offset 23-22 - Memory Limit (Inclusive) (0000h) RW

15-4 Memory Limit AD[31:20] ..... default = 0

3-0 Reserved ..... always reads 0

Device 1 Offset 25-24 - Prefetchable Mem Base (FFF0h) RW

15-4 Prefetchable Memory Base AD[31:20]default = FFFh

3-0 Reserved ..... always reads 0

Device 1 Offset 27-26 - Prefetchable Memory Limit (0000h) .....RW

15-4 Prefetchable Memory Limit AD[31:20] . default = 0

3-0 Reserved ..... always reads 0

Device 1 Offset 34 - Capability Pointer (80h) .....RO

Contains an offset from the start of configuration space.

7-0 AGP Capability List Pointer..... always reads 80h

Device 1 Offset 3F-3E – PCI-to-PCI Bridge Control (0000h) ..... RW

15-4 Reserved .....always reads 0

3 VGA-Present on AGP

0 Forward VGA accesses to PCI Bus..... default

1 Forward VGA accesses to AGP Bus

Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.

2 Block / Forward ISA I/O Addresses

0 Forward all I/O accesses to the AGP bus if they are in the range defined by the I/O Base and I/O Limit registers (device 1 offset 1C-1D)

..... default

1 Do not forward I/O accesses to the AGP bus that are in the 100-3FFh address range even if they are in the range defined by the I/O Base and I/O Limit registers.

1-0 Reserved .....always reads 0

Device 1 PCI-to-PCI Bridge Device-Specific Registers

AGP Bus Control

Device 1 Offset 40 - CPU-to-AGP Flow Control 1 (00h) RW

7 CPU-to-AGP Post Write
- 0 Disable ..... default
- 1 Enable

6 CPU-to-AGP One Wait State Burst Write
- 0 Disable ..... default
- 1 Enable

5-4 Read Prefetch Control
- 00 Always prefetch ..... default
- x1 Never prefetch
- 10 Prefetch only for Enhance command

3 Reserved ..... always reads 0

2 MDA Present on AGP
- 0 Forward MDA accesses to AGP ..... default
- 1 Forward MDA accesses to PCI

Note: Forward despite IO / Memory Base / Limit

Note: MDA (Monochrome Display Adapter) addresses are memory addresses B0000h-B7FFFh and I/O addresses 3B4-3B5h, 3B8-3BAh and 3BFh (10-bit decode). 3BC-3BE are reserved for printers.

Note: If Rx3E bit-3 is 0, this bit is a don't care (MDA accesses are forwarded to the PCI bus).

1 AGP Master Read Caching
- 0 Disable ..... default
- 1 Enable

0 AGP Delay Transaction
- 0 Disable ..... default
- 1 Enable

Table 6. VGA/MDA Memory/IO Redirection

3E[3] VGA Pres.	40[2] MDA Pres.	VGA is on	MDA is on	Axxxx, B8xxx Access	B0000 -B7FFF Access	3Cx, 3Dx I/O	3Bx I/O
0	-	PCI	PCI	PCI	PCI	PCI	PCI
1	0	AGP	AGP	AGP	AGP	AGP	AGP
1	1	AGP	PCI	AGP	PCI	AGP	PCI

Device 1 Offset 41 - CPU-to-AGP Flow Control 2 (08h) RW

7 Retry Status
- 0 No retry occurred ..... default
- 1 Retry Occurred ..... **write 1 to clear**

6 Retry Timeout Action
- 0 No action taken except to record status ..... def
- 1 Flush buffer for write or return all 1s for read

5-4 Retry Count
- 00 Retry 2, backoff CPU ..... default
- 01 Retry 4, backoff CPU
- 10 Retry 16, backoff CPU
- 11 Retry 64, backoff CPU

3 CPU-to-AGP Bursting Timeout
- 0 Disable
- 1 Enable ..... **default**

2 Reserved ..... always reads 0

1 CPU-to-PCI/AGP Cycles Invalidate PCI/AGP Buffered Read Data
- 0 Disable ..... default
- 1 Enable

0 Reserved ..... always reads 0

Device 1 Offset 42 - AGP Master Control (00h) ..... RW

7 Reserved (Must Be Programmed to 1) ..... def = 0

When this bit is set, the chip will automatically resolve the problem of AGP master cycles being blocked by PCI Master Cycles.

6 AGP Master One Wait State Write
- 0 Disable ..... default
- 1 Enable

5 AGP Master One Wait State Read
- 0 Disable ..... default
- 1 Enable

4 Break Consecutive PCI Master Accesses
- 0 Disable ..... default
- 1 Enable

3 Reserved ..... always reads 0

2 Claim I/O R/W and Memory Read Cycles
- 0 Disable ..... default
- 1 Enable

1 Claim Local APIC FEEx xxxx Cycles
- 0 Disable ..... default
- 1 Enable

0 Snoop Write Enable 2T Rate, Support Host Side Snoop Cycles at 2T Rate
- 0 Disable ..... default
- 1 Enable

Device 1 Offset 43 - AGP Master Latency Timer (22h) RW

7-4 Host to AGP Time slot
- 0 Disable (no timer)
- 1 16 GCLKs
- 2 32 GCLKs ..... default
- ... ...
- F 128 GCLKs

3-0 AGP Master Time Slot
- 0 Disable (no timer)
- 1 16 GCLKs
- 2 32 GCLKs ..... default
- ... ...
- F 128 GCLKs

Device 1 Offset 45 – Fast Write Control (72h) ..... RW

7 Force Fast Write Cycle to be QW Aligned (if Rx45[6] = 0)
- 0 Disable ..... default
- 1 Enable

6 Merge Multiple CPU Transactions Into One Fast Write Burst Transaction
- 0 Disable
- 1 Enable ..... **default**

5 Merge Multiple CPU Write Cycles To Memory Offset 23-20 Into Fast Write Burst Cycles (if Rx45[6] = 0)
- 0 Disable
- 1 Enable ..... **default**

4 Merge Multiple CPU Write Cycles To Prefetchable Memory Offset 27-24 Into Fast Write Burst Cycles (if Rx45[6] = 0)
- 0 Disable
- 1 Enable ..... **default**

3 Assert GSTOP# When CPU Has An Open AGP Request and Master Timeout
- 0 Disable ..... default
- 1 Enable

2 Fast Write Burst 4T Max (No Slave Flow Control)
- 0 Disable ..... default
- 1 Enable

1 Fast Write Fast Back to Back
- 0 Disable
- 1 Enable ..... **default**

0 Fast Write Initial Block 1 Wait State
- 0 Disable ..... default
- 1 Enable

Rx45 Bits 7-4	CPU Write Address in Mem1	CPU Write Address in Mem2	Fast Write Cycle Alignment
x1xx	-	-	QW aligned, burstable
0000	-	-	DW aligned, nonburstable
x010	0	0	n/a
0010	0	1	DW aligned, non-burstable
x010	1	-	QW aligned, burstable
x001	0	0	n/a
x001	-	1	QW aligned, burstable
0001	1	0	DW aligned, non-burstable
x011	0	0	n/a
x011	1	-	QW aligned, burstable
x011	0	1	QW aligned, burstable
1000	-	-	QW aligned, non-burstable
1010	0	1	QW aligned, non-burstable
1001	1	0	QW aligned, non-burstable

AGP Bus Control (continued)

Device 1 Offset 47-46 – PCI-to-PCI Bridge Device ID...RW

15-0 PCI-to-PCI Bridge Device ID ..... default = 0000

Device 1 Offset 48 – AGP / PCI2 Error Reporting .....WC

7 AGP Cycle Data Parity Error.....WC
- 0 Parity Error did not occur.....default
- 1 Parity error occurred .....write 1 to clear

6 PCI #2 GSERR Error.....WC
- 0 Parity Error did not occur.....default
- 1 Parity error occurred .....write 1 to clear

5 Reserved ..... always reads 0

4 Generate Parity Error on AGP Data Parity Error
- 0 Disable .....default
- 1 Enable

3-2 Reserved ..... always reads 0

1 Generate Parity Error on PCI #2 Data Parity Error
- 0 Disable .....default
- 1 Enable

0 Generate Parity Error on PCI #2 Address Parity Error
- 0 Disable .....default
- 1 Enable

Power Management

Device 1 Offset 80 – Capability ID (01h) ..... RO

7-0 Capability ID .....always reads 01h

Device 1 Offset 81 – Next Pointer (00h)..... RO

7-0 Next Pointer: Null .....always reads 00h

Device 1 Offset 82 – Power Mgmt Capabilities 1 (02h).. RO

7-0 Power Mgmt Capabilities .....always reads 02h

Device 1 Offset 83 – Power Mgmt Capabilities 2 (00h).. RO

7-0 Power Mgmt Capabilities .....always reads 00h

Device 1 Offset 84 – Power Mgmt Ctrl/Status (00h)..... RW

7-2 Reserved .....always reads 0

1-0 Power State
- 00 D0 ..... default
- 01 -reserved-
- 10 -reserved-
- 11 D3 Hot

Device 1 Offset 85 – Power Mgmt Status (00h)..... RO

7-0 Power Mgmt Status ..... default = 00

Device 1 Offset 86 – P2P Br. Support Extensions (00h). RO

7-0 P2P Bridge Support Extensions ..... default = 00

Device 1 Offset 87 – Power Management Data (00h) ..... RO

7-0 Power Management Data ..... default = 00

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T_C	Case Operating Temperature	0	85	°C	1
T_S	Storage Temperature	–55	125	°C	1
V_{IN}	Input Voltage	–0.5	V_{RAIL} + 10%	Volts	1, 2
V_{OUT}	Output Voltage	–0.5	V_{RAIL} + 10%	Volts	1, 2

Note 1. Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

Note 2. V_{RAIL} is defined as the V_{CC} level of the respective rail. The HyperTransport CPU interface is CPU dependent (typically 1.2V). V-Link is 1.5V. AGP is 1.5V (4x transfer mode) or 0.8V (8x transfer mode).

Supply Current and Power Characteristics

T_C = 0-85°C, V_{RAIL} = V_{CC} ± 5%, V_{CORE} = 2.5V ± 5%, GND=0V

Table 8. Supply Current and Power Characteristics – Internal and Interface Digital Logic

Symbol	Parameter	Typ	Max	Unit	Condition
I_{CC}	Power Supply Current – VCC	–	76	mA	All conditions
I_{SUS}	Power Supply Current – VCCSUS	1.0	1.1	**uA**	All conditions
I_{CCHT}	Power Supply Current – VCCHT	–		mA	8-bit, 200 MHz
I_{CCVL}	Power Supply Current – VCCVL	–	1.8	mA	4x transfer mode
$I_{CCVLIDLE}$	Power Supply Current – VCCVL	–	8	**uA**	Idle
I_{CCG}	Power Supply Current – VCCAGP	–	16	mA	No AGP cycles active
I_{CCQQ}	Power Supply Current – VCCQQ	–		mA	No AGP cycles active
P_D	Power Dissipation – Entire Chip	–		W	Max operating frequency

Table 9. Supply Current and Power Characteristics – Analog and Reference Voltages

Symbol	Parameter	Typ	Max	Unit	Condition
I_{CCGREF}	Power Supply Current – AGPVREF	–	2.4	mA	No AGP cycles active
$I_{CCVLREF}$	Power Supply Current – VLVREF	–	5.0	mA	4x transfer mode
I_{CCATX}	Power Supply Current – VCCATX			mA	8-bit, 200 MHz
I_{CCARX}	Power Supply Current – VCCARX			mA	8-bit, 200 MHz

DC Characteristics

T_C = 0-85°C, GND = 0V, V_{CC} = 2.5V ±5%, V_{CCHT} = 1.2V±5%, V_{CCAGP} = 1.5V±5% (4x) or 0.8V±5% (8x), V_{CCVL} = 2.5V±5%

Table 10. DC Characteristics – HyperTransport

Symbol	Parameter	Min	Typ	Max	Unit	Condition / Signal
V_{HTIL}	Single-Ended Input Low Voltage	–0.30	–	0.7	V	LDTSTOP#
V_{HTIH}	Single-Ended Input High Voltage	1.7	–	V_{CC} + 0.3	V	LDTSTOP#
V_{HTOL}	Single-Ended Output Low Voltage	–	–	0.7	V	HTRST#
V_{HTOH}	Single-Ended Output High Voltage	1.7	–	–	V	HTRST#
I_{HTIL}	Single-Ended Input Leakage	–	–	±500	uA	V_{CC} = Max, V_I = Gnd or V_{CC}
V_{HTOD}	Differential Output Voltage†	495	600	715	mV	TCADx, TCLKx, TCTLx
V_{HTID}	Differential Input Voltage†	300	600	900	mV	RCADx, RCLKx, RCTLx
Delta V_{HTID}		–125	0	125	mV	
V_{ICM}	Input Common Mode Voltage	450	600	800	mV	
Delta V_{ICM}		–110	0	110	mV	
T_R	Differential Signal Rise Time	2		8	V/ns	
T_F	Differential Signal Fall Time	–2		–8	V/ns	

For Reference Only – See HyperTransport Standard documents for detailed specifications
†HyperTransport differential I/O assumes N>P = logical 0 and P>N = logical 1.

Table 11. DC Characteristics – V-Link

Symbol	Parameter	Min	Max	Unit	Condition
V_{VIL}	Input Low Voltage	–0.50	0.8	V	
V_{VIH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{VOL}	Output Low Voltage	-	0.55	V	I_{OL} = 4.0 mA
V_{VOH}	Output High Voltage	2.4	–	V	I_{OH} = –1.0 mA
I_{VIL}	Input Leakage Current	–	±10	uA	$0 < V_{IN} < V_{CCVL}$

Table 12. DC Characteristics – AGP

Symbol	Parameter	Min	Max	Unit	Condition
V_{AIL4x}	Input Low Voltage – 4x Transfer Mode	–0.50		V	
V_{AIH4x}	Input High Voltage – 4x Transfer Mode		V_{CC} + 0.5	V	
V_{AOL4x}	Output Low Voltage – 4x Transfer Mode	-		V	I_{OL} = x.x mA
V_{AOH4x}	Output High Voltage – 4x Transfer Mode		–	V	I_{OH} = –x.x mA
V_{AIL8x}	Input Low Voltage – 8x Transfer Mode	–0.50		V	
V_{AIH8x}	Input High Voltage – 8x Transfer Mode		V_{CC} + 0.5	V	
V_{AOL8x}	Output Low Voltage – 8x Transfer Mode	-		V	I_{OL} = x.x mA
V_{AOH8x}	Output High Voltage – 8x Transfer Mode		–	V	I_{OH} = –x.x mA
I_{AIL}	Input Leakage Current	–	±10	uA	$0 < V_{IN} < V_{CCAGP}$
I_{AOZ}	Tristate Leakage Current	–	±20	uA	$0.55 < V_{OUT} < V_{CCAGP}$

For Reference Only – See AGP 3.0 Standard documents for detailed specifications

AGP Signal Levels

AGP 3.0 (8x transfer mode) specifies a 0.8V voltage swing, end-terminated and referenced to ground as opposed to AGP 2.0 (4x transfer mode), which specified a rail-to-rail 1.5V series-terminated voltage swing.

This change permits a higher data rate and a common signaling voltage, which can be realized in multiple generations of silicon technology. The figure below shows the relationship between the VCCQQ and GNDQQ rails and the corresponding output voltage swing for AGP 3.0-compatible 8x transfer mode.

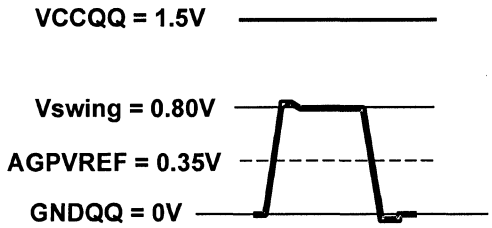


Figure 4. AGP 3.0 (8x) Signal Levels

Table 13. DC Characteristics – Reset, Power OK, Suspend Status and Test

Symbol	Parameter	Min	Max	Unit	Condition
V_{VIL}	Input Low Voltage	–0.50	0.8	V	
V_{VIH}	Input High Voltage	2.0	3.8	V	3.3V Tolerant
I_{VIL}	Input Leakage Current	–	±10	uA	$0 < V_{IN} < V_{CC}$

AC Timing Specifications

AC timing specifications provided are based on external zero-pf capacitance load. Min/max cases are based on the following table:

Table 14. AC Timing Min / Max Conditions

Parameter	Min	Max	Unit
2.5V Power (Internal Logic)	2.375	2.625	Volts
1.5V Power (VCCQQ for 4x transfer mode)	1.425	1.575	Volts
0.8V Power (VCCQQ for 8x transfer mode)	0.76	0.84	Volts
Case Temperature	0	85	°C

Drive strength for selected output pins is programmable and may effect AC timing specifications.

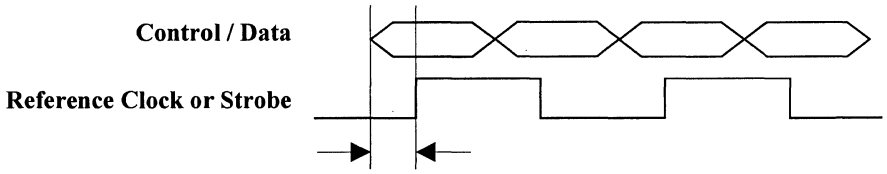
Table 15. AC Characteristics – HyperTransport CPU Interface Receive

Symbol	Parameter	Setup	Hold	Unit
T_{RLS4}, T_{RLH4}	RCAD0-7, RCTL / RCTL# input relative to RCLK0 / RCLK0# - 400 MT/s	300	300	pS
T_{RLS8}, T_{RLH8}	RCAD0-7, RCTL / RCTL# input relative to RCLK0 / RCLK0# - 800 MT/s	200	200	pS
T_{RLS12}, T_{RLH12}	RCAD0-7, RCTL / RCTL# input relative to RCLK0 / RCLK0# - 1.2 GT/s	150	150	pS
T_{RLS16}, T_{RLH16}	RCAD0-7, RCTL / RCTL# input relative to RCLK0 / RCLK0# - 1.6 GT/s	120	120	pS
T_{RHS4}, T_{RHH4}	RCAD8-15 input relative to RCLK1 / RCLK1# - 400 MT/s	300	300	pS
T_{RHS8}, T_{RHH8}	RCAD8-15 input relative to RCLK0 / RCLK0# - 800 MT/s	200	200	pS
T_{RHS12}, T_{RHH12}	RCAD8-15 input relative to RCLK0 / RCLK0# - 1.2 GT/s	150	150	pS
T_{RHS16}, T_{RHH16}	RCAD8-15 input relative to RCLK0 / RCLK0# - 1.6 GT/s	120	120	pS

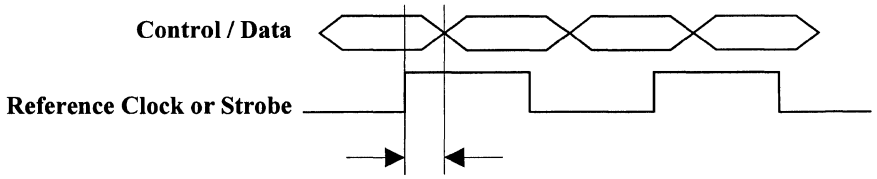
Table 16. AC Characteristics – HyperTransport CPU Interface Transmit

Symbol	Parameter	Min	Max	Unit
T_{TLD4}	TCAD0-7, TCTL / TCTL# output delay from TCLK0 / TCLK0# - 400 MT/s	650	1800	pS
T_{TLD8}	TCAD0-7, TCTL / TCTL# output delay from TCLK0 / TCLK0# - 800 MT/s	325	950	pS
T_{TLD12}	TCAD0-7, TCTL / TCTL# output delay from TCLK0 / TCLK0# - 1.2 GT/s	220	625	pS
T_{TLD16}	TCAD0-7, TCTL / TCTL# output delay from TCLK0 / TCLK0# - 1.6 GT/s	180	475	pS
T_{THD4}	TCAD8-15 output delay from TCLK1 / TCLK1# - 400 MT/s	650	1800	pS
T_{THD8}	TCAD8-15 output delay from TCLK1 / TCLK1# - 800 MT/s	325	950	pS
T_{THD12}	TCAD8-15 output delay from TCLK1 / TCLK1# - 1.2 GT/s	220	625	pS
T_{THD16}	TCAD8-15 output delay from TCLK1 / TCLK1# - 1.6 GT/s	180	475	pS

Termination resistor values: R_{TT} = 100 Ω ±10%, R_{ON} = 50 Ω ±10%



Input: Setup Time
Output: Data Valid before Strobe



Input: Hold Time
Output: Data Valid after Strobe

Figure 5. Timing Diagram – HyperTransport Setup / Hold and Data Valid

Table 17. AC Characteristics – HyperTransport CPU Interface Reset / Stop

Symbol	Parameter	Min	Max	Unit
T_{HRPW}	HTRST# Input Pulse Width		–	uS
T_{HSPW}	LDTSTOP# Input Pulse Width		–	uS
	CPU STPGNT# to LDTSTOP#	32	–	uS
	LDTSTOP# to SUSST# Asserted	32	–	uS
	Resume Event to SUSST# Deasserted	1250	–	uS
	SUSST# Deasserted to LDTSTOP# Deasserted	32	–	uS

Table 18. AC Characteristics – AGP 8x

Symbol	Parameter	Min	Max	Unit
T_{GS8}	Data / Control Input Setup Time Relative to Strobe – 8x Transfer Mode	250	–	pS
T_{GH8}	Data / Control Input Hold Time Relative to Strobe – 8x Transfer Mode	250	–	pS
T_{GS4}	Data / Control Input Setup Time Relative to Strobe – 4x Transfer Mode	500	–	pS
T_{GH4}	Data / Control Input Hold Time Relative to Strobe – 4x Transfer Mode	500	–	pS
T_{GDV8}	Data / Control Output Valid Relative to Strobe – 8x Transfer Mode	–550	650	pS
T_{GDV4}	Data / Control Output Valid Relative to Strobe – 4x Transfer Mode	–1000	1000	pS

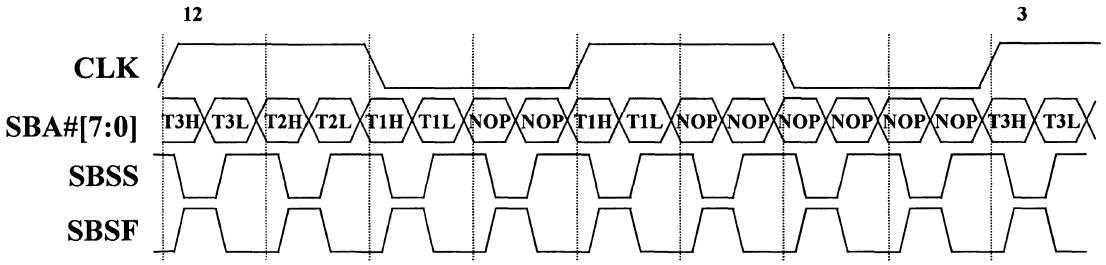


Figure 6. Timing Diagram – AGP 8x Sideband Address Timing

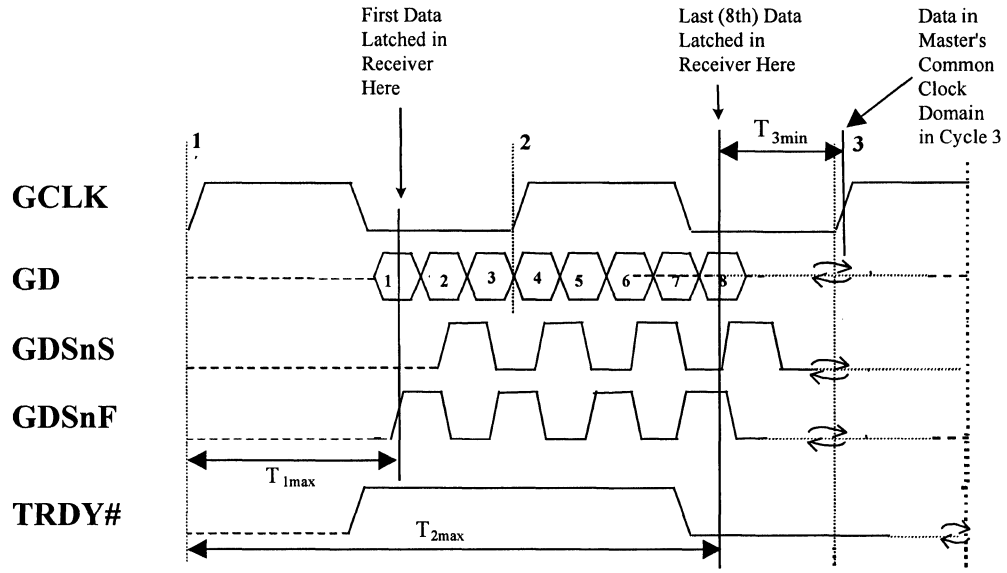
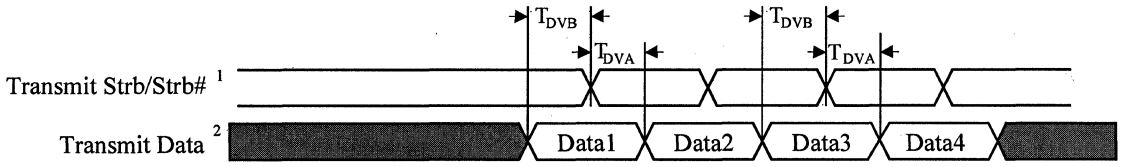


Figure 7. Timing Diagram – AGP 8x Data Transfer Timing



Note 1: This waveform represents two differential strobes
Note 2: Data refers to any of the 2x/4x capable signal groups: GD[31:0], GBE[3:0]# or SBA[7:0]

Figure 8. Timing Diagram – AGP 4x Transmit Timing

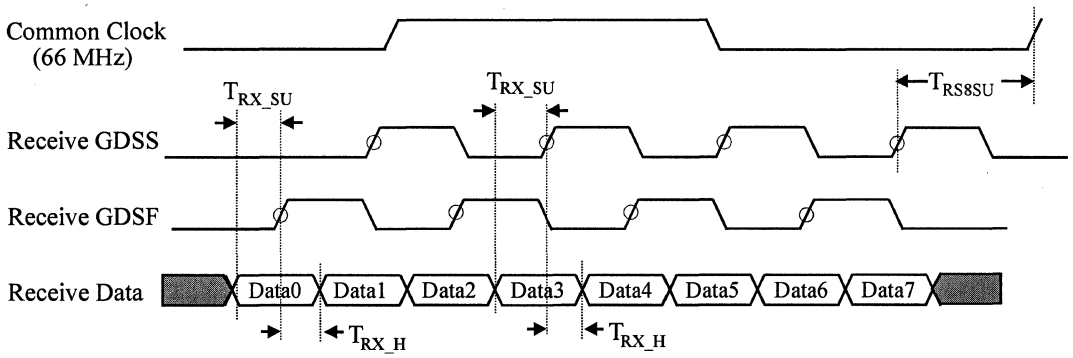
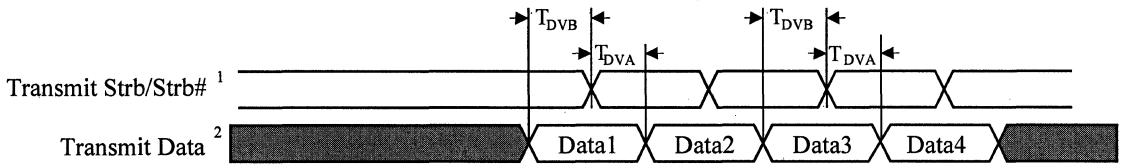


Figure 9. Timing Diagram – AGP 4x Receive Timing



Note 1: This waveform represents two differential strobes
Note 2: Data refers to any of the 2x/4x capable signal groups: GD[31:0], GBE[3:0]# or SBA[7:0]

Figure 10. Timing Diagram – AGP 8x Transmit Source-Synchronous Timing

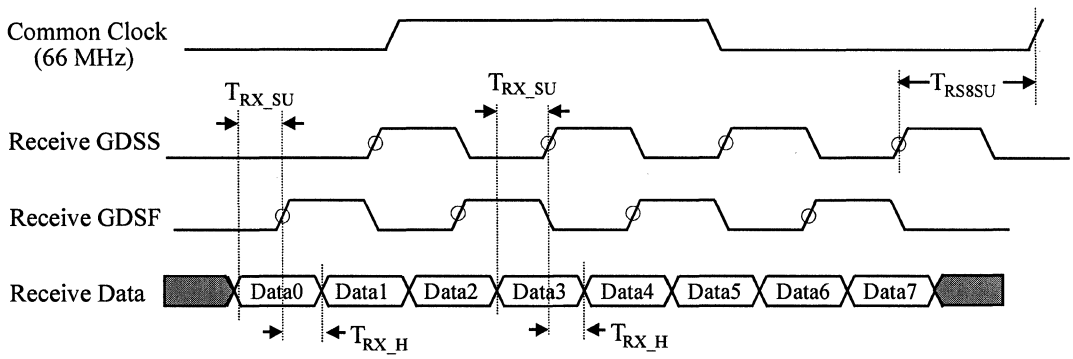


Figure 11. Timing Diagram – AGP 8x Receive Source-Synchronous Timing

Table 19. AC Characteristics – V-Link Interface

Symbol	Parameter	Min	Max	Unit	Condition
T_{VUS4}	VADn, VPAR, VBE#, UPCMD Input Setup to UPSTB / UPSTB#	500	–	**pS**	4x mode
T_{VUH4}	VADn, VPAR, VBE#, UPCMD Input Hold From UPSTB / UPSTB#	500	–	**pS**	4x mode
T_{VUS8}	VADn, VPAR, VBE#, UPCMD Input Setup to UPSTB / UPSTB#	250	–	**pS**	8x mode
T_{VUH8}	VADn, VPAR, VBE#, UPCMD Input Hold From UPSTB / UPSTB#	250	–	**pS**	8x mode
T_{VDD4}	VADn, VPAR, VBE#, DNCMD Output Delay from DNSTB / DNSTB#	–650	750	**pS**	4x mode
T_{VDD8}	VADn, VPAR, VBE#, DNCMD Output Delay from DNSTB / DNSTB#	–1100	1100	**pS**	8x mode
T_{VUP4}	UPSTB / UPSTB# Input Pulse Width			nS	4x mode
T_{VUF4}	UPSTB / UPSTB# Input Frequency		266	MHz	4x mode
T_{VUP8}	UPSTB / UPSTB# Input Pulse Width			nS	8x mode
T_{VUF8}	UPSTB / UPSTB# Input Frequency		533	MHz	8x mode
T_{VDP4}	DNSTB / DNSTB# Output Minimum Pulse Width			nS	4x mode
T_{VDF4}	DNSTB / DNSTB# Output Frequency		266	MHz	4x mode
T_{VDP8}	DNSTB / DNSTB# Output Minimum Pulse Width			nS	8x mode
T_{VDF8}	DNSTB / DNSTB# Output Frequency		533	MHz	8x mode

Table 20. AC Characteristics –Reset, Power OK and Suspend

Symbol	Parameter	Min	Max	Unit
T_{RLPU}	RESET# Low On Power Up	0	–	msec
T_{RLPW}	RESET# Low Pulse Width from PWROK	7	–	msec
T_{PLPU}	PWROK Low On Power Up After Power Supply Voltages Stable	50	–	msec
T_{SLPW}	SUSST# Low Pulse Width	1.2	–	msec
T_{VCSL}	Primary Voltages Removed After SUSST# Goes Low	64	–	**usec**
T_{VCSH}	Primary Voltages Stable (PWROK) Before SUSST# Returns High	250	–	**usec**

MECHANICAL SPECIFICATIONS

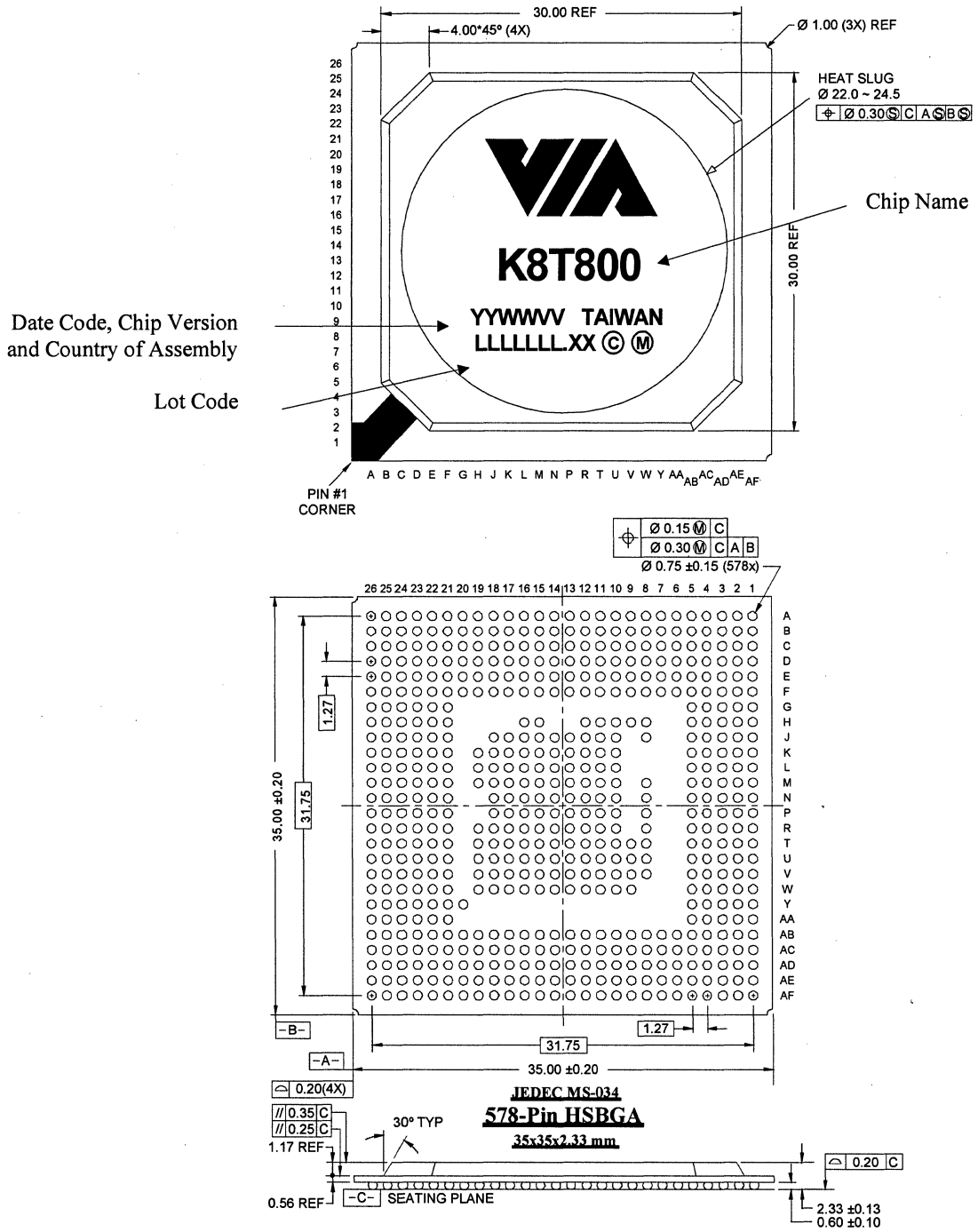


Figure 12. Mechanical Specifications – HSBGA-578 Ball Grid Array Package

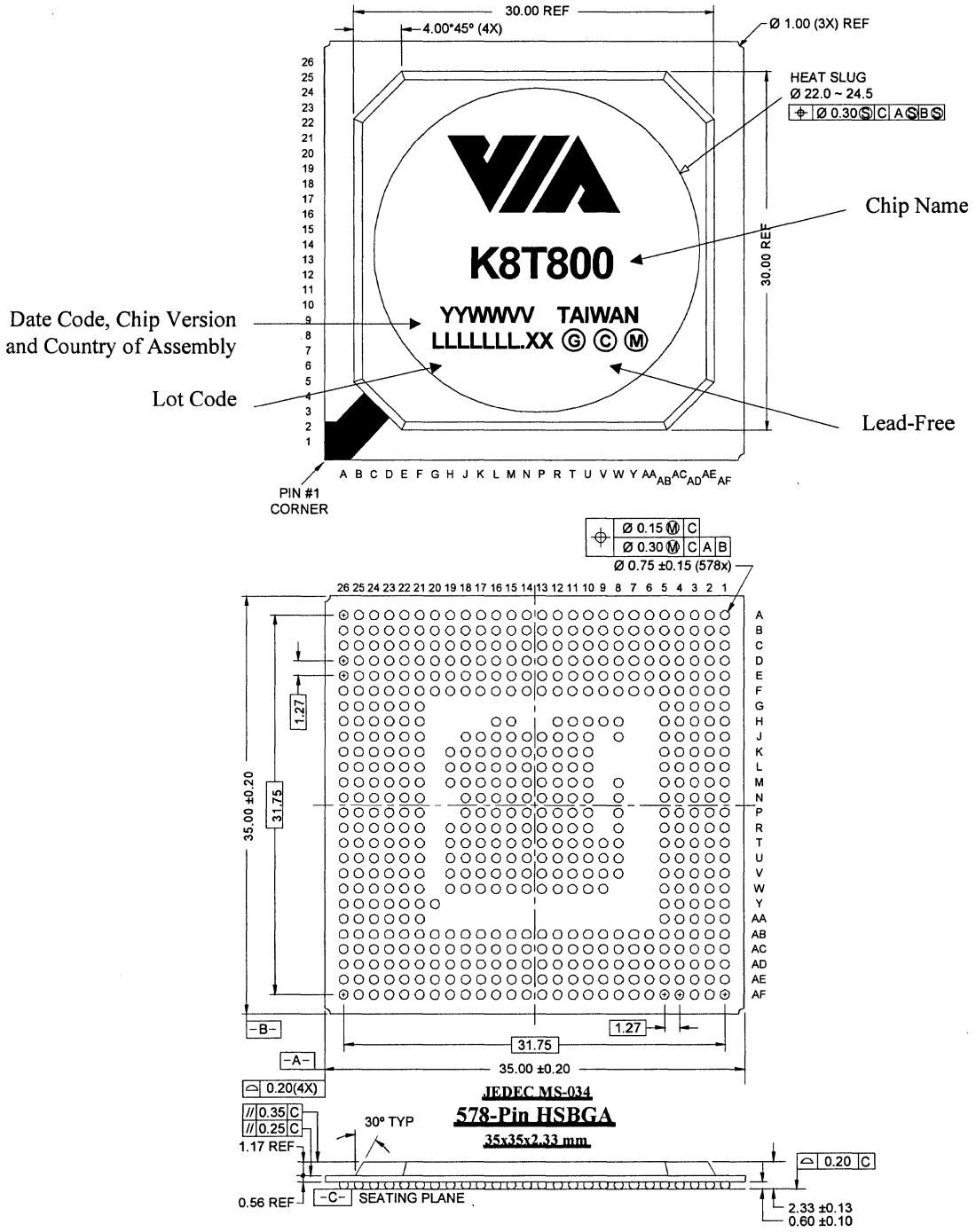


Figure 13. Lead-Free Mechanical Specifications – HSBGA-578 Ball Grid Array Package