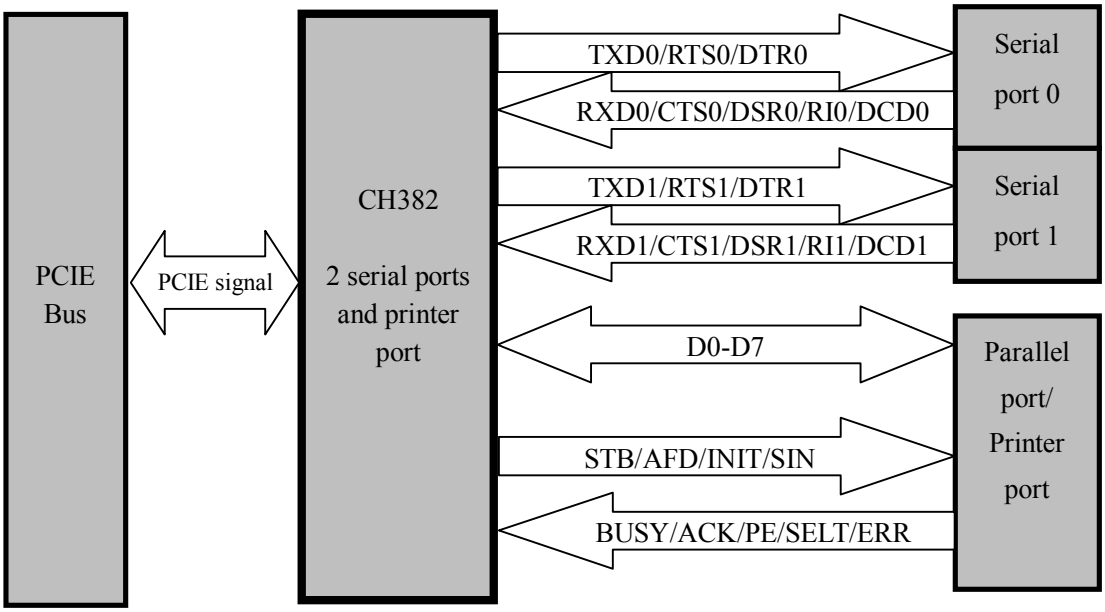
PCIE Bus Dual Serial Ports and Printer Port Chip CH382

Brief
Version: 1
http://wch.cn

1. Introduction

CH382 is a PCI-Express bus converter chip, which converts PCIE bus to dual serial ports and printer port, including two asynchronous serial ports compatible with 16C550 or 16C750, and one EPP/ECP enhanced bidirectional parallel port. The asynchronous serial port provides a transceiver with independent 256-byte FIFO buffer, supports communication baud rate up to 8Mbps and can be used for RS232 serial port expansion of PCIE bus, PCIE high-speed serial port with automatic hardware flow control, serial ports networking, RS485 communication, parallel/printer port expansion, etc.

The figure below shows its general application block diagram.



2. Features

2.1. Overview

- The same chip can be configured as a dual-channel serial ports, single parallel port/printer port, dual serial ports and parallel port/printer port of PCIE bus.
- Provides two-wire serial host interface, and EEPROM device similar to 24C0X which can be connected to store non-volatile data.
- The device identification (Vendor ID, Device ID, Class Code, etc.) of the PCIE board can be set in the EEPROM device.
- Drivers support Windows 98/ME/NT4.0/2000/XP/Vista/7/8/8.1/10/SERVER 2003/2008/2012/2016/2019and Linux.
- 3.3V power supply, I/O pins supports 5V withstand voltage, serial ports support low-power sleep mode.
- The chip function is equivalent to CH367 with CH438, providing 4 serial ports, 8 serial ports and more serial applications.
- Supports PCMCIA ExpressCard notebook card.

2.2. Serial Port

- 2 fully independent asynchronous serial ports, compatible with 16C550, 16C552, 16C554 and 16C750 and enhanced.
- Supports 5, 6, 7 or 8 data bits and 1 or 2 stop bits.
- Supports odd, even, mark, space and no parity. .
- Programmable communication baud rate, supports communication baud rate of 115200bps and up to 8Mbps.
- Internal 256-byte FIFO buffer, supports four FIFO trigger levels.
- Supports MODEM interface signals CTS, DSR, RI, DCD, DTR and RTS, which can be converted to RS232 signals.
- Supports automatic handshake and automatic transmission rate control of hardware flow control signals CTS and RTS, compatible with TL16C550C.
- Supports serial port frame error detection and Break line interval detection.
- Supports full-duplex and half-duplex UART communication.

2.3. Parallel Port

- Supports SPP, Nibble, Byte, PS/2, EPP, ECP and other IEEE1284 parallel port/printer port working modes.
- Supports bidirectional-data transmission and a transmission speed of up to 1M byte/s.

3. Package

Package	Width of Plastic	Pitch of Pin		Instruction of Package	Ordering Information
LQFP-64	7mm x 7mm	0.4mm	15.7mil	Ultra small LQFP64 patch	CH382L

4. Configuration

4.1. Global Function Configuration

CH382 has three main hardware function modes:

MDPRT# Pin	MDSEL Pin	Function Modes/Device ID	Abbreviation
Connect to VCC33 or suspended, which is MDPRT#=1	Connect to VCC33 or suspended, which is MDSEL=1	Dual serial ports, DID=3253H	2S
Connect to GND, which is MDPRT#=0	Connect to VCC33 or suspended, which is MDSEL=1	Dual serial ports and parallel port, DID=3250H	2S1P
Connect to GND, which is MDPRT#=0	Connect to GND, which is MDSEL=0	Single parallel port, DID=3050H	1P

CKSEL pin of CH382 is used to select the clock frequency of the internal 2 serial ports:

CKSEL is connected to VCC33 or suspended, i.e. when CKSEL=1, the clock is input from XO pin, the frequency is determined by the external crystal, and the internal frequency coefficient is 1/12 frequency division by default, and frequency doubling can be selected through CK2X or CKnS;

CKSEL is connected to GND, that is, when CKSEL=0, the clock is input from XO pin. The frequency is determined by the external crystal, and the internal frequency coefficient is always forced to be frequency doubling. For example, the serial port set to 115200bps by the application software is actually 230400bps;

CKSEL is connected to PERST# pin, that is, when CKSEL=R, the internal crystal oscillator is

disabled(XI and XO pins can be suspended without external crystal and capacitor), the internal PLL provides the clock with a frequency of 125MHz, and the internal frequency coefficient is 1/68 frequency division by default, and supported to select no frequency division through CK2X or CKnS. The 114.9kbps obtained by internal PLL mode 1/68 frequency division is only 0.27% different from the standard 115.2kbps, which is acceptable.

In single parallel port mode, CKSEL should be connected to PERST# pin to disable the internal crystal oscillator.

4.2. External Configuration Chip

CH382 will check the data in the external 24CXX configuration chip after each power-on or PCIE Bus reset. If the configuration chip is connected and the data is valid, it will be automatically loaded into CH382 to replace the default PCIE identification information.

The following table shows the data definition in the configuration chip 24CXX.

Byte address	Abbreviation	Description of Chip Configuration Data Area	Default
00H	CFG	The valid flag of the external configuration chip, must be 52H	52H
01H	FREQ	Bit 1 to bit 0are respectively used to select the internal frequency coefficient of serial port 1 to port 0	0FFH
03H-02H	RSVD	(Reserved)	0000H
05H-04H	VID	Vendor ID, the default is 1C00H	Customize
07H-06H	DID	Device ID, Abbreviated as DID	Customize
08H	RID	Chip version: Revision ID	Customize
0BH-09H	CLS	Device type code: Class Code	070005H
0DH-0CH	SVID	Subsystem Vendor ID	Customize
0FH-0EH	SID	Subsystem ID	Customize
1FH-10H	RSVD	(Reserved)	00H or FFH
Other address	APP	User or application program custom unit	

5. Applications

5.1. Dual Serial Ports + Parallel Port (Figure below)

This is the basic circuit for PCIE dual serial ports + parallel/printer port based on CH382. The figure does not include RS232 voltage conversion chip.

U3 is an optional external configuration chip, and the online configuration tool software for Windows system is available on the website.

IEEE1284 requires the printer port signals to keep impedance matching. Therefore, the parallel data singals of the printer port may be connected to resistors in series and capacitors in parallel, which can also be eliminated when the requirement is not high.

Crystal X1, capacitors C15 and C16 are used in the clock oscillation circuit. If the CKSEL pin is connected to the PERST# pin, then X1, C15 and C16 can be omitted. Other capacitors are used for power supply decoupling. The capacitor with a capacity of 10uF is a tantalum capacitor, and the capacitor with a capacity of 0.1uF is a monolithic or high-frequency ceramic capacitor, which are connected in parallel to the power pins of CH382 respectively.

CH382 supports common communication baud rate: 1200, 2400, 4800, 9600, 19.2K, 38.4K, 57.6K, 115.2K, 230.4K, 460.8K, 921.6K, 1.8432M, 2.7648M, 7.8125M, etc.

CH382 can be used to expand additional high-speed RS232 serial ports and parallel ports /printer ports for

computers through PCIE bus, high baud rate serial ports that support automatic hardware rate control, RS422 or RS485 communication interfaces, etc.

CH382is a high frequency circuit. Please refer to PCIE Bus specification or PCIE_PCB.PDF document when designing the PCB board.