XCELL

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XILINX®
The Programmable Logic Company℠

Inside This Issue:

GENERAL FEATURES

Ireland Facility On-Line

Xilinx's new 100,000 square foot facility in Dublin, Ireland is now processing all European orders...

See Page 9

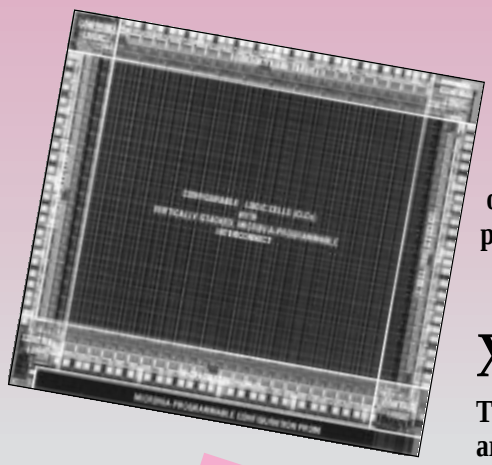
PRODUCT INFORMATION

Introducing three new FPGA Families!

XC4000E Family

With a myriad of new features, the XC4000E FPGA family increases performance over the existing XC4000 family by up to 50%...

See Page 18



XC8100 Family

The first Xilinx one-time-programmable FPGA family, based on MicroVia technology, enters production.

See Page 20

XC6200 Family

The new XC6200 SRAM-based FPGA architecture is the first FPGA specifically designed to implement reconfigurable coprocessors in embedded system applications.

See Page 22

PCI Compliant ≠ PCI Suitable

By BRADLY FAWCETT ◆ Editor

The rapid adoption and proliferation of the PCI (Peripheral Component Interconnect) bus has been one of the computer market's major success stories of the past year.

Originally defined by Intel, PCI has become an industrywide standard controlled by a consortium — the PCI Special Interest Group, or PCI SIG. The high-performance PCI bus can handle the throughput demands of data-intensive applications such as multimedia and high-speed networking.

Full compliance to the PCI SIG specification is a must for systems and boards that will be sold in the general marketplace where interoperability among multiple vendors is required.

To achieve high throughput and ensure interoperability between a wide variety of boards and host systems, the PCI specification includes a strict definition of its electrical interface. IC components that can meet the performance, loading and drive requirements of this electrical interface are said to be "PCI-compliant." By submitting the appropriate paperwork, component suppliers that are members of the PCI SIG can have their compliant devices added to an "Integrators List" that is available to other PCI SIG members.

Market Pressures and Marketing Tactics

PCI-related designs are a large potential market for high-density CPLDs and FPGAs. The flexibility of a programmable approach is attractive in a PC card market characterized by changing market needs and short product life cycles. These devices are, in fact, finding their way into many prototype and production PCI designs. Thus, programmable logic vendors are working hard to establish themselves as suppliers to this market. One tactic is to submit as many devices as possible for inclusion on the PCI SIG's Integrators List, and then, based on their inclusion on the list, advertise these devices as being "PCI Approved" (or a similar designation).

Designers of PCI boards and systems are advised to be leery of these claims. First, the PCI SIG does not guarantee the compliance of any device or offer any form of approval; submissions to the PCI SIG are strictly on the "honor system" and are not verified independently. (In fact, the component section of the Integrators List specifically states that functional testing is not required to be listed. The PCI SIG disclaims responsibility for any errors in the listings.) The Integrators List is considered confidential to PCI SIG members and is for their convenience only. Again, inclusion on the Integrators List does not constitute any endorsement or approval by the PCI SIG.

> *"...being 'PCI-compliant' does not necessarily mean these devices are suitable for use in a PCI application."*

Continued on page 5

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GUEST EDITORIAL

Developing New PLD Solutions

by CHUCK FOX ◆ Vice President, Product Marketing

By the end of 1995, Xilinx will have introduced more new programmable logic device family solutions in the last 18 months than in our prior ten-year history. Why so many? Why now? As with most semiconductor products, the answer to both questions stems from the convergence of technology and market needs.

Technology and Markets

First, there is the "push factor" of rapid advancements in IC fabrication technology. It took the industry nearly a decade to migrate from 2.0 micron to 1.0 micron technology. Yet, the move from 1.0 to 0.5 micron has taken less than five years (and 0.35 micron technology is only a year or so away). These shrinking IC geometries, along with larger wafer sizes, additional layers of metal interconnect, new software technologies and new packaging technologies have allowed dramatic increases in device density and performance. Equally dramatic price reductions have followed.

Advances in IC processing technology have accelerated the development of new programming structures. Xilinx is the only PLD company that is providing cost-effective and reliable SRAM, antifuse, EPROM and FLASH processes now available in volume production.

These technology shifts, of course, influence PLD architectural development. What conventional wisdom assumed was impossible yesterday may be feasible today. For example, the shift from two-layer to three-layer metal processes alters the "logic vs. routing" trade-offs in FPGA design (as evident in the new XC8100, XC5200, and XC6200 FPGA family architectures). Thus, advances in process technology lead to new programmable logic architectures.

Just as influential is the "pull factor" of increasingly competitive end-use markets. Today's electronic system market is characterized by global competition and changing industry standards, resulting in higher-performance products with shorter life cycles.

Design methodologies are changing; higher levels of design abstraction and automated tools are required to meet the twin challenges of increased complexity and decreased time-to-market.

> *"Xilinx is the only PLD company that is providing cost-effective and reliable SRAM, antifuse, EPROM and FLASH processes now available in volume production."*

Inspiration + Ability = New Architectures

Thus, our new product offerings reflect the goal of every electronics design: leverage advancing technology to best match users' needs. In some cases, this takes the form of evolutionary improvements to current products, such as enhancing the popular XC4000 FPGA architecture to create the XC4000E family. In other cases, it involves new product development to take full advantage of new technologies or to address new markets; for example, the XC5200 architecture leverages 3-layer metal technology to lower FPGA costs, thereby expanding FPGA

Continued on the next page

XILINX®

The high-performance XC7336Q is just one of the new products introduced by Xilinx in the first half of 1995.

Continued from the previous page

usage in high-volume applications.

Why so many PLD architectures? CPLDs and FPGAs are being used in an amazingly wide variety of logic applications, ranging from simple interface logic to reconfigurable computing arrays. While PLD use in communications, industrial and peripheral control applications continues to expand, increasing PLD capabilities and decreasing prices are opening up new markets in PC and consumer applications. Different applications have different needs. Different users have different preferences. No single technology or architecture can meet all those needs and desires.

The SRAM-based XC2000, XC3000A/XC3100A, XC4000E and XC5200 architectures remain the best FPGA architectures for "glue logic" applications. Each has a slightly different mix of attributes. The XC3100A family offers the best raw speed, the XC4000E provides the largest densities and feature set (including on-chip memory), and the XC5200 delivers the lowest cost per gate. We will continue to enhance these architectures and improve these product families. The new XC6200 FPGA architecture, with its built-in processor interface, targets a different type of application — reconfigurable coprocessing (although it will undoubtedly find its way into other applications as well). The XC8100 FPGAs are ideal for those applications requiring "instant-on" operation, the increased security of a one-time-programmable solution, or a more "ASIC-like," synthesis-friendly design flow.

Some applications fit better with a CPLD-type architecture. The XC7300 family, featuring industry-leading performance, continues to expand with the recent additions of the XC73144 and XC7336Q. A revolutionary, new, in-system programmable architecture, based on flash memory technology, will be introduced later this year.

"A broad product line supported by a powerful, unified suite of development tools gives the user the best of both worlds — the choice of the most-appropriate PLD architecture, and no need to purchase and learn a new set of design tools."

Industry Leadership

Why now? It has always been our corporate goal to be the leading supplier of programmable logic. Simply put, we want to fulfill all of our users' high-density programmable logic needs. As Xilinx and the programmable logic market grew in the late 1980s and early 1990s, we became the leading PLD supplier and could afford to make substantial investments in research and development. The new products appearing now are the result of years of development. As the largest and most successful supplier of programmable logic, we have the engineering resources to explore different approaches and support multiple development efforts. With the recent acquisition of FPGA-software-supplier NeoCAD, we are setting the standard for leading-edge development software to support multiple component families.

High-density PLDs are rapidly becoming a critical, strategic technology for leading electronic systems companies. A broad product line supported by a powerful, unified suite of development tools gives the user the best of both worlds — the choice of the most-appropriate PLD architecture, and no need to purchase and learn a new set of design tools. We think this is crucial to being not only your programmable logic *supplier*, but also your programmable logic *partner*. ◆

Continued from page 2

Compliance No Simple Task

Secondly, and more importantly, being "PCI-compliant" does not necessarily mean these devices are suitable for use in a PCI application. Electrical compliance only guarantees that the device meets the bare minimum electrical characteristics. It does not guarantee that the device has the logic capacity, functionality and overall speed to effectively implement a PCI interface design—the device may or may not be suitable for a real-world design.

For example, the PCI specification allows a 10 pF maximum load on a bus signal (except the clock signal, which is allowed a 12 pF maximum load), as well as a maximum trace length of 1.5 inches from the card edge connector to limit trace capacitance. Taken together, these two factors imply that each bus signal attaches to only one IC pin per board (that is, a signal coming from the connector can have only one destination).

Practically speaking, all the interface logic would need to be implemented in a single device in a fairly small package (such as a quad flat pack) so that all the pins can be close to the connector. A simple PCI interface typically requires about 100 I/O, about 4,000 usable gates, and well over 100 registers. The need for a single-chip solution eliminates a lot of the smaller PALs and CPLDs that have found their way on to the Integrators List and are advertised as "PCI-compliant" by their manufacturers.

The internal architectures of some devices do not easily meet the needs of PCI interface design. For example, many PCI bus signals are bidirectional and must be driven by three-state buffers. Some FPGA and CPLD architectures limit the number of different output enables that may be present on the device. Target interfaces require a minimum of four output enables; initiators require at least six. This is a bare minimum. It does not include the output enables needed for interrupts, controlling byte transactions, or connecting to the back-end logic. Real-world designs require several more output enables. Thus, devices with limited output enable capability are not practical for PCI designs.

Beyond the Basics

There are, of course, many other issues. Can the device deliver the needed performance to operate at any frequency from 0 to 33 MHz? Do the development tools make it easy to control circuit speed along the critical paths? The PCI bus has to attach to something — what are the requirements of the back-end interface? Compliant electrical characteristics are just the first step in selecting a programmable logic device for PCI interface design. Labeling a product as "PCI-compliant" does not ensure suitability for a particular design.

Xilinx does offer several devices that are both electrically compliant and architecturally suitable for PCI interface implementations. These include the XC3100A and new XC4000E FPGA families, as well as the higher-density members of the XC7300 EPLD family. Xilinx components have already been used in a number of successful PCI designs. In fact, the PCI SIG chose a Xilinx XC3100A FPGA for a board included in their BIOS compliance test kit.

For more information about programmable logic products for PCI designs, including application notes and reference designs, please contact us via E-mail at pci@xilinx.com or call your local Xilinx representative.

Copies of the PCI specification can be obtained from the PCI Special Interest Group, P.O. Box 14070, Portland, OR 97214 (tel: 800-433-5177). ◆

MEMBER
PCI LOCAL BUS
SPECIAL INTEREST GROUP

"Xilinx does offer several devices that are both electrically compliant and architecturally suitable."

P.S. Our thanks to the thousands of engineers who joined us for the Programmable Logic Breakthrough '95 seminars this spring. We know your time is valuable and we appreciate your participation

Xilinx Spins Internet Web Site

Many new items have been added recently to the Xilinx webLINX site on the World Wide Web, including technical application notes, FPGA and EPLD data sheets, press releases, training schedules, financial news and stock quotations, and University Program news. An interactive, on-line technical support database and FTP site for file transfers are available as well.

Most Xilinx Web documents are "published" using Adobe Acrobat™. Acrobat displays documents on the screen just as they would appear from a color printer. The Acrobat Reader is available free on the Internet., enabling anyone with Internet Web access to view and print high-quality Xilinx literature directly from the Web.

Look for future additions such as the Xilinx Annual Report, employment opportunity listings as well as current and previous issues of *XCELL*. Other possibilities include a search engine to permit quicker access to all the documents on a given topic and real-time order status. Your feedback is encouraged; if there is a document or feature you'd like to see on the Xilinx Web, please send an E-mail message to webmaster@xilinx.com.

The Xilinx home page on the World Wide Web can be accessed at http://www.xilinx.com. ◆

FINANCIAL RESULTS

Record Revenue and Another Kachina Award

Xilinx revenues rose to a record $125.8 million in the first quarter of fiscal 1996 (ending July 1, 1995). This represents a 15 percent increase from the immediately preceding quarter, and a 67 percent increase from the same quarter last year.

Once again, revenue growth was driven by increasing demand for high-speed XC3100 and XC4000 family products. International sales constituted 36 percent of total revenue; sales from Japan showed the largest increase, benefiting from the strengthened yen.

Xilinx stock split 3-for-1 on August 11, 1995 for shareholders of record as of July 28. The stock split is indicative of the confidence of the Xilinx Board of Directors in the company's ability to maintain continued growth. The stock split will increase the total number of outstanding shares to 70 million. It is the first stock split since the company went public in 1990. Xilinx stock is traded on the NASDAQ exchange under stock symbol XLNX.

Five Consecutive Kachinas

In May, market research firm In-Stat Inc. named Xilinx as the Best Financially Managed IC Company for a record fifth consecutive year. The coveted Kachina Award was presented to Xilinx at In-Stat's annual Semiconductor Forum. (The Kachina Award is a statue carved by the Hopi Indians of Arizona. According to Hopi legend, the Kachina is a warrior who faces great difficulties and shows great strength.)

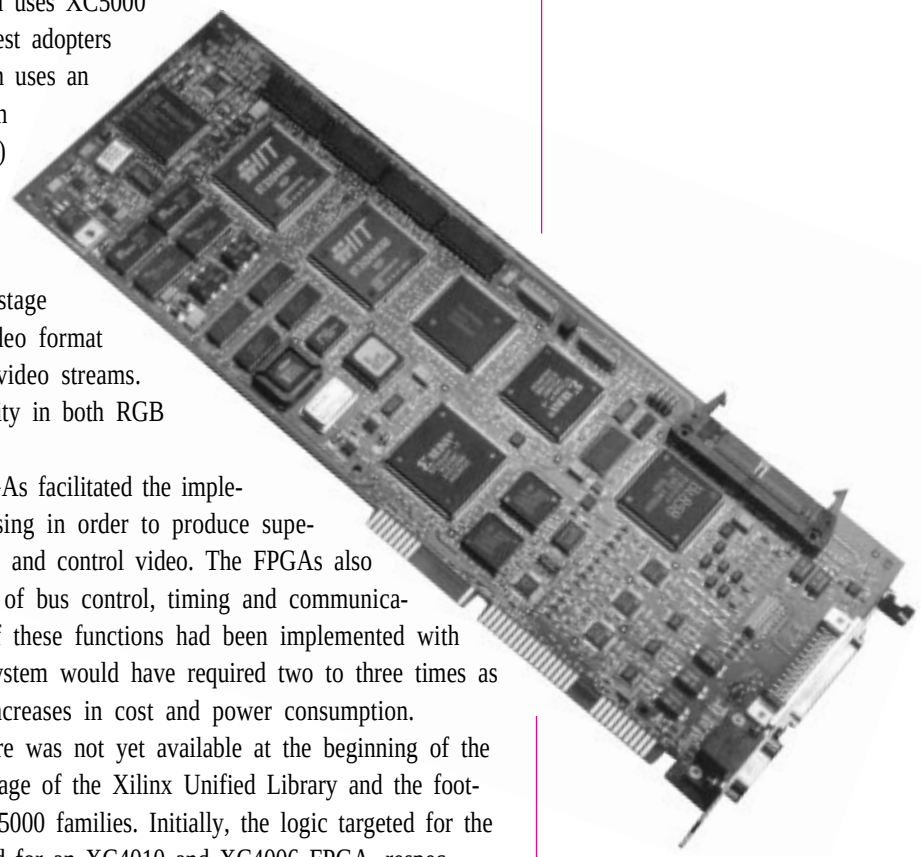
Separate awards are presented for IC companies that do and do not own their own fabrication facilities. The companies are ranked based on criteria such as operating income, net income, return on investment, inventory turnover and sales per employee. Xilinx beat out all other "fabless" companies, including Adaptec, Altera and Lattice Semiconductor. Xilinx has won this award each year since going public in June, 1990. No other semiconductor company, with or without a foundry, has received this award for more than two consecutive years. ◆

Videoconferencing
with XC5000 FPGAs

VTEL Inc. designs and manufactures high-quality, multimedia videoconferencing systems. It is the leading provider of videoconferencing equipment for the remote education and medical industries.

The VTEL systems are based on architectures that employ multiple heterogeneous processor subsystems, interconnected and controlled using custom data paths and control logic. Xilinx FPGAs provide a cost-effective, adaptable solution for implementing this custom hardware, and have been used in several generations of VTEL systems.

VTEL's latest videoconferencing system uses XC5000 family FPGAs, making it one of the earliest adopters of this new FPGA family. The new design uses an XC5210 and an XC5206 device (in 240-pin and 160-pin PQFP packages, respectively) to implement specialized video and communication data pipelines and control logic. The FPGAs contain custom video processing control logic with multistage data pipelines to perform high-quality video format conversions and the adaptive overlay of video streams. Video is processed at near broadcast quality in both RGB and YUV formats.



The flexibility of the SRAM-based FPGAs facilitated the implementation of custom video merge processing in order to produce superior integration of multiple streams of live and control video. The FPGAs also were used to consolidate a large number of bus control, timing and communications signal routing, and test functions. If these functions had been implemented with PALs and/or discrete logic devices, the system would have required two to three times as many circuit boards, with the resulting increases in cost and power consumption.

Since the XC5000 development software was not yet available at the beginning of the design cycle, VTEL engineers took advantage of the Xilinx Unified Library and the footprint-compatibility of the XC4000 and XC5000 families. Initially, the logic targeted for the XC5210 and XC5206 devices was designed for an XC4010 and XC4006 FPGA, respectively. Logic capture, simulation and printed-circuit board layout were completed in this manner. The designs were captured and verified on a Sun workstation using the Viewlogic PowerView schematic editor and ViewSim simulator. Altogether, about six man-months of effort were required to enter, simulate and implement the designs.

Once the XC5000 library was available, the conversion to the XC5000 family parts went smoothly. After some floorplanning of the data path logic, the automatic tools of the XACT- system produced an implementation that exceeded the performance requirements of VTEL's application.

The compatibility between the XC4000 and XC5000 families was exploited again during prototyping and initial system test. The XC5210 FPGA was available when the first

Continued on the next page, see VIDEOCONFERENCING

VTEL
COMMUNICATION WITHOUT BOUNDARIES™

See page 37 for a listing of new application notes.

New Product Literature

Learn about the newest Xilinx products and services through our extensive library of product literature. The most recent pieces are listed below. To order or to obtain a complete list of all available literature, please contact your local Xilinx sales representative. ◆

TITLE	DESCRIPTION	PART NUMBER
FPGAs		
XC4000E Overview	*Features & benefits*	#0010257-01
XC6200 Overview	*Features & benefits*	#0010258-01
XC8100 Overview	*Features & benefits*	#0010254-01
XC8100 Advanced Information	*Technical Data*	#0010193-03
EPLDs		
XC7300 Family Brochure	*Product Overview*	#0010253-01

UPCOMING EVENTS

Look for Xilinx technical papers and/or product exhibits at these upcoming industry forums. For further information about any of these conferences, please contact Kathleen Pizzo (Tel: 408-879-5377 FAX: 408-879-4676). ◆

8th Annual IEEE ASIC Conference (ASIC '95)
Sept. 18-22
Austin, Texas

European Design Automation Conference (EURO-DAC '95)
Sept. 18-22
Brighton, United Kingdom

DSP '95
Oct. 18-20
Paris, France

Photonics East
Oct. 22-26
Philadelphia, Pennsylvania

1995 International Conference on Signal Processing Applications and Technology and DSP World Exhibition (ICSPAT)
Oct. 23-27
Boston, Massachusetts

WESCON
Nov. 7-9
San Francisco, California

International Integrated Circuits Conference
Nov. 8-10
Shanghai, China

Videoconferencing

Continued from page 7

prototype systems were built, but the XC5206 was not, so it was replaced by the pin-compatible XC4006.

The anticipated improved routing capabilities of the XC5000 architecture increased the effective usable capacity enough to allow the inclusion of additional test functions during the latter stages of product development. This additional functionality significantly enhanced board-level product testing capabilities.

VTEL design engineer Richard Glass noted, "Xilinx has provided VTEL with excellent FPGA support through several generations of system designs. VTEL especially values the ease of development and flexibility of the Xilinx FPGA products, which facilitates rapid development and allows incremental design improvement over product life cycles. By using FPGA technology, we have been able to adapt the subsystem designs to meet changing market requirements both during product development and in the field." ◆

Xilinx Ireland Comes On-Line

In keeping with the corporate goal of increasing international sales to half of total revenue, Xilinx has established a major new facility at the Citywest Business Campus in Dublin, Ireland. Construction of the 100,000 square foot manufacturing facility is scheduled to be completed late this year.

The new facility will be used to produce and distribute Xilinx products for Europe and other international markets. It is the company's first wholly-owned manufacturing facility outside of the United States. Besides providing additional capacity for a growing business, Xilinx Ireland provides closer access to European users, ultimately resulting in better service and faster response times.

The new Irish facility will replicate the activities of the company headquarters in San Jose, with the exception of field sales and marketing. Customer service is a key part of the Irish operation; all European orders are being received and processed in Dublin now; all international orders will be processed there by the end of the year.

After the manufacturing and customer service resources are in place, emphasis will be placed on system software testing and quality analysis. Eventually, IC and software design groups will be established. This venture is expected to create more than 300 jobs.

When construction is finally complete late this year, Xilinx Ireland will contain 100,000 square feet of manufacturing and office space.

Operations commenced in a temporary building at the Citywest site in April, starting with the processing of all European distributors' orders. The first product to ship from Ireland was delivered to an Italian distributor in mid-April. Xilinx Ireland is now processing all European and some Asian orders; production capacity will continue to rise throughout the year. The company is undertaking an intensive program to achieve ISO 9002 quality standards certification for the Dublin facility in 1996. ◆

Training Class Update Supports XACT*step*, version 6

The Xilinx training courses are being kept up-to-date with information about the latest products. The standard three-day training course will be updated for XACT*step*™ version 6 as well as the new XC5200 and XC4000E families as soon as the software begins production shipment. Our policy is to always base the course on the latest software versions available to our entire user base.

If you have a design starting now or have an immediate need for training, you should attend the current class. The instructor will be able to point out some of the key changes coming with the next release. Also, a one-day "update" class will be made available at the same time as the XACT*step* version production shipment. This class will be targeted at those who have used the previous version, or who have already attended training. The XC8100 family and its supporting software are also slated for production release this autumn. A class will be available at that time. ***For more information, contact your local sales office, or Xilinx Training at (408) 879-5090, (800) 231-3386x1, or e-mail to customer.training@xilinx.com.*** ◆

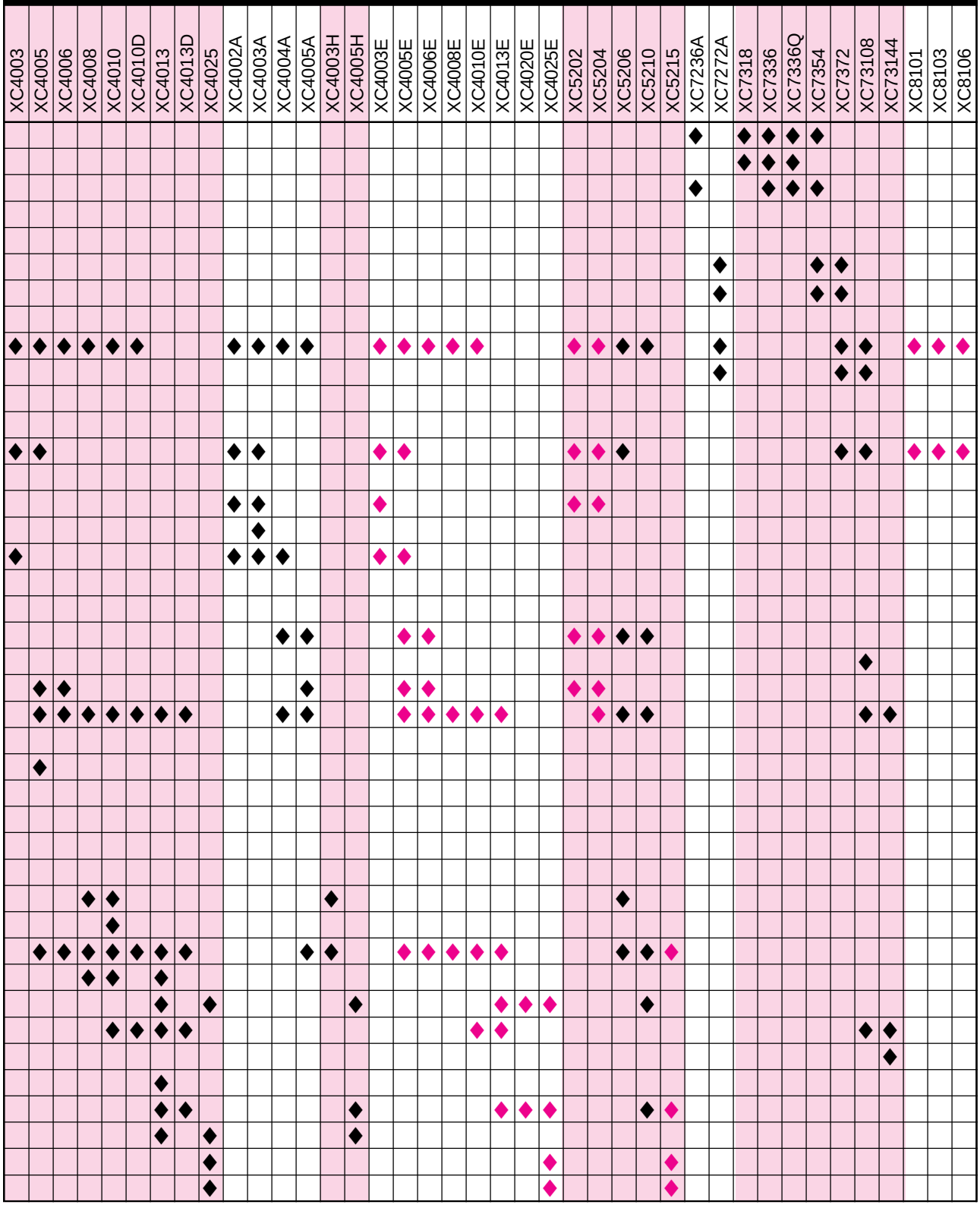
◆ = Product currently shipping or planned

◆ = New since last issue of XCELL

COMPONENT AVAILABILITY CHART

PINS	TYPE	CODE	XC2064	XC2018	XC2064L	XC2018L	XC3020	XC3030	XC3042	XC3064	XC3090	XC3020A	XC3030A	XC3042A	XC3064A	XC3090A	XC3020L	XC3030L	XC3042L	XC3064L	XC3090L	XC3120A	XC3130A	XC3142A	XC3164A	XC3190A	XC3195A
44	PLASTIC LCC	PC44	◆	◆				◆					◆										◆				
	PLASTIC QFP	PQ44																									
	CERAMIC LCC	WC44																									
48	PLASTIC DIP	PD48	◆																								
64	PLASTIC VQFP	VQ64		◆	◆	◆							◆					◆					◆				
68	PLASTIC LCC	PC68	◆	◆	◆		◆	◆				◆	◆									◆	◆				
	CERAMIC LCC	WC68																									
	CERAMIC PGA	PG68	◆																								
84	PLASTIC LCC	PC84		◆		◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆
	CERAMIC LCC	WC84																									
	CERAMIC PGA	PG84		◆			◆	◆	◆			◆	◆	◆								◆	◆	◆			
100	CERAMIC QFP	CQ100					◆		◆																		
	PLASTIC PQFP	PQ100					◆	◆	◆			◆	◆	◆								◆	◆	◆			
	PLASTIC TQFP	TQ100		◆				◆	◆														◆	◆			
	PLASTIC VQFP	VQ100				◆							◆	◆				◆	◆				◆	◆			
	TOP BRZ. CQFP	CB100					◆		◆			◆		◆								◆		◆			
120	CERAMIC PGA	PG120																									
132	PLASTIC PGA	PP132							◆	◆				◆	◆									◆	◆		
	CERAMIC PGA	PG132							◆	◆				◆	◆									◆	◆		
144	PLASTIC TQFP	TQ144												◆	◆				◆	◆				◆	◆		
	CERAMIC PGA	PG144																									
156	CERAMIC PGA	PG156																									
160	PLASTIC PQFP	PQ160								◆	◆				◆	◆									◆	◆	◆
164	CERAMIC QFP	CQ164									◆																
	TOP BRZ. CQFP	CB164									◆					◆										◆	◆
175	PLASTIC PGA	PP175									◆					◆										◆	◆
	CERAMIC PGA	PG175									◆					◆										◆	◆
176	PLASTIC TQFP	TQ176														◆					◆					◆	
184	CERAMIC PGA	PG184																									
191	CERAMIC PGA	PG191																									
196	TOP BRZ. CQFP	CB196																									
208	PLASTIC PQFP	PQ208									◆					◆										◆	◆
	METAL MQFP	MQ208																									
223	CERAMIC PGA	PG223																									◆
225	PLASTIC BGA	BG225																									
	WINDOWED BGA	WB225																									
228	TOP BRZ. CQFP	CB228																									
240	PLASTIC PQFP	PQ240																									
	METAL MQFP	MQ240																									
299	CERAMIC PGA	PG299																									
304	HI-PERF. QFP	HQ304																									

AUGUST 1995


XC4003
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XC4008E
XC4010E
XC4013E
XC4020E
XC4025E
XC5202
XC5204
XC5206
XC5210
XC5215
XC7236A
XC7272A
XC7318
XC7336
XC73360
XC7354
XC7372
XC73108
XC73144
XC8101
XC8103
XC8106

ALLIANCE PROGRAM - COMPANIES & PRODUCTS - SEPTEMBER 1995

Company	Product Name	Version	Function	Design Kit	2K/3K/4K Support	XC5200 Support	EPLD Support	Unified Lib. Support
Acugen	ATGEN	2.60	Automatic Test Generation	AALCA interface	✓	Aug	✓	
	Sharpeye	2.60	Testability Analysis	AALCA interface	✓	Aug	✓	
ALDEC/Susie-CAD	Active-Xilinx	2.0	Schematic Entry/Simulation	Included	✓	✓	✓	✓
	Active-Xlx-State	2.0	Schematic State Editor/ HDL Editor Simulation	Included	✓	✓	✓	✓
	Active-Xlx-Syn	2.0	Schematic State Editor/ HDL Editor Synthesis Sim.	Included	✓	✓	✓	✓
Aptix	System Explorer	2.1	System Emulation	Axess 2.1	✓	✓		
	ASIC Explorer	2.3	ASIC Emulation	Axess 2.3	4K	✓		✓
Cadence (Valid)	Concept	2.0-P7	Schematic Entry	Xilinx Front End	✓	Q4	✓	✓
	Rapidsim	4.2	Simulation	Xilinx Front End	✓	Q4	✓	✓
	Composer	4.3.3	Schematic Entry	Xilinx Front End	✓	Q4	✓	✓
	Verilog	2.2.1	Simulation	Xilinx Front End	✓	Q4	✓	✓
	FPGA Designer	3.3	Synthesis	FPGA Synthesis	✓	Q4	✓	✓
Capilano	DesignWorks	3.1	Schematic Entry/Simulation	XD-1	✓			
Compass	Asic Navigator		Schematic Entry	Xilinx Design Kit	✓	✓		
	QSim		Simulation		✓	✓		
	X-Syn		Synthesis		✓			
Data I/O	ABEL	6.1	Synthesis	XEPLD Fitter			✓	✓
	Synario	2.1	Schematic Entry, Synthesis and Simulation	SYN-LCA SYN-XEPLD	✓	Sep	✓	✓
Escalade	Design Book		Design Entry		✓			✓
Exemplar Logic	Galileo	3.04	Synthesis	Included	✓	✓	✓	✓
Flynn Systems	FS-ATG	2.6	Automatic Test Generation	FS-High Density	✓			
IBM-EDA	Boole-Dozer		Synthesis		✓			
IK Technology	G-DRAW	5.0	Schematic Entry	GDL2XNF	✓			
	G-LOG	4.03	Simulation	XNF2GDL	✓			
Ikos	Voyager	2.10	Simulation	Xilinx Tool Kit	✓			
Incases	Theda	2.0	Schematic Entry	Xilinx Kit	✓			
Intergraph	ACE Plus	12.2	Schematic Entry	Xilinx FPGA Design Kit	3K,4K			✓
	AdvanSIM-1076	12.0	Simulation	Xilinx FPGA Design Kit	3K,4K			✓
	VeriBest Sim	14.0	Simulation	Xilinx FPGA Design Kit	3K,4K	✓		✓
	Veribest DMM	14.0	Design Flow Manager	Xilinx FPGA Design Kit	3K,4K	✓		✓
	VeriBest Syn	14.0	Synthesis	Xilinx FPGA Design Kit	3K,4K	✓		✓
	Synovation	12.2	Synthesis	SynLib	3K,4K			✓
	PLDSyn	12.0	Design entry, synthesis sim.	Included	✓		✓	
ISDATA	LOG/iC2	4.2	Synthesis, simulation	Xilinx Mapper	✓	✓	✓	✓
	LOG/iC Classic	4.2	Synthesis	LCA-PP	✓		✓	
IST	ASYL+	3.21	Synthesis	XNFinterface	✓	✓	✓	✓
ITS	XNF2LAS	1a	Lasar model gen.	XNF2LAS	✓			
Logic Modeling (Synopsys Division)	Smart Model		Simulation Models	In Smart Model Library	✓		✓	
	LM1200		Hardware Modeler	Xilinx Logic Module	✓		✓	
Logical Devices	CUPL	4.5	Synthesis	Xilinx Fitter	✓		✓	
Mentor Graphics	QuickSim II	A.x_F	Simulation	Call Xilinx	✓	✓	✓	✓
	Design Architect	A.x_F	Schematic Entry	Call Xilinx	✓	✓	✓	✓
	Autologic	A.x_F	Synthesis	Xilinx Synthesis Library	✓	✓	✓	✓
MINC	PLDesigner-XL	3.3	Synthesis	Xilinx Design Module	✓			
Minelec	Ulticap	1.32	Schematic Entry	Xilinx Interface	2K,3K			
OrCAD	SDT 386+	1.2	Schematic Entry	Call Xilinx	✓	XACT6	✓	✓
	Capture	6.0	Schematic Entry	Call Xilinx	XACT6	XACT6	XACT6	XACT6
	VST 386+	1.2	Simulation	Call Xilinx	✓		✓	✓
	Simulate	6.0	Simulation	Call Xilinx				
	PLD 386+	2.0	Synthesis	Call OrCAD	✓			
Protel	Advanced Schematic	2.2	Schematic Entry	Xilinx interface	✓		✓	
Quad Design	Motive	4.0	Timing Analysis	XNF2MTV	✓			
Simucad	Silos III	95.100	Simulation	Included	✓			✓
Sophia Systems	Vanguard	5.31	Schematic Entry	Xilinx I/F Kit	✓		✓	
Synopsys	FPGA Compiler	3.3	Synthesis	Call Xilinx	3K,4K	✓	✓	✓
	Design Compiler	3.3	Synthesis	Call Xilinx	✓	✓	✓	✓
	VSS	3.3	Simulation	Call Xilinx	✓	✓	✓	✓

Continued

ALLIANCE PROGRAM - COMPANIES & PRODUCTS - SEPTEMBER 1995 (con't)

Company	Product Name	Version	Function	Design Kit	2K/3K/4K Support	XC5200 Support	EPLD Support	Unified Lib. Support
Synplicity	Synplify Synplify-Lite	2.5 2.5	Synthesis Synthesis	Included Xilinx Mapper	3K,4K 3K,4K			✓ ✓
Teradyne	Lasar	6	Simulation	Xilinx I/F Kit	✓			
Tokyo Electron	ViewCAD	5.0502a	FLDL to XNF translator	XNFGEN	✓			
Topdown Design	V-BAK	1.1	XNF to VHDL translator	XNF interface	✓	✓		✓
transEDA	TransPRO	1.2	Synthesis	Xilinx Library	✓			
VEDA	Vulcan	4.5	Simulation	Xilinx Tool Kit	✓			
Viewlogic	ProCapture ProSim ProSynthesis	6.1 6.1 5.02	Schematic Entry Simulation Synthesis	Call Xilinx Call Xilinx Call Xilinx	✓ ✓ ✓	XACT6 XACT6 XACT6	✓ ✓ ✓	✓ ✓ ✓
Viewpoint	VitalBridge VeriLink	1.0 1.0	Vital VHDL Verilog lib. back-annotation	VHDL I/F kit Verilog I/F kit	✓ ✓			
Visual Software Solutions	StateCAD	2.4	State diagram	Xilinx fitter	✓			
Zycad	Paradigm XP Paradigm RP		Gate-level simulation Rapid prototyping		✓ ✓			

ALLIANCE PROGRAM - PLATFORMS & CONTACTS

Company	Contact Name	*PLATFORM* PC	Sun	RS6000	HP7	Phone Number
Acugen	Peter de Bruyn Kops	✓	✓		✓	603-881-8821
Aldec/Susie-CAD	David Rinehart	✓				702-293-2271
Aptix Corporation	Wolfgang Hoeflich		✓		✓	408-428-6200
Cadence	Itzhak Shapira Jr.		✓	✓	✓	408-428-5739
Capilano Computing	Chris Dewhurst	✓				604-522-6200
Compass Design	Shahid Khan		✓		✓	408-433-4880
Data I/O	Dave Kohlmeier	✓	✓			206-867-6802
Escalade	Jerry Rau		✓	✓		408-481-1336
Exemplar Logic	Stan Ng	✓	✓		✓	510-337-3700
Flynn Systems	Mike Jingozian	✓				603-891-1111
IBM-EDA	John Orfitelli			✓		914-433-9073
IK Technology	Hiroyuki Kataoka				✓	+81-3-3464-5551
Ikos	Brad Roberts		✓		✓	408-366-8509
Incases	Richard Collins				✓	214-373-7344
Intergraph Electronics	Greg Akimoff	✓	✓		✓	415-691-6541
ISDATA	Ralph Remme	✓	✓		✓	+49-721-751087
IST	Gabriele Saucier	✓	✓		✓	+33-76-70-51-00
ITS	Frank Meunier		✓		✓	508-897-0028
Logic Modeling	Marnie McCollow		✓		✓	503-531-2412
Logical Devices	David Mot	✓				303-279-6868
Mentor Graphics	Sam Picken		✓	✓	✓	503-685-1298
MINC	Lynne Dolan	✓	✓		✓	719-590-1155
Minelec (Belgium)		✓				+32-02-4603175
OrCAD	Troy Scott	✓				503-671-9500
Protel Technology	Matthew Schwaiger	✓				408-243-8143
Quad Design Tech.	Vern Potter		✓		✓	805-988-8250
Simucad	Richard Jones	✓				510-487-9700
Sophia Systems	Bob Armstrong	✓	✓		✓	408-943-9300
Synopsys	Lynn Fiance		✓	✓	✓	415-694-4102
Synplicity	Alisa Yaffa	✓	✓		✓	415-961-4962
Teradyne	Mike Jew		✓		✓	617-422-3753
Tokyo Electron	Shige Ohtani					+81-3-5561-7212
TopDown	Art Pisani	✓	✓	✓		603-888-8811
transEDA	James Douglas		✓		✓	+44-1703-255118
VEDA	George Sher		✓		✓	408-496-4516
ViewLogic	Preet Virk	✓	✓	✓	✓	508-480-0881
Viewpoint International	Ramesh Bhimarao	✓	✓		✓	408-954-7370
Visual Software Solutions	Ricky Escoto					305-346-8890
Zycad	David Allenbaugh		✓		✓	510-623-4451

XILINX RELEASED SOFTWARE STATUS - AUGUST 1995

Product Category	Product Description	Product Function	Xilinx Part Number	Previous Ver. Rel.	Current Version By Platform PC1 *6.2*	SN2 *4.1.x*	AP1 *10.4*	HP7 *9.01*	Last Update
XILINX INDIVIDUAL PRODUCTS									
CORE EPLD	XC7K Support	Core Implementation	DS-550-xxx	5.02	5.11	5.10		5.10	01/95
Floorplanner[4]	Hi-Density Des. Kit	Core Implementation	ES-HD4K-SN2	N/A		5.10			N/A
Mentor[2]	A.1-F	I/F and Libraries	DS-344-xxx	5.02		5.11	5.10	5.11	05/95
OrCAD[2]		I/F and Libraries	DS-35-xxx	5.00	5.10				01/95
Synopsys[2]		I/F and Libraries	DS-401-xxx	3.20		3.30		3.30	06/95
Viewlogic[2]	ProCapture	I/F and Libraries	DS-390-xxx	5.02	5.11				05/95
Viewlogic[2]	ProSim	I/F and Libraries	DS-290-xxx	5.02	5.11				05/95
Viewlogic[2]		I/F and Libraries	DS-391-xxx	5.10	5.11	5.11		5.11	01/95
XABEL[2]		Entry, Sim, Lib, Opt.	DS-371-xxx	5.00	5.10	5.10			01/95
X-BLOX[1]		Module Generation & Opt.	DS-380-xxx	5.00	5.10	5.10		5.10	01/95
Verilog[4]	2K, 3K, 4K, 7K Lib.	Models & XNF Trans.	ES-VERILOG-xxx			1.00		1.00	N/A
XILINX PACKAGES									
Cadence	Standard		DS-CDN-STD-xxx			5.11		5.11	05/95
Mentor 8	Standard		DS-MN8-STD-xxx	5.02		5.11	1.10	5.11	05/95
Mentor	Advanced[5]		DS-MN8-ADV-xxx	N/A		7.00		7.00	N/A
OrCAD	Base		DS-OR-BAS-PC1	5.02	5.10				01/95
OrCAD	Standard		DS-OR-STD-PC1	5.02	5.10				01/95
Synopsys	Standard		DS-SY-STD-xxx	5.11		5.12		5.12	06/95
Synopsys	Advanced[5]		DS-SY-ADV-xxx	N/A		7.00		7.00	N/A
Viewlogic	Base		DS-VL-BAS-PC1	5.02	5.11				05/95
Viewlogic	Standard		DS-VL-STD-xxx	5.02	5.11	5.11		5.11	05/95
Viewlogic	Advanced[5]		DS-VL-ADV-xxx	N/A	7.00	7.00		7.00	N/A
Viewlogic/S	Base		DS-VLS-BAS-PC1	5.02	5.11				05/95
Viewlogic/S	Standard		DS-VLS-STD-PC1	5.02	5.11				05/95
Viewlogic/S	Extended[3]		DS-VLS-EXT-PC1	5.02	5.11				05/95
Viewlogic/S	Advanced[5]		DS-VLS-ADV-PC1	N/A	7.00				N/A
XC5000 Pre-Rls.[4]	Standard	Core + VL Libraries	PR-VL-STD-xxx-5K	1.00	2.00	2.00		2.00	4/95
XC5000 Pre-Rls.[4]	Standard	Core + MN8 Libraries	PR-MN8-STD-xxx	N/A		2.00		2.00	N/A
XC8000	Extended	8K Core + Synthesis Libs.	DS-8000-EXT-xxx			1.00		1.00	N/A
3rd Party	Standard	FPGA/EPLD Core	DS-3PA-STD-xxx	N/A	5.10	5.10		5.10	N/A
3rd Party Alliance	Advanced[5]		DS-3PA-ADV-xxx	N/A	7.00	7.00		7.00	N/A
XILINX HARDWARE									
Device Pgmr.	PROM/EPLD/ XC8100 Pgmr.		HW-130		1.0	3Q95		3Q95	N/A
THIRD PARTY PRODUCTION SOFTWARE VERSIONS									
Cadence	Composer	Schematic Entry	N/A	4.3		4.3.3		4.3.3	N/A
Cadence	Verilog	Simulation	N/A	2.1		2.1.2		2.1.2	N/A
Cadence (Valid)	Concept	Schematic Entry	N/A	1.7		1.7-P4		1.7-P4	N/A
Cadence (Valid)	Rapidsim	Simulation	N/A	4.10		4.2		4.2	N/A
Mentor	Design Architect	Schematic Entry	N/A	8.2_5		A.1-F	A.1-F	A.1-F	N/A
Mentor	QuickSim II	Simulation	N/A	8.2_5		A.1-F	A.1-F	A.1-F	N/A
OrCAD	SDT 386+	Schematic Entry	N/A	1.10	1.20				N/A
OrCAD	VST 386+	Simulation	N/A	1.10	1.20				N/A
Synopsys	FPGA/Design Comp.	Synthesis	N/A	3.2b		3.3a	3.3a	3.3a	N/A
Viewlogic	ProCapture	Schematic Entry	N/A		6.1	5.3		5.3	N/A
Viewlogic	ProSim	Simulation	N/A		6.1	5.3		5.3	N/A
Data I/O	ABEL Compiler	Entry and Simulation	N/A		6.1	6.0			N/A
Data I/O	Synario	Entry and Simulation	N/A		2.1				N/A

NOTE: [1]FPGA only. [2]FPGA and EPLD. [3]Includes ViewSynthesis v2.3.1.
[4]Engineering software by request only. [5]Integrates NeoCAD Foundry tools.

PROGRAMMER SUPPORT FOR XILINX XC1700 SERIAL PROMS — AUGUST 1995

MANUFACTURER	MODEL	1736A/ 1765	17128	1736D/ 1765D	1716L/ 1765L	17128D	17256D	DIP8	PC20	SO8
ADVANTECH	PC-UPROG		V2.1	V2.0	V2.0	V2.1	V2.1	X		
	LABTOOL-48		V1.0	V1.0	V1.0	V1.0	V1.0	X	PLCC2020-01	
ADVIN	PILOT-U24	10.53	10.76C	10.71	10.77	10.78B	10.78B	X	PX-20	SO-8
	PILOT-U28	10.53	10.76C	10.71	10.77	10.78B	10.78B	X	PX-20	SO-8
	PILOT-U32	10.53	10.76C	10.71	10.77	10.78B	10.78B	X	PX-20	SO-8
	PILOT-U40	10.53	10.76C	10.71	10.77	10.78B	10.78B	X	PX-20	SO-8
	PILOT-U84	10.53	10.76C	10.71	10.77	10.78B	10.78B	X	PX-20	SO-8
	PILOT-142	10.73	10.76C	10.73	10.77	10.78B	10.78B	AM-1736	PX-20	SO-8
	PILOT-143	10.73	10.76C	10.73	10.77	10.78B	10.78B	AM-1736	PX-20	SO-8
	PILOT-144	10.73	10.76C	10.73	10.77	10.78B	10.78B	AM-1736	PX-20	SO-8
	PILOT-145	10.73	10.76C	10.73	10.77	10.78B	10.78B	AM-1736	PX-20	SO-8
AVAL	PECKER-50		C	C				X		
	PKW5100		C	C				X		
B&C MICROSYSTEMS INC.	Proteus-UP40	V3.4e	V3.4e	V3.5f	V3.7f	V3.7I	V3.7I	X	AMUPLC84	
BP MICROSYSTEMS	CP-1128	C	V2.17*	V2.21c*	V2.34*	V3.06	V3.06	FH28A	FH28A + 3rd Party	FH28A + 3rd Party
	EP-1140	C	V2.17	V2.21c	V2.34	V3.06	V3.06	FH40A	FH40A + 3rd Party	FH40A + 3rd Party
	BP-1200	C	V2.17	V2.21c	V2.34	V3.06	V3.06	SM48D	SM20P or SM84UP	3rd Party
BYTEK	135H-FT/U	V42	V51	V51	V51			TC-824D		
	MTK-1000	V42	V51	V51	V51			TC-824D		
	MTK-2000	V42	V51	V51	V51			TC-824D		
	MTK-4000	V42	V51	V51	V51			TC-824D		
DATA I/O	UniSite/Site 40/48	V4.0	V4.1	V4.1	V4.6	V4.8	V4.8	X	USBASE-PLCC	USBASE-SOIC
	UniSite/ChipSite	V4.0	V4.1	V4.1	V4.6	V4.8	V4.8	X	USBASE-PLCC	USBASE-SOIC
	UniSite/PinSite	V4.0	V4.1	V4.1	V4.6	V4.8	V4.8	X	USBASE-PLCC	USBASE-SOIC
	2900	V2.1	V2.2	V2.2	V3.4	V3.6	V3.6	X	2900-PLCC	2900-SOIC
	3900	V1.5	V1.6	V1.6	V2.4	V2.6	V2.6	0101	3900-PLCC	3900-SOIC
	AutoSite	V1.5	V1.6	V1.6	V2.4	V2.6	V2.6	DIP-300-1	PLCC-20-2	
	UniPak 2B	V24						351B120		
	ChipLab	V1.1	V1.0	V1.0	V1.1			X		080801S300
DEUS EX MACHINA	XPGM		V1.00	V1.00	V1.00	V1.10	V1.10	Adapter 0	Upgrade to Adapter 0	Adapter 16
ELECTRONIC ENGINEERING TOOLS	ALLMAX/ALLMAX+	V1.3	V1.5	V1.5	V1.5	V2.3	V2.3	X		
	PROMAX	V2.34	V2.34	V2.34	V2.34	V2.34	V2.34	X	Module #4	
ELAN DIGITAL SYSTEMS	3000-145	C	C					A116		
	5000-145	C	C					A116		
	6000 APS	K2.01	K2.02	K2.01	K2.10	K2.14	K2.14	X	PDi84UPLC	PDi16USOI
HI-LO SYSTEMS RESEARCH	All-03A	V3.30	V3.30	V3.30	V3.30	V3.50	V3.50	X	CNV-PLCC-XC1736	CVN-SOP-NDIP16
	All-07	V3.30	V3.30	V3.30	V3.30	V3.47	V3.47	PAC-DIP40	PAC-PLCC44	
ICE TECHNOLOGY LTD	Micromaster 1000/1000E	V1.1	V3.00	V3.00	V3.07	V3.00	V3.00	X	AD-1736/65-PLCC	
	Speedmaster 1000/1000E	V1.1	V3.00	V3.00	V3.07	V3.00	V3.00	X	AD-1736/65-PLCC	
	Micromaster LV		V3.00	V3.00	V3.00	V3.00	V3.00	X		
	LV40 Portable		P 3Q95	P 3Q95	P 3Q95	P 3Q95	P 3Q95	X		
	Speedmaster LV		V3.00	V3.00	V3.00	V3.00	V3.00	X		
LINK COMPUTER GPHX	CLK-3100	V5.08	V5.08	V5.08				X17XXB	PLCC-17XX	SOIC-16
LOGICAL DEVICES	ALLPRO-40	V2.2						X	OPTPLC-208	OPTSOI-080
	ALLPRO-88	V2.2	V2.3	V2.3		V2.5	V2.5	X		OPTSOI-080
	ALLPRO-88XR	V1.1	V2.3	V1.3		V2.3	V2.3	X		OPTSOI-080
	CHIPMASTER 3000	V2.0	V2.1	V2.0	V2.3			X	OPTPLC-208	OPTSOI-080
	CHIPMASTER 5000	V1.15						X	OPTPLC-208	OPTSOI-080
	XPRO-1	V1.01	V1.01	V1.01	V1.01			MODXLN-173	MODXLN-173	MODXLN-173
MQP ELECTRONICS	MODEL 200	C	6.45	6.45	6.45	6.46	6.46	AD13A-16		
	SYSTEM 2600		P 3Q95	P 3Q95	P 3Q95	P 3Q95	P 3Q95	MP6		
	PINMASTER 48		P 3Q95	P 3Q95	P 3Q95	P 3Q95	P 3Q95	X		
MICRO PROSS	ROM 5000 B	C	V1.70	V1.70	V1.80	V1.80	V1.80	Mu 40		
	ROM 3000 U	C	V3.60	V3.60	V3.70	V3.70	V3.70			
	ROM 9000				V1.5	V1.5	V1.5			
NEEDHAM'S ELECTRONICS	EMP20	V1.5	V1.5	V2.37	V2.37	V2.37	V2.37	04B		
RED SQUARE	IQ-180	C	V9.2	V8.2	V9.2	V9.2	V9.2			
	IQ-280	C	V9.2	V8.2	V9.2	V9.2	V9.2			
	Uniwriter 40	C	V9.2	V8.2	V9.2	V9.2	V9.2			
	Chipmaster 5000	C	V9.2	V8.2	V9.2	V9.2	V9.2			
RETNEL SYSTEMS	ZAP-A-PAL	C		V3.8J				Module #36		
SMS	Expert	B/93	A/94	A/94	A1/94	Cx/94	Cx/94	TOP40DIP	TOP1PLC or	
	Optima	B/93	A/94	A/94	A1/94	Cx/94	Cx/94	"	TOP3PLC/TOP3PLC	
	Multisyte			A/94		Cx/94	Cx/94	"	"	
	Plus48	B/93	A/94	A/94	A1/94					
	Sprint Plus	B/93	A/94							
STAG	Eclipse		4.4	V2.2	V4.3	V4.10.31	V4.10.31	EPU48D	EPU84P	
	Quasar	10.76C	10.76C	V10.76C	V10.76C	V10.78B	V10.78B	X	AMPLCC20	
SUNRISE	T-10 UDP	V3.31	V3.31	V3.31	V3.31	V3.31	V3.31	X	X	X
	T-10 ULC	V3.31	V3.31	V3.31	V3.31	V3.31	V3.31	X	X	X
SUNSHINE	POWER-100	V8.18	V8.18	V8.18	V8.18	V8.18	V8.18	X		
	EXPRO-60/80	V8.18	V8.18	V8.18	V8.18	V8.18	V8.18	X		
SYSTEM GENERAL	TURPRO-1	V2.21F	V2.21F	V2.21F	V2.21F	V2.21F	V2.21F	DIP-Adapter	P20-Adapter	
	Turpro-1 F\X	V2.21F	V2.21F	V2.21F	V2.21F	V2.21F	V2.21F	DIP-Adapter	P20-Adapter	
	APRO	C	V2.14	V2.01	V2.12	S 2Q95	S 2Q95	X	X	
TRIBAL MICROSYSTEMS	TUP-300	C	V3.31	V3.31	V3.37C	V3.47	V3.47	X	CNV-PLCC-XC1736	
	TUP-400	C	V3.31	V3.31	V3.37C	V3.50	V3.50	X	"	
	FLEX-700	C	V3.31	V3.31	V3.37C	V3.47	V3.47	X	"	
XELTEK	SuperPRO	1.5B	1.7C	1.7D	1.8	2.2A	2.2A	X*	20-PL/8-D-ZL-XC1736	16SO15/D6-ZL
	SuperPRO II	1.5B	1.7C	1.7D	1.8	2.2A	2.2A	X*	20-PL/8-D-ZL-XC1736	16SO15/D6-ZL
XILINX	HW-112	C	V3.11	V3.31	V3.31	V5.0.0	V5.0.0	X	HW-112-PC20	HW-112-SO8
	HW-120	V5.00	V5.00	V5.00	V5.00	P 6/95	P 6/95	HW-120-PRM	HW-120-PRM	HW-120-PRM
	HW-130		V1.00	V1.00	V1.00	V1.00	V1.00	HW-137-DIP8	S 5/95	S 5/95

C = Currently Supported, P = Planned, S = Scheduled Release Date, X=Package Supported; WHITE = change since last issue

Programmer Support for Xilinx XC7200 EPLDs — August 1995

VENDOR	MODEL	7236	7236A	7272	7272A	PC44	PC68	PC84	PG84	Comments
Advantech	PC-UPROG LabTool-48	V2.4 V1.0	V2.4 V1.0	V2.4 V1.0	V2.4 V1.0	X SDP-UNIV-44	SDP-7272-68 SDP-7272-68	SDP-7272-84 SDP-7272-84		
Advin Systems	Pilot-U40 Pilot-U84	10.77E 10.77E	10.77E 10.77E	10.77E 10.77E	10.77E 10.77E	USA-84 USA-84	USA-84 USA-84	USA-84 USA-84	 AM-XC84G	
B&C Microsystems, Inc.	Proteus	V3.6j	V3.6j	V3.7h	V3.7h	AMUPLC84	AMUPLC84	AMUPLC84		
BP Microsystems	BP-1200	v2.32	v2.32	v2.34	v2.34	SM44P	SM68P or SM84UP	SM84P or SM84UP	SM84UGA	
DATA I/O	UniSite 2900 3900 AutoSite	v4.3 V3.4* v2.1 V2.4*	v4.6* V3.4* V2.4* V2.4*	v4.5 v2.3 v2.3	v4.5** v2.3** v2.3**	USBASE-PLCC PPI-0243 3900-PLCC PLCC-44-1	USBASE-PLCC PPI-0246 3900-PLCC PLCC-68-1	USBASE-PLCC PPI-0208 3900-PLCC PLCC-84-1		*7236A=PPI-0243 **7272A=PPI-0246 (PC68) **7272A=PPI-0247 (PC84)
Deus Ex Machina	XPGM	V1.00	V1.00	V1.00	V1.00	Adapter 1	Adapter 2	Adapter 3		
Elan Digital Systems	6000 APS	K2.04	K2.04	K2.06	K2.06	PDi84UPLC	PDi84UPLC	PDi84UPLC	PDi84PGx	
Electronic Engineering Tools	ALLMAX/ALLMAX+ PROMAX	V2.1 V2.34	V2.1 V2.34	V2.1 P 6/95	V2.1 P 6/95	Module 05+PA44-84U Module 19 + H44	PA68-48A	PA84-48A		
Hi-Lo Systems Research	All-03A All-07	V3.01 V3.01	V3.01 V3.01	V3.00 V3.00	V3.00 V3.00	ADP-XC7236-PL44 PAC-PLCC44	ADP-XC7272-PL68 PAC-PLCC68	ADP-XC7272QPI-84		
ICE Technology Ltd.	Micromaster 1000/E Speedmaster 1000/E Micromaster LV Speedmaster LV	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	AD-XC7236-PLCC-44 AD-XC7236-PLCC-44 AD-XC7236-PLCC-44 AD-XC7236-PLCC-44	AD-XC7272-PLCC-68 AD-XC7272-PLCC-68 AD-XC7272-PLCC-68 AD-XC7272-PLCC-68	AD-XC7272-PLCC-84 AD-XC7272-PLCC-84 AD-XC7272-PLCC-84 AD-XC7272-PLCC-84		
Logical Devices	ALLPRO-88 ALLPRO-88XR XPRO-1	2.2 1.35 1.01	V2.4 V2.4 1.01	2.2 1.35 1.01	V2.4 V2.4 1.01	C C MODXP1-44L	C C MODXP1-68L	C C MODXP1-84L	 MODXP1-84G	
Micropross	ROM 9000	P 3Q95	P 3Q95	P 3Q95	P 3Q95					
MQP Electronics	SYSTEM2000 PINMASTER48	P 3Q95 P 3Q95	P 3Q95 P 3Q95	P 3Q95 P 3Q95	P 3Q95 P 3Q95	MP1	MP1	MP1		 Universal Programmer
Needham's Electronics	EMP20	V2.37	V2.37	V2.37	V2.37	19A+H44	20A+U68CB	20A+U84CB		
Stag	Eclipse	V5.7.3	V5.7.3	V5.7.3	V5.7.3	EPU84P+	EPU84P+	EPU84P+		
SMS	Expert Optima Multisyte	A1/94 A1/94 A1/94	A1/94 A1/94 A1/94	A1/94 A1/94 A1/94	A1/94 A1/94 A1/94	TOP1 TOP1 TOP1	TOP1 TOP1 TOP1	TOP1 TOP1 TOP1		
Sunrise Electronics	T-10 UDP T-10 ULC	V3.31 V3.31	V3.31 V3.31	V3.31 V3.31	V3.31 V3.31	X X	X X	X X	X X	All adapters are custom All adapters are custom
Sunshine Electronics	POWER-100 EXPRO-60/80	V8.16 V8.16	V8.16 V8.16			CNV-UNIVERSAL-PLCC44 CNV-UNIVERSAL-PLCC44				
System General	TURPRO-1 TURPRO-1 F\X	v2.12 v2.12	v2.12 v2.12	v2.12 v2.12	v2.12 v2.12	P44 P44	P68 P68	P84 P84		
Tribal Microsystems	TUP-300 TUP-400 FLEX-700	v3.0 v3.0 v3.0	v3.0 v3.0 v3.0	v3.0 v3.0 v3.0	v3.0 v3.0 v3.0	TUP-7236 TUP-7236 TUP-7236	TUP-7272 TUP-7272 PAC-PLCC68			 PAC-PLCC44
Xeltek	SUPERPRO SUPERPRO II	1.7C 1.7C	2.2 2.2	2.1 2.1	2.1 2.1	XXC7236-44PL/40D XXC7236-44PL/40D	XXC7272-68PL/68D XXC7272-68PL/68D	XXC7272-84PL/84D XXC7272-84PL/84D		
Xilinx	HW-120 HW-130	V3.14 V1.00	V3.14 V1.00	V3.14 S 5/95	V3.14 S 6/95	HW-120-PC44 HW-132-PC44*	HW-120-PC68 S 5/95*	HW-120-PC84 S 5/95*	HW-120-PG84	*HW-12x EPLD adapters can be used on HW-130

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PROGRAMMER SUPPORT FOR XILINX XC7300 EPLDS — AUGUST 1995

VENDOR	MODEL	7318	7336	7354	7372	73108	73144	PC44	PC68	PC84	PQ44	PQ100	PG144	PQ160	PG184	BG225
ADVANTECH	PC-UPROG LabTool-48	V2.4 V1.0	V2.4 V1.0	V2.4 V1.0	 V1.04	 V1.04	P 3Q95 P 3Q95	X SDP-UNIV-44	SDP-7354-68 SDP-7354-68	 X						
ADVIN SYSTEMS	PILOT-U40 PILOT-U84	10.78N 10.78B	10.78N 10.78B	10.78N 10.78B	10.78N 10.78B	10.79 10.79	P 3Q95 P 3Q95	USA-84 USA-84	USA-84 USA-84	USA-84 USA-84		AM-XC100Q AM-XC100Q	AM-XC144G AM-XC144G	AM-XC160Q AM-XC160Q		
B&C MICROSYSTEMS	Proteus	3.7k	3.7k	3.7k	P 3Q95	3.7k	P 3Q95	C	C	C						
BP MICROSYSTEMS	BP-1200	V3.01	V3.01	V3.01	V3.07	V3.06A		SM44P		FHSM84PX						
DATA I/O	2900 3900 UniSite AutoSite	V3.5 V2.5 V4.7 V2.5	V3.5 V2.5 V4.7 V2.5	V3.5 V2.5 V4.7 V2.5	 V2.6 V4.8 V2.6	 V2.6 V4.8 V2.6	 P 3Q95 P 3Q95 P 3Q95	2900-PLCC 3900-PLCC USBASE-PLCC PLCC-44-1	 3900-PLCC USBASE-PLCC PLCC-68-1	 3900-PLCC USBASE-PLCC PLCC-84-1	0529 0529 0529 0529	 0557 0557		 0558 0558		 PPI-1101 PPI-1101 PPI-1101
DEUS EX MACHINA	XPGM	V1.00	V1.00	V1.00	V1.10	V1.10	P 3Q95	Adapter 5	Adapter 6 (13 for 7372)	Adapter 7				Adapter 9		
ELECTRONIC ENGIN- EERING TOOLS	ALLMAX/ALLMAX+ PROMAX	V2.1 V2.34	V2.1 V2.34	V2.1 V2.34	V2.1 V2.57		P 3Q95 P 3Q95	Module 04+PA44-48U Module #19 + H44	PA68-48B (7354) PA68-48C (7372)	PA84-48B						
ELAN	6000 APS	k2.13	k2.13	k2.13	k2.13	k2.13	P 3Q95	PDi84UPLC	PDi84UPLC	PDi84UPLC	PDi044QFx	PDi100QFx	PDi160QFx		PDi225BGx	
HI-LO SYSTEMS RESEARCH	All-03A All-07	V3.04 V3.02	V3.04 V3.02	V3.04 V3.02	V3.05 V3.01	V3.01 V3.00	P 3Q95 P 3Q95	ADP-XC7336-PL44 PAC-PLCC44	ADP-XC7372-PL68 PAC-PLCC68	ADP-XC73108-PL84						
ICE TECHNOLOGY LTD	Micromaster 1000/E Speedmaster 1000/E Micromaster LV Speedmaster LV	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	P 3Q95 P 3Q95 P 3Q95 P 3Q95	AD-73XX-PLCC-44 AD-73XX-PLCC-44 AD-73XX-PLCC-44 AD-73XX-PLCC-44	AD-7354-PLCC-68 AD-7372-PLCC-68 AD-7354-PLCC-68 AD-7372-PLCC-68 AD-7354-PLCC-68 AD-7372-PLCC-68 AD-7354-PLCC-68 AD-7372-PLCC-68	AD-73XX-PLCC-44 AD-73XX-PLCC-44 AD-73XX-PLCC-44 AD-73XX-PLCC-44						
LOGICAL DEVICES	ALLPRO-88 ALLPRO-88XR XPRO-1	V2.5 V2.5 1.01	V2.5 V2.5 1.01	V2.5 V2.5 1.01	V2.5 V2.5 1.01	V2.5 V2.5 1.01	P 3Q95 P 3Q95 P 3Q95	C C MODXP1-5444L	C C MODXP1-5468L	C C MODXP1-108L				MODXP1-160Q	MODXP1-184G	MODXP1-108B
MICROPROSS	ROM 9000	P 3Q95	P 3Q95	P 3Q95	P 3Q95	P 3Q95	P 3Q95									
MQP ELECTRONICS	SYSTEM 2000 PINMASTER 48	P 3Q95 P 3Q95	P 3Q95 P 3Q95	P 3Q95 P 3Q95	P 3Q95 P 3Q95	P 3Q95 P 3Q95	P 3Q95 P 3Q95	MP1	MP1	MP1						
NEEDHAM'S ELECTRONICS	EMP20	V2.37	V2.37	V2.37	V2.37	V2.37	P 3Q95	19B + H44	20A + U68CA	20A + U84CA						
SMS	EXPERT OPTIMA	C/94 C/94	C/94 C/94	C/94 C/94	P 2Q95 P 2Q95	P 2Q95 P 2Q95	P 3Q95 P 3Q95	TOP1 TOP1	TOP1 TOP1	TOP1 TOP1						
STAG	ECLIPSE	V4.10.31	V4.10.31	V4.10.31	V4.10.31	V4.10.31	P 3Q95									
SUNRISE	T-10 UDP T-10 ULC	V3.31 V3.31	V3.31 V3.31	V3.31 V3.31	V3.31 V3.31	V3.31 V3.31	P 3Q95 P 3Q95	X X	X X	X X						
SUNSHINE	POWER-100 EXPRO-60/80	P 5/95 P 5/95	P 5/95 P 5/95		P 5/95 P 5/95	P 5/95 P 5/95	P 3Q95 P 3Q95	CNV-UNIVERSAL-PLCC44 CNV-UNIVERSAL-PLCC44								
SYSTEM GENERAL	TURPRO-1	V2.2	V2.2	V2.2	V2.2	V2.2	P 3Q95	C								
TRIBAL MICROSYSTEMS	ALL-07	V3.02	V3.02	V3.02	V3.01	V3.00	P 3Q95	PAC-PLCC44	PAC-PLCC68							
XELTEK	SUPERPRO SUPERPRO II	2.1 2.1	2.2A 2.2A	2.1 2.1	2.2B 2.2B	P 3Q95 P 3Q95	P 3Q95 P 3Q95	XXC7354-44PL/40D XXC7354-44PL/40D	XXC7354-68PL/40D XXC7354-68PL/40D							
XILINX	HW-120 HW-130	V5.00 V1.00	V5.00 V1.00	V5.00 V1.00	V5.00 S 5/95	V5.00 S 5/95	P 6/95 S 5/95	HW-126-PC44 HW-133-PC44	HW-126-PC68	HW-126-PC84	HW-126-PQ44	HW-126-PQ100	HW-126-PG144	HW-126-PQ160	HW-126-PG184	HW-126-BG225

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The High-Performance XC4000E Family

New Family Achieves 50 Percent Performance Increase Over the Popular XC4000 Family

Xilinx has begun shipping the new XC4000E family, the successor to the popular XC4000 FPGA family. The XC4000E FPGA family increases performance over the existing XC4000 family by up to 50 percent, and is ideal for high-density, high-performance applications such as microprocessor bus interfacing, digital signal processing, image processing, and high-speed telecommunications.

This dramatic performance improvement results from an improved design, a new 0.5µ triple-layer-metal process technology, and the new Select-RAM™ on-chip memory feature. The XC4000E family features eight devices ranging from 3,000 to 25,000 gates, including the XC4020E device, the first 20,000 gate device offered by Xilinx. (Higher-density devices will be announced later this year.) Since the XC4000E family is based on the XC4000 family architecture, XC4000E devices are backward compatible (i.e., drop-in, with the same bitstream) with the equivalent XC4000 devices.

Unique capabilities and features of the XC4000E FPGAs include:

- Up to 50 percent faster circuit speed (XC4000E-2 as compared to XC4000-4; *see table on page 24)*
- 60 percent faster carry chain for arithmetic functions
- Lower component prices than the XC4000 family
- Select-RAM memory reduces chip count and design time while increasing RAM performance by up to 2X
- Select-RAM memory is mode-selectable
  - synchronous/asynchronous
  - single-port/dual-port
- 100 percent PCI compliant and suitable

Architectural Features of the XC4000E

The architecture of the XC4000E is a superset of the XC4000; XC4000E devices are bitstream and pin-compatible with the equivalent XC4000 family FPGAs. Thus, current designs using XC4000 FPGAs can take immediate advantage of the XC4000E's increased speed by simply inserting new devices into existing XC4000 sockets.

The XC4000E architecture features an enhanced CLB (configurable logic block) with several new modes for configuring on-chip memory (called Select-RAM). As with the XC4000 architecture, the CLB's look-up tables optionally can be used as

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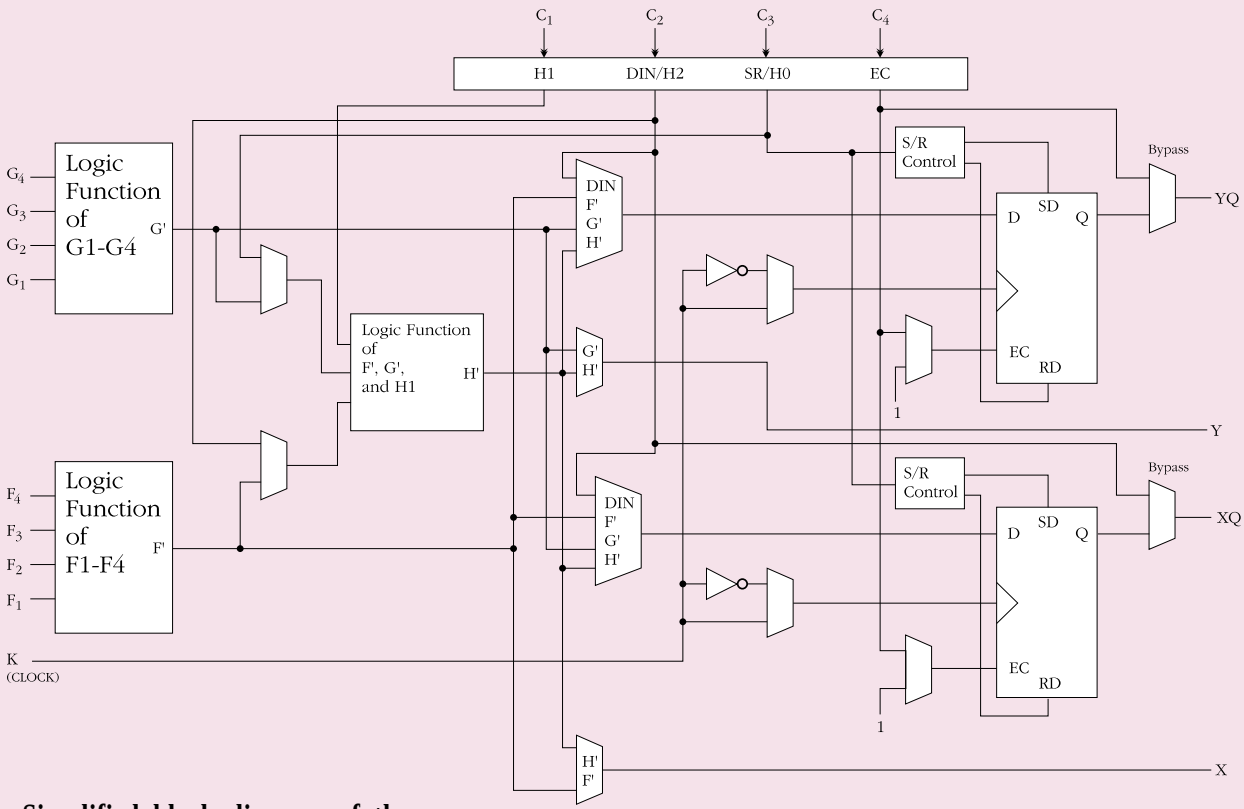
on-chip ROM or RAM memory; memory blocks of any size or width can be constructed from multiple CLBs and located anywhere in the array. The XC4000E extends that flexibility by adding an optional synchronous (edge-triggered) mode that simplifies the timing of the memory interface, and an optional dual-port mode that supports simultaneous read and write functions. Furthermore, the memory cells can be programmed during device operation or initialized as part of FPGA configuration. The synchronous and dual-port RAM modes ease the implementation of embedded configuration registers and on-chip data buffering in applications such as local area networking (LAN) switches, Peripheral Component Interconnect (PCI) bus interfaces, and asynchronous transfer mode (ATM) controllers.

Additionally, the routing scheme of the XC4000E architecture was redesigned and optimized to improve CLB access and increase routing connectivity through the addition of more routing switches. New paths also were added within the CLB; the H function generator has two additional sources for inputs *(see figure)*. This new architecture improves utilization and provides shorter wire lengths, thereby reducing interconnect delay.

Other new features include built-in clock enables for the registers in the I/O blocks, programmable TTL or CMOS input voltage thresholds and output levels, and "Soft Start-Up," a feature that activates the

See XC4000E, page 24



Simplified block diagram of the XC4000E CLB (RAM and Carry Logic functions not shown)

The XC8100 FPGA Family

The new XC8100 family is Xilinx's first single-chip, one-time-programmable FPGA family, based on the MicroVia™ antifuse process. There are four initial members in the family *(see table 1)*, and samples are available now for the XC8101-1, XC8103-1 and XC8106-1 devices.

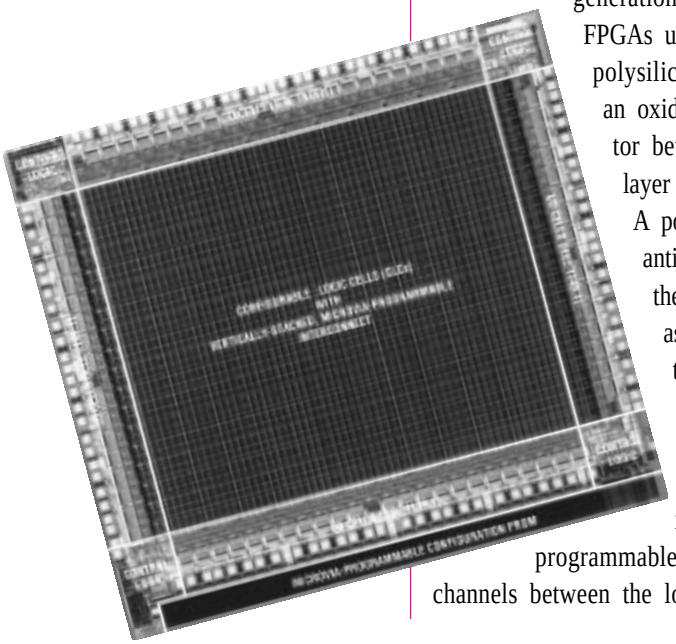
Table 1: *XC8100 FPGA family members*

	XC8101	XC8103	XC8106	XC8109
Capacity (gates)	1200	3300	5600	8700
Cells	384	1024	1728	2688
Flip-flops (max)	182	512	864	1344
I/O	80	128	168	208

MicroVia

The new MicroVia technology combines a three-layer-metal CMOS process, a metal-to-metal antifuse programming element and a sea-of-gates architecture. The combination of these three elements allows the development of FPGAs with extensive routing resources and high gate utilization in a very small die size.

Antifuse programming elements are non-conductive until programmed. Earlier generations of antifuse-based FPGAs use a transistor-type, polysilicon antifuse wherein an oxide forms an insulator between a polysilicon layer and the silicon die. A portion of the antifuse is made from the same silicon layer as the transistors on the die. As a result, the FPGA architectures must be "channeled" (the interconnect and its programmable switches run in channels between the logic cells).



The new MicroVia antifuse uses amorphous silicon as the insulator between two metal layers. When combined with three-layer-metal processes, the MicroVia antifuses can reside between the second and third metal layers. Thus, both the programming elements and the interconnect routing can reside above the logic cells, significantly decreasing die size.

In other words, the XC8100 FPGA's routing resources — both wires and programmable interconnections — are stacked above the gates, as in a sea-of-gates gate array. Because the routing no longer takes up die area, the XC8100 achieves the seemingly contradictory combination of extensive routing on a very small die. Hundreds of test cases and real-world designs (entered with VHDL or Verilog and usually designed for another FPGA or ASIC architecture) have been retargetted to the XC8100 devices; all have been implemented successfully.

The XC8100 Architecture

The XC8100 FPGA architecture has three main configurable resources: configurable logic cells (CLCs), input/output blocks, and interconnections.

The CLCs provide the functional elements for constructing the design's combinatorial and sequential logic. In keeping with the sea-of-gates architecture, the CLCs have a fine-grained structure. Each CLC has four inputs and one output, plus a special cascade input and output. The CLCs are internally programmable to allow a wide range of logic functions to map efficiently to the architecture; programmable choices include input inversions, several types of combinatorial functions, synchronous logic internal feedback paths, three-state enables, and cascade enables. Each cell can be used to implement combinatorial logic (sum-of-products or AND functions), a latch or a three-state buffer.

Enters Production

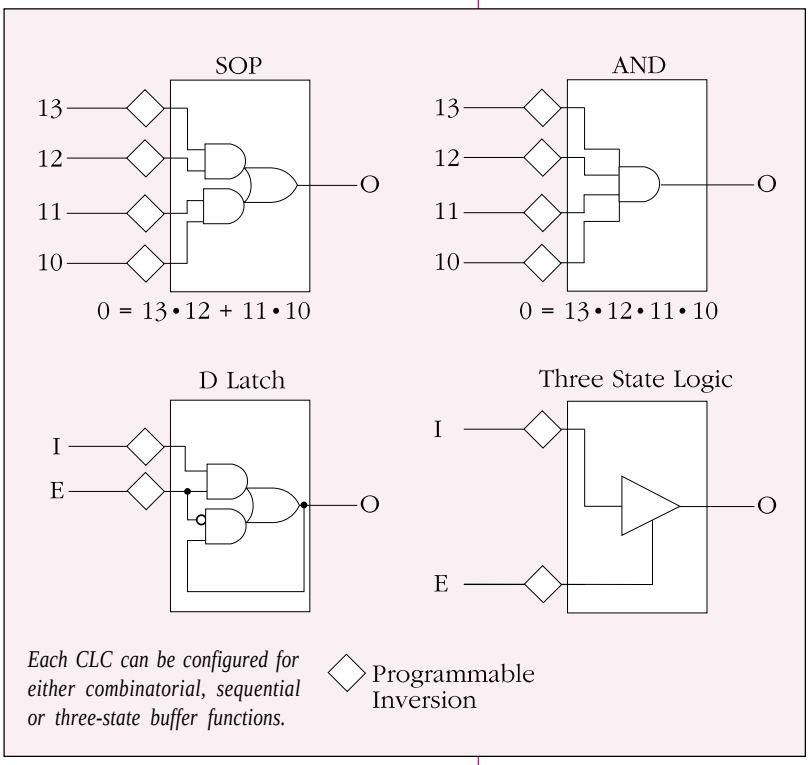
Two adjacent latches are combined through the cascade connection to create a D-flip-flop.

Thus, depending on the input netlist, any CLC can implement a combinatorial, synchronous or three-state buffer function. The XC8100 software has the flexibility to choose the best cell structure depending on the function to be implemented. The objective is to allow the user to design entirely at a high level, without regard to the resources available on the device, and still achieve near-100-percent gate utilization. Designs can be entered in HDLs with little concern for the FPGA architecture. Thanks to the programmable CLC and an abundance of routing resources, XC8100 devices often will replace competitive FPGAs claimed to be 30-50 percent larger. Other features of the architecture include:

- Low power CMOS technology
- Pin-compatible with the XC4000 and XC5200 FPGA families
- 24 mA drive per pin with capacitive or resistive load drivers
- Built-in JTAG boundary scan logic
- Flexible clocks/buffers (e.g., the XC8106 can have up to 72 clocks.)
- Extensive test circuitry for 100 percent testability

Design Security

The XC8100 offers a high level of security for designs that might be subject to reverse-engineering attempts. First, the XC8100 software automatically stores design information in a compressed and encrypted format. Second, the MicroVia technology is practically impossible to reverse-engineer. The antifuses are programmed between the second and third metal layers and, therefore, are covered by a layer of metal and a protective passivation layer. The programmed state of the antifuse cannot be detected by inspection; removal of the protective layers would inevitably damage the underlying antifuses. Furthermore, antifuses are virtually indistinguishable from regular, permanent "vias" between the metal layers. (The XC8106 has more than 750,000 antifuses, about two percent of which are programmed in a typical application.)



Each CLC can be configured for either combinatorial, sequential or three-state buffer functions.

XACT*step* Series 8000 Software

Because the XC8100 architecture is gate-array-like, the design flow is ASIC-like. Like all new Xilinx architectures, the XC8100 uses the standard Xilinx library conventions. However, the very different XC8100 architecture required a new placer, router and other development software. Thus, the initial software for the XC8100 is different from that of the SRAM-based products and will be offered separately.

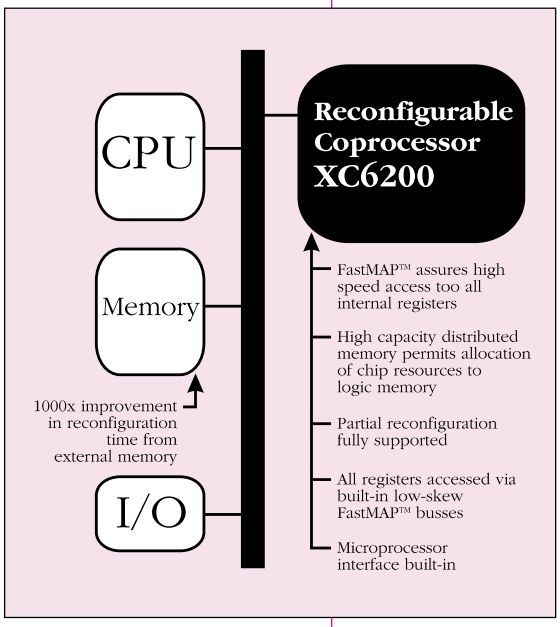
The first CAE interfaces focus on synthesis, both workstation and PC-based. This includes support for Synopsys, Mentor Graphics Autologic, Viewlogic

See XC8100 PRODUCTION, page 24

Introducing the XC6200 FPGA Architecture:

Reconfigurable processing refers to the use of in-system-programmable FPGAs as processing elements, combining the versatility of a programmable solution with the performance of dedicated hardware. *(See XCELL #16.)* Most FPGA-based processors are implemented as coprocessors dedicated to offloading computationally-intensive tasks from a host processor; in other words, the main program is executed by a traditional processor, and certain tasks are assigned to the FPGA-based coprocessor to accelerate their execution.

This approach exploits the fact that most of the processing time for compute-intensive tasks is spent in relatively small portions of the code, and hardware acceleration can significantly improve overall performance. Tasks can be swapped in and out of the coprocessor as needed through reconfiguration of the FPGAs.



Today's FPGA architectures are being used to construct reconfigurable coprocessors. (The XC4000 FPGA family, with it's on-chip memory capability, has been particularly popular for reconfigurable computing applications.) However, these general-purpose architectures have some limitations.

The interface to the main processor's bus must be implemented using programmable logic resources in the FPGA, which may consume a significant portion of the FPGA resources. The internal FPGA architectures are not always optimal for the data-path algorithms typical of coprocessing applications. Providing bus access to large numbers of internal registers requires careful design. On-chip memory capacities are too small for some algorithms. Reconfiguration times are relatively long (several milliseconds) for computing operations, and partial reconfiguration (reconfiguring just a portion of the FPGA) is difficult.

These limitations have been addressed in the new XC6200 FPGA architecture — an SRAM-based FPGA architecture specifically designed for implementing reconfigurable coprocessors in embedded system applications. The XC6200 architecture features a built-in processor interface, a fine-grained cell structure, abundant routing, and support for fast partial or full reconfiguration. The register-rich XC6200 is ideally suited for computationally-intensive datapath applications.

XC6200 FPGA Architectural Features

- **FastMAP™ interface.** Besides the usual progammable I/O, the XC6200 architecture includes a dedicated interface, called the FastMAP interface, designed to connect directly to a host processor bus. The interface can be configured for a 32-bit, 16-bit or 8-bit interface. This built-in, memory-like interface simplifies system design and directly interfaces to most embedded processors without consuming any FPGA resources. The FastMAP interface provides high-speed access to all internal registers in the logic cells. Any register can be mapped into the memory address space of the host processor, allowing for simple hardware and fast data transfers.
- **Ultra fast configuration and reconfiguration.** The FastMAP interface also provides ultra-fast configura-

The First FPGA Architecture Optimized for Coprocessing in Embedded System Applications

tion capability — up to 1,000 times faster than traditional FPGAs. System performance is further improved by the dynamic partial configuration capability, allowing the modification of parts of the FPGA while the other algorithms in the FPGA continue uninterrupted. A serial configuration mode is available.

- **Flexible, fine-grained logic cell.** The programmable logic of an XC6200 FPGA is composed of a large array of simple, reconfigurable logic cells. Each cell contains both programmable logic and routing resources. The cells are simpler than previous FPGA generations, since coprocessing applications tend to be more regular and register-intensive than random logic. Each cell contains a flip-flop and combinatorial logic capable of implementing any two-input function or any type of 2-to-1 multiplexer. Cells are arranged in 4-by-4 blocks and 16-by-16 tiles.
- **High capacity distributed memory.** The very nature of coprocessing demands varying amounts of memory depending on the algorithm being executed at a given time. The XC6200 addresses this by offering high-capacity distributed memory that the user can tailor to suit the application. Each cell can be used for either logic or memory functions. In the memory mode, each cell can be configured to provide two bytes of ROM or RAM. This memory can be accessed via the FastMap interface, by logic implemented in the FPGA, or both.
- **Abundant routing resources.** Six different types of hierarchical routing resources are offered in the XC6200 architecture yielding fast predictable routing delays. In most other architectures these routing delays grow geometrically with distance, whereas in the XC6200 they grow logarithmically.
- **Symmetric architecture for position independent design mapping.** The XC6200 architecture is very symmetric in cell structure and routing resources, making it possible to implement designs that are position-independent. This ability to relocate designs within the FPGA can greatly increase utilization and provides greater latitude in swapping algorithms in and out of an XC6200 family FPGA.

The XC6200 Product Family

The initial product roadmap consists of devices with gate counts as high as 100K gates or memories as large as 256K bits. Products will become available over the next four quarters.

New XACT*step* Series 6000 Development System

The advanced XC6200 architecture has an equally advanced development system. The system fully exploits the architecture with the push of a button or give the designer complete hands-on control. At about 100 gates/second of place and route time, it's every bit as fast as the XC6200 architecture. ◆

Product	Function Cells	Usable Gates[1]	Max. Memory	Availability
XC6209	2304	9K ~ 14K	36K bytes	1H96
XC6216	4096	16K ~ 25K	64K bytes	4Q95
XC6236	9216	36K ~ 56K	144K bytes	1H96
XC6264	16348	64K ~ 100K	256K bytes	2H96

[1]based upon 4~6 gates/function cell.

XC4000E

Continued from page 19

output buffers with a slow slew rate at the end of the configuration process to avoid system noise. Once the I/O blocks are activated, slew rates are set to their programmed values.

Begin Designing TODAY!

Because the XC4000E FPGAs are drop-in compatible with the equivalent XC4000 devices, you can begin exploiting the speed of the XC4000E-3 today using the existing XC4000 support software! Simply download the -3 speed files from the Xilinx bulletin board (in the Software Help area) and begin designing. You'll be able to program your XC4000E-3 the day it arrives. (Of course, this approach does not provide access to the new features of the XC4000E architecture.)

A new module for the new XACT*step* system that allows users to take advantage of the enhanced features of the XC4000E family will be available in early 4Q95 at no charge to users with an active maintenance contract.

Table 2 lists the initial members of the XC4000E family and their projected availability.

Favorable reports have come in from early users of the XC4000E family. Jim Simkins, senior engineering specialist at E-Systems, a manufacturer of military and government systems, reports that "There are dramatic speed increases using the XC4025E device — in fact, up to two to three times in several cases. Currently, E-Systems is using an XC4025E device to implement a DSP function that processes 11.5 bops (billion arithmetic and storage operations per second), with an equivalent capacity of 170,000 LSI Logic gates." ◆

TABLE 1: *Example benchmarks*

	XC40XXE-2	XC40XXE-4
Data Path	156 MHz	109 MHz
State Machine	69 MHz	55 MHz
16 Bit pre-scaled counter	115 MHz	64 MHz
Address map decoder	71 MHz	50 MHz

TABLE 2:

DEVICE	DENSITY RANGE WITHOUT RAM (inusable gates)	DENSITY RANGE WITH RAM*	AVAILABILITY *Sampling*	AVAILABILITY *Production*
XC4003E	2,500 - 3,000	4,000 - 6,000	4Q95	Q196
XC4005E	4,000 - 5,000	7,000 - 11,000	Now	4Q95
XC4006E	5,000 - 6,000	8,500 - 15,000	Now	4Q95
XC4008E	6,500 - 8,000	11,000 - 18,000	Now	4Q95
XC4010E	8,000 - 10,000	14,000 - 22,000	Now	4Q95
XC4013E	10,000 - 13,000	19,000 - 31,000	Now	4Q95
XC4020E	18,000 - 20,000	28,000 - 44,000	4Q95	4Q95
XC4025E	22,500 - 25,000	36,000 - 57,000	Now	4Q95

**10% - 30% RAM usage*

XC8100 Production

Continued from page 19

ProSynthesis, Exemplar, and Motive, as well as VHDL and Verilog models. *(Contact your local Xilinx representative for more details or information about other interfaces.)*

There are several significant new features in the Series 8000 software. First, all logic and nets, including hierarchy, are maintained by the back-end XC8100 tools, so this information is consistent for simulation and debugging; this feature is called TrueMap™ logic mapping. Second, a new router, called PowerMaze™, routes thousands of gates per second. Third, thanks to a new algorithm, Series 8000 software can do incremental design within the synthesis environment. Fourth, patented circuitry and software allows every device to be 100 percent testable, including an automatic post-programming verification without test vectors.

For more information

A data sheet and a product overview are available from your local Xilinx representative and on the Xilinx World Wide Web site. License-free demonstration software also is available. Contact your local Xilinx sales office or representative for the latest availability and pricing information. ◆

Improved Synthesis Support for EPLDs

Synthesis users have plenty of reasons to try the new and improved XACT*step* version 6. This latest version of the Xilinx core software has been optimized for synthesis, providing significant improvements in speed and density among several new features that make EPLD designs easier to develop. Improvements include:

- **Logic Optimization** - XACT*step* EPLD implementation tools automatically produce shorter cycle times, shorter setup times, and reduced pin-to-pin delays. The EPLD fitter now uses refined algorithms for flattening gate level logic produced from synthesis, resulting in better overall speed and density. Table 1 details performance improvements seen in actual customer designs.
- **Timing Driven Optimization** - XACT-Performance™ optimizes designs based on user-specified timing requirements. The software now supports path-timing constraints for EPLDs in the same manner as for any other ASIC technology; for HDL-based designs, these timing specifications are expressed directly through the synthesis tool interface. Timing specifications are automatically transmitted to the XEPLD fitter using the same TIMESPEC attributes currently used for Xilinx FPGAs. The task of producing high-performance designs is now a lot easier.
- **Full Timing Analyzer** - XACT*step* version 6 includes a new timing analyzer that can create a variety of reports to meet specific needs. These reports can provide summaries of the full system or just specific paths and path types. This new EPLD timing analyzer is now compatible with the Xilinx FPGA timing analyzer. Timing reports are easier to read with more detailed information.

Xilinx is committed to providing the best synthesis support in the programmable logic industry with on-going support and development for many third-party synthesis tools, including:

- Synopsys - FPGA Compiler, Design Compiler logic synthesis; VSS full-timing simulation.
- Exemplar - Galileo version 3 logic synthesis (new from Exemplar).
- ViewLogic - ViewSynthesis logic synthesis
- Cadence - Synergy logic synthesis; Verilog timing simulation.
- Mentor Graphics - AutoLogic logic synthesis.
- Data I/O - Synario and ABEL HDL logic synthesis.

Continued on the next page

"Xilinx is committed to providing the best synthesis support in the programmable logic industry with on-going support and development for many third party synthesis tools."

Table 1: *Cycle Time and Density Improvements in XEPLD 6.0*

	XEPLD 5.1 Device	Macro-cells	tCYCLE	XEPLD 6.0 Device	Macro-cells	tCYCLE
1	7336-5PC44	32	28.0ns	7336-5PC44	16	10.4ns
2	73108-7PC84	76	31.0ns	7354-7PC44	25	10.5ns
3	73108-10PQ160	82	31.0ns	73108-10PQ160	75	16.0ns
4	73144-10PQ160	95	49.0ns	73108-10PC84	95	31.0ns
5	None (No Fit)	(142)	-	73144-10PQ160	105	38.5ns

This table is based on customer designs that were expressed in generic VHDL with no instantiations. The designs were processed by the Synopsys FPGA compiler, targeting the Xilinx XC7000 library, to produce XNF netlists. The netlists were processed with the indicated version of the XACT fitter, using default options and no timespecs.

For most designs there is a significant improvement in cycle time, and density is often improved enough to allow use of a smaller device. So, higher performance designs are produced at a lower cost.

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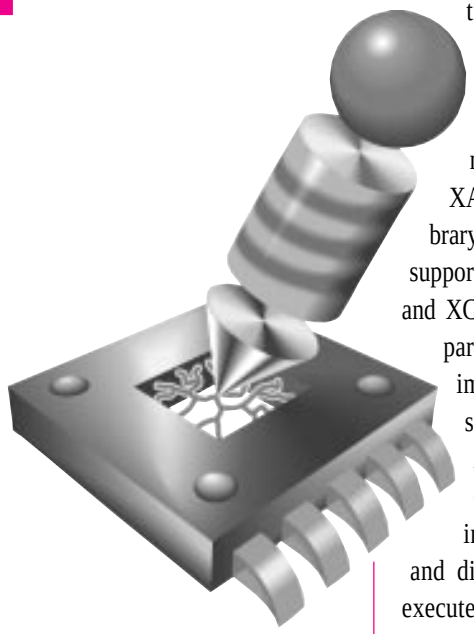
New XSATCET Advanced Design System

As reported in *XCELL* #17, Xilinx has merged with NeoCAD, Inc. of Boulder, Colorado, a leading supplier of FPGA design software. As a result of the merger, Xilinx recently brought to market a new FPGA design system called the XACT*step*™ Advanced package — the first new product offering that leverages the NeoCAD software technology.

The Advanced package features XACT*step* Foundry, NeoCAD's core design system for FPGA implementation (formerly called NeoCAD FPGA Foundry), bundled with the XACT*step* system from Xilinx (formerly called XACT).



XACT*step* Foundry, featuring advanced timing driven placement and routing technology, has a proven track record for helping users achieve maximum utilization and performance for Xilinx FPGA designs. XACT*step* Foundry is netlist and library compatible with XACT*step*, and supports the Xilinx XC4000, XC3100/A, and XC3000/A FPGA families. It adds particularly significant value to the implementation of high-density designs, and includes support for the XC4025. XACT*step* Foundry includes optional high-level synthesis integration, multi-device partitioning and distributive processing capabilities. It executes on PCs and workstations, including Sun Solaris.

The XACT*step* Advanced package is available now. Easy upgrade paths for existing XACT and NeoCAD FPGA Foundry users also are available. ***Contact your local Xilinx sales representative for ordering information.*** ◆

Update News

The latest revision of XACT*step* Foundry (version 7) was shipped this summer to NeoCAD FPGA Foundry owners with a Xilinx configuration and active maintenance contract.

XACT*step* version 6 updates are scheduled for first customer ship in October. Most users will receive their updates in the fourth quarter. XACT*step* version 6 supports the XC2000, XC3000, XC3100, XC4000, XC5000, and XC7000 component families.

Xilinx is hard at work finalizing a new software technology strategy and release plan leveraging the best software technologies of both Xilinx and NeoCAD. New products integrating the best of XACT*step* and XACT*step* Foundry, scheduled for introduction in 1996, will result in unparalleled power, functionality and ease-of-use for FPGA designers. Details on these products will become available in the coming months. ◆

Synthesis Support

Continued from the previous page

Tools for both VHDL and Verilog HDL design entry are available. VITAL-compliant simulation models are available for a variety of third-party simulation tools including Cadence Verilog and Model Technologies. In addition, the EPLD physical device models are available from Logic Modeling, a division of Synopsys.

So, no matter what tools are used, Xilinx provides everything needed to produce high-performance EPLD designs with minimal effort.

For product availability or other information, please contact your local Xilinx representative. ◆

HDL Synthesis Design Guide for FPGAs

To help designers who are new to HDL-based design with Xilinx FPGAs, Xilinx has created the *HDL Synthesis Design Guide for FPGAs*. This 250-page guide provides general design methodologies for targeting FPGAs from synthesis.

Hardware Description Languages (HDLs) are used to describe the behavior and structure of system and circuit designs. The HDL source code is then synthesized to the target device (e.g., an FPGA). In general, synthesis can produce results that are equal to or exceed those of a well-designed schematic. However, synthesis results depend on the quality of the synthesis tool and the style in which the HDL code is written. Often, it is not sufficient that the HDL code is just "functionally correct"; the code must be written in a manner that directs the synthesis tool to generate an efficient hardware implementation and that matches the idiosyncrasies of the particular synthesis tool being used.

For designs that push the limits of FPGA speed and density, synthesis alone is not good enough—designer intervention is necessary. Synthesis tools are not a substitute for good digital design techniques and knowledge of an FPGA's architecture.

Most documentation available today describes how to use synthesis tools effectively to target ASICs. However, not all of the methods used for ASICs apply to programmable logic design. ASICs have more gates and routing resources than FPGAs. Poorly written code or the use of a synthesis tool not designed for FPGAs can result in an inefficient design. The Xilinx *HDL Synthesis Design Guide for FPGAs* addresses the use of HDLs and synthesis tools for FPGA design.

Although the guide uses the Synopsys FPGA Compiler and the XC4000 device to illustrate the design methodologies, the concepts also apply to other synthesis tools and other Xilinx FPGAs. Synopsys and non-Synopsys users alike will find this document extremely useful. All design examples are available in Verilog and VHDL. Xilinx endorses both (though some find VHDL more difficult to learn than Verilog).

To get the most from this guide, Xilinx recommends that you be conversant with VHDL (or Verilog), the synthesis tool and the Xilinx Development tools.

Table of Contents

This guide covers the following topics.

- Chapter 1, "Getting Started," provides a general overview of designing Field Programmable Gate Arrays (FPGAs) with HDLs. It includes installation requirements and instructions.
- Chapter 2, "HDL Coding Hints," discusses design hints and examples to help you develop an efficient coding style.
- Chapter 3, "HDL Coding for FPGAs," provides design examples to help you incorporate FPGA system features into your HDL designs.
- Chapter 4, "Floorplanning Your Design," describes basic operations of the XACT-Floorplanner™ and provides HDL design examples that illustrate which HDL constructs benefit from floorplanning.
- Chapter 5, "Building Design Hierarchy," describes how to partition your designs to improve synthesis results and reduce routing congestion.

Continued on the next page

> *"For designs that push the limits of FPGA speed and density, synthesis alone is not good enough."*

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HDL Synthesis Design Guide

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- Chapter 6, "Understanding High-Density Design Flow," discusses the design flow for high-density HDL designs.
- Appendix A, "Accelerate FPGA Macros with One-Hot Approaches," reprints an article describing one-hot encoding in detail.
- Appendix B, "Top Design Scripts," includes the three script files used to compile the Top design described in the "Building Design Hierarchy" chapter of the manual.
- Appendix C, "Tactical Software and Design Examples," lists the tactical software and design examples that are described in this manual.

How Do I Get a Copy?

The manual and the design examples are available at the Xilinx Internet FTP site (ftp.xilinx.com), the World Wide Web site (http://www.xilinx.com), and the Xilinx Technical Bulletin Board (XTBB); they also will be included on the XACT*step* version 6 CD-ROM when it is released.

To read the online version, you will need a copy of the Adobe Acrobat™ reader. You can obtain instructions and a free copy of the software from the Xilinx WEB site, XTBB, the Xilinx Programmable Logic Breaklthrough '95 CD-ROM, or the appLINX July '95 CD-ROM.

The design guide refers to three utility programs, 27 VHDL design examples and 25 Verilog design examples. Two utilities, AddTNM and MakeTNM were created using Perl. To run these utilities, you will need Perl 4.0 or 5.0 *(see right)*.

The instructions on how to retrieve the manual and the design examples from the Xilinx FTP site, World Wide Web site and Xilinx Bulletin Board are described below. A description of the design examples' files and instructions on how to extract the files are in the "Extracting the Files" section of "Getting Started" in the design guide.

CONTINUED

Xilinx Internet FTP

The manual and design examples are available on the Xilinx FTP site. Descriptions and sizes of the files are shown in the following table.

Files	Description	Compressed File	File/Directory Size
hdl_dg.pdf	HDL Synthesis Design Guide for FPGAs in Adobe Acrobat format	——	1.9 MB
XSI_files	• Tactical code • XNF files for RPMs • Default Synopsys setup file	83 K	344 K
XSI_vhdl	VHDL Examples with SIM, SYN and MRA files in Work directory	5.1 MB	13 MB
XSI_vhdl_no_work	VHDL Examples without SIM, SYN and MRA files in Work directory.	3.3 MB	10.2 MB
XSI_verilog	Verilog Examples	3 MB	9.2 MB

Procedures to retrieve the manual from the Xilinx FTP site:

1. Go to the directory on your local machine where you want to download the files:
   ```
   cd directory
   ```
2. Invoke the FTP utility — Unix users, type: **ftp**
   PC users: contact your system administrator for assistance.
3. Connect to the Xilinx Internet FTP machine, ftp.xilinx.com:
   ```
   ftp> open ftp.xilinx.com
   ```
4. Log onto the guest account. It gives you download privileges.
   ```
   Name (machine:user-name):ftp
   Password: your_email_address
   ```
5. Go to the pub/XSI_HDL directory.
   ```
   ftp> cd pub/XSI_HDL
   ```
6. Retrieve the manual hdl_dg.pdf and the appropriate design files as follows. Both VHDL and Verilog users should retrieve XSI_files.tar.Z. VHDL users can retrieve the smaller design file XSI_vhdl_no_work.tar.Z or the file with the WORK directory, XSI_vhdl.tar.Z. Verilog users should retrieve the file XSI_verilog.
   ```
   ftp> get hdl_dg.pdf
   ftp> get XSI_file.tar.Z
   ftp> get design_files.tar.Z
   ```
7. Extract the example files as described in the "Extracting the Files" section of this article.

World Wide Web

A copy of the manual and design examples can be obtained from the Xilinx World Wide Web site. Access the Xilinx home page under "Product Information -> Application Notes -> HDL Design Guide."

You can download the Adobe Acrobat reader for Windows, Mac and SPARC from a link to Adobe's home page in the Application Notes section. The design examples are also available on the Web.

Xilinx Technical Bulletin Board

The manual and design examples are available on the Xilinx Bulletin Board (XTBB). XTBB is a 24-hour electronic bulletin board available to all registered XACT*step* customers. Refer to the 1994 version of *The Programmable Logic Data* book for a complete description of XTBB, including how to locate and download files.

A description and size of the files are shown in the table following. Note: The manual hdl_dg.zip is very large and may take a long time to download.

Files	Description	Compressed File	Directory Size
hdl_dg.zip	HDL Synthesis Design Guide for FPGAs in Adobe Acrobat format Zipped (using PKZIP)	1.6 MB	
tactical.uu	• Tactical code • XNF file for RPMs • Default Synopsys setup file	115 K	344 K
vhdl_ex.uu	Source files and major files for VHDL Examples	2.6 MB	5.1 MB
ver_ex.uu	Source files and major files for Verilog Examples	2.5 MB	4.7 MB

To retrieve the files from the XTBB:

1. Go to the directory on your local machine where you want to download the files:
   `cd directory`
2. Access the XTBB as described in of *The Programmable Logic Data* book (Chapter 6).
3. Locate the files in the application area of the XTBB. The directory names are listed in the table above.
4. Retrieve the zip and encoded design files.
5. Unzip the file hdl_dg.zip file:
   `unzip hdl_dg.zip`
6. Follow the instructions below to undecode and uncompress the files.

Extracting the Compressed and Encoded files

After you have retrieved the manual and design examples, perform the following to extract the compressed and encoded files:

1. If the file is uu encoded (i.e. has an .uu extention) undecode the file as follows:
   `uudecode file.uu`
2. Uncompress the files:
   `uncompress file.tar.Z`
3. Extract the files:
   `tar xvf file.tar`

How to Get Perl

Get information about Perl (Perl FAQ) from the Unix FTP site:

- North America:
  ftp://fpt.cis.ufl.edu/pub/perl/doc/FAQ
  ftp://fwp.khoros.unm.edu/pub/perl/faq.gz
- Europe:
  ftp://ftp.cs.ruu.nl/upb.NEWS.ANSWERS/perl-faq/
  ftp://ftp.funet.fi/pub/languages/perl/doc/faq
- Access Perl All-Sorts information on the World Wide Web:
  http://www.khoros.unm.edu/staff/neilb/perl/
  http://www.metronet.com/1h/perlinfo
  http://ww.cis.ufl.edu/perl

Software Requirements

To synthesize, floorplan and implement the design examples, you need the following versions of software installed on your system. (Either XACT*step* or XACT*step* Foundry is required, but not both.)

SOFTWARE	VERSION
Xilinx Synopsys Interface (XSI)	3.2.0 or later
XACT*step*	5.1.0 or later
XACT*step* Foundry*	7.0 or later
Synopsys FPGA Compiler	3.2 or later
Xilinx Floorplanner	Contact Xilinx sales rep.
XC4025 die files	Contact Xilinx sales rep.

** XACTstep Foundry v7 does not support the Xilinx Floorplanner.*

Overshoot and Undershoot

The "Absolute Maximum Ratings" table in the *Xilinx Data Book* restricts the signal-pin voltage to a maximum 500 mV excursion above V_{CC} and below ground. The purpose of this tight specification is to prevent uncontrolled current in the input-clamping ESD-protection diodes. Such specifications are common in the industry; some manufacturers limit the excursion to 300 mV.

This specification seems to be clean and simple, but it is violated in almost every practical design. When modern CMOS devices on PC boards are interconnected with unterminated traces, reflections (commonly called "ringing") cause overshoots and undershoots of substantial amplitude (2 V and more). The recent migration to smaller device geometries has made the IC outputs even faster and increased the slew-rate, causing more reflections, even on short PC-board traces.

Fortunately, this problem has an easy solution:

The input voltage is not the important consideration. The real concern is the current through the input protection diode and other input structures. Excessive current can cause latch-up if it exceeds hundreds of milliamps **and** if it lasts for microseconds (shorter duration current spikes do not activate the SCR-like latch-up mechanism).

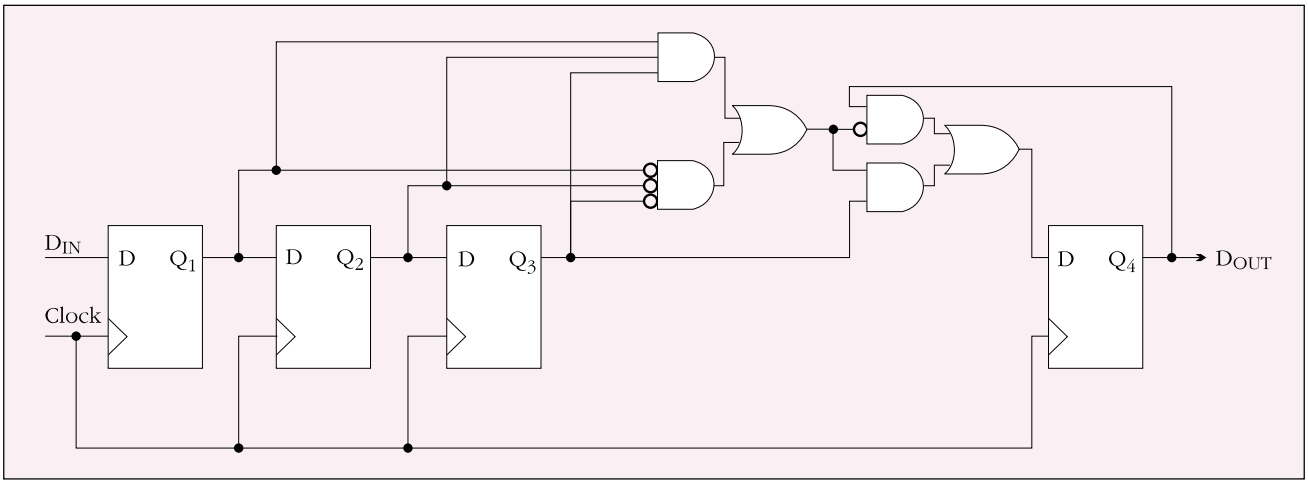
PC-board reflections, on the other hand, usually have a short duration (just a few nanoseconds), and have an impedance of 40 to 100 Ω, which makes them incapable of causing latch-up. They don't drive enough current and they don't last long enough to cause any harm.

Here is the new Xilinx specification:

"Maximum DC overshoot or undershoot above V_{CC} or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to V_{CC} + 2.0 V, provided this overshoot or undershoot lasts less than 20 ns". ◆

Low-Pass Filtering of Noisy Inputs

In the rare case of severe noise on a digital input, a low-pass filter, as illustrated, can clean up the signal, at the expense of additional throughput delay. This circuit uses two CLBs and recognizes an input change only after three successive samples have been identical. In other words, all disturbances shorter than two clock periods are guaranteed to be suppressed. *(For a slow clock source, see the RC oscillator on page 9-22 of the Xilinx Data Book.)* ◆



Examining XC4000E RAM Capabilities

Although it provides increased performance and several new features, each member of the new XC4000E FPGA family is pin- and bitstream-compatible with its corresponding XC4000 cousin.

While maintaining all of the XC4000's capabilities, the XC4000E adds these prominent new features:

- Distributed on-chip RAM
- Synchronous or edge-triggered RAM writing that simplifies timing and improves performance. Careful timing relationships between address, data, and write enable are no longer required.
- Dual-port RAM mode that provides simultaneous read/write capability. This mode is especially useful for building FIFOs and buffer memories. Dual-port RAM is always edge triggered.
- The ability to pre-initialize the contents of RAM on power-up. This feature simplifies an overall design in that RAM values are automatically defined. No additional logic is required to perform the initialization.

Table 1 describes the relative capabilities of the XC4000 and XC4000E families.

Using the new capabilities, memory-based designs operate at much higher speeds. For example, a First-In, First-Out Memory (FIFO) can double in speed when implemented with edge-triggered RAM compared to level-sensitive RAM. Designs can take advantage of the edge-triggered functionality to eliminate input data registers, significantly reducing the size of the circuit.

Dual-port mode allows simultaneous reading and writing, effectively quadrupling the speed of a FIFO over level-sensitive implementations (a first doubling as a result of edge-triggered write, and a second doubling due to the dual-port mode).

Table 1. *RAM Capabilities of XC4000 and XC4000E*

Feature	XC4000	XC4000E
On-chip RAM	✓	✓
Level-sensitive RAM write	✓	✓
Single-port capability	✓	✓
Dual-port capability		✓
Edge-triggered RAM write		✓
Initialized RAM data at power-up		✓

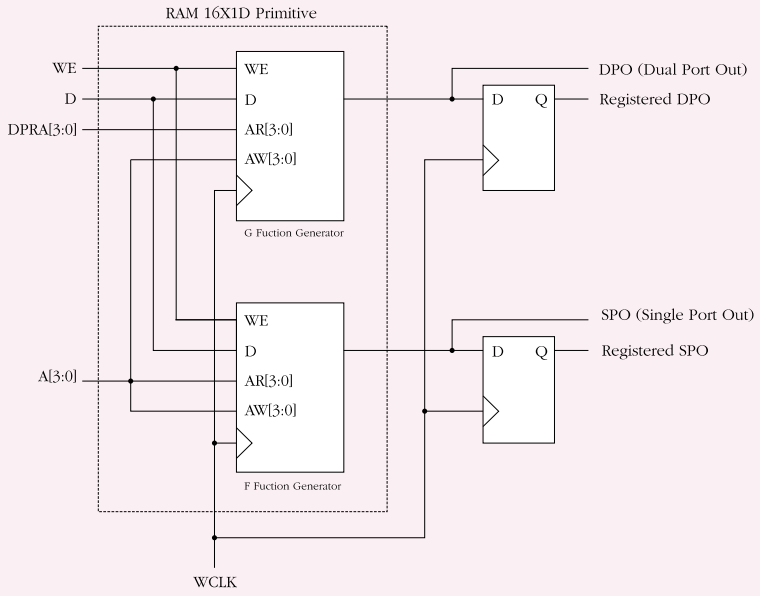


Figure 1: *Conceptual model of dual-port memory implemented in an XC4000E CLB.*

XC4000E Conceptual Model

Figure 1 shows a conceptual model of the XC4000E RAM, configured as a 16x1 dual-port, edge-triggered RAM.. This diagram will be used to describe the various edge-triggered and dual-port capabilities available within each XC4000E logic block. (The diagram is not intended to convey the actual circuit implementation, but rather to describe the functionality.)

A single Configurable Logic Block (CLB) contains two function generators, which can be configured as one 16x1 dual-port RAM, as shown in Figure 1, or as a 32x1 single-port RAM. Alternatively,

Continued on the next page

Examining XC4000E RAM Capabilities

Continued from previous page

the two function generators can be individually configured as any combination of 16x1 single-port RAM and 4-input combinatorial logic functions. The RAM outputs, as with any other function generator outputs, can optionally be registered within the same logic block.

Edge-Triggered Write

The XC4000E provides the choice of level-sensitive or edge-triggered write capabilities. Both options are available for single-port mode, while dual-port mode is always edge-triggered. Most designers are familiar with level-sensitive RAM. This type of RAM is similar to most SRAM devices available on the market.

One disadvantage of level-sensitive RAM is that it requires a precise timing relationship between the Address, Data and Write Enable signals. Maintaining such relationships inside an array-based device can be difficult because the designer does not have direct control over the routing delays within the device.

A better approach for system design is to use clocked or edge-triggered RAM, because edge-triggered writing simplifies the RAM timing. With the introduction of the XC4000E, this option is now available to FPGA designers. Instead of a complex relationship between various timing parameters, the XC4000E RAM timing operates like writing to a data register. Data and address are presented. The register is enabled, after which a clock edge loads the data into the register as shown in Figure 2.

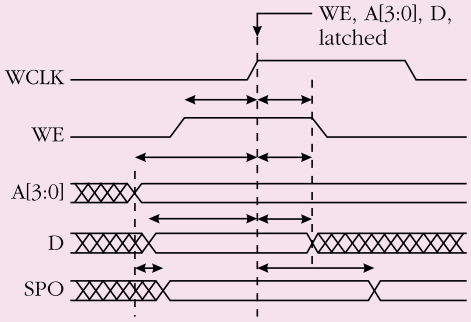


Figure 2. *Edge-Triggered RAM Write Cycle*

The signals used during a write operation are described in Table 2. These signals are derived from Figure 1.

During a write operation, data is presented on the D input. The write location is presented on the address inputs, A[3:0]. The RAM block is enabled for writing by a logic high on the write enable input, WE.

The write clock input, WCLK, can be configured as active on either the rising edge (default) or the falling edge. The rising edge will be used throughout these examples. On the rising edge of WCLK, the D, A[3:0], and WE inputs are captured as shown in Figure 2, thereby synchronizing them to the clock.

A short, built-in delay on the WCLK signal allows the signals to propagate through the decoder logic that enables the appropriate memory cell — the one corresponding to the correct address location in the RAM. The data is clocked into the enabled cell by the delayed clock edge. The new RAM data is available at the RAM outputs a short time later. The timing diagram in Figure 2 shows the case where the A[3:0] address does not change, and SPO reflects the data just written.

The WCLK input to the logic block is the same input used to clock the CLB flip-flops, but it can be separately inverted. Consequently, RAM output data can be captured in the flip-flops, if desired, on either the inactive edge or the next active edge of WCLK.

Table 2. *Edge-triggered RAM Description*

Signal	I/O	Description
A[3:0]	I	Address input for writing both ports of the RAM, and reading the single port.
DPRA[3:0]	I	Address input for reading the dual port.
D	I	RAM Data input.
WE	I	Write enable input. When high, the RAM may be written with the data presented on the D input.
WCLK	I	Write clock input. Clocks the data into the RAM when WE is high. Also captures and synchronizes the A[3:0], D, and WE inputs.
SPO	O	Single-port RAM output. RAM location is controlled by A[3:0] inputs. SPO is not controlled by the WCLK input.
DPO	O	Dual-port RAM output. RAM location is controlled by DPRA[3:0] inputs. DPO is not controlled by the WCLK input.

Dual-Port Mode

Most RAMs have a single address port and a single output port. These are called single-port RAMs. However, some applications require more than one port. FIFOs are

one example of an application that benefits from additional output and address ports.

In a FIFO, there are separate read and write addresses for the memory. A FIFO can be implemented using a single-port memory by multiplexing both the read and write addresses onto a single address port. This approach, however, prevents a simultaneous read and write operation. Either a read or a write operation can access the RAM at different times, but not both at the same time. The extra multiplexers and their associated control logic add to the complexity of a RAM-based FIFO design. A dual-port RAM—one with two address inputs and two data outputs—would simplify a FIFO design.

Again, Figure 1 provides an example. The logic in the figure is configured as a 16x1 edge-triggered dual-port RAM. Data can be read and written using the A[3:0] address port and the RAM data appears on the SPO output, just as it would for a single-port RAM.

Simultaneously, data can be read—but not written—using the DPRA[3:0] address port. The RAM data appears on the DPO output. Operations with the DPRA[3:0] address port are independent of the A[3:0] address port. Consequently, a RAM location can be accessed simultaneously through two different ports using the two sets of address and data ports as described in Table 3.

If both addresses point to the same location, and a write is performed using the A[3:0] inputs, data appears first on SPO and then on DPO a short time later.

Selecting an Appropriate RAM Mode

Table 4 shows the recommended usage for each RAM mode in the XC4000E architecture.

Frankly, there is little reason to use level-sensitive mode in new designs now that edge-triggered RAM is available. In cases where CLB usage must be minimized, single-port edge-triggered mode is recommended. This mode offers the best density, although a lower system throughput than dual-port mode for some applications. If simultaneous read and write capability is an asset and silicon efficiency is not a priority, consider using dual-port, edge-triggered mode for maximum system throughput.

Schematic Symbols

Using the XC4000E edge-triggered and dual-port RAM capabilities requires special schematic symbols available within the XC4000E library. All edge-triggered RAMs have symbols that begin with “RAM” and end with S (in the case of single-port, edge-triggered RAMs) or D (in the case of dual-port RAMs). If no letter is appended, the level-sensitive RAM is referenced.

Initializing RAMs

The XC4000E can initialize RAM to a known value during FPGA configuration. All types of XC4000E RAM can be initialized, including the original level-sensitive mode. The INIT attribute or property is used to initialize RAM to a known value. If omitted, the initial value defaults to all zeros. RAM contents are not affected by a global reset.

Table 3. *Address Port Functionality*

Address Port	Operation	Output Data
A[3:0]	Read and Write	SPO
DPRA[3:0]	Read only	DPO

Table 4. *RAM Mode Selection*

	Level-Sensitive	Edge-Triggered	Dual-Port Edge-Triggered
Use for New Designs?	No	Yes	Yes
Density (Registered 16x1)	1/2 CLB	1/2 CLB	1 CLB
Simultaneous Read/Write?	No	No	Yes
Relative Performance	X	2X	4X (Effective)

Software Support

The edge-triggered and dual-port capabilities are supported in XACT*step*™ version 5.2, or later. An XC4000E update may be required. Edge-triggered, single-port and dual-port RAM are supported in X-BLOX™ with the SYNC_RAM and DP_RAM modules. ◆

Building FIFO Memories in the XC4000E

First-in-first-out memories (FIFOs) receive three significant benefits from the new edge-triggered RAM option of the XC4000E architecture:

- Greatly simplified logic design due to the elimination of timing from the external write enable pulse.
- Fewer data and control logic registers and logic blocks required because synchronization is performed by the WCLK pulse within the RAM.
- An approximate doubling of the overall speed compared with conventional designs.

The remarkable speed improvement results from the elimination of the external write enable signal as the active control. In a traditional FIFO design using level-sensitive RAM, two methods are available to generate the write enable. An external 2x clock can be used to generate a pulse in the third quarter of the FIFO clock period, or the falling edge of the FIFO clock can be used to trigger a glitch on write enable. (The latter method is discouraged because of the risks inherent in internal race conditions.)

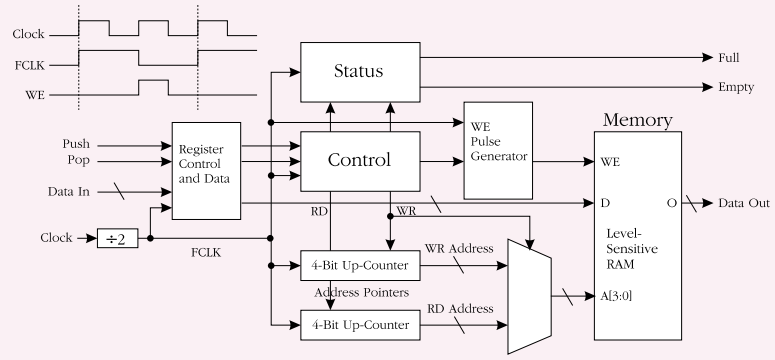


Figure 1: *Traditional FIFO with level-sensitive RAM*

A block diagram of a FIFO using an external 2x clock and level-sensitive RAM is shown in Figure 1. Whichever method is used, only half of a FIFO clock period is available for data and address lines to settle prior to initialization of the Write Enable pulse.

By redesigning the same FIFO to use edge-triggered RAM, an entire clock pulse is available for data and address lines to settle. For FIFOs of any size, loading on the address lines usually determines the speed of operation for the FIFO. Therefore, the modified FIFO operates at about twice the speed of the level-sensitive version.

Figure 2 shows a block diagram of the edge-triggered FIFO. The divide-by-two on the clock has been removed, along with the logic generating the RAM write enable pulse. The registers on data and control inputs are also no longer necessary.

A FIFO in a PCI (Peripheral Component Interconnect) bus interface must operate at 33 MHz, and is typically 8 or 16 words deep by 32 bits wide. A 16x32 PCI write FIFO was implemented using a portion of a PCI-compliant Xilinx XC4005E-3. Using the level-sensitive RAM mode, PCI performance was met, but not exceeded. Switching to edge-triggered mode, a FIFO was produced that reliably runs at 60-65 MHz, without any manual editing required.

Dual-Port FIFO

To implement a FIFO that can read and write at the same time, use only the DPO output. A[3:0] is the write address, and DPRA[3:0] is the read address. The multiplexer on the address lines can be removed. The arbitration logic in the Control block, which normally selects between a Read and a Write operation when both commands are received simultaneously, can also be removed.

The block diagram for a dual-port edge-triggered FIFO is shown in Figure 3. The original nine logic blocks in Figure 1 are reduced to five.

When the PCI FIFO referenced above was modified to use dual-port RAM, the operating frequency was about the same — the advantage of removing the address

CONTINUED

multiplexers was offset by the routing requirements of the increased number of address lines. Although the clock frequency is approximately 60 MHz, the same as the single-port implementation, simultaneous read and write allows a data transfer rate equivalent to 120 MHz in a single-port FIFO. ◆

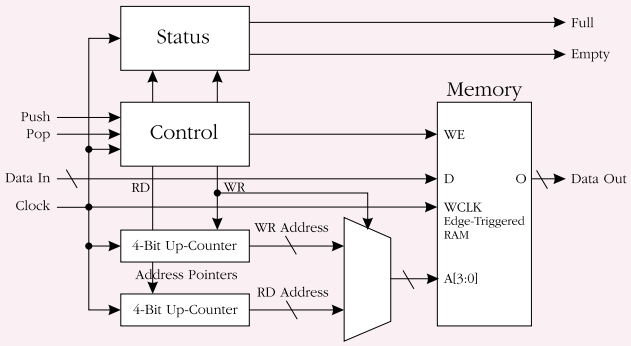


Figure 2: *FIFO with edge-triggered RAM*

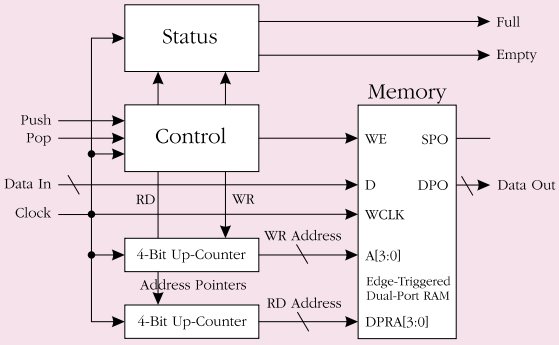


Figure 3: *Dual-port FIFO with edge-triggered RAM*

Mixing 3.3 Volt and 5 Volt Devices

In the past, almost all digital logic devices operated on a 5 volt standard. To reduce chip size and meet the demand for higher integration and reduced power consumption, the semiconductor industry has started the transition to 3.3 V logic. In the future, 3.3 volts is likely to become the dominant supply voltage. For the time being, designers must accommodate both types of ICs in the same design. What are the potential problems?

3.3 V Devices Driving Inputs on 5 V Devices

The lowest output High voltage (V_{OH}) must be high enough to exceed the V_{IH} requirements of the 5 V device. This is not a problem if the 5 V device uses TTL-compatible input thresholds, available on all Xilinx devices. If the 5 V device has CMOS input thresholds, a pull-up resistor to 5 V on each such input will assure a sufficiently High input voltage. The resistor should be somewhere between 10 kΩ and 1 kΩ in value. The upper limit causes the rising input transition to be slow; the lower limit is set by the output current sinking capability of the 3.3 V device output. In the High state, the voltage will be clamped by the protection diode of the 3.3 V device. With only 1 V across the resistor, this current will be fairly small, but care should be taken that the sum of these pull-up currents does not exceed the 3.3 V supply current, thereby reverse-biasing and raising the 3.3 V supply voltage.

5 V Devices Driving Inputs on 3.3 V Devices

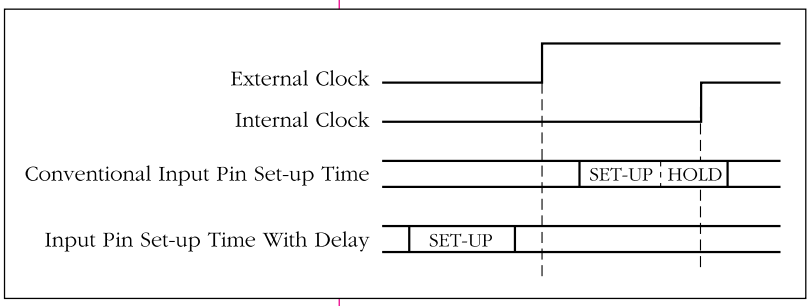
The highest output voltage may not force excessive current into the input of the 3.3 V device. If the 5 V device has a truly complementary CMOS output (like all Xilinx FPGAs and CPLDS except the XC4000 family devices), then the input current must be limited by a series resistor of no less than 100 Ω. This guarantees an input current below 10 mA, flowing through the input protection diode backwards into the 3.3 V supply. Care must be taken to avoid raising the nominally 3.3 V supply voltage above its 3.6 V maximum when a large number of active High inputs drive the 3.3 V device.

If the 5 V device has “totem-pole” n-channel only outputs, V_{OH} is reduced by one threshold and the series resistor can be reduced or even eliminated, provided the nominally 5 V supply never exceeds 5.25 V. ◆

"Hold" is a Four-Letter Word

Beware of hold-time problems, because they can lead to unreliable, temperature-sensitive designs that can fail even at low clock rates.

"Set-up time" and "hold time" describe the timing requirements on the data input of a flip-flop or register with respect to the clock input. The set-up and hold times describe a window of time during which data must be stable in order to guarantee predictable performance over the full range of operating conditions and manufacturing tolerances.



A positive set-up time describes the length of time that the data must be available and stable *before* the active clock edge. A positive hold time, on the other hand, describes the length of time that the data to be clocked into the flip-flop must remain available and stable *after* the active clock edge. A positive set-up time limits the maximum clock rate of a system, but a positive hold time can cause malfunction at any clock rate. Thus, chip designers and system designers strive to eliminate hold-time requirements.

The IC design usually guarantees that any individual flip-flop does not require a positive hold time with respect to the clock signal *at this flip-flop*.

Hold-time requirements between flip-flops or registers on the same chip can be avoided by careful design of the on-chip clock distribution network. If the worst-case clock-skew value is shorter than the sum of minimum clock-to-Q plus minimum interconnect delays, there is never any on-chip hold-time problem.

It is, however, far more difficult to avoid a hold time problem in the device input flip-flops, with respect to the device clock input pin. When specifying the data pin-to-clock pin set-up and hold times, the chip-internal clock distribution delay must be taken into consideration. It effectively moves the timing window to the right *(see figure)*, thus subtracting from the specified internal set-up time (which is good), but adding to the hold time (which is very bad). If the clock distribution delay is any longer than the data input delay — and it easily might be — the device data input has a hold-time requirement with respect to the clock input.

This means that the data source, usually another IC driven by the same clock, must guarantee to maintain data beyond the clock edge. In other words, the data source is not allowed to be very fast. If it is, the receiver might erroneously input the new data instead of the data created by the previous clock, as it should. This is called a race condition, and can be a fatal system failure.

If the receiving device has a hold time requirement, the source of data must guarantee an equivalent minimum value for its clock-to-output delay. Almost no IC manufacturer is willing to do this, and in the few cases where it is done, the minimum value is usually a token 1 ns. Any input hold time requirement is, therefore, an invitation to system failure. Any clock distribution skew on the PC-board can compound this issue and wipe out even the specified short minimum delay.

Xilinx has addressed this problem by adding a deliberate delay to every FPGA data input. In XC3000, and XC3100 FPGAs, this delay is fixed and always present; in XC4000 and XC5200 FPGAs, the delay is optional; its value is tailored to the clock distribution delay (i.e. it is larger for bigger devices). As a result we can claim that no Xilinx FPGA Data input has a hold-time problem (i.e., none has a positive hold time with respect to the externally applied clock), when the design uses the internal global clock distribution network (and, in XC4000 and XC5200, uses the delayed input option). Most competitive devices do not offer this feature. ◆

Acquiring Application Notes and Design Files

Xilinx constantly strives to provide application notes on topics important for programmable logic users. Table 1 lists some of the newer application notes, including the targeted device family and available design files:

Table 1. *Recently Published Xilinx Application Notes.*

TITLE	FAMILY	DESIGN FILES	XDOCS XFACTS	WEB
XC4000 Edge-Triggered and Dual-Port RAM Capability	XC4000E		80004	Yes
Implementing FIFOs in XC4000E RAM	XC4000E	VIEWdraw	80003	Yes
16-Tap, 8-Bit FIR Filter Applications Guide	XC4000/XC4000E	VIEWdraw	80000	Yes
Plug and Play ISA in an XC4000	XC4000/XC5200	VIEWdraw + ABEL	80007	Yes
2910-Compatible Microprogram Sequencer in an XC4000 FPGA	XC4000	VIEWdraw		Yes
Dynamic Microcontroller in an XC4000 FPGA	XC4000	VIEWdraw	80005	Yes
Designing Flexible PCI Interfaces With Xilinx EPLDs	XC7300	ABEL, VHDL		Yes
EPLD-Based Segmented Elastic Frame Store for ATM	XC7300		80010	Yes
Fully Compliant PCI Interface in an XC3164A-2 FPGA	XC3100A	Verilog, VIEWdraw	80006	Yes
Configuring FPGAs Over a Processor Bus	All SRAM FPGAs	VIEWdraw	80011	Yes
Pulse-Width Modulation in Xilinx Programmable Logic	All	VIEWdraw	80009	Yes
Voltage Monitoring for XC2000 Devices	XC2000		80008	Yes

Family — The family for which the application note was written.

Design Files — If indicated, this column shows which design files and formats are available.

XDOCS/XFACTS — If indicated, use this number to retrieve the document from the XDOCS E-mail server or from the XFACTS fax server.

- For XDOCS, send an E-mail message to '**xdocs@xilinx.com**' with '**send <number>**' in the subject header. The server will automatically send a uuencoded and compressed PostScript file that you can send to any PostScript-compatible printer. (You can also send an E-mail to XDOCS with '**help**' in the subject header to retrieve full instructions on using XDOCS.)
- For XFACTS, just dial 1-408-879-4400 and specify the document number along with your return fax number.

Web

If "yes," the document is available on the World Wide Web. The Xilinx home page, called webLINX, can be found at '**http://www.xilinx.com/**'. The document can be found under Application Notes, which is under Product Information. The documents are in Adobe Acrobat™ format. If you do not already have the Acrobat reader installed on your machine, then you can jump to the Adobe home page to download it. ◆

IMPORTANT:

Updated Package Pinout Information

If you are designing with the following devices and packages, please be aware that pinout information in the *1994 Xilinx Programmable Logic Data Book,* third edition, is incorrect for **XC4010BG225, XC4013BG225** and **XC4025.**

Updated pinout information is available on the Xilinx WebLINX under Part Information, on the Xilinx Bulletin Board (filename "newpins.zip") and via XFACT/XDOCS (request document #80012). ◆

General

Q. What are the FXC Libraries included with XACT 5.1.1?

A. In addition to the XC2000, XC3000, XC4000, and XC7000 libraries, the 5.1.1 release also includes libraries called FXC2000, FXC3000, FXC4000, and FXC7000 that can be used in place of the Unified libraries to reduce simulation runtime. Simulation of designs with the 5.0.0 Unified libraries suffered significant increases in simulation runtime due to the addition of more comprehensive violation checking. The FXC simulation libraries do not contain the additional violation checks but are identical in every other way. NOTE: The XC libraries should be used to perform a final timing simulation so that the new violation checking will be performed.

Q. How do I turn off the internal oscillator in an XC5200 family FPGA?

A. Set the Makebits tag for the oscillator clock to the user clock setting ("OscClk:UserClk"). This means that the internal oscillator clock is replaced by the user clock. The default is "OscClk:Cclk". Doing this may produce a DRC error since XACT expects a net to be connected to the osc.CK pin in the top right corner of the XACT Design Editor. You may either ignore the DRC error, or, to eliminate the DRC error, connect a grounded net to the osc.CK pin. ◆

Viewlogic

Q. I just installed XACT 5.1.1, and ProSeries reports:

```
SYSCMD.PIF or SYSBLOCK.PIF
Cannot find file.
Check to insure the path and
 filename are correct.
```

How is this corrected?

A. The system window opened by a sys command or a print command requires the files syscmd.pif and sysblock.pif. These two files are missing from the DS-VLS-STD-PC1 package. You can retrieve these two files either by installing "PROSYN" from the DS-VLS-EXT-PC1 package, by unzipping the prosyn1.zip file from the wn1\prosyn\group2 directory, or by downloading 511FIX.ZIP from the BBS. Make sure these two .pif files are in either the PROSER\ or Windows\ directory.

Q. Why do I get the message "Type Mismatch" from ProSeries?

A. PROvhdl, PROgen, PROlib, PROsynth, and PROgen return this error message when no project has been defined. Defining a project via PROjman or PROcapture will cause the message to go away.

Q. I can run all of the ProSeries software except ProSim. What could be wrong?

A. PROsim is the only program in the PRO Series 6.0 release that uses the WIN32S 32-bit extender. If all the other PROseries software works, the problem may be that WIN32S is not installed or the version installed is not compatible. Try installing WIN32S from the 5.1.1 CD. The WIN32S setup.exe program is located in the WIN32S directory.

Q. Why do I get the error message, "The 386 chip is currently executing in virtual mode under the control of another program" from PROseries tools?

A. The versions prior to XACT 5.1.1 contained executables that could not be run in Windows. Attempting to run these executables in an MS-DOS box would result in this error message. Typically, this occurs when an older, non-Windows compatible executable appears in the path before the new PROSER directory. Remove all references to WORKVIEW in the following system variables: PATH, WDIR, and SYSPLT, and the message should go away. ◆

Synopsys

Q. How can I tell what version of XSI I have?

A. At your command prompt, type syn2xnf <CR>. A help screen will come up with a version number of syn2xnf:

```
syn2xnf v3.5.0=XSI 3.2
syn2xnf v3.6.0=XSI 3.3
```

Q. I was using Synopsys 3.2a and XSI 3.2. Now, I've upgraded Synopsys to v3.3a. When I try to compile my design, I get an error message from the Synopsys Compiler:

```
Error: The entity add_sub_ub'
depends on the package
'std_logic_arith' which has
been analyzed     more
recently.
Please re-analyze the source
file for 'add_sub_ub' and try
again.
Information: Compile
terminated abnormally.
```

A. If you have an existing setup of Synopsys and XSI, and you upgrade your version of Synopsys as above, then you must reanalyze your designware and simulation libraries. Please see the release notes section entitled 'Analyzing the Designware and Simulation Libraries.'

Q. Can Synopsys 3.2a work with XSI 3.3?

A. No. XSI is only compatible with versions of Synopsys equal to or greater than the XSI version. In other words:

```
XSI 3.2 can work with Synopsys
3.2a and greater.
XSI 3.3 can work with Synopsys
3.3a and greater.
Synopsys 3.2a will not work
with XSI 3.3.
```

Q. What are some of the new features in XSI 3.3?

A. Among the major improvements: XSI 3.3 supports XC5200 family designs, and XBLOX optimization has been improved. ◆

Automated Support Systems

An incorrect number for the telephone hotline service in Germany was published on page 29 of *XCELL* #17. Our apologies for any inconvenience that may have caused. The correct number is given below. ◆

Xilinx home page - available at http://www.xilinx.com.
XDOCS E-mail document server - send an E-mail to xdocs@xilinx.com with 'help' as the only item in the subject header. You will automatically receive full instructions via E-mail.
XFACTS fax document server - available by calling 1-408-879-4400.

In order to provide timely support for new, high-growth markets, Xilinx Applications has established a series of E-mail addresses to direct technical inquiries. These addresses may be used to request information packets or to ask in-depth technical questions:

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