XCELL

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XILINX®

The Programmable Logic Company℠

Inside This Issue:

GENERAL FEATURES

XCELL On The Web

This journal, as well as a wide range of literature about Xilinx products, job opportunities, training schedules and much more are available on WebLINX, the Xilinx World Wide Web site...

See Page 9

PRODUCT INFORMATION

Family of In-System Programmable CPLDs Introduced

The high-performance XC9500 CPLD family features FastFLASH™, offering exceptional ISP capabilities ...

See Page 20

Run XACT*step*™ Direct From CD!

Complete instructions on running XACT*step* version 6 alone or in conjunction with Viewlogic's PRO Series...

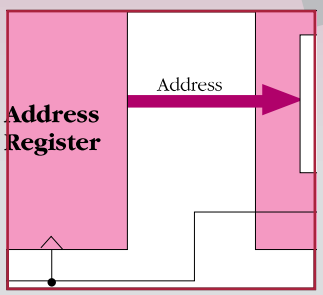
See Page 26

DESIGN TIPS & HINTS

Synchronous RAM Timing in the XC4000E

Taking advantage of the XC4000E family's synchronous memory mode makes it possible to operate near maximum clock frequency...

See Page 30



100,000 Gates and Beyond

By BRADLY FAWCETT ◆ Editor

The time is fast approaching when programmable logic devices will exceed 100,000 usable gates of logic and 100 MHz system clock speed. At these performance levels, the device architectures, design tools and development flows that have been successful for sub-10,000 gate designs will not always suffice. Ignoring for now the issue of how to actually measure "gate capacity," let's examine what will be required of very high-density programmable logic in the near future. (And I'm sure you won't be surprised to learn that Xilinx is well-positioned to meet those requirements.)

As FPGA-based designs get larger and more complex, FPGA architectures and development tools must support a design methodology that mimics high-density ASIC design flows, while delivering the flexibility and time-to-market benefits of FPGA technology. The FPGA device and its development tools must be "synthesis-friendly" — they must easily yield efficient, cost-effective solutions when starting with a high-level description of the design.

Achieving this goal requires attacking the problem from both ends; the architecture must be symmetrical, regular and provide an "easy" target for both synthesis and "place and route" tools. Furthermore, the tools — especially the synthesis compilers — must be tuned to produce the best results for the particular architecture. This, in turn, implies close cooperation between the designers of the FPGA architecture and developers of the synthesis tools. To this end, Xilinx has a Synthesis Syndicate program dedicated to sharing information with third-party CAE developers, as well as an ongoing co-development agreement with Synopsys, the leading supplier of synthesis tools.

Some Tools Already In Place

As with today's high-density FPGAs, **timing-driven tools** that take into account the design's performance requirements during placement and routing (such as the XACT-Performance™ feature of PPR) are key to meeting performance goals in large, complex designs. Very large FPGA designs also could benefit from something that is not available today — **timing-driven mapping**. Much of the technology mapping (that is, the mapping of the user's logic into the logic blocks and other resources of the FPGA architecture) must occur during synthesis so the synthesis tools can make the appropriate area/performance trade-offs. This again implies close cooperation between the chip architects and the synthesis providers.

> *"As FPGA-based designs get larger and more complex, FPGA architectures and development tools must support a design methodology that mimics high-density ASIC design flows, while delivering the flexibility and time-to-market benefits of FPGA technology."*

Designs with 100,000-gates are likely to include datapath logic and memory func-

Continued on page 4

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GUEST EDITORIAL

A Unique Product Strategy

by CHUCK FOX ◆ *Vice President, Product Marketing*

Xilinx is the world's largest supplier of programmable logic — approximately 50 percent larger than the second-largest supplier. We achieved that leading position through a continuing commitment to providing a complete product solution. This encompasses a focus on all three critical areas of the high-density PLD product solution **triangle**: *components*, *software* and *service*.

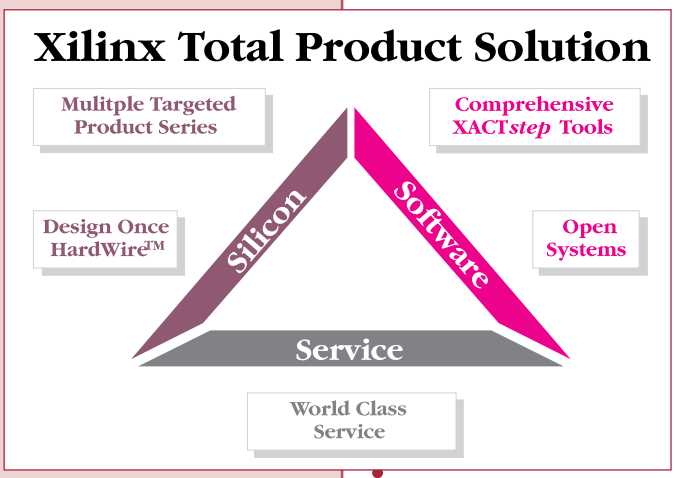
Components

In components, we will continue to leverage new deep submicron process technologies aggressively to deliver improvements in speed, density and cost. We will combine this with innovative, targeted product families in all three major technology segments — CPLDs, reprogrammable FPGAs and one-time programmable FPGAs — supported by the industry's only seamless, no-risk cost-reduction path — the mask-programmed HardWire LCA. Each of these high-growth PLD technologies serves unique requirements in the industry.

Xilinx is the only supplier to deliver leading solutions in all three of these high-growth technologies. Our strategy is to continue to invest heavily in the research and development of innovative solutions in each area. Recently, we have introduced new solutions in all three.

The **XC6200** family of reprogrammable FPGAs provides extremely fast, in-system configuration speeds (as low as 40 ns/cell) and a unique, high-speed dedicated microprocessor interface. These features are ideal for using FPGAs in high-speed "reconfigurable coprocessing" applications.

The **XC8100** series of one-time programmable FPGAs, featuring the industry's first Sea-of-Gates FPGA architecture, is based on a proprietary metal-to-metal antifuse technology called MicroVia™ that, when combined with a unique, fine-grained cell architecture, delivers a powerful, single-chip FPGA solution optimized for an ASIC-like design flow.



The **XC9500** series of CPLDs is the industry's first 5V FLASH solution, representing the next generation in In-System Programmable (ISP) capability. This CPLD family delivers a superior ISP capability targeted at today's total product life cycle requirements.

Software

In software, our **open systems** strategy means we provide seamless integration into all the leading EDA environments, supporting popular front-end HDL, schematic, and simulation systems (as opposed to shipping our own proprietary front-end) as well as supporting industry standards such as EDIF, VHDL, Verilog-HDL and ABEL. We combine this with our comprehensive back-end XACT*step*™ tools to provide a completely technology-independent design system supporting all our component

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XILINX®

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tions, as well as the traditional "glue logic" found in today's FPGA designs. **Automatic placement tools** must support the effective placement of these various types of circuit structures, and will need to be augmented by interactive floorplanning tools. XACT*step*™ version 6 includes a new version of PPR with improved structured-placement capabilities, as well as the industry's first FPGA floorplanner. The synthesis tools will need links to the automatic placement and floorplanning tools, allowing for the passing of design constraints and the back-annotation of timing information.

With large designs, design iterations and last-minute changes are even more inevitable than they are today. Thus, the implementation tools should be re-entrant and tolerant of change, so minor logic changes do not cause major alterations in the physical layout. Xilinx pioneered re-entrant FPGA implementation tools with the Guide option in PPR.

Accurate **simulation** should be available at any point in the design cycle using a common set of simulation vectors. This means that the post-place-and-route timing results need to be back-annotated into the original netlist created by the synthesis program, as opposed to creating a new netlist based on the structure of the FPGA. Once again, this implies a "synthesis-friendly" FPGA architecture, a synthesis compiler capable of efficient technology mapping to that architecture, and a strong link between the synthesis compiler and the "place and route" tools.

Design errors are reduced and design cycles are compressed when users don't need to re-invent common functions. Many leading ASIC providers give users large, pre-defined macro functions, sometimes called cores or megacells. As FPGA densities increase, users should expect similar **large macro functions** to be

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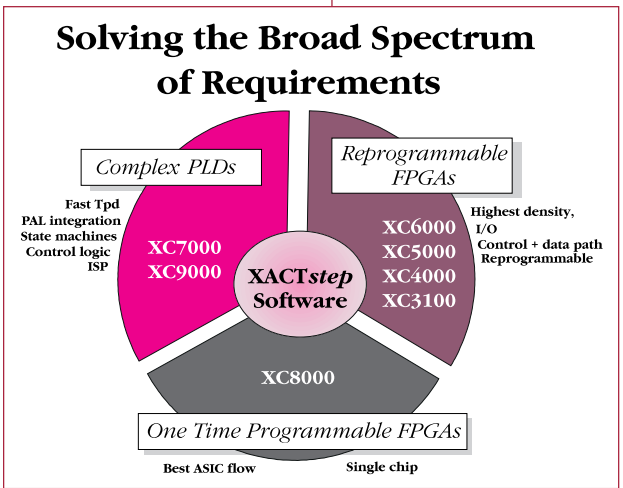
families. Xilinx is committed to providing the best programmable logic design system in the industry with an integrated solution capable of meeting all of your PLD design requirements.

This quarter, we began shipping a major new version of our leading development software**. XACT*step* version 6** delivers six new, Windows®-based productivity tools, providing easy-to-use yet powerful design capability. All Xilinx users under warranty are now receiving their updates. Try it — we guarantee you'll like it.



Service

Providing global, world-class manufacturing, technical support, and sales/distribution support is an essential **foundation** of our product strategy. Many PLD companies severely underestimate the importance of service to the user base. You may have already used one of the several, new, automated technical support facilities that we've established this year, such as XDOCS, XFACTS or our home page on the World Wide Web.

In summary, our product strategy is simple but unique: provide leading solutions in all three high-growth segments of the programmable logic industry — complex PLDs, reprogrammable FPGAs, and one-time programmable FPGAs — support them with the industry's easiest-to-use yet powerful XACT*step* integrated software solution, and deliver unquestioned world-class service. Let us know how we're doing. ◆

available as building blocks for FPGA designs. Similarly, "user-customizable" macro functions, such as those found in the X-BLOX™ library, will ease the designer's task. Ideally, such macros will be inferred during the synthesis process in order to preserve the portability of the high-level design description, as opposed to having to be specifically instantiated in the HDL code .

Synthesis Friendly Architecture

The features that make an FPGA architecture "synthesis-friendly" include regularity, symmetry and granularity.

In many ways, the choice of logic block **granularity** is a trade-off between utilization and performance. With a smaller block, less of each block is wasted for a given logic function, but performance suffers because more levels of logic are needed for a given large function. Of course, other factors also play a role. For example, configuration information must be supplied to each cell; a very fine-grained cell can increase the number of configuration elements per usable gate. The "ideal" ratio will vary with the size and type of configuration element (SRAM cells versus antifuses, for example). So, for FPGAs, it's more appropriate to think in terms of a "sea-of-blocks" rather than a "sea-of-NAND-gates".

For SRAM-based FPGAs, past experience has shown that 4-input lookup-tables are among the most-efficient logic structures; this is not likely to change as FPGAs increase in size. Synthesis algorithms that target lookup-table-based architectures have become more efficient. The lookup-table approach also has the benefit of increasing routing flexibility due to its symmetric nature; that is, signals can be freely swapped among the inputs to the table merely by making the corresponding changes to the contents of the memory cells in that lookup table. Thus, one likely candidate for the "basic logic block" in a high-capacity, synthesis-friendly, SRAM-based FPGA is the lookup-table/flip-flop pair already common to several Xilinx FPGA families.

Memory/Logic Integration

As stated before, large designs typically need to integrate both memory and logic functions. The **on-chip memory** capability pioneered in the XC4000 family will continue to be a desirable feature for very high-density FPGAs. There are three ways of implementing memory in an FPGA:

- small, distributed blocks that can be used as memory or lookup-table-based logic (as in the XC4000 architecture),
- larger embedded blocks of dedicated memory, or
- configuration memory cells that can optionally be used as contiguous memory in the end application (as in the XC6200 architecture).

Each approach has its advantages and disadvantages, and future FPGAs are likely to offer at least one if not some combination of these options.

Connections

The performance of programmable routing resources is more dependent on the number of programmable switches that must be traversed along a signal path than the length of the metal lines. However, it is wasteful both in terms of resource allocation and overall performance to use a long metal segment for a short point-to-point connection. Thus, the programmable routing resources in a large FPGA should be **segmented and hierarchical** in nature, with a mix of local (short), mid-range, and long metal lines. While the amount of local interconnect surrounding a block does not need to change as the logic array grows, the number of longer interconnect lines should increase. A good analogy can be made to the layout of streets in a growing city; the size and relative density of local streets

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does not need to change dramatically as the city gets larger, but the size and number of freeways and major highways must grow with the city.

General-purpose routing resources need to be complemented by dedicated, global, **low-skew nets** for distributing clocks and similar high fan-out control signals. As a rule of thumb, the clock distribution scheme should provide for a worst-case clock skew that is less than 5 percent of the clock period (for example, less than 0.5 ns for a 100 MHz clock).

Internal three-state buffers that provide the capability of implementing bi-directional and multiplexed busses within the FPGA, as pioneered in the XC3000 and XC4000 architectures, will remain a critical architectural feature for larger FPGAs. The need for efficient, on-chip bussing will become more acute as 32-bit and 64-bit busses become more common in microprocessor-based systems.

"Xilinx is poised to deliver new FPGA solutions that fulfill all the requirements for very high density designs."

As FPGA gate capacity increases, the number of **input/output pads** also needs to increase. However, the ability to implement larger designs in a single device will eliminate the need to partition designs among multiple FPGA devices, which will reduce I/O needs to a large degree. Input and output buffers will need to be compatible with a wide variety of signaling standards (for example, JEDEC 3.3V, 5V TTL, 5V CMOS and GTL) to facilitate interfacing to most available IC technologies. Time-to-market demands may cause the user to freeze the I/O placement early in the design cycle, allowing the FPGA design and PCB layout to proceed in parallel. Thus, abundant routing between the I/O blocks and logic array will be required to ensure flexibility in pin placement during design iterations. Furthermore, as with current Xilinx families, maintaining the same package "footprint" across several family members will give system designers the option of moving to higher or lower density devices without modifications to the PCB layout.

Power

High gate capacities and clock rates mean **greatly increased power consumption**. The next generation of large FPGAs probably will be based on the 3.3 V power standard. The transition to 3.3 V logic decreases dynamic power dissipation by 56 percent as compared to a 5 V device running the same design at the same speed. Circuit design techniques that minimize the turn-on overlaps of the P- and N-channel transistors in a CMOS device will be employed to further reduce power consumption. Of course, advanced packaging with good thermal conduction characteristics also will be required.

Both the architecture and underlying transistor-level implementation of a high-density FPGA family should be "**scaleable**" to take advantage of future improvements in IC fabrication technology. Again, Xilinx has a strong track record in this regard, as process advancements have led to faster, larger, and less expensive devices in established FPGA families, such as those based on the XC3000 and XC4000 architectures.

On Toward One Million

While there is plenty of life left in the evolution of Complex PLD architectures (as evidenced by continuing advancements in the Xilinx CPLD product lines), for the near term, PAL-like architectures cannot deliver the flexibility, density, or ASIC-like design flow needed for designs exceeding 100,000 gates.

Meeting the requirements of designs over 100,000 gates will require more than just larger versions of today's devices and tools. Using the highly-successful XC4000 and XC5000 architectures as a stepping stone, Xilinx is poised to deliver new FPGA solutions that fulfill all the requirements for very high density designs.

And we're already thinking about one million gates... ◆

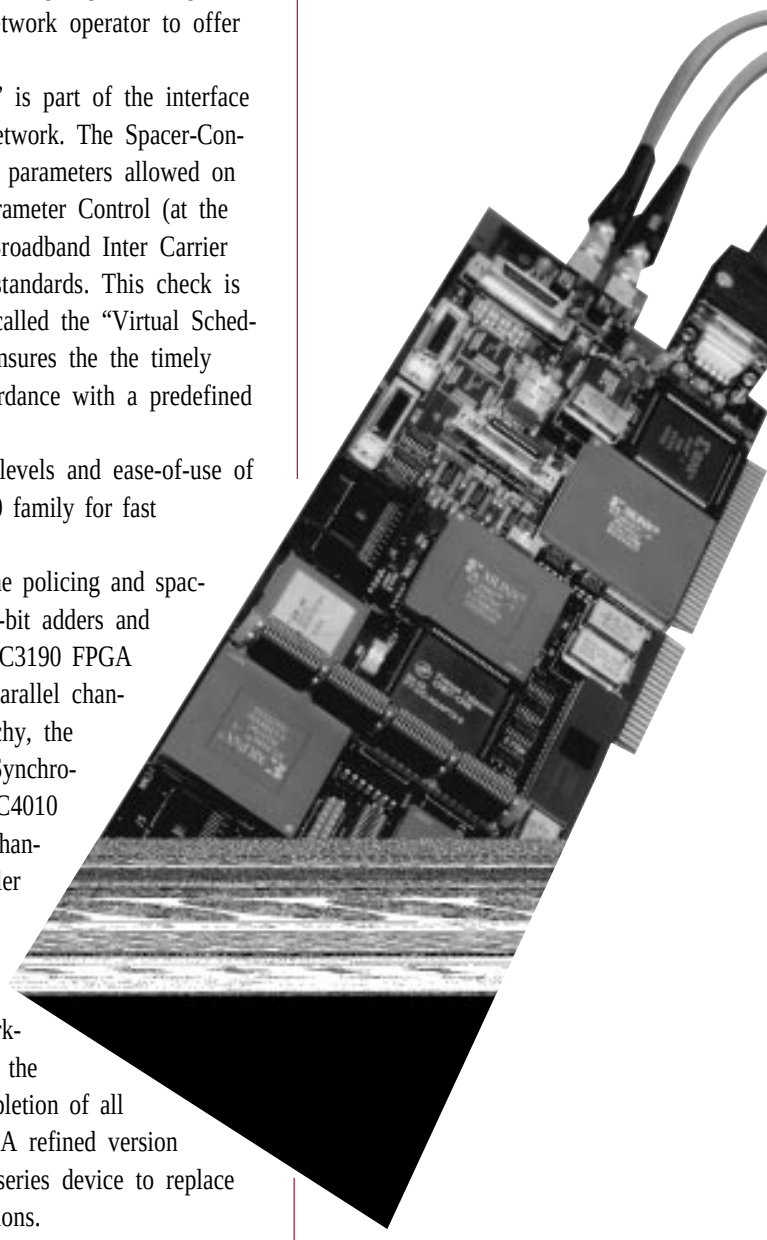
FPGAs Contrd ATM Connections to French Telecom Network

The Lannion-based laboratory of France Telecom's research center, **Centre National d'Etudes des Telecommunications** (CNET), has found Xilinx FPGAs useful in its research on Asynchronous Transfer Mode (ATM) telecommunications for high-speed communications over ordinary telephone lines. One of seven laboratories operated by France's public telephone company, CNET engineers have been designing, building and testing prototypes of the equipment needed to allow a public network operator to offer ATM connections.

One such piece of equipment, dubbed the "Spacer-Controller," is part of the interface between the sources of the ATM streams and the public ATM network. The Spacer-Controller must check that each received cell conforms to the traffic parameters allowed on that substream. This policing function is referred to as Usage Parameter Control (at the User Network Interface) or Network Parameter Control (at the Broadband Inter Carrier Interface) in the International Telecommunications Union (ITU) standards. This check is performed using an ITU standard algorithm developed at CNET called the "Virtual Scheduling Algorithm." Subsequent to this check, a spacing function ensures the the timely smoothing out of cells belonging to the same substream in accordance with a predefined Peak Emission Interval.

Based on eight years of experience with the high integration levels and ease-of-use of Xilinx FPGAs, the CNET engineers chose members of the XC3100 family for fast prototyping of these highly complex ATM traffic functions

Driven by a 20 MHz clock, four XC3190 FPGAs implement the policing and spacing functions. At the heart of these functions are the multiple 32-bit adders and comparators used for the Virtual Scheduling Algorithms. A fifth XC3190 FPGA selects one of four incoming channels — two proprietary 8-bit parallel channels, one 34 Mbit/s PDH channel (Plesiochronous Digital Hierarchy, the European equivalent to T3), and one 155 Mbit/s SDH channel (Synchronous Digital Hierarchy, the European equivalent to STS-3). An XC4010 and XC4003 FPGA hold the logic for adaptation from the PDH channel to ATM format. This prototype version of the Spacer-Controller is capable of handling 4,096 VP or 65,536 ATM connections on a single link of up to 155.52 Mbit/s on a PC board.



Along with the XACT software, the CNET researchers used Viewlogic tools on a PC and Cadence tools on Sun and IBM workstations to complete the FPGA designs. Logic block utilization of the FPGAs exceeded 90 percent in all but one of the XC3190s. Completion of all the FPGA designs required an estimated one man-year of effort. A refined version currently in development will use a single high-density XC4000 series device to replace the four XC3190s that implement the policing and spacing functions.

This equipment will allow a public network operator to offer ATM connections at an attractively low cost (since the user is granted the lowest possible bandwidth allocation compatible with the application) and with as few constraints as possible (the capability for cell delay variation absorption means that the user does not need to consider the detailed traffic characteristics of his connections at subscription time). ◆

New Product Literature

Learn about the newest Xilinx products and services through our extensive library of product literature. The most recent pieces are listed below. To order or to obtain a complete list of all available literature, please contact your local Xilinx sales representative. ◆

TITLE	DESCRIPTION	NUMBER
Corporate		
Product Overview Brochure	Features & Benefits	#0010130-05
EPLDs		
XC7336 Data Sheet	Technical Data	#0010269-01
FPGAs		
User Access to XC6200 Configuration Memory	Application Note	#0010264-01
Interfacing XC6200 to Microprocessors (TMS320C50)	Application Note	#0010265-01
Interfacing XC6200 to Microprocessors (MC68020)	Application Note	#0010266-01
XC5200 Data Sheet	Technical Data	#0010267
XC8100 Data Sheet	Technical Data	#0010193-04

UPCOMING EVENTS

Look for Xilinx technical papers and/or product exhibits at these upcoming industry forums. For further information about any of these conferences, please contact Kathleen Pizzo (Tel: 408-879-5377 FAX: 408-879-4676). ◆

Design SuperCon 96
Jan. 30-Feb. 1
Santa Clara, California

1996 ACM/SIGDA Fourth International Symposium on FPGAs
Feb. 11-13
Monterey, California

European Design and Test Conference
Mar. 12-14
Paris, France

DSPx 96
Mar. 11-14
San Jose, California

International IC Conference
Mar. 27-29
Shanghai, China

PCI 96
Apr. 14-18
San Jose, California

Digitronics
Apr. 17-18
Birmingham, UK

FINANCIAL RESULTS

Strong Revenue Growth Continues

Xilinx sales revenues for the second fiscal quarter (ending September 30, 1995) rose to a record $141.2 million, an increase of 12 percent from the previous quarter and 78 percent from the same quarter one year ago.

The revenue increase resulted from growth in several product families. The XC4000 family continued its strong pace, accounting for 43 percent of total revenues and 50 percent of incoming orders. EPLD revenues grew 80 percent to more than $3 million. The new XC5200 family generated its first million dollars in sales revenue.

Geographically, revenues from North America remained strong, increasing 15 percent over the previous quarter. The European market was surprisingly robust for a summer quarter, growing 33 percent from the previous quarter and contributing 22 percent of total revenues.

Looking ahead to the next six months, CEO Bernie Vonderschmitt stated that, “Our recent bookings momentum, strong backlog position, and new product strength position Xilinx favorably for continued growth in the second half of the year.”

Xilinx stock is traded on the NASDAQ exchange under stock symbol XLNX. ◆

What's New at WebLINX?

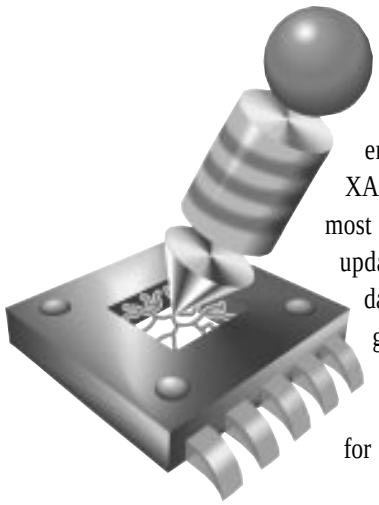
- ***XCELL* journal** issues 17, 18, and 19
- **New Technology Licensing and Partnership Program—** Xilinx is always looking for leading-edge hardware and software technologies, new products, and new services. Here's where to input your ideas.
- **Product Literature**
  - — XC8100 FPGA family press release, product overview and data sheet
  - — XC6200 FPGA family data sheet
  - — Updated XC4000E FPGA family data sheet
  - — New application notes
- **Coming Soon: Keyword Searching** — Find what you want fast with a search of all Xilinx WebLINX HTML and PDF files, as well as other programmable logic sites (distributors, universities, partners, etc.)

Any Suggestions?

What new content, service, or searchable web site would you like to see on WebLINX? Send suggestions to webmaster@xilinx.com. ◆

One-Day XACT*step* 6.0 Update Class

Xilinx now offers a one-day training class for current users focusing on the XACT*step*™ version 6 update. This class provides the fastest way to make the transition to the new features of XACT*step*, including the Windows-based interface, the XACT-Floorplanner™, and XC5200 and XC4000E FPGA family support. Emphasis is placed on gaining hands-on experience with the new graphical tools.



The update does not overlap with previous seminars. Users should have experience with the current XACT® 5.*x* tools to get the most from the one-day update; the standard three-day class, which integrates software training into the overall design flow, is recommended for new users. In the one-day update, all the new features will be described in relation to the previous XDM-based environment. Again, there is little overlap with earlier training; in fact, the update class is best for those who have attended Xilinx training on the earlier tools.

Although most of the Windows-based tools are only available on the PC, workstation users have access to the new graphical Floorplanner. Current workstation users can attend the morning part of the update session, which covers the new devices and the Floorplanner.

Classes are scheduled at many of our existing training locations. Tuition is $100 in North America, but will be waived for those who attended the three-day training since April, 1995. ***Contact your local sales office, send e-mail to customer.training@xilinx.com, or check the WebLINX web site for details.*** ◆

COMPONENT AVAILABILITY CHART

PINS	TYPE	CODE	XC2064	XC2018	XC2064L	XC2018L	XC3020	XC3030	XC3042	XC3064	XC3090	XC3020A	XC3030A	XC3042A	XC3064A	XC3090A	XC3020L	XC3030L	XC3042L	XC3064L	XC3090L	XC3142L	XC3190L	XC3120A	XC3130A	XC3142A	XC3164A	XC3190A	XC3195A	XC4003	XC4005	XC4006	XC4008	XC4010	XC4010D	XC4013	XC4013D	XC4025
44	PLASTIC LCC	PC44	◆	◆				◆					◆												◆														
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120	CERAMIC PGA	PG120																												◆								
132	PLASTIC PGA	PP132							◆	◆				◆	◆											◆	◆												
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144	PLASTIC TQFP	TQ144												◆	◆				◆	◆		◆	◆			◆	◆												
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156	CERAMIC PGA	PG156																													◆	◆							
160	PLASTIC PQFP	PQ160								◆	◆				◆	◆											◆	◆	◆		◆	◆	◆	◆	◆	◆	◆	◆		
164	CERAMIC QFP	CQ164									◆																												
	TOP BRZ. CQFP	CB164									◆					◆												◆	◆		◆								
175	PLASTIC PGA	PP175									◆					◆												◆	◆										
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176	PLASTIC TQFP	TQ176														◆					◆		◆					◆										
184	CERAMIC PGA	PG184																																					
191	CERAMIC PGA	PG191																															◆	◆					
196	TOP BRZ. CQFP	CB196																																◆					
208	PLASTIC PQFP	PQ208									◆					◆												◆	◆		◆	◆	◆	◆	◆	◆	◆		
	METAL MQFP	MQ208																															◆	◆		◆			
	HI-PERF QFP	HQ208																																					
223	CERAMIC PGA	PG223																											◆							◆		◆
225	PLASTIC BGA	BG225																																◆	◆	◆	◆		
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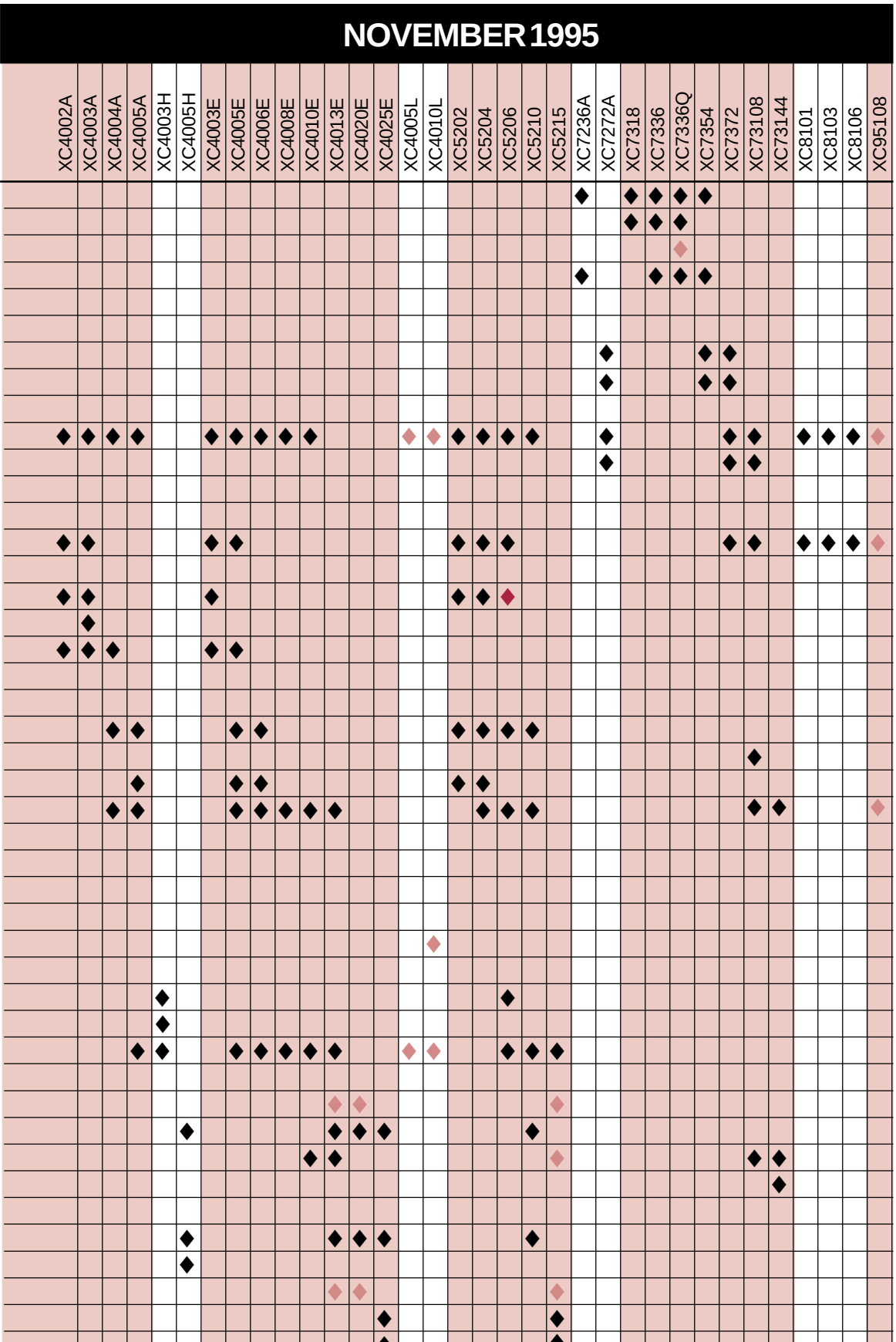
228	TOP BRZ. CQFP	CB228																																		◆			
240	PLASTIC PQFP	PQ240																																		◆	◆		
	METAL MQFP	MQ240																																		◆		◆	
	HI-PERF QFP	HQ240																																					
299	CERAMIC PGA	PG299																																				◆	
304	HI-PERF. QFP	HQ304																																				◆	

◆ = Product currently shipping or planned ◆ = New since last issue of XCELL


NOVEMBER 1995
XC4002A
XC4003A
XC4004A
XC4005A
XC4003H
XC4005H
XC4003E
XC4005E
XC4006E
XC4008E
XC4010E
XC4013E
XC4020E
XC4025E
XC4005L
XC4010L
XC5202
XC5204
XC5206
XC5210
XC5215
XC7236A
XC7272A
XC7318
XC7336
XC7336Q
XC7354
XC7372
XC73108
XC73144
XC8101
XC8103
XC8106
XC95108

ALLIANCE PROGRAM - COMPANIES & PRODUCTS - NOVEMBER 1995

Company	Product Name	Version	Function	Design Kit	2K/3K/4K Support	XC5200 Support	EPLD Support	Unified Lib. Support
Acugen	ATGEN	2.60	Automatic Test Generation	AALCA interface	✓	✓	✓	
	Sharpeye	2.60	Testability Analysis	AALCA interface	✓	✓	✓	
ALDEC/Susie-CAD	Active-Xilinx	2.0	Schematic Entry/Simulation	Included	✓	✓	✓	✓
	Active-Xlx-State	2.0	Schematic State Editor/ HDL Editor Simulation	Included	✓	✓	✓	✓
	Active-Xlx-Syn	2.0	Schematic State Editor/ HDL Editor Synthesis Sim.	Included	✓	✓	✓	✓
Aptix	System Explorer	2.1	System Emulation	Axess 2.1	✓	✓		
	ASIC Explorer	2.3	ASIC Emulation	Axess 2.3	4K	✓		✓
Cadence (Valid)	Concept	2.0-P7	Schematic Entry	Xilinx Front End	✓	Q4	✓	✓
	Rapidsim	4.2	Simulation	Xilinx Front End	✓	Q4	✓	✓
	Composer	4.3.3	Schematic Entry	Xilinx Front End	✓	Q4	✓	✓
	Verilog	2.2.1	Simulation	Xilinx Front End	✓	Q4	✓	✓
	FPGA Designer	3.3	Synthesis	FPGA Synthesis	✓	Q4	✓	✓
Capilano	DesignWorks	3.1	Schematic Entry/Simulation	XD-1	✓			✓
Compass	Asic Navigator		Schematic Entry	Xilinx Design Kit	✓	✓		
	QSim		Simulation		✓	✓		
	X-Syn		Synthesis		✓			
Data I/O	ABEL	6.1	Synthesis	XEPLD Fitter			✓	✓
	Synario	2.1	Schematic Entry, Synthe-	SYN-LCA	✓	✓	✓	✓
			sis and Simulation	SYN-XEPLD			✓	✓
Escalade	DesignBook		Design Entry		✓			✓
Exemplar Logic	Galileo	3.1.1	Synthesis	Included	✓	✓	✓	✓
Flynn Systems	FS-ATG	2.6	Test Vector Generation	Xilinx Kit	✓	✓	✓	
	Probe	2.6	Testability Analysis	Xilinx Kit	✓	✓	✓	
	CKTSIM	2.6	Logic Analysis	Xilinx Kit	✓	✓	✓	
	FS-SIM	2.6	Simulation	Xilinx Kit	✓	✓	✓	
IBM-EDA	Boole-Dozer		Synthesis		✓			
IK Technology	G-DRAW	5.0	Schematic Entry	GDL2XNF	✓			
	G-LOG	4.03	Simulation	XNF2GDL	✓			
Ikos	Voyager	2.10	Simulation	Xilinx Tool Kit	✓			
Incases	Theda	2.0	Schematic Entry	Xilinx Kit	✓			
Intergraph	VeriBest Design Capture	14.0	Design Capture	Xilinx FPGA Design Kit	3K,4K	✓		✓
	VeriBest Simulator	14.0	Simulation	Xilinx FPGA Design Kit	3K,4K	✓		✓
	Veribest DMM	14.0	Design Management	Xilinx FPGA Design Kit	3K,4K	✓		✓
	VeriBest Synthesis	14.0	Synthesis	Xilinx FPGA Design Kit	3K,4K	✓		✓
	ACEPlus	12.2	Schematic Entry	Xilinx FPGA Design Kit	3K,4K			✓
	AdvanSIM-1076	12.0	Simulation	Xilinx FPGA Design Kit	3K,4K			✓
	Synovation	12.2	Synthesis	Xilinx FPGA Design Kit	3K,4K			✓
	PLDSyn	12.0	Design entry, Synthesis		✓		✓	
ISDATA	LOG/iC2	4.2	Synthesis, simulation	Xilinx Mapper	✓	✓	✓	✓
	LOG/iC Classic	4.2	Synthesis	LCA-PP	✓		✓	
IST	ASYL+	3.2.1	Synthesis, Partitioning	XNF interface	✓	✓	✓	✓
ITS	XNF2LAS	1a	Lasar model gen.	XNF2LAS	✓			
Logic Modeling (Synopsys Division)	Smart Model		Simulation Models	In Smart Model Library	✓		✓	
	LM1200		Hardware Modeler	Xilinx Logic Module	✓		✓	
Logical Devices	CUPL	4.5	Synthesis	Xilinx Fitter	✓		✓	
Mentor Graphics	QuickSim II	A.x_F	Simulation	Call Xilinx	✓	✓	✓	✓
	Design Architect	A.x_F	Schematic Entry	Call Xilinx	✓	✓	✓	✓
	Autologic	A.x_F	Synthesis	Xilinx Synthesis Library	✓	✓	✓	✓
MINC	PLDesigner-XL	3.3	Synthesis	Xilinx Design Module	✓			
Minelec	Ulticap	1.32	Schematic Entry	Xilinx Interface	2K,3K			
OrCAD	SDT386+	1.2	Schematic Entry	Call Xilinx	✓	XACT6	✓	✓
	Capture	6.1	Schematic Entry	Call Xilinx	XACT6	XACT6	XACT6	XACT6
	VST 386+	1.2	Simulation	Call Xilinx	✓		✓	✓
	Simulate	6.0	Simulation	Call Xilinx				
	PLD 386+	2.0	Synthesis	Call OrCAD	✓			
Protel	Advanced Schematic	2.2	Schematic Entry	Xilinx interface	✓		✓	
Quad Design	Motive	4.3	Timing Analysis	XNF2MTV	✓			
Simucad	Silos III	95.100	Simulation	Included	✓			✓
Sophia Systems	Vanguard	5.31	Schematic Entry	Xilinx I/F Kit	✓		✓	
Synopsys	FPGA Compiler	3.3	Synthesis	Call Xilinx	3K,4K	✓	✓	✓
	Design Compiler	3.3	Synthesis	Call Xilinx	✓	✓	✓	✓
	VSS	3.3	Simulation	Call Xilinx	✓	✓	✓	✓

ALLIANCE PROGRAM - COMPANIES & PRODUCTS - NOVEMBER 1995 (con't)

Company	Product Name	Version	Function	Design Kit	2K/3K/4K Support	XC5200 Support	EPLD Support	Unified Lib. Support
Synplicity	Synplify Synplify-Lite	2.5c 2.5c	Synthesis Synthesis	Included Xilinx Mapper	3K,4K 3K,4K	✓ ✓		✓ ✓
Teradyne	Lasar	6	Simulation	Xilinx I/F Kit	✓			
Tokyo Electron	ViewCAD	5.0502a	FLDL to XNF translator	XNFGEN	✓			
Topdown Design	V-BAK	1.1	XNF to VHDL translator	XNF interface	✓	✓		✓
transEDA	TransPRO	1.2	Synthesis	Xilinx Library	✓			
VEDA	Vulcan	4.5	Simulation	Xilinx Tool Kit	✓			
Viewlogic	ProCapture ProSim ProSynthesis WorkView Office	6.1 6.1 5.02 5.5	Schematic Entry Simulation Synthesis, Timing Analysis Schem/Sim/Synth	Call Xilinx Call Xilinx Call Xilinx Call Xilinx	✓ ✓ ✓ ✓	XACT6 XACT6 XACT6 XACT6	✓ ✓ ✓ ✓	✓ ✓ ✓ ✓
Viewpoint	VitalBridge VeriLink	1.0 1.0	Vital VHDL Verilog lib. back-annotation	VHDL I/F kit Verilog I/F kit	✓ ✓			
Visual Software Solutions	StateCAD	2.4	State diagram	Xilinx fitter	✓			
Zycad	Paradigm XP Paradigm RP		Gate-level simulation Rapid prototyping		✓ ✓			

ALLIANCE PROGRAM - PLATFORMS & CONTACTS

Company	Contact Name	PC	Sun	RS6000	HP7	Phone Number
		PLATFORM				
Acugen	Peter de Bruyn Kops	✓	✓		✓	603-881-8821
Aldec/Susie-CAD	David Rinehart	✓				702-293-2271
Aptix Corporation	Wolfgang Hoeflich		✓		✓	408-428-6200
Cadence	Itzhak Shapira Jr.		✓	✓	✓	408-428-5739
Capilano Computing	Chris Dewhurst	✓				604-522-6200
Compass Design	Shahid Khan		✓		✓	408-433-4880
Data I/O	Dave Kohlmeier	✓	✓			206-867-6802
Escalade	Jerry Rau	✓	✓			408-481-1336
Exemplar Logic	Stan Ng	✓	✓		✓	510-337-3700
Flynn Systems	Mike Jingozian	✓				603-598-4444
IBM-EDA	John Orfitelli			✓		914-433-9073
IK Technology	Hiroyuki Kataoka				✓	+81-3-3464-5551
Ikos	Brad Roberts		✓		✓	408-366-8509
Incases	Richard Collins				✓	214-373-7344
Intergraph Electronics	Greg Akimoff	✓	✓		✓	415-691-6541
ISDATA	Ralph Remme	✓	✓		✓	+49-721-751087
IST	Gabriele Saucier	✓	✓		✓	408-982-2557
ITS	Frank Meunier		✓		✓	508-897-0028
Logic Modeling	Marnie McCollow		✓		✓	503-531-2412
Logical Devices	David Mot	✓				303-279-6868
Mentor Graphics	SamPicken		✓	✓	✓	503-685-1298
MINC	Kevin Bush	✓	✓		✓	719-590-1155
Minelec (Belgium)		✓				+32-02-4603175
OrCAD	Troy Scott	✓				503-671-9500
Protel Technology	Matthew Schwaiger	✓				408-243-8143
Quad Design Tech.	Dermott Lynch	✓	✓	✓	✓	805-988-8250
Simucad	Richard Jones	✓				510-487-9700
Sophia Systems	BobArmstrong	✓	✓		✓	408-943-9300
Synopsys	Lynn Fiance		✓	✓	✓	415-694-4102
Synplicity	Alisa Yaffa	✓	✓		✓	415-961-4962
Teradyne	Mike Jew		✓		✓	617-422-3753
Tokyo Electron	Shige Ohtani					+81-3-5561-7212
TopDown	ArtPisani	✓	✓	✓		603-888-8811
transEDA	James Douglas		✓		✓	+44-1703-255118
VEDA	George Sher		✓		✓	408-496-4516
ViewLogic	Preet Virk	✓	✓	✓	✓	508-480-0881
Viewpoint International	Ramesh Bhimarao	✓	✓		✓	408-954-7370
Visual Software Solutions	Ricky Escoto					305-346-8890
Zycad	David Allenbaugh		✓		✓	510-623-4451

XILINX RELEASED SOFTWARE STATUS - DECEMBER 1995

Product Category	Product Description	Product Function	Xilinx Part Number	Previous Ver. Rel.	Current Version By Platform			Last Update
					PC1 *6.2*	SN2 *4.1.x*	HP7 *9.01*	
XILINX INDIVIDUAL PRODUCTS								
CORE EPLD	XC7K Support	Core Implementation	DS-550-xxx	5.11	6.00	5.20	5.20	11/95
Mentor	8.4 (A.3-F)	I/F and Libraries	DS-344-xxx	5.11		5.20	5.20	11/95
OrCAD		I/F and Libraries	DS-35-PC1	5.10	5.20			11/95
Synopsys		I/F and Libraries	DS-401-xxx	3.30		5.20	5.20	11/95
Viewlogic	ProCapture	I/F and Libraries	DS-390-PC1	5.11	6.00			11/95
Viewlogic	ProSim	I/F and Libraries	DS-290-PC1	5.11	6.00			11/95
Viewlogic		I/F and Libraries	DS-391-xxx	5.11	6.00			11/95
XABEL		Entry, Sim, Lib, Opt.	DS-371-xxx	5.10	5.20	5.20	5.20	11/95
X-BLOX[1]		Module Generation & Opt.	DS-380-xxx	5.10	5.20	5.20	5.20	11/95
Verilog[2]	2K, 3K, 4K, 7K Lib.	Models & XNF Trans.	ES-VERILOG-xxx	N/A		1.00	1.00	N/A
XILINX PACKAGES								
Cadence	Standard		DS-CDN-STD-xxx	5.11		5.20	5.20	11/95
Mentor	Standard		DS-MN8-STD-xxx	5.11		5.20	5.20	11/95
Mentor	Advanced[3]		DS-MN8-ADV-xxx	N/A		7.00	7.00	N/A
OrCAD	Base		DS-OR-BAS-PC1	5.11	6.00			11/95
OrCAD	Standard		DS-OR-STD-PC1	5.11	6.00			11/95
Synopsys	Standard		DS-SY-STD-xxx	5.12		5.20	5.20	11/95
Synopsys	Advanced[3]		DS-SY-ADV-xxx	N/A		7.00	7.00	N/A
Viewlogic	Base		DS-VL-BAS-PC1	5.11	6.00			11/95
Viewlogic	Standard		DS-VL-STD-xxx	5.11	6.00	6.00	6.00	11/95
Viewlogic	Advanced[3]		DS-VL-ADV-xxx	N/A	7.00	7.00	7.00	N/A
Viewlogic/S	Base		DS-VLS-BAS-PC1	5.11	6.00			11/95
Viewlogic/S	Standard		DS-VLS-STD-PC1	5.11	6.00			11/95
Viewlogic/S	Extended		DS-VLS-EXT-PC1	5.11	6.00			11/95
Viewlogic/S	Advanced[3]		DS-VLS-ADV-PC1	N/A	7.00			N/A
XC8000	Extended	8K Core + Synthesis Libs.	DS-8000-EXT-xxx	N/A		1.00	1.00	N/A
3rd Party Alliance	Standard	FPGA/EPLD Core	DS-3PA-STD-xxx	5.10	6.00	5.20	5.20	11/95
3rd Party Alliance	Advanced[3]		DS-3PA-ADV-xxx	N/A	7.00	7.00	7.00	N/A
XILINX HARDWARE								
Device Pgmr.	PROM/EPLD/ XC8100 Pgmr.		HW-130	N/A	1.0			N/A
THIRD PARTY PRODUCTION SOFTWARE VERSIONS								
Cadence	Composer	Schematic Entry	N/A	4.2.2		4.3.3	4.3.3	N/A
Cadence	Verilog	Simulation	N/A	2.0.5		2.1.2	2.1.2	N/A
Cadence (Valid)	Concept	Schematic Entry	N/A	1.6		1.7-P4	1.7-P4	N/A
Cadence (Valid)	Rapidsim	Simulation	N/A	4.1		4.2	4.2	N/A
Data I/O	ABEL Compiler	Entry and Simulation	N/A	N/A	6.1	6.0		N/A
Data I/O	Synario	Entry and Simulation	N/A	N/A	2.1			N/A
Mentor	Design Architect	Schematic Entry	N/A	8.2_5		A.3-F	A.3-F	N/A
Mentor	QuickSim II	Simulation	N/A	8.2_5		A.3-F	A.3-F	N/A
OrCAD	SDT 386+	Schematic Entry	N/A	N/A	1.20			N/A
OrCAD	VST 386+	Simulation	N/A	N/A	1.20			N/A
Synopsys	FPGA/Design Comp.	Synthesis	N/A	3.3a		3.3b	3.3b	N/A
Viewlogic	ProCapture	Schematic Entry	N/A	N/A	6.10			N/A
Viewlogic	ProSim	Simulation	N/A	N/A	6.10			N/A
Viewlogic	ViewSynthesis	Synthesis	N/A	N/A	5.02x	2.3	2.3	N/A

NOTES: [1]FPGA only.
[2]Engineering software by request only.
[3]Advanced packages integrate NeoCAD Foundry tools.

PROGRAMMER SUPPORT FOR XILINX XC1700 SERIAL PROMS — NOVEMBER 1995

MANUFACTURER	MODEL	1736A 1765	17128	1718D 1736D 1765D	1718L 1765L	17128D	17256D	DIP8	PC20	SO8
ADVANTECH	PC-UPROG		V2.1	V2.0	V2.0	V2.1	V2.1	X		
	LABTOOL-48		V1.0	V1.0	V1.0	V1.0	V1.0	X	PLCC2020-01	
ADVIN	PILOT-U24	10.53	10.76C	10.71	10.77	10.78B	10.78B	X	PX-20	SO-8
	PILOT-U28	10.53	10.76C	10.71	10.77	10.78B	10.78B	X	PX-20	SO-8
	PILOT-U32	10.53	10.76C	10.71	10.77	10.78B	10.78B	X	PX-20	SO-8
	PILOT-U40	10.53	10.76C	10.71	10.77	10.78B	10.78B	X	PX-20	SO-8
	PILOT-U84	10.53	10.76C	10.71	10.77	10.78B	10.78B	X	PX-20	SO-8
	PILOT-142	10.73	10.76C	10.73	10.77	10.78B	10.78B	AM-1736	PX-20	SO-8
	PILOT-143	10.73	10.76C	10.73	10.77	10.78B	10.78B	AM-1736	PX-20	SO-8
	PILOT-144	10.73	10.76C	10.73	10.77	10.78B	10.78B	AM-1736	PX-20	SO-8
	PILOT-145	10.73	10.76C	10.73	10.77	10.78B	10.78B	AM-1736	PX-20	SO-8
B&C MICROSYSTEMS INC.	Proteus-UP40	V3.4e	V3.4e	V3.5f	V3.7f	V3.7I	V3.7I	X	AMUPLC84	
BP MICROSYSTEMS	CP-1128	C	V2.17*	V2.21c*	V2.34*	V3.06	V3.06	FH28A	FH28A + 3rd Party	FH28A + 3rd Party
	EP-1140	C	V2.17	V2.21c	V2.34	V3.06	V3.06	FH40A	FH40A + 3rd Party	FH40A + 3rd Party
	BP-1200	C	V2.17	V2.21c	V2.34	V3.06	V3.06	SM48D	SM20P or SM84UP	3rd Party
BYTEK	135H-FT/U	V42	V51	V51	V51			TC-824D		
	MTK-1000	V42	V51	V51	V51			TC-824D		
	MTK-2000	V42	V51	V51	V51			TC-824D		
	MTK-4000	V42	V51	V51	V51			TC-824D		
DATA I/O	UniSite	V4.0	V4.1	V4.1	V4.6	V4.8	V4.8	X	USBASE-PLCC	USBASE-SOIC
	2900	V2.1	V2.2	V2.2	V3.4	V3.6	V3.6	X	2900-PLCC	2900-SOIC
	3900	V1.5	V1.6	V1.6	V2.4	V2.6	V2.6	0101	3900-PLCC	3900-SOIC
	AutoSite	V1.5	V1.6	V1.6	V2.4	V2.6	V2.6	DIP-300-1	PLCC-20-2	
	ChipLab	V1.1	V1.0	V1.0	V1.1	V3.0	V3.0	X		080801S300
	2700	V3.0	V3.0	V3.0	V3.0	V3.0	V3.0			
DEUS EX MACHINA	XPGM		V1.00	V1.00	V1.00	V1.10	V1.10	Adapter 0	Adapter 0	Adapter 16
ELECTRONIC ENGINEERING TOOLS	ALLMAX/ALLMAX+	V1.3	V1.5	V1.5	V1.5	V2.3e	V2.3e	X		
	PROMAX	V2.34	V2.34	V2.34	V2.34	V2.34	V2.34	X	Module #4	
ELAN DIGITAL SYSTEMS	3000-145	C	C					A116		
	5000-145	C	C					A116		
	6000 APS	K2.01	K2.02	K2.01	K2.10	K2.14	K2.14	X	PDi84UPLC	PDi16USOI
HI-LO SYSTEMS RESEARCH	All-03A	V3.30	V3.30	V3.30	V3.30	V3.50	V3.50	X	CNV-PLCC-XC1736	CVN-SOP-NDIP16
	All-07	V3.30	V3.30	V3.30	V3.30	V3.47	V3.47	PAC-DIP40	PAC-PLCC44	
ICE TECHNOLOGY LTD	Micromaster 1000/1000E	V1.1	V3.00	V3.00	V3.07	V3.00	V3.00	X	AD-1736/65-PLCC	
	Speedmaster 1000/1000E	V1.1	V3.00	V3.00	V3.07	V3.00	V3.00	X	AD-1736/65-PLCC	
	Micromaster LV	V3.003	V3.00	V3.00	V3.00	V3.00	V3.00	X		
	LV40 Portable							X		
	Speedmaster LV		V3.00	V3.00	V3.00	V3.00	V3.00	X		
LEAP ELECTRONICS										
LINK COMPUTER GPHX	CLK-3100	V5.08	V5.08	V5.08				X17XXB	PLCC-17XX	SOIC-16
LOGICAL DEVICES	ALLPRO-40	V2.2						X	OPTPLC-208	OPTSOI-080
	ALLPRO-88	V2.2	V2.3	V2.3		V2.5	V2.5	X		OPTSOI-080
	ALLPRO-88XR	V1.1	V2.3	V1.3		V2.3	V2.3	X		OPTSOI-080
	CHIPMASTER 3000	V2.0	V2.1	V2.0	V2.3			X	OPTPLC-208	OPTSOI-080
	CHIPMASTER 5000	V1.15						X	OPTPLC-208	OPTSOI-080
	XPRO-1	V1.01	V1.01	V1.01	V1.01	V3.04	V3.04	MODXLN-173	MODXLN-173	MODXLN-173
MQP ELECTRONICS	MODEL 200	C	6.45	6.45	6.45	6.46	6.46	AD13A-16		
	SYSTEM 2600							MP6		
	PINMASTER 48							X		
MICRO PROSS	ROM 5000 B	C	V1.70	V1.70	V1.89	V1.89	V1.89	Mu 40		
	ROM 3000 U	C	V3.60	V3.60	V3.79	V3.79	V3.79			
	ROM 9000				V1.5	V1.5	V1.5			
NEEDHAM'S ELECTRONICS	EMP20	V1.5	V1.5	V2.37	V2.37	V2.37	V2.37	04B		
RED SQUARE	IQ-180	C	V9.2	V8.2	V9.2	V9.2	V9.2			
	IQ-280	C	V9.2	V8.2	V9.2	V9.2	V9.2			
	Uniwriter 40	C	V9.2	V8.2	V9.2	V9.2	V9.2			
	Chipmaster 5000	C	V9.2	V8.2	V9.2	V9.2	V9.2			
SMS	Expert	B/93	A/94	A/94	A1/94	Cx/94	Cx/94	TOP40DIP	TOP1PLC or	
	Optima	B/93	A/94	A/94	A1/94	Cx/94	Cx/94	"	TOP3PLC/TOP3PLC	
	Multisyte			A/94		Cx/94	Cx/94	"	"	
	Sprint Plus48	B/93	A/94	A/94	A1/94					
STAG	Eclipse		4.4	V2.2	V4.3	V4.10.31	V4.10.31	EPU48D	EPU84P	
	Quasar	10.76C	10.76C	V10.76C	V10.76C	V10.78B	V10.78B	X	AMPLCC20	
SUNRISE	T-10 UDP	V3.31	V3.31	V3.31	V3.31	V3.31	V3.31	X	X	X
	T-10 ULC	V3.31	V3.31	V3.31	V3.31	V3.31	V3.31	X	X	X
SUNSHINE	POWER-100	V8.18	V8.18	V8.18	V8.18	V8.18	V8.18	X		
	EXPRO-60/80	V8.18	V8.18	V8.18	V8.18	V8.18	V8.18	X		
SYSTEM GENERAL	TURPRO-1	V2.21F	V2.21F	V2.21F	V2.21F	V2.21F	V2.21F	DIP-Adapter	P20-Adapter	
	Turpro-1 F\X	V2.21F	V2.21F	V2.21F	V2.21F	V2.21F	V2.21F	DIP-Adapter	P20-Adapter	
	APRO	C	V2.14	V2.01	V2.12				X	X
TRIBAL MICROSYSTEMS	TUP-300	C	V3.31	V3.31	V3.37C	V3.47	V3.47	X	CNV-PLCC-XC1736	
	TUP-400	C	V3.31	V3.31	V3.37C	V3.50	V3.50	X	"	
	FLEX-700	C	V3.31	V3.31	V3.37C	V3.47	V3.47	X	"	
XELTEK	SuperPRO	1.5B	1.7C	1.7D	1.8	2.2A	2.2A	X*	20-PL/8-D-ZL-XC1736	16SO15/D6-ZL
	SuperPRO II	1.5B	1.7C	1.7D	1.8	2.2A	2.2A	X*	20-PL/8-D-ZL-XC1736	16SO15/D6-ZL
XILINX	HW-112	4:02	4:06	4:06	4:05	4:05	4:06	X	HW-112-PC20	HW-112-SO8
	HW-120	2:03	2:03	2:03	2:03	3:01	3:01	HW-120-PRM	HW-120-PRM	HW-120-PRM
	HW-130		2:00	2:00	2:00	2:00	2:00	HW-137-DIP8	HW-137-PC20/SO8	HW-137-PC20/SO8

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Programmer Support for Xilinx XC7200 EPLDs — November 1995

VENDOR	MODEL	7236	7236A	7272	7272A	PC44	PC68	PC84	PG84	Comments
Advantech	PC-UPROG LabTool-48	V2.4 V1.0	V2.4 V1.0	V2.4 V1.0	V2.4 V1.0	X SDP-UNIV-44	SDP-7272-68 SDP-7272-68	SDP-7272-84 SDP-7272-84		
Advin Systems	Pilot-U40 Pilot-U84	10.77E 10.77E	10.77E 10.77E	10.77E 10.77E	10.77E 10.77E	USA-84 USA-84	USA-84 USA-84	USA-84 USA-84	 AM-XC84G	
B&C Microsystems, Inc.	Proteus	V3.6j	V3.6j	V3.7h	V3.7h	AMUPLC84	AMUPLC84	AMUPLC84		
BP Microsystems	BP-1200	BBS	BBS	v2.34	v2.34	SM44P	SM68P or SM84UP	SM84P or SM84UP	SM84UGA	
DATA I/O	UniSite 2900 3900 AutoSite	v4.3 V3.4* v2.1 V2.4*	v4.6* V3.4* V2.4* V2.4*	v4.5 v2.3 v2.3	v4.5** v2.3** v2.3**	USBASE-PLCC PPI-0243 3900-PLCC PLCC-44-1	USBASE-PLCC PPI-0246 3900-PLCC PLCC-68-1	USBASE-PLCC PPI-0208 3900-PLCC PLCC-84-1		*7236A=PPI-0243 **7272A=PPI-0246 (PC68) **7272A=PPI-0247 (PC84)
Deus Ex Machina	XPGM	V1.00	V1.00	V1.00	V1.00	Adapter 1	Adapter 2	Adapter 3		
Elan Digital Systems	6000 APS	K2.04	K2.04	K2.06	K2.06	PDi84UPLC	PDi84UPLC	PDi84UPLC	PDi84PGx	
Electronic Engineering Tools	ALLMAX/ALLMAX+ PROMAX	V2.1 V2.34	V2.1 V2.34	V2.1 V2.5	V2.1 V2.5	Module 05+PA44-84U Module 19 + H44	PA68-48A	PA84-48A		
Hi-Lo Systems Research	All-03A All-07	V3.01 V3.01	V3.01 V3.01	V3.00 V3.00	V3.00 V3.00	ADP-XC7236-PL44 PAC-PLCC44	ADP-XC7272-PL68 PAC-PLCC68	ADP-XC7272QPI-84		
ICE Technology Ltd.	Micromaster 1000/E Speedmaster 1000/E Micromaster LV Speedmaster LV	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	AD-XC7236-PLCC-44 AD-XC7236-PLCC-44 AD-XC7236-PLCC-44 AD-XC7236-PLCC-44	AD-XC7272-PLCC-68 AD-XC7272-PLCC-68 AD-XC7272-PLCC-68 AD-XC7272-PLCC-68	AD-XC7272-PLCC-84 AD-XC7272-PLCC-84 AD-XC7272-PLCC-84 AD-XC7272-PLCC-84		
Leap Electronics										
Logical Devices	ALLPRO-88 ALLPRO-88XR XPRO-1	2.2 1.35 3.3	V2.4 V2.4 3.3	2.2 1.35 1.01	V2.4 V2.4 1.01	C C MODXP1-44L	C C MODXP1-68L	C C MODXP1-84L	 MODXP1-84G	
Microprogss	ROM 9000									
MQP Electronics	SYSTEM2000 PINMASTER48					MP1	MP1	MP1		 Universal Programmer
Needham's Electronics	EMP20	V2.37	V2.37	V2.37	V2.37	19A+H44	20A+U68CB	20A+U84CB		
Stag	Eclipse	V5.7.3	V5.7.3	V5.7.3	V5.7.3	EPU84P+	EPU84P+	EPU84P+		
SMS	Expert Optima Multisyte	A1/94 A1/94 A1/94	A1/94 A1/94 A1/94	A1/94 A1/94 A1/94	A1/94 A1/94 A1/94	TOP1 TOP1 TOP1	TOP1 TOP1 TOP1	TOP1 TOP1 TOP1		
Sunrise Electronics	T-10 UDP T-10 ULC	V3.31 V3.31	V3.31 V3.31	V3.31 V3.31	V3.31 V3.31	X X	X X	X X	X X	All adapters are custom All adapters are custom
Sunshine Electronics	POWER-100 EXPRO-60/80	V8.16 V8.16	V8.16 V8.16			CNV-UNIVERSAL-PLCC44 CNV-UNIVERSAL-PLCC44				
System General	TURPRO-1 TURPRO-1FIX	v2.12 v2.12	v2.12 v2.12	v2.12 v2.12	v2.12 v2.12	P44 P44	P68 P68	P84 P84		
Tribal Microsystems	TUP-300 TUP-400 FLEX-700	v3.0 v3.0 v3.0	v3.0 v3.0 v3.0	v3.0 v3.0 v3.0	v3.0 v3.0 v3.0	TUP-7236 TUP-7236 TUP-7236	TUP-7272 TUP-7272 PAC-PLCC68			 PAC-PLCC44
Xeltek	SUPERPRO SUPERPRO II	1.7C 1.7C	2.2 2.2	2.1 2.1	2.1 2.1	XXC7236-44PL/40D XXC7236-44PL/40D	XXC7272-68PL/68D XXC7272-68PL/68D	XXC7272-84PL/84D XXC7272-84PL/84D		
Xilinx	HW-120 HW-130	2:02 1:02	2:02 1:02	2:02 1:02	2:02 1:02	HW-120-PC44 HW-132-PC44	HW-120-PC68 HW-132-PC68	HW-120-PC84 HW-132-PC84	HW-120-PG84 HW-132-PG84	*HW-12x EPLD adapters

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PROGRAMMER SUPPORT FOR XILINX XC7300 EPLDS — NOVEMBER 1995

VENDOR	MODEL	7318	7336	7336Q	7354	7372	73108	73144	PC44	PC68	PC84	PQ44	PQ100	PG144	PQ160	BG225
ADVANTECH	PC-UPROG LabTool-48	V2.4 V1.0	V2.4 V1.0		V2.4 V1.0	 V1.04	 V1.04		X SDP-UNIV-44	SDP-7354-68 SDP-7354-68	 X					
ADVINSYSTEMS	PILOT-U40 PILOT-U84	10.78N 10.78B	10.78N 10.78B		10.78N 10.78B	10.78N 10.78B	10.79 10.79		USA-84 USA-84	USA-84 USA-84	USA-84 USA-84		AM-XC100Q AM-XC100Q	AM-XC144G AM-XC144G	AM-XC160Q AM-XC160Q	
B&C MICROSYSTEMS	Proteus	3.7k	3.7k		3.7k		3.7k		C	C	C					
BP MICROSYSTEMS	BP-1200	V3.01	V3.01		V3.01	V3.07	V3.06A		SM44P		FHSM84PX					
DATA I/O	2900 3900/AutoSite UniSite	V3.5 V2.5 V4.7	V3.5 V2.5 V4.7		V3.5 V2.5 V4.7	 V2.6 V4.8	 V2.6 V4.8		2900-PLCC 3900-PLCC USBASE-PLCC	 3900-PLCC USBASE-PLCC	 3900-PLCC USBASE-PLCC	0529 0529 0529	 0557 0557		0558 0558	 PPI-1101 PPI-1101
DEUS EX MACHINA	XPGM	V1.00	V1.00	V1.30	V1.00	V1.10	V1.10		Adapter 5	Adapter 6 (13 for 7372)	Adapter 7				Adapter 9	
ELAN	6000APS	k2.13	k2.13		k2.13	k2.13	k2.13		PDi84UPLC	PDi84UPLC	PDi84UPLC	PDi044QFx	PDi100QFx	PDi160QFx		
ELECTRONIC ENGINEERING TOOLS	ALLMAX/ALLMAX+ PROMAX	V2.1 V2.34	V2.1 V2.34		V2.1 V2.34	V2.1 V2.57			Module 04+PA44-48U Module #19 + H44	PA68-48B (7354) PA68-48C (7372)	PA84-48B					
HI-LO SYSTEMS RESEARCH	All-03A All-07	V3.04 V3.02	V3.04 V3.02		V3.04 V3.02	V3.05 V3.01	V3.01 V3.00		ADP-XC7336-PL44 PAC-PLCC44	ADP-XC7372-PL68 PAC-PLCC68	ADP-XC73108-PL84					
ICE TECHNOLOGY LTD	Micromaster 1000/E Speedmaster 1000/E Micromaster LV SpeedmasterLV	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00		VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00		AD-73XX-PLCC-44 AD-73XX-PLCC-44 AD-73XX-PLCC-44 AD-73XX-PLCC-44	AD-7354-PLCC-68 AD-7372-PLCC-68 AD-7354-PLCC-68 AD-7372-PLCC-68 AD-7354-PLCC-68 AD-7372-PLCC-68 AD-7354-PLCC-68 AD-7372-PLCC-68	AD-73XX-PLCC-44 AD-73XX-PLCC-44 AD-73XX-PLCC-44 AD-73XX-PLCC-44					
LEAP ELECTRONICS																
LOGICAL DEVICES	ALLPRO-88 ALLPRO-88XR XPRO-1	V2.5 V2.5 3.3	V2.5 V2.5 3.3		V2.5 V2.5 1.01	V2.5 V2.5 1.01	V2.5 V2.5 1.01		C C MODXP1-5444L	C C MODXP1-5468L	C C MODXP1-108L				MODXP1-160Q	MODXP1-108B
MICROPROSS	ROM 9000															
MQP ELECTRONICS	SYSTEM 2000 PINMASTER 48								MP1	MP1	MP1					
NEEDHAM'S ELECTRONICS	EMP20	V2.37	V2.37		V2.37	V2.37	V2.37		19B + H44	20A + U68CA	20A + U84CA					
SMS	EXPERT OPTIMA	C/94 C/94	C/94 C/94		C/94 C/94				TOP1 TOP1	TOP1 TOP1	TOP1 TOP1					
STAG	ECLIPSE	V4.10.31	V4.10.31		V4.10.31	V4.10.31	V4.10.31									
SUNRISE	T-10 UDP T-10 ULC	V3.31 V3.31	V3.31 V3.31		V3.31 V3.31	V3.31 V3.31	V3.31 V3.31		X X	X X	X X					
SUNSHINE	POWER-100 EXPRO-60/80								CNV-UNIVERSAL-PLCC44 CNV-UNIVERSAL-PLCC44							
SYSTEMGENERAL	TURPRO-1	V2.2	V2.2		V2.2	V2.2	V2.2		C							
TRIBAL MICROSYSTEMS	Flex-700 TUP-300 TUP-400	V3.02 V3.03 V3.03	V3.02 V3.03 V3.03		V3.02 V3.03 V3.03	V3.01 V3.03 V3.03	V3.00		PAC-PLCC44	PAC-PLCC68						
XELTEK	SUPERPRO SUPERPRO II	2.1 2.1	2.2A 2.2A		2.1 2.1	2.2B 2.2B			XXC7354-44PL/40D XXC7354-44PL/40D	XXC7354-68PL/40D XXC7354-68PL/40D						
XILINX	HW-120 HW-130	3:13 1:13	3:13 1:18	1:00 1:03	3:00 1:34	1:01 1:08	3:01 1:03	1:00	HW-126-PC44 HW-133-PC44	HW-126-PC68 HW-133-PC68	HW-126-PC84 HW-133-PC84	HW-126-PQ44 HW-133-PQ44	HW-126-PQ100 HW-133-PQ100	HW-126-PG144 HW-133-PG144	HW-126-PQ160 HW-133-PQ160	HW-126-BG225 HW-133-BG225

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Xilinx Achieves Impressive Reliability Results

Because Xilinx FPGAs are built on a standard, highly-reliable CMOS SRAM process, Xilinx has outstanding quality results. The following data is from the Xilinx internal reliability monitor. A FIT is a Failure In Time measured as failures that occur in one billion (10^9) hours of device operation. If you are more familiar with Mean Time to Failure (MTTF) as a measure of reliability, then just take the inverse of the FIT measurement:

FIT = failures/10^9 hours = 1/MTTF

For example, equipment that contains 1,000 devices, each with a 4 FITs reliability level, has a 50 percent probability of having one device failure in 10^9/(4 x 1000) = 250,000 hours (about 30 years) of uninterrupted operation (24 hours/day).

As is clear from the chart, Xilinx continues to deliver world-class reliability in these high-volume FPGA products. Xilinx FPGAs have significantly better reliability than many other forms of logic.

Xilinx's quality and reliability guide, available from your local sales representative, is updated on a quarterly basis. ◆

Static and Dynamic High Temperature Operating Life (HTOL) Test • FIT Rate at 70°C

Quarter	XC2000	XC3000	XC3100	XC4000
June 1992	6.0 FIT	20.0 FIT	-	45.0 FIT
June 1993	4.0 FIT	28.0 FIT	23.0 FIT	35.0 FIT
June 1994	5.0 FIT	21.0 FIT	10.0 FIT	38.0 FIT
June 1995	1.0 FIT	17.0 FIT	1.0 FIT	29.0 FIT

Xilinx Earns ISO 9002 Certification

International Recognition Complements Awards From Customers

The Xilinx manufacturing facility in San Jose, California obtained certification in October to ISO 9002 — "Quality Systems - Model for Quality Assurance in Design, Development, Production, Installation, and Servicing."

The ISO quality standards were developed by the International Organization for Standardization, a Geneva-based organization with representatives from 91 countries. In simple terms, the ISO 9000 standards state that you must document what you do, perform to the documents, and record the results.

The high quality standards at Xilinx have not gone unnoticed by our users. Recent awards received from Xilinx customers include:

- Honeywell's "Top Rated Supplier"
- Bull's "Quality Vendor"
- Kodak's "Class-B Certification"
- Siemen's "72500 Compliant"
- AT&T's "Partners in Qualification"

Each of these certifications involves "dock-to-stock" programs, wherein the companies do not inspect Xilinx products on receipt, instead relying on the inspection and testing programs at Xilinx, and, thereby, saving considerable time and expense.

Xilinx currently is undertaking an intensive program to achieve ISO 9002 certification for the new manufacturing facility in Dublin, Ireland in 1996. ◆

A company must earn high ratings in these 19 elements to earn ISO 9002 certification:

1. Management responsibility
2. Quality system
3. Contract review
4. Document and data control
5. Purchasing
6. Control of customer-supplied product
7. Product identification and traceability
8. Process control
9. Inspection and testing
10. Control of inspection, measuring, and testing equipment
11. Inspection and test status
12. Control of nonconforming product
13. Corrective and preventive action
14. Handling, storage, packaging, preservation, and delivery
15. Control of quality records
16. Internal quality audits
17. Training
18. Servicing
19. Statistical techniques

XC8100 Shines in 6502 Processor Benchmark

As reported in the December 1994 issue of *Electronic Engineering Times*, VHDL model vendor **VAutomation Inc**. has evaluated several different FPGA technologies using a technology-independent VHDL description of the 6502 8-bit microprocessor.

VAutomation's V6502 synthesizable module allows this processor to be integrated into an ASIC device along with other logic and memory functions. However, their customers often want to prototype the ASIC design prior to committing to silicon, thus providing the motivation to test how this model is implemented in FPGAs.

The design was compiled with PC-based synthesis tools from Exemplar Logic, using the default constraints. Each implementation was then placed and routed using the respective FPGA vendor's tools, again using default settings. The V6502 proved a difficult model to implement in an FPGA since it is very logic intensive; that is, the model has a high ratio of logic gates to flip-flops, largely due to the large amount of highly-interconnected logic needed to decode the processor's opcodes.

VAutomation recently benchmarked the XC8106 FPGA using the V6502 model. The XC8100 architecture is designed to be especially efficient when using top-down, high-level design methodologies. Since the XC8100 logic cell can be used to implement either logic or register functions, the ratio of logic gates to registers in the design has little effect on utilization. As a result, the design fit into a 6,000-gate XC8106 device, as opposed to requiring 10,000-gate or larger devices in other FPGA technologies *(see Table 1)*. The design uses 90 percent of the cells in the XC8106.

The VAutomation engineer was able to install the XC8100 design tools, learn their use, and complete the design within five days of receiving the beta site software from Xilinx. After completing the design and programming the device, the chip was plugged into an adapter that attached to the 6502's socket in an Apple IIc computer. The computer was then booted up, and it worked the very first time!

Table 2 shows the production status of XC8100 devices and the XACT*step* Series 8000 development tools. Please contact your local Xilinx sales representative for further pricing and availability information. ◆

Table 1: Utilization Comparison

Device	Vendor's Claimed Gate Capacity	Logic Block Utilization for V6502 Implementation	Number of Required "FPGA Gates"*
FPGA - Vendor A1	15,000	81%	12,150
FPGA - Vendor A2	10,000	96%	9,600
Xilinx XC8106	5,600	90%	5,040

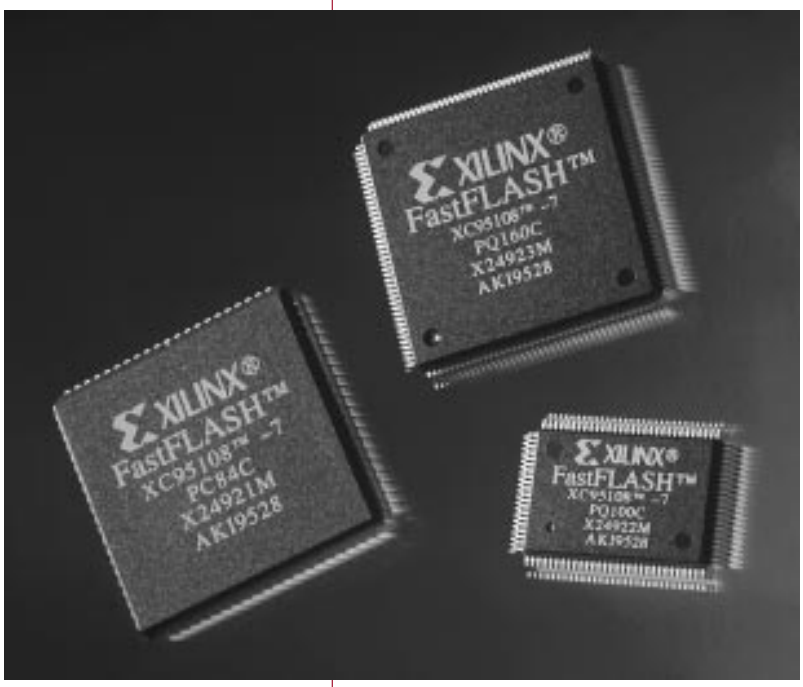
** as based on vendor's claimed capacity*

Table 2: Production Status

	Samples	Production
XC8100 PC44	Contact Factory	1Q96
XC8101 PC84; PQ100	Now	Now
XC8103 PC84; PQ100	Now	Now
XC8106 PC84; PQ100	Now	Now
XC8109 PC84; PQ160; BG225	Now	1Q96
XACTstep Series 8000 software		
Workstation version 1.0		Now
PC version 1.1		12/95
HW-130 Programmer		Now

XILINX®

Introducing the FastFLASH XC9500



The new XC9500 family is the second generation of Xilinx CPLDs, developed especially for system designers who require complete in-system programming, test and manufacturing capability. The XC9500 family provides a total product life cycle support solution from initial prototyping to system integration, manufacturing and field upgrades. It also offers the industry's best pin-locking capability, a necessity for maintaining device pinouts throughout the complete product life cycle.

The innovative FastFLASH technology provides exceptional in-system programmable (ISP) capabilities by offering more than 10,000 program/erase cycles — one or two orders of magnitude more than other comparable CPLDs. This high endurance level allows the XC9500 devices to be used in applications requiring frequent field upgrades and reconfigurations.

In addition, the XC9500 family provides both superior density and performance, with seven devices ranging in density from 800 to 6,400 usable gates, and pin-to-pin propagation delays as fast as 5 ns.

Product Features

- High-performance
  - — 5 ns pin-to-pin logic delays on all pins
  - — Maximum external frequency to 145 MHz
- Large density range
  - — 36 to 288 macrocells with 800 to 6,400 usable gates
- 5 V in-system programmability (ISP)
  - — Endurance of 10,000 program/erase cycles
  - — Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
- Extensive IEEE 1149.1 boundary-scan (JTAG) support
- Programmable speed/power options on individuals macrocells
- Slew rate control on individual outputs
- User programmable ground pins capability
- Extended pattern security features for design protection
  - — Read security bit prevents unauthorized copying of design
  - — Write security bit protects against inadvertent user programming/erase
- High-drive 24 mA outputs with 3.3 V or 5 V I/O
- 100-percent PCI compliant (-10, -7 speed grades)
- Advanced 0.6µm CMOS 5 V FastFLASH technology

Product Life Cycle Support

During the prototyping stage, a device might be reprogrammed hundreds of times while soldered on a printed circuit board (PCB). If the architecture does not support locking the device pinout, an expensive and time-consuming re-layout

Family *The Industry's Most Complete Solution for In-System Programmable CPLDs.*

of the PCB is necessary. The XC9500 family provides industry-leading pin-locking capability for preserving PCB board layout throughout the design cycle.

When the entire system is assembled for test and debug, all important logic states should be easily accessible, and internal logic implementations within each CPLD should be capable of being checked. Each XC9500 device supports the IEEE 1149.1 boundary scan specification, including INTEST and USERCODE instructions used to access and debug user logic and track pattern revisions, respectively. In addition, both the superior pin-locking and high endurance features of the XC9500 family are critical in facilitating design modifications during the debugging process.

Full JTAG Support

The XC9500 family expands the manufacturing process capability with the industry's most complete IEEE 1149.1 JTAG support. By integrating device programming with final board testing, the XC9500 technology eliminates the need for stand-alone mark and programming steps. Built-in version control, concurrent programming of multiple devices and in-system board customization all contribute to manufacturing flexibility.

Since the XC9500 family is easily programmed through the JTAG port, field upgrades to the CPLD's configuration are possible. The industry's best pin-locking architecture ensures against changes to the PCB layout.

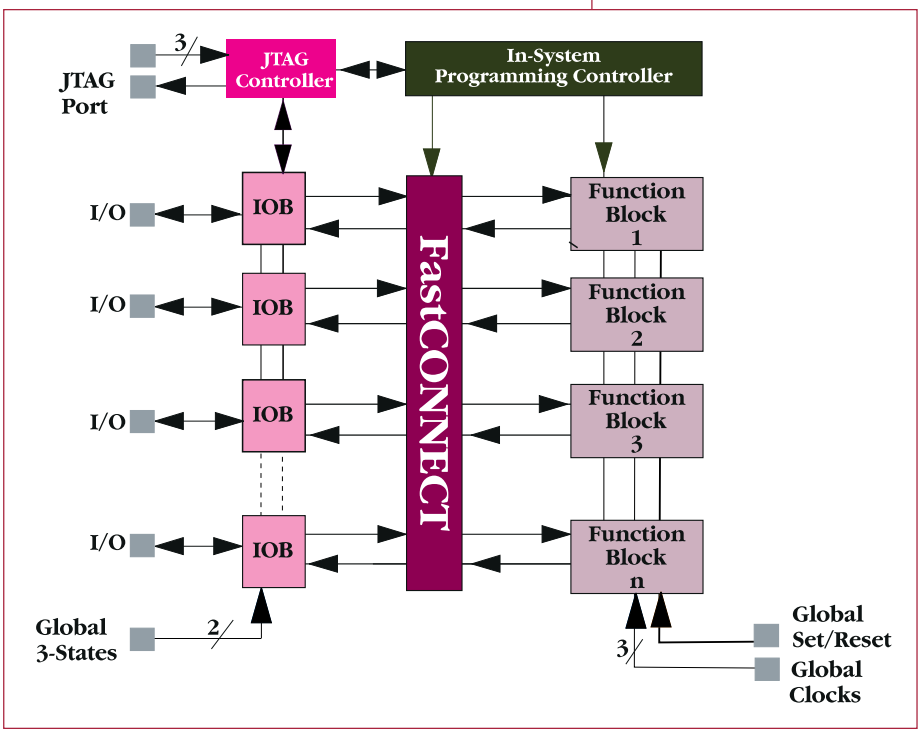
Simple Yet Flexible Architecture

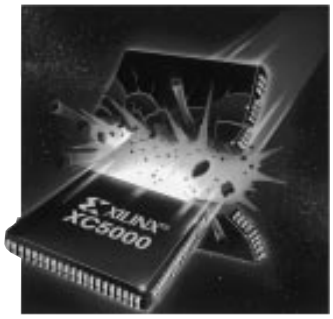
Each XC9500 device may be viewed as a subsystem consisting of "36V18-type" Function Blocks and I/O Blocks interconnected by the FastCONNECT™ switch matrix. As you have come to expect from Xilinx CPLDs, the full FastCONNECT switch matrix provides 100-percent interconnect of all pins and function block outputs to all function block inputs. Additionally, wide function block fan-in (36 total inputs) and flexible product term allocation work with the FastCONNECT matrix to ensure that design changes will not cause changes to the device pinouts.

The XC95108, featuring approximately 2,400 usable gates and up to 160 I/O pins and its software support tools are available now. The remaining six devices in the XC9500 family will become available throughout 1996.

The new XC9500 CPLD family, based on the industry's first 5 V Flash ISP process, provides CPLD users the best solution for addressing their needs throughout the entire product life cycle: design, system integration, volume manufacturing, and field upgrades. ◆

XC9500 Architecture





XC5200 Family Now In Volume

All XC5200 family devices and the supporting XACT*step*™ design software are now in volume production. With five devices — ranging from 2,000 to 18,000 usable gates — offered in 15 different packages, there are now more than 100 different device/package/speed combinations available to meet the most exacting design requirements. Complete footprint compatibility between all devices in a common package allows the migration to higher or lower density devices without modifying the printed circuit board. All XC5200 devices are also footprint-compatible with the XC4000 and XC8100 families.

By optimizing the XC5200 family for a 0.6 micron, three-layer-metal SRAM process and by delivering architectural innovations, Xilinx has dramatically reduced die area and size. Xilinx now provides the industry's highest value family of FPGAs.

Device	Usable Gates
XC5202	2,200–2,700
XC5204	3,900–4,800
XC5206	6,000–7,500
XC5210	10,000–12,000
XC5215	14,000–18,000

With powerful new features such as the VersaRing™ I/O interface, dedicated JTAG logic for increased testability, and fast carry logic for high speed arithmetic functions, the XC5200 is the optimal solution

XC3100A-09: *The World's Fastest FPGA*

The popular XC3100A family has attained a 50 percent boost in performance from changes in manufacturing process and layout. The new XC3100A-09 and XC3100A-1 devices were designed with an optimized 0.6µ, triple-layer-metal process technology.

The XC3100A-09 has 40 percent shorter block delays, 50 percent faster chip-to-chip speed and decoding functions, as well as 100 percent faster interconnect speed compared with the XC3100A-2 device *(see Table 1)*.

Fully PCI compliant, the XC3100A is ideal for high-speed serial-to-parallel conversions, fast ATM switches, video control functions and 3D graphics/imaging. Designs which require high-speed clock distribution can also benefit.

The Software Help area of the Xilinx bulletin board (408-559-9327) contains advance speed files for use with XACT™ design software. The combination of XC3100A silicon and XACT*step*-Performance™, Xilinx's timing-driven placement software, provide a high level of productivity for high-performance designs.

The new XC3100A devices are fully backward compatible with earlier XC3100A devices (that is, they may be dropped in with the same bitstream). *See Table 2 for device availability.* ◆

Table 1
-09 vs. -02 Performance Comparisons

	XC3100A-09	XC3100A-2
Combinatorial Delay	1.4 ns	2.2 ns
Clock to Out (pin-to-pin)	6 ns	7.8 ns
Setup (pin-to-pin)	3.5 ns	6.5 ns
Interconnect (normalized)	4.4 ns	10 ns
State Machine	112 MHz	68 MHz
Data Path	356 MHz	233 MHz
Max Chip-to-Chip	110 MHz	70 MHz

Table 2
XC3100A-09 and XC3100A-1 Availability

Device	Sampling	Production
XC3120A	December	2Q96
XC3130A	December	2Q96
XC3142A	Now	2Q96
XC3164A	December	2Q96
XC3190A	Now	1Q96
XC3195A	Now	1Q96

Production

for high density designs not requiring the high performance and on-chip RAM of the XC4000 series.

The XC5200 family is completely integrated into the powerful XACT*step* design tools. All in-warranty users will receive XC5200 software as part of the XACT*step* version 6 (Windows) and XACT*step* 5.2 (DOS) production release.

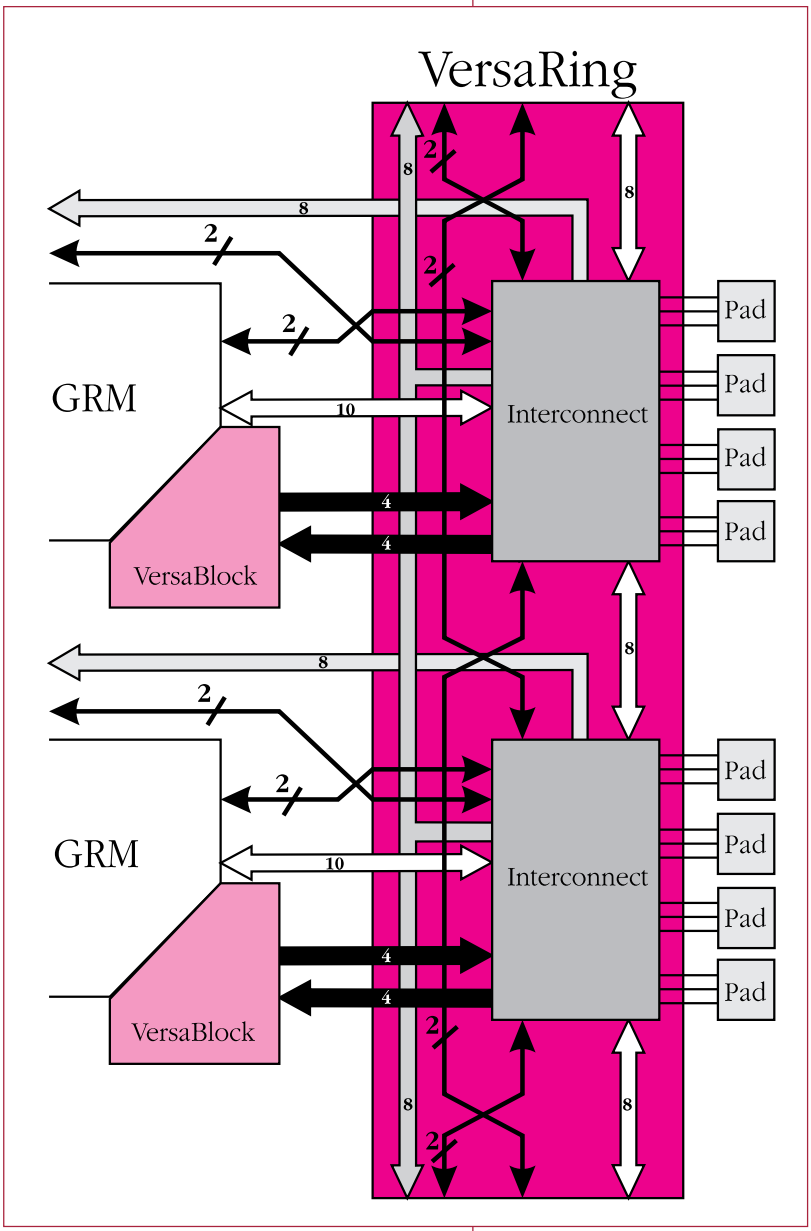
VersaRing Increases Pin Locking Flexibility

As an increasing number of users design with the XC5200 family, one thing is becoming clear — the VersaRing I/O interface is delivering on its promise of allowing users to make last minute logic changes **without** having the pinouts change, forcing a new PCB layout. Designers have long wanted an FPGA solution that allowed the flexibility of pre-assigning, or "locking," I/O locations before the logic design was completed. This facilitates an early release of the PCB design, thereby accelerating total system design time.

The VersaRing feature of the XC5200 architecture provides an incremental layer of routing resources along the edge of the device *(see diagram)*. This gives the routing software dramatically improved freedom to pre-assign pins, since connections between IOBs and CLBs can now be made by routing along the edge of the device rather than through the core logic. It's important to note, however, that while the VersaRing provides a dramatic improvement in pin-locking capability, it cannot provide the same pin-locking guarantee that can be made by Xilinx EPLDs, with their 100-percent connectivity of the Universal Interconnect Matrix (UIM™).

It's a fact that designs change during all stages of the design/manufacturing cycle. The XC5200 VersaRing enhances the benefits of reprogrammability by allowing more of these changes to occur without forcing a PCB modification. Combined with the lowest cost per gate of any FPGA solution and system performance extending to 50 MHz, the XC5200 delivers a very robust solution for designs up to 18,000 gates.

Please contact your local Xilinx sales representative for the latest information on XC5200 family availability and pricing. ◆



XC4000 Hi-Rel Product Family

Extended with Faster Speed Grades and New Packaging

Xilinx's ongoing commitment to high-reliability defense and aerospace applications continues. New hi-rel products that have been qualified recently include higher-performance versions of the XC4005 and XC4010 FPGAs and a new surface-mount package for the XC4013 FPGA.

With the introduction of hi-rel versions of the XC4005-5 and XC4010-5 products, the hi-rel XC4000 family has reached new performance levels, expanding the range of applications that can be addressed by these full-featured FPGAs. Both of these new devices are available in ceramic pin grid array (PG) and surface-mount ceramic quad flat pack (CB) packages.

The XC4013 FPGA is now available in a hi-rel surface-mount package, the CB228, a 228-pin ceramic quad flat pack. This package features a non-conductive tie-bar that improves handling and eliminates bent leads during test and shipment. Hi-rel versions of the XC4013 are available in both the -10 and -6 speed grades.

These new products are now fully-qualified in M grade, B grade, and SMD versions (see table). Like all the XC4000 family members, they include the powerful features, such as built-in JTAG test circuitry, on-chip RAM, fast carry logic, and wide edge decoders, that have made the XC4000 the world's most-used FPGA family. ◆

Hi-Rel Part Number Matrix (New Products)

Xilinx Part Number	SMD Part Number	Comments
XC4005-5PG156M	N/A	Pin Grid Array
XC4005-5PG156B	5962-9225203MXC	Pin Grid Array
XC4005-5CB164M	N/A	Quad flat pack with base mark
XC4005-5CB164B	5962-9225203MZC 5962-9225203MYC	Quad flat pack with base mark Quad flat pack with lid mark
XC4010-5PG191M	N/A	Pin Grid Array
XC4010-5PG191B	5962-9230503MXC	Pin Grid Array
XC4010-5CB196M	N/A	Quad flat pack with base mark
XC4010-5CB196B	5962-9230503MYC 5962-9230503MZC	Quad flat pack with base mark Quad flat pack with lid mark
XC4013-10CB228M	N/A	Quad flat pack with base mark
XC4013-6CB228M	N/A	Quad flat pack with base mark
XC4013-10CB228B	5962-9473001MYC 5962-9473001MZC	Quad flat pack with base mark Quad flat pack with lid mark
XC4013-6CB228B	5962-9473002MYC 5962-9473002MZC	Quad flat pack with base mark Quad flat pack with lid mark

Thank You

To the participants of the 3.3V Fax-Back Survey (XCELL #17, page 31):

Thank you very much for your participation. We had many responses from all over the world. We are especially appreciative of the responses from outside the United States. We will use the data to continue providing you with leading-edge low-voltage logic solutions.

Leo Laperriere of CAE Electronics in Canada was the winner in the drawing for the Sony Watchman. Congratulations Leo! ◆

Leo Laperriere

Logic Synthesis for FPGAs - An Update

As FPGA designs get larger and more complex and time-to-market pressures continue to increase, more designers are turning to VHDL or Verilog-HDL based design flows. Xilinx remains firmly committed to supporting these users.

Synthesis for Xilinx FPGAs has taken major steps forward during 1995. We are now seeing cases where synthesis tools can produce results that are smaller and faster than a schematic design for modest size functions (such as a digital filter).

At the beginning of the year, only a few vendors were performing full mapping to the basic logic elements of Xilinx devices. This "what you synthesize is what you get" (WYSIWYG) methodology is preferred by ASIC designers familiar with VHDL/Verilog-HDL design. It provides a very high degree of correlation between the synthesis results and the final device, while also assuring that cell delay and interconnect delay estimates made during the synthesis process are consistent with the actual delays calculated by the FPGA implementation software later in the design process.

This design methodology was first supported by the **Synopsys** FPGA Compiler; it began supporting full mapping to XC4000 CLB and IOB structures in February 1993. Synopsys extended their FPGA support to include generic look-up table (LUT) mapping in the FPGA Compiler v3.3a release in March 1995. Xilinx took advantage of this feature to implement full mapping to the function generators (LUTs) of the XC3000 and XC5200 families with libraries released in the Xilinx-Synopsys Interface (DS-401) version 3.3 in June 1995. Other vendors, including **Data I/O, Viewlogic, Exemplar Logic, IST**, and **Synplicity**, have followed Synopsys' lead by implementing WYSIWYG design flows for the XC3000, XC4000 and XC5200 families during 1995.

The **XC5200** family is of particular interest because, from a synthesis standpoint, its architecture is simpler and more regular than the XC3000 and XC4000. If a synthesis tool can map to 4-input look up tables (LUTs) and registers, and map arithmetic functions to X-BLOX™ elements (in order to use the fast carry logic), that synthesis compiler will be using all of the XC5200 logic resources. With the attractive pricing of the XC5200 family, these devices can be used as a production solution for 5,000-15,000 gates.

The new **XC8100** FPGA family also supports a WYSIWYG synthesis. Its fully-configurable logic cell can be supported by any conventional, cell-based synthesis tool, eliminating the need for special synthesis algorithms. These tools, rather than targeting the look-up table elements found in the SRAM-based Xilinx devices, target a set of logic functions in a library. For each of the library's logic cells, there will be a particular configuration of one or more Configurable Logic Cells (CLCs) in the XC8100 architecture that corresponds to that function. The XC8100 is supported by synthesis libraries for

Continued on the next page

What You SYNTHESIZE Is What You Get

XILINX®

Executing from the XACTstep CD-ROM

To preserve precious space on your PC's hard disk, XACT*step*™ version 6 and Viewlogic PRO Series programs can be executed directly from the CD-ROM without being installed on the system's hard drive. Users must configure the system properly and set up a program group in Windows® to access the software located on the CD-ROM correctly. When executing from CD-ROM, the graphical tools will seem to take longer. Non-graphical programs, such as PPR, will be delayed only two to five minutes depending on the program loading time. ◆

XACT*step* only

This procedure for running XACT*step* from the CD-ROM assumes that C:\ is a local drive and that D:\ is the CD-ROM drive containing the XACT*step* CD-ROM.:

1) If running Windows, exit.
2) Create a local XACT*step* directory.
   Example: C:\CDXACT
3) Make the following changes to the AUTOEXEC.BAT file:
   SET XACT=D:\XACT;
   SET PATH=D:\XACT;<other_paths>

NOTE: The only path added to the PATH environment variable is the CD-ROM executable path XACT. The local path created in the previous steps does not need to be added.

   SET XACTUSER=C:\CDXACT

*NOTE: To ensure that the XACT*step *software has a directory that can be written to, the XACTUSER environment variable should be set to a local directory.*

4) Reboot your machine or execute your AUTOEXEC.BAT file so that the new changes take effect.
5) Start Windows.

Now that the system has been properly configured to run the software from the CD-ROM, all that remains is to create a

Logic Synthesis

Continued from previous page

Synopsys, Viewlogic, Mentor Graphics, and Exemplar Logic tools.

Table 1 shows the current state of synthesis support from major EDA vendors for the Xilinx FPGA products. Support is indicated as either "gates" or "mapped," where mapped supports indicates that the synthesis compiler maps to the fundamental logic cell elements of that architecture.

Table 1 - *Xilinx FPGA Synthesis Support by Third-Party Vendors*

	XC3000	XC4000	XC5200	XC8100
Data I/O	Mapped	Mapped	Mapped	
Exemplar Logic	Gates	Mapped	Mapped	Mapped
IST	Mapped	Mapped	Mapped	
Mentor Graphics	Gates	Gates	Gates	Mapped
Synopsys	Mapped	Mapped	Mapped	Mapped
Synplicity	Mapped	Mapped	Mapped	
Viewlogic	Mapped	Mapped	Gates	Mapped

VHDL or Verilog-HDL designers now have a number of choices in FPGA synthesis, both in terms of tools and device architectures. Many synthesis vendors are supporting full ASIC design methodologies for Xilinx. With the fast, PCI-compliant XC3100A, the cost-effective XC5200, the high density XC4000 with on-chip RAM, and the highly-configurable and non-volatile XC8100 families, Xilinx offers cost-effective, high-performance FPGA solutions for HDL-based design. ◆

CD-ROM program group. To create a program icon, perform the following steps:

1) To create a new program group in the Program Manager, select the New command from the File menu. The New Program Object dialog is displayed.
2) Select the Program Group radio box and click on OK. The Program Group Properties dialog is displayed.
3) Enter the name of the new group in the Description text field and click on OK. For example, type "CD-ROM XACTstep 6.0". The new program group is created and displayed in the Program Manager.
4) To create a new Program Item in the new group, select the New command from the File menu.
5) Select the Program Item radio box and click on OK. The Program Item Properties dialog is displayed.
6) In the Description text field, type: Xilinx Design Manager
7) In the Command Line text field, type: D:\XACT\DSGNMGR.EXE
8) In the Working Directory text field, type: C:\CDXACT
9) Click on OK.
10) If your are using a network connection to mount the CD-ROM, confirm the Network Path Specified dialog. The CD-ROM XACT*step* 6.0 program group is updated to include the Xilinx Design Manager program icon. ◆

PRO Series and XACT*step*

The following procedures describe how to set up a PC to run both the Viewlogic PRO Series and the Xilinx XACT*step* tools directly from the CD-ROM. It assumes that C:\ is a local drive and that D:\ is the CD-ROM drive that contains the XACT*step* CD-ROM.

1) If running Windows, exit.
2) Create a local PRO Series directory.
   Example: C:\CDPROSER
3) Create a STANDARD sub-directory in the PRO Series directory.
   Example: C:\CDPROSER\STANDARD
4) Create a local XACT*step* directory.
   Example: C:\CDXACT
5) Create a DATA sub-directory in the XACT*step* directory.
   Example: C:\CDXACT\DATA
6) Copy the PARTLIST.XCT file from the CD-ROM XACT*step* DATA sub-directory to the XACT*step* DATA sub-directory.
   Example: copy D:\XACT\DATA\PARTLIST.XCT C:\CDXACT\DATA
7) Make the following changes to the AUTOEXEC.BAT file:

SET WDIR=C:\CDPROSER\STANDARD;D:\PROSER\STANDARD
NOTE: The first directory in the WDIR environment variable MUST be a writable directory. This is where the project information will be written. The second path included in WDIR is the CD PRO Series STANDARD directory and is used by the PRO Series software to find data files.

SET XACT=C:\CDXACT;D:\XACT;D:\PROSER
*NOTE: The first directory in the XACT environment variable MUST contain a writable version of the PARTLIST.XCT data file in its DATA sub-directory. This is used by Xilinx PROflow which will fail if the CD-ROM version which is not writable is used. The second path included in XACT is the CD XACT directory and is used by the XACT*step *software to locate data files.*

SET PATH=D:\XACT;D:\PROSER;<other_paths>
NOTE: The only paths added to the PATH environment variable are the CD-ROM executable paths XACT and PROSER. You do NOT need to add the local paths created in the previous steps.

SET XACTUSER=C:\CDXACT
*NOTE: To ensure that the XACT*step *software has a directory that can be written to, the XACTUSER environment variable should be set to a local directory. Because a local XACT*step *directory has already been created to store a local copy of the partlist it can be used as the temporary file storage area as well.*

8) Reboot your machine or execute your AUTOEXEC.BAT file so that the new changes take effect.
9) Start Windows.

Now that the system has been properly configured to run the software from the CD-ROM, all that remains is to create a CD-ROM program group. To create a program icon for Xilinx PROflow, perform the following steps:

1) To create a new program group in the Program Manager, select the New command from the File menu. The New Program Object dialog is displayed.
2) Select the Program Group radio box and click on OK. The Program Group Properties dialog is displayed.
3) Enter the name of the new group in the Description text field and click on OK. For example, type "CD-ROM XACTstep 6.0". The new program group is created and displayed in the Program Manager.
4) To create a new Program Item in the new group, select the New command from the File menu.
5) Select the Program Item radio box and click on OK. The Program Item Properties dialog is displayed.
6) In the Description text field, type: Xilinx PROflow
7) In the Command Line text field, type: D:\PROSER\PSFM.EXE
8) In the Working Directory text field, type: C:\CDPROSER
   NOTE: It is important that the Working Directory be located on the same drive as projects that will be used in Xilinx PROflow.
9) Click on OK.
10) If your are using a network connection to mount the CD-ROM, confirm the Network Path Specified dialog. The CD-ROM XACT*step* 6.0 program group is updated to include the Xilinx PROflow program icon. ◆

Synchronous RAM Improves System Speed

The XC4000 FPGA architecture allows the option of using two of the memory-look-up-table-based function generators in each logic block as small blocks of RAM or ROM memory. These distributed RAM blocks —16 or 32 addresses deep — are a popular feature of the XC4000 devices.

These RAM blocks offer sub-5 ns access times and write pulse widths; they can greatly improve system performance by avoiding inter-chip delays. On-chip, distributed memory facilitates the efficient implementation of register banks, status registers, shift registers and high-speed FIFO buffers that bridge the gap between subsystems that have different access times and data burst rates.

However, writing into these fast, asynchronous RAM blocks can pose timing challenges. While a READ operation is simple (data is available a short time after the address inputs are stable), a WRITE operation must be timed more carefully. The actual writing is controlled by a Write Enable (WE) or write strobe signal. This signal must exceed a specified minimum width, and it must not start until the address inputs at the RAM cell have been stable for a specified address set-up time. The address inputs must remain stable for the duration of the WE pulse and for the specified address hold time after WE returns to its inactive state. The data to be written must be stable a specified time before the end of WE and also a short hold time after the end of WE. Violating any of these specifications can result in wrong data being written into the selected location, or data being written into a location not selected .

Such timing requirements are common to all conventional static RAMs. A relatively easy challenge with 35-ns SRAMs, timing becomes more difficult when dealing with 4-ns RAM blocks located inside an FPGA.

In a typical synchronous system, timing requirements are easily met if a write operation can be stretched over two or more system clock periods; however, most systems require higher performance for their memory functions.

To perform a write operation in only one clock period, the circuit must be designed to:

1) generate the address and route it to the memory block,
2) generate a WE signal and route it to the RAM block so that it is arrives several nanoseconds after all address inputs are stable,
3) terminate WE and route it so that it ends at the RAM cell while the address remains stable for several more ns, and
4) generate proper data timing with respect to the trailing edge of WE.

If all of this must be achieved within one clock period — with only two identifiable clock edges — the user faces several difficult problems.

An elegant solution appears on page 8-139 of the *Data Book* which uses the low-skew global clock network as a synchronous active-High write strobe. Address and data can be generated synchronously by the falling edge of this global clock, while routing delays can be controlled to be less than the clock Low time, thus meeting the address set-up time requirement. WE timing is well controlled, and the natural delay in generating and routing the next address provides sufficient address hold time. Since the write strobe is unconditional, a write operation occurs on every clock pulse. To prevent the writing of new data, a multiplexer must connect the old data back to the data input. This method results in a robust, single-clock synchronous design. However, it sacrifices perfor-

mance — only half of one clock period is available for address routing. The data multiplexer also sacrifices density.

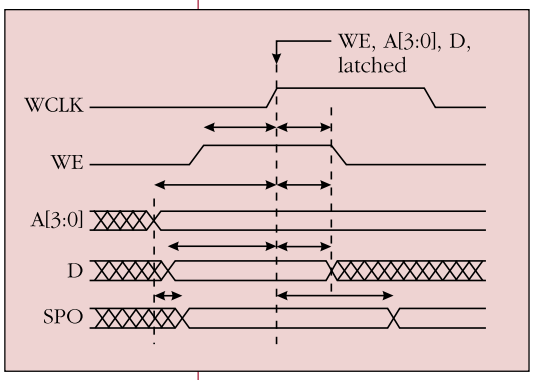
Synchronous RAM

The XC4000E family features a synchronous RAM option that provides more performance and density. When the synchronous RAM option is invoked, writing to the RAM is like writing to a flip-flop or register. The user connects a clock signal — preferably a low-skew global clock net — to the RAM block and selects one clock edge (for example, the rising edge). The write requirements are now simple: Address, Data, and the WE control signal must be available and stable at the RAM block input a short set-up time before the active clock edge *(see figure)*. There is no hold-time, and there are no other timing requirements.

Internal to the RAM block, Address, Data and WE drive latches are transparent when the clock is Low, and latched when the clock is High. When a WE signal is recognized, the rising clock edge generates a short internal write pulse that writes data into the addressed RAM location. The width of this pulse naturally adapts to the requirements of the RAM cell. A slow device at high temperature and low supply voltage generates a wider pulse than a fast device at low temperature and high supply voltage.

Using the same clock and the same clock edge to generate address, data, WE, and to clock the RAM, the system designer has a whole clock period to generate and distribute these signals. *(See related article on page 30.)* Thus, interfacing to the RAM is the same as interfacing to other registers. As a result, system speed can be almost doubled, while logic density can be increased substantially, compared with older asynchronous design methods.

Synchronous mode does not affect the read operation. The read address bypasses the address latches, and synchronous and asynchronous read operation are, therefore, identical.



Edge-Triggered RAM Write Cycle

Synchronous, Dual-Port Mode

In synchronous, dual-port mode, the F-address drives the address latches in both the F and the G RAMs; the data input is common to both RAMs . Identical data is thus written into both RAMs, but the G read address can be used to read data independently, and present it at the G' output.

This addressing mechanism is ideal for FIFOs, with the F address used for writing and the G address used for reading. The user then only has to design the control circuitry for detecting the extreme situations of full and empty.

Synchronous dual-port mode achieves the highest possible speed, and can be run with asynchronous read timing, but it sacrifices storage capacity. For large and relatively slow FIFOs, the synchronous single-port mode may be the more efficient choice.

Small, distributed RAMs offer an attractive system solution for registers, shift registers and FIFO buffers. Previous fully-asynchronous designs had demanding timing constraints that limited their speed and density. The new synchronous distributed RAM feature in the XC4000E family makes distributed RAMs as easy to use as flip-flops and registers, and allows RAM operations at 70 MHz with a 14 ns synchronous clock cycle time (-3 speed grade). The optional dual-port mode makes FIFO designs fast and simple. ◆

Synchronous RAM Timing in the

The XC4000E FPGA's synchronous memory mode simplifies the timing of the memory interface and contrbutes to increased utilization and performance (as compared to asynchronous timing schemes). With proper attention to address routing delays, synchronous RAMs constructed from the CLBs of an XC4000E FPGA can be operated at, or close to, the maximum clock frequency, as determined by the minimum write cycle time. This is 70 MHz for XC4000E-3 devices. (All calculations below are for the -3 speed grade).

Write Operations

Most applications generate the RAM address in a synchronous register or counter, clocked by the same Global Clock edge as the synchronous RAM *(Figure 1)*. The address output is guaranteed to be available T_{CKO} after the active clock edge, and this address must arrive at the CLB-RAM one T_{ASS} set-up time before the next active clock edge. At 70 MHz, this leaves 9.2 ns for routing the address to all the CLBs that make up the RAM block. With appropriate CLB placement, this should not be difficult. Of course, set up times on the write data input also must be met.

WRITE TIMING, FIGURE 1

Clock Pulse Width	T_{WPS}	7.2 ns
Write Cycle Time	T_{WCS}	14.4 ns minimum (70 MHz maximum)
Address Register clock-to-out delay	T_{CKO}	2.8 ns maximum
Address Set-up Time	T_{ASS}	2.4 ns minimum
Maximum allowed address routing delay @ 70 MHz		14.4–2.8–2.4 = 9.2 ns

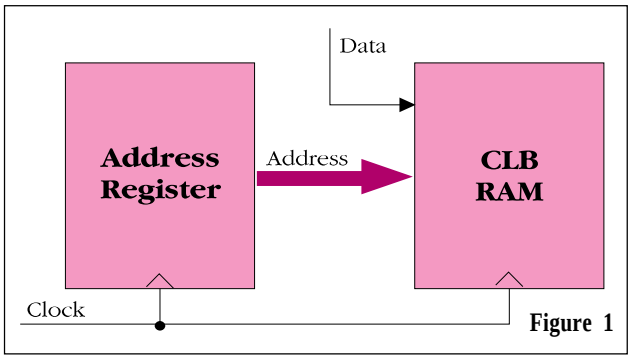


Figure 1

Read Operations

The output from a CLB function generator being used as RAM can be either combinatorial or synchronized using the CLB flip-flop. The combinatorial output from the CLB-RAM is guaranteed to be valid one T_{ILO} (for the 16x2 memory mode) or T_{IHO} (for the 32x1 memory mode) after the arrival of the address at the CLB. Again assuming that the address is held in a register, the total time from the active clock edge at that register to valid data out is

T_{CKO} + address routing delay + (T_{ILO} or T_{IHO}).

If a CLB-internal flip-flop is used to register data read from the RAM *(Figure 2)*, read timing is simple. Of the whole clock period, only T_{CKO} and T_{ICK} are consumed as logic delays; the remainder of the clock period is available for address routing.

READ TIMING, FIGURE 2

Address Register clock-to-out delay	T_{CKO}	2.8 ns maximum
CLB register set-up time (16x2)	T_{ICK}	3.0 ns
CLB register set-up time (32x1)	T_{IHCK}	4.6 ns
Maximum allowed address routing delay @ 70 MHz (16x2)		14.4–2.8–3.0 = 8.6 ns
Maximum allowed address routing delay @ 70 MHz (32x1)		14.4–2.8–4.6 = 7.0 ns

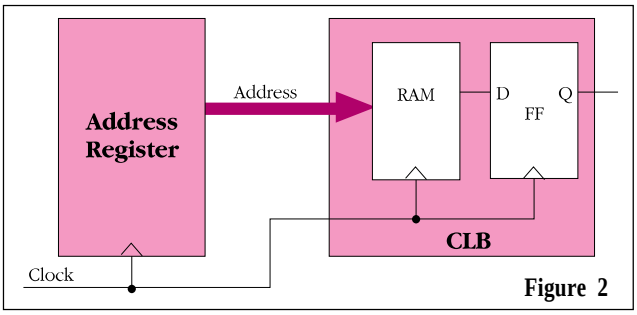


Figure 2

Read Operations *(continued)*

If the pipelined output drives the data input to another CLB-RAM *(Figure 3)*, only T_{CKO} and T_{DSS} are consumed as logic delays on the data path, the remainder of the clock period is available for data routing. The routing delay to the nearest neighbor is already included in T_{CKO}; that is, there is no additional routing delay to take into account if the RAM data is being propagated to the neighboring CLB. Otherwise, the maximum allowable delay for routing the data is calculated as follows (assuming that the second RAM's address is available T_{ASS} before the clock edge):

READ TIMING, FIGURE 3

Registered Data valid after clock	T_{CKO}	2.8 ns
Data input set-up time (16x2)	T_{DSS}	3.2 ns
Data input set-up time (32x1)	T_{DSTS}	1.9 ns
Maximum allowed registered data routing delay (16x2)		14.4–2.8–3.2 = 8.4 ns
Maximum allowed registered data routing delay (32x1)		14.4–2.8–1.9 = 9.7 ns

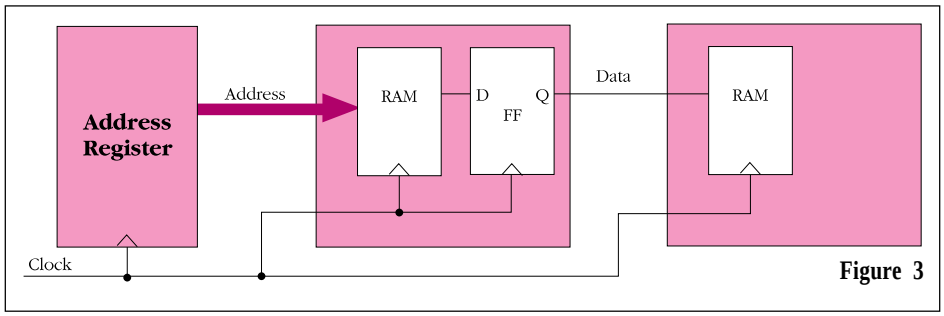


Figure 3

Suppose that the RAM data output bypasses the register in its CLB, but is an input to a function in another CLB, and the output of that function generator is registered with the same clock that is used to register the RAM address *(Figure 4)*. Valid data must be available at that register T_{ICK} before the next active clock edge. Thus, T_{CKO} + (T_{ILO} or T_{IHO}) + T_{ICK} + data routing delay is the minimum time needed to read the CLB-RAM and gets its output to the destination CLB, through its function generator and to the register.

READ TIMING, FIGURE 4

Address Register clock-to-out delay	T_{CKO}	2.8 ns maximum
Data Valid After Address (16 x 2)	T_{ILO}	2.0 ns maximum
Data Valid After Address (32 x 1)	T_{IHO}	4.3 ns maximum
Register Set-up Time	T_{ICK}	3.0 ns minimum
Maximum allowed data routing delay @ 70 MHz		14.4–2.8–2.0–3.0 = 6.6 ns

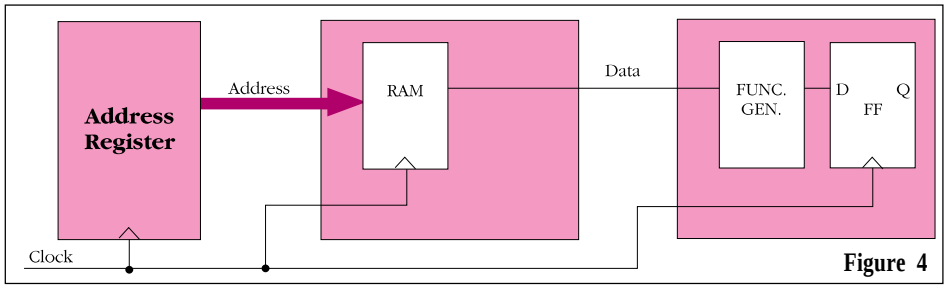


Figure 4

Conclusion

Controlling the timing of synchronous RAM operation is fairly straightforward. For most applications, synchronous RAMs constructed from the CLBs of an XC4000E FPGA can be operated at, or close to, the maximum clock frequency as determined by the minimum write cycle time. ◆

Sensitivity to Power Glitches

Any digital logic device with internal data storage in latches or flip-flops is sensitive to power glitches. This includes every microprocessor, microcontroller, and peripheral circuit. Only purely combinatorial circuits can be guaranteed to survive a severe power glitch without any problem.

Xilinx SRAM-based FPGAs store their configuration in latches that lose their data when the supply voltage drops below a critical value (substantially below 3 V for the 5 V devices). However, all configuration data is extremely robust and reliable while V_{CC} stays above 3 V.

All Xilinx configuration latches are implemented as cross-coupled, complementary inverters with active pull-down n-channel transistors and active pull-up p-channel transistors. Both High and Low logic levels have an impedance of less than 5 kΩ with respect to their supply rail. This impedance is a million times lower than the 5 Gigaohm polysilicon pull-up resistors used in typical SRAMs. Thus, the data in Xilinx latches is far more rugged and reliable than the data in popular SRAMs.

Most digital circuits rely on V_{CC} staying within specification. Xilinx FPGAs have an internal voltage monitoring circuit. Whenever the 5 V supply voltage dips below 3 V, the internal monitoring circuit causes the Xilinx FPGA to stop normal operation. All outputs go 3-state, and the device waits for the supply voltage to rise closer to 4 V, when it either demands (slave or peripheral mode) or initiates (master mode) a reconfiguration. (In the range from 5 V down to 3 V, all CMOS devices maintain their functionality and their data storage, they just get slower as the voltage goes down.)

Xilinx has made sure that the FPGA cannot be corrupted by a power glitch. The most sensitive circuit is the low-voltage detector. It kicks in while all other configuration storage and user logic is still guaranteed to be functional. The voltage monitoring feature in the Xilinx device can even be used to protect other circuitry, or it can be coordinated with external monitoring circuits.

As a result of these careful precautions, we contend that Xilinx FPGAs are safer than all other types of circuitry (except purely combinatorial circuits). A microprocessor can lose the content of its address register, its accumulator or other control registers due to an undetected power glitch, with disastrous consequences to the subsequent operation. A Xilinx FPGA detects the power glitch and always plays it safe by flagging the problem.

No complex system of any kind can function reliably when V_{CC} is unreliable. Xilinx FPGAs do the safest thing possible, whenever such problems occur. ◆

Readback in FPGAs

All Xilinx SRAM-based FPGAs allow an unlimited number of **readback** cycles; that is, the user can read the contents of both the configuration memory and the registers within logic blocks. All the XC2000, XC3000, XC4000, and XC5200 family devices have similar readback mechanisms. (The XC6200 devices have a different readback mechanism).

The readback mechanism originally was intended for internal test purposes, not as a user-accessible function. However, there are two reasons why a user may want to initiate a readback operation:

- **To read the status of internal data storage elements**, as "a poor man's In-Circuit-Emulator." New software in XACT*step*™ version 6, the Hardware Debugger, makes this process much easier and more versatile.
- **To verify that the configuration data is unchanged**. This is explicitly required by certain military applications, and it might also be meaningful

XC4000 Drives 3.3 V Devices Safely

LOW POWER

Although a variety of 3.3 V components are becoming available, some systems require a mix of 3.3 V and 5 V devices. Xilinx offers several solutions for such mixed-voltage systems. Among these are the 5 V XC4000 and XC4000E FPGA families; their output buffers can safely drive either 5 V or 3.3 V devices.

The XC2000 and XC3000/XC3100 family devices have complementary outputs that require some current-limiting resistor when driving 3.3 V devices in order to protect the inputs and ESD protection circuitry of the 3.3 V device. In contrast, the XC4000 FPGAs have n-channel-only, totem-pole-like outputs that are more gentle driving V_{OH}. The XC4000H and XC4000E devices offer both types of outputs; the totem-pole-like outputs are available in the TTL output mode.

The table lists the worst-case output current for three FPGA families, assuming a 5.0 V supply for the FPGA. (The numbers on page 9-23 of the *Data Book* are typical, not worst-case). For higher or lower supply voltages, adjust the output voltage accordingly, one-to-one; that is, apply the V_{CC} error directly to the output voltage, mV for mV.

The input of a 3.3 V device will have negligible input current until the input voltage is 0.6 V or more above the nominally 3.3 V supply. Even if an XC4000 output is driving a 3.3 V device with a worst-case supply voltage of 3.0 V, the XC4000 output will forward-bias the input protection diode with less than 1 mA, which is not sufficient to cause harm or latch-up on any reasonably designed CMOS input. Thus, all XC4000 outputs (as well as XC4000E and XC4000H outputs in TTL mode) can directly drive the inputs of 3.3 V logic devices safely without requiring current-limiting resistors. ◆

Output Voltage V_{OH}	Maximum Output Current		
	XC4000	XC3000A	XC3100A
5.00	65 nA	55 nA	2 µA
4.50	45 nA	-20mA	-18 mA
4.00	22 nA	-39mA	-34 mA
3.90	zero	-43mA	-37 mA
3.70	-20µA	-49 mA	-43 mA
3.50	-1.0 mA	-56 mA	-48 mA
3.30	-3.5 mA	-62 mA	-54 mA
3.00	-9 mA	-71mA	-62 mA
2.50	-24mA	-84 mA	-73 mA
2.00	-46mA	-95 mA	-82 mA
1.50	-72mA	-104 mA	-90 mA
1.00	-100 mA	-110 mA	-95 mA
0.50	-130 mA	-113 mA	-98 mA
0.00	-160 mA	-114 mA	-99 mA

for some telecommunications or industrial applications, where, once configured, the device configuration is maintained for weeks, months or even years.

Xilinx FPGA configuration data is extremely robust and reliable while V_{CC} stays within specification. *(See related article on page 32.)* As a result, there is no reason to worry about the reliability of Xilinx configuration bits. When required by the system specification to read back the configuration data and compare it against the content of the original configuration bitstream, the user will have this confidence confirmed. **This readback operation does not interfere with the normal operation of the device**. In fact, it is possible to use logic implemented in an FPGA to process the data obtained during a readback of its own configuration memory. ◆

LOW POWER

Minimizing Power Consumption in FPGA Designs

In general, the CMOS technology used to produce FPGAs is a low-power technology. Virtually all power consumption results from the dynamic charging and discharging of internal capacitive nodes and capacitive loads on the device outputs.

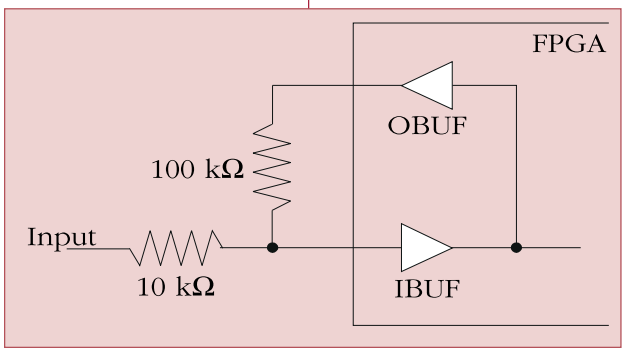
Here are some techniques that can be used to minimize power consumption in an FPGA design:

- *Chip outputs dissipate a lot of power.* Use as few as possible, and have them switch as infrequently as possible. Although there is no need to three-state outputs unnecessarily, don't allow an output to change continuously if the external circuitry is ignoring the data.
- Similarly, *don't allow internal FPGA nodes to toggle unnecessarily.* Clock enable functions on flip-flops often can be used to "turn off" inactive portions of a synchronous circuit.
- *Use APR or PPR (or even XDE) to maximize the performance of the design,* even if the resulting performance is far in excess of requirements. Power dissipation is proportional to capacitance, and routing capacitance is the main cause of low performance. Circuits that are able to run faster can do so because of lower routing capacitance. Consequently, they dissipate less power at any given clock frequency.
- *For XC3000A/XC3100A designs, use ACLK for global clocking,* and floorplan to minimize the number of vertical clock segments used. This minimizes the power associated with clock distribution.

For very power-sensitive applications, power consumption can be dramatically reduced by using the 3.3 V Zero+ XC2000L and XC3000L FPGA families. These devices were designed to provide very low quiescent current consumption, and consume less than half the dynamic power of their 5 V counterparts. Also, remember that the XC2000 and XC3000 FPGAs feature a power-down mode, wherein the FPGA's configuration is preserved, but all other circuitry is powered down. ◆

User-Defined Schmitt Triggers

All inputs to Xilinx FPGAs have a hysteresis of 100 to 200 mV. It helps avoid noise propagation from slowly rising or falling input signals. Users requiring more hysteresis can design their own **Schmitt trigger** circuits easily with only two resistors. However, it uses one additional output pin, driven (non-inverted) from the input pin, as in the diagram.



A 10 kΩ serial input resistor combined with a 100 kΩ feedback resistor gives 500 mV of hysteresis. (Hysteresis is the difference between the effective input threshold voltages on the Low-to-High transition and the High-to-Low transition. That difference is equal to V_{CC} times the resistor ratio.)

A 1 kΩ/10 kΩ combination gives the same hysteresis, but reduces the delay caused by the pin-to-ground capacitance from 100 ns to 10 ns. On the other hand, it requires more input current.

For TTL-threshold inputs, the hysteresis should be kept below 1 V; for CMOS inputs, it can be up to 2 V. ◆

Reconfigurable Computing Developer's Program

The new Reconfigurable Computing Developer's Program is designed to proactively spur commercial development of reconfigurable computing applications and products.

The program is an easy way for small companies or projects to become directly tied to our reconfigurable computing thrust. It supplies commercial companies with:

a) substantial discounts when purchasing Xilinx components and software,
b) potential product promotions via our sales literature, web site, and mailing lists, and
c) potential eligibility for financial grants to fund development projects involving reconfigurable computing and based on Xilinx devices.

Current program members are involved with a wide range of applications and products, including test vector analysis, floating point mathematics, real-time audio processing, wireless communications, distributed network computing, engineering development tools, real-time imaging processing and video processing.

We believe that these applications are just the tip of the iceberg. We are discovering that the market for reconfigurable computing includes many of the applications currently solved with embedded microprocessors, DSPs and ASICs. Reconfigurable computing based on FPGAs combines the performance of a dedicated circuit with the flexibility and convenience of a programamble solution. (After reviewing a competing product that uses Xilinx FPGAs, one engineer returned to his DSP-centric company stating, "I have seen the future and we're not in it." This engineer was then instrumental in getting his company to apply for the Developer's Program.)

The large number of interesting reconfigurable computing project proposals has prompted us to create the Application of the Quarter award. The first winner will be selected in the first quarter of 1996. ◆

Further information on the Reconfigurable Computing Developers Program is available on WebLINX, the Xilinx World Wide Web site. To apply for admission in the Program, please contact John Watson at Xilinx, San Jose (Tel: 408-879-6584 E-mail: john.watson@xilinx.com).

OVERVIEW OF TECHNICAL SUPPORT FACILITIES

Automated Support Systems

Xilinx Web site - available at http://www.xilinx.com.
XDOCS E-mail document server - send an E-mail to xdocs@xilinx.com with 'help' as the only item in the subject header. You will automatically receive full instructions via E-mail.
XFACTS fax document server - available by calling 1-408-879-4400.

In order to provide timely support for new, high-growth markets, Xilinx Applications has established a series of E-mail addresses to direct technical inquiries. These addresses may be used to request information packets or to ask in-depth technical questions:

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PCMCIA card applications ..... pcmcia@xilinx.com
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fax: (49) 89 904 4748
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Applications Update:

PCI, ATM, DSP, Plug & Play, RC

PCI *(Peripheral Component Interconnect Bus)*

MEMBER
PCI LOCAL BUS
SPECIAL INTEREST GROUP

Product News — Xilinx is now shipping three 100-percent PCI-compliant product families:

- **XC4000E-3** and faster speed grades in plastic quad-flat packages. Gate densities ranging from 5,000 to 13,000 gates. On-chip RAM provides burst FIFOs for the industry's fastest PCI data transfer rate in a programmable device.
- **XC3100A-2** and faster speed grades in plastic quad-flat packages.
- **XC7300-10** and faster speed grades in plastic quad-flat packages.

Application Notes —

- **Xilinx XC4000E PCI System Module Design Guide** describes a fully-verified PCI Target and Initiator macro for the XC4000E family.
- **Fully Compliant PCI Interface in an XC3164A-2 FPGA**.
- **Designing Flexible PCI Interfaces With Xilinx EPLDs**.

Other Projects — Xilinx Applications has developed a **PCI Target and Initiator** macro for use with the XC4000E. This macro provides a single-chip, fully-verified, 100-percent PCI-compliant, 33 MHz solution. Integrated burst FIFOs provide the highest data transfer rate of any programmable logic-based solution.

The fully-verified 100% PCI-compliant Target macro was released to beta-site customers in mid-October. Fully-verified PCI Target and Initiator designs will be released to the general design community by February, with limited release to select customers by the end of 1995.

E-mail Contact — pci@xilinx.com ◆

Telecommunications

Product News —

- **XC5200** FPGA family provides an excellent solution for most telecommunications design. It combines good performance with low cost in a flip-flop intensive architecture.
- **XC4000E, XC3100A**, and **XC7300** are ideal for higher-performance telecommunications applications such as ATM, SONET, etc.

E-mail Contact — atm@xilinx.com ◆

Digital Signal Processing

Product News—

- **XC4000E** FPGA family in production. The on-chip RAM increases the effective density of many DSP designs. The added performance of XC4000E carry chains boost overall performance.
- **XC6200** FPGA provides an ideal solution for imbedded co-processing designs. The XC6200's fine-grain, regular architecture is useful in systolic array, image processing and computationally-intensive applications. The integrated processor bus interface provides a high-bandwidth connection to standard microprocessors or DSP processors.

Application Notes — **16-Tap, 8-Bit FIR Filter Applications Guide** describes how to build a filter using Sequential Distributed Arithmetic (SDA).

Other Projects — Implemented a fully-parallel version of the 16-tap, 8-bit FIR filter, providing users with a higher-performance solution *(see Table 1)*. An application note will be available next quarter.

DSP (con't)

Table 1 — *Performance of a 16-Tap, 8-Bit FIR Filter Design.*

"PROCESSOR"	SAMPLE RATE	CLBS
XC4003E-3 using Sequential Distributed Arithmetic (SDA)	8.1 Mhz	68
XC4010E-3 using Parallel Distributed Arithmetic (PDA)	48 Mhz	390
XC4013E-3 using Parallel Distributed Arithmetic (PDA)	55 Mhz	432
50 MHz Fixed-Point DSP Processor	3.125 Mhz	N/A

Conference Papers and Articles —

"A distributed arithmetic approach to designing scaleable DSP chips," Bernie New, *EDN*, August 17, 1995, pages 107-112.

"Using Programmable Logic to Accelerate DSP Functions," Steve Knapp, Designing with Programmable Logic Devices Seminar, October 17–24, 1995, *Asian Electronics Engineer*.

"Using Xilinx FPGAs to Design Custom Digital Signal Processing Devices," Greg Goslin, *Proceedings of DSP Deutschland 95*, September 25,26, 1995, pages284-294.

"Using FPGAs in Digital Signal Processing Applications," Greg Goslin, ICSPAT'95/DSP World Expo, October 24–26, 1995.

"Using Xilinx FPGAs for Application-Specific DSP Algorithms," Greg Goslin, ICSPAT'95/DSP World Expo, October 24–26, 1995.

"The FPGA as FFT Processor," Les Mintzer, ICSPAT'95/DSP World Expo, October 24–26, 1995.

E-mail Contact — dsp@xilinx.com ◆

Plug and Play - ISA Bus

Product News —

- **Windows 95** released. Plug and Play is a major feature.
- **XC5200** in production. Though the application note is written for XC4003, the design also fits into the lower-cost XC5204.

Application Note — **Plug and Play ISA Using Xilinx FPGAs** describes how to build a Plug and Play interface in an XC4003 FPGA. The same design also fits into the lower-cost XC5204

E-mail Contact — PnP@xilinx.com ◆

Reconfigurable Computing

Product News —

- **XC6200** FPGA provides an ideal solution for reconfigurable co-processing. The XC6200's integrated processor bus interface provides a high-bandwidth connection to standard microprocessors or DSP processors. This interface offers fast configuration (< 1 ms) and fast partial reconfiguration.
- Newer FPGA families include faster configuration methods. The **XC5200** family offers Express Mode which provide eight times faster configuration.

Application Notes — Configuring FPGAs Over a Processor Bus. Useful to any designer that wants to program an SRAM-based FPGA from the processor bus.

Other Projects — Reconfigurable Computing Developers Program *(see page 35)*

E-mail Contact —
reconfig@xilinx.com ◆

EPLD

My design requires a 3.3 V output on the I/O pins of an XC7300 device. If I tie V_{CCIO} to a 3.3 V supply, can I still drive inputs on the I/O pins at 5 V?

Yes, when the V_{CCIO} pin is supplied by 3.3 V, only the logic output is affected. The thresholds on all input buffers are compatible with both 5 V and 3.3 V inputs, and the ESD protection diodes are connected to 5 V. There is no need for external resistors.

I am using an ABEL source file for a design on the XC7372. I have explicitly assigned the critical signals to the fast inputs on the device. The timing report however shows that they are treating them as standard I/O. How do I enable the fast inputs?

The default configuration for ABEL is to route the input pins through the UIM as a normal input. In order to utilize the fast inputs, you must explicitly declare them using the property statement in ABEL. For example, if signals A, B, and C need to be fast inputs, use the following statement in your ABEL file:

```
PLUSASM PROPERTY 'INPUTPIN (FI)
  A B C';
```

I am using an XC7300 in a design with a large number of input and output signals switching. I am concerned that I may have problems with ground bounce. What can I do to minimize this possibility?

There are several options to minimize potential ground bounce. If the system is designed for TTL levels, you may be able to connect V_{ccio} to a 3.3 V supply voltage. This will reduce the amount of current needed to swing outputs. Also, you can slow the output slew rate from the default 1.5 V/ns to 1.0 V/ns by using the PLUSASM command,

```
FAST OFF <signal names>
```

or in ABEL,

```
PLUSASM PROPERTY 'FAST OFF
  <signal names>'
```

ABEL

Looking at several ABEL files, I've noticed that in some cases, the OR operator appears as the # symbol and at other times as the + symbol. Is there a difference between the two?

ABEL supports two operator sets. Using the command

```
@alternate
```

invokes the alternative operator set. The following table lists both sets.

ABEL Operator	Alternative	Description
!	/	NOT
&	*	AND
#	+	OR
$	:+:	XOR
!$	:*:	XNOR

Note that while using the alternative operators, the mathematical operators for addition, multiplication, and division are not available. The standard ABEL operators, however, are still in effect while using the alternative set. If you wish to mix the two, you can turn the alternative operators off by using the command

```
@standard
```

What happens if I make multiple assignments to the same identifier in ABEL?

When ABEL finds multiple assignments to a single identifier, they are logically ORed together. If a complement operator is found on the left side of an equation, then the complement is performed after the expressions have been ORed. For example,

```
A = B;
A = !C;
!A = D;
!A = E;
```

is equivalent to

```
A = B # !C # !(D # E);
```

Synopsys

How do I take a Synopsys design into a Viewlogic schematic?

If you want to move a Synopsys design into a Viewlogic schematic, then the Synopsys design must be converted into a .xnf file for a Viewlogic schematic symbol. The procedure to follow is:

1) Compile the design in Synopsys and write out a .sxnf or .sedif file.
2) run syn2xnf -s on the .sxnf/.sedif file. For example, let's say you've created a design called *count8*. To bring *count8* into a Viewlogic schematic, type:

```
syn2xnf -s count8
```

This will produce an .xnf file that can be used in a Viewlogic schematic.

How do I read an .xnf file into Synopsys?

1) Compile the design to an .lca file.
2) Run lca2xnf on the .lca file.
3) Run xnf2vss (xnf2vss is only in XSI 3.2 and greater) on the .xnf file from step (2). This will produce a file with the extension .vxnf
4) Rename the .vxnf file to a .xnf file.
5) Read this renamed .xnf file into Synopsys.

For example, if you have a .lca file called count.lca, lca2xnf would produce a file called count8.xnf. Next, xnf2vss would be run on count8.xnf. A file called count8.vxnf would be produced. Finally, after renaming count8.vxnf to count8.xnf, now you will have a .xnf file that can be read into Synopsys.

Why does xnf2vss create a .vxnf file and a .nrf file when it is run?

The .vxnf file is for reading a .xnf file into Synopsys *(see previous question).* The .nrf file shows how the .xnf names are changed for the Synopsys VSS simulation flow. Synopsys and XACT using different naming conventions. So, when the .xnf is brought into VSS, sometimes the symbol names and netnames in the .xnf file are modified. The .nrf file will show you the modifications.

OrCAD

Can OrCAD Capture for Windows be used to enter designs in XACT*step*?

The OrCAD interface in XACT*step* is designed for use with SDT 386+. However, a methodology has been developed for using Capture with XACTstep. The appropriate FPGA libraries must be translated into OrCAD Capture and selected during schematic entry. When adding properties or attributes to a component, they must be named using the default names from OrCAD SDT. The schematic must be saved as an .SDF file. A document detailing this methodology can be obtained using the XDOCS E-mail document retrieval system; please request document number 26121.

We currently recommend completing existing designs in SDT 386+ before migrating to OrCAD Capture. The translation process can lose attributes that are not specified as PART FIELD properties.

Mentor Graphics

How can I obtain the latest copy of the Xilinx Autologic libraries?

You can obtain the latest version of the libraries (v1.2 as of October 1995) from Mentor's FTP site at supportnet.mentorg.com (137.202.128.4).

These libraries are located in:

```
/pub/mentortech/tdd/libraries/
  fpga/xc2k_1.2.tar.Z
/pub/mentortech/tdd/libraries/
  fpga/xc3k_1.2.tar.Z
/pub/mentortech/tdd/libraries/
  fpga/xc4k_1.2.tar.Z
/pub/mentortech/tdd/libraries/
  fpga/xc7k_1.2.tar.Z
```

These libraries are compatible with both Autologic I and Autologic II.

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