XCELL

Issue 27
First Quarter 1998

THE QUARTERLY JOURNAL FOR XILINX PROGRAMMABLE LOGIC USERS

XILINX®
The Programmable Logic Company℠

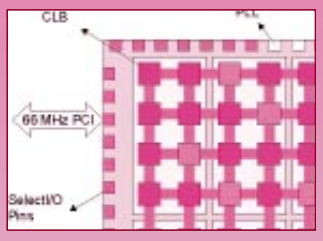
Inside This Issue:

PRODUCT INFORMATION

FOUR New FPGA Families!

Xilinx has recently announced four new FPGA families, with record-breaking technology innovations:

Virtex



The industry's highest-density, highest performance technology, using our new 0.25 micron process and an advanced architecture.

See pages 4-5

Spartan

The industry's lowest-cost FPGAs, for high volume applications, with devices under $2.00 by the year 2000.

See page 6

XH3

The industry's first FPGA-specific ASIC called "FpgASIC", making ASIC conversions easier than ever before.

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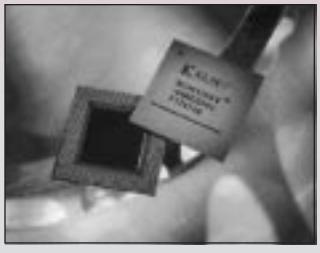
XC4000XV



The industry's first 500K gate FPGA family with devices containing over 25 million transistors, the industry's largest FPGA.

See pages 8-9

Xilinx Record-Breaking Technology – Today

by CARLIS COLLINS ◆ Editor

We are aggressively expanding the limits of both device and software technology, as you will see from the articles in this issue of *XCell*. We are the number one supplier of FPGAs worldwide because we spend a large portion of our revenues on research and development. As a result, we have created the industry's most advanced, highest-performance, 0.25-micron technology, and the broadest line of powerful and efficient device architectures that are creating new design opportunities never before possible. Our new device families include:

> *"We have created the industry's most advanced, highest-performance, 0.25 micron technology, and the broadest line of powerful and efficient device architectures that are creating new design opportunities never before possible."*

- Our XC4000XV family of high-performance FPGAs (up to 500,000 system gates at over 100 MHz).
- Our Virtex™ family of high-performance, very dense, system-level FPGAs (up to 1,000,000 system gates at over 100 MHz).
- Our Spartan™ family of low-cost devices (up to 40,000 system gates at over 80 MHz).
- Our XH3 family of HardWire™ ASIC devices that provide unprecedented ease-of-use, quick turnaround, and guaranteed performance for high-volume applications.

Powerful Software

We have also been working diligently to create the most powerful and efficient development tools in the industry. With our Alliance Series and Foundation Series software, you can quickly develop and debug FPGA and CPLD designs for all of our devices, using any combination of design methods, including VHDL and schematics. These development tools give you the most comprehensive and powerful solutions available anywhere, and we are constantly refining and updating our tools with the latest software advances, both from our in-house development team and from our Alliance partners.

Along with our advanced development tools, we offer an expanding library of intellectual property cores that will become increasingly important as you begin to create designs for our high-density devices. With the use of intellectual property, your next generation designs will be faster and easier to produce. In addition, we continue to develop new tools that will automatically create complex, customized functions for you. For example, using our core generator tools, you will soon be able to automatically create massively parallel DSP functions that are much faster than any commercially available DSP device.

We are doing our best to anticipate your needs and provide you with the most advanced technology, services, and technical support. In this magazine, and on our WebLINX Web site (www.xilinx.com), we intend to provide you with interesting and informative articles and timely reference information that make your job easier and more productive.

We welcome and respond to your requests and your suggestions for improvement in all areas. Please let us know how we're doing by writing to editor@xilinx.com. ◆

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The Xilinx Customer Education Group has developed two new courses: a one-day Foundation Series schematic entry course and a one-day synthesis course based on Synopsys. The Foundation Series schematic-entry course offers a combination of lecture and labs to enhance the learning experience. The course syllabus includes the Schematic Editor, HDL Editor, State Machine Bubble Diagrammer, Simulator, and Project Manager. To reinforce the lecture materials, the course includes four lab exercises, plus an optional lab presenting the advanced features of the simulator.

The one-day Synopsys-based synthesis course focuses on the implementation of an FPGA from a synthesized design. The course is designed for experienced Xilinx and Synopsys users familiar with the Alliance Series software and the FPGA Compiler. Topics included in this course include: Setting up for Synthesis, Generation of Efficient HDL code, and the Xilinx and Synopsys methodologies. Three labs are included to further enhance the synthesis learning experience.

We offer these new courses at the Xilinx headquarters office in San Jose, Calif., and our distributors worldwide will also be offering these same courses. You can find the exact dates for the scheduled distributor courses in your area by checking with your distributor or by browsing the educational information on WebLINX (www.xilinx.com). ◆

1998 Xilinx Data Book Now Available

The new *1998 Xilinx Data Book* is now available in paper, CD, and Web versions. All data sheets have been updated since the previous printing, and several new product introductions are included, such as:

- Spartan and Spartan-XL FPGA Families
- XC4000XV 2.5V FPGA Series
- XC4000XLT FPGA Series
- XC1701/L Serial PROMs

The book also includes these updated data sheets:

- XC9500 CPLDs
- XC4000E/EX/XL Series FPGAs
- XC5200 Series FPGAs
- XC3000 Series FPGAs
- XC1700D Serial PROMs

Product overviews are provided for several new products, with additional detail on WebLINX:

- HardWire FpgASIC™ Products
- High-Reliability XC4000E/X Series
- Alliance and Foundation Development System Products
- CORE Solutions

Included in the 700+ pages of the data book are several application notes providing additional technical product information, including a new Technical Overview for the first-time user. Complete packaging, programming, and quality information is also included, and everything is easy to find with 15 tabbed sections and a complete index.

Electronic Versions

All of the information in the data book is available on WebLINX (www.xilinx.com), the Xilinx Web site. The latest files can also be found on Rev. 5 of the AppLINX CD-ROM, which provides quick hyperlinks from the table of contents, index, or bookmarks to any topic in the book.

WebLINX and AppLINX include the complete collection of Xilinx application notes, as well as information on products that were not included in the general data book (such as the XC6200 series of reconfigurable processing units). Both WebLINX and AppLINX allow easy searching of the data book and application notes.

To order your copy of the *1998 Data Book* or the latest AppLINX CD-ROM, contact your local Xilinx salesperson, or send e-mail to literature@xilinx.com. ◆

Virtex *Our New Million-Gate 100-MHz FPGA Technology*

Leading process technology, architectural innovation, intellectual property cores, and ASIC design methodology are combined in the new Xilinx Virtex series.

Virtex is the next generation of Xilinx FPGA technology; a new series of high-performance, high-density, system-level devices with a revolutionary new architecture, built with leading 0.25 micron process technology. These FPGAs meet the rapidly growing demand for high-speed system-level functions, helping you create smaller, lower power, more reliable products with more features.

"You can begin Virtex designs today, because Xilinx has been working closely with its EDA partners to provide immediate delivery of the Xilinx Alliance Series software libraries."

You can begin Virtex designs today, because Xilinx has been working closely with its EDA partners to provide immediate delivery of the Xilinx Alliance Series software libraries. This development software solution for ASIC designers provides higher performance, faster compile times, and unique innovations that make it much easier to develop very high-density, very high-performance FPGA designs.

The Virtex series, combined with the Xilinx software, represents a new way to approach system-level design.

SelectI/O

The Virtex SelectI/O interface allows a single device to interface with multiple standards simultaneously, eliminating the challenges of multiple signal standards in system design. The Virtex architecture, with its 2.5-volt supply voltage, offers the industry's first devices capable of directly interfacing beyond CMOS and TTL logic. The Virtex series also supports important low-voltage standards such as LVTTL, LVCMOS, GTL+, and SSTL3.

SelectRAM+

The Virtex SelectRAM+ feature allows distributed RAM, block RAM, and high-speed access to external RAM. A common example of system-level designs requiring fast access to varied RAM configurations is a video processing application; where video frame data is stored in megabytes, line data is stored in kilobytes, and pixel and coefficient data is stored in bytes.

For megabytes of storage, the Virtex SelectI/O feature provides 133 MHz external synchronous DRAM access compatible with the SSTL3 I/O standard. Kilobytes of data can be stored in block SelectRAM memory; the Virtex series offers up to 32 blocks of 133-MHz dual-port synchronous SRAM, yielding an internal memory bandwidth of up to 17 gigabytes/second. For bytes of data, Virtex offers distributed SelectRAM memory. Pioneered in the Xilinx XC4000 family, the distributed SelectRAM allows you to create fast and flexible dual-port synchronous SRAMs.

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New CLB Architecture

The Virtex architecture is based on logic cells, which are 4-input look-up tables with a register. Each CLB contains four of these logic cells. Each CLB also contains special circuitry for propagating the carry, in addition to special circuitry for implementing efficient multipliers. Combining these features with an abundance of registers makes it very easy to create very high speed, pipelined multipliers for use in DSP and other applications.

Vector-Based Interconnect

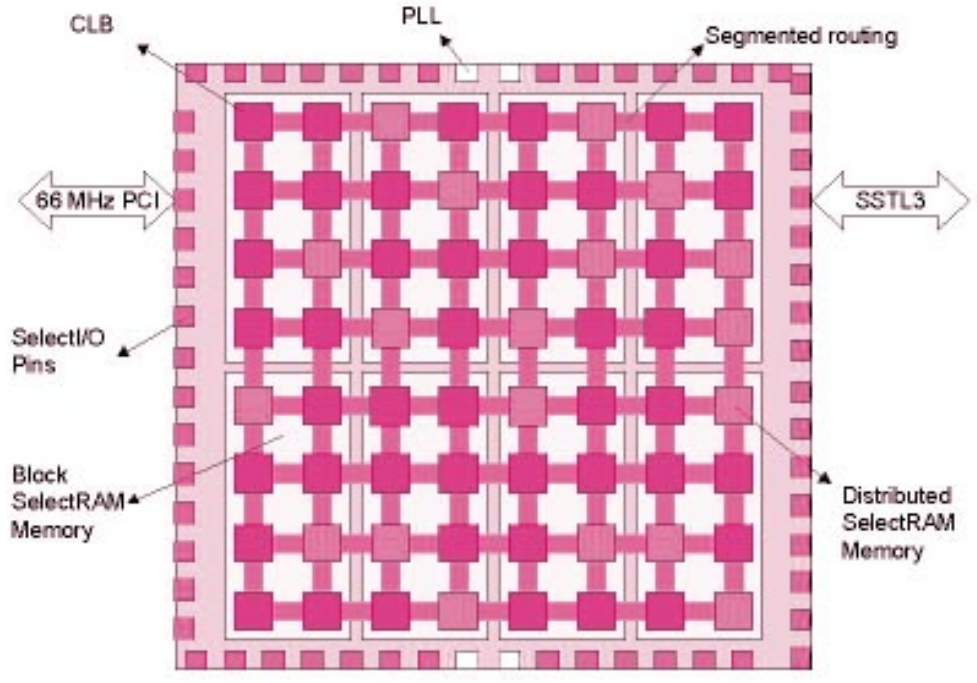
The Virtex series uses a vector-based, variable-length, segmented routing architecture, optimized to allow minimal interconnect delays; this routing is faster and more predictable than that of non-segmented architectures. Vector-based routing results in short, predictable delays that are not sensitive to minor changes in placement. This allows synthesis tools to accurately model interconnect delays in the Virtex Series, without placement information.

Cores

Because it would take many designer-years to create a million-gate system from scratch, Xilinx made the Virtex architecture very adaptable to cores. By optimizing its segmented interconnect capability to create a fundamentally faster architecture, Xilinx reduced the need for architecture-specific cores. Therefore, you can easily implement cores with highly predictable performance using high-level languages.

Availability

The first Virtex device contains 250,000 system gates and 316 user I/O pins. It is expected to be sampling in the second quarter of 1998. Virtex devices that offer up to one million system gates are expected in the second half of 1998. ◆



The new Xilinx Virtex architecture features Xilinx SelectRAM+ memory with distributed and block RAM, plus high-speed access to external RAM via the SSTL3 standard, phase locked loops (PLL), Xilinx SelectI/O pins, Xilinx segmented-routing, and vector-based interconnect.

Figure 1 – *Virtex Functional Block Diagram*

Introducing the New Spartan™
FPGA Family for Low Cost Applications

Under $2 by the Year 2000

In early January, Xilinx announced the new Spartan series of FPGAs, designed to address high-volume FPGA applications. This series incorporates a new technology with on-chip RAM, easy core implementation, high performance, and low cost. Initial devices are available in 5-volt versions, based on our 0.5-micron technology *(see Table 1)*; 3.3-volt versions based on our 0.35-micron technology are scheduled for 3Q98.

"It's not enough to simply offer low-cost replacements for traditional ASIC designs. Designers want the benefits of performance, RAM, intellectual property, and lower costs to add in-system programmability and time-to-market advantages, especially in the fast-paced consumer markets," said Wim Roelandts, Xilinx president and chief executive officer.

New Process Technology Generates New Feature Set

"In our aggressive process migration, we've realized new layout and circuit-design techniques through finer geometries and new technologies that translate directly to cost savings for our customer," continued Roelandts.

These leading-edge process technology advances offer the smallest possible die sizes. Further, for the first time in the PLD industry, low-cost ASIC replacement solutions incorporate on-chip RAM using the Xilinx SelectRAM™ feature pioneered in the XC4000 series. Together, the robust Spartan series offers a total cost management solution while delivering all the key ASIC requirements of performance, on-chip SelectRAM, cores, and low price, with all the time-to-market advantages of FPGAs.

Table 1

Device	Logic cells	System gates	Max. I/Os	Max RAM bits	High Volume Price*
XCS05	238	2,000 - 5,000	80	3,200	$3.95
XCS10	466	3,000 - 10,000	112	6,272	$5.50
XCS20	950	7,000 - 20,000	160	12,800	$6.50
XCS30	1368	10,000 - 30,000	192	18,432	$7.95
XCS40	1862	13,000 - 40,000	224	25,088	$19.95

**100,000 unit pricing for end-98*

To address total cost management, Xilinx reduced the cost of Spartan devices by not only reducing the die size but by also re-assessing all stages of the manufacturing cycle, including packaging, test, and manufacturing overhead costs.

In the third quarter of 1998, Xilinx will introduce the 3.3-volt version of this series. You can design now using our 5-volt technology with confidence that the new 3.3-volt devices will be completely footprint compatible. Additionally, the 3.3-volt devices will be offered at even lower price points than their 5-volt predecessors, taking advantage of the process migration step to 0.35 micron.

Software Support

The majority of Xilinx high-volume customers are sensitive to time-to-market pressures, preferring a complete front-to-back development environment, with minimal learning curves and high-quality results. The Xilinx Foundation Series software is the ready-to-use solution that meets this need. The Foundation and Alliance Series software are available for all Spartan devices, with software pricing starting at $495.

In addition to design tools, intellectual property cores will be offered, specifically targeting the Spartan Series, including a new PCI interface. Cores are available today from several of the Xilinx AllianceCORE partners, including T7L, Integrated Silicon Systems, Virtual IP Group (formerly ARM Semiconductor), and Memec Design Services (offering RISC processors, microprocessor peripherals, and DSP cores). All DSP cores in the Xilinx LogiCORE product series, and AllianceCORE products from third-party providers are also available.

Available From Distributors Now

The first three members of the Spartan family, the XCS20, XCS30, and the XCS40, are available today in high-volume quantities. Package offerings will include plastic quad (PQ), thin quad (TQ), and very thin quad (VQ) flat packs; plastic leaded chip carrier (PLCC); and ball grid array (BGA) options. ◆

The New XH3 Architecture Combines FPGA and ASIC Technologies

With the new XH3 architecture, Xilinx has combined its FPGA advantages with eight years of HardWire ASIC experience to create the first FPGA-specific ASIC or "FpgASIC."

FpgASICs are true ASIC devices that are designed to meet the performance and feature requirements of Xilinx FPGAs. Both the conversion method, called DesignLock,™ and the device silicon are customized to make the transition from FPGA to ASIC as easy as possible.

The XH3 family has Xilinx-specific FPGA I/Os, JTAG, and control logic built into the base layers of the device. They are exact, pre-verified, ASIC versions of the FPGA features, which are often the most difficult to convert from an FPGA to an ASIC.

For example, the devices have the exact Xilinx FPGA I/O built into the silicon. More than 220 different I/O models have been verified, allowing perfect timing matches for XC4000, XC4000E, XC4000EX, and XC5200 device family conversions.

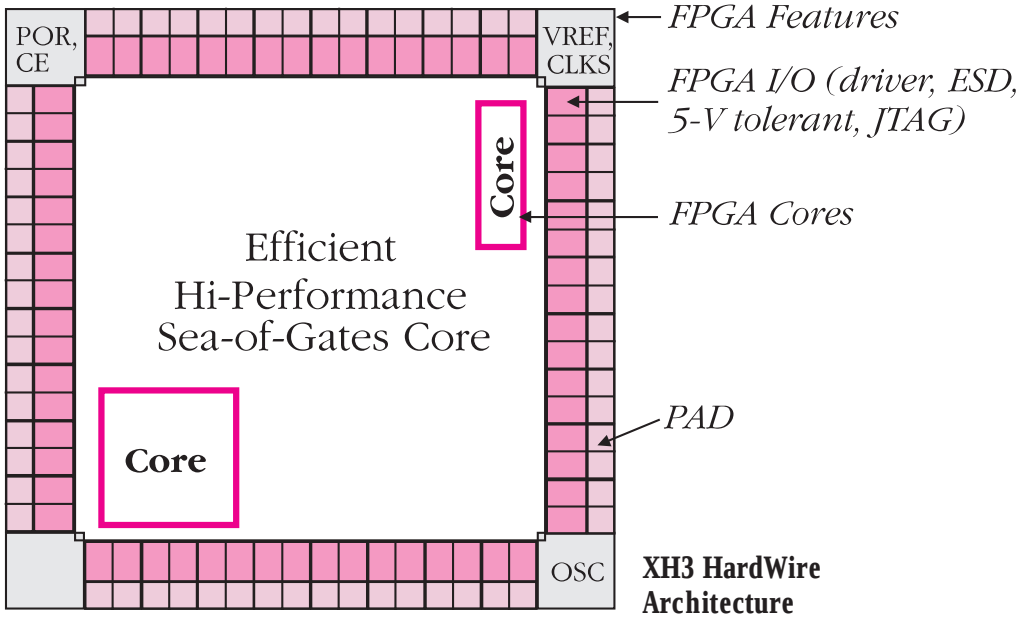
XH3 HardWire ASICs also support Xilinx LogiCORE functions. The PCI macro is completely pre-verified so the transition from FPGA to ASIC is able to encompass tight PCI specifications.

The HardWire DesignLock methodology begins with your completed FPGA files, including the timing, placement and routing information. Throughout the conversion process, these crucial elements are kept intact. The ASIC die are much smaller than the FPGA die, because the programmable elements are replaced with metal vias. However, the relative timing and spatial relationships in the devices are preserved.

As with all conversions, ASIC timing is usually much faster than that of the original FPGA. However, Xilinx tools take all the timing relationships and constraints into consideration so that each path can be precisely verified. Even asynchronous paths can be exactly timed.

The original functionality of the FPGA is preserved throughout the conversion process, eliminating the need for additional vector development. At every step, the conversion process can verify that the original functionality is intact. The Xilinx full-scan methodology generates a complete set of manufacturing fault coverage vectors, with an average fault coverage of over 98%.

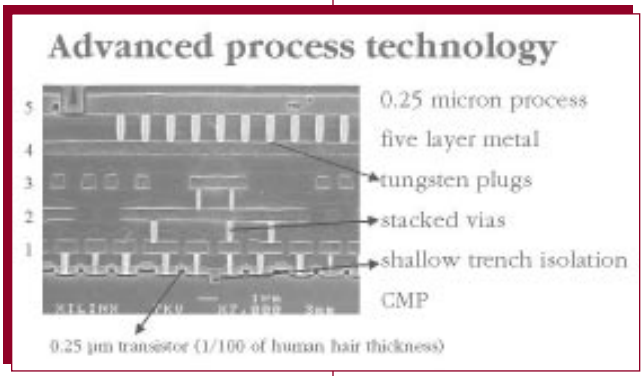
XH3 technology is unique in the FPGA/ASIC industry. The HardWire ASIC conversion process now gives you the luxury of designing with FPGAs, while taking full advantage of ASIC cost reductions. ◆



XH3 HardWire Architecture

The World's First

0.25-micron FPGA Family



Leading the logic industry with the most advanced semiconductor manufacturing processes, Xilinx, in partnership with United Microelectronics Corporation (UMC) has developed a new 0.25-micron FPGA process technology. This leading-edge technology is the basis of our new, very-high-density, XC4000XV FPGA family. The first device in this family, the XC40125XV, incorporates 25 million transistors in a single piece of silicon — more than three times that of today's highest performance microprocessors, such as the Intel Pentium II (with 7.5 million transistors). Samples of the XC40125XV — the industry's largest FPGA device — are available now, and production shipments will begin early in the first quarter of 1998.

Technology Made Possible Through Partnerships

For its 0.25-micron product development, Xilinx partnered with four of its suppliers — Cadence Inc., DuPont Photomasks Inc. (DPI), Dai Nippon Printing (DNP) and UMC.

Xilinx partner **Cadence** provided the physical verification tools necessary to create this new technology. "With 25 million transistors on an FPGA, Xilinx is providing a dramatic increase in capability for its customers," said Bill Portelli, vice president and general manager of the Cadence Custom IC Business Unit. "Xilinx turned to Vampire, Cadence's state-of-the-art hierarchical physical verification tool, to verify the correctness of the world's most complex FPGA device. First-pass working silicon is a testament to excellent IC design, a great tool, and impressive teamwork between Xilinx and Cadence on this project."

Xilinx partners **DuPont Photomasks** and **Dai Nippon Printing** met the challenge of developing a set of photomasks that would unite the Xilinx design specifications with UMC's manufacturing process technology. The extraordinary density of the larger Xilinx FPGA die required DPI's extensive technical expertise to meet the demanding 0.25-micron design and manufacturing specifications. DPI also drew on the strengths of its global network to manufacture the photomasks, with data collection and coordination occurring in Santa Clara, Calif., and actual production taking place in its Ichon, Korea, facility.

Xilinx partner **UMC,** based in Hsin-Chu City, Taiwan, is Taiwan's first private sector manufacturer of integrated circuits. UMC operates two wafer fabs in the Science-Based Industrial Park in Hsin-Chu City. "As the first dedicated foundry to market with 0.25-micron technology, we lead the industry in this next generation of processing. The UMC 0.25-micron CMOS process with dual-gate oxide and five-layer metal is a very demanding and rugged technology that will enable end products with better integrity, yields, quality, and performance," stated Don Brooks, UMC board member. "Furthermore, UMC offers Xilinx and other customers additional advanced technology, including low-voltage and mixed signal capability. With our progress in 0.18-micron technology, we will continue our leadership in process introductions."

"Our close partnerships with industry-leading manufacturing partners has directly aided our delivery of advanced processes," said Wim Roelandts, Xilinx president and chief executive officer. "Furthermore, it's more than just having access to industry-leading technology in order to deliver on this process. Our unique methods for rapid deployment of new architectures on new processes allows us to bring better products to market faster and, in turn, bolster the success of our customers." ◆

0.25µ

The XC4000XV:

Introducing The Industry's First 500K Gate FPGA Family

The new XC4000XV FPGA family delivers densities up to 500,000 system gates (20,000 logic cells). This new family includes four devices, offering system performance greater than 100 MHz, and featuring 2.5-volt internal operation with 3.3-volt I/Os to allow optimum performance and compatibility with existing voltage standards.

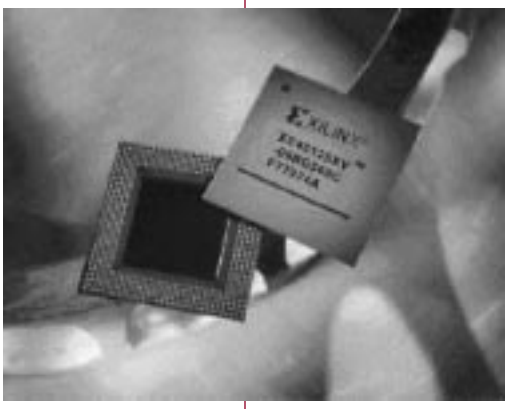
"We announced our five-year roadmap last January, which clearly defined our plans to provide higher-density FPGA families on advanced processes. In the course of six months, we have delivered ten members of the XC4000XL family of high-density and high-performance FPGAs. These are widely accepted by customers as leaders in density and performance," said Wim Roelandts, Xilinx president and chief executive officer. "With our migration to a 0.25-micron process, the XC4000XV FPGA family represents our next leadership step to bring the benefits of FPGA reconfigurability and time-to-market advantages to traditional ASIC users who demand high-performance and high-density logic."

Delivering ASIC Performance and Density, Today

Digital designers who have traditionally used custom ASIC devices are now considering the time-to-market benefits that Xilinx high-density, high-performance FPGAs can offer. According to Jordan Selburn, principal analyst at Dataquest, the Xilinx XC4000XV family, in conjunction with the Xilinx HardWire ASIC capability, can address approximately 45 percent of the 1997 gate-array design starts, based on the XC4000XV maximum performance and density levels.

Vincent Coli, director of product marketing at Aptix, the leader in reconfigurable system prototyping solutions, says "We use Xilinx for their density because it's here today. Our customers are demanding several million gates of programmable logic in our most advanced product, the System Explorer. By using the XC40125XV, the highest density programmable logic device available today, we are able to achieve these density levels."

Architectural Advantages of The XC4000X Series

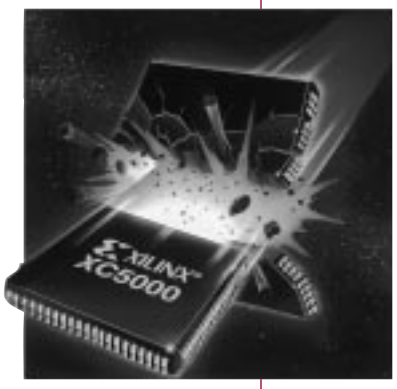


The XC4000XV family is a more advanced implementation of our XC4000EX/XL architecture, which uses segmented routing and distributed RAM. These features make an ideal platform for implementing cores. For example, our segmented routing architecture allows predictable performance regardless of device size or how much logic is employed. With the non-segmented routing used by our competitors, cores will slow down unpredictably as surrounding logic is added or when designs are moved to larger devices. Our performance predictability is a requirement for designs using intellectual property (cores) because you want to choose cores independently of device density, and you expect the core's performance to remain the same as the design evolves. In addition, due to footprint-compatibility advantages, current XC4000XL customers can easily and immediately upgrade to our higher-density XC4000XV products. ◆

The XC4000XV Family

Device	Logic Cells	System Gates	Available
XC40125XV	10,982	80,000 - 265,000	now
XC40150XV	12,312	100,000 - 300,000	Q198
XC40200XV	16,758	130,000 - 400,000	1H98
XC40250XV	20,102	180,000 - 500,000	1H98

The XC5200 Family – *Now 30% Faster*



The XC5200 family is now 30 percent faster with the introduction of the new XC5200-3 and XC5200-4 speed grades. Xilinx introduced the XC5200 family in 1995 as the first FPGAs optimized for the high-volume, low-cost, consumer applications that once required custom gate arrays. Now, due to wide acceptance, the XC5200 is the industry's fastest growing FPGA family, and the third-largest in unit shipments, with more than three million units shipped.

This family offers five devices ranging from 256 to 1,936 logic cells, allowing you to replace gate arrays using up to 20,000 logic gates. The devices come in 17 different packages, in both commercial and industrial grades, including our new VQ64 package that provides the most space-efficient footprint for consumer, hand-held, and other small form factor applications. And, footprint compatibility allows you to easily move to the XC4000 family for higher speed, higher density, on-chip RAM, or 3-volt operation.

The new XC5200 data sheet, with the latest specifications and an expanded architectural description, is available in our new *1998 Data Book* and on WebLINX (www.xilinx.com), the Xilinx site on the World Wide Web. The XC5200-3 speed files with 30 percent higher performance are available from the "file download" area of WebLINX.

All XC5200 devices are fully supported by the Xilinx Foundation and Alliance Series software solutions. The low-cost base system has been extended to add support for the XC5206 and XC5210 devices, in addition to the XC5202 and XC5204 devices. The combination of powerful, easy-to-use software and a low-cost programmable architecture, gives you the shortest time-to-market, eliminating the need for gate arrays, even in high-volume consumer applications. ◆

Using IBIS Specifications

The IBIS files, initiated by Intel, are an attempt to describe the strength of CMOS output drivers as black boxes, giving only voltage and current values without getting into proprietary circuit details. Xilinx now has IBIS files for all FPGA families.

The problem with IBIS is the large number base; usually you just want to know the strength of the pull-down transistor (sink capability) and the pull-up transistor (source capability). Close to either rail, the outputs are resistive, which means the voltage is proportional to the current.

The following table shows the condensed IBIS information, expressed as output resistance in ohms, for a sink voltage less than one volt above ground, and a source voltage less than one volt below Vcc. For the XC4000 devices, with their n-channel pull-up transistors, the source resistance is calculated between two and three volts.

IBIS specifies minimum and maximum current values, converted here to min and max resistor values. ◆

Device Family	Sink Resistance (ohms)		Source Resistance (ohms)	
	min	max	min	max
XC3000A	13.5	19.2	25.6	40.1
XC3100A	12.3	16.9	29.7	46.0
XC4000	14.4	19.8	25.8	33.1
XC4000E	22.1	27.7	53.3	60.5
XC4000EX	14.4	18.8	48.1	58.7
XC5200	20.5	29.4	32.9	54.0
XC4000XL	14.4	20.5	28.0	41.0

Matrox Graphics

The XC5204 is Used in The New Rainbow Runner

Until recently, the home computer has been tucked away in an office or den, separated from other entertainment media such as the television and VCR. But the latest developments in digital video technology are bringing these products together.

At the forefront of this convergence is the Matrox Graphics Rainbow Runner series of video upgrades for Matrox PC add-in cards. Together, Rainbow Runner and Matrox's graphics accelerators open a whole new universe of video at home. They make possible high-quality video editing, frame capture, video conferencing, PC-to-TV output, hardware MPEG playback, and TV on the PC.

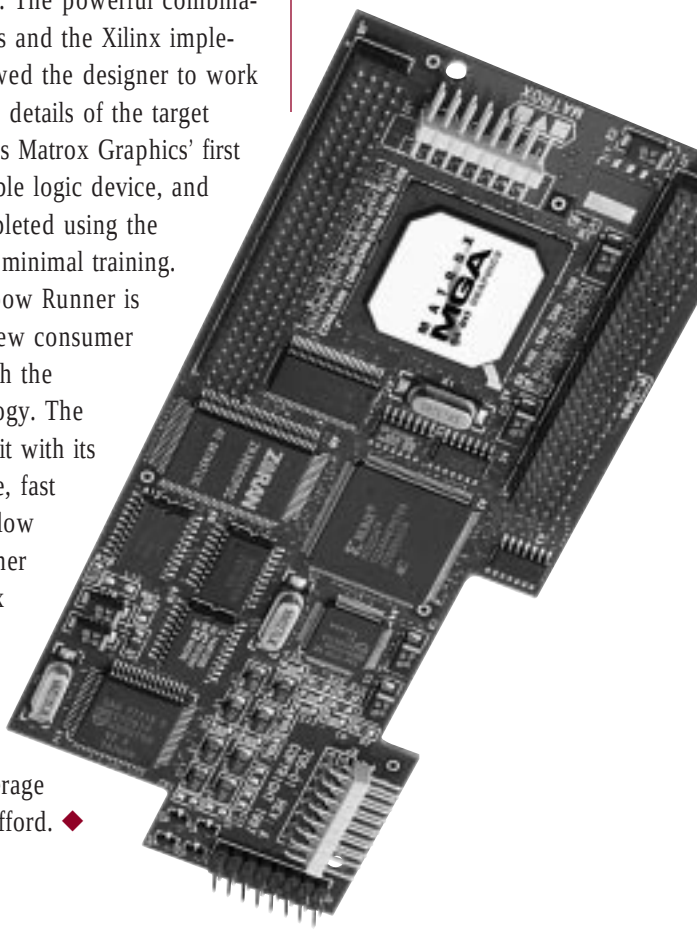
Matrox Graphics, a Montreal-based company that has more than doubled its sales of PC graphics add-in cards in each of the last three years, has selected the Xilinx XC5204 device for the high-volume Rainbow Runner daughtercard. The XC5204 was chosen for this consumer application because of its low cost, high I/O count, and reprogrammability during development. The XC5204 was able to add new functionality without having to redesign the custom graphics processor on the add-in card.

"Matrox is committed to providing innovative, leading-edge technology to deliver the best performance at competitive prices, " says Lorne Trottier, president, Matrox Graphics Inc. The new Rainbow Runner series of video companion cards is an example of the company's commitment to developing breakthrough technology and delivering it at breakthrough pricing. The XC5204 device is used on the Rainbow Runner daughtercard for the Matrox Millenium, providing high-quality video editing, video conferencing, computer-based training, multimedia and Web authoring.

The flexibility of a programmable solution allowed frequent design changes during development, while maintaining the required pinouts. Board space is critical in an add-in card, and the Xilinx XC5200 family enabled a solution that would not be feasible with discrete logic. Plus, a large number of I/Os were needed for the bus interface, met by the 124 I/O points of the XC5204. Matrox expects to sell hundreds of thousands of the daughtercards, and sees no need to go to a fully customized ASIC, even in this high-volume consumer application, because of the Xilinx cost-saving HardWire technology.

The design was created with generic VHDL synthesized by Viewlogic's ViewSynthesis product. The designer chose VHDL because of the ability to make high-level design changes. The powerful combination of ViewSynthesis and the Xilinx implementation tools allowed the designer to work independently of the details of the target architecture. This was Matrox Graphics' first use of a programmable logic device, and the design was completed using the Xilinx software with minimal training.

The Matrox Rainbow Runner is an example of the new consumer applications that push the envelope of technology. The XC5204 is a perfect fit with its powerful architecture, fast time-to-market, and low cost compared to other solutions. For Matrox Graphics, it made possible an advanced video companion card at a cost that the average computer user can afford. ◆



The Hewlett-Packard Companion Scanner - A Partnership Success Story

The Hewlett-Packard Companion scanner is a copier accessory that allows any picture or document to be scanned to an HP Laserjet printer without first downloading the data to a PC. Facing very tight time constraints, the Design Group at the HP Printer Division in Boise, Idaho realized it could not rely on fully customized ASICs as it had in the past.

According to the group's leader, Doug Keithly, they decided to use FPGAs so they could meet the planned product release date.

The FPGA vendor decision was based on three major factors:

1. Level of service (the group was new to FPGA design).
2. A proven cost-reduction path to an ASIC device.
3. The ability to support a non-VHDL PC environment (the designers did not want to spend an additional two weeks learning the rudiments of VHDL design).

HP chose Xilinx because it offered a complete HardWire ASIC cost-reduction plan (including a schedule that met their target), a schematic-based PC development environment, and on-site engineering help.

HP picked the full sea-of-gates HardWire approach for the smallest, most cost-effective die, and Xilinx provided all the vector generation and guaranteed the functionality of the ASIC.

Doug and his team began the development project with a block diagram of the system. Within a month, by using the FPGA, they had a PC board with the first implementation. By the end of the second month, they had achieved 95% functionality and were close to a final solution. During this phase, the system itself was still being defined. After the design itself was finalized, they needed two additional months for other mechanical design including paper handling, motor control, and firmware testing. Because they were constantly making changes during this phase, device programmability was key.

The HP design team used the FPGA to enhance system functionality by using the device for DSP functions, processing pixels at up to 2mb per second. Even the on-board microprocessor could not handle the data speeds required, so all of the signal processing is done by the HardWire ASIC, with the microprocessor providing set-up and coordination between functions.

After four months, HP was ready for final release. They sent the FPGA to Xilinx, and waited two weeks to receive the design conversion report, which looked clean. Within three weeks, Doug had ASIC prototypes in hand.

On the first functional test, the team discovered a potential speed problem. However, with the help of Kiran Buch, a Xilinx HardWire design expert, Doug identified an asynchronous path where speed caused a race condition. The path was not used at all in the design and Doug never checked it in the original FPGA design, so he had not applied constraints to the path as he had to all the other asynchronous paths.

Kiran sent two HP devices back to be de-capped. Using focused ion beam technology, he disabled the path and sent the parts back to Doug. The modified devices worked perfectly. Xilinx made a quick change to the mask and fabricated the modified ASIC. With the HardWire ASIC on the board, the system went to final test where the remaining system bugs were worked out.

The scanner is now in full production and Doug said, "This was a slam dunk for Xilinx. We were *really* pleased." ◆

> *"This was a slam dunk for Xilinx. We were <u>really</u> pleased."*

Major Program Success at **Raytheon T.I.** Made Possible with Xilinx Hi-Rel FPGAs

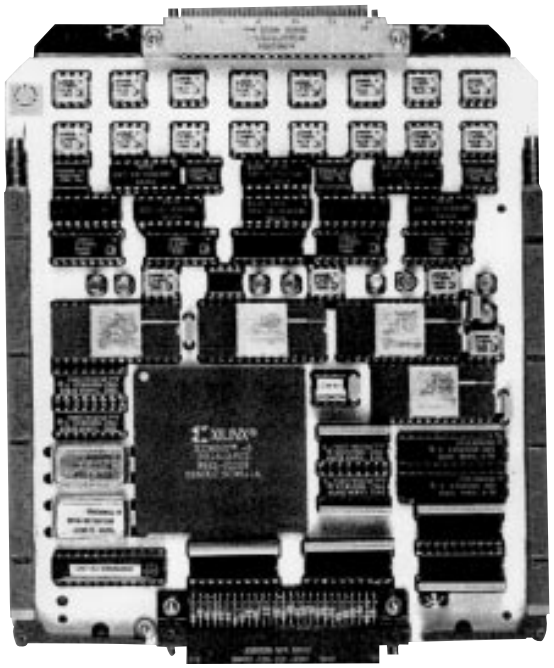
Designers of defense systems have long recognized the benefits of using FPGAs for their system designs. The flexibility, reconfigurability, and easy access to devices used for prototyping are but a few of the compelling reasons why FPGAs are rapidly becoming the technology of choice for defense industry designers. This has been dramatically demonstrated with the recent design successes of a team of engineers at Raytheon T.I. Systems in McKinney, Texas, where they have successfully designed Xilinx FPGAs into their Horizontal Technology Integration (HTI) system.

The HTI system, being developed by Raytheon T.I. and Hughes, is a second generation FLIR (forward looking infrared) system that can be used in many different land-based fighting vehicles, as well as attack aircraft. First generation FLIR fire control systems were used successfully in Operation Desert Storm. However, the development of FLIRs with higher resolution and a longer identification range is critical to extending the advantage of the U.S. and its allies over future adversaries.

The design team at Raytheon T.I. was faced with some formidable challenges — notably, cost and development time. Xilinx high-reliability (Hi-Rel) FPGAs are the heart of the HTI system. However, before this decision could be reached, a careful trade study of Hi-Rel FPGAs versus Hi-Rel ASICs was performed. Careful consideration of Hi-Rel ASIC NRE costs, development time, required design reviews, prototype delivery schedules, and the inherent risks associated with doing an ASIC led to the conclusion that FPGA technology should be preferred.

Mr. Cal Tenhet, Electrical Design Engineer at Raytheon T.I. said, "Because ASIC suppliers are no longer supporting the Hi-Rel market, the rapidly changing technology evolution for ASICs is forcing designers to continually redesign to make timing specifications fit smaller process parameters. While FPGAs are going through a similar evolution, the continued support of Xilinx to the Hi-Rel market enables us to proceed without these continuous redesigns. Additionally, by using Xilinx FPGAs, we did not need to use valuable time and engineering resources generating test vectors."

Multiple Xilinx FPGAs are used in the HTI system to perform numerous control functions. On the scan control CCA (circuit card assembly), an FPGA serves as a microprocessor interface to all A/D-D/A converters. It's also the serial interface to the digitizer CCA, transferring data and signal controls. The FPGA emulates a UART RS232 interface between the video converter and scan control CCAs, generates video timing gates, and provides optical position sensor counters.



Tenhet and the design team at Raytheon T.I. also had to deal with a highly accelerated development schedule for the HTI program. The flexibility of Xilinx FPGAs enabled them to meet a very aggressive schedule, on time.

"We were able to go to layout and pick pin configuration prior to the completion of the design," Tenhet said. "With Xilinx FPGAs, we could make any necessary design changes right up to production. In fact, due to the flexibility of the FPGAs, we were able to do our design sequentially and incrementally —

Continued on the following page

Raytheon T.I.

Continued from the previous page

a real plus given the tight schedule we were working under."

The ability to make system upgrades in the field proved important to the HTI program. "If we need to make upgrades to the system in the field, we can do so by reconfiguring the serial PROMs' firmware, which is very cost-effective," Tenhet said. "We couldn't do this with ASICs."

System designers continue to face the dilemma of finding suppliers committed to the Hi-Rel market. With so many others choosing to exit this market, it has become more difficult for defense industry designers to find reliable long-term sources of supply. Xilinx, a QML supplier to MIL-PRF-38535, and its active SMD program are making this search easier.

"The commitment of Xilinx to the Hi-Rel/Military market also played a very big part in our decision to use their FPGAs for HTI," Tenhet said. "Because of this level of commitment, Xilinx provided high levels of support during the design cycle, and helped resolve problems quickly to keep us on schedule. In fact, because Xilinx acted as part of the design team, our schedule never slipped. The HTI program could not have succeeded without Xilinx Hi-Rel FPGAs, and a lot of the successes enjoyed by our engineering team on this program can be directly attributable to Xilinx." ◆

CPLD CUSTOMER SUCCESS STORY

Ericsson Telecom

Using XC9500 CPLDs for High-Performance Telecommunications Equipment

Ericsson Telecom in Scandinavia has introduced a new line of data communication products used to improve the quality and bandwidth of satellite communication systems. The designers at Ericsson needed the benefits of in-system programmability (ISP) in order to fit the designs into the smallest possible space (they planned to use the latest surface mount packaging, and wanted to program the chips on the circuit board to minimize handling problems).

"Ericsson chose the XC95108-7TQ100C because it met all of these stringent requirements."

This design, which was for a custom, high-performance microprocessor interface, needed to be fast, dense, and extremely flexible. Ericsson chose the XC95108-7TQ100C because it met all of these stringent requirements. The flexibility of the XC9500 CPLDs enabled Ericsson to considerably shorten its logic design cycle, because the design was extremely complex in parts and required several iterations before it functioned correctly.

The Ericsson engineers also found they could fit large amounts of logic into the XC95108, and still make substantial logic changes without any significant changes in device performance or pinouts. Ericsson saved a substantial amount of time and money because the XC95108 maintained fixed pinouts after design changes; therefore, new PC boards were not required. Pin-locking is an especially critical feature in this application because Ericsson estimates there is a very high possibility that at least one field upgrade will have to be performed during each device's lifecycle.

One of the key features of the XC9500 family, which also contributed significantly to Ericsson's choice, was the fact that all XC9500 products can be programmed, debugged, and tested through an industry standard IEEE 1149.1 JTAG Boundary-Scan port. This enables design iterations to be completed very quickly, and greatly simplifies the volume production of the final product. ◆

Synplify Achieving Optimal Synthesis Results

The technical development team of Synplicity, Inc. has been cooperating with Xilinx to deliver Synplify, a fast, easy-to-use synthesis tool that produces extremely high-quality results. The latest version of Synplify supports the Xilinx XC3X00A/L, XC4000E/X, XC5200, and XC9500 families, as well as the XC40125XV device.

Synplify accepts timing constraints placed in a constraint file. In this article you will learn how to apply design constraints for synthesis and optimization.

Design Constraints

Synplify supports user-defined timing constraints to help improve your synthesis results. Timing constraints, for timing-driven synthesis, should be specified in a synthesis timing constraint file, *<design_name>.sdc*, and added into the list of source files. Synplify encourages you to set constraints to closely match your design goal by ±5%.

The following design constraints are used for synthesis and are passed to the implementation tools for timing-driven place and route.

- **Clock Constraint** - Allows you to specify a specific frequency goal for synthesis.

```
define_clock CLK1 -freq 33.0
```

- **Input Delay Constraint** - Allows you to model the interface of the inputs of your FPGA with the outside environment, such as the delay before the signal arrives at the input pin.

```
# Set the input delay on input
  port A to 10.0 ns.
define_input_delay A 10.0
```

- **Output Delay Constraint** - Allows you to model the interface of the outputs of your FPGA with the outside environment, such as the delay of the logic outside your FPGA that is driven by your outputs.

```
# Set the default output delay
  for all outputs to 10.0 ns
define_output_delay -default 10.0
```

Optimization Constraints

Synplify provides optimization constraints, which focus the synthesis engine on critical timing paths within a design; these constraints are not passed to the place and route tools. They control synthesis optimization without over-constraining the place and route engine.

- **-improve <ns>** - Using this option forces Synplify to restructure your design during optimization to try and meet the clock frequency goal. In the example, the input delay for input_a is 1 ns. The "-improve" option forces Synplify to try harder and reduce the clock period by 2.0 ns.

```
define_input_delay input_a
  1.0 -improve 2.0
```

- **-route <ns>** - Using this option forces Synplify to use additional route delay in its calculations to try and meet the clock frequency goal. In the example, the routing delay reported by the place and route engine for input_a was 1.8 ns more than predicted by Synplify. Also, input_a has a 1.0 ns input delay. The "-route" option forces Synplify to re-run and try to improve results by 1.8 ns, by adding 1.8 ns of additional route delay to the timing calculations.

```
define_input_delay input_a
  1.0 -route 1.8
```

Summary

Synplicity is focused on delivering the highest quality results for Xilinx FPGAs and CPLDs. The Synplify 3.0b release introduces a new Xilinx mapper that has shown 5-20 percent performance and area improvements. The Synplify 3.0c release will support features such as:

- Passing timing constraints to the Alliance Series implementation tools.
- Speed and area improvements to the Xilinx mapper.
- Synthesis support for Spartan, Virtex, and XC4000XV. ◆

XILINX®

New UNISIM Libraries for Functional VHDL

With the new UNISIM libraries from Xilinx, you can simulate RTL behavioral code with gate-level instantiations, gate-level descriptions imported from schematics, and gate-level VHDL and Verilog descriptions exported from synthesis, prior to place and route.

> *"The libraries are tailored for synthesis-based HDL design flows and include special HDL support for global signals."*

These new libraries complement the VHDL and Verilog SIMPRIM Libraries currently available for timing simulation, and are available in the Alliance Series and Foundation Series 1.4 software, completing the Xilinx HDL-based flow. **Figure 1** illustrates the new simulation flows that are now possible.

The libraries are tailored for synthesis-based HDL design flows and include special HDL support for global signals. They are called UNISIM to distinguish them from Unified Library schematic-based libraries, and contain all the Unified Library cells used by synthesis, as well as the cells that are instantiated due to limitations in inferencing.

You can now instantiate cells such as I/Os, RAMs, ROMS, oscillators, and so on, in their RTL code, and proceed to simulation without converting your synthesized design to SIMPRIMS. Furthermore, the UNISIM Libraries are fully compatible with the LogiBlox-generated behavioral models. Designs can have both LogiBlox and UNISIM instantiations. Alliance synthesis vendors are planning to write structural VHDL and Verilog that is compatible with the UNISIM libraries to enable the post-synthesis simulations that are particularly useful for verifying high-density synthesis results prior to implementation.

Because Verilog lacks a configuration statement to choose between different behavioral models, a Verilog library has been created for each Xilinx technology. VHDL, on the other hand, does have a configuration statement, allowing you to select between different models for the same component. Therefore only one VHDL library has been created for all Xilinx technologies.

Whether the pre-route descriptions are VHDL or Verilog, special attention must be paid to global signals in HDL code. Both the VHDL and Verilog UNISIM libraries have mechanisms for handling GSR, GR, PRLD, and GTS signals to match pre-route and post-route initializations. The mechanisms are adapted to use the features that are best suited for each language.

The Verilog testbench can be used to drive internal signals. Therefore, the UNISIM library uses Verilog macros to define global signals. You set variables to drive the GSR, GR, PRLD, or GTS global signals used in the macros. After the variables are defined, the macros are activated and the reset and configuration 3-state conditions are enabled.

VHDL in contrast, requires a port for every signal to be stimulated by a testbench. Furthermore, it also does not have a good mechanism for handling global signals in a way that is VITAL compliant. Therefore the following five unique cells have been developed to support the VHDL synthesis and simulation design flow:

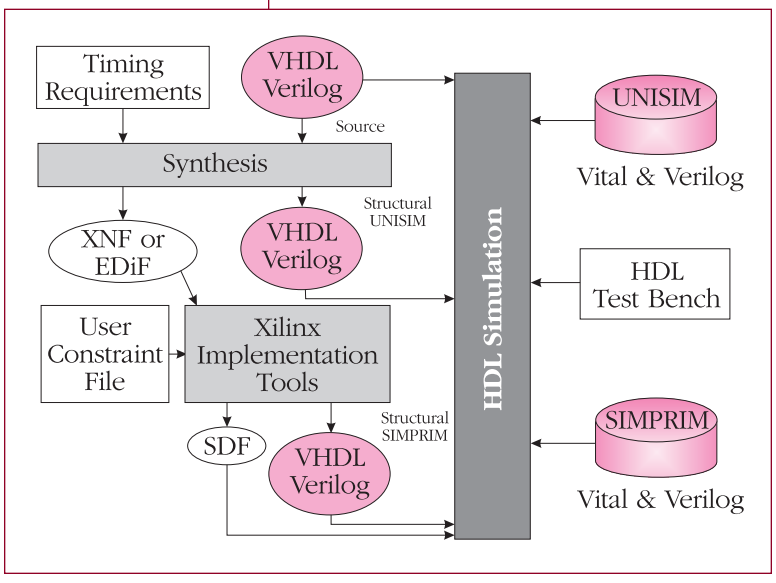


Figure 1 - *UNISIM libraries.*

and Verilog Simulations

- **ROC**: Emulates the chip-generated *reset on configuration* pulse.
- **ROCBUF**: Allows the testbench to drive the chip-generated *reset on configuration* without implementing an actual input pin on the chip.
- **TOC**: Emulates the chip-generated *3-state on configuration* pulse.
- **TOCBUF**: Allows the testbench to drive the chip-generated *3-state on configuration* without implementing an actual input pin on the chip.
- **STARTBUF**: A technology-independent version of the STARTUP block supported for simulation.

These five cells allow control over the global reset and 3-state signal emulation so you can create pre-route initialization simulations to match post-route simulations. The cells also drive implementation tools to add or delete pins, and to select which net is to be routed as the GSR, GR, PRLD, or GTS net.

Summary

The UNISIM libraries for Verilog and VHDL give you an HDL flow for RTL with instantiations, imported schematics, and post-synthesis functional simulations. The libraries are completely compatible with synthesis- and LogiBlox-oriented flows and will help you match your pre-route global signal initializations with your post-route simulations. ◆

INNOVATIVE APPLICATIONS

An FPGA Can Control Its Own Reconfiguration

An XC4000 or XC5200 FPGA can initiate its own reconfiguration by driving its own PROGRAM input Low. This is a reliable operation although the reconfiguration sequence stops the output from driving PROGRAM Low; the reconfiguration process, once triggered, will continue.

For example, an FPGA could have multiple configurations stored in a parallel PROM, selected by a binary switch that drives the upper PROM address lines. The FPGA could also use these codes as input, comparing them against an internal code that is uniquely determined by the configuration. When you turn the switch, the mismatch is detected and a new reconfiguration is initiated, according to the new switch setting. The reconfiguration could also be delayed until additional conditions are met.

Even without a manually operated switch, the FPGA can initiate reconfiguration to a selected section of the parallel PROM if an external CMOS latch or register is used to maintain the most significant bit(s) of the new PROM address throughout the configuration process.

If you have any novel FPGA or CPLD applications that you would like to share with other readers, send them to editor@xilinx.com. ◆

Xilinx is now shipping Foundation Series design solutions capable of supporting both VHDL and Verilog.

The Foundation Series Software Now Delivers VHDL and Verilog

Our Foundation Series software remains simple, yet continues to deliver complete front-to-back development tools supporting all Xilinx CPLD and FPGA devices. There are two schematic packages and two HDL packages. Both Foundation Series HDL packages include VHDL and Verilog, design entry, synthesis using the Synopsys FPGA Express, and implementation tools from Xilinx.

Increased Software Performance

The rapidly increasing performance capabilities of FPGA and CPLD technologies demand increased performance from design solutions. In fact, the latest architecture from Xilinx delivers 1,000,000 gates at speeds greater than 100MHz.

To meet that challenge, Foundation software solutions are continually enhanced to provide high-quality results in a ready-to-use package. The software delivers push-button tools without compromising device complexity, functionality, or density.

The Foundation HDL tools have been specifically designed to quickly move you through the HDL learning curve; the moment the tools are taken out of the box, you can quickly install the product and be implementing designs in minutes. If you have exceptional needs, Xilinx offers comprehensive support services providing assistance on Xilinx technologies as well as advanced application assistance.

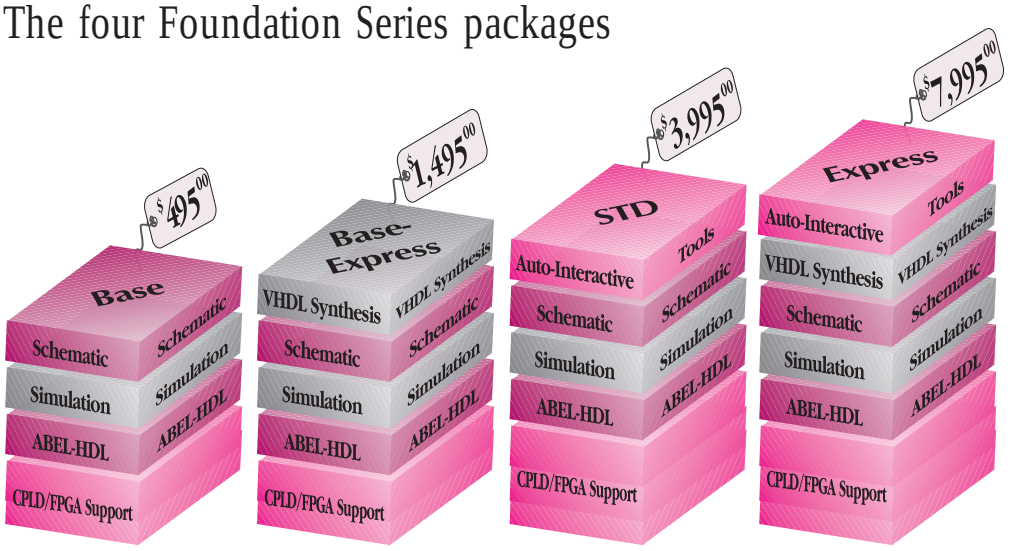
Powerful Synthesis

This past year, Xilinx added the Synopsys Express technology to the Foundation Series software. With Synopsys' history of providing state-of-the-art synthesis solutions for high-density designs, it's not surprising that the new Foundation Express product is particularly effective for large programmable logic devices. There are many advanced synthesis features in Foundation Express, including timing optimization, area optimization, graphical constraint entry and analysis.

New Product Configurations

There are four Foundation packages: Base, Standard, Base Express, and Express. Base and Standard packages support XABEL for CPLDs but do not support VHDL or Verilog. Base Express and Express support XABEL, VHDL, and Verilog languages. Although there are device size limits in the Base and Base Express products, all Spartan devices are supported by all Foundation packages. All of the Xilinx Foundation Series packages are available today for PC platforms running Windows 95 and Windows NT platforms.

The four Foundation Series packages

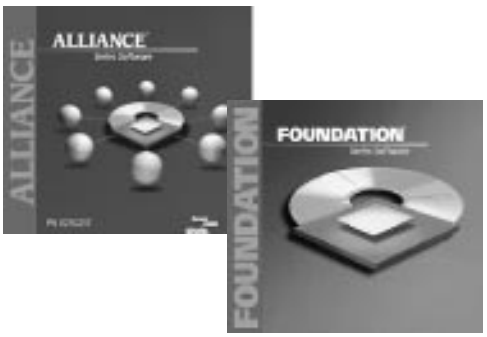


Visit the Xilinx WebLINX Web site (www.xilinx.com) or contact your local Xilinx representative for more information or to request a demonstration. ◆

Alliance and Foundation Series Software Configurations

Last year, we released our Alliance and Foundation Series software solutions. This innovative software gives you the best FPGA and CPLD development tools in the industry, in a range of configurations designed to meet your needs on any platform. These configurations cover the entire spectrum of programmable logic from schematic-based CPLD designs to HDL-based high-density FPGA designs using LogiCores.

To help you choose the best solution for your needs, this article describes the available software configurations.



Alliance Series

Choose the Alliance Series if you want to integrate Xilinx software into your existing EDA tools environment. With this series, you can choose from the widest range of design methods in the industry.

This product line works on both PCs and workstations, and comes in two different versions. The Alliance **Base** is limited to a maximum of 10,000 gate FPGAs and the Alliance **Standard** supports our full range of FPGAs. Both Base and Standard versions include support for our CPLD devices, libraries and interfaces, and the LogiBLOX module generator.

In addition, using the new Alliance Series Turns Engine, you can achieve clock performance improvements of up to 25% by running an unlimited number of place-and-route runs on multiple workstations.

ALLIANCE BASE	
PC	DS-ALI-BAS-PC
Workstation	DS-ALI-BAS-WS
ALLIANCE STANDARD	
PC	DS-ALI-STD-PC
Workstation	DS-ALI-STD-WS

Foundation Series

Choose the Foundation Series for a complete, ready-to-use development system that incorporates design entry, synthesis, simulation, and FPGA/CPLD implementation tools into a single, fully integrated design environment.

The Foundation Series is also divided into **Base** (limited FPGA gate count) and **Standard** versions, and is only available for the PC. In addition, there are VHDL options for Standard or Base versions, and a system called Foundation Express which incorporates the Synopsys FPGA Express technology.

Foundation Base	DS-FND-BAS-PC
Foundation Base w/Express	DS-FND-BSX-PC
Foundation Standard	DS-FND-STD-PC
Foundation Express	DS-FND-EXP-PC

LogicCORE Development Options

We also offer two Core solutions available as options for the Alliance and Foundation Series: the PCI target and initiator, and the PCI target only. See our web site for more information on our PCI cores.

PCI Target & Initiator	DO-DI-PCIM
PCI Target only	DO-DI-PCIS

For the most recent pricing, availability, and upgrade options, contact your local Xilinx sales representative. ◆

System-Level Design Capabilities Using Active-CAD From Aldec

By complementing the Xilinx Foundation Series software with a new configuration of Aldec's Active-CAD™ product, you get system-level design capabilities. The "Active-CAD for Xilinx" promotion enables Foundation users to design and simulate multiple Xilinx devices along with CMOS, TTL, and memory components; microprocessor simulation models are also available for an additional licensing fee. Because Active-CAD uses the same core EDA technology as the Foundation Series, you will be immediately productive. One environment now supports both PLD and system-level design.

The Xilinx Foundation Series software delivers a complete design solution for all Xilinx programmable logic devices. Foundation's use of a standard Windows interface in a mixed mode (HDL and Schematic) design environment ensures that you can effectively and immediately design Xilinx programmable logic devices. While the Foundation Series has become the solution of choice for many Xilinx customers, the application of Aldec's system-level design tools and techniques can be employed to further improve your overall design process.

"I previously spent six weeks debugging a system-level design that contained multiple Xilinx FPGAs and discrete logic devices. Since purchasing Active-CAD, I have been able to debug the same design within days,"

"Aldec's contributions to the Foundation Series solution are key to the product's success. Their extension of these technologies to the Active-CAD for Xilinx promotion ensures a highly integrated, easy-to-use, system-level design solution for Xilinx designers" said Rich Sevcik, executive vice president of software development for Xilinx.

The use of system-level design techniques has enabled many Xilinx customers to accelerate their design cycle by allowing the simulation of multiple Xilinx devices along with discrete logic components.

"I previously spent six weeks debugging a system-level design that contained multiple Xilinx FPGAs and discrete logic devices. Since purchasing Active-CAD, I have been able to debug the same design within days," says Don Conemac, vice president of hardware development for Advanced Laser Technology.

In addition to extending the design entry and simulation capabilities of the Xilinx Foundation Series solution, Aldec's Active-CAD software offers proven integration into the industry's most popular PCB layout tools. This tight integration allows you to complete your programmable logic and PCB designs on any standard Pentium-class PC.

The Active-CAD for Xilinx promotion is sold exclusively by Aldec and its authorized worldwide distributors. Registered, in-warranty customers owning any Xilinx Foundation Series product are eligible to take advantage of this special offer.

To order Active-CAD, or to receive more information on its capabilities, contact Aldec, Inc. Three Sunset Way, Suite F, Henderson, NV 89015 – Tel. 800-487-8743 x17, Fax 702-456-1310, info@aldec.com ◆

Industry's Highest Performance PCI Solution for FPGAs

MEMBER PCI LOCAL BUS SPECIAL INTEREST GROUP

You can achieve the highest possible performance in your PCI applications by using our latest LogiCORE™ PCI interface and our new XC4000XLT FPGA family. The XC4000XLT family includes the XC4013XLT, XC4028XLT, and XC4062XLT, all optimized for PCI. The biggest device allows you to integrate the PCI interface plus 124K system gates of application-specific logic. Some Xilinx customers have achieved 124 Mbyte/sec throughput. And, for high-volume applications, you can migrate your design to a low-cost HardWire FpgASIC.

The LogiCORE PCI Interface v2.0 supports fully-compliant zero-wait-state bursts, and has a well-defined and well-documented backend interface, allowing maximum sustained performance. In addition, the XC4000XLT family has the same SelectRAM feature as the rest of the XC4000 series. With SelectRAM memory you can build a dual-port, synchronous or asynchronous FIFO, sized to support your application. So, you have everything you need to quickly design a complete system that supports the highest possible bandwidth over the PCI bus.

The XC4000XLT family is optimized for PCI and the devices include the required upper clamp diodes on the PCI inputs. This clamp diode is mandatory for a 3.3-volt PCI system to ensure data integrity. These diodes are connected to eight separate VTT pins, which are connected to 3.3 volts for a 3.3-volt PCI system or 5 volts for a 5-volt PCI system. **Table 1** lists the supported XC4000XLT device/package combinations and the number of system gates that are available for your specific backend function.

Using the Xilinx PCI core, you can quickly complete your design with a flexible FPGA, debug and verify PCI compliance of your board by plugging it into different vendors' PCs, and then convert the FPGA to a HardWire FpgASIC for low-cost, high-volume production.

During the conversion process, Xilinx will review the design to ensure that the HardWire FpgASIC is fully compatible with the FPGA and automatically generate the necessary test programs for manufacturing. The HardWire solution allows you to complete a customized, one-chip, PCI interface with your unique backend design, at a price that is lower than most standard PCI chips currently available on the market.

"The HardWire solution allows you to complete a customized, one-chip, PCI interface with your unique backend design, at a price that is lower than most standard PCI chips..."

Xilinx intends to provide you with PCI solutions that allow you to design the highest performance and highest density PCI systems. When the first LogiCORE PCI interface was released in 1995, Xilinx was the first FPGA vendor to support the PCI market. Today, Xilinx has a complete engineering and applications team dedicated to PCI, and the most robust PCI core in the market, licensed to almost 300 customers.

For more information on the Xilinx PCI solution and other core products, please visit the Xilinx Web site, WebLINX at www.xilinx.com/products/logicore/logicore.htm. ◆

Table 1:
Supported XC4000XLT devices and available user-gates

Device	P/HQ208	P/HQ240[1]	BG432	Typical Gate Range available for user design[2]
4013XLT	✓	✓		4,000 - 6,000
4028XLT		✓		12,000 - 44,000
4062XLT		✓	✓	34,000 - 124,000

1) All devices pin-compatible in P/HQ240
2) Max values of Typical Gate Range include 20-30% of CLBs used as RAM/FIFO

I/O Characteristics of the XC4000XL/XV and Spartan XL Families

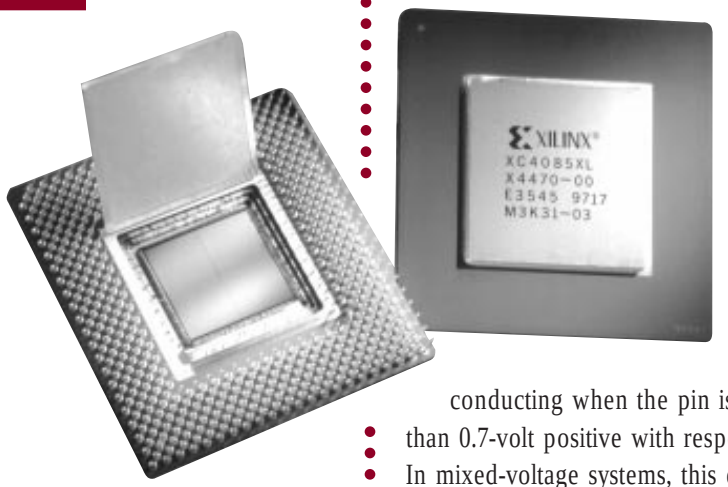
By Peter Alfke

This article describes the electrical input and output characteristics of our new 3.3-volt device families. Input thresholds and 5-volt tolerance are described, the output source and sink impedances are listed, and the effect of additional capacitive loading on delays, rise-times, and fall-times is explained.

Inputs

Input threshold is stable over temperature, but proportional to Vcc: 37-38 percent of Vcc for the falling threshold, 39-42 percent for the rising threshold. And, there is 50-150 mV of hysteresis, smallest at hot and high Vcc, largest at cold and low Vcc.

Many systems will still use a mixture of older 5-volt devices and newer 3.3-volt devices. This can pose a problem when a 5-volt logic High drives a 3.3-volt input. On most CMOS ICs, each signal pin has a clamp diode to Vcc to protect the circuit against electrostatic discharge (ESD). This diode starts conducting when the pin is driven more than 0.7-volt positive with respect to its Vcc. In mixed-voltage systems, this diode presents a problem, because it might conduct tens of milliamps whenever a 5-volt logic High is connected to a 3.3-volt input.



In the XC4000XL/XV and Spartan XL devices, Xilinx has overcome this difficulty by eliminating the clamp diode between the device pins and Vcc. The pins can thus be driven as High as 5.5 volts, irrespective of the actual supply voltage on the receiving input. These devices are therefore unconditionally 5-volt tolerant; you can ignore all interface precautions, and need not worry about power sequencing.

Excellent ESD protection (up to several thousand volts) is achieved by means of a patented diode-transistor structure that connects to ground, and not to Vcc. The structure behaves like a Zener diode; it becomes conductive at greater than six volts and diverts the charge or current directly to ground. It can handle current spikes of several hundred milliamps, but continuous current must be kept below 20 mA to avoid reliability problems caused by on-chip metal migration.

For more information, see our application note: XAPP080 "Supply-Voltage Migration, 5 V to 3.3 V."

PCI-Compliance

The Xilinx 'XL I/O structure is designed to be PCI compliant and also 5-volt tolerant. PCI compliance requires a clamping diode to Vcc. On the other hand, 5-volt tolerance does not permit such a diode. Therefore, the n-well of

"Excellent ESD protection (up to several thousand volts) is achieved by means of a patented diode-transistor structure that connects to ground, and not to Vcc."

XILINX®

the p-channel output transistor must not be tied to the 3.3-volt Vcc because the parasitic diode would prevent the I/O pin from going substantially more positive than 3.3 volts. To satisfy these conflicting requirements, an internal diode is added to each output, with its cathode connected to an internal Vtt rail.

In the PCI-compliant XC4000XLT devices, the Vtt rail is internally connected to eight device pins which externally must be connected to the appropriate Vcc supply (5-volt or 3.3-volt). In all other 'XL devices, the Vtt rail is internally left unconnected, thus assuring 5-volt tolerance.

Output Source and Sink Capability:

The strength of the pull-down transistor (sink capability) and the pull-up transistor (source capability) are shown below. Close to either rail, the outputs are resistive, which means the voltage is proportional to current.

The table below shows the condensed IBIS information expressed as output resistance in ohms, for a sink voltage less than one volt above ground, and a source voltage less than one volt below Vcc. IBIS gives minimum and maximum current values, converted here to min and max resistor values. This data is based on SPICE simulation.

Device Family	Sink Resistance to GND (ohms)		Source Resistance to Vcc (ohms)	
	min	max	min	max
XC4000E	22.1	27.7	53.3	60.5
XC4000EX	14.4	18.8	48.1	58.7
XC4000XL/XV SpartanXL	14.4	20.5	28.0	41.0

"These results are consistent with the IBIS-derived output impedance."

Effect of Additional Capacitive Loading on Transition Times and Delays

- **Transition Time:** At the specified 50 pF external load, the rise time is 2.4 ns, and the fall time is 2.0 ns. For additional capacitive loads, add 60 ps/pF to the rise time, and 40 ps/pF to the fall time.
- **Delay:** Add 30 ps/pF to the rising-edge delay at 3 volts, add 23 ps/pF at 3.6 volts. Add 25 ps/pF to the falling-edge delay at any supply voltage. These values were derived from measurements using the fast output option, but the slew-rate limited output option behaves almost identically.

These results are consistent with the IBIS-derived output impedance, because the delay increases with approximately one RC time constant, and the rise and fall times increase with approximately two time constants. These are not guaranteed and tested parameters; they were established by sampling a few devices. Therefore, we suggest that you add a 20 percent guardband (multiply by 1.2) when calculating additional delay due to capacitive loading above the guaranteed test limit of 50 pF.

For the same reason, subtract 20 percent (multiply by 0.8) when calculating reduced delay due to a capacitive load that is less than 50 pF, external.

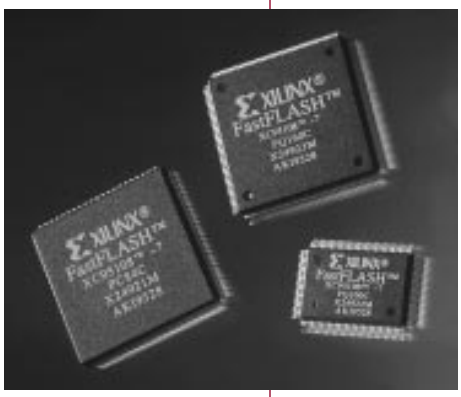
When comparing Xilinx numbers to those from competitors who use 35 pF as a standard load, reduce the Xilinx-specified delay by 0.4 ns, the rise time by 1.0 ns, and the fall time by 0.6 ns, thus changing both to 1.4 ns.

For an external lumped capacitive load of 200 pF, the rising-edge delay increases by 1.2 x 150 pF x 30 ps/pF = 5.4 ns over the guaranteed data sheet value.

The rising-edge transition time increases by 1.2 x 150 pF x 60 ps/pF = 10.8 ns over the 50-pF transition time of 2.4 ns. The rise time is thus 13.2 ns. ◆

Using XC9500 JTAG and ISP in Manufacturing

Our XC9500 CPLD family includes a unique combination of JTAG test capability and in-system programmability (ISP) that can save considerable time and money during the manufacturing process. Because the ISP and JTAG functions are both controlled through the same industry-standard, four-wire JTAG port, automatic test equipment (ATE) can perform system test, device test, and device programming in one integrated operation. And, Xilinx supplies the tools that make this easy.



A large number of Xilinx customers have successfully integrated the XC9500 ISP capability into their manufacturing flows, choosing to simply integrate JTAGProgrammer (formerly known as EZTag) into their final test process to program their XC9500 devices. Because Xilinx devices are shipped from the factory in an erased state, the "skip erase before programming" option can be used to reduce programming time, maximize product flow through the process, and reduce costs.

Other Xilinx customers have determined that it is more economical to integrate the programming step directly into their manufacturing tests. This effectively uses their ATE as programming hardware. This method, while conceptually more complicated, can make better use of available hardware resources. It can also reduce the total number of steps in the manufacturing process, thereby streamlining and optimizing operations, and eliminating fallout due to increased handling.

Xilinx supplies a set of free tools to facilitate this integration (available from our Web site, WebLINX, at www.xilinx.com). These tools retarget the standard serial vector format (SVF) Boundary-Scan stimulus description language to the native stimulus input formats for the industry's most popular ATEs. Full support is available for the Hewlett Packard HP3070 series, the GenRad GR228X series, and the Teradyne Z1800 series of ATE.

In the manufacturing environment, stray electrical noise can result in incorrect Boundary-Scan test failures. In the same manner, this noise can contribute to ISP operation failures. Therefore, all XC9500 devices include the optional Boundary-Scan HIGHZ instruction which forces all device pins into a 3-state condition. Xilinx XC9500 CPLDs are the only type that make this optional instruction available. You can use this instruction to make certain that XC9500 devices act as a "quiet" Boundary-Scan neighbor during ISP and test operations.

By forcing the XC9500 device outputs into a 3-state condition, while other parts are being tested or programmed, you can minimize the noise generated by active system signals and effectively "silence" the board. Many test engineers have made use of this functionality in improving their overall system test and ISP reliability.

By supporting the optional Boundary-Scan IDCODE and USERCODE instructions, XC9500 devices are fully identifiable as to their type and programmed contents so that you can selectively run tests based on the PLD composition of the system under test, or based on the contents of those devices.

Finally, gross functional test via the 4-pin Boundary-Scan interface is supported by the optional INTEST instruction. This allows for the application of functional test stimuli using low-pin-count testers or other Boundary-Scan-based tools.

Xilinx is the only CPLD manufacturer providing this high level of JTAG and ISP functionality, thus continuing to make major advancements in the practical application of ISP in the manufacturing environment. ◆

"Xilinx is the only CPLD manufacturer providing this high level of JTAG and ISP functionality."

Designing With XC9500 CPLD Family User-Programmable Grounds

XC9500 CPLDs have a unique feature that helps you create rock-solid designs. User-Programmable Grounds (UPGs) are a very easy way to provide additional noise immunity if you have very large numbers of simultaneously switching outputs (SSOs). UPGs can also deliver a correct (non-floating) CMOS voltage level to a floating output pin. This is done with a special programming cell that connects the output pin to an external ground or internally forces the output driver low, while retaining the macrocell logic capability behind the pin, as illustrated in **Figure 1**.

Using UPGs

When macrocell outputs change state, they may produce current transitions for a few nanoseconds, causing the internal device ground voltage to rise. If you have a very large number of SSOs, this ground rise could possibly cause unwanted state transitions. By providing additional grounds, near the SSOs, this unwanted ground rise can be kept well within safe limits by providing a low impedance path to dissipate the voltage spikes.

If you have more than 20 SSOs, with a load capacitance of 50 pF or more, UPGs can be very useful, giving you extra noise margin. It takes approximately three UPGs to deliver the same grounding capability as a dedicated ground pin. If you have large numbers of unloaded SSOs (a total of well over 100 is acceptable) or less than 20 loaded SSOs, no UPGs are needed.

Software Support

Using the Design Manager in the Xilinx Alliance Series and Foundation Series software, you can easily specify that all unconnected output pins must become connected to a UPG. If you are unsure about what may be connected to these unused pins, it is best to avoid this UPG setting, because you could accidentally ground any attached external signals. However, if you have completed your design and wish to tie-off unused macrocell outputs or introduce extra grounding benefit, set "UPG ON." It can be reset in the future if needed, by taking advantage of the XC9500 family's in-system programability.

In general, UPGs are convenient for terminating unused output signals. On the rare occasion where additional grounding may be beneficial, UPGs become an even more valuable asset. ◆

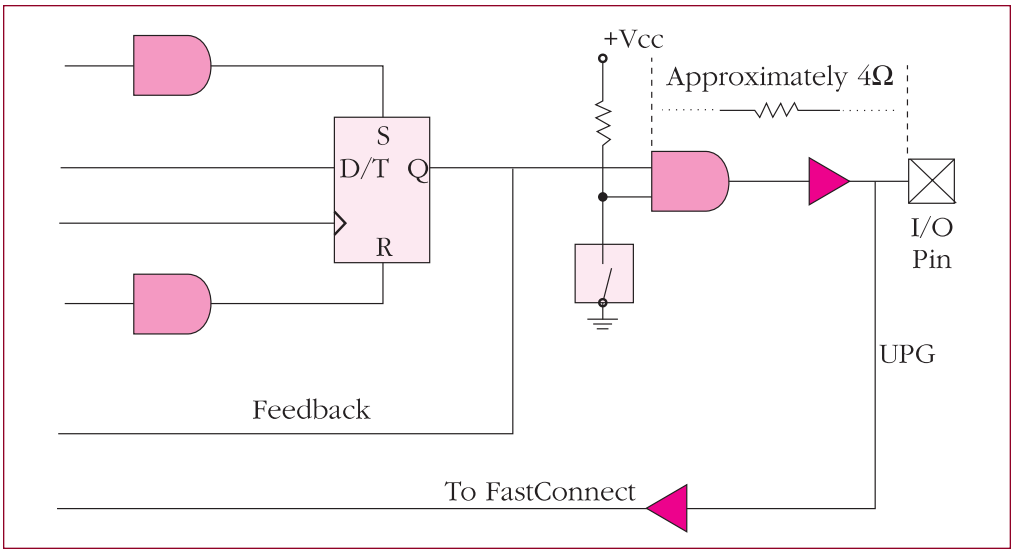


Figure 1 - *UPG for XC9500 devices*

A 200-MHz Pulse Generator

By Peter Alfke

Using XC4000E or XC4000XL devices, you can reliably clock and manipulate data at up to 200 MHz, over the full voltage and temperature range.

In the design example shown in **Figure 1**, the frequency of a commercially available 100-to-200 MHz Voltage Controlled Oscillator (VCO) is divided by any selected power of 2, from 2^0 to 2^{23}, generating an output frequency that covers the range from 12 Hz to 200 MHz.

The output frequency is potentiometer-adjusted over a 2-to-1 range, and is switch-selected over 24 octaves. The frequency scaler uses seven CLBs, and the switch encoder uses six CLBs. Thus, the design, including the switch encoder, uses a total of 13 CLBs — a mere 13% of the smallest XC4000E family device.

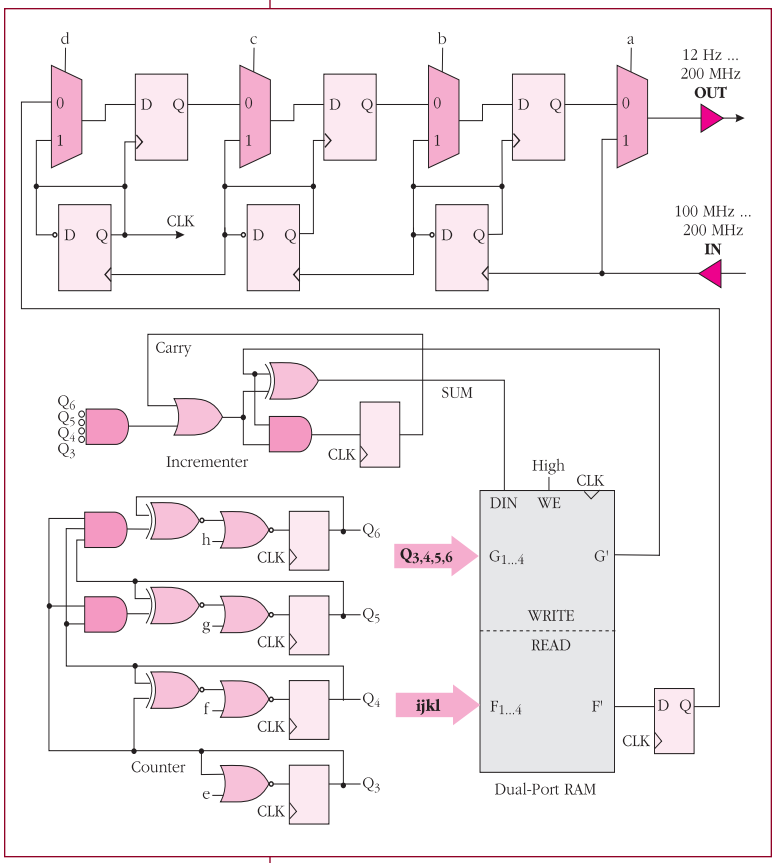


Figure 1 - *A 200 MHz pulse generator with 24 frequency ranges.*

The VCO output clocks one CLB. This CLB is placed directly adjacent to the oscillator input and the output drivers, thus minimizing the speed-critical part of the design. Two additional CLBs complete a 3-bit ripple counter and an output signal multiplexer; because this is an instrument with a single output, there is no reason to design these very fast stages as synchronous counters. However, the remaining 20 binary divider stages are implemented as a synchronous RAM-based state machine, using two CLBs as a counter, one CLB as an adder, and one CLB as a 16-bit dual-port RAM.

Q3 through Q6 address the synchronous RAM, which effectively acts as an adjustable-length shift register. Four control inputs determine the cycle length of the address counters to create a 1-, 2-, 4-, 8-, or 16-bit shift register. The shift register output feeds back to its input through a serial adder, thus implementing a serial incrementer or counter, which is 1, 2, 4, 8, or 16 bits long.

When the read port addresses location zero continuously, it sees a level change for every period of the variable-length address counter. The re-synchronized read output thus divides the RAM clock rate by 2, 4, 8, 16, or 32, as determined by the period of the Q3-Q6 counter.

When the counter divides by 16, the RAM output frequency can be further reduced by advancing the read address. Each address increment reduces the output frequency by a factor of two. A constant read address of all ones creates the lowest output frequency, which equals the RAM clock frequency divided by 2^{20} or the VCO frequency divided by 2^{23}. The 50% duty cycle output frequency can thus be adjusted to any value from 200 MHz to 12 Hz.

This example shows that FPGAs can be used at clock rates that are far above the limitations of conventional synchronous state machine designs. As FPGAs continue to migrate to faster processes, these limits will be pushed even farther, but there will always be an opportunity to achieve the seemingly impossible, through creative understanding of device architecture and I/O capabilities. ◆

An Innovative Way to Reduce Electromagnetic Interference

By Peter Alfke

Unwanted EMI (electromagnetic interference) can be difficult and expensive to control. Usually, designers simply shield their systems in order to comply with regulations. However there is another, less expensive alternative.

Most digital systems are clocked by a stable, 50% duty cycle, crystal-controlled frequency. This simplifies design, debugging, and timing margin analysis, but also generates a high level of EMI — at the clock frequency, its third harmonic, and its fifth harmonic.

By frequency-modulating the clock, you can spread the radiated energy over a wider band and thus reduce the energy at any specific frequency. Spreading a 40 MHz clock frequency just ±2.5% (between 39 and 41 MHz) reduces the amplitude of the fundamental frequency by 9.5 dB, the third harmonic by 11.2 dB, and the fifth harmonic by 13.0 dB. It would take expensive shielding to achieve a similar reduction.

Many display systems and telecom devices cannot tolerate a frequency-modulated clock, but where applicable, a spread-spectrum clock can offer an inexpensive solution to a difficult problem.

International Microcircuits offers a number of low-cost crystal-controlled EMI-reducing oscillators. Visit their web site (www.imicorp.com) for more information. ◆

Using Decoupling Capacitors in 3.3-V Systems

A power supply decoupling structure is like a tree, starting at the supply and ending at the individual Vcc pin. At each level, you should not allow a voltage drop (delta V) of more than 30 mV.

General Formula: delta V = I • t / C

The following example shows how to calculate capacitor values in a typical application. These calculations ignore the series inductance in each capacitor, and make assumptions about power and frequency that may not fit every application.

There is a decupling capacitor at every Vcc pin. A dc current of 200 mA per pin is a reasonable assumption, but this current might come as a 1-Amp spike with 20% duty cycle at perhaps 40 MHz:

C= 1 A • 5 ns / 30 mV = 150 nF = 0.15 µF

This capacitor also must support the charging of load capacitors. Let's assume eight pins with 50 pF each = 400 pF total:

C= 3 V • 0.4 nF/ 30 mV = 40 nF = 0.04 µF

This means that a 0.1 µF decoupling capacitor is marginal for supplying the internal dynamic current (1 A•5 ns), but can easily supply eight full-swing outputs.

There is a larger capacitor, one per device, that evens out slower current changes. This capacitor might supply 5 Amps dc for a microsecond:

C = 5 A•1 µs / 30 mV = 150 µF.

At the output of the switching supply is a capacitor that supplies 50 Amps to the whole board, and covers the 100 kHz period of the switching supply:

C= 50 A • 10µs / 30 mV = 15,000 µF.

Vcc decoupling is important, and becomes more critical as chips get bigger, as clock frequencies and supply current increase, and as supply voltage decreases. ◆

By Peter Alfke

The Dangers of Hot Plug-In

Plugging a board or device into a powered-up system is dangerous because the pins make contact in an unpredictable sequence. There may be many milliseconds from making the first contact to the last one, and it's what occurs in between that causes the problem.

"The normal ramping up of Vcc in a digital system is complicated enough.... A haphazard plug-in procedure is much worse. You should avoid hot plug-in unless the equipment is specially designed."

In the best cases, ground and Vcc mate first before any signal pins make contact. There are connectors that enforce such a mating sequence; their ground and Vcc pins are longer, so they always mate first. These kinds of sockets are popular in telecom applications where hot plug-in is standard practice. With such specialized connectors, there are no electrical hazards, and you need only be concerned about the unpredictable sequence of logic connections being made. For example, what happens on a data bus when new drivers are connected, perhaps before the control signals are valid?

Without a specialized connector, permanent electrical damage is possible. Consider the case where ground and a few signal pins make contact first, and one of these signals is driven High by a 5-volt CMOS driver with a 20 ohm output impedance. Until the Vcc pins make contact, this High signal will forward-bias the electrostatic discharge (ESD) protection diode and try to drive the not-as-yet-connected Vcc distribution network to a marginally High level.

The logic signal acts as a surrogate Vcc supply, but none of the signal traces and circuit elements are strong enough for that job. The current value depends on the number and the nature of the devices fed from the unpowered Vcc net. SRAM-based FPGAs may power-up sufficiently close to 3.5 volts to start the configuration process in master mode, still only powered by one or a few logic signals. As a result, the configuration will usually be aborted before it is finished. These uncontrolled activities and uncontrolled electrical overstresses are not desirable.

When Vcc and a few signals make contact before the ground is connected, a similar problem occurs. A Low signal output on the powered-up board acts as the surrogate ground for the plug-in device, with current coming in through the ESD-protection diode from the unpowered device.

The ESD-protection diodes seem to be the main cause of hot plug-in problems, but these diodes are absolutely necessary to protect CMOS inputs against high voltages. Gate oxides are now 50 to 100 Å thick, and 5 volts across a gate oxide of 50 Å means a field strength of 1,000 volts per micron — a megavolt per millimeter. Even the best silicon dioxide reaches its limits under these conditions.

Modern CMOS devices usually have two strong diodes on each input pin, one connected to ground, and one connected to the Vcc, to send excessive input charge into the supply rails. The new Xilinx XC4000XL devices do not have a diode to Vcc, but rather use a positive discharge structure to ground. This eliminates some of the hot-plug-in problems, and makes these devices immune to power-supply sequencing, which is a related but easier problem.

Summary

The normal ramping-up of Vcc in a digital system is complicated enough, with different devices coming "alive" at different voltage levels. A haphazard plug-in procedure is much worse. You should avoid hot plug-in unless the equipment is specially designed. ◆

XC4000XL Power Calculation

Almost all power consumption in Xilinx FPGAs is dynamic, the result of charging and discharging internal and external capacitance. The small exception is the static power used for internal housekeeping operations, for leakage current, and for driving external resistive loads.

The total dynamic power in XC4000XL devices is the sum of three major ingredients:

- Clock distribution power.
- Output power.
- Power used for internal logic and driving the interconnections.

The balance between these depends on the design implementation, but often the three ingredients have roughly equal magnitude.

Global Clock Distribution Power

All XC4000 Series devices use a clock distribution network that achieves short clock delay, negligible clock skew, and the lowest possible power consumption. Each global clock signal is routed to the center of the chip and then drives a horizontal "backbone." Each column of CLBs has several vertical clock distribution "Longlines," each serving the upper or lower half of a column. These Longlines are only driven when the flip-flop placement requires it, and flip-flop clock inputs are only connected to a clock line when needed. Clock power is thus minimized.

The total power for each global clock input has three ingredients:

- **A** - the power to drive the backbone.
- **B** - the discretionary power to drive each vertical half-Longline.
- **C** - the power to clock each individual flip-flop.

A and B are device-size dependent, while C is constant. Table 1 lists the values for A, B, and C , expressed in µW/MHz, with a nominal 3.3 V power supply. The power consumption varies with the square of the supply voltage, but is almost independent of temperature and of the device speed grade.

To calculate total clock power, you must know N (the number of flip-flops driven by the clock) and you must estimate V (the number of vertical half-length Longlines used for distributing the clock). A reasonable estimate is that V is the square root of N.

The total power consumed by one global clock is thus: $P = f \cdot (A + B \cdot \sqrt{N} + C \cdot N)$

For example, a 60 MHz clock driving 300 flip-flops in an XC4036XL consumes:

$60 \cdot (300 + 17 \cdot 50 + 300 \cdot 8)\mu W =$

$60 \cdot (300 + 850 + 2400)\mu W = 213$ mW

Output Power Due to Charging Capacitive Loads

The following estimates assume an internal 10 pF pin capacitance.

- One output driving a 10 pF external load:
  0.2 mW/MHz =
  0.1 mW per million transitions per second
- One output driving a 50 pF load:
  0.6 mW/MHz =
  0.3 mW per million transitions per second.

***Note**: Clock frequency can be a misleading way to measure logic activity; counting all transitions avoids this ambiguity.*

Logic and Interconnect Power

- One internal flip-flop driving nothing but its neighboring CLB:
  0.08 mW per million transitions per second.
- One internal flip-flop driving nine loads (very high fan-out):
  0.16 mW per million transitions per second.

Conclusion

This information allows you to estimate device power consumption. The fundamental difficulty is finding the toggle frequency of internal nodes, which requires you to know the statistical behavior of all system inputs to the chip, not just the clock rate. Some estimates assume that 12.5% of the internal flip-flops toggle at the clock rate. However, this is a gross oversimplification, based on the behavior of 16-bit counters. In real designs, the average activity can be significantly lower or higher than 12.5%. ◆

Table 1 -
Clock Power Consumption in µW/MHz

Device	Back-bone	per Vertical	per Flip-Flop
XC4005XL	120	19	8
XC4010XL	170	28	8
XC4013XL	200	33	8
XC4020XL	230	39	8
XC4028XL	270	44	8
XC4036XL	300	50	8
XC4044XL	330	56	8
XC4052XL	370	61	8
XC4062XL	400	67	8
XC4085XL	470	78	8

COMPONENT AVAILABILITY CHART

PINS	TYPE	CODE	XC3020A	XC3030A	XC3042A	XC3064A	XC3090A	XC3020L	XC3030L	XC3042L	XC3064L	XC3090L	XC3142L	XC3190L	XC3120A	XC3130A	XC3142A	XC3164A	XC3190A	XC3195A	XC4003E	XC4005E	XC4006E	XC4008E	XC4010E	XC4013E	XC4020E	XC4025E	XC4002XL	XC4005XL	XC4010XL	XC4013XL	XC4020XL	XC4028XL	XC4036XL	XC4044XL
44	PLASTIC LCC	PC44		◆												◆																				
	PLASTIC QFP	PQ44																																		
	PLASTIC VQFP	VQ44																																		
	CERAMIC LCC	WC44																																		
64	PLASTIC VQFP	VQ64		◆					◆							◆																				
68	PLASTIC LCC	PC68	◆	◆											◆	◆																				
	CERAMIC LCC	WC68																																		
84	PLASTIC LCC	PC84	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆				❖	◆	◆					
	CERAMIC LCC	WC84																																		
	CERAMIC PGA	PG84	◆	◆	◆										◆	◆	◆																			
100	PLASTIC PQFP	PQ100	◆	◆	◆										◆	◆	◆				◆	◆							❖	◆	◆					
	PLASTIC TQFP	TQ100														◆	◆																			
	PLASTIC VQFP	VQ100		◆	◆				◆	◆			◆			◆	◆				◆								❖	◆						
	TOP BRZ. CQFP	CB100	◆		◆										◆	◆	◆																			
120	CERAMIC PGA	PG120																			◆															
132	PLASTIC PGA	PP132			◆	◆											◆	◆																		
	CERAMIC PGA	PG132			◆	◆											◆	◆																		
144	PLASTIC TQFP	TQ144			◆	◆	◆			◆	◆	◆	◆	◆			◆	◆	◆			◆	◆							◆	◆					
	CERAMIC PGA	PG144																																		
	HI-PERF TQFP	HT144																														◆	◆			
156	CERAMIC PGA	PG156																				◆	◆													
160	HI-PERF QFP	HQ160																																◆	◆	◆
	PLASTIC PQFP	PQ160				◆	◆											◆	◆	◆		◆	◆	◆	◆	◆				◆	◆	◆	◆			
164	TOP BRZ. CQFP	CB164					◆												◆	◆		◆														
175	PLASTIC PGA	PP175					◆												◆	◆																
	CERAMIC PGA	PG175					◆												◆	◆																
176	PLASTIC TQFP	TQ176					◆					◆		◆					◆												◆					
	HI-PERF TQFP	HT176																														◆	◆			
191	CERAMIC PGA	PG191																						◆	◆											
196	TOP BRZ. CQFP	CB196																							◆											
208	PLASTIC PQFP	PQ208					◆												◆	◆		◆	◆	◆	◆	◆				◆	◆	◆	◆			
	HI-PERF QFP	HQ208																							◆	◆	◆							◆	◆	◆
223	CERAMIC PGA	PG223																		◆						◆	◆	◆								
225	PLASTIC BGA	BG225																							◆	◆										
228	TOP BRZ. CQFP	CB228																								◆		◆								
240	PLASTIC PQFP	PQ240																								◆						◆	◆			
	HI-PERF QFP	HQ240																								◆	◆	◆						◆	◆	◆
256	PLASTIC BGA	BG256																													◆	◆	◆	◆		
299	CERAMIC PGA	PG299																										◆						◆		
304	HI-PERF. QFP	HQ304																										◆						◆	◆	◆
352	PLASTIC BGA	BG352																																◆	◆	◆
411	CERAMIC PGA	PG411																																	◆	◆
432	PLASTIC BGA	BG432																																	◆	◆
475	CERAMIC PGA	PG475																																		
559	CERAMIC PGA	PG559																																		
560	PLASTIC BGA	BG560																																		

JANUARY 1998

PINS	TYPE	CODE	XC4052XL	XC4062XL	XC4085XL	XC40125XV	XC4005L	XC4010L	XC4013L	XC5202	XC5204	XC5206	XC5210	XC5215	XC6216	XC6236XL	XC6264	XC9536	XC9572	XC95108	XC95144	XC95216	XC95288	XCS05	XCS10	XCS20	XCS30	XCS40
44	PLASTIC LCC	PC44																◆	◆									
	PLASTIC QFP	PQ44																										
	PLASTIC VQFP	VQ44																◆										
	CERAMIC LCC	WC44																										
64	PLASTIC VQFP	VQ64																										
68	PLASTIC LCC	PC68																										
	CERAMIC LCC	WC68																										
84	PLASTIC LCC	PC84					◆	◆		◆	◆	◆	◆						◆	◆				❖	❖			
	CERAMIC LCC	WC84																										
	CERAMIC PGA	PG84																										
100	PLASTIC PQFP	PQ100								◆	◆	◆							◆	◆	❖							
	PLASTIC TQFP	TQ100																	◆	◆	❖							
	PLASTIC VQFP	VQ100								◆	◆	◆												❖	❖	❖	❖	
	TOP BRZ. CQFP	CB100																										
120	CERAMIC PGA	PG120																										
132	PLASTIC PGA	PP132																										
	CERAMIC PGA	PG132																										
144	PLASTIC TQFP	TQ144								◆	◆	◆	◆												❖	❖	❖	
	CERAMIC PGA	PG144																										
	HI-PERF TQFP	HT144													◆													
156	CERAMIC PGA	PG156								◆	◆																	
160	HI-PERF QFP	HQ160																										
	PLASTIC PQFP	PQ160									◆	◆	◆	◆						◆	❖	◆						
164	TOP BRZ. CQFP	CB164																										
175	PLASTIC PGA	PP175																										
	CERAMIC PGA	PG175																										
176	PLASTIC TQFP	TQ176						◆				◆	◆															
	HI-PERF TQFP	HT176																										
191	CERAMIC PGA	PG191									◆																	
196	TOP BRZ. CQFP	CB196																										
208	PLASTIC PQFP	PQ208					◆	◆	◆			◆	◆													❖	❖	❖
	HI-PERF QFP	HQ208												◆								◆	◆					
223	CERAMIC PGA	PG223											◆															
225	PLASTIC BGA	BG225							◆				◆	◆														
228	TOP BRZ. CQFP	CB228																										
240	PLASTIC PQFP	PQ240							◆				◆														❖	❖
	HI-PERF QFP	HQ240	◆	◆										◆	◆	❖	◆											
256	PLASTIC BGA	BG256																									❖	❖
299	CERAMIC PGA	PG299												◆	◆													
304	HI-PERF. QFP	HQ304	◆	◆										◆														
352	PLASTIC BGA	BG352												◆								◆	◆					
411	CERAMIC PGA	PG411	◆														◆											
432	PLASTIC BGA	BG432	◆	◆												❖												
475	CERAMIC PGA	PG475		◆																								
559	CERAMIC PGA	PG559			◆	❖																						
560	PLASTIC BGA	BG560	◆	◆	◆	❖											◆											

◆ = Product currently shipping or planned

❖ = New since last issue of *XCell*

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