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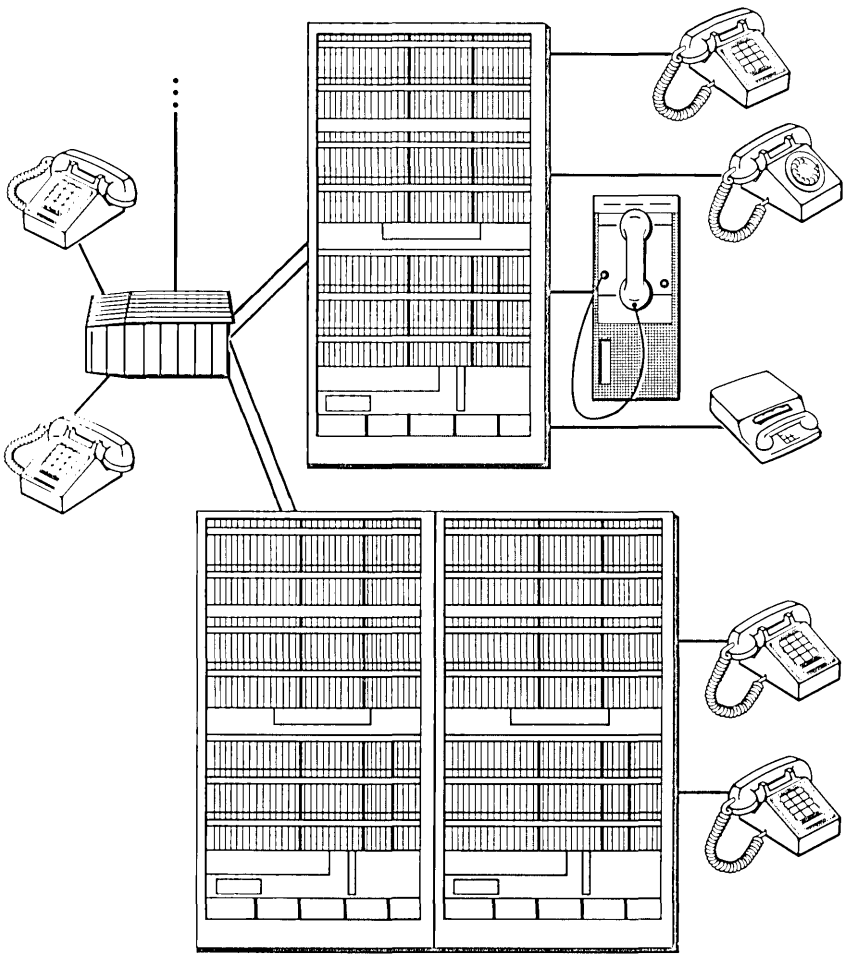

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NO. 10A REMOTE SWITCHING SYSTEM

R. W. Downing, *Guest Editor*

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No. 10A Remote Switching System:

System Overview

By N. B. ABBOTT, K. J. S. CHADHA, D. P. SMITH, and T. F. WICKHAM

(Manuscript received May 28, 1980)

This paper gives an overview of the No. 10A Remote Switching System, including background planning studies, system objectives, and information on the major hardware and software elements of the system.

I. INTRODUCTION

This paper is an overview of the No. 10A Remote Switching System (10A RSS), including some background, results of earlier planning studies, system objectives, and information on the major hardware and software elements of the system. Companion papers in this issue of *The Bell System Technical Journal* will discuss some of these elements in greater detail.

The major components of the 10A RSS include a host Electronic Switching System (ESS), one or more 10A RSS frames and data links for communication between the host and remote site(s). Figure 1 details this arrangement. At this time, the host function has been developed for the Western Electric No. 1 ESS machines, and work is now in progress to develop the host capability for the Western Electric No. 1A and No. 2B ESS machines. The data link used for the No. 1/1A ESS-RSS communication function is a new design utilizing an intelligent peripheral unit controller (PUC-DL) which can interface with up to 16 data links. The 10A RSS data link communication makes use of the X.25 protocol. The 10A RSS basic frame can serve up to 1024 lines. A companion frame may be added to allow up to 2048 lines to be served by a single RSS entity. The design is such that the basic element of

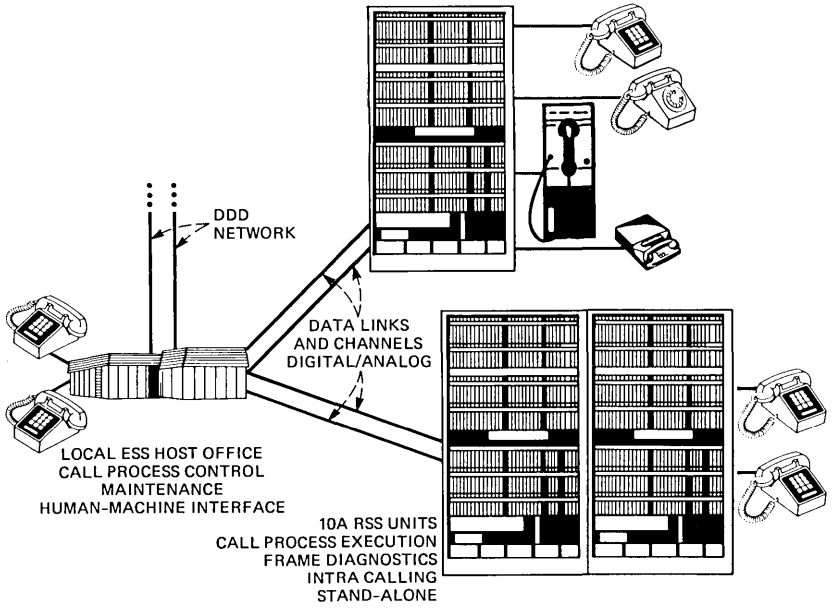

Fig. 1—No. 10A RSS for ESS.

growth can be as small as eight lines. Voice and control communications between the remote and the host can be made over either digital or analog carrier facilities, and the range may be as far as 280 miles, depending primarily on the specific type of transmission facility.

In the event of total carrier system or data link outage, the 10A RSS is arranged to automatically transfer to a stand-alone mode of operation which provides basic telephone service between stations connected to that RSS unit. In the stand-alone mode, special provisions can be made to handle emergency types of traffic such as "911."

All major units of the 10A RSS are duplicated, and a continuous dialogue is exchanged between the host and remote site concerning the overall health of the system. The basic system philosophy is that the remote unit is a complete slave to the host and, in general, merely reports events to the host and then receives a stream of explicit orders from the host concerning that event. All maintenance procedures must be controlled from the host. Initiation of diagnostics and other functions may be further remoted to a Switching Control Center (SCC).

II. BACKGROUND

With the evolution in electronic technology currently in progress, it was evident that intelligent remotely controlled devices could be

brought into the central office switching environment. Early work in this area tended toward the design of systems primarily as pair gain devices. That is, electronic systems that allow the extension of the central office to remote areas by means of substituting electronics for wire pairs. Considerable economic advantages evolved from this approach. As investigations in this area progressed, it was recognized that the merging together of an intelligent (although subordinate) remote terminal with an intelligent controlling host would create a new type of switching vehicle with vast potential for serving a myriad of Bell System switching needs. A system which could effectively and economically remote large portions of its network over large distances could rapidly be deployed over major segments of the Bell System network. This would provide the Bell System with the opportunity to bring the advantages of ESS stored program control with its rich feature content into areas that previously could not economically justify the installation of an ESS.

The era of electronic switching began with the introduction of the No. 1 ESS into commercial service in 1965.[1] Since then, there has been a continual evolution of electronic switching systems, designed for particular segments of the switching environment of the Bell System. For example, the No. 1 ESS is a large machine and is best suited for metropolitan and large city environments. To meet the needs of the suburban and rural market, the No. 2/2B ESS and No. 3 ESS machines, respectively, have been created.[2] In spite of this activity, there remains a large segment of Bell System central offices that until the introduction of the 10A RSS could not justify the introduction of electronic switching technology. These offices are primarily in the size range of less than 1500 lines. With the 10A RSS, it is possible to economically provide service to these areas, thereby making available the specializing services, improved maintenance, and the inherent reliability of electronic switching.

III. PRELIMINARY PLANNING STUDIES

In the early design stages of the 10A RSS, the pressing need for a small switching system to serve the multitude of very small Community Dial Offices (CDOs) in the Bell System was very evident. Surveys of operating telephone companies in 1970 and 1971 by Bell Laboratories had identified many of the characteristics and new feature requirements of small CDOs of fewer than 1000 lines in size.

The concept of remote switching had been investigated before for other needs, for example, switching of wideband data services. Until the mid-1970s, there had been no economically or technically feasible solutions to many of the challenges presented by remote switching,

such as reliability. However, in the exploratory design stages of the 10A RSS, advancing LSI and microprocessor technology suggested possible solutions to many of these questions.

In 1975, Bell Laboratories began an initial market concept testing study in conjunction with the New York Telephone Company in the Buffalo area. The purpose of this study was to explore the economic potential for remote switching in the replacement and consolidation of small central offices, and to identify other potential applications of remote switching. Besides CDO modernization, this early study pointed out some other promising possibilities. Use of a low start-up cost switch would permit introduction of electronic switching technology to new wire centers at smaller line sizes. The use of electronics in the outside loop plant to reduce the number of physical cable pairs to the central office is called pair gain, and has been used traditionally in long, slowly growing, small cross-section feeder routes in rural areas. The Buffalo study pointed out a need for a larger pair gain system to be deployed in suburban areas when, for example, a new housing development, apartment complex or shopping center threatened exhaust of outside plant facilities. Later studies have confirmed the need for large pair gain systems.

The Buffalo study also supported the collocation of a remote switch in an older electromechanical office to provide ESS features to customers willing to take a number change, or to postpone an equipment or a building growth addition. However, further studies of this application indicated that it is only marginally attractive, largely due to the costs of the split trunk groups and administrative overhead.

Subsequently, systems engineering organizations conducted extensive studies of remote switching which validated economics, developed planning guidelines, and contributed to the decisions concerning host development, carrier compatibility, distance constraints and features. These planning studies, and in particular, the studies relating to the impact of the 10A RSS in the modernization of the Bell System network are described in Refs. 3 and 4.

IV. SYSTEM REQUIREMENTS AND OBJECTIVES

4.1 Size

Based on the primary market objective of CDO modernization, the 10A RSS design was optimized for the 200- to 1000-line range. The initial frame can terminate 1024 equipped lines, and a second frame can be added for a maximum size of 2048 lines in central office applications.

A major advantage of the 10A RSS is its small physical size. A single 7- by 3-ft, 3-in. frame contains all of the switching equipment needed

for 1024 lines, plus the necessary transmission facility interfaces to the host ESS when T1 carrier is used. The only major equipment items not included in this frame are the −48 volt central office battery plant, plus its commercial ac power interface, the main distributing frame, and any miscellaneous circuits.

In CDO replacements where floor space is limited, the 10A RSS may prevent costly building additions because of its compact size. A dramatic comparison of a 1000-line 10A RSS with the equivalent step-by-step switch it would replace is illustrated in Fig. 2. Even where floor space is not a problem, the achievement of greater circuit packing density by minimizing size and power requirements permits significant savings in system cost and energy consumption—an important factor in the tight economics of the CDO market. Of course, in pair gain applications small size contributes to unobtrusiveness, as well as economy.

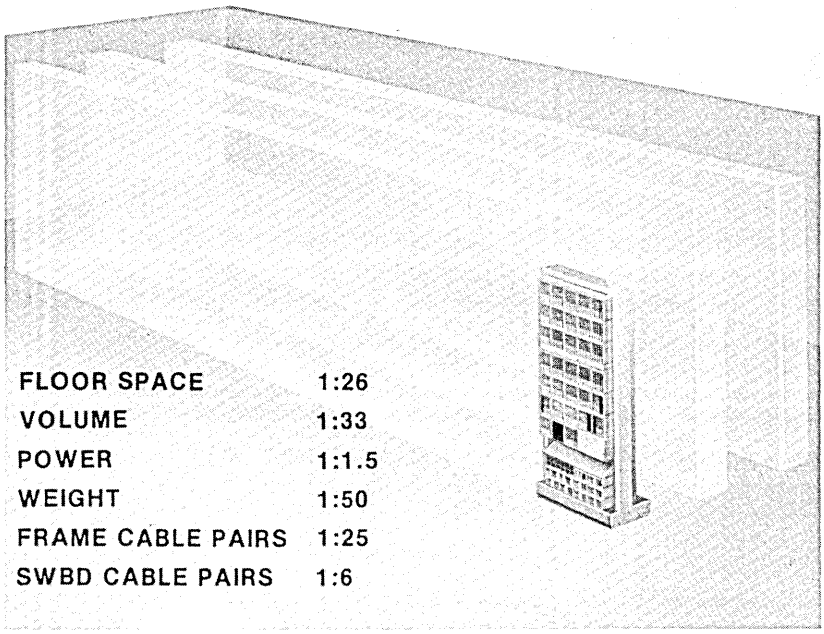

Fig. 2—Remote switching system versus step-by-step comparison (1,000-line offices).

4.2 Cost

The major cost objective for the 10A RSS was that it be competitive with step-by-step equipment life cycle growth costs in the small CDO replacements that are its primary target market. To achieve this objective, a low startup cost was essential. Most of the cost of the system is invested in the line interface circuitry. Line interfaces are packaged with eight on a circuit board which also contains one stage of the switching network. Thus, small growth increments of only eight lines at a time are possible.

The basic concept of remote switching is dependent upon sharing the resources of the controlling host. Since the 10A RSS shares these resources (e.g., service circuits and access to the toll network), a smaller investment is required at the remote terminal in processor intelligence, equipment and trunk groups, than it would for an independent entity.

All of these factors work together to keep costs within the economic framework dictated primarily by the cost profile of CDO modernization.

4.3 Features

The general philosophy adopted in defining the 10A RSS feature complement was to extend all of the ESS host line features to RSS lines, except those with no apparent applicability in identified target markets. The 10A RSS provides a full range of local central office features including: *TOUCH-TONE** calling, automatic number identification, individual and multiparty service, public telephone service operation, and the administrative and maintenance aids normally associated with ESS, such as automatic traffic measurements, billing and system diagnostics. Vertical services that are offered by the host ESS, such as Custom Calling, are also available to 10A RSS lines.

A single ESS host can control multiple remote units (up to 31 RSS units on a No. 1 ESS) at distances of up to 75 to 280 miles, depending upon the type of transmission facilities used. A 10A RSS and its host may be assigned the same or different NXX (office) codes. They may be in the same or in different Numbering Plan Areas.

An important feature of the 10A RSS in central office applications is its stand-alone operation in the event of data or voice transmission isolation from the host ESS. If the duplicated data link between host and remote unit fails, because of a cable cut or an equipment problem, the microprocessor in the remote unit will be able to continue processing intra-RSS calls. This stand-alone mode of operation provides only a very basic type of service. Vertical services, billing, maintenance,

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traffic measurements, and all other functions normally performed by the host ESS are not available in this mode of operation. Calls to directory numbers not served by the 10A RSS are connected to reorder tone source or an optional recorded announcement, although limited special routing may be provided at the option of the telephone company for a few emergency directory numbers.

Another valuable 10A RSS feature in central office applications is its compatibility with existing main distributing frames, battery, and power plant. This, combined with small system size, is particularly important where building space is cramped.

The set of features provided by the 10A RSS is complete enough to make it attractive in a variety of applications, and yet streamlined enough to enable it to be competitive in its target markets.

4.4 Performance

The 10A RSS has a network capacity of approximately 6000 total originating, plus terminating (O + T), Average Busy Season (ABS) CCS (hundred call seconds). There are up to 120 channels provided to the host from each 1024-line frame. Two of these from the first equipped frame are used for the data links of the system, but the rest are free for intersystem traffic and intra-RSS call setup. Channels will typically carry 25 to 30 CCS and are terminated as high usage host line appearances, like private branch exchange trunks.

The 10A RSS has a two-stage, folded, full access, 4:1 concentrated switching network, such that each line can be connected to each and every channel within a 1024-line frame. The 64 by 16 inlet switch is liberally engineered so that any 16 of the 64-line appearances can simultaneously access any of the 16 outputs of the switch. Because of this richness of the network, a relatively high concentration ratio is possible; for example, with a traffic load of 3 CCS/line and a fairly low intra-RSS calling rate of 10 percent, a concentration approaching 10:1 (lines:channels) can be attained. Where the intra-RSS calling rate is higher, this concentration can be much greater, because intra-RSS calls only use channels to the host during call setup—a clear advantage in CDO applications where intraoffice traffic is typically high. Where a large proportion of the lines in a system have fairly high traffic (4 to 7 CCS/line), then the concentration of the inlet switch can be reduced by deloading the line appearance on the 10A RSS.

The 10A RSS has an engineered processing capacity of about 6000 O + T busy-hour calls for a maximum size two-frame system. A 10A RSS also places an additional call processing load on the host ESS, since each 10A RSS call will require between 100 and 200 percent more host processor real time than an equivalent call in the No. 1 ESS host.

4.4.1 Grade of service

The grade of service objective of the 10A RSS design is to provide transmission performance comparable to that of its host ESS from the point of view of the customer. The RSS is considered to be an extension of the host ESS line appearances into a remote serving area, and so it does not have a unique network office class in the toll hierarchy, but is part of the class 5 office. Therefore, there is no additional loss allocation for the host-to-remote voice links. By the introduction of new matching networks and sophisticated automatic loop measurement techniques, the 10A RSS design is able to utilize 0 dB links to the host, and meets or exceeds its transmission objective.

Since 10A RSS dial tone is normally provided by the host ESS, the remote unit network and the channels have been engineered to provide a combined probability of blocking that will result in the same effective dial tone grade of service for 10A RSS customers as those served directly by the host ESS. This is true for all connections requiring access to the host network. To further ensure good performance, an extensive network retry strategy has been implemented for many 10A RSS connections through the host network.

4.4.2 Stand-alone performance

In the stand-alone mode of operation, the 10A RSS traffic handling will be reduced to about two-thirds of its normal call processing capacity. Thus, an RSS operating in this mode will have a capacity of approximately 4000 busy-hour calls.

In transitions to and from the stand-alone state, the 10A RSS minimizes customer annoyance by maintaining stable intra-RSS calls in a talking state.

4.5 Reliability and maintenance objectives

The overall maintenance objective for the 10A RSS is twofold: (*i*) to provide ESS quality, reliability, and maintenance features, and (*ii*) to keep maintenance procedures as similar as possible to existing telephone company procedures in all phases of 10A RSS maintenance, including lines, carrier channels, and data links, as well as the system itself.

4.5.1 Reliability objectives

The reliability objectives of the 10A RSS are the same as that of its host ESS.[1] To enhance its reliability, the 10A RSS design includes hardware redundancy, automatic and regularly scheduled or manually initiated diagnostics, automatic error recovery, and internal error analysis of failures resulting in automatic removal from service of defective units. All essential components (e.g., microprocessor, mem-

ory, data link) are duplicated. All other components which affect more than 64 lines are replicated. An automatic switch to off-line duplicated circuits is made when trouble occurs. The stand-alone operation is invoked when both data links fail, and when the host does not respond to a remote terminal prompt within a specified time interval.

4.5.2 Maintenance objectives

Responsibility for maintenance of a 10A RSS is centralized with the switching craft responsible for its host ESS, who may be located at the host office or at an SCC. The 10A RSS teletypewriter messages, alarms, and SCC interface are provided through its host ESS. Although it shares the resources of the host, the RSS is recognized as an individual entity when failures occur.

The following features are provided by 10A RSS for effective maintenance:

(*i*) Built in diagnostics to enable localization of troubles and permit dispatch of the appropriate craft.

(*ii*) Craft/machine interfaces in the form of the host maintenance teletypewriter, a maintenance panel at the remote terminal, and alarm circuits.

(*iii*) Diagnostics to test and identify faulty circuit packs which are replaceable entities.

(*iv*) T Carrier Administration System interfaces at the host ESS.

(*v*) Automatic line insulation testing of customer loops.

(*vi*) Remote loop testing capability via the Remote Test System (RTS) at the Local Test Desk (LTD).

(*vii*) Manual and automatic channel testing capability, including compatibility with Centralized Automatic Reporting On Trunks (CAROT).

Ease, consistency, and centralization of maintenance operations and procedures will be especially important in the remote, unstaffed, small offices and suburban loop plant applications that are the primary target markets for the 10A RSS.

V. INSTALLATION

The installation of a 10A RSS requires four major elements:

(*i*) Proper generic program with the 10A RSS feature package loaded in the host ESS office.

(*ii*) Installation of a PUC-DL frame which can support up to 16 data links. Two data links are required per 10A RSS unit.

(*iii*) Carrier system between the remote terminal and the host.

(*iv*) Remote unit equipped as required.

The 10A RSS host interface has been designed to allow it to be easily installed in a working host environment with no service affecting penalties on the existing system. The 10A RSS frame has been com-

pletely tested at the factory by emulating the host interface and performing all possible diagnostic tests. In addition, all circuit packs have been burned in and the entire frame subjected to a strenuous heat and power cycle requirement. All cabling to the 10A RSS frame is connectorized, including the subscriber tip and ring pairs. As a result, the actual installation interval for a 10A RSS unit is short, since all cabling can be performed before the arrival of the 10A RSS frame on site. The frame is then powered up, the data links attached, and the extensive data link diagnostics are then exercised to verify the communication link.

Once the data links are operational, the remaining cabling can be plugged in and the diagnostic programs for all the remote terminal hardware executed to ensure that the hardware is still operational and has not been damaged in transit. Once the hardware is verified, translation data to assign the remote terminal equipment can be entered in on the host service order teletypewriter channel and the system prepared to run the board-to-board verification and final acceptance tests.

Cutover of the new system is routine since the existing hosts provide very sophisticated mechanisms for transferring the system from a precut to a post-cut state.

VI. MAINTENANCE

Remote unit maintenance is scheduled and performed at the remote end. There are over 20 circuit board types. A diagnostic program for each board type is resident at the remote terminal. Diagnostics are scheduled routinely and those that fail are reported to the host. No circuits are taken out of service as a result of these routine diagnostics. The host also has the capability of manually requesting specific diagnostics and also of removing equipment from service. The only exception to this host control is the microprocessor complex. Since it takes time to report a failure to the host and to have the host respond to this failure, an error in the microprocessor complex (e.g., a memory parity error) can cause an immediate switch to the duplicate processsor complex. This remote terminal action is justified by the fact that the delay necessary for host action could cause a degradation in telephone service. In the event of an erratic processor complex causing frequent switching, the host has a mechanism to manually override the remote terminal's action in this area.

In addition to the routinely scheduled diagnostics, the remote terminal performs an extensive set of per-call tests to verify proper operation of the system. These tests include the usual verification of network path continuity and extend to proper operation of various control functions, such as verifying that the High Level Service Circuits

(HLSCs) are generating the proper ring polarity. Failure of these tests generally results in immediate notification to the host so that proper failure actions may be initiated for the call. In addition, the remote terminal retains the identification of the failing circuit(s) and performs peer group analysis on that circuit with a past history record of other circuits of the same type. If the results of this analysis indicate that this particular circuit is performing poorly, a message is sent to the host indicating this poor performance. If the internal automatic maintenance limits have not been exceeded, the circuit is removed from service and the craft people are informed of this removal action. If the automatic limits have been reached, the craft force is alerted and manual action by a craft person will be required to remove the faulty circuit from service.

The transmission objectives for remote switching require that the host-to-remote channels must be maintained at a 0-dB loss. To ensure that this objective is met, a miniresponder is located at the remote terminal. This miniresponder provides the host channel maintenance programs with the ability to measure all the required transmission items, such as ac continuity, gain slope, 1000-Hz loss, 3000-Hz loss, etc. Channel diagnostics are run routinely from the host and can be accessed externally by the CAROT system. In addition, channel diagnostics can be requested manually [from a maintenance teletypewriter (TTY) or a test panel] or run whenever the system detects a fault and the RSS channel is suspect. Even though RSS channels appear on the line side of the ESS network, they receive the same general maintenance treatment as trunks. They can be removed from service automatically up to a predetermined maintenance limit which can only be overridden by manual action.

The major human-machine interface for maintenance of the 10A RSS is the maintenance teletypewriter of the host ESS. This philosophy falls in precisely with the general move of ESS-type maintenance activities into a centralized SCC, where skilled craft people can be effectively pooled to share their expertise over many switching machines and even more remote switching units.

When a trouble has been isolated to a 10A RSS unit, a craft person still must be dispatched to the remote site to make the necessary repairs. To facilitate this operation and to reduce the skill level required of the person making the repair, a maintenance panel is provided at the remote unit (Fig. 3). This panel is under the control of the host, and is not active unless the host issues the proper commands. The panel is precharged via a software buffer with a list of suspected faulty circuit packs. The craft person can only request a local diagnostic on those particular circuit packs. A flowchart is provided on the panel indicating the allowable steps a craft person may perform and their

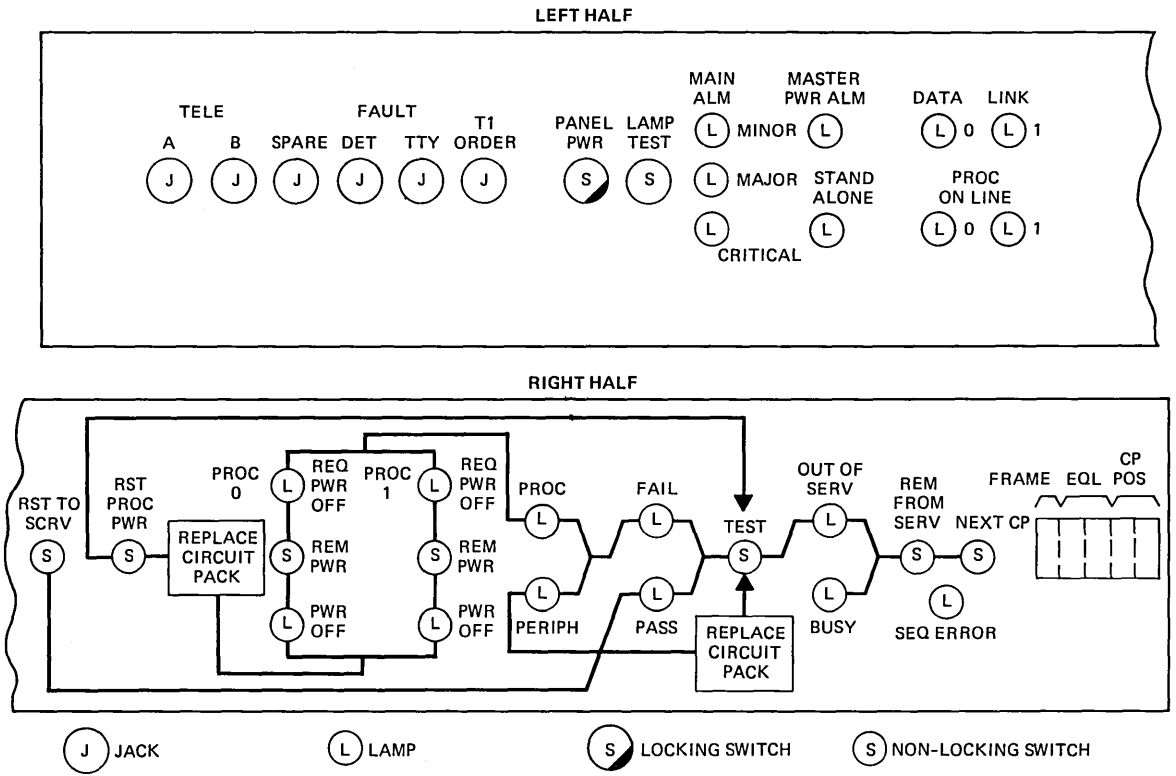

Fig. 3—Remote maintenance panel.

particular order. Any deviation will cause a sequence error and a reversion back to the first step. This panel operation will allow a relatively unskilled individual to successfully verify suspect circuit packs, replace those identified as faulty, while effective control and monitoring is maintained at the host or associated SCC.

VII. HARDWARE DESIGN PLAN

The hardware design of the 10A RSS is a fundamental departure from the equipment and techniques used in previous ESSs designed for local class 5 service. The 10A RSS utilizes a low-level electronic switching network, multifunction programmable high-level signaling circuits, LSI microprocessor control techniques, and ultraviolet (UV) erasable memory technology to implement the functions of the local central office. In addition, transmission equipment and switching equipment have been integrated into the same physical frame eliminating the need for relay technology signaling protocols and redundant circuit functions. The block diagram of Fig. 4 illustrates the major elements of the 10A RSS remote terminal.

The rationale behind these design decisions is the fundamental system objective of providing economical service at small (<2000) line sizes while simplifying both the initial engineering and subsequent growth of the system. A basic characteristic of any low-level electronic network is the concentration of equipment cost in the line interface circuit. Optimal use of silicon technology and dense packaging techniques made it possible to package part of the switching network, battery feed and supervision, and metallic access for ringing and testing for eight customer lines on a single plug-in circuit pack. This circuit pack is the basic growth element of the remote terminal, and it can be equipped as desired, thus deferring major equipment expense until the equipment is actually required.

Another important feature of the remote terminal design is the use of multifunction HLSCs, instead of engineered special-purpose circuits. In a small office environment such as that which the 10A RSS is designed to serve, the small usage groups of a particular type of circuit make it more economical to use a multipurpose circuit, even though the cost of such a multipurpose circuit may be higher than a simple ringing circuit. An additional benefit of this design approach is the elimination of service circuit engineering since the multifunction circuits are always provided in a fixed ratio depending on the number of equipped lines.

The size of the control program [200 kilobytes (K)] made it difficult and time consuming to back up the program store at the host and "pump-up" random access memory (RAM) at the remote unit in the event of loss at the remote. Use of UV memory technology at the

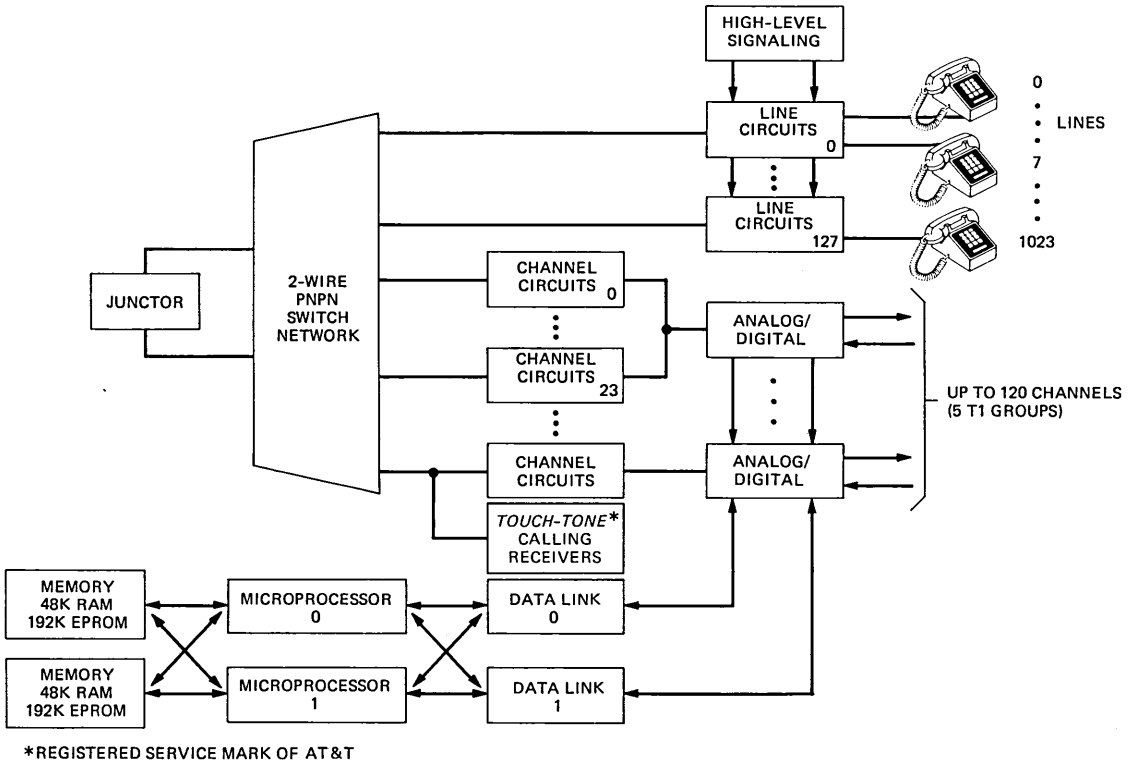

Fig. 4—No. 10A RSS remote terminal hardware.

remote solves these system problems and is expected to be more economical than read-only memory (ROM) memory technology, as long as the program change activity exceeds two changes per year. Use of the microprocessor controller also makes practical major system feature enhancements, such as the ability to handle intra-RSS calls in the remote unit in the event of total data link failure.

Finally, integration of transmission equipment into the design eliminates duplication of function and makes possible substantial equipment savings in both size and cost. The existence of an electronic switching network in 10A RSS requires that most of the functions associated with the channel unit of conventional transmission equipment must be performed on the 10A RSS line interface circuit. This simplified the channel unit design and allowed for compact physical design, an important criteria in the overall 10A RSS objectives. In the case where T1 links connect the host and remote, the functional equivalent of five D-type channel banks have been integrated into the 10A RSS equipment. In the event of interface with N carrier analog equipment, the functional equivalent of the F-type signaling equipment is integrated into the 10A RSS frame.

VIII. SWITCHING NETWORKS

As indicated in Fig. 4, the voice switching network in the 10A RSS is a two-wire space division network which utilizes semiconductor PNPN crosspoints. The crosspoint device itself is an integrated 4 by 8 array of PNPN devices packaged in an 18-pin dip. The low cost and small size of this integrated device makes it practical to design a switching network which utilizes large nonblocking switches in place of conventional multistage switches of similar inlet/outlet capability. For example, the inlet concentrator switch in RSS is a 64 by 16 full-access single-stage switch. The inlet concentrator switch used in No. 2 ESS is also a 64 by 16 switch; however, it is a two-stage switch and is not a full access (nonblocking) switch. The advantage of the full-access switch in the 10A RSS application is the elimination of load balancing within a concentrator group and somewhat higher traffic capability per terminal.

The voice switching network topology in the 10A RSS is a folded, two-stage switch which grows in three basic preengineered increments. For the smallest systems (512 lines), the second stage switch is partially equipped as a 16 by 16 matrix as illustrated in Fig. 5. The 128 junctor circuits illustrated in Fig. 5 are preengineered and packaged on the same circuit packs as the 16 by 16 switch and are never rearranged during subsequent growth. When the number of lines exceeds 512 and/or the traffic load exceeds 1900 CCS, a second group of circuit packs are equipped in the second stage of the switch which build out the 16 by

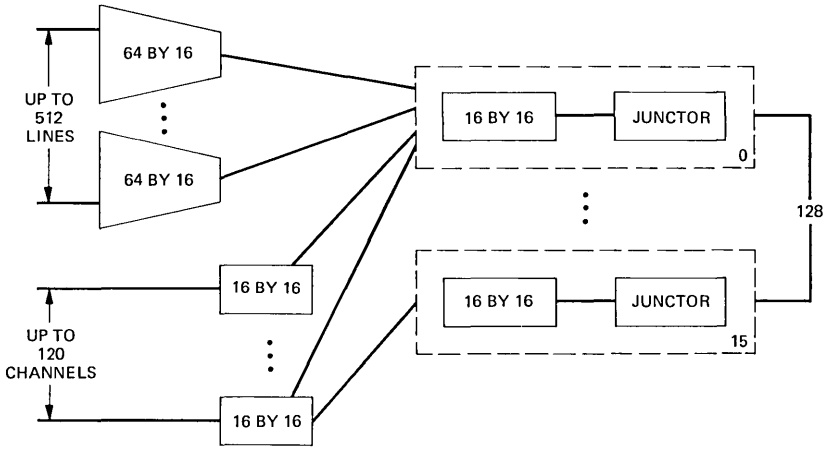

Fig. 5—No. 10A RSS switching network, 0 to 512 lines.

16 switch to a 24 by 24 matrix and add additional preengineered junctors as illustrated in Fig. 6. The final growth phase of the remote terminal involves the addition of a second bay of equipment for up to 2048 lines with interconnection established through reserved junctors when the number of lines served exceeds 1024 and/or the traffic load exceeds 4000 CCS. The low cost and highly integrated nature of the network fabric and junctor circuits makes it possible to preengineer and simplify equipment growth in this manner without substantial cost penalty.

Since the PNPN network carries only low-level voice signals, an auxiliary metallic network must be provided to handle high-level signals such as ringing (88 Vrms) and coin signals. The traffic requirements of this signaling network are such that a continuous path to a high-level service circuit is not required for more than 2 seconds during each 6-second period of time (assuming that loop supervision during the silent 4 seconds of ringing can be provided from the line interface circuit). This signaling network must also provide a path to the loop for occasional continuous line testing purposes without denying service to other nonaffected customers. These operational requirements are met by the topology of the signaling network illustrated in Fig. 7. The HLSCs indicated are reconfigured during each 2-second interval to meet the requirements of a particular loop. For example, the same HLSC may be supplying ordinary bridged ringing during a particular 2-second interval and may be reprogrammed to provide a coin collect function during the next 2-second interval. The universal nature of these high-level signaling circuits makes it possible to preengineer them without regard to the nature of the particular mix of coin, two-party, and

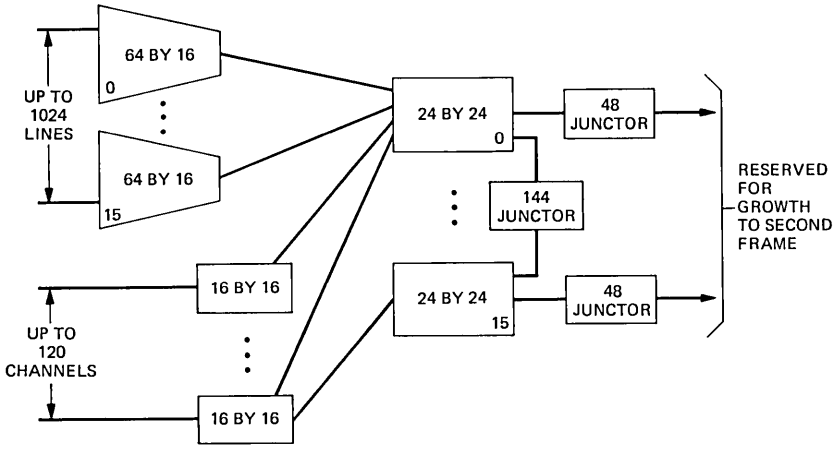

Fig. 6—No. 10A RSS switching network, 512 to 1024 lines.

multiparty lines in a particular group. The circuit design details of both the low-level voice and high-level signaling networks are discussed in the companion article on "Peripheral Systems Architecture and Circuit Design."

IX. LINE INTERFACE

Since the switching network fabric in the 10A RSS is a low-level switch, a line interface circuit is required for each customer line. This circuit isolates the low-level network from high-level signals which may be present on the customer loop, provides battery to the station

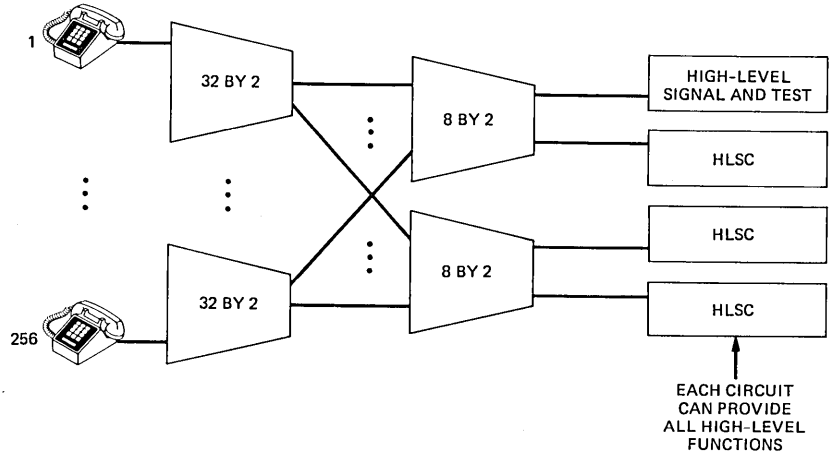

Fig. 7—High-level service circuit network.

set, supervises the loop for origination and switchhook status, and provides high-level switching for ringing and testing functions. The line interface circuits for eight customer lines are packaged on a single circuit pack, along with the first stage switch of the low-level switching network, and this plug-in forms the basic building block for incremental system growth.

An important key to packaging eight line interface circuits on an economical circuit pack is the reduction of heat dissipation both during the scanning for service request and the active talking state of the line. Equally important is the reduction in size of components traditionally used to provide the battery feed and high-level access functions. Important from the long-term operational aspects of the switch is the minimization of energy costs. For these reasons, a new technique has been developed which utilizes a small (1.5 watt) dc-to-dc power converter per customer loop to provide battery and to monitor the customer loop. This efficient converter never dissipates more than 0.8 watts of internal circuit heat at any customer loop length and saves 30 percent of the average busy-hour battery power required for this function over that which would be required if conventional techniques were used. The packaged circuit, including a small ferrite core pulse transformer, switching transistor, and control integrated circuit, is less than half the size of a conventional circuit which performs the same functions.

Additional circuit details are described in the companion article on "Peripheral Systems Architecture and Circuit Design" and in Ref. 5.

X. TRANSMISSION INTERFACE

The basic 10A RSS transmission plan differs from that of previous class 5 offices in that system economics require the RSS remote terminal to terminate on an existing class 5 switch. Maintenance of grade-of-service objectives for all Bell System loops (0 to 1600 ohms) thus implies that no loss can be allocated to the remote terminal or the transmission facilities which connect it to the host. This constraint implies that the actual transmission facility must run with a small amount of gain as measured from channel termination to channel termination. To maintain acceptable singing margin performance over this 0-dB link in the environment of service to both loaded and nonloaded loops on the 10A RSS system, special terminations must be provided at the 2-to-4 wire hybrid circuits depending on whether or not the customer loop is loaded or nonloaded. In the 10A RSS, the determination of the loaded/nonloaded status of the loop is done automatically by a special-purpose circuit [Electronic Loop Segregator (ELS)], while the customer loop is on-hook. The result of this measurement is stored in system memory, and this information is used to pick

the proper termination when this loop is involved in a connection to the host over the transmission facility. Additional information regarding the transmission interface is available in the companion article on "System Maintenance."

The overall system cost of implementing this function is minimized by concentrating the 2-to-4 wire circuits and the special hybrid termination function behind the two-wire network in the channel circuits as illustrated in Fig. 4.

It is also significant that the existence of a low-level switching network and line interface circuit in 10A RSS implies that most of the functions usually performed in a trunk circuit on a transmission facility are not required when interfacing with a 10A RSS. The functions which are required in a channel circuit are low-level operations, such as 2-to-4 wire conversion and A/D conversion. These functions can be economically packaged on the same large circuit packs used to package the other equipment in RSS. By taking advantage of this fact, the 10A RSS greatly reduces the amount of equipment required to interface with digital carrier or analog carrier facilities.

XI. CONTROL

The control techniques and duplication architecture of 10A RSS also represent a significant departure from "duplicated matching" and "self-checking" systems previously used in ESS applications. The 10A RSS microprocessors normally operate in a "dual simplex" mode where one processor is in control and is executing instructions in a mode where all memory write operations are executed both in the on-line and in the off-line store (double store write mode). The other microprocessor is in an inactive hold state during normal system operation and is not executing instructions. Error detection circuits and program sanity checks monitor the operation of the on-line processor. In the event that an error is detected, depending on its severity, control is initiated in the off-line mate processor and it becomes the on-line processor. The coupling between the microprocessors which is used to determine the on-line off-line status of the control complex is configured such that several "mutual consent" conditions are required. These conditions are intended to prevent a hardware fault from locking both microprocessors offline or both online.

The small physical size of 10A RSS makes it possible to utilize a dc-coupled parallel access control bus to control peripheral circuits on the frame. Associated with each microprocessor controller is a group of up to 32 fanout boards which serve as interface and control access to the peripheral circuit packs as illustrated in Fig. 8. Control signals from the duplicated fanout boards are OR-ed in the backplane before reaching the unduplicated peripheral circuits. Since final gate failures

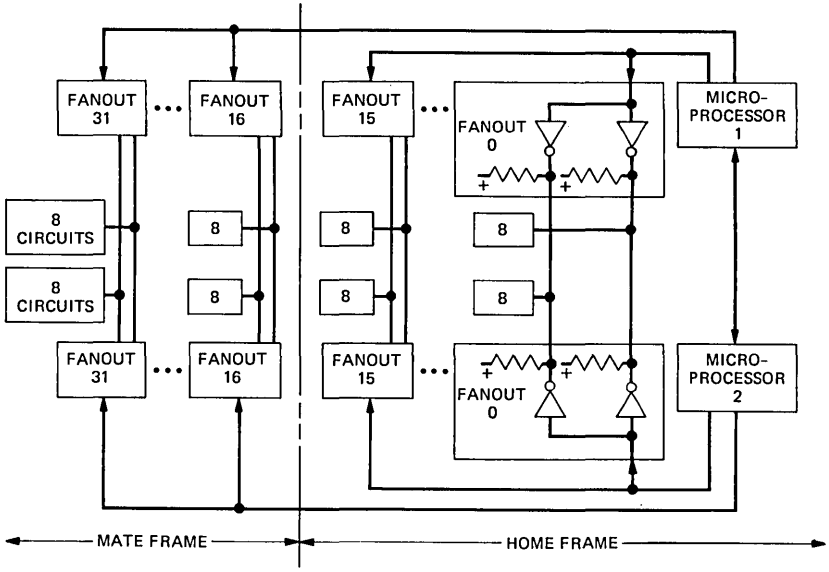

Fig. 8—No. 10A RSS control.

in this arrangement can affect both controllers' access to the affected peripheral circuit group, the number and functions of each circuit type in a peripheral control group must be carefully designed. In the 10A RSS, no more than eight circuit packs share a particular control signal in the backplane. The control assignments are arranged such that no more than 64 lines, 32 junctors, 24 channels, or 4 HLSCs can be affected by such control faults.

Peripheral circuit operations are handled in the microcontroller as memory read or write operations in a dedicated portion of the microprocessor address space. Read or write operations in this dedicated address space are decoded as special operations and sufficient "wait" states are generated in the controller to allow for a basic 6-μs peripheral read or write operation. In a peripheral read operation, data are returned from all eight circuit packs in a peripheral group in a single peripheral cycle. During a peripheral write operation, three of the peripheral address bits are decoded to select only one of the eight circuit packs in a control group. The effect of this additional decoding is the operation of a single control point specified by a unique 16-bit address. This control architecture minimizes the real-time burden of the numerous periodic scanning operations because 8-bit read operations are possible. It also minimizes the program data manipulation complexity of dealing with single-bit control operations by providing a unique address per control bit.

A final feature of the 10A RSS peripheral control is the analog/digital (A/D) nature of the data between peripheral circuit and fanout board. Certain network maintenance and scanner levels are passed from the peripheral circuit packs on the data bus as analog voltages between 0 and 5 volts. A programmable A/D converter provides an adjustable level to the data comparators on the fanout board. If the analog data exceeds the level of the previously programmed threshhold, the result of the peripheral read operation is a logic "1" on that data bit at the processor; otherwise the result is a logic "0". This feature of the design allows powerful hardware level checking at minimal system cost with the added flexibility of programmable level changes in the event of future hardware design changes.

XII. NO. 10A RSS INTERCONNECTION

A 10A RSS system occupies a position in the switching hierarchy as an extension of a class 5 or local office. This is illustrated in Fig. 9. A 10A RSS unit is interconnected to the Class 5 via two distinct facilities. These are data links for signaling and control, and channels for voice connections. As previously mentioned, either digital or analog carrier facilities, or a combination of digital and analog facilities, may be used.

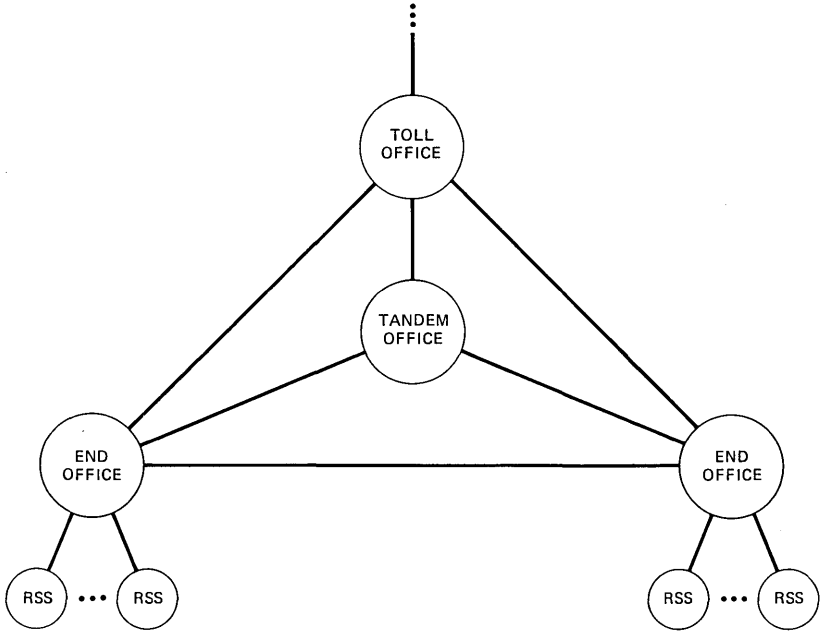

Fig. 9—Position in switching hierarchy.

A 10A RSS can be connected to one and only one host ESS, and a multiple number of RSSs can be served by an ESS.

The ESS provides the DDD network interface for both the incoming calls to, and outgoing calls from, an RSS unit. The ESS also provides the billing interface [be it Local Automatic Message Accounting (LAMA) or Centralized AMA (CAMA)], SCC interface, and the Engineering and Administrative Data Acquisition System (EADAS) interface.

High-level call control is provided by the host ESS over data links to a 10A RSS. A 10A RSS operates as an intelligent switching concentrator controlled remotely by an ESS.

An up-to-date database for each 10A RSS served by an ESS is kept in the host ESS. An abbreviated copy of this also resides in the 10A RSS. When the telephone company personnel modify this database in the host ESS (e.g., to add a RSS line), using ESS administration programs, ESS updates not only its database but also, in real time, the database residing in the affected 10A RSS. The telephone numbers for RSS lines are assigned from the office codes of the host ESS.

From a telephone company's point of view, a host ESS thus serves as a switching node in the DDD network for its subtending remote units. Thus, the introduction of 10A RSS effectively reduces the switching nodes in the network by either eliminating the existing nodes by replacing the CDO, or by delaying the introduction of future nodes when used in a pair-gain application.

XIII. NO. 1/1A HOST DATA LINK SYSTEM

Figure 10 illustrates the data link interconnection between the 10A RSS and its host ESS. The data link system's interconnection with the ESS is of the traditional nature. It is connected to the ESS via the peripheral unit bus system and treated as another ESS peripheral. The major difference between this data link system and any other periph-

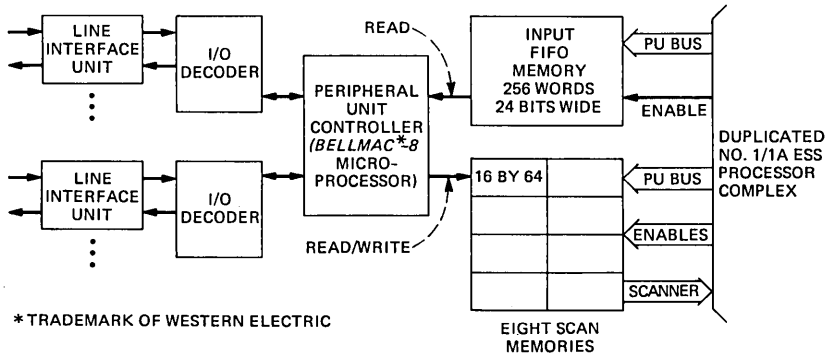

Fig. 10—Data link system block diagram.

eral is that the ESS transmits large amounts of data over its peripheral unit bus to the data link system, and the data link system does the converse over the scanner answer bus. Because of this additional new use of the peripheral bus system, the No. 1/1A ESS peripheral bus system has been modified to provide added data error handling capabilities to ensure the accuracy of data transmission.

The interconnection between a 10A RSS and the data link system is over a 2400 b/s full duplex synchronous link. The transmission facility can be T1 or N or radio carrier. Other digital and analog system links are planned to increase the overall versatility of the system. For added reliability, it is suggested that the facility links should be over diverse facility routes. The data link system supports RS-422/423 line interface requirements. Also, it provides link level X.25 protocol, as defined in CCITT recommendation X.25 of March 2, 1976.

The sections of the data link system consist of an FIFO (First-In/First-Out) buffer memory, scan memory, peripheral unit controller, I/O decoders, and line interface units. All the messages that need to be shipped to a 10A RSS must first be loaded by the ESS into the FIFO buffer. The peripheral unit controller unloads these, forms message frames of 16 data bytes or fewer, and loads these into appropriate destination buffers.

There is only one destination buffer per remote-end device (e.g., one 10A RSS), since the data link controller can concurrently serve a multiplicity of remote devices. The messages are unloaded by the peripheral unit controller from the destination buffers and shipped via the line interface units to the far-end device. The incoming messages from the far-end device are unloaded from the line interface unit by the peripheral unit controller and after appropriate protocol processing, loaded into the scan memory. The ESS receives these messages by reading this scan memory on a scheduled basis.

The heart of the data link system is the peripheral unit controller. It consists of two *BELLMAC**8 microprocessors running in a matched mode per ESS peripheral unit bus. This architecture provides a high degree of redundancy and error checking ability which ensures the overall reliability of the data link system.

XIV. REMOTE TERMINAL FIRMWARE

The 10A RSS remote terminal utilizes the *BELLMAC*-8 microprocessor as the control element. The *BELLMAC*-8 is an 8-bit microprocessor which is specifically designed to efficiently support the C language,[6] since it is a stack-oriented machine with registers that are

* Trademark of Western Electric.

resident in RAM, and with specific instructions concerning the storage and restoring of register variables. As a result, over 80 percent of the 10A RSS remote terminal software is written in the C language. The remainder is primarily a portion of the operating system kernel and those routines that run on a sufficiently frequent interval that they justified using assembly language. The *BELLMAC*-8 design permits memory-mapped I/O and, therefore, 32K of the available 64K address spectrum was allocated to the 10A RSS periphery. The RSS program required approximately 200K, with additional storage required for transient call data and translations. This requirement necessitated devising a multiple memory bank scheme with the operating system controlling the bank selection mechanism. Figure 11 shows the overall address spectrum. This arrangement required that in certain cases code that must be executed out of RAM (for efficiency or for data access) had to be loaded at a different location than where it was actually executed. An overlay loader was designed to automatically resolve the interbank references, although a slight but still manageable compile time linkage resolution remains within the operating system.

The operating system uses a variety of techniques to minimize program interaction. Each identifiable process has its own stack and register area. Audits are provided to ensure that stacks are not overrun, and a preprocessor is used to determine the nested depth of each process. With the stack system, real-time breaks are simple to implement and code is written in a straightforward manner without the need to artificially preserve variables over a real-time segment.

The operating system consists of three basic levels and a multiplicity of failure levels. The three basic levels are as follows:

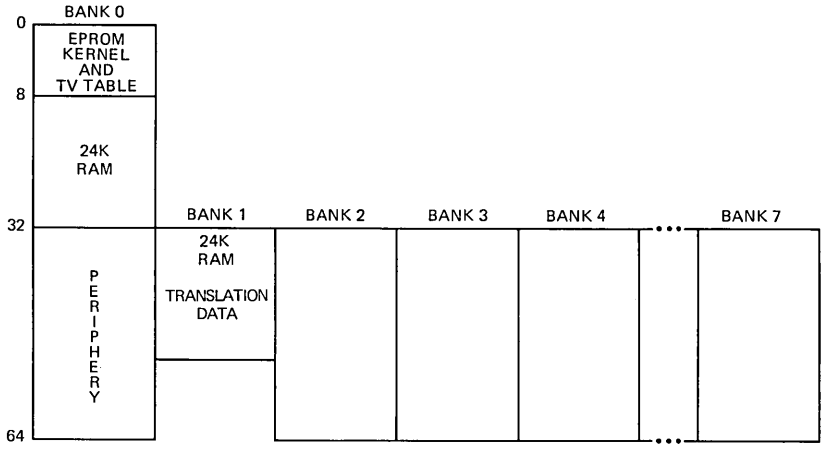

Fig. 11—Remote terminal memory organization.

(*i*) Data link interrupt—Data byte received or ready to be transmitted. This is a random event and at worst case can occur at a 3-ms interval. This is the highest priority job.

(*ii*) 10-ms interrupt—This interrupt is caused by a programmable interrupt chip. Three major jobs are scheduled by this interrupt.

(a) 10-ms repeat supervision—Lines in the dialing state have their on-hook/off-hook status repeated over the channel at a 10-ms rate. This rate ensures that dial pulses will be accurately transmitted to the host.

(b) HLSC execution—HLSCs in the act of setting up a control function, such as ringing, coin collect, etc., require a fast timing rate to control the setting of the various HLSC control points. Once the HLSC is in a stable state, this fast timing is no longer required.

(c) 20-ms repeat supervision—Lines in the ringing state have supervision repeated over the channel to the host at a 20-ms rate. This fast rate is required to minimize any possible speech clipping effects after the called party answers and the final talking connection is setup. This is the lowest priority interrupt function and can be slipped in the event of severe overload.

(*iii*) Base level—Base level is divided into three priority classes, A, B, and C, with class A having the highest priority. A measure of system real-time availability is the C-C (which is the average time it takes to complete the base level loop) and the total number of C intervals within a 15-minute period is output on the host TTY for each 10A RSS. This is analogous to the host base processor cycle time as a measure of the real-time capacity of the machine. Within this C-C cycle, line scanning is performed as a fixed-time interval job. The operating system keeps track of time and only performs line scanning at a 200-ms rate. If the line scan rate exceeds a 200-ms visitation rate, the total number of these slips is recorded in the 15-minute traffic summary for each 10A RSS.

On C level, the operating system allows for a queue of background tasks. Diagnostics and specialized requests from the host are considered background tasks and will be executed in order of arrival. Provisions are made for executing certain background tasks as a priority request, but all background tasks must have an abort capability.

Initialization of the system is under control of the host, but can be triggered automatically either by the host or the remote. The host also has manual control of the remote terminal initialization function. There are four levels of initialization. These are as follows:

(*i*) Reset—System detected a transient error. If possible, a switch to the standby controller was made. The job in progress was lost.

(*ii*) Minimal Clear—System detected multiplicity of errors. Some

minimal portion of the call store is cleared. Some transient calls will be lost because of reset of the system constants.

(*iii*) Transient Clear—System experiencing difficulty possibly because of multiple interrupts. The transient area of call store is cleared and all transient calls are lost. If possible, a switch to the standby controller was made.

(*iv*) Stable Clear—System experiencing great difficulty, and all memory is cleared. If the translation data do not meet internal consistency checks, the host is requested to reinitialize the data base. All calls are cleared from the system. This function can only be requested by a manual action.

To perform its call processing function, the 10A RSS requires certain data concerning each assigned line in the remote unit. The database for these translations resides in the host ESS and is periodically transmitted to the remote unit. A set of remote unit programs maintains the translation database and calculates check sum data so that the operating system can verify the correctness of the data.

The operating system maintains several triggers which verify correct communication with the host. If these triggers fail, the operating system will generate a modified transient clear and go into the stand-alone mode. In this mode, new processes are spawned that route call originations to the stand-alone programs, which control the connection to digit receivers and then analyze dialed digits to route intra-RSS calls to the proper terminations. All other calls are routed to reorder or to an optional announcement. Call capacity during stand-alone is somewhat reduced because of limited availability of system resources, but the machine is protected by a last-in/first-out overload strategy which limits ineffective attempts. During stand-alone operation, calls to emergency numbers, such as "0," "911," or other special numbers can be handled with telephone company prepared inputs. Stand-alone can handle all basic telephone service with the exception that all billing functions are suspended. The basic list of call functions handled during stand-alone operation is as follows:

Intraoffice calling
2-party revertive
4/8 party revertive
Manual line (dial "0")
Permanent signal
Multiline hunt (limited)
Special numbers (911, etc.)
Coin intra (coin returned)
Hotel/Motel (no message register actions)

When data communications are reestablished with the host, the

stand-alone mode is removed and normal call processing actions are resumed. Stable intra-RSS calls are maintained in the transition out of the stand-alone mode.

XV. STATUS

The first 10A RSS was placed into commercial service in December, 1979, in a rural community in upstate New York. The 10A RSS is located in Clarksville and is served by a No. 1 ESS host located at Guilderland, New York, just outside of Albany. Clarksville is connected to the Guilderland host via T1 carrier. The 10A RSS unit at Clarksville serves approximately 700 lines with a mixture of individual, 2-party, 4-party, and coin service. Performance to date has been excellent with notable transmission improvement. The second 10A RSS installation was cutover in June, 1980, in Neola, Iowa. Neola was the first application of the analog carrier host-remote interface. Additional 10A RSS units have been placed into service. At this time, additional development is ongoing to provide 10A RSS host capability for the No. 1A and No. 2B ESS systems.

XVI. SUMMARY

The 10A RSS represents a major milestone in the evolution to an all electronic stored program controlled network. It is now possible to provide economic modern telephone service down to the smallest size community. The 10A RSS has additional applications in areas such as pair gain and feature extension. Its small size and modular construction makes the system extremely portable and no doubt will enable the 10A RSS unit to be rapidly deployed to restore telephone service in disaster situations or to meet a brief need for additional telephone capacity.

This overview of the 10A RSS system is an introduction to the companion papers that follow.

XVII. ACKNOWLEDGMENTS

The authors wish to acknowledge the contributions of many individuals at Bell Laboratories, AT&T, and Western Electric, who have contributed to this work. In addition, the experience of many operating companies provided valuable feedback during the design process.

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No. 10A Remote Switching System:

Control-Complex Architecture and Circuit Design

By R. K. NICHOLS and T. J. J. STARR

(Manuscript received May 22, 1980)

The Remote Switching System (RSS) control complex contains the common circuitry needed to communicate with the host ESS and operate the other equipment in the RSS frame (switching network, line interface circuits, transmission channels, service circuits, etc.) as required to perform the functions of detecting originations, establishing and tearing down network connections, ringing telephones, and all of the other basic functions of a telephone switching system. In this capacity, the RSS control complex is analogous to the central control of a conventional ESS, rather than being a simple frame controller. This control complex contains two equivalent processors. One is active and the other is standing by to ensure reliability.

I. INTRODUCTION

The purpose of this paper is to give a detailed description of the architecture and circuit design of the No. 10A Remote Switching System (RSS) control complex. The RSS control complex contains the common circuitry needed to communicate with the host ESS and operate the other equipment in the RSS frame (switching network, line interface circuits, transmission channels, service circuits, etc.) as required to perform the functions of detecting originations, establishing and tearing down network connections, ringing telephones, and all of the other basic functions of a telephone switching system. In this capacity, the RSS control complex is analogous to the central control of a conventional ESS, rather than being a simple frame controller. This analogy becomes even more exact when one recognizes that the RSS must, when its connection to the host is severed, operate in a stand-

alone mode, and in this mode the RSS control complex provides the entire intelligence for operating the system.

1.1 Elements of the control complex

The RSS control complex can be functionally subdivided into five elements: the processor, which provides the data manipulation and decision-making functions; the memory, which includes both the non-volatile program store and the writable store used for translations and transient data; the data link, which provides communication with the host ESS; the peripheral access circuitry, which links the control complex with the other circuits in the frame; and the maintenance panel, which provides a rudimentary human interface. An additional piece of equipment, used for writing the circuit packs which contain the operating program, is also described here, although it has no direct connection to the RSS frame.

1.2 Design objectives

The principal constraint on the design of the control complex derives from the size of the RSS—typically a single frame. This severely limits the space available for the control complex which must nonetheless, as pointed out above, provide many of the processing functions of a conventional ESS office.

The RSS control complex utilizes the current state of integrated circuit technology which makes possible a processor on a single circuit pack and five circuit packs containing a total of 240K* of memory. These six circuit packs, together with a data link circuit pack, one miscellaneous/interface circuit pack, and 16 fanout circuit packs (located throughout the frame near the peripheral circuits which they control) make up one side of the duplicated control complex. When the RSS is expanded to its maximum size by the addition of a mate frame, an additional 16 fanout circuit packs in that frame (32 including duplication) complete the control complex.

II. GENERAL ORGANIZATION

Figure 1 is a block diagram of the RSS control complex. With the exception of the maintenance panel, the entire control complex is duplicated. Certain of the duplicated elements of the control complex are associated in groups that are always used together. Thus, one processor, one set of memory circuit packs, and one set of fanout circuit packs form a "processor complex" which can be considered as a single unit. A processor complex contains a memory bus, which connects the processor to its memory, and a peripheral bus, which

* As is customary when speaking of memory sizes and addressing, $1K = 1024 = 2^{10}$

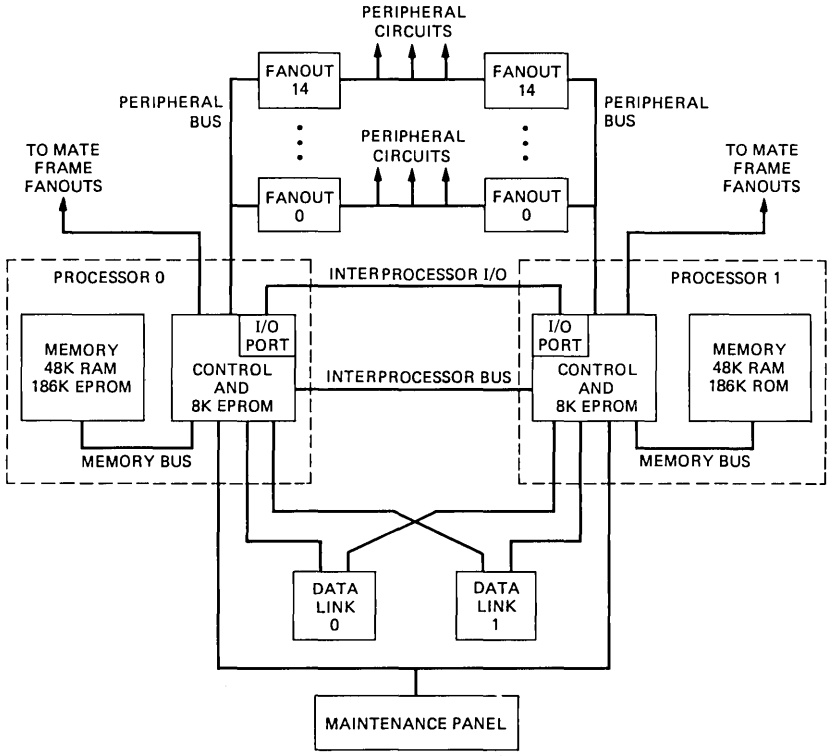

Fig. 1—Remote switching system control complex.

connects the processor to the fanout circuit packs. When a mate frame is provided, a separate peripheral bus provides access to the fanout circuit packs in that frame. Each processor has completely separate access to each of the data links. Thus, there are four possible operating modes for the control complex, as determined by the two processor complexes and the two data links.

2.1 Processor interactions

In normal operation, one processor is active (on-line) and the off-line processor is halted, allowing the on-line processor to gain access to the internal busses of the off-line processor via the interprocessor bus. Through this bus, the on-line processor can keep the off-line memory up-to-date and perform diagnostics to verify the health of the off-line processor complex. This manner of operation is referred to as "dual simplex," i.e., the processor is duplicated (dual) but the on-line processor runs alone (simplex) and does not depend for its error checking upon matching with a synchronously operated mate processor, as would a "duplex" system.

It is possible for both processors to be running simultaneously. This is the case during certain diagnostics, and it can also occur when the system is trying to find a working configuration. The interprocessor bus cannot be used in this condition, and so an eight-bit-wide I/O port is provided to allow messages to be passed between the processors.

III. PROCESSOR

The RSS processor is built around the *BELLMAC**-8 processor, an 8-bit microprocessor with an extensive, general-purpose instruction set. Some of the significant architectural features of the *BELLMAC*-8 processor are as follows:

(*i*) A 16-bit address bus, permitting direct addressing of 65536 (64K) 8-bit bytes.

(*ii*) A single address-space, with no special instructions or control for input/output (I/O) operations as opposed to memory reads and writes (memory-mapped I/O), and no differentiation between the instruction address-space and the data address-space.

(*iii*) Sixteen general-purpose 16-bit registers which, rather than being located within the microprocessor chip itself, occupy a block of memory locations which can lie anywhere in the 64K address space.

(*iv*) One maskable interrupt which can be automatically vectored anywhere in the first 256 bytes of the address-space.

(*v*) One nonmaskable interrupt (reset) which always vectors to location zero.

(*vi*) The ability to synchronize itself with slow memory or peripheral devices by means of an external "ready" indication.

Processor circuitry surrounding the *BELLMAC*-8 processor provides other functions required in the RSS application. These include:

(*i*) Buffering and timing generation for interface to other circuits.

(*ii*) An expansion of the address-space beyond the 64K provided by the *BELLMAC*-8 processor.

(*iii*) Provision for multiple interrupts and generation of the required vector.

(*iv*) Error checks needed to assure proper operation of the system.

(*v*) Circuitry for interfacing and coordination with the mate processor.

3.1 Expanded address structure

The addressing requirements for the RSS processor greatly exceed the 64K that the *BELLMAC*-8 processor can address directly. The addressing must encompass the nearly 200K of program store, the

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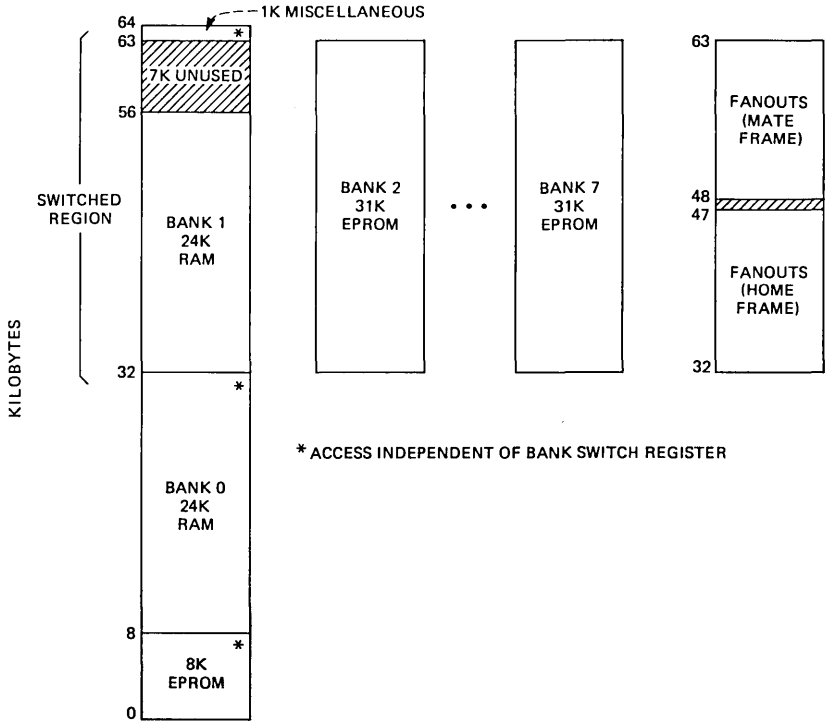

Fig. 2—Remote terminal address space.

48K of writable memory, and the 30K addresses required by the bit-addressable periphery. To accomplish this, a bank-switching scheme is employed.

Figure 2 depicts the bank-switch architecture. The low 32K locations of the address space are not switched, and the memory which occupies this space is, therefore, always accessible. Included in this space, are 8K of program store beginning at address zero and 24K of writable memory. The program store is used for programs which must always be available or which access locations in the switched portion of the address space. Examples of programs which must always be available are the handlers for the maskable and nonmaskable interrupts and the bank-switch monitor. Programs which access the switched portion of the address space include the subroutines which read and write the periphery. The writable memory in this unswitched space includes not only the transient database for the system, but also memory required by the *BELLMAC*-8 processor for use as its general-purpose registers and subroutine-calling stacks.

The uppermost 1024 addresses are also unswitched. This space is

used for I/O port addresses (recall that the *BELLMAC*-8 processor uses memory-mapped I/O). These locations must always be accessible because they include the bank-switch register itself, as well as the interrupt-acknowledge address, from which the *BELLMAC*-8 processor reads the value of the interrupt vector whenever an interrupt occurs.

The remaining 31K portion of the address space (i.e., all but the top 1024 of the upper 32K locations) can be switched either to the fanout circuit packs which control the periphery or to one of seven additional memory banks, which can be either writable memory (as is bank 1, 24K) or program store (banks 2 through 7, 31K each). It should be noted that this architecture prohibits direct references between the switched banks, i.e., a program residing in one of the switched banks cannot directly access anything which lies in a different switched bank. All such references must be performed via subroutines residing in the unswitched portion of the address space.

3.2 Interrupts (maskable)

The processor provides for five sources of interrupts in a software-assisted priority arrangement. The interrupt sources are

(*i*) Data link 0.

(*ii*) Data link 1.

(*iii*) A programmable timer, used to generate the 10-ms interrupt.

(*iv*) A programmable timer, used for miscellaneous timing functions.

(*v*) The interprocessor I/O port.

The *BELLMAC*-8 processor has a single input for requesting a maskable interrupt. This interrupt is termed "maskable" because it is masked internal to the *BELLMAC*-8 processor by an "interrupt-enable" status bit which is under program control. When the *BELLMAC*-8 processor recognizes an interrupt request, it reads a predetermined address (the interrupt-acknowledge address) and interprets the 8-bit value received as an address (in the first 256 bytes of memory) to which control should be transferred. Whenever an interrupt occurs, the *BELLMAC*-8 processor automatically inhibits further maskable interrupts by clearing the interrupt-enable bit. Additional circuitry in the processor provides:

(*i*) An interrupt source register, which records the occurrence (possibly momentary) of an interrupt request from each source. The program can also read and write this register to control processing and aid diagnostics.

(*ii*) An interrupt mask register, which permits the program to enable or disable individual interrupt sources.

(*iii*) Vector generation logic, which generates the data presented to

the *BELLMAC*-8 processor when it reads the interrupt-acknowledge address. These data are determined by the highest-priority interrupt source which is active and enabled.

The hardware-determined priority is only effective for resolving the vector to be generated when multiple interrupt requests are present simultaneously. There is no automatic masking of interrupts having priorities equal to or lower than the one currently being processed. If an interrupt handler is to permit other interrupts to occur, it must, prior to reenabling interrupts in the *BELLMAC*-8 processor, adjust the interrupt mask register such that only higher-priority interrupts are enabled. It must, then, restore the original mask before terminating.

3.3 Error checks

The RSS processor utilizes a combination of software and hardware checks to ensure proper operation of the system. As a consequence of the improved reliability brought about by the use of large-scale integration, the amount of error checking hardware has been considerably reduced from what has been traditional in ESS processors. The most significant change relates, naturally, to the microprocessor itself. The *BELLMAC*-8 processor, like other microprocessors, is almost completely lacking in internal checks. A reasonable way to check such a circuit is to utilize a matcher between two synchronously-operated devices. However, in view of the anticipated failure rate of the *BELLMAC*-8 processor, it is expected that most RSS installations will never experience a single *BELLMAC*-8 processor failure in their 40-year life. Similar, although less dramatic, reliability improvements in other areas have suggested that error-checking circuits should be confined to those areas in which simple circuits can produce a significant benefit rather than having a goal of 100 percent fault coverage. The areas not covered by the hardware check circuits, such as the microprocessor itself, can be tested periodically by software exercise routines.

3.3.1 Nonmaskable interrupt architecture

There are seven circuits in the processor which generate nonmaskable interrupts (resets). The *BELLMAC*-8 processor has a single "reset" input which acts like the interrupt-request input, except that it is unaffected by the internal interrupt-enable bit and it always vectors to address zero, regardless of the data which are read from the interrupt-acknowledge address. The processor contains circuitry to support the various reset sources in a manner somewhat like the maskable interrupt sources, specifically:

- A reset source register which records the occurrence of each condition. The program can read and clear this register.
- A reset mask register (actually, selected bits of the interrupt mask

register) which can individually mask the conditions. This differs from the interrupt mask in that a masked interrupt remains pending, whereas a masked reset is cleared and ignored.

3.3.2 Hardware check circuits

Each of the following circuits can cause a reset and has an associated bit in the reset source register:

(*i*) Miscellaneous decoder check—This detects faults in the circuits which decode the individual enable signals from the top 1024 locations in the address space. Each time an address in this space is accessed, an odd or even parity indication is reconstructed from the decoder output and compared to the parity over the original address. A mismatch raises this error condition. This check has no mask bit.

(*ii*) Write-protect—Memory is write-protected in 4K blocks. An attempt to write into a protected block or an attempt to write into program store is suppressed and this error condition is raised. This check has no mask bit, but the protection status of the writable memory is under program control.

(*iii*) Manual reset—A key on the maintenance panel generates this reset in both processors. It cannot be masked.

(*iv*) Sanity timer—The processor contains a sanity timer which the program must clear at least every 200 ms but not twice within a 40-ms period. A violation of either the minimum or maximum interval raises this error condition, which cannot be masked.

(*v*) Data parity check—On every write operation, the processor generates odd parity over the eight data bits. Whenever data are read from memory or from a data link, parity is checked, and this error condition results if the parity is not odd. This check has an associated mask bit. It should be noted that no parity bit is supplied on reads from the periphery or from any of the special addresses in the processor itself, and this check is, therefore, suppressed in these cases.

(*vi*) Peripheral addressing check—This check is similar to the miscellaneous decoder check, above. On every peripheral access the fanout board reconstructs a parity indication and sends this signal back to the processor. The processor compares this with the parity computed over the original address, and a mismatch raises this error condition. This check has an associated mask bit.

(*vii*) Mate processor reset—This signal is generated under program control in the mate processor. It is used when the on-line processor wishes to initialize the off-line. This reset can be masked.

To simplify the task of the processor diagnostic program, an additional level of control over the resets has been provided. This is a "block hardware checks" bit in a status control register. When this bit is set, only the sanity timer and the manual reset can actually send a

reset signal to the *BELLMAC*-8 processor. The other reset sources can still set their bit in the reset source register, but any further action is suppressed.

3.3.3 Firmware checks

To complement the above check circuits, tests and defensive checks are built into the firmware. Although a full discussion of these safeguards is beyond the scope of this article, certain areas are worthy of note.

(*i*) The processor sanity test (a subset of the processor diagnostic tests) is run on a continuous basis, completing its cycle about every five minutes. This verifies the operation of the *BELLMAC*-8 processor itself, as well as the other parts of the processor not covered by check circuits.

(*ii*) The peripheral data bus is checked during normal use by such techniques as readback checks to verify that an expected state change actually occurred in a peripheral circuit and operational checks which verify the ability to read and write both zeros and ones over each data bit path.

(*iii*) The interprocessor bus is tested as part of the continuous process of verifying that the contents of the on-line and off-line memories match.

3.4 Interface with the mate processor

In addition to the "mate processor reset" described above, there are three areas of explicit interaction between the processors: the interprocessor bus, the interprocessor I/O port, and the peripheral lockout circuit.

3.4.1 Interprocessor bus

The interprocessor bus consists of a 16-bit bidirectional address bus, an 8-bit bidirectional data bus, and a group of control and timing leads. It couples the internal buses of the two processors in a manner which gives the on-line processor almost unrestricted control over the off-line. Whenever a processor is running, its internal bus is protected against interference from the mate. When a processor decides that it should be off-line, it puts itself into a special "hold" state which stops the microprocessor and opens the bus coupling gates to control signals from the mate. The off-line processor is released from hold by the occurrence of a reset or under program control from the on-line. This hold state is controlled by a bit in the processor's bus control register.

Bits in the on-line processor's bus control register control the operating mode of the bus. The bus can be operating in "split" mode, i.e., not accessing the mate at all. Another mode, "double write," causes all

write operations to be performed in both the on-line and off-line processors. A third mode, "mate read," causes read operations having addresses in a specified range to be performed in the mate and the resulting data returned to the on-line processor. It is also permissible for the "double write" and "mate read" modes to be active simultaneously. The 8-bit bus control register, then, contains one bit to control the double-write mode, one bit to activate the mate-read mode, and a bit which causes the hold state to be entered. The other five bits of the register define a 2K block of addresses for which the mate-read mode will be effective.

A processor is prevented from writing into the bus control register of its mate. This is done so that the on-line processor can freely alter its own bus control register without inadvertently releasing the mate from hold. When the on-line processor wishes to release the mate, it can perform a write (with any data) to a special "bus control clear" address while in the double-write mode, thus clearing both bus control registers. The mate processor will resume execution with the instruction following the one that put it in hold, unless it finds an active interrupt request. Of course, it is the responsibility of the software to ensure that the state of the off-line processor has not been so altered while in hold that the resumption of execution would cause an error.

3.4.2 Interprocessor I/O port

The interprocessor I/O port provides communication between the two processors when both are running. This is necessary under certain conditions when the processors are trying to decide which of them should be on-line. The interconnection consists of an 8-bit bidirectional data bus with additional control and interlock leads and both an input buffer and an output buffer at each end. When a processor wishes to send a message to its mate, it writes a byte into its output buffer. These data will be transferred to the input buffer of the mate processor provided that this buffer is not already full and that the interconnecting bus is not busy. The processor can then write another byte into its output buffer, and this will be transferred as soon as the mate reads the first byte from its input buffer. A processor can arrange to be interrupted whenever its input buffer is full or when its output buffer is empty or both.

3.4.3 Peripheral lockout

The processor contains circuitry designed to ensure that the on-line processor can prevent its (possibly insane) mate from accessing the periphery or the data links while, at the same time, keeping its own access unimpeded. This problem is a difficult one in the RSS environment since the office is unattended and there is no independent

communication link over which an outside agency could exercise control of the system—the existing data links function only with the aid of the processor.

Each processor has two flip-flops which control peripheral lockout. One, designated *A*, affects the processor's own access to its fanout boards and to the data links. The other, designated *B*, affects the mate processor's peripheral and data link access. A processor's access is determined by exclusive OR-ing its own *A* flip-flop with a signal from the mate's *B* flip-flop. If these two flip-flops are in the same state, the processor is locked out from its fanout boards and from the data links. Thus, as long as the mate processor's *A* and *B* flip-flops do not change state, a processor can control its own peripheral access with its *A* flip-flop, while its *B* flip-flop controls the mate processor's access.

To reduce the probability that an insane off-line processor would continually alter the state of its *A* and *B* flip-flops, thus making it impossible for the on-line processor to control the system, two separate actions are required to load data into the flip-flops. First, two bits of a register in the processor must be loaded with the data bits destined for the *A* and *B* flip-flops. Then a write must be performed (with any data) to a special "lockout strobe" address. This write clocks the two data bits into the actual *A* and *B* flip-flops. As an additional precaution, this lockout strobe is ineffective if any bit of the reset source register is nonzero.

IV. MEMORY

The RSS control complex contains two types of memory: writable random-access memory (RAM) and nonwritable erasable programmable read-only memory (EPROM). Each of the duplicated processors has its own dedicated memory.

4.1 Memory organization

To permit access from the *BELLMAC*-8 processor's limited 64K address space, memory is divided into banks (see Fig. 2). The low 32K addresses are used to access one 24K bank of RAM and a special 8K block of EPROM. The remaining banks, one 24K RAM bank and six 31K EPROM banks, are accessed selectively from the upper half of the address space, under control of the processor's bank switch register.

4.1.1 Physical arrangement

Each RAM circuit pack contains 24K by 9 bits of storage (24K with parity) built up from 4K by 1 bit devices in a straightforward array. Each RAM circuit pack corresponds to a logical bank.

The 8K block of EPROM is located on the Processor B circuit pack (one of the two packs that make up each processor). The 8K by 9 bits

of storage are provided on five 2K by 8-bit devices in a manner similar to that used for the 64K EPROM circuit packs described below, although the details of the parity-bit mapping are different.

The 31K EPROM banks are contained on circuit packs, each of which contains 64K by 9 bits of storage built up from 2K by 8-bit devices. Each circuit pack contains two banks. The devices which contain the eight data bits are arranged in a conventional fashion with all of the devices paralleled onto a common data bus and selectively enabled by decoding the higher-order address bits and the bank-select. The required 64K parity bits are contained in four additional devices.

The data outputs from these devices are paralleled into an 8-to-1 multiplexor which selects one of the eight data bits, with the selection being determined by the low-order three address bits. The address bits supplied to these four EPROM devices, and to the decoder which selects them, are shifted three bits compared to the address supplied to the array containing the data bits. Thus, the first address in the first parity EPROM contains the eight-parity bits which correspond to the first eight bytes in the data EPROMs, with the multiplexor selecting the proper parity bit for the particular location being read. Of the 64K bytes on each EPROM circuit pack, only 62K can actually be accessed by the processor. The missing addresses (1024 in each bank) are occupied by the "miscellaneous decoder" locations at the high end of the processor's address-space.

The EPROM circuit packs and the processor B circuit pack contain additional control and access which permit the devices to be programmed after the board has been assembled. Thus, the devices can be soldered directly into the circuit pack, avoiding the reliability problems inherent in having large numbers of sockets, while still allowing the devices to be erased (by UV light) and reprogrammed as needed. The RSS frame provides neither the 25V power supply nor the necessary control signals for the programming operation, thus protecting the data against alteration while the packs are installed in the system. A separate piece of equipment, called *PROMUS** reprogrammer is required to erase and program data into these circuit packs.

4.2 Memory access

The memory does not contain any identifiable controller. All of the required address, data, and timing signals are generated in the processor itself.

4.2.1 Random-access memory

The access time of the RAM circuit pack (250 ns) is such that a single

* Trademark of Western Electric Company.

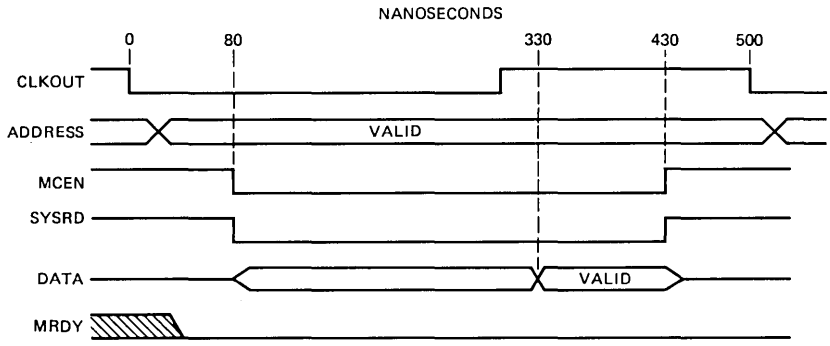

Fig. 3—Random-access memory read cycle.

BELLMAC-8 processor clock cycle is sufficient for the operation. Figure 3 shows the timing of a RAM read cycle. The *BELLMAC*-8 processor's CLKOUT signal is used as a timing reference. The primary timing signal to the memory is the chip-enable, MCEN, which is applied to the selected memory devices to define the access cycle. It is a 350-ns pulse delayed 80 ns from the negative transition of CLKOUT to allow the address and bank selection to propagate. The SYSRD signal going to a low level identifies this cycle as a read access and controls the buffers which gate the data from the memory onto the backplane bus. The selected memory circuit pack pulls MRDY low to indicate to the processor that the access can be completed in a single clock cycle.

4.2.2 Random-access memory write cycle

The write cycle (Fig. 4) is initially the same as a read. The SYSRD remains high, however, turning on the buffers which gate the data off of the backplane bus into the memory. Late in the cycle a write pulse, MWRT, causes these data to be loaded into the addressed memory cells.

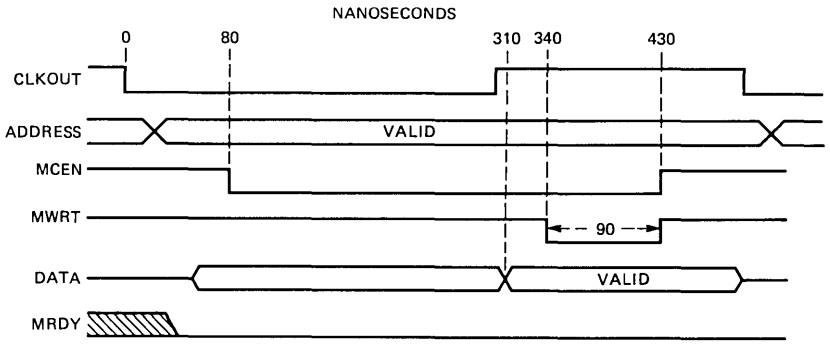

Fig. 4—Random-access memory write cycle.

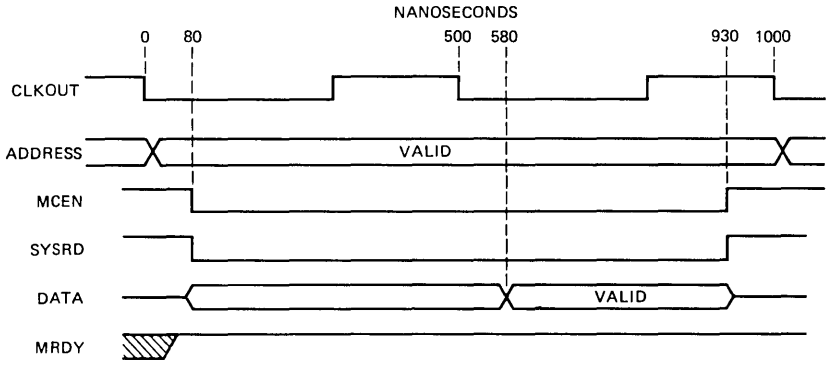

Fig. 5—Erasable programmable read-only memory read cycle.

This write pulse is short (90 ns) because the data from the *BELLMAC*-8 processor are not available until late in the cycle. This, of course, represents a significant requirement imposed on the devices used in the memory.

4.2.3 EPROM access

The EPROM devices are too slow to be accessed in a single clock cycle. The access (Fig. 5) is otherwise similar to a RAM read. The MCEN timing signal enables the addressed devices, and SYSRD turns on the data buffers. The MRDY signal remains high throughout the cycle, informing the processor that it must wait an extra clock cycle for the data to become valid.

4.2.4 Write protection

The write-protect circuitry is intended to prevent accidental alteration of semipermanent data in RAM (e.g., translations). The RAM is write-protected in 4K blocks. Each RAM circuit pack contains an 8-bit register which holds the protection status for the six 4K blocks on the pack (two of the bits are unused). Whenever a protected block is addressed, the memory pack grounds a backplane lead, WPBLK, which informs the processor that any write should be suppressed and treated as an error. The RAM circuit pack does not itself suppress the write. The EPROM circuit packs also ground WPBLK whenever an EPROM bank is addressed. Although the "write" in this case would be harmless, the resulting error indication does help to catch program bugs that cause writes to EPROM.

V. REMOTE SWITCHING SYSTEM DATA LINK

The RSS data link provides a fully duplicated path for the flow of control messages between the RSS remote terminal and its associated host ESS. Two voice channels, among the many provided by the

transmission system between the remote terminal and the host, are dedicated for use by the two data links. Serial, full-duplex information flows at a rate of 2.4 kb/s. The two voice channels used by the data link may be provided by either analog or T1 carrier facilities. Channel 12 of the first two carrier groups is used. The X.25 version of the Synchronous Data Link Control (SDLC) protocol is used to provide message synchronization and error control.

5.1 Overview of the data link

Figures 6 and 7 show the various units in the data link path for a T1 carrier and an analog carrier application. The T1 carrier specifies a frame format that time division multiplexes 24 voice channels together onto a high-speed line. The data rate on the high-speed transmit pair and on the receive pair of wires is 1.544 Mb/s. The analog carrier may be a metallic connection, radio, or N carrier. The N3 and N4 carrier frequency division multiplexes 24 voice channels onto two pairs of wires; the N2 carrier multiplexes 12 channels.

Data links from various systems attach to the Peripheral Unit Controller (PUC), and each line attaches to a separate Line Interface Unit (LIU). The PUC acts as a front-end processor for the ESS by performing the processing associated with the X.25 protocol, including acknowledging received messages and autonomously retransmitting messages as needed.

5.1.1 The T1 data path

Figure 6 shows only one data link; the other link follows a similar path. Both data links connect to the same PUC, but separate *D*4 banks are used at the host end and separate T1 circuits are used at the remote terminal.

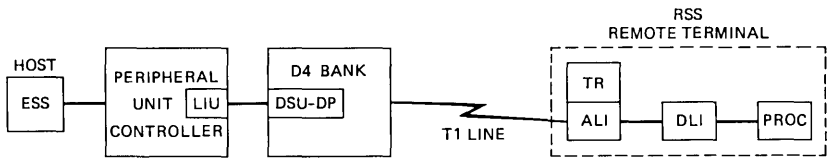

Fig. 6—Block diagram of digital carrier data link.

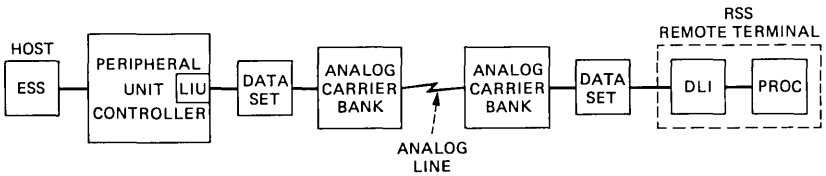

Fig. 7—Block diagram of analog carrier data link.

The time multiplexed frames of information on the T1 line are encoded and decoded by the *D*4 channel bank at the host end of the link. This bank has a separate plug-in for each of the 24 channels; slot 12 contains a Data Service Unit, Data Port (DSU-DP) plug-in. Channel 12 is used by the data link and the other slots contain voice channel units. The DSU-DP converts the serial 2.4 kb/s data to a speed and format suitable to the T1 carrier. The interface between the PUC-LIU and the DSU-DP is specified by the Electronics Industries Association (EIA) Recommended Standard (RS) 449 interface described in section 5.2.3.

The length of the T1 span from host to remote terminal is constrained by the need to provide an acceptable grade of voice service, not by the data link. The Alarm-Line Interface (ALI), and Transmit-Receive (TR) circuit packs located in the remote terminal integrate the function of the *D*4 bank common equipment into the RSS frame.

A portion of the Data Link Interface (DLI) circuit pack is a subset of the DSU-DP. The remainder of the DLI provides the hardware needed to process the X.25 protocol and an interface to the two processors in the remote terminal. The connection between the DLI and the RSS processors is cross-coupled to allow either processor to access both data links.

5.1.2 Analog data path

Figure 7 shows the data link path for the analog carrier. Again, two of the channels provided for voice are dedicated for data link use. The functions and connections to the PUC are the same as for the T1 carrier. The 201*C* data set uses phase-shift modulation to convert the 2.4 kb/s serial data to and from the PUC to a form suitable for the voice channel. A four-wire connection is made from the data set at each end of the link to the analog carrier facility. This data set allows the use of a standard voice channel unit in the analog carrier bank for the data link. The restriction on the length of the analog carrier data link is similar to the limit for the T1 carrier, i.e., the link length is restricted by the voice transmission requirements.

A connection is made, at the remote terminal, between the data set and the DLI circuit by means of the EIA RS-449 interface described in section 5.2.3. The connection between the DLI and the processors is the same as described for the T1 carrier.

5.1.3 Maintenance features

There are three data link loop-back modes under control of the ESS processor and three loop-backs under control of the RSS processor. When a processor activates a loopback any data sent from that

processor travel down the link until it reaches the loopback point. It is then "reflected" back to the originating processor.

Data from the host may be looped back at the PUC, at the DSU-DP (the data set for analog carrier), or at the DLI (data set) at the remote terminal. Data from the RSS processor may be looped back at the DLI protocol section, at the T1 circuit on the DLI (data set for analog carrier), or at the host DSU-DP (data set). One of the bits generated in the T1 data port encoding is reserved for controlling the remote T1 loopback mode. Note that for both T1 and analog carriers these loopbacks affect only the data link channel.

5.1.4 Link duplication

With the exception of certain data link diagnostic routines, only one data link needs to be used, but two links are provided to achieve a high degree of reliability. To ensure that a single fault cannot affect both links, they do not share any common equipment. The PUC is internally duplicated, and separate LIUs are used for each link. Separate cables from the two LIUs connect to separate DSU-DPs that are in different T1 digroups. In the case of an analog carrier, the PUC-LIUs attach to separate data sets which use different analog carrier facilities. Regardless of the type of carrier used, the two links utilize independent transmission facilities. In the ideal case, the facilities would be geographically diverse. This philosophy of link duplication is continued in the design of the remote terminal with two processor interfaces to the two DLI circuit packs.

5.1.5 Data link protocol

The host ESS always decides which data link to use. On an average there is more link traffic from the host, than to it. Typical messages from the host include call processing commands such as set up a path, ring a phone, or collect a coin. Other messages from the host request diagnostics, or request a reconfiguration. Typical messages from the remote terminal include: order acknowledgment, line origination, diagnostic results, audit results, traffic measurement results, and error reports.

The widely used X.25 protocol provides message synchronization and error control. The protocol operations are supported by hardware located in the PUC-LIU and the RSS-DLI. This protocol is a refinement of the SDLC protocol proposed by IBM.[1] For the RSS application, the messages are formed into blocks of 0 to 16 bytes of data, with 6 bytes of protocol overhead. The first and last eight bits of each block are a flag character (01111110). An extra zero is inserted after every fifth contiguous one before transmission to prevent the body of the block

from mimicking the flag character. The extra zeros are automatically stripped upon reception of the data.

Every block has a 16-bit Cyclic Redundancy Code (CRC) word to provide error control. This word results from the successive division using the CRC-CCITT polynomial. The CRC check was selected because it requires only a shift register with a few feedback gates and a comparator. Also, the probability of the CRC check detecting even a large burst of errors is better than 99.99 percent.

If a message is garbled or entirely lost it will be ignored and a retransmission will be requested. Several retrials will be made before a protocol impasse is reported to the host.

5.2 Data link interface circuit pack

The DLI connects to the two remote terminal processors via parallel data buses. The data pass through the X.25 protocol logic where protocol control fields are added. The data then undergo a speed and/or level conversion, and are presented to either the T1 circuits integrated into the remote terminal, or to an outboard data set for analog carrier. The DLI uses mostly TTL SSI, and MSI technology, with some PMOS and NMOS LSI circuits. The few analog functions of the DLI are performed by a handful of discrete devices. The two DLIs are powered from separate converters, and reside at opposite sides of the frame. Figure 8 shows the DLI block diagram.

5.2.1 Processor interface

There are four busses that connect the two processors to the two DLIs. Each is a private connection between one processor and one DLI. Two identical circuits on the DLI provide interfaces to the two processors.

Each bus has 8 bidirectional data bits and a bidirectional odd parity bit. The three low-order address bits are sent from the processor to select which register on the DLI is used. The upper bits of the address are decoded on the processor boards to generate two enables. The Data Link Enable A (DLENA) selects the group of registers that reside in the protocol circuit. The Data Link Enable B (DLENB) selects the group of registers that support the processor interface. A signal called INHIB from each processor sanity circuit indicates if signals from a processor should be ignored. The WE and RE signals are timing strobes used for the read and write operations.

Any data link interrupt condition is passed to each processor by the Interrupt (INT) signal. Most of the actions by the data link control program are prompted by an interrupt. During normal operations an interrupt results from a data byte being received, or the transmitter being ready for the next byte of out-going data. The following error

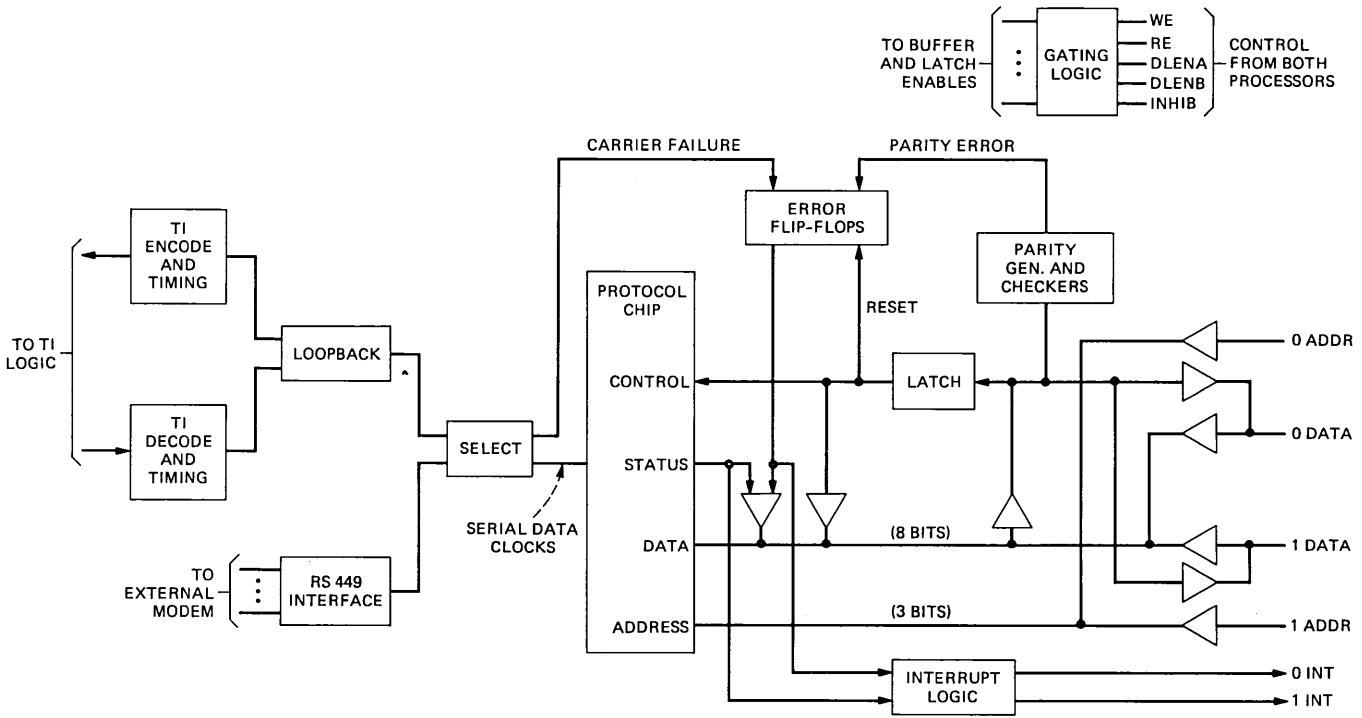

Fig. 8—Remote switching system data link interface functional block diagram.

conditions will also cause an interrupt: overflow of the receiver, underflow of the transmitter, received message with bad CRC, write parity error, and carrier loss on the transmission facility. An interrupt will remain pending until all causes are serviced by program action.

The first action taken by the DLI control program to service an interrupt is to read the interrupt cause register in the DLI. A separate bit in this register is assigned to each cause for an interrupt. Depending on the state of the DLI, the control program will then either read the received data register, write the transmit data register, or operate the DLI control latch to clear an error condition.

A timing wait-state is generated by the processor to allow the DLI a 1-μs operation cycle. If both processors access the same DLI at the same instant, a bus conflict may result internal to the DLI.

During read operations, the DLI generates an odd parity bit. To allow diagnosis of the processor parity checker, the DLI has a parity error register which, when read, places bad parity on the data bus.

5.2.2 Protocol logic

Almost all of the X.25 protocol circuitry is held in a single 40-pin, dual-in-line package integrated circuit. This NMOS LSI circuit is made by Signetics Corporation,[2] and is called the 2652 Multiprotocol Universal Synchronous Receiver/Transmitter. The 2652 interfaces parallel data to a serial synchronous data communications channel, with the high-level protocol functions left to the processor. The 2652 is a full duplex interface; thus, the transmit and receive sections operate independently of each other.

The 2652 performs a serial/parallel conversion, and buffers up to two bytes of data in both the transmit and receive directions. If the buffering capability is exceeded, an error flag is set.

To start the transmission of a block, the processor toggles the "transmit start of message" bit in the transmitter status register. The 2652 then generates a beginning flag character and indicates that the transmitter is ready for out-going data. During the body of the block, the 2652 inserts a zero after every fifth contiguous one to ensure that a flag-like character will not appear in the middle of a block. When the end of a block is reached, the processor toggles the "transmit end of message" bit in the transmitter status register. This causes the CRC check-word that the 2652 has been accumulating to be transmitted followed by an ending flag, also generated by the 2652.

When the start of a message is received by the DLI, the 2652 recognizes the in-coming flag and sets the "receive start of message" bit in the receiver status register. Every time another data byte is received the "received data available" condition causes an interrupt to the processor. During the body of the received block, the zeros inserted

after five contiguous ones are automatically removed making the zero insertion transparent to the processor. When the ending flag is received, the "receive end of message" bit is set in the receive status register, and the preceding CRC check-word is automatically examined by the 2652 to determine if the message was garbled.

Setting the "maintenance loop" bit in the DLI control latch causes data to be looped back to the remote terminal processor after passing through the processor interface and the 2652 IC.

5.2.3 Analog carrier interface

When the carrier select input, CARSEL, to the DLI is not grounded at the remote terminal backplane, the analog carrier serial interface is selected. The functions of the analog interface signals are specified by EIA RS 449.[3] The electrical characteristics for the unbalanced signals are described by EIA-RS 423.[4] Wave-shaping is used to limit the high-frequency content of the signals. This allows the signals to travel up to 1000 ft. The only departure from the standards is that a separate ground is used for each data and clock signal to improve noise immunity. This interface is compatible with the digital interface provided by the 2024A data set and the DSU-DP.

A positive 5-volt potential on the TR data lines represents a logic zero, and negative 5-volt potential represents a logic one. A voltage transition from +5 volts to −5 volts on the receive clock signal causes the DLI to sample the receive data signal. A voltage transition from negative to positive on the transmit clock input to the DLI causes it to shift out the next bit on the transmit data line.

The local and remote loopback signals from the DLI cause the data set to loop data when at a potential of +5 volts. Minus five volts on the signal quality line from the data set informs the DLI that the data set has lost its receiver carrier.

5.2.4 The T1 carrier interface

When the carrier select input, CARSEL, to the DLI is grounded at the remote terminal backplane, the T1 carrier interface is selected. The 2.4 kb/s data from the protocol logic is encoded and transformed in speed by the T1 carrier interface, and presented to the ALI and TR circuits in the remote terminal. The T1 carrier interface circuitry is a close copy of the primary logic in the DSU-DP. The next section discusses this logic.

5.3 Data service unit—data port (DSU-DP)

The DSU-DP is a channel unit that allows synchronous, binary data to pass over a T1 channel. A switch in the DSU-DP selects a data rate of 2.4, 4.8, or 9.6 kb/s. For the DSU-DP to operate in a *D4* bank, an OIU-

2 (Office Interface Unit) must be installed in the common equipment section and backplane wiring must be present to convey an integrated 8- and 64-kHz clock from the OIU-2 to the data port(s). The "customer" interface is the same as the RS-449 interface described in section 5.2.3. After data channel control information and data redundancy are added, the steady 2.4 kb/s data rate is converted to 1.544-Mb/s bursts of 8 bits every 125 μs. This yields an average T1 line per data channel bit rate of 64 kb/s.

5.3.1 D4 bank signals

Transmit data from the DSU-DP are gated on the time multiplexed TNDATA line to the *D4* common equipment. Receive data to the DSU-DP are sampled from the time multiplexed RNPCM line from the *D4* common equipment. The multiplexing of the 24 channels is controlled by two sets of signals. One set is a 1-out-of-6 select and the other is a 1-out-of-4 select. The TDCLK, and RCLK signals provide the TR 1.544-MHz data bit timing. The TWD and RWD indicate the timing windows for transmit and receive channels at an 8-kHz rate.

When the DSU-DP sees its channel selected, and the timing window present, data are transferred to/from the common equipment. The RNDIS signal from the common equipment goes low as soon as a loss of T1 synchronization is detected, and the DSU-DP passes this along to the signal quality indicator at the RS-449 interface.

5.3.2 Encode/decode

The data between the DSU-DP and the *D4* common equipment are in a Digital Data System (DDS) line format. The first bit of each 8-bit T1 data byte is a zero. The last bit is a one for data and a zero for the remote loop command. The center 6 bits are the data from the "customer interface." This byte is transmitted 20 times, and then the next six bits, plus control bits, are sent 20 times, and so on. Error correction is performed by majority logic on reception. A random line bit error rate of one bit error per 10^6 improves to one bit error per 10^{17} after error correction.

5.3.3 Loopback operation

When the local loop command is active at the RS-449 interface, the transmit data from the RS-449 interface are looped back after passing through only the first stage of many levels of encoding. When the remote loop command is active at the RS-449 interface, a remote loop code is sent over the T1 line. It is interpreted at the remote end after passing through all but one level of decoding. The remote DSU-DP logic then returns the code and the originating end loops the data from its transmit line to its receive line.

A "fly-wheel" mechanism is used to turn the remote loop made on and off. To turn it on, the remote loopback code must be received three times in a row. It is turned off when no remote loopback code is received in five successive bytes.

5.4 Analog carrier data set

The 201C data set is a 2.4-kb/s synchronous private-line modem. This full duplex data set has a 4-wire, 600-ohm analog interface. The digital interface is the RS-232C interface described above. To prevent the data set and carrier system from over-driving each other, a resistive attenuator must be placed between the two.

The 201C uses phase-shift keyed modulation to send digital data over a 3002-type private line channel.

VI. PERIPHERAL ACCESS

The basic architecture for the peripheral access can be seen in Fig. 1. The peripheral busses and fanout circuit packs are duplicated and dedicated to a particular processor. The peripheral bus, which interconnects the processor and the fanouts, contains a unidirectional address bus and a bidirectional 8-bit data bus. For reasons of electrical loading and fault resolution, the peripheral busses for the home frame are separate from those for the mate frame. Each fanout board connects to its associated peripheral circuits via a set of wires which is common with its mate fanout board. The peripheral circuit packs are divided into groups of eight which share a common set of leads from the duplicated fanout boards. The peripheral bus is dc-coupled, as is the interface between the fanout boards and the peripheral circuits.

6.1 Fanout circuit pack

The fanout circuit pack provides the following functions:

(*i*) Recognition of its address on the peripheral bus.

(*ii*) Enabling of the addressed peripheral circuit(s).

(*iii*) Writing a single bit of data to an addressed peripheral circuit.

(*iv*) Reading digital data or an analog voltage level from a group of eight peripheral circuits.

(*v*) Generation of error-checking signals to verify proper addressing.

6.1.1 Data flow

The data paths shown in Fig. 9 provide for both reading and writing of peripheral circuit packs, as well as control of the fanout circuitry which permits measurement of analog signal levels from the peripheral packs.

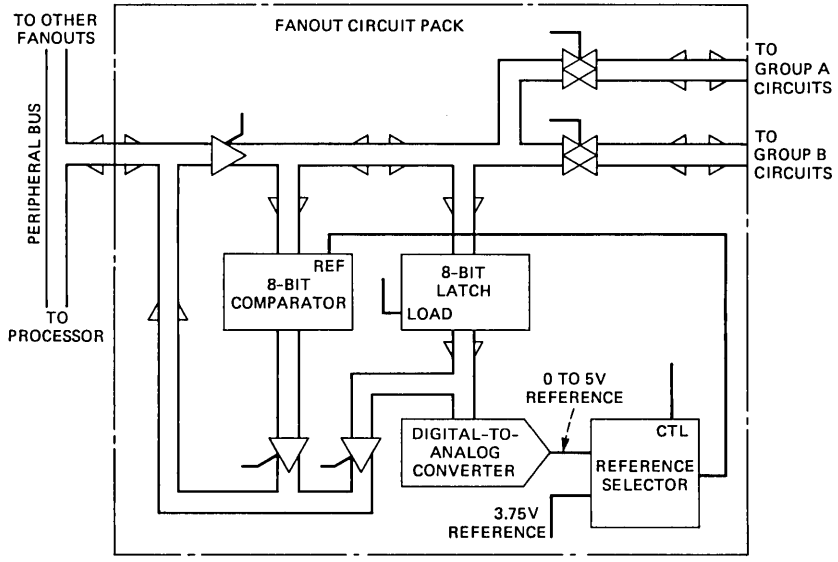

Fig. 9—Fanout data paths.

The data paths for the write operation are straightforward. The buffers which receive data from the processor (via the peripheral bus) are turned on by the lack of the READ signal. One of the two groups of analog switches is turned on, steering the data to the addressed circuit group. Within this group, each of the eight circuit packs receives one of the eight data leads. One of the peripheral packs is then enabled by the addressing logic (see below) to receive its data bit. Thus, writing is performed on a single-bit basis.

The read operation is more complex. One of the two groups of analog switches is turned on as before, gating a signal from each of the eight circuit packs into its corresponding comparator. The reference inputs of all eight comparators are supplied with the output from a digital-to-analog converter (DAC) located on the fanout board. The DAC can be program-controlled to provide an output from 0.0 volts through 5.0 volts in 25-mV steps. Alternatively, a control lead on the peripheral bus can select a fixed 3.75-volt reference. The READ signal turns on the buffers which gate the comparator outputs onto the peripheral bus. Thus, 8 data bits are returned—the results of the 8 comparisons of the voltages from the circuit packs against the selected reference.

The 3.75-volt fixed reference is provided to assist certain interrupt-level programs which perform directed (i.e., nonsequential) read operations. This reference is selected on all fanout boards by a single bit in a processor register in contrast with the DAC reference, which is controlled by a register on each fanout board. By selecting the fixed

reference, the interrupt-level program is relieved of the task of saving and restoring the DAC setting during each operation. The 3.75-volt reference value was chosen to be optimal for scanning lines.

6.1.2 Addressing

Figure 10 shows the peripheral address format and the associated fanout circuitry. The address bits on the peripheral bus can be considered in three groups: those bits which select a particular fanout board and circuit group, those bits which select a peripheral circuit pack within the group of eight, and those bits which select particular circuits and functions within a peripheral circuit pack.

The address bits which select a particular fanout board are present in the peripheral bus in both their true and complemented form. The address for a particular fanout board is determined by the wiring of its connector position such that a unique combination of true and complemented bits is presented to the NOR gates which enable the pack. Each fanout board accesses two electrically separate groups of eight circuit packs. The access to these groups is kept as separate as possible for reliability reasons, but the required circuitry is placed on a single fanout board for economic considerations. Thus, the fanout board has two enabling NOR gates whose addresses differ only in the group-select bit (bit 9).

Address bits 6 through 8 are used in write operations only and serve to select the single circuit pack to be written. These bits are decoded on the fanout board to generate a single write pulse in the proper group when a write timing pulse is received from the processor. If the operation is a read rather than a write, a common READ signal is sent to all eight packs in the group.

The remaining address bits (0 through 5) are simply passed on to the selected circuit group. They are bussed to all eight circuit packs, where they are used to address particular circuits and functions within the packs. Bits 0 through 2 are called the circuit select bits, and bits 3 through 5 the function select bits, corresponding to their usage on line interface circuit packs. This usage, however, is not universal.

6.1.3 Miscellaneous operations

The fanout board reserves the address combinations of function code 7 with circuit select codes 4 through 7 for internal operation involving the DAC. One code is used to read or write the 8-bit register which provides the input to the DAC. Another code gates the output from the DAC to the data input of one of the comparators. By performing a read of this address and using the fixed reference, the DAC output can be compared to the 3.75-volt reference as a maintenance check.

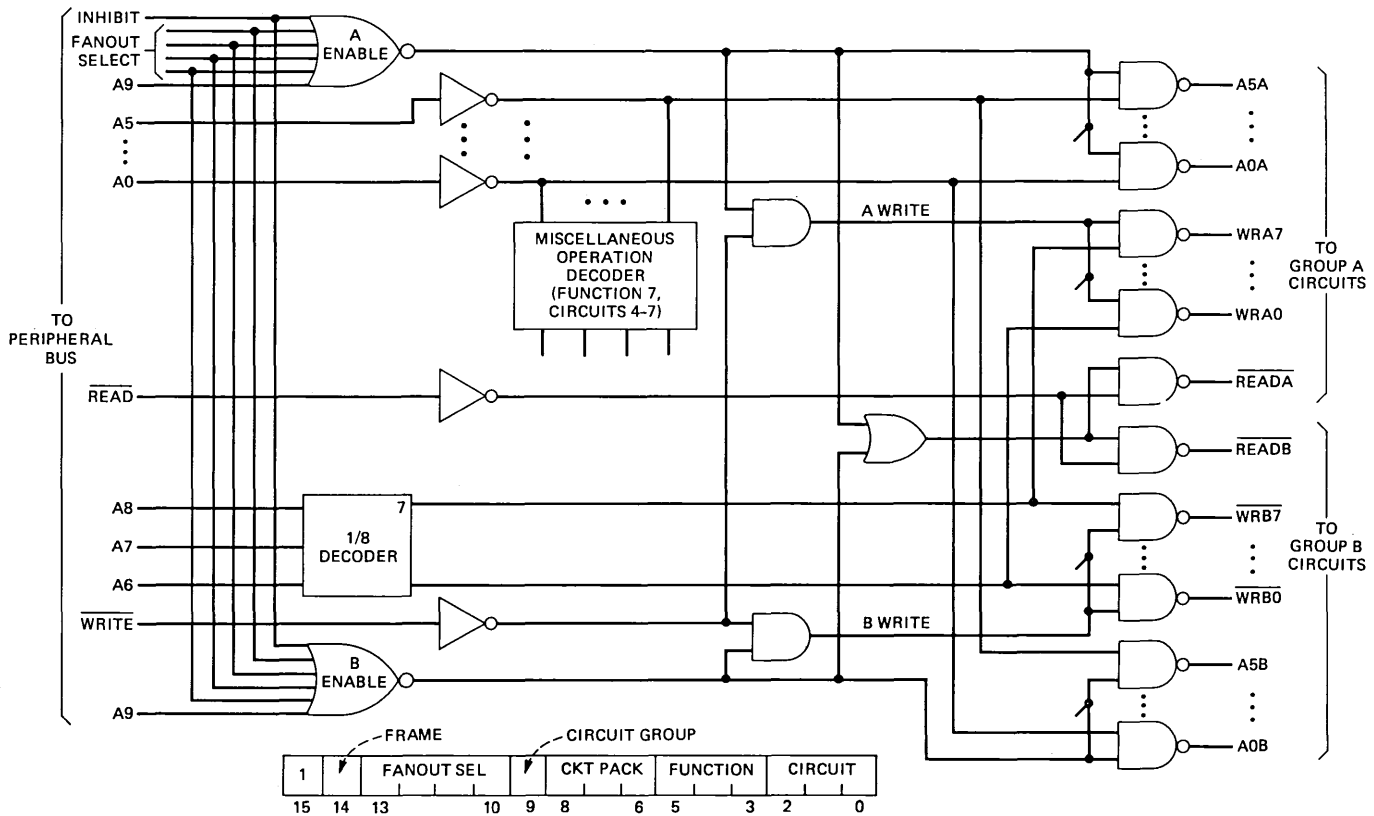

Fig. 10—Fanout addressing.

6.1.4 Error detection

The fanout board returns address checking signals to the processor during every operation. A parity signal is reconstructed from the fanout board selection and from the address, read, and write signals which the fanout sends to the peripheral circuits. The result is returned to the processor on a one-out-of-two basis. The processor can then check the parity signal received against the expected parity computed over the address bits. This check gives assurance that the correct circuit was addressed. Verification of the data paths is left to program checks which observe the operation of the controlled circuits.

6.2 Peripheral timing

Peripheral read and write operations take 6.5 μs. The timing on the peripheral bus is shown in Fig. 11. Initially, all address and control signals are high. The cycle begins when the processor places the address on the bus. In the case of a read cycle, the READ signal goes low, 1.0 μs later. The selected fanout board passes the READ signal and the low-order address bits to the circuit packs in the selected group. The voltages returned from these packs pass through the comparators on the fanout board, and the resulting digital signals returned to the processor on the data bus. The processor latches up the returned data about 0.5 μs before the end of the cycle. The address and READ signals then go high, ending the operation. While the READ signal is active, the fanout board also returns the parity check signal used for address verification.

In the case of a write cycle, the processor places the data on the bus about 0.5 μs after the address. After a 2.0-μs delay to ensure that the address and data have reached the peripheral circuit, the processor

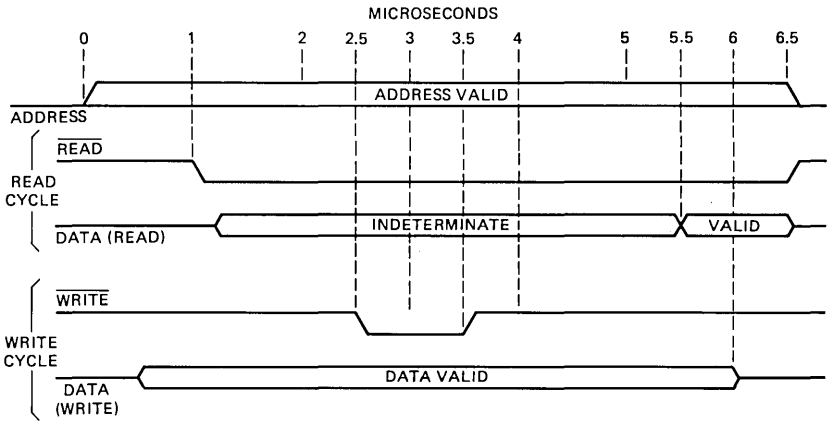

Fig. 11—Peripheral timing.

generates a 1.0-μs write pulse. The fanout board passes this write pulse to the addressed circuit pack and returns a parity check signal. The processor then provides a 2.5-μs hold time on the address and data before ending the cycle.

VII. MAINTENANCE PANEL

The maintenance panel provides the local human interface to the RSS frame. Inasmuch as the primary control of the RSS is from the host ESS via the data link, the maintenance panel assumes a position of minor importance. It is provided mainly as a convenience for certain maintenance operations. Accordingly, the design objective of simplicity took precedence over providing additional functions and even over making the processor-to-panel interface tolerant of faults in the off-line processor.

The panel keys and indicators, shown in Fig. 12, can be separated into two groups: those which have a direct interaction with the hardware, and those which only connect to I/O ports on the processors.

7.1 Direct hardware interactions

There are five keys and two indicators which fall in this category. The two RMV PWR (remove power) keys and the RST PROC POWER (restore process power) key are used to remove and restore power from a processor complex. They directly control the relays which sequence the processors' power. The two associated PWR OFF indicators are controlled by these relays to show that power has been removed. To reduce the likelihood of an unfortunate human error, the RMV PWR keys are individually enabled under processor control. The circuitry which performs this function, however, is not part of the maintenance panel but is located on the Power Alarm and Monitor circuit pack which is accessed via a fanout board.

The PANEL PWR key simply removes and restores power to the panel indicators. As a safety precaution, the other panel keys are disabled whenever the indicator power is off.

An additional SYSTEM BOOTSTRAP key, not shown in the figure, provides a direct reset to both processors. This key provides a means, independent of the data links, to force the system to its highest level of initialization.

7.2 System status indicators

Nine indicators are controlled by the processor to indicate the system status. These are

(*i*) MAJOR, MINOR, and CRITICAL, which are the standard system alarm indicators.

(*ii*) MASTER PWR ALARM, which indicates a blown fuse or trouble with a power converter.

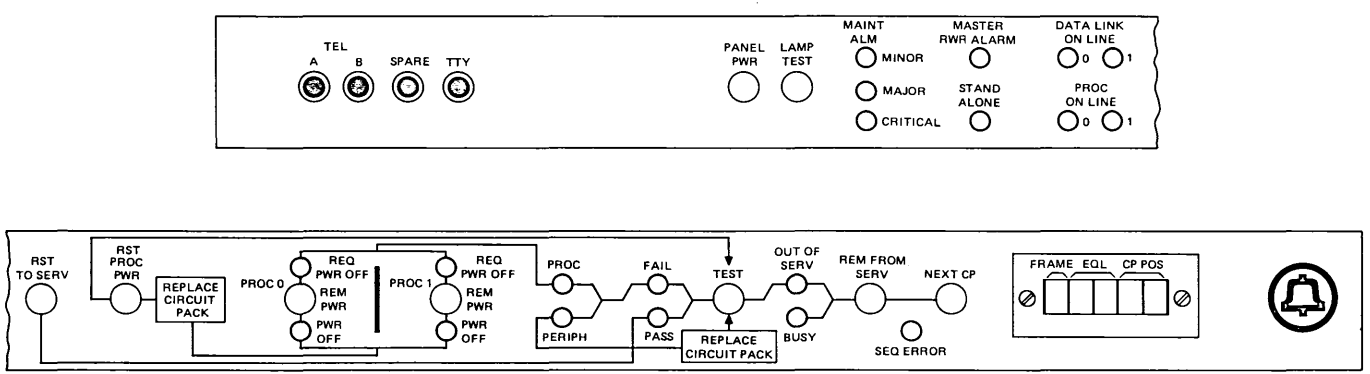

Fig. 12—No. 10A RSS maintenance panel.

(*iii*) STAND ALONE, which indicates that the system is operating without a data link to the host.

(*iv*) The two DATA LINK ON LINE indicators.

(*v*) The two PROCESSOR ON LINE indicators.

7.3 Diagnostic control keys and indicators

The remaining keys and indicators and the digital display are used by a craft person who is attempting to repair a fault by replacing circuit packs. To do this, the RSS is first "primed" with a list of suspect circuit packs. When this has been done, pressing the NEXT CKT PACK (next circuit pack) key will step through this list, displaying each pack's equipment location in the digital display. The pack indicated in the display can be removed from service, tested, and restored to service by means of the other panel keys. The other indicators inform the craft person of the results of tests and indicate other actions which should be taken. For example, the REQ PWR OFF (request power off) lamps indicate when power should be removed before replacing a defective circuit pack in a processor complex.

7.4 Processor interface

The processor interface was designed to require a minimum of circuitry in the panel itself. Each indicator is controlled directly by a lead to a processor I/O port. The digital display contains its own latches to hold the digit values, and the processor interface consists of four leads to carry the binary-coded value and five-digit enable leads to load this value into one of the digit positions. These leads as well are driven by I/O ports in the processor. Each key simply grounds a corresponding lead to each processor. These leads connect to bits of an I/O port which is periodically scanned to detected operated keys.

The processor I/O ports which drive the indicators and the digital display are simply wire OR-ed together by the connecting cable. Thus, either processor can keep an indicator on or ground one of the control leads to the display. The only indicators not wired in this fashion are the PROCESSOR ON LINE indicators, where each processor controls only its own, and the REQ PWR OFF indicators, where each processor controls the indicator for its mate. The keys, on the other hand, each have a separate contact for each processor. This prevents a fault in one processor from making it appear to the other processor that a key has been pressed.

VIII. *PROMUS*

The *PROMUS* reprogrammer is a piece of bench-top equipment (J1C144A) that programs or reprograms memory circuit packs used to

Table I—Programming time for *PROMUS* compatible memory packs

System	Circuit-Pack Type	Size	Approximate Programming Time
RSS	Program store	64K by 9	1.5 h
RSS	Processor B	8K by 9	12 min
RSS	Remote line test	6K by 8	8 min
PUC DL/DCT	Program store	16K by 9	25 min
PUC DL/DCT	Processor	8K by 8	10 min
PUC DL	Line interference CCIS	8K by 8	10 min
PROMUS	Program store	28K by 9	40 min

store firmware. Circuit packs containing EPROM devices to be updated must be removed from the RSS and first placed in the *PROMUS* reprogrammer's erase chamber. Ultraviolet (UV) light erases the old data in all the EPROMs. The new data to be programmed may be obtained from a remote computer via a dial-up data link, or may be copied from an already-programmed memory circuit pack. The sequencing needed to program each EPROM is performed by a control complex in the *PROMUS* using a *BELLMAC*-8 microprocessor. After the data are programmed, they are extensively verified.

The initial version of the *PROMUS* reprogrammer can program two circuit packs at once; the later version will provide eight programming slots. Because of the ease of reconfiguration, any of the circuit packs listed in Table I may be programmed. Other circuit pack types or systems may be added in the future. The set of signals at the edge connector of these circuit packs provides all the control necessary to individually program the many EPROM devices on a given circuit pack. This allows the *PROMUS* equipment to update firmware on a circuit-pack basis; there is no need to remove the devices from the board. A potential reliability problem is eliminated by not placing a large number of devices in sockets.

The erase operation requires 45 minutes, and may be done at the same time a pack in the programming chamber is being programmed or verified. Operations are invoked by typing commands on a hard-copy terminal connected to the *PROMUS* reprogrammer.

IX. CONCLUSION

The RSS processor complex has proven to have sufficient processing capacity and long-term reliability.

X. ACKNOWLEDGMENTS

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No. 10A Remote Switching System:

Peripheral Systems Architecture and Circuit Design

By J. M. ADRIAN, L. FREIMANIS, and R. G. SPARBER

(Manuscript received May 22, 1980)

This paper provides a general description of the circuits and units that make up the No. 10A Remote Switching System. The components of the system were designed to provide the operating and maintenance features of an electronic switching system, while keeping size, cost, and external equipment to a minimum. Fundamental new design approaches are described.

I. INTRODUCTION

The goal of this paper is to provide a general insight into the 10A RSS circuits and units making up the remote unit, with the exception of control which is covered in a separate article. These system building blocks are designed to provide the ESS features and maintenance desired while keeping size, cost, and external equipment to a minimum. Fundamental new design approaches important to obtaining these goals were pursued and are emphasized when encountered in the following sections.

II. LINE INTERFACE

Switching systems with metallic networks, such as ESS No. 1, 2, and 3 provide the battery feed and rotary dial digit collection functions on a concentrated basis. The architecture of the RSS and the nature of its network require a circuit incorporating these functions at each line appearance (see Fig. 1). It is the purpose of the line interface to implement those functions efficiently and economically.

The major problem with adapting a conventional battery feed ar-

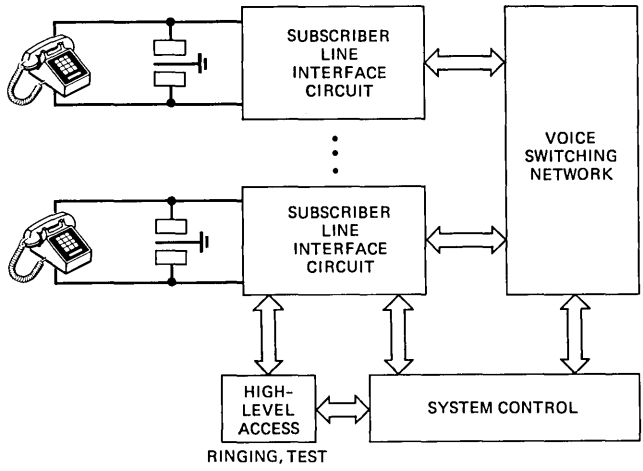


Fig. 1—RSS line interface.

rangement for RSS is heat dissipation. Eight such circuits feeding short loops may dissipate over 30 watts and, if densely packaged, require elaborate cooling facilities. Another requirement unique for RSS line interface is protection of the rather fragile network from hostile outside plant interferences, such as lightning and power crosses. Furthermore, the supervisory functions must be performed in face of substantial 60-Hz longitudinal induction.

The line interface circuit developed for RSS dissipates no more than 650 mW, and because of its floating nature is immune to longitudinal interference. Lightning protection for the network is provided by an isolating voice frequency transformer, voltage limiting semiconductors, and the junctor structure of the network itself.

The dramatic reduction (see Fig. 2) of heat dissipation is achieved by using a compliant floating power converter. The converter has three modes of operation. In the full-power mode, it supplies controlled current to the microphone and *TOUCH-TONE** service oscillators, collects rotary dial pulses, and supervises switch hook signaling, and generates a voltage proportional to loop resistance used for transmission compensation. The maximum current supplied on zero loop is based on a comprehensive study of the effect of loop current on transmission/grade of service (Ref. 1), and the converter maintains this current when the battery voltage drops during commercial power failure. Most of the time, however, the subscriber's station is on-hook, and the system is waiting for a service request. To conserve energy

* Registered service mark of AT&T.

	CONVENTIONAL 2 x 200 Ω	CONVERTER
MAXIMUM LOOP LENGTH 48 V BATTERY	1600 Ω	1600 Ω
WORST-CASE HEAT DISSIPATION	4.2 W	0.65 W
AVERAGE BATTERY POWER	2.3 W	1.4 W
LOOP CURRENT RANGE	100-23 mA	42-23 mA
ORIGINATION MODE POWER	0	50 mW

Fig. 2—Performance comparisons between conventional battery feed and RSS line interface.

and reduce heat dissipation, the converter is put into a low-power origination mode consuming only about 50 mW.

During ringing and loop testing, the audio and battery feed must be disconnected from the loop. This is accomplished by stopping the converter and allowing the disconnect thyristor to open (Fig. 3). Twenty-Hz ringing is then applied from a common bus via dry reed relay contacts. There are two such relays for each line interface circuit to accommodate ringing in the busy hour, as well as line testing. The relays are controlled by the system via latches and relay drivers on a per-line integrated circuit. This integrated circuit (IC) also controls the

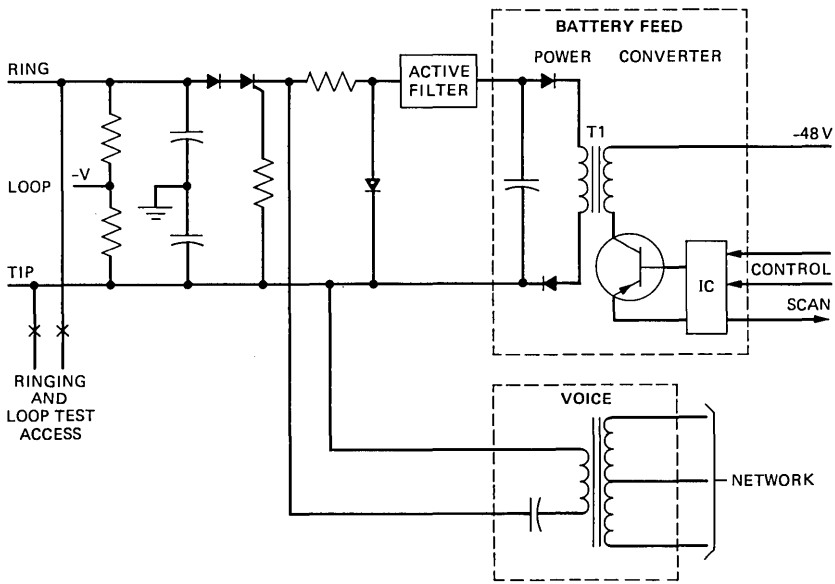


Fig. 3—Functional schematic of RSS line interface circuit.

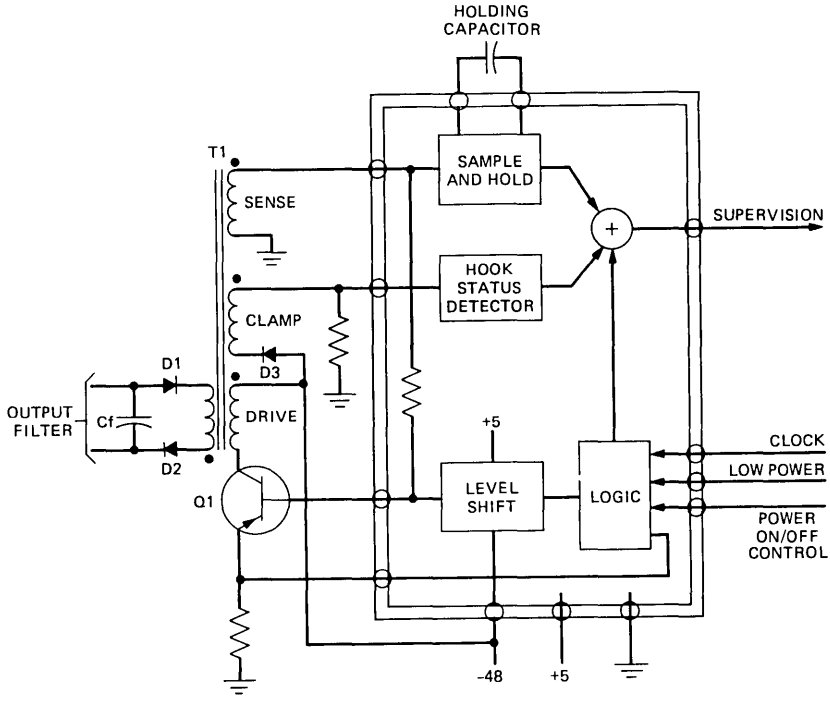


Fig. 4—Block diagram of the converter IC.

states of the converter, participates in the network path set up, and multiplexes the supervisory information onto the data bus.

Another integrated circuit (Fig. 4) controls the switching transistor in the power converter. In the full power mode with the switching transistor on, a linear current ramp is generated in the drive winding and energy stored in the magnetic field of the pulse transformer. Output rectifier diodes are reverse-biased, and base drive to the switching transistor is supplied by the sense winding. The ramp is terminated at a predetermined level by the comparator via a level shift circuit. Voltages on all windings reverse and the stored energy discharges into the filter capacitor and the loop. When the discharge is complete, voltages reverse again and the negative swing on the sense winding initiates a new cycle.

An equilibrium condition is imposed by the equal voltage-time product requirement on the output winding, and establishes an average voltage on the filter capacitor unique to the loop resistance. A scaled version of this voltage is sampled on the sense winding and held on the holding capacitor. An appropriate fraction of this voltage is applied to the scan point and multiplexed to the data bus.

In the full power mode, the converter frequency becomes a function of the loop resistance and varies between 40 and 90 kHz.

When the loop resistance increases above 2000 ohms, the positive and negative voltage excursions on the output winding become equal in amplitude, and the converter enters into a clamp mode. Excess energy is returned to the battery during the discharge cycle, and the peaks of the return current pulses are sampled by a comparator, which triggers a timer and activates a pull-up current source on the scan point whenever the loop resistance is above 7000 ohms, indicating a break in the rotary dial pulse or a switchhook signal. In the low-power origination mode, current has to be supplied only to loop leakages and the control of the converter is transferred to a low-frequency clock. Power dissipation is further reduced by disabling part of the level shift circuit between clock pulses. Negative bias for the level shift circuit is derived from the −48 volt battery by an on-chip isolated zener diode string. The pull-up source in this mode is kept active by the voltage on the hold capacitor. When service is requested by closing the loop, this voltage drops, trips the comparator and deactivates the source. The supervisory trip point in this case is considerably higher than in the full power mode (see Fig. 5). This feature eliminates the need for a pretrip test before 20-Hz ringing is applied. Ring-trip supervision during the silent intervals will be performed by the line circuit in the full power mode with reduced sensitivity to loop leakages.

The presently used line interface circuit in RSS (see Fig. 6) has been designed for a maximum loop resistance of 1600 ohms. An extended range can be readily accommodated by adjusting the turns ratio on the pulse transformer.

III. VOICE NETWORK

The main switch in the remote switching system is the voice network. It is an electronic space division network using PNPN semiconductor crosspoints for two-wire balanced audio transmission. Thirty-two PNPN crosspoints are fabricated on an integrated circuit. The network is formed from these PNPN ICs interconnected with a junctor circuit at the center feeding bias current to maintain active network paths. Specialized integrated circuits have been developed for network terminal control and to form the junctor circuit. Several alternative network technologies, including time division, were considered for RSS during its design. None was found superior to the design presented here with respect to size, cost, growth characteristics, or power.

3.1 The PNPN

A PNPN is a silicon device consisting of four alternate *p*- and *n*-semiconductor regions. A more common name, usually applied to

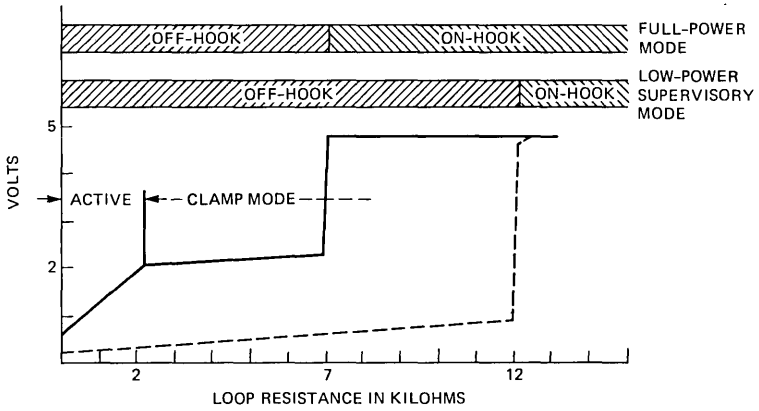


Fig. 5—Voltage levels on scan point.

higher power devices, is the silicon controlled rectifier or SCR. Two transistors may be interconnected as in Fig. 7 to simulate the device. For use in RSS, a series gate diode to simplify control and an anode-to-gate resistor to reduce transient turn-on susceptibility are added. Like an SCR, if current is drawn anode-to-gate, while current is flowing anode-to-cathode, the gate current may be removed and the PNPN will continue to conduct anode-to-cathode. Since no other state storage device is used, this effect is called self-latching. Thirty-two PNPN elements—the PNPN, gate diode, and anode-to-gate resistor—are formed on a common integrated circuit[2] in a 4 by 8 array shown in Fig.

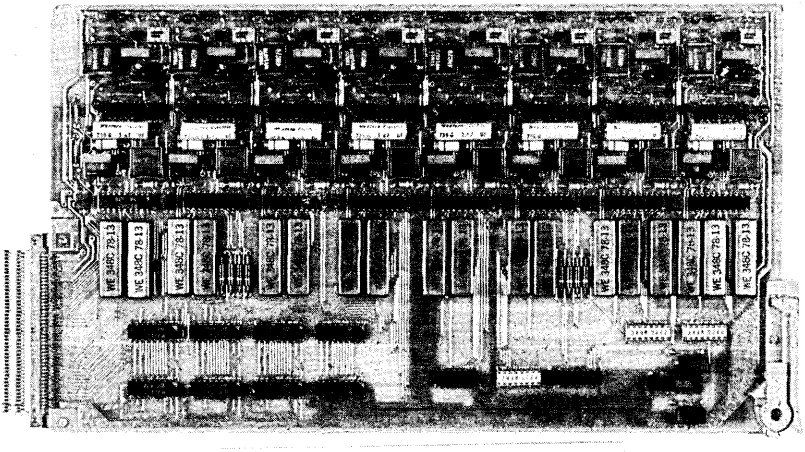


Fig. 6—FE101 line interface circuit pack.

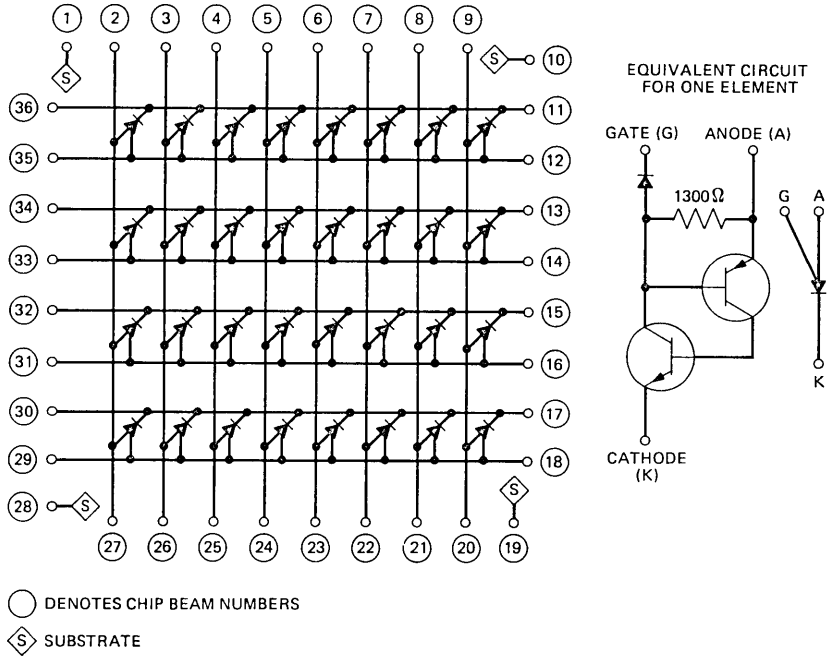


Fig. 7—Equivalent circuit of the PNPN array.

7. The conductor common to eight-gate diodes is called the diode rail. Table I shows the RSS PNPN to have reasonable on-resistance and off-capacitance parameters. This corresponds to low loss and crosstalk. This PNPN was also designed to have very low ac signal-to-substrate

Table I—Electrical properties of the PNPN array

Characteristics and Conditions	Typical (T = 25°C)	Units
DC Cathode-substrate leakage current (Iak = 0, Vak = 35 V)	0.6	μA dc
AC Cathode-substrate leakage current (Iak = 10 mA dc, Iak = 10 mA peak-to-peak, Vas = 20 Vdc)	0.03	μA pp
Forward leakage (Vak = 30 Vdc, Vks = 0 V)	0.01	μA dc
Reverse leakage (Vak = 30 Vdc, Vks = 0 Vdc)	0.01	μA dc
Gate-anode leakage current (Vag = 30 Vdc, Vas = 0 V)	0.01	μA dc
On-resistance (Iak = 10 mA dc)	9.0	Ω
Forward voltage (Iak = 10 mA dc)	0.9	Vdc
Holding current	1.1	mA dc
DC gate trigger voltage (Vak = 20 Vdc)	1.35	Vdc
DC gate trigger current (Vak = 20 Vdc)	0.6	mA dc
Anode-to-cathode capacitance (Vak = 20 V)	1.0	pF

Iak = Current anode-to-cathode
Vak = Voltage anode-to-cathode
Vas = Voltage anode-to-substrate
Vks = Voltage cathode-to-substrate
Vag = Voltage anode-to-gate

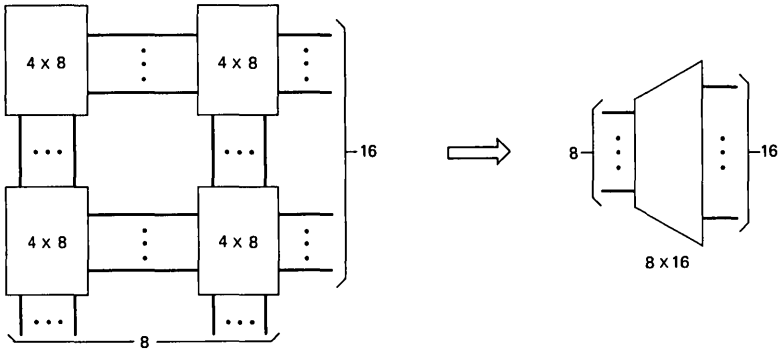


Fig. 8—Construction of line interface pack 8 x 16 switch.

loss—a common problem in this type of device—to keep loss variation negligible.

3.2 Topology, partitioning, and growth

The RSS voice network topology is quite rich especially in the first stage with 68 percent of the total crosspoints. This is possible because of the low cost and small size of the PNPN crosspoint used, but is enhanced by a network partitioning that allows the first stage to be equipped only as needed. Good traffic handling capabilities have resulted while rearrangement of line appearances, because of the possibility of high traffic lines tying up a first-stage switch, have been minimized.

Each line interface pack, LI, in RSS has an 8 by 16 expansion stage made from the 4 by 8 PNPN ICs, Fig. 8. Two-wire balanced transmission

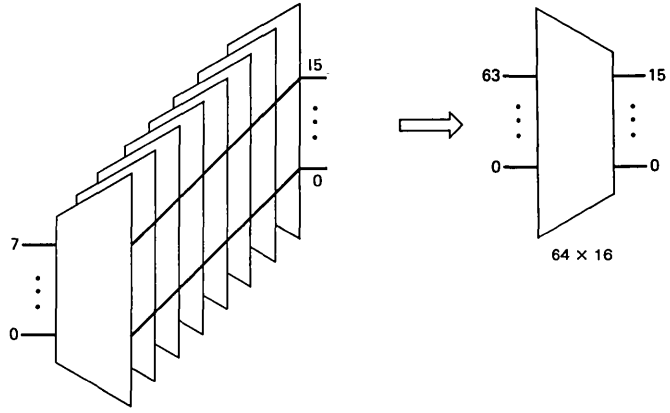


Fig. 9—Construction of 64 x 16 first-stage switch using multiple line interface pack 8 x 16 switches.

is used in the network so each lead shown is physically a pair of wires and each 4 by 8 switch is actually two 4 by 8 PNPN ICs. The network leads between the first and the second stage are called links. A full 64 by 16 first-stage line concentrator is formed by parallel connections of the links of 8 LI pack 8 by 16 switches, which are physically adjacent, as shown in Fig. 9. Carrier interface, (CI) packs use a similar arrangement of four 4 by 16 switches to form a 16 by 16 switch.

A full 512-line RSS network with two-stage folded topology is shown in Fig. 10. The first stage is made up of the CI, LI, and receiver off-hook (ROH) packs with the second stage formed from the 16 by 16 switches on the grid-junctor (G-J) pack. *TOUCH-TONE* service packs are not

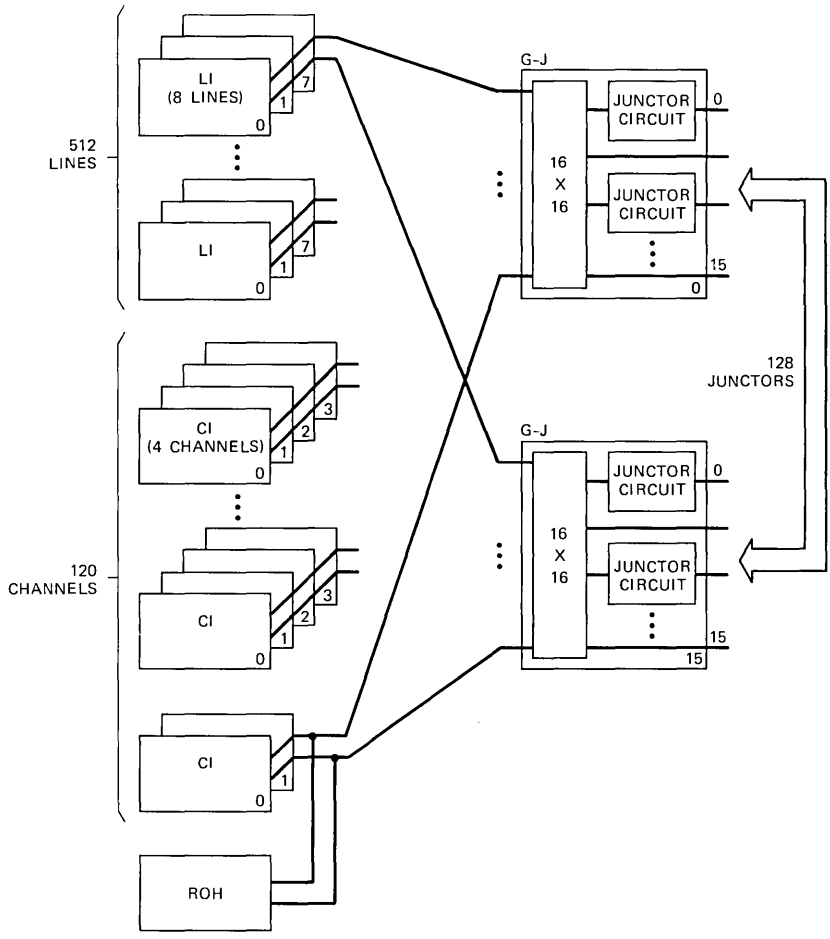


Fig. 10—Network configuration for up to 518 lines.

shown, but multiple onto the last CI switches. A path through the network is folded in that it always passes through a first-stage switch, a second-stage switch, a junctor circuit to bias the path, then back through a second-stage and first-stage switch. A complete junctor circuit is on each even appearance of the 16 by 16 second-stage switch, while odd appearances have no junctor circuit. The interconnection of the 16 by 16 switches is by leads, called junctors, that always connect an even switch appearance to an odd, including one complete junctor circuit in each junctor.

Growth of the network beyond 512 lines requires use of Build-Out Switch (BOS) packs that enlarge the second-stage switches from 16 by 16 to 24 by 24 and include extra junctor circuits on all even junctor

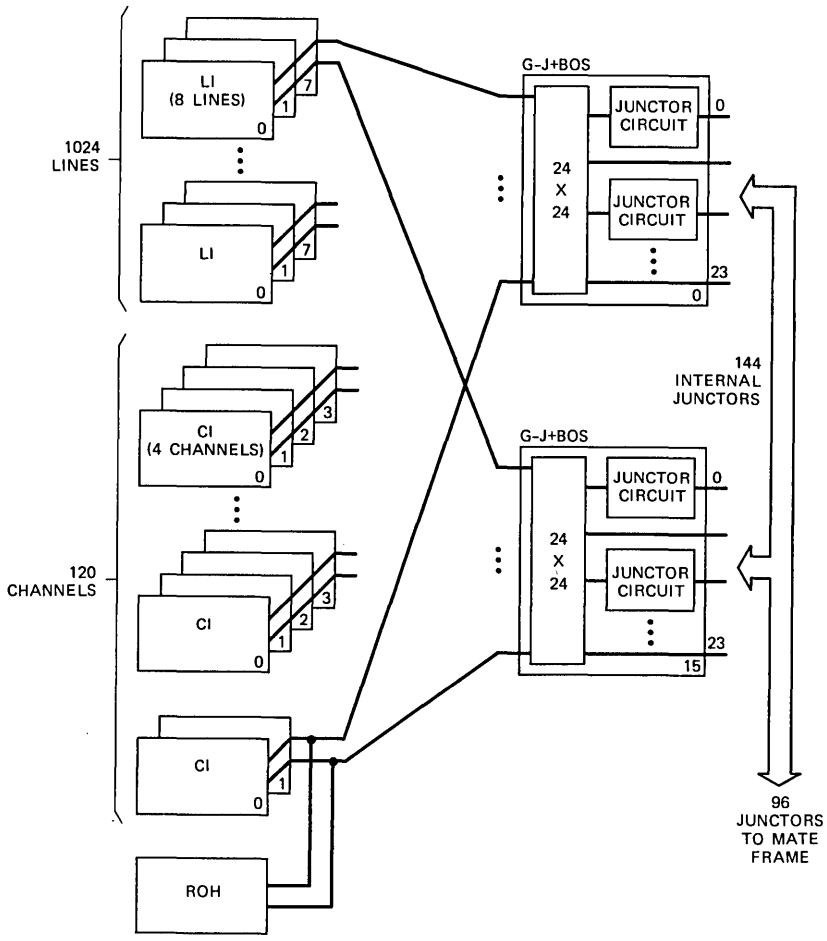


Fig. 11—Network configuration for up to 1024 lines and interconnect to optional mate frame.

appearances, as shown in Fig. 11. This expansion allows growth to a full single mod frame capacity of 1024 lines and extra junctors to interconnect to a 1024-line RSS mate frame with an identical network yielding a network growth limit of 2048 lines.

The RSS network traffic limit for the line-to-line calls is shown in Fig. 12 for a single frame. This curve assumes deloading line appearances by not equipping all 64 lines in a line concentrator to gain extra traffic capacity.

3.3 A PNPN voice network path

A line-to-line network path is shown in Fig. 13. In an active stable path, all current sources in the used junctor circuit are on with current from them passing through the on or active PNPNs to be sunk by the line-audio coupling transformer center taps. Many PNPNs are not shown that connect from this active path to other lines, but they are all off. The diode rails from the used PNPNs are at a high potential such that no gate current is sunk. The PNPNs in the active path are held on or latched only by the current bias from the junctor circuit. At least the current from one hold current source (I_{HA} or I_{HB}) will always flow through each PNPN in the path because of the diodes in the junctor circuit. A pair of coupling capacitors in the junctor circuit center allows for small dc voltage offsets in the path.

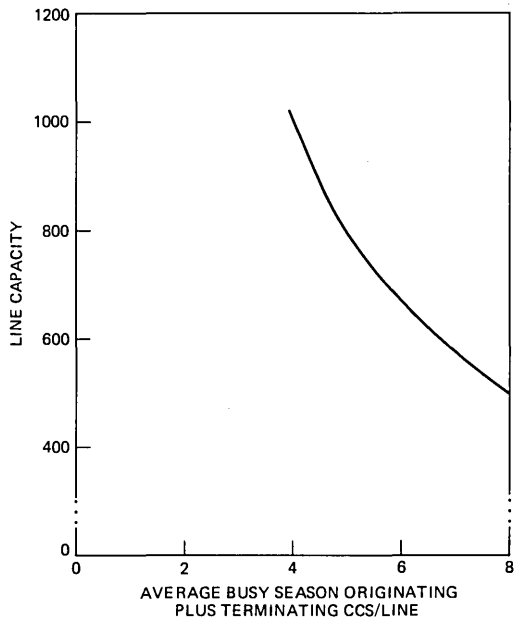


Fig. 12—Remote switching system line capacity—one-module RSS.

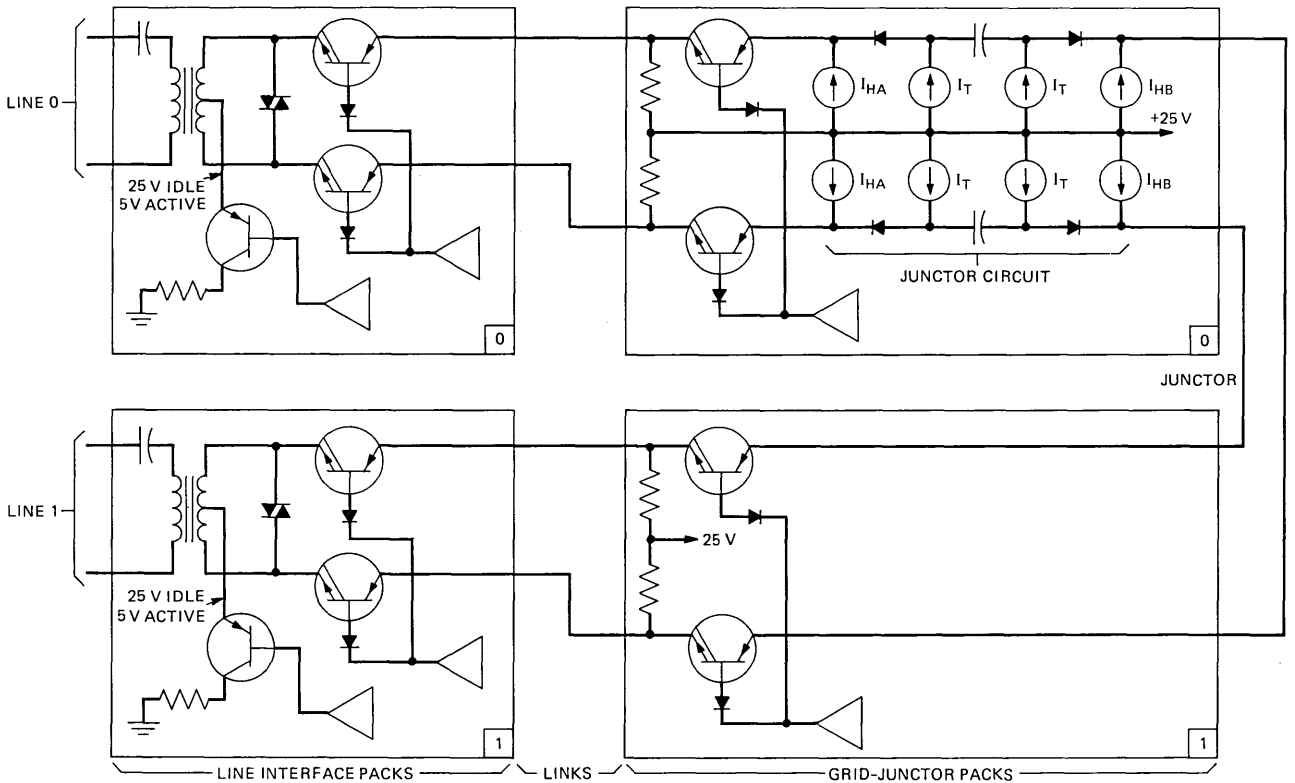


Fig. 13—A line-to-line network pass.

Path setup starts at the junctor circuit where the hold and talk sources are controlled as three separate groups: I_{HA}, I_{HB}, and I_T. Initially, all points in an idle path are at a high potential and all junctor circuit current sources are off. The path is set up in halves working from the junctor circuit. Starting, I_{HA} is enabled, the two diode rails are sequentially operated to their lower potential, and then the audio coupling transformer center-tap is lowered on line 0. The operated diode rails are now released. Repeating the process from I_{HB} through G-J pack 0 to line 1, two half paths are constructed. Finally, the talk sources, I_T, are enabled to complete the audio connection. Since the path potential is now controlled by the center-tap 5-volt potential, other paths may be constructed without interference with this path. All diode rail and center tap control potentials are ramped to eliminate parasitic coupling between paths momentarily canceling active path current and dropping paths.

To release a network path connection, talk sources are disabled, transformer center-taps are brought back to a high potential, and hold sources are disabled.

3.4 Network support circuitry

Associated with the network path is the control, current bias, and maintenance circuitry. In RSS, this circuitry has been integrated where practical. Check circuitry is included to detect faults and localize them.

At the network terminals—a line, channel, or other network point, a special bipolar IC is used incorporating a form of I^2L logic and analog interfaces.[3,4] This IC has many functions as discussed in Section II; however, here its important capabilities are controlling the 25-volt potentials of the voice network center-tap and diode-rail of a network terminal. Also, this IC repeats the bias current from the center-tap through a resistor and can repeat the developed potential to the fanout pack. This point is examined for no bias before path construction is initiated, after the center-tap is brought low for hold bias, and before a path is torn down for hold, plus talk bias.

The junctor circuit of RSS is made with a special bipolar IC also. Two of these ICs, plus two capacitors make up each junctor circuit exclusive of control. This IC, shown in simplified form in Fig. 14, contains the hold sources, talk sources, and diodes. A hold scan point is included which indicates three states: hold source off; hold source on and supplying current; and hold source on and not supplying current. The talk current sources are modified to appear as an ideal current source with a negative resistance to ground. This negative resistance cancels some of the line circuit and network losses to yield a typical 0.5-dB loss line-to-line.

Each G-J and BOS pack also contains control logic and diode rail

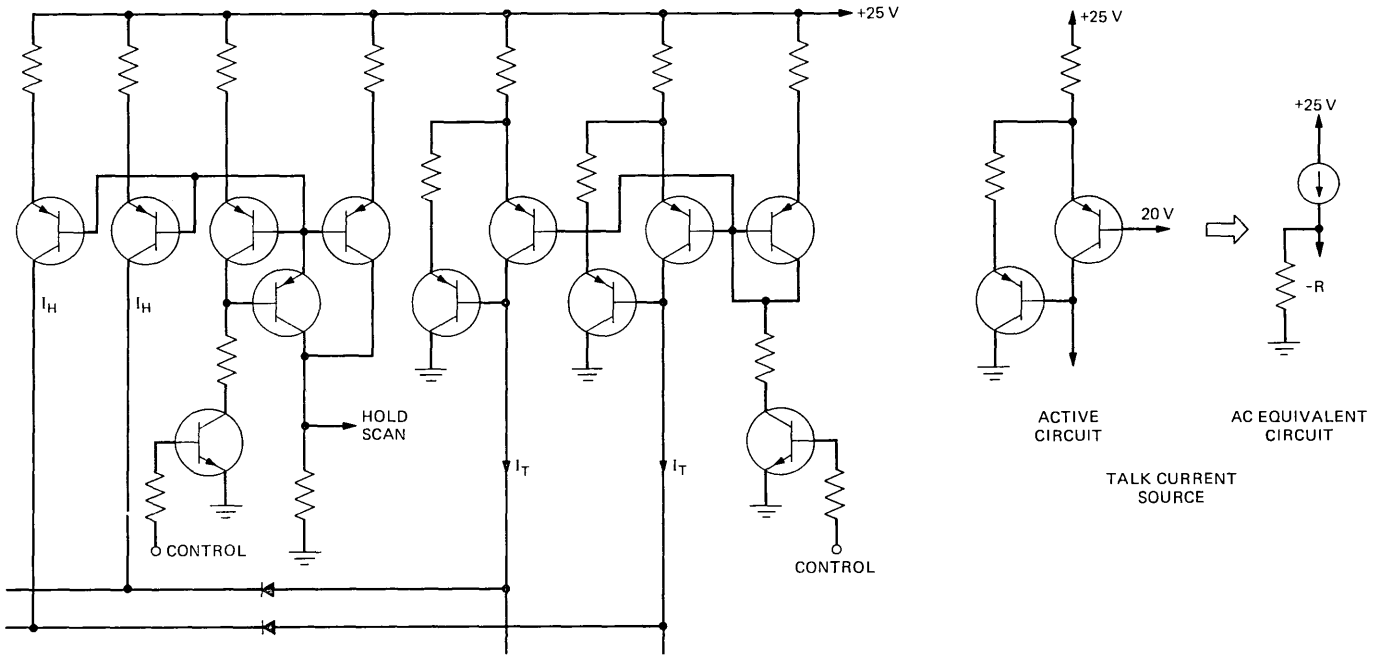


Fig. 14—Junctor circuit diagram and implementation of negative resistance.

drivers. The latches that contain the state of the diode rail driver and talk sources may be read back to the fanout pack. Circuitry to guard against system malfunctions clears any diode rail after 100 ms and will not allow the hold B sources to be enabled before the hold A sources.

IV. UNIVERSAL SERVICE CIRCUIT OVERVIEW

The Universal Service Circuit (USC) performs customer line functions which cannot be performed through the ac-coupled low-power electronic network of RSS. Figure 15 shows a photo of the USC which is, in essence, a 15-watt dc-dc converter with current sense on its outputs. It can supply ringing, coin control, party test, and test for power cross on a line among other functions. Each line circuit in RSS has two metallic reed relays which connect to a group of four USC packs which contain a second stage of switching.

The USC combines functions which have been performed by a number of separate circuits in previous ESS systems. Also, the USC, and its associated metallic connection to a line, is only used during the actual high-power interval of the line function—for instance, when ringing is applied, but not during the silent interval between rings. This combination of functions and time-divided usage allows for far fewer USCs than would be required using more dedicated circuits and a reduction in high-level network size. The high-level network is also used to gain metallic access to the line through the USC for several low-occupancy test circuits.

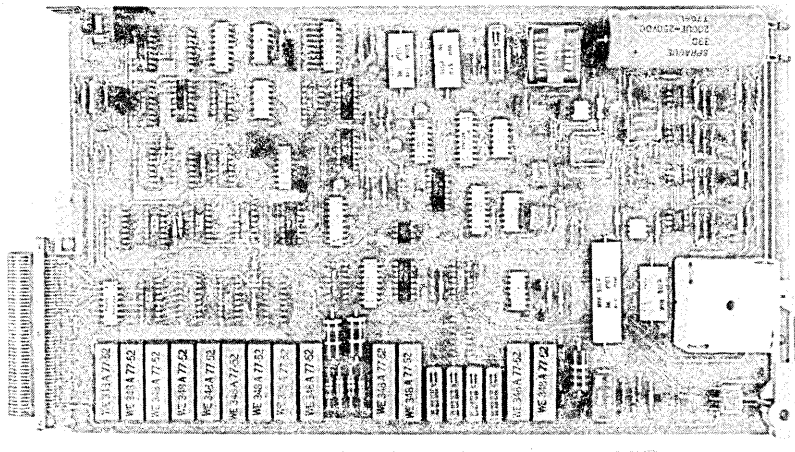


Fig. 15—Universal-level service circuit circuit pack.

4.1 Universal service circuit description

Figure 16 is a functional representation of the USC pack. The USC supplies dc output voltages of ±150 volts in increments of 10 volts from a switching mode amplifier voltage source under control of a fanout pack. The current is limited to ±125 mA from the amplifier by an optically coupled overcurrent sensing circuit. This protection is provided for both directions of current. The ac ringing voltage of 88 volt rms 20 Hz may be superimposed on any selected dc output voltage up to ±80 volts. The amplified voltage is then applied to one of the eight possible high-level metallic access buses through selectable output impedances of 200 ohms, 2 kilohms, or 20 kilohms. Voltage and ground may be applied on either tip or ring. Two test-access ports are also available for those test circuits that require metallic access to lines.

The USC packs can also measure voltages to ±200 volts and currents to ±80 mA. Voltage is directly fed as a fraction of the voltage present to the fanout pack for interpretation. Current measurements may be either single ended, metallic current on either the tip or ring, or differential current on both tip and ring. An analog voltage linearly proportional to the measured current is passed to the fanout with two full-scale sensitivities: ±120 mA and ±80 mA. Digital current thresholds are also available with different sensitivities and different degrees of low-pass filtering.

±10 mA fast (2-ms response)
±10 mA slow (30-ms response)
±10 mA very slow (100-ms response)
−4 mA slow (30-ms response)
−4 mA fast (2-ms response)

Fast-response digital current threshold measurements are used for such functions as power cross detection and ringing current continuity detection. Slow-response thresholds are for such functions as two-party line tip party identification and coin-phone coin-presence tests. Very slow scan points are used for ring-trip.

A high-impedance voltage detector is used to verify connection integrity whenever a metallic access relay on the USC is operated. If another line is connected to this bus inadvertently by control or by a circuit fault, closing another line relay to this bus could result in a short-duration, large current flow, while charge redistribution between the lines takes place. This could damage the dry reed relay that is last to operate. If the detector finds a significant voltage, the function in progress by the USC is halted and attempts are made to clear the unwanted connection before relay damage can occur.

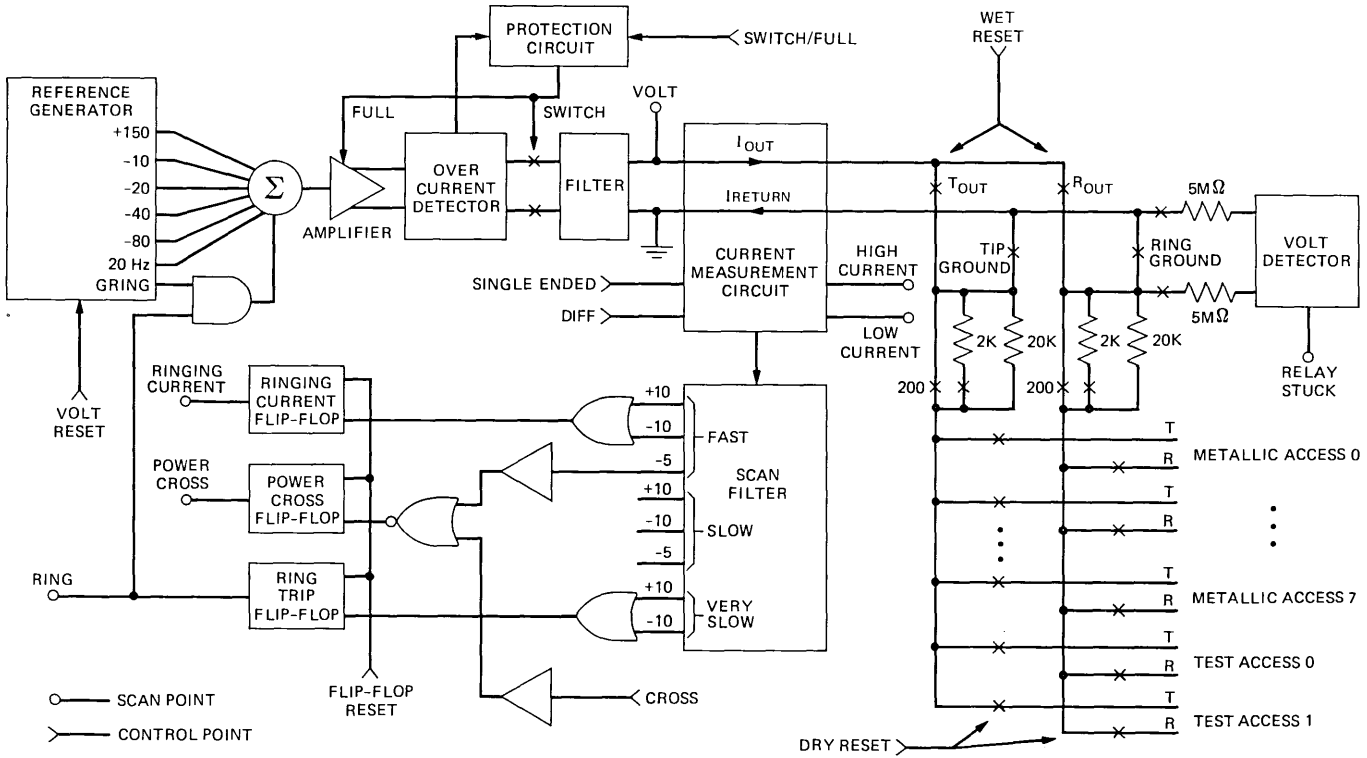


Fig. 16—Universal service circuit block diagram.

4.1.1 The usc voltage source

Figure 17 is a diagram of the USC voltage source. An initial dc-dc switching converter steps up the −48 volt RSS supply voltage to 200 volts. This is followed by the ±125 mA overcurrent detector which shuts down the circuit during overload. The optically coupled bridge switch couples the 200-volt source to the output filter. Depending on the duty cycle of oppositely paired transistors, any voltage up to ±200 volts will be available at the output. The output is heavily filtered with a Balun transformer and capacitance to allow switching mode conversion and eliminate output voltage transients.

To control the bridge switch, a triangular wave is compared to the output of the programmable reference signal generator. One pair or the other pair of transistors in the bridge switch is enabled depending on whether the reference signal is greater or less than the triangular signal. Turn-on delay is added to the control circuitry of the bridge switch to ensure that only one pair is turned on. Otherwise, a short would be placed across the 200-volt supply. The USC voltage source has been described here as a programmable power supply, but it could, just as well, be considered a low-frequency dc-coupled amplifier for the reference signal generator.

4.1.2 The usc current sense circuit

The USC current sense circuit, shown in Fig. 18, uses toroidal ferrite coils to provide isolation from the large voltages present at times on the measured conductors. It is a differential, or metallic, current measurement device as shown, but it is also used as a longitudinal current sensor by bypassing tip or ring current around the device.

The current sense circuit relies on a clock signal to saturate the drive transistor. This provides a current through the drive windings large enough to saturate both toroids and drop their permeability substantially. When the clock signal is removed, the toroids recover from saturation with a large increase in permeability. Any current flow through the tip and ring windings will generate an increase in magnetic field that will induce a current in the sense winding. The sense winding is sampled at this time by a JFET enabled by release of the drive winding, and an inverting integrator begins to supply a current in the sense winding of opposite polarity to that induced by the tip and ring windings. Equilibrium is reached when the integrator provides a current to the sense winding that will provide a field exactly opposing that generated by the tip and ring windings. The integrator amplifier output is then a direct function of tip and ring current. Two toroidal cores are used so that the drive signal is canceled in both tip and ring and in the sense windings.

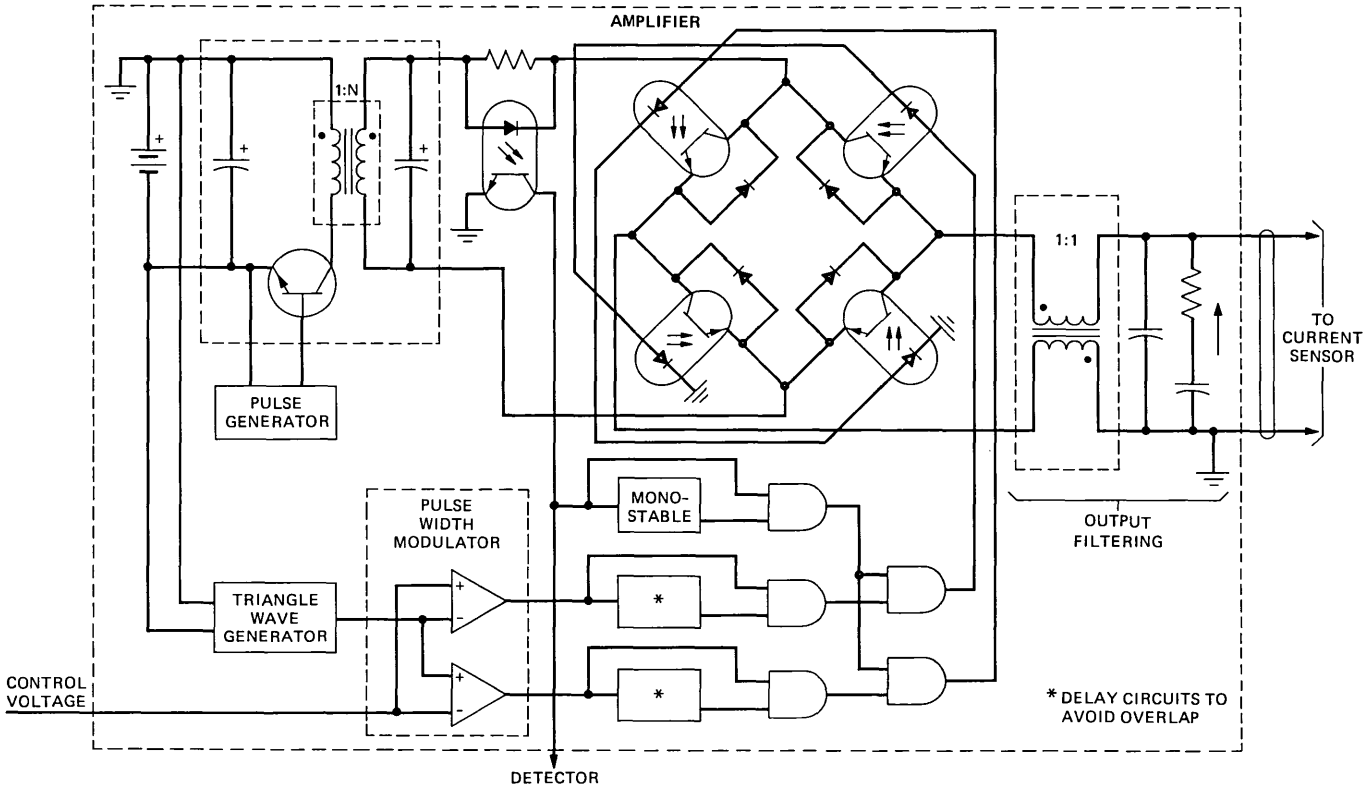


Fig. 17—Universal-level service circuit voltage source.

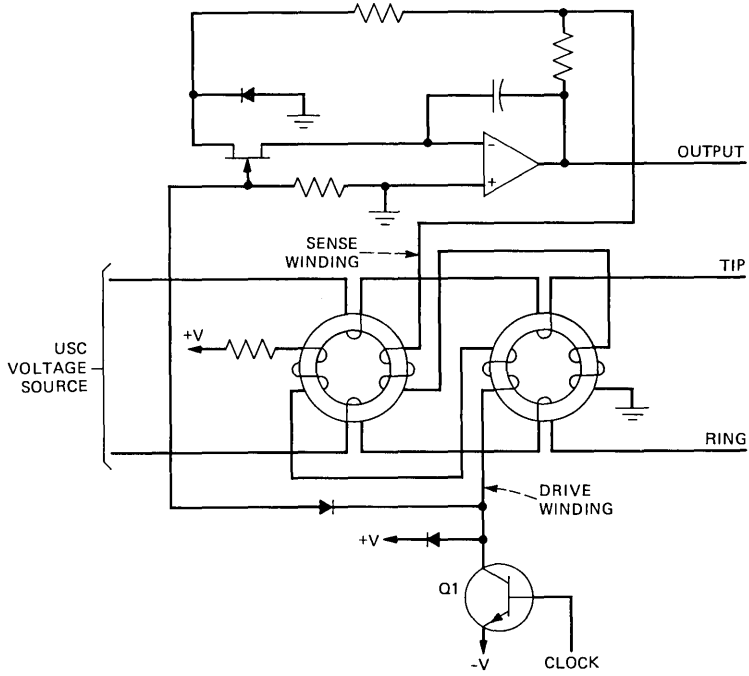


Fig. 18—Universal-level service circuit current sense circuit.

4.2 Metallic access network

The RSS metallic access network is based on a shelf serving 256 lines (Fig. 19). Each line has access to an A and a B bus connecting to two groups of USC circuits. All high-power line functions or test functions requiring metallic dc-coupled line access must use this network. Table II outlines these functions and categorizes them according to actual time required per usage. Because the only function requiring a long holding time was manual loop testing and since this is a very slow occupancy function, the usage of the metallic access network was time-divided.

Figure 20 shows the timing of the metallic access network for one possible very busy bus. In a given bus cycle of 6.9 seconds, three 2-second periods are allowed for functions no longer than 2 seconds. A sample of functions that might occur on a very busy bus is shown. Code-1 ringing (nominally 2 seconds on and 4 seconds off) is easily accomplished with a slight lengthening of the silent interval. The line is supervised by the line circuit during the silent interval before the next ringing interval or ring-trip. Code-2 ringing used for multiparty lines (nominally 1 second on, 1 second off, 1 second on, and 3 seconds off) is compressed to 0.7 seconds on, 0.6 seconds off, 0.7 seconds on

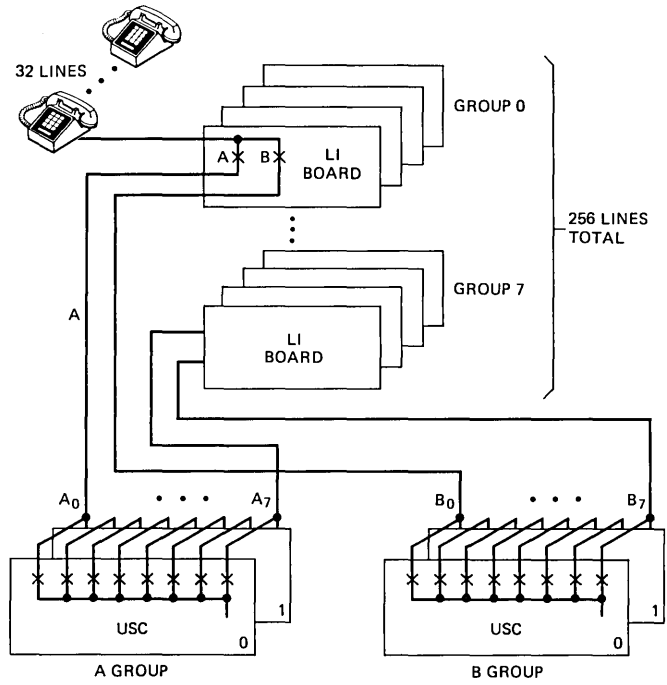


Fig. 19—Metallic access network.

and 5 seconds off. A human factors study of the modifications made to code-1 and code-2 patterns was conducted and both codes were found to be satisfactory. The timing of the other functions shown was not affected by time dividing the metallic buses.

With fixed periods for ringing and test functions, the A and B bus groups are run 1.15 seconds out of phase to reduce the average delay of a line receiving metallic bus access. To further reduce delays, test functions will be performed during a bus period if enough time remains

Table II—High-level signaling and testing functions

Holding Time on the Bus		
Short (less than 0.33 s)	Long (less than 2 s)	Continuous
Power cross test*	Single-party ringing‡	Manual loop testing†
Party test*	Multiparty ringing‡	
Coin presence test*	Coin collect or return*	
	Interface circuit testing†	
	Automated loop testing†	

* Low traffic, no delay acceptable.
† Very low traffic, substantial delay acceptable.
‡ Repeated periodically, high traffic, one period of delay acceptable.

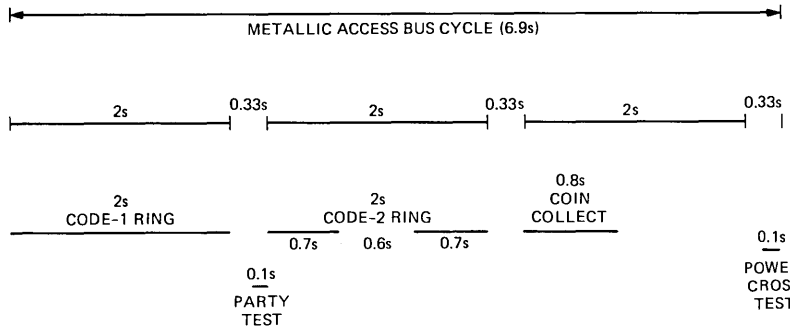


Fig. 20—Metallic access network timing.

even though the period has begun and code-1 ringing will begin if at least half the 2-second interval remains.

Blocking and delay in the metallic access network has been studied with a summary of the results shown in Table III. A bus occupancy corresponding to 0.3 CCS/line was used which is three times the average busy-hour usage expected to allow for peaking. With both buses available, service is excellent with accceptable service still offered during the low-probability period of one bus being out-of-service or used for manual testing. Manual testing is denied to a group of 32 lines that has a bus out of service.

V. CARRIER INTERFACE

All voice connections, supervision, and data between the host ESS and RSS passes over carrier. No provision is available for metallic facilities linking the two since degradations in the audio signal transmission over metallic facilities would be very difficult to overcome.

Two types of carrier interfaces may be provided: a T1 digital carrier interface and an analog carrier interface. The T1 carrier interface is entirely self-contained in the RSS. In many cases, no external T1 carrier

Table III—Metallic access network blocking and delays

	Simultaneous Time Slots		1.15-s Staggered Time Slots	
	Normal	1 Bus Out	Normal	1 Bus Out
Probability delay greater than next time slot	0.005	0.11	0.07	0.11
Probability delay greater than next time slot +1.1 s	—	—	0.005	—
Probability of blocked ringing	$<10^{-7}$	0.0013	$<10^{-7}$	0.0013
Average ringing delay (s)	1.15	1.5	0.68	1.5
Average 2-party dial tone delay (s)	0.06	0.17	0.05	0.17
Probability of blocking a 2-time slot reverting call	10^{-5}	0.034	$<10^{-4}$	0.034

or transmission equipment will be required at the RSS location. In about a third of the RSS applications, however, the use of other carriers is more attractive than T1. This may be because of the reuse of existing equipment or other incompatibilities. In these cases, the analog carrier interface provides a universal 4-wire interface to carrier equipment external to the RSS.

The two carrier interface types may be mixed in a single RSS as groups of 24 channels. Full compatibility is provided in that the two types plug into the same frame locations and are fully control-compatible. Up to 5 of these 24-channel groups may be provided in a single-module 1024-line frame or 10 in a dual-module 2048-line application.

5.1 The RSS T1 carrier interface

The RSS uses 24-channel T1 digital carrier with standard 8-bit μ-255 law Pulse Code Modulation (PCM) voice encoding. A shared coder-decoder (CODEC) is used with a good portion of the circuitry originally developed for the D4 channel bank.[5] Each 24-channel digital group (DIGROUP) is packaged on eight 3/4-inch-spaced circuit packs. Since up to 5 DIGROUPs may be equipped in a single RSS frame, this DIGROUP compactness is a necessity.

Shown in Fig. 21 is a single DIGROUP from RSS to the host ESS. The

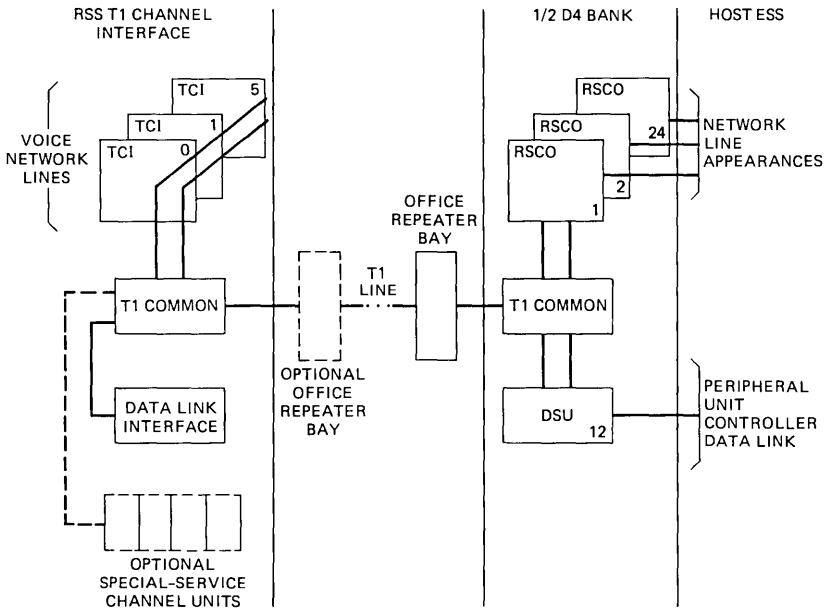


Fig. 21—No. 10A RSS T1 carrier connection for a single DIGROUP.

T-Carrier Interface (TCI) multiplexes up to 24 samples from the voice network links and their associated supervisory state. The T1 common circuitry encodes this information into a 1.554-Mb serial bitstream and drives the two-pair T1 line. Office repeater bays which normally terminate a T1 carrier line are not required at the RSS location if the T1 line span from the last office is not too long to be powered by that office. This distance can be up to 20 miles and will be the normal case when using RSS in a small minihut.

At the host RSS, an office repeater bay is required to interface to the line. A D4 channel bank is then used to decode the T1 signal. A special channel unit called a RSCO (RSS Central Office End) has been designed which has more gain and a different hybrid balance network compared to other standard channel units. Functionally, this unit converts the four-wire transmission of the carrier to the two-wire transmission of the host ESS and provides a supervisory loop closure in the two-wire path. No supervision is detected or transmitted from the host ESS to RSS.

Each of the first two DIGROUPS in RSS also carry a data link, for the control of RSS from the host, and optional special service channels. The data link interface uses channel 12 of each DIGROUP with the TCI disabled for this channel. At the host, a data service unit DSU data port is placed in the D4 bank channel unit position 12 to interface the data channel to the peripheral unit controller data link port of the ESS. As an RSS frame option, cabling may be included to use the last four channels of the first two DIGROUPS for special-service access to the T1 carrier instead of RSS voice channels. In this way, a small number of special services, such as foreign exchange lines, may be provided at an RSS location without having additional carrier equipment. Standard D4 bank channel units are used both in RSS and in the host D4 bank to handle these services.

An RSS T-carrier DIGROUP is shown in Fig. 22. Only three pack codes are used with all the T1 common functions contained on the Transmit-Receive (TR) pack and the Alarm and Line Interface (ALI) pack.

5.1.1 The alarm and line interface

An ALI pack receives the balanced 1.544-Mb T1 line self-clocked bipolar signal. Automatic gain control allows for varying line loss while an inductor-capacitor tank circuit recovers the clock and data. This pack must also generate the T1 line signal transmitted from RSS. In this direction, one of several different networks on the pack are enabled with different backplane options on the connector pins. These networks attenuate and shape the line signal when office repeaters are used with RSS and allow for three different cabling distances. The T1 carrier line dc current, used to power line repeaters, may be looped

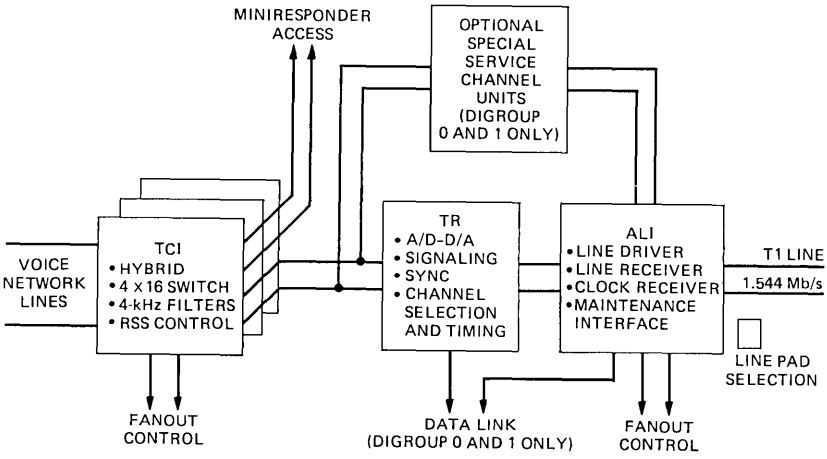


Fig. 22—No. 10A RSS internal T1 carrier interface.

through isolation transformers in the ALI to maintain a sealing current for splices even though no part of the ALI is powered from the T1 line.

Alarm and trunk processing status of the DIGROUP is indicated with LEDs on the ALI. A red alarm from the TR pack, indicating loss of synchronization, is displayed and passed onto control. A yellow alarm, indicating a red alarm at the host for this DIGROUP, is found by integrating a signal from the TR and, if found, it is displayed and also passed to control. If either alarm is found, three relays are operated under program control to trunk process, i.e., place in a benign state, the special-service channel units.

Several clocks which run the DIGROUP are also derived on the ALI. The 1.544-MHz receive clock which is derived from the incoming signal has already been mentioned. A quartz-crystal-based 6.176-MHz clock to run the transmit portion of the TR is synchronized to the receive clock unless a red alarm occurs. Then it is allowed to run free. A third 64-kHz clock for the data link interface and special-service data units is derived from the transmit clock by a phase-locked loop circuit operating from signals from the TR.

5.1.2 The transmit-receive circuit pack

A TR pack contains the shared CODEC and control logic for a DIGROUP. Multiplexed Pulse Amplitude Modulation (PAM) is used to pass samples of the channel audio signals between itself and the TCIs.

The transmit coder performs a sequential sample-and-hold on the PAM sample of each of the possible 24 channels at an 8-kHz rate. This sample is first examined for sign and then a successive approximation analog-to-digital conversion is performed with the comparison level

formed from a thin-film-resistor weighting network. The 8-bit result is serially transferred to the ALI for transmission. In every sixth sample, however, the supervisory state of the channel is also sampled and inserted as the least-significant bit. After all 24 channels have been sampled, a single framing bit is added whose pattern allows the D4 bank receiver to synchronize on the incoming bitstream. If the receive portion of the TR pack is generating an alarm, another bit in each time slot is stuffed to signal the far end with a yellow alarm that a problem exists.

Instead of audio information, each time slot may also contain data. If a TCI does not respond to its enable signals for a time slot, the transmit circuit sends 8 bits of data present on a separate serial data input.

The receive circuit is functionally the inverse of the transmit circuit. Line data with the recovered clock from the ALI pack are examined bit-by-bit for the framing bit, and synchronization is eventually established. If synchronization cannot be established or is broken, an out-of-frame signal to the ALI results in a red alarm. To decode a receive time slot to audio, the 8 bits are directly converted from digital-to-analog using another thin-film weighting network and sent to the TCIs as a PAM sample. At the same time, the proper TCI channel is enabled to receive the sample. In addition, the bit carrying supervision is transferred to the channels every six frames and the bit carrying the yellow alarm is sent to the ALI for yellow-alarm detection.

If data are being sent for a channel instead of an audio sample, no special actions are taken by the receive circuit. The receive bitstream and clock are available to the data link interface pack and special-service channel units to enable extraction of data based on timing from the receive circuit.

5.1.3 The T1 carrier interface pack

The TCI is the first stage of conversion from the RSS voice frequency electronic network and control complex to the T1 carrier line. Each TCI pack provides four audio channels from RSS by including one stage of switching, transmission path conditioning circuitry, and conversion from voice frequency to PAM (Fig. 23). A 16 by 4 PNPN crosspoint switch connects the single transformer hybrid circuit of a channel into the voice network. The hybrid balancing network contains an inductor to balance out the shunt inductance of the hybrid itself and the line circuit transformer. To balance the line impedance, two different networks previously selected by the electronic line segregation circuit are used. In the four-wire portion of the circuit following the hybrid, 2 dB of loss may be added. This loss is inserted on short loops where *TOUCH-TONE* service signals may be clipped by the PCM encoding

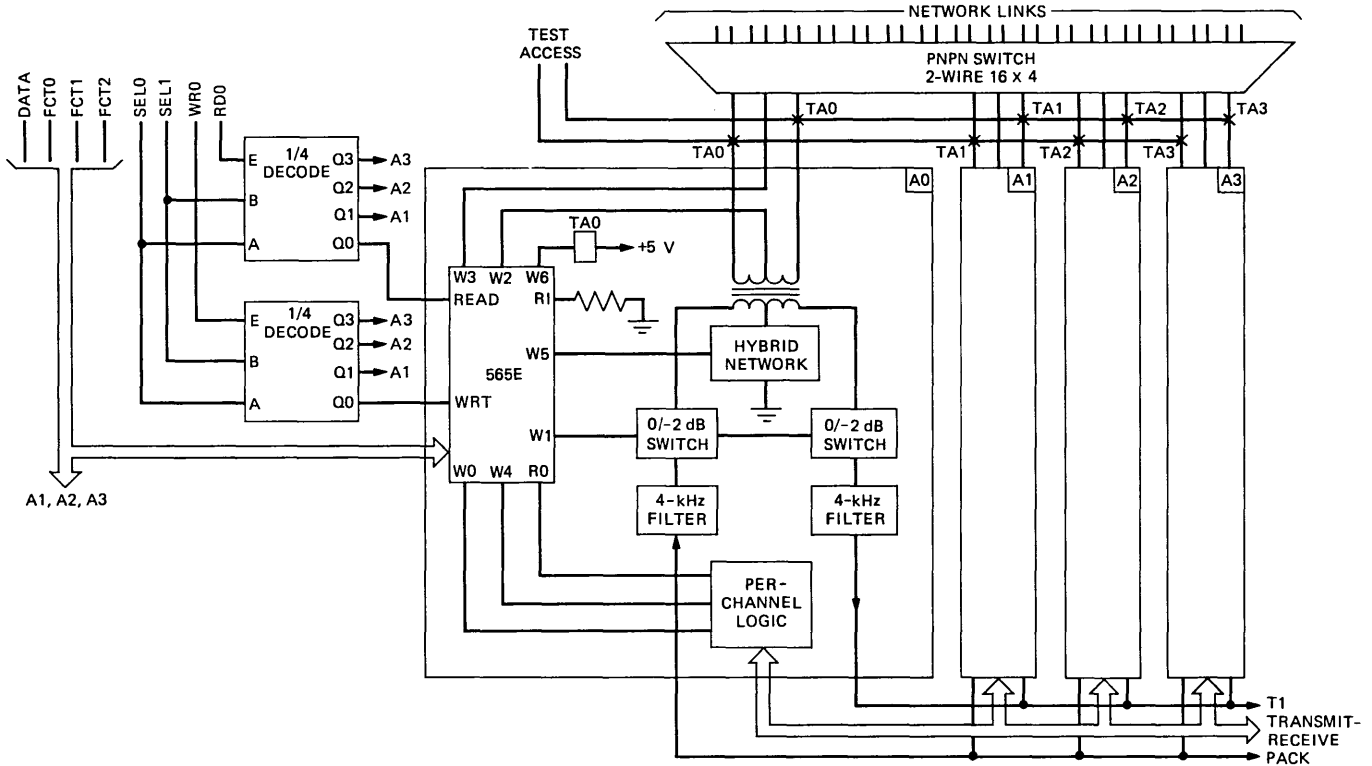


Fig. 23—No. 10A RSS T1 carrier interface circuit pack.

or if a line is suspected of being an extremely poor impedance match to the balancing networks. After this, 4-kHz cutoff low-pass filters prevent aliasing and noise from the PAM signals. A 60-Hz notch filter is included in the transmit filter. Per-channel logic interprets the timing signals from the TR pack. This logic controls PAM bus and supervision bus usage.

The same custom IC used per line circuit controls each channel. Network control is identical, with the other functions unique: a test access relay may be operated to allow miniresponder access for transmission testing, the hybrid network state, 2-dB loss, receive supervision for test purpose only, transmit supervision, and channel receive PAM bus enabling. This last function is used to stop audio reception when the channel is not in use to eliminate a possible oscillation condition and to quiet the channel when an alarm is present. Again, the state of the latches in this circuit may be interrogated under fanout pack control.

5.2 The analog carrier interface

When other carriers besides T1 using D4 banks are used with RSS, the carrier equipment is external to the RSS frame (Fig. 24). The data links are interfaced to the carrier using modems. A new interface for the audio channels is now also required between the RSS and its carrier terminal and between the carrier terminal at the host ESS and its network.

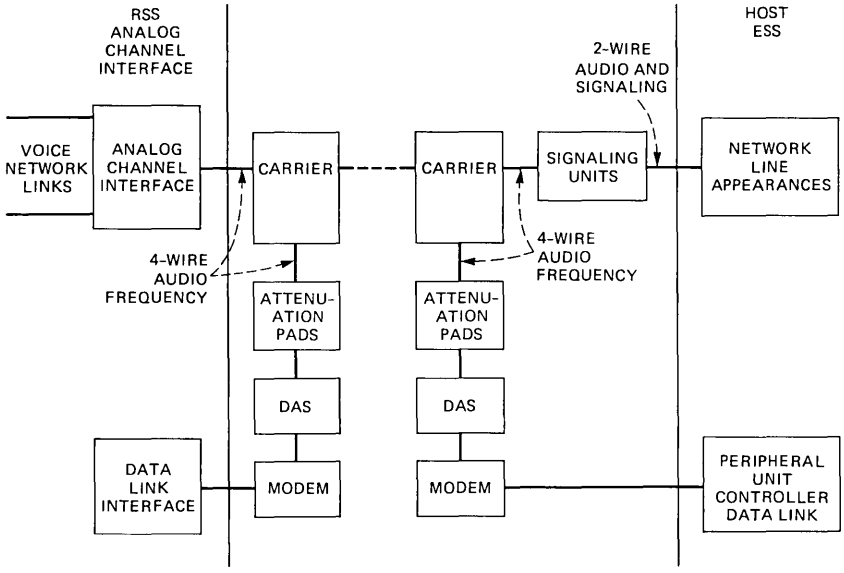


Fig. 24—No. 10A RSS general carrier interface.

At RSS, the Analog Carrier Interface pack (ACI) provides conversion from the RSS two-wire transmission voice frequency electronic network and the control complex to the four-wire transmission and Single Frequency (SF) signaling used by the carriers. As may be seen in Fig. 25, the ACI is identical to the TCI in RSS control and until after the 2-dB loss section of the four-wire transmission path. This similarity is important as it maintains control compatibility between the two. The difference after this point is due to the four-wire audio connection to the carrier and SF signaling.

Each ACI pack has a quartz-crystal-based 2600 Hz sine wave generator, with a voltage reference controlled output level as a source for SF signaling tone. Each channel contains a timing IC for signaling that also uses the 2600 Hz as a time base. When the channel is on-hook, −36 dBm 0 SF is transmitted and the audio from the hybrid is cut off. When the channel goes off-hook, SF is cut off and the hybrid audio is cut through after 120 ms delay. If the channel goes back on-hook, audio is immediately cut and −24 dBm 0 SF is transmitted for 400 ms. If the channel is still on-hook after 400 ms, the SF is reduced back to −36 dBm 0.

An audio cut-off under individual control is in the receive path to emulate the receive PAM bus enabling control available on a TCI channel. An adjustable attenuator with a range of 1.5 dB is included in both transmission directions of an ACI channel to allow for wiring losses to the carrier bank.

At the host ESS (Fig. 24), an SF unit, including the special balancing network for the four-wire to two-wire hybrid, was made by adding a slight modification to an already existing SF signaling unit.

VI. TEST CIRCUITS

Two families of test circuits exist in the RSS. Some circuits are used to test customers' telephone lines, while the rest are part of transmission testing.

Line testing equipment is designed to be compatible with existing test facilities like the Local Test Desk (LTD). Craft are able to remotely test RSS lines with the same ease that they test host lines.

Transmission testing equipment is also designed to be compatible with existing test facilities. Automatic testing of the transmission facilities between the RSS and host is accomplished by circuits similar to those in No. 1 ESS type trunk testing equipment.

6.1 Line testing

Customer line testing is done through the ringing bus of the RSS. A Test Access Bus (TAB) runs between all Universal Service Circuits (USCs) and to all line testing circuits. The USC is able to connect the

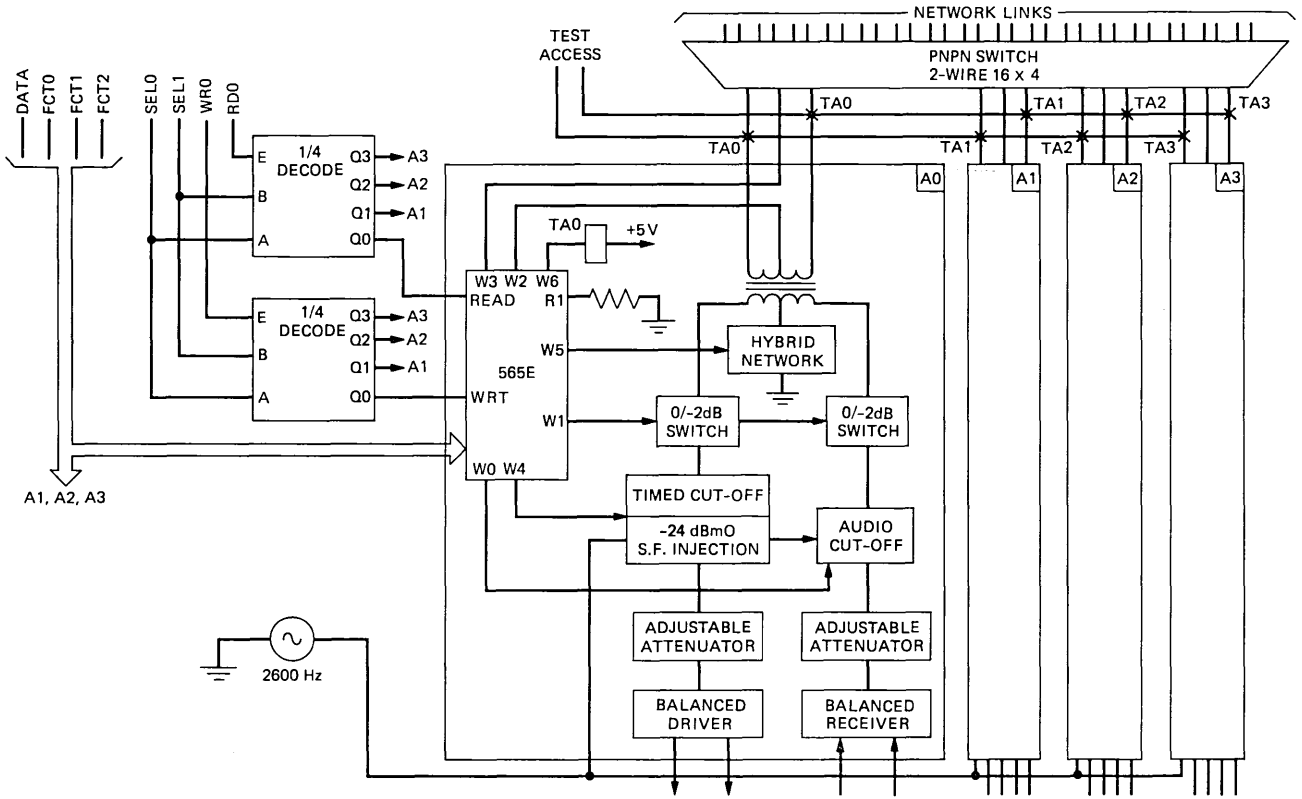


Fig. 25—No. 10A RSS analog carrier interface circuit pack.

TAB to one of its ringing buses. A test circuit reaches a line by seizing the TAB, an idle USC, and one of the ringing buses.

If the 10A RSS is within metallic range of the LTD, a pair of wires is run from the host to the RSS (see Fig. 26). The LTD connects to the host in the usual manner through an LTD trunk.

The metallic test path terminates as a line appearance on the host. Out at the RSS, the loop terminates on a pair of boards called Metallic Line Access Ports (MLAP). Under control of the host, they provide the connection from the test path to the TAB.

For those cases where the RSS is too far from the host, telemetry is used. This telemetry system is an option on the LTD. The corresponding remote line testing equipment is available for use by all switching systems. The Remote Line Test (RLT) equipment for RSS is functionally the same as for other systems, only the implementation is different (see Fig. 27). Three boards have replaced half of a frame of equipment.

In Fig. 27, note the circuit at the interface between LTD and LTD trunk. This circuit, called the Local Test Desk Applique (LTDA) monitors all signals sent to the RLT. When a code is seen from the desk that requires action by the host, the LTDA passes the data to the LTD trunk. By injecting data at this point in the system, much of the existing line testing software was utilized.

Line testing through an RSS has one major problem not found in other ESSs. Each line on the RSS has a pair of resistors associated with it to bias the line negative. A 100-kilohm resistor is present from the tip to a −96 volt supply. The ring conductor has similar treatment. If unassisted test equipment tried to read leakage or foreign potentials on the customer's line, the 100 kilohms and −96 volts would be seen.

This problem is solved by using precision negative 100-kilohm resistors tied to −96 volts during line testing (see Fig. 28). The parallel combination of the positive and negative resistors is nominally an open circuit. Under worst-case conditions, the magnitudes of the 100-kilohm bias resistors are still boosted to a value over 8 megohms.

One negative 100-kilohm resistor exists on each MLAP board. The

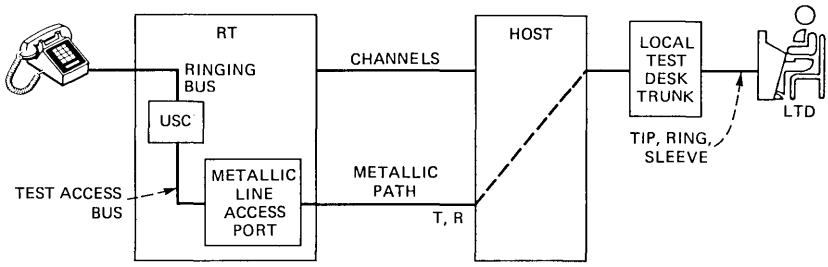


Fig. 26—Line test equipment using a metallic test path.

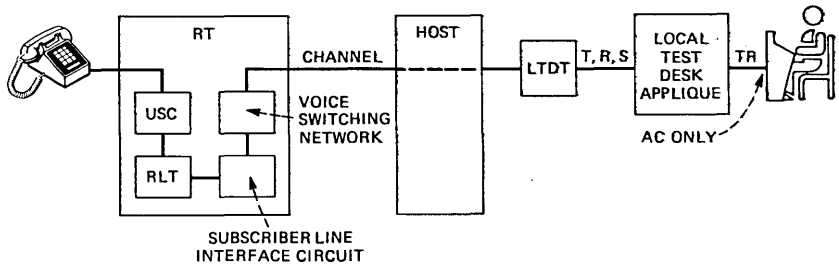


Fig. 27—Line test equipment using a telemetry path.

complexity of this board comes from two requirements. First, the worst-case tolerance of the negative resistor must be better than ±0.2 percent. Secondly, it must keep that accuracy over an applied voltage range of −96 volts to +200 volts. This voltage range is necessary to prevent any line testing equipment from saturating the negative resistor circuits and seeing the 100-kilohm resistors.

A number of circuit techniques are employed to meet the above requirements. A structure was chosen that contains a Multiplying Digital-to-Analog Converter (MDAC). With it circuit gain can be adjusted until the negative resistor has the proper value. The MDAC is controlled by a calibration circuit that also resides on the board. The calibration circuit contains a precise positive 100-kilohm resistor which can indicate when negative 100 kilohms has been achieved.

Linearity of the negative resistor is essential to the overall circuitry accuracy. A low-cost MDAC with the same linearity as an operational amplifier was developed. Speed is not important here so miniature mercury relays are used to switch various resistors into the signal path.

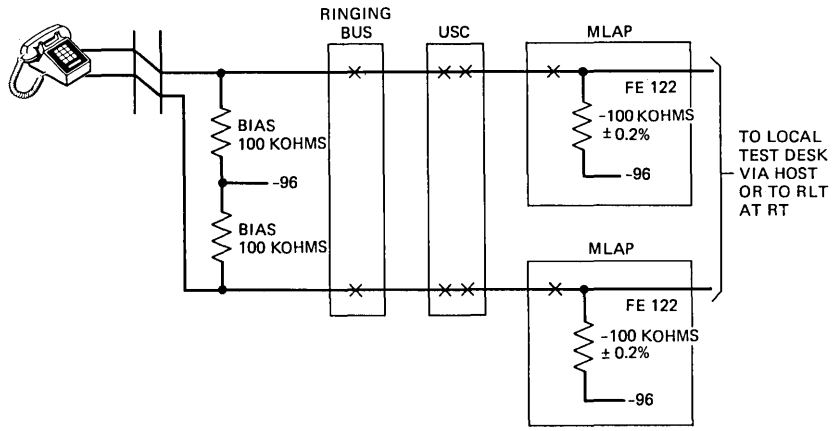


Fig. 28—Line testing with bias resistors.

The result is a very linear 8-bit MDAC with a large dynamic range passing through 0 volts.

Another source of potential nonlinearity is the transistor operated as a currrent source. We have two current sources in the signal path. They must have a large dynamic range and a constant gain. The alpha of the output transistors is a function of collector current and, therefore, was a potential problem.

The problem was solved by using local feedback. Any transistor with a beta greater than one becomes able to have an effective alpha very close to one. In practice, no variation in alpha can be seen over four decades of collector current.

The large voltage range of the negative resistor requires high-voltage transistors. When worst-case parameters are considered, little margin for transients exists. Rather than use even higher voltage transistors, a new circuit was developed. We have available a signal proportional to the collector voltage of our critical transistor. This information is used to quickly move the emitter of that same transistor. In this way, the collector-to-emitter voltage can be set to a single value independent of the collector voltage. Part of a quad operational amplifier and a small floating power supply are required. A low-voltage transistor can then stand a large voltage on its collector.

6.2 Transmission testing

Most of the transmission test equipment in the RSS resides on one board. This board includes an automated transmission test circuit called the miniresponder in addition to a number of tone sources and a tone detector. A microprocessor on the board is used for local control.

The miniresponder is functionally the same as a 56A remote office test line. It operates under the control of the CAROT to test carrier channels between the RSS and host.

During a transmission test, the CAROT transmits multifrequency signals to the miniresponder over the path to be tested (see Fig. 29). In response, the miniresponder configures itself to do the test. Then it either sends or receives test tones and, if required, reports the results to CAROT.

Upon command, the miniresponder can do various two-way loss and noise tests. If the microprocessor detects a problem in the miniresponder, it can give a detailed account to CAROT.

The tone sources available on this board are used for manual testing of carrier channels. Requests for a tone source can be initiated from one of the host's maintenance trunk test panels. This causes a data link message to be sent to the RSS which, in turn, instructs the board to output the proper signal. Circuit failures are detected by the on-board microprocessor and passed back to the RSS. A data link message is then sent to the craft indicating the problem.

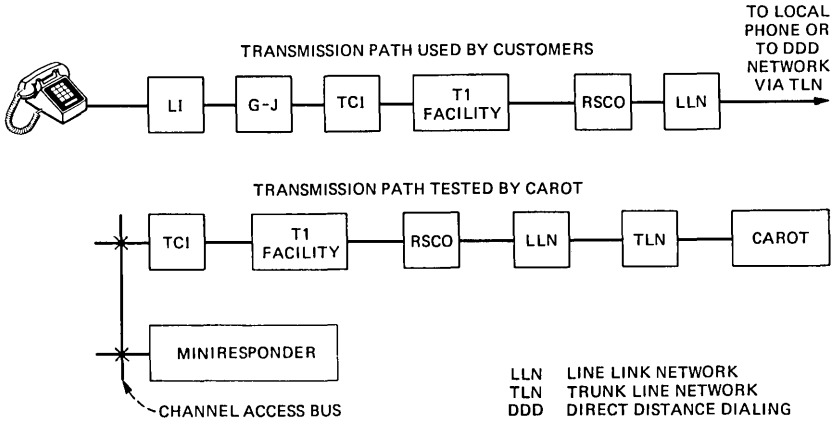


Fig. 29—Transmission testing.

Up to this point transmission testing of carrier channels has been considered. Alternating current testing is also done within the RSS. This is to ensure that customers have ac continuity through the line appearances to the network. As part of the line interface diagnostic, a tone is applied to the customer's line via the TAB. It is seen by a tone detector switched to that line appearance through the network.

VII. LOW-LEVEL SERVICE CIRCUITS

7.1 Functions

Normally, tones such as dial tone, busy, reorder, and audible ring are supplied by the host ESS and sent to an off-hook customer over one of the available voice channels. *TOUCH-TONE* service digits from a customer *TOUCH-TONE* pad are also received and decoded by the host ESS using one of its *TOUCH-TONE* service receivers. However, when the RSS is in stand-alone, because of the loss of both data links, the host facilities cannot be used and these functions must be provided within the RSS frame.

The ROH tone is never sent from the host ESS to an off-hook customer. The high level of this signal would overload the corresponding T1 Carrier Channel resulting in the ROH signal being distorted. The ROH tone is, therefore, also generated within the RSS frame.

A general-purpose ac source and matching ac detector are provided within the RSS frame for performing ac continuity tests on network A-links, junctors, and line circuits.

7.2 Circuits

The *TOUCH-TONE* service circuit pack contains the precise tone plant and *TOUCH-TONE* service receiver circuit. The precise tone

plant produces dial tone, busy tone, reorder tone, and audible ring. Circuitry is also provided to interface a recorded announcement machine into the RSS network. The circuit pack also contains an 8 by 16 first-stage switch that provides 8 appearances to the network. Up to six TT circuit packs are used in a frame with the number being dependent on frame line size.

The ROH/ELS circuit pack contains the ROH tone source and detector, a 1400-Hz test source, an ac continuity detector, and the Electronic Loop Segregator (ELS). The ELS portion will be described elsewhere. The circuit pack also contains an 8 by 16 first-stage switch that provides 8 appearances to the network. The ac continuity detector also has a metallic test-access bus appearance for use in performing ac continuity tests of line interface circuits. There is one ROH/ELS circuit pack per RSS frame.

VIII. POWER

The RSS frame uses a single battery voltage of −48 volts, making it compatible with existing CDO battery plants. It has a current drain of up to 20 amps depending upon frame circuit pack equipage and active call traffic.

Besides −48 volts, within the RSS frame, there exists a multiconverter complex to provide five additional voltages of +5, +12, +24, −12, and −96, as needed by the electronic circuitry used throughout the frame.

8.1 Converters

As shown in Figs. 30 and 31, the RSS power complex uses various types of power converters. Some of the converters are dedicated to a certain group of packs, while others are connected in a parallel fashion on a common bus, which is then used throughout the entire frame. Also, some of the converters have a single output voltage, while others are of the multivoltage type—all converters used are of the pulse width controlled (PWC) type.

The power complex has been designed around a modular philosophy in that all converters are pluggable and all are *not* needed in the basic frame configurations. Hence, the power complex grows with the number of lines and channels.

8.2 Distribution

The philosophy behind distribution of power to and within the RSS frame is consistent with that philosophy used in all other areas of the frame design: there should be *no* single fault which would eliminate service to more than 64 customer lines. This has been accomplished by the following (refer to Fig. 30.):

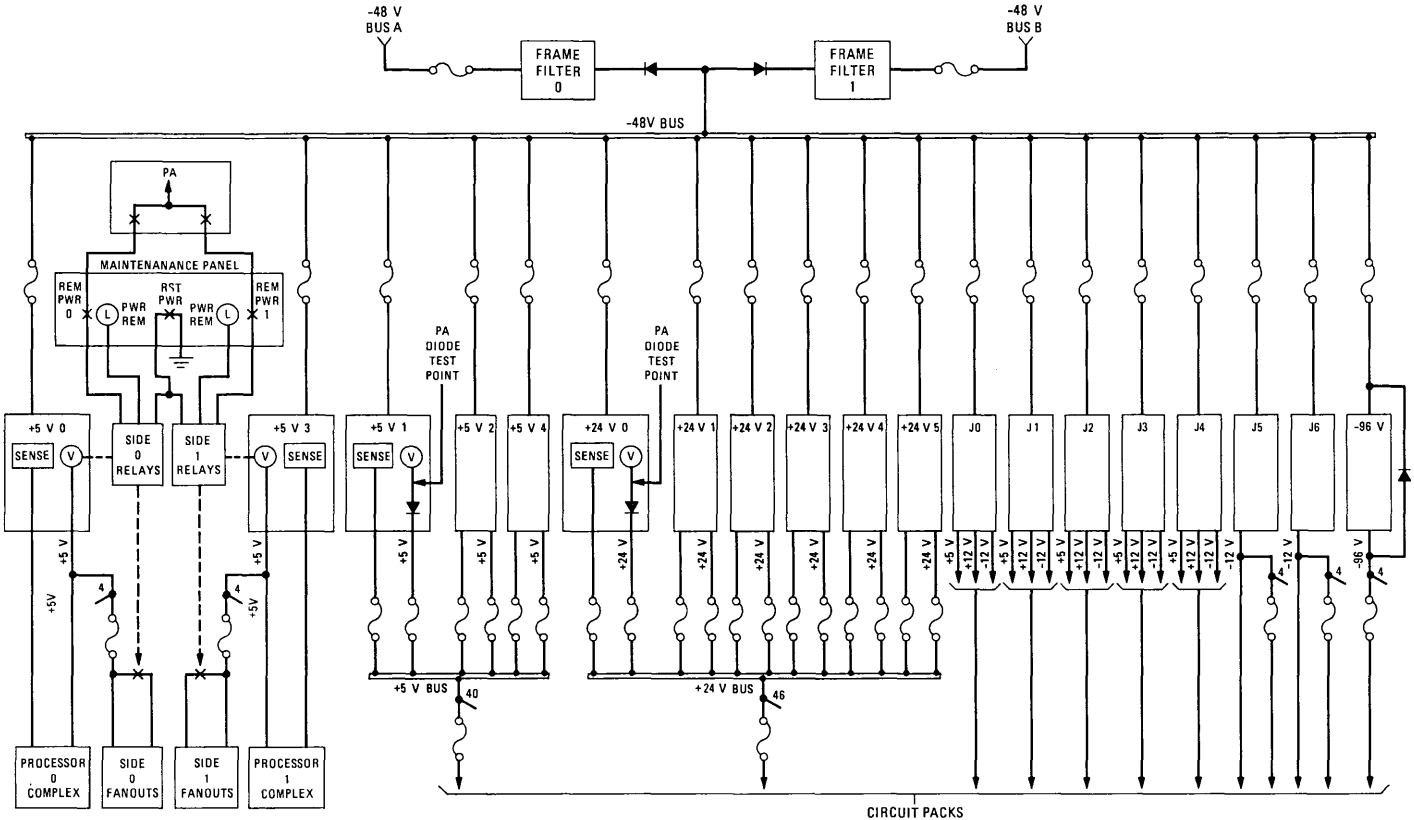
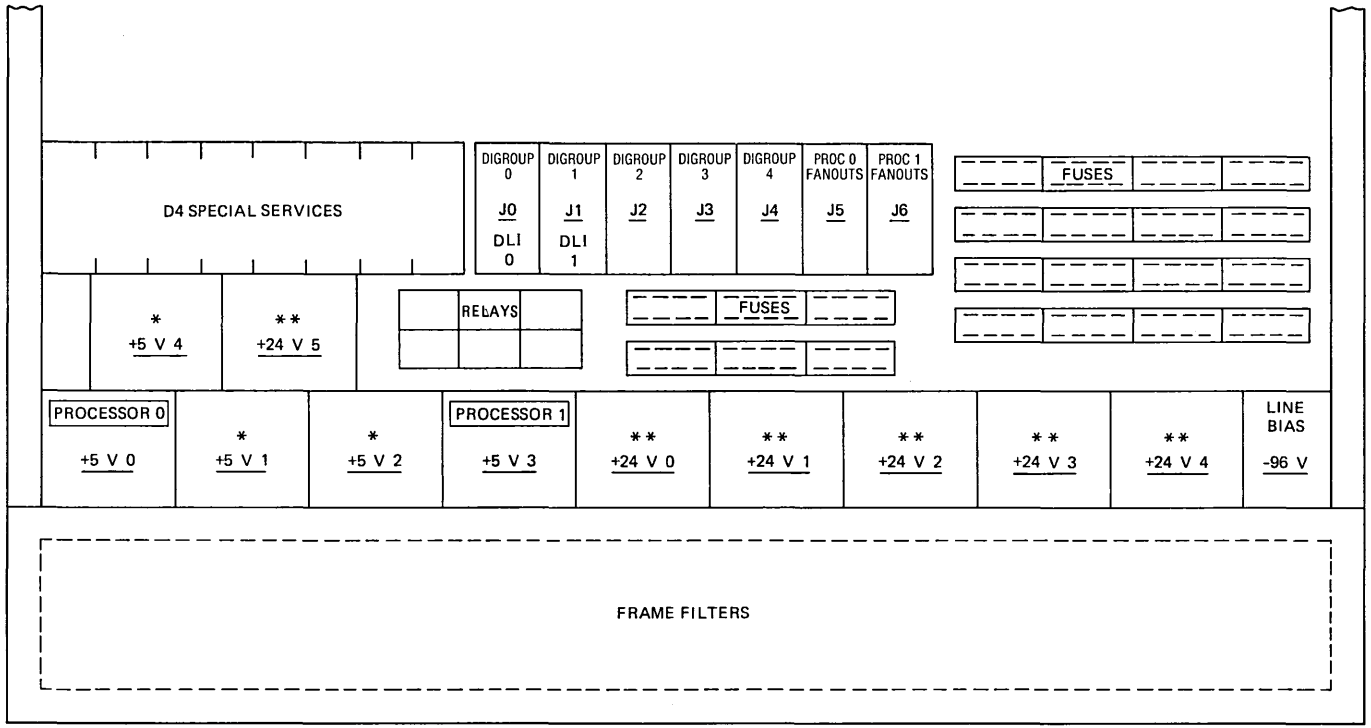


Fig. 30—Power distribution.



* CONVERTERS +5 V 1, 2, 4 ARE CONNECTED IN PARALLEL TO A COMMON +5 V BUS.

** CONVERTERS +24 V 0-5 ARE CONNECTED IN PARALLEL TO A COMMON +24 V BUS.

Fig. 31—Converter identification.

(*i*) Circuit packs have been fused such that any blown fuse will not cause a service outage to more than 64 lines (180 fuses total).

(*ii*) The main −48 volt frame power bus has been duplicated from the battery plant and connected together at the RSS in a "diode OR" manner before powering the frame.

(*iii*) The dedicated power converters have only been used on those circuits which are duplicated or nonservice affecting (microprocessor, DIGROUPS, DLI, miniresponder, RLT, ROH/ELS).

(*iv*) Two groups of converters in the power complex have been connected in the aforementioned parallel manner on a common bus in order to provide two very reliable system voltages of +5 and +24 volts. The number of converters used within each group is based on frame load (circuit pack equipage) and an $n + 1$ philosophy to provide an on-line hot spare. As shown in Fig. 30, each converter within a group is also connected to its common bus through an "ORing diode" for system protection and isolation against a converter fault.

8.3 Monitoring

The various power complex functions (converter output voltages, fuse alarms) are monitored by the RSS processor using the power alarm monitor (PA) circuit pack.

The 180 fuses in the power complex have been logically divided into 19 groups. Associated with a fuse group is a scan point on the PA. When a fuse blows, the corresponding group scan point is activated on the PA to indicate a blown fuse condition to the processor. The determination of which exact fuse is blown is left up to central office personnel by the visual indication presented on the fuse block near the base of the frame. (There is a separate visual indicator per fuse.)

Each voltage produced by a power converter in Fig. 31 has a corresponding scan point associated with it on the PA, resulting in 29 different converter scan points. The processor can monitor the condition of the power converters by determining if these scan points are within a specific range.

8.4 Diagnostics

Several diagnostic features have been designed into the power complex to maintain its integrity.

A diagnostic feature has been provided on the PA to ensure that there are no fuse alarm scan points stuck in a normal state and not capable of indicating a fuse alarm. By operating a distribute point on the PA, all fuse alarm scan points will toggle to the alarm state.

Those converters which are connected to a common bus must be routinely tested to ensure that their ORing diodes are not shorted and will perform their duty in the event of a converter fault. The RSS

processor via the PA routinely shuts down each paralleled converter, one at a time, and measures the corresponding converter output voltage on the converter side of the ORing diode. (Refer to Fig. 30.) If the ORing diode is not shorted, the output will decay to 0 volts. Several hardware safeguards have been designed into the converter shutdown circuitry on the PA to prevent an RSS processor from maliciously or accidentally shutting down a power converter. Also, once a converter has been shutdown, hardware prevents another shutdown until the first converter is restored to service.

The PA has also been designed such that any single hardware failure on the circuit pack will not affect the power converters in such a way that overall system service is affected.

IX. SUMMARY

Various circuits have been described here in the areas of line interface, transmission, line testing, and power.

A 10A RSS customer's line is powered and supervised by an efficient switching-mode battery feed circuit. The customer receives ringing and other high-voltage signals from a universal-level service circuit which gains access to the line through a time-shared relay access network. Audio from the customer is switched through a low-level integrated electronic network to either another customer or to a carrier channel back to the host ESS. Two types of carrier interfaces may be used, self-contained T1 carrier, or a general interface to external carrier banks.

Testing of customer lines is done with LTD compatible equipment. Both metallic and remote testing is possible.

All transmission tests use a single circuit pack. Using a microprocessor, it is able to communicate with automatic, as well as manual, test equipment at the host.

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No. 10A Remote Switching System:

Host Software

By D. W. BROWN, J. J. DRISCOLL, and F. M. LAX

(Manuscript received April 29, 1980)

The Remote Switching System (RSS) *is a distributed control system which has the call-processing control in the host* ESS. *This design provides the capability of easily giving* RSS *lines the same features that are available to host* ESS *lines. A significant amount of new software is required in the host* ESS *to provide the control of the 10A* RSS. *This article describes the* RSS *host call-processing functions and the administrative and message handling software necessary to provide this control.*

I. INTRODUCTION

A local Electronic Switching System (ESS) provides the call control for a 10A Remote Switching System (RSS). The 10A RSS acts as a slave executing orders sent to it from the host ESS and reports events, such as line originations, to the host. A major advantage of this type of distributed control is that the complex tasks of call processing can use existing host software and share host equipment and trunking facilities. This sharing of host ESS software provides the capability of easily providing RSS lines with the sophisticated features that are offered to host ESS lines.

Figure 1 shows the system configuration consisting of a host ESS office, a 10A RSS (remote terminal), a data link controller, interconnecting voice channels, and data links. The data links are used for communication between the host ESS and the 10A RSS, and provide the means by which orders from the host are transmitted to the 10A RSS and acknowledgments are returned to the host. Voice channels are used to provide the RSS lines with access to the host network and are selected dynamically. In the No. 1 ESS RSS host implementation, the

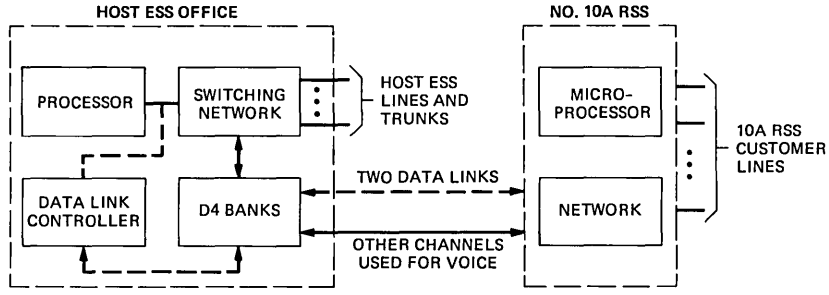

Fig. 1—Remote switching system configuration using digital carrier.

data link controller is a Peripheral Unit Controller/Data Link (PUC/DL).

The host ESS software structure for RSS is influenced by five basic system requirements:

(*i*) All existing host ESS line features should be capable of being provided to RSS lines with comparable service performance.

(*ii*) The effects on the host capacity to process non-RSS calls should be minimized.

(*iii*) Although the first RSS development uses a No. 1 ESS for a host, the design should be portable to other local ESSs with minimum development.

(*iv*) New host features should be able to be provided to RSS lines with minimum development.

(*v*) The 10A RSS hardware and firmware must be identical for all host machines.

The first requirement is met by making maximum use of the existing host call processing, translation and administration programs, with modifications wherever necessary. This also tends to minimize the overall development since a major portion of these programs are independent of RSS. Modifications, where necessary, are done in a manner to minimize the cost in processor real time to non-RSS calls and functions [Requirement (*ii*)].

The reduction of the cost of development over different ESS machines is realized by recognizing that a major portion of any software development is spent on requirements, planning, design, and testing, with a lesser portion of the time spent on the actual program coding. Fundamentally, all the ESS machines have similar software facilities to perform switching functions, although the method of implementation may differ. These factors are used in the RSS by producing host software requirements and designs that strive for machine independence to maximize portability between different host machines. Since the programs are functionally equivalent, higher level test plans are also portable between the machines.

This paper describes the RSS host software architecture, call-processing functions, and the database administration and integrity facilities. The host software structures to provide RSS resource administration and to handle RSS messages are also described.

Although most of the designs and functions are discussed from a host-independent viewpoint, the data linking and message handling structures discussed in Section V apply specifically to the No. 1 ESS design. This is because the input/output (I/O) structure of the different local ESSs are quite different, and the data link controller used in No. 1 ESS (PUC/DL) will differ from other systems. However, the data link protocol and the message structures are the same for all systems so that the same 10A RSS is used for all host ESSs.

II. RSS HOST SOFTWARE ARCHITECTURE

An overview of the major components of the RSS host software is given in Fig. 2. The design of the software architecture is such that all software was put into one of the following three categories:

(*i*) Hooks in existing programs—These are basically decision functions in the host programs that make a decision concerning some aspect of the 10A RSS feature. They are required in host programs that are shared by RSS where a special action is required for RSS lines. For example, in Fig. 2 hooks are required at appropriate places in the host

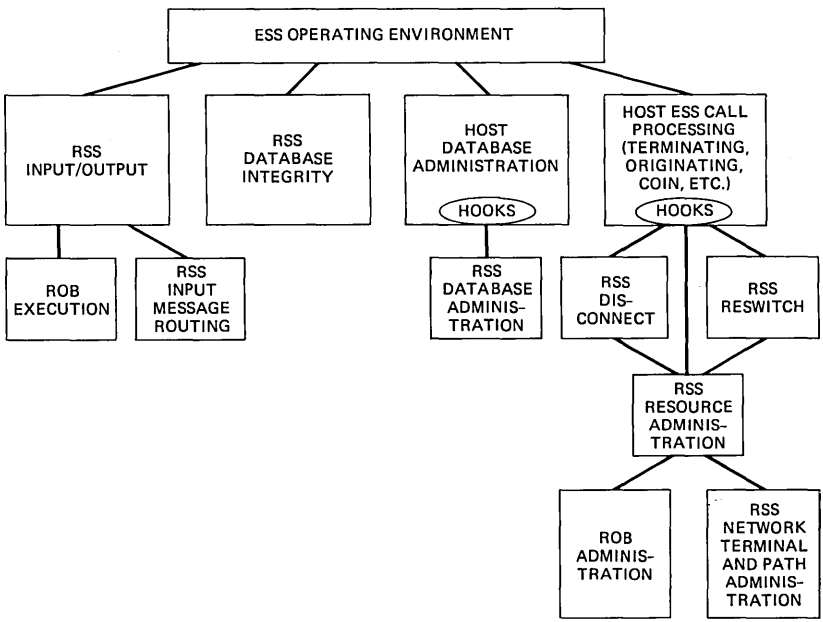

Fig. 2—Remote switching system host software architecture overview.

call-processing programs to invoke routines to perform RSS administrative functions. These hooks are coded in the host ESS standard language and the location of these hooks is quite dependent on the host software structure; thus, they are not directly portable to other hosts. However, high-level structure charts and functional descriptions may be portable since the same RSS actions are generally required in a call sequence independent of the host.

(*ii*) Unique RSS, host-dependent software—This is host software that performs unique RSS functions but whose design is different for different host ESSs. In Fig. 2, the RSS I/O and Remote Order Buffer (ROB) administration functions fall into this category. Software may be put into this category to utilize some aspect of the existing host system or to save on host resources, such as real-time. Structure charts and functional descriptions are highly portable to other hosts; however, pseudocode and state diagrams normally are not.

(*iii*) Unique RSS, host-independent software—This is host software that performs unique RSS functions whose implementation is host-independent since they only interact with the host 10A RSS database and are not dependent on the host operating system or database. This class of programs is highly portable to other host machines, even at a detailed level. The structure charts, flow charts, functional descriptions state diagrams, and even the pseudocode generated during the development process should be portable. To increase the portability of this code to other hosts, these programs were written in a high-level language. The RSS Network Terminal and Path Administration programs in Fig. 2 fall into this category.

The host software components shown in Fig. 2 are discussed in the following sections.

III. RSS RESOURCE ADMINISTRATION

The processing of RSS calls requires the allocation and management of resources that are physically located at the 10A RSS or shared between the host ESS and the 10A RSS. These resources include the channels that interconnect the host and 10A RSS, receiver off-hook (ROH) tone circuits located at the 10A RSS and the 10A RSS network crosspoints. Also, the status of RSS lines is maintained at the host. Several factors were considered in deciding whether to place these functions in the 10A RSS or in the host ESS. These factors are

(*i*) The effect on service because of the additional time delay if the 10A RSS has to be interrogated to determine line status, and to hunt voice channels and network paths.

(*ii*) The additional software development required if the host ESS programs have to take a real-time break to interrogate the 10A RSS to obtain a line's status. Host software is structured around data that are accessed without taking a real-time break.

(*iii*) The duplication of development effort that is required to provide the same functions in several host ESS systems.

Factor (*iii*) indicates that the overall development effort would be reduced by placing the line, channel and 10A RSS network path administration in the 10A RSS. However, the service criteria and the effect on the existing host software were judged to be more important; therefore, these functions are allocated to the host ESS.

The overall development effort is reduced by making the program and data structure designs independent of the host ESS. Thus, they are highly portable between ESS machines. This section describes the data structures and programs required to administer the RSS resources.

3.1 Data structures

Data structures are required in the host ESS memory (call store) to record the status of the RSS facilities and to provide for their administration. These data structures are contained in one contiguous memory block, called the RSS Path Memory Block. To simplify the engineering of the office, the RSS Path Memory Block is provided in one of three sizes corresponding to three basic network sizes of the 10A RSS. Each of the substructures in the Path Memory Block is described below.

3.1.1 Network map

The network map is only provided in one size (for a fully equipped 10A RSS network) and contains a status bit for each A-link and junctor in the 10A RSS network.

3.1.2 Path memory remote record

A path memory remote (PMR) record is provided for each possible line and channel network appearance. Since the 10A RSS network can be equipped in three different sizes, considerable ESS memory is saved by also providing PMRs in substructure sizes corresponding to the network size. The PMRs contain information about the state of the terminal and a pointer which is used to link the PMR to another PMR or to point to another memory block (call register or path memory for junctor (PMJ) involved in the call.

3.1.3 Path memory for junctor record

A PMJ record is a block of call store that is associated with a junctor in the 10A RSS network and is provided for each equipped junctor. It is used to store path and terminal information when the junctor is in a network path. A PMJ also contains a state and pointer which is used to link to another PMJ or to a call register.

3.1.4 Remote miscellaneous scan point status map

Scan points are provided at the 10A RSS for use in alarms, make-busy keys, and stop hunt keys, etc. The remote unit periodically scans these scan points and reports any changes to the host ESS via the data link. The RSS Path Memory Block contains a scan point status map which has a bit for each possible remote scan point and is updated to indicate the present state of the scan points. Host ESS programs determine the state of a scan point by interrogating the map in the host rather than sending a data link message to the remote terminal.

3.1.5 Channel head cells

The channel head cells contain memory for linking the idle voice channel PMRs onto a one-way linked list, as well as for traffic usage and peg counts. One head cell is provided for the channels terminating on each of the two modules of the 10A RSS.

3.2 Programs

The responsibility for managing the RSS resources resides within the host in the RSS terminal and network administration programs. These programs are designed to provide the functions required by client programs, such as hunting channels, hunting 10A RSS network paths, and fetching or changing the state of a line. In general, the client program is isolated from the data structures since the administration programs provide the interface with the RSS resources. This technique of "data hiding" keeps the data structure access confined to the portable programs.

3.2.1 Network terminal administration programs

The 10A RSS network terminal administration program contains routines for channel hunting, channel idling, changing the state of a terminal (line or channel), and for determining the state of a terminal. These routines have the responsibility for maintaining the state and pointer fields of the line or channel PMR (see Fig. 3) to indicate the status of the terminal.

The PMRs for idle channels are put on a one-way linked list, with the last channel idled at the bottom of the list. Channels are selected from the top of the list, thus providing rotation among channel usage. A linked list is provided for each of the two frames of the 10A RSS (see Section 3.1.5). A channel PMR on an idle link list has the state field (see Fig. 3) set "idle"; the pointer field contains the remote equipment number (REN) of the next channel on the idle linked list. The pointer field of the last PMR contains an "end" code.

The first choice on selecting an idle channel is to select from the same module on which the REN that is to be connected to it appears.

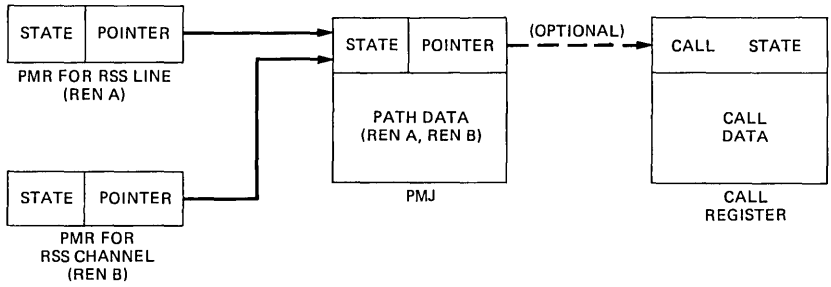

Fig. 3—Two-terminal RSS path memory configuration.

This conserves the usage of the limited number of intramodule junctors. However, if there are no idle channels on the desired module, an attempt is made to find an idle channel on the other module.

3.2.2 Network path administration programs

The main functions of the 10A RSS network path administration programs are to hunt and idle network paths between a given pair of RSS network terminals. In the course of performing these functions, these routines administer three types of data structures: the RSS Network Map, PMRs, and PMJs. A path hunt is performed by selecting an idle junctor and A-links (using the busy/idle status in the network map) so that when the corresponding network crosspoints are closed, a talking path exists between the two given network terminals. This hunt is exhaustive in that it looks for all possible combinations of junctors and A-links that could be used to form a path. The selected junctor and A-links are marked busy in the network map so that they are not selected by the next path hunt request.

A record of the path configuration between two terminals is maintained in the PMRs of the two terminals and the PMJ for the junctor included in the path. Figure 3 shows how the path memory elements are set up. The state field of the PMRs indicates that the PMR is in a path and the pointer fields contain pointers to the PMJ. The usage of the state and pointer fields of the PMJ is similar to that of the PMR. The pointer field may optionally be empty or it may be set up to point to a call register. The state field indicates which situation applies. Other data fields in the PMJ contain the REN of each of the associated terminals in the path. This structure permits the entire path to be reconstructed from the data in the PMRs and PMJ. Path trace routines, included as part of the network path administration programs, accept as input the REN of either terminal and trace through the structure to obtain the other REN and the junctor associated with the path. The identity of the A-links are also known since only one A-link can connect a given network terminal to a given end of the junctor.

More complex RSS network path configurations arise during special switching actions, such as when two RSS lines that are connected together through the ESS network are in the process of being "re-switched-down" (to be described in Section 6.4) so that they are connected solely through the RSS network. The process of linking PMRs and PMJs is extended for these cases to include all the path elements. Figure 4 shows how the elements are linked for a 4-terminal path where two pairs of terminals (A1-C1 and A2-C2) are connected and a reserved path (marked busy in memory but idle in hardware) exists between A1 and A2. As with the two-terminal path, all the RENs and path element identities can be obtained by tracing the structure given any REN associated with the path.

Routines that idle paths perform the reverse function of the path hunt routines. Given any REN associated with the path to be idled, a path trace is performed to obtain all the RENs and the junctor used in the path. The A-link and junctor status bits in the network map, the PMRs, and the PMJ, are then marked idle.

IV. DATABASE ADMINISTRATION

In addition to the generic programs, ESS machines have an extensive database that provides the information necessary for these programs to process calls and perform maintenance and administration functions. These data are called translation data and contain information such as line features, call routing and charging, and equipment configurations. Many functions, such as routing and charging, are not af-

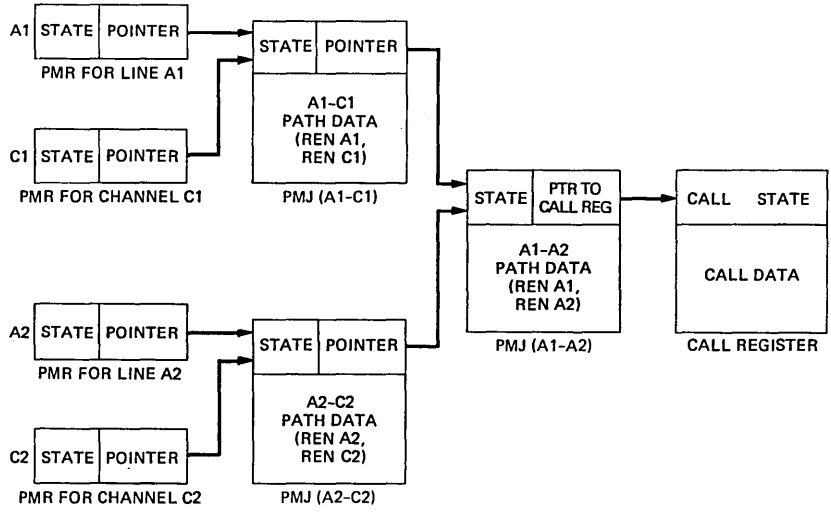

Fig. 4—Four-terminal RSS path memory configuration.

fected by the RSS feature and, therefore, most translation data are not affected either. However, changes and additions to the existing host translation data are required where it is necessary to identify line terminations and scan or distributor points as being RSS items. Also new translators are required for new RSS items. This section describes the modifications that are required for the host ESS translators, the new translators, and the programs to administer them.

4.1 Translations

Translations refers to the office-dependent data that describes the office and customer characteristics, the programs for accessing the data, and the means for changing the data. All translation data are stored in the host ESS and items that are required at the remote terminal are periodically transmitted to it via the data link. Since the host ESS performs all of the call-processing control functions, such as routing, charging and trunk selection, most of the existing translations are not affected by RSS.

The additional translations required for RSS fall into the categories of new translations and modifications to existing translations. The new translators required are the

(*i*) REN translators, which contain the originating translation data for RSS lines. If the REN is associated with an RSS channel, then the translators contain the associated ESS host line equipment numbers.

(*ii*) Remote scan point number (RMSN) translations, which define the scan point usage, are used to determine the action to be taken when a scan point changes state.

(*iii*) Remote terminal (i.e., 10A RSS) translators that contain data on the equipage and stand-alone* features for the RSS.

Both the REN and RMSN translators have corresponding host translators, and the data substructures for the new RSS translators are made identical to the ESS translators. This permits the existing host programs that access and change these translators to be used for the RSS translators with only small modifications. Another important consideration is the requirement that service features available to the host ESS lines be also available to RSS lines. By using the same data structures, this requirement is easily met and new features offered in the future will be available on RSS lines with minimum additional development. It also lessens the impact upon the client call-processing programs since the data returned by the access routines have the same formats. New programs are required to administer the remote terminal translator since it has no ESS counterpart.

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* Stand-alone refers to the operation whereby the 10A RSS processes intra-RSS calls when communications with the host ESS are lost.

In addition to the new translators, several existing translators require modifications for RSS. An indicator has been added to the directory number translator output to specify whether the called party is an RSS or an ESS line. Several other translators that can contain equipment numbers require indicators to specify whether the equipment number is remote or local. For example, multiline hunt lists can contain a mixture of RSS and ESS lines. Similarly, some translators require an indication that scan and distributor points be specified as either remote or local.

After initial call setup, the host call-processing programs use the line equipment number (LEN) of the ESS end of the voice channel in the call register data area rather than the REN for the line involved in the call. This permits the existing host software to handle RSS calls without making extensive changes. However, since the REN of the RSS line is required for some call actions, such as disconnect and coin functions, a means must be provided to obtain this line REN from the ESS LEN of the channel. This means is provided by way of the LEN translator which contains the channel REN for the RSS channel. The path memory associated with the channel REN can then be traced, as described in Section 3.2.2, to obtain the RSS line REN from the PMJ used in the RSS line to channel path.

Corresponding to the RSS translation data discussed above, the host recent change and service order programs are modified to enable these data to be changed by the operating company. The same recent change message formats used for host lines are also used for RSS lines, with different keywords to indicate items that are RSS-related—for example, LEN is replaced by REN in the No. 1 ESS application. Additional keywords are added where a new item is required, and new messages are provided for the unique 10A RSS translation data. The flexibility of the ESS recent change programs permits this to be easily implemented.

4.2 Remote terminal translation data update

Although the host call-processing programs use the translation data stored in the host, there is a subset of translation data that is required at the remote terminal for use during both normal operation with the host and during stand-alone operation. These data are

(*i*) Multiparty ringing option (ac/dc or superimposed).

(*ii*) Ground start applique circuit number for ground start and coin lines.

(*iii*) Hardware equipage information, such as the network size and channel interface board equipage.

In addition to the above data items, stand-alone operation, whereby the 10A RSS processes intra-RSS calls when communications with the

host ESS have been lost, requires additional data to perform the following translations:

(*i*) Emergency directory number routing data. Up to four, 3-, 6-, or 10-digit directory numbers (such as 911) can be specified for special routing during stand-alone operation.

(*ii*) Terminating directory number translations to yield the REN and type of ringing.

(*iii*) Multiline hunting lists.

(*iv*) Originating line translation data which includes the type of dialing, distributor point assignments and major class. The major class stored at the remote terminal is a subset of the major classes served by the host. It can be individual, two-party, multiparty, coin, manual, or unassigned. The major class of each RSS line, as stored in the host translation database, is mapped into one of these major classes before the data are sent to the 10A RSS.

The 10A RSS copy of an individual subscriber's translation data is updated whenever a recent change on that line is entered into the host. At that time, a translation data update message, which contains all the data pertaining to that line, is sent to the remote terminal. A total update of all remote terminal translation data is done whenever the remote terminal requests it. This is done on a routine basis, once a day, and whenever the remote terminal suspects that the data may have become mutilated. The update can also be requested manually from the host teletypewriter.

V. THE RSS MESSAGE HANDLING

5.1 Hardware overview

Figure 5 is a diagram of the 10A RSS No. 1 ESS host interface and the hardware components involved in the transmission of data between the remote terminal and the host. Communication between the two machines takes place over a pair of low-speed data links that share the same transmission facilities as the voice channels that interconnect the remote terminal with the host. Each data link is placed on a separate transmission facility for reliability. Where carrier facilities are used, the links are assigned to a dedicated voice channel on the carrier system with each link being assigned to a separate carrier terminal.

Both RSS links are 2400 bps synchronous links. The on-line link is active and carries the entire data traffic between the host and 10A RSS, while the off-line link is maintained in a standby state as a spare. The on-line, off-line status of the links is determined by the host office based on error information accumulated by the software responsible for running the links. At the remote terminal, the link is interfaced to the microprocessor through a data link interface circuit (DLI). The DLI provides a small amount of data buffering and performs a number of

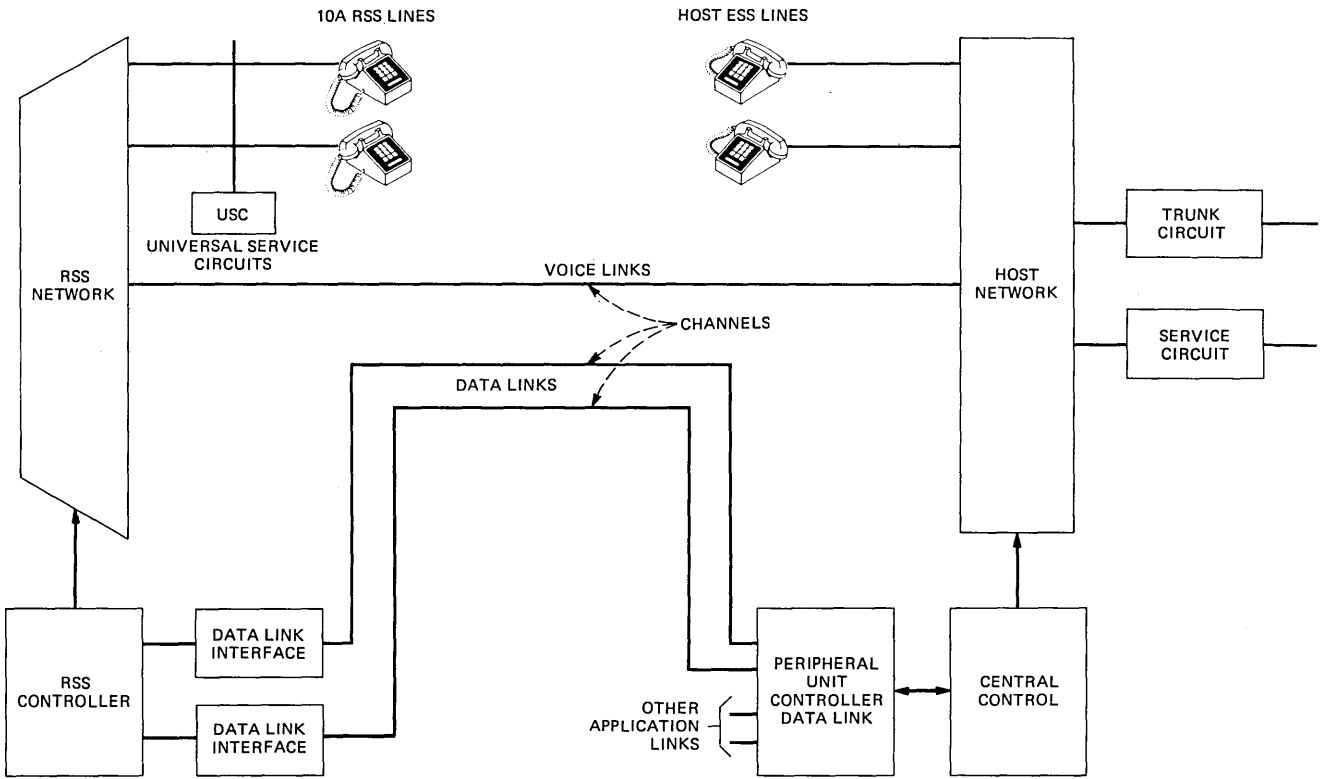

Fig. 5—No. 10A RSS—No. 1 ESS host interface.

control functions essential to implementing the synchronous link protocol.

At the host, the link interfaces with a functionally similar line interface unit that is part of the PUC/DL. The PUC/DL is a peripheral unit controller that has been equipped with the hardware and firmware to serve as a data link terminal for up to 16 data links. The function of the PUC/DL is to provide the control for physically transmitting and receiving data on the links and to provide data buffering for the host office. The data being transmitted and received by the PUC/DL are buffered on a per-link basis within the terminal. Sufficient data buffering is provided to allow the host to efficiently exchange large blocks of data with the terminal on a schedule that is efficient to the host.

5.2 Software overview

The routines that control the data transmission between the remote terminal and host are located in the remote terminal, the PUC/DL, and the host office. The organization of these programs is illustrated in Fig. 6. There are two basic functions to be performed. Data must be transferred reliably over the link and an interprocess communication system must be provided to allow software processes in the host to communicate with processes in the remote terminal. These two functions are provided by the data link protocol software and a set of message routing routines. The protocol software provides virtually error-free transmission of data over the link by executing a set of error-detection and error-correction procedures. The message routines allow a process in one machine to direct a message to a process in the other. These two systems are largely independent and bear a hierarchical relationship to one another in the sense that the message routing routines rely on the link protocol routines to accurately transmit data from one end of the link to the other.

5.3 Data link protocol

The protocol routines are executed in the remote terminal and the PUC/DL. The 10A RSS application uses the link level portion of the X.25 protocol to control the link. This is an industry standard protocol which is suitable for other link applications furnished from the PUC/DL in addition to RSS. It is a bit-oriented protocol designed for synchronous link operation. To provide for error detection and correction, the data to be transmitted are segmented into numbered blocks termed frames. The frame format is shown in Fig. 6. As frames are transmitted, they are sequentially numbered and a cyclic check code is computed over the data in the frame. The frame number is transmitted in a control byte at the beginning of the frame, and the check code is appended to the end. The frame numbering scheme makes it possible

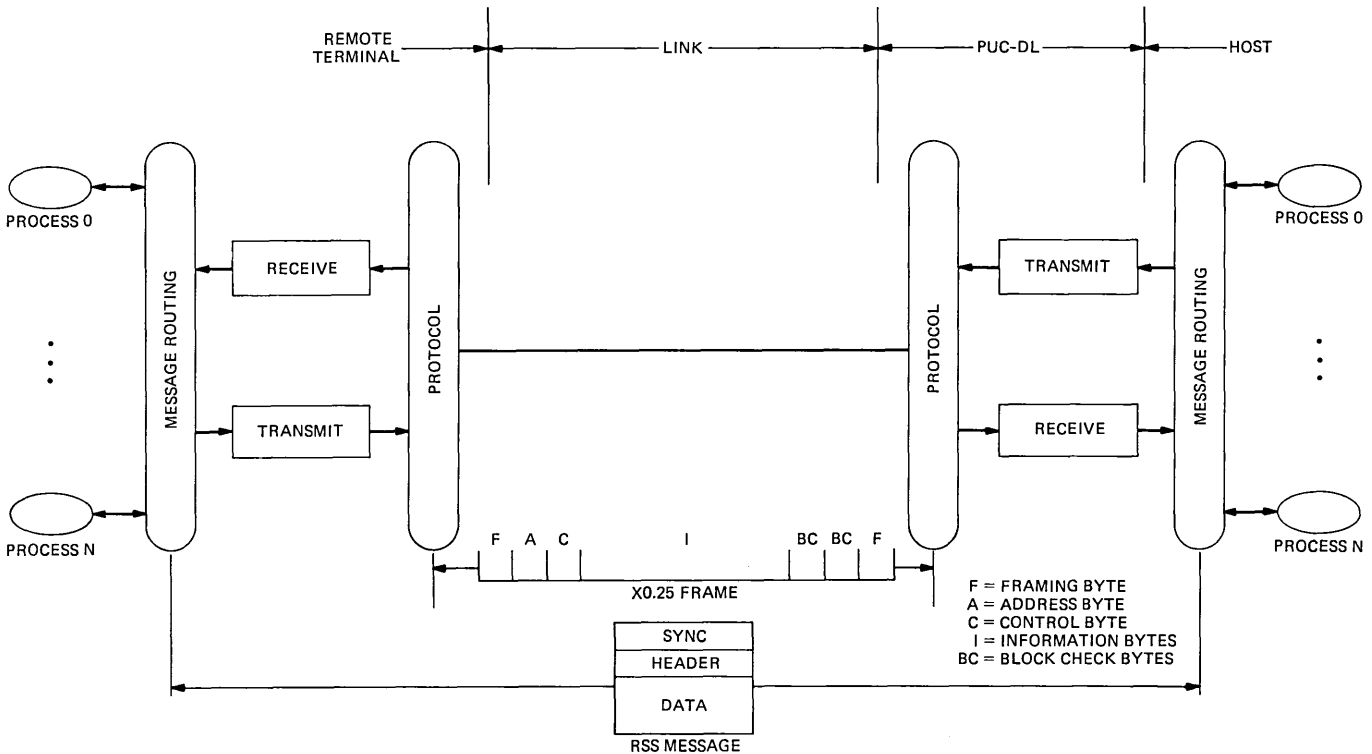

Fig. 6—Data transmission program overview.

to identify frames for retransmission and to detect missing frames in the received data. As frames are processed at the receiving end of the link, the cyclic check code is recomputed and compared to the one transmitted with the frame. A mismatch indicates that a transmission error has occurred. A positive acknowledgment is returned to the data transmitter for all frames received correctly, and a retransmission request is returned if a frame is received in error. In response to a retransmission request, the data transmitter will retransmit all the frames it has previously transmitted starting with the one in error.

The protocol software at the PUC/DL has the additional function of providing link status reports to the host machine. Error conditions such as high transmission error rate, frame acknowledgment time outs, and loss of data carrier are monitored by the protocol and reported to the host. The transmission error rate is determined from the number of retransmission commands received and sent by the PUC/DL protocol program. From these data, the host data link state control can take action to remove a link from service if it becomes inoperative or if its throughput is restricted because of excessive data errors.

5.4 Message routing routines

The routines that are responsible for routing data between individual processes in the two machines are executed by the remote terminal and the host processor. These programs assume that data received from the link protocol programs are error free and that any additional error control procedures for detecting transmission errors are unnecessary. These programs are designed to transmit data between buffers associated with client programs in the two machines. A program having data to transmit will load the data into its associated buffer. When the data are completely assembled, the buffer will be activated for the message routing routines and the data will then be transferred to a buffer associated with the destination program.

To facilitate the data transfer, the message routines assemble the data to be transmitted into messages that can be addressed to a particular destination. The RSS message format is shown in Fig. 7. A message is comprised of 16-bit data words, which is a convenient length for both the PUC/DL and the remote terminal processors. The two initial words are a SYNC word and a message header. The SYNC word denotes the start of the message and the header contains the address information necessary to route the message to a particular client program and buffer. It is possible for multiple buffers to be allocated to certain programs, such as the remote terminal call-processing routines, so that multiple processes can be executed concurrently. The message address structure allows data to be routed to an individual buffer associated with a client program by providing a CI

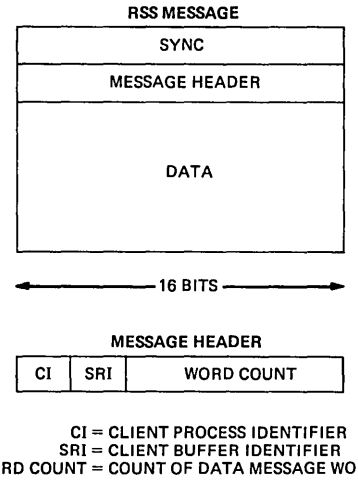

Fig. 7—Remote switching system message structure.

field to identify the program and an SRI field to identify one of its associated buffers. The word count in the header, along with the SYNC word, enables the message routing routines to parse individual messages from the received data supplied by the protocol programs.

5.5 Host data reception

The routines and buffers in the host that handle messages transmitted from the remote terminal are pictured in Fig. 8. The data received by the PUC/DL from the remote terminal are buffered in a RAM memory within the PUC/DL that is accessed from the host in the same manner as an existing scan memory. Message data in the PUC is then transferred to the host programs in two stages. Data are first transferred to a receive buffer in host call store by an interrupt level routine that executes every 25 ms. It is executed frequently enough at this rate to ensure that data from the link will not overflow the scan memory in the PUC/DL. This is necessary since the PUC/DL is not equipped to initiate a data transfer into the host when data are received from the link. In a No. 1 ESS host equipped with a signal processor, this is performed by a signal processor program.

A second routine, executed by the host Central Control (CC) at base level, is responsible for unloading the call store receive buffers and routing messages to destination client buffers. Individual messages are defined in the receive buffer by scanning for the SYNC word at the beginning of a message and using the message word count in the header to locate the final word.

Once a complete message has been received, the client identity (CI)

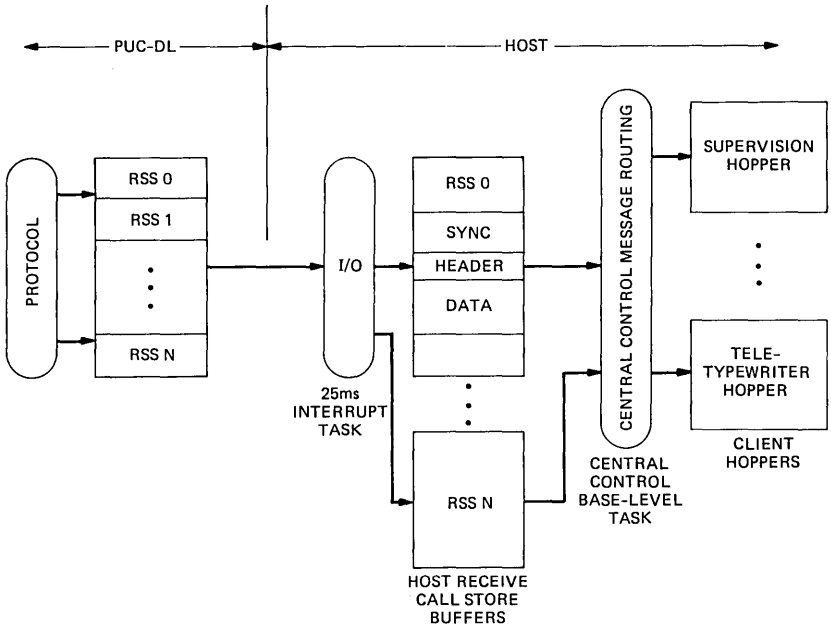

Fig. 8—Host message reception.

and SRI indexes (see Fig. 7) are used to locate the client buffers. A set of routing tables, as shown in Fig. 9, are supplied for each RSS. The primary route table is indexed with the CI in the message header. There are two types of entries in this table. If the client program has a single buffer associated with it, the entry contains the address of the load head cell for the buffer. The load pointer in the head cell enables the routing program to transfer the message from the receive buffer to the client buffer.

If the client program has multiple buffers, the primary route table entry is the address of a subroute table associated with the client program. The subroute tables are indexed with the SRI entry in the message header to obtain the load head cell address for a specific destination buffer. After the message transfer is complete, the client program is alerted to the fact that a message has arrived and is available to be processed.

5.6 Host data transmission

The buffering technique adopted for the transmission of peripheral orders to the remote terminal was designed to be compatible with the structure of the existing host software. The order buffering and message transmission must be tailored to the host software structure if the existing call processing and maintenance routines are to be preserved.

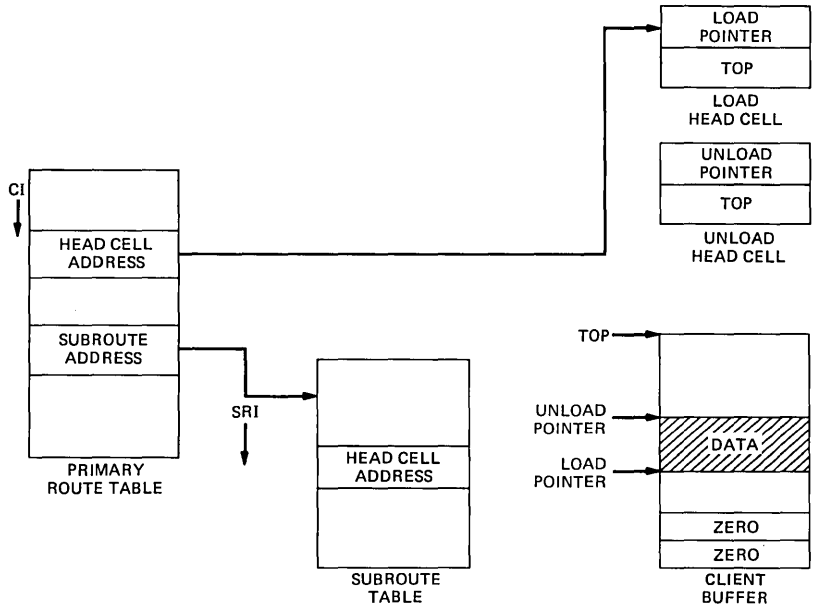

Fig. 9—Message routing tables

A few remarks on the nature of the call processing programs are necessary to understand the interface requirements.

The host call-processing programs are divided into call segments that process an input from a subscriber or a peripheral circuit to completion in one real-time segment (Fig. 10). All the peripheral orders required to process the input are generated by the program segment, but their execution is carried out by a separate set of input/output (I/O) programs. Peripheral operations in the host or remote terminal take tens or hundreds of milliseconds to execute, which precludes their direct execution within the call segment. During execution, a typical program segment may generate several remote terminal peripheral messages that are destined for different RSSs. In most cases, it will also generate a number of orders to be executed in the host periphery in conjunction with the remote terminal actions. The execution routines must be able to coordinate the host-remote terminal peripheral actions and coordinate the transmission of the remote terminal orders to the different RSSs. Frequently, it is necessary to execute the remote terminal-host peripheral actions in a predefined sequence where either the host or the remote terminal action must occur first.

The call processing and maintenance programs are coupled to the I/O programs through a set of I/O buffers that are loaded with the peripheral orders to be executed. All host peripheral orders are

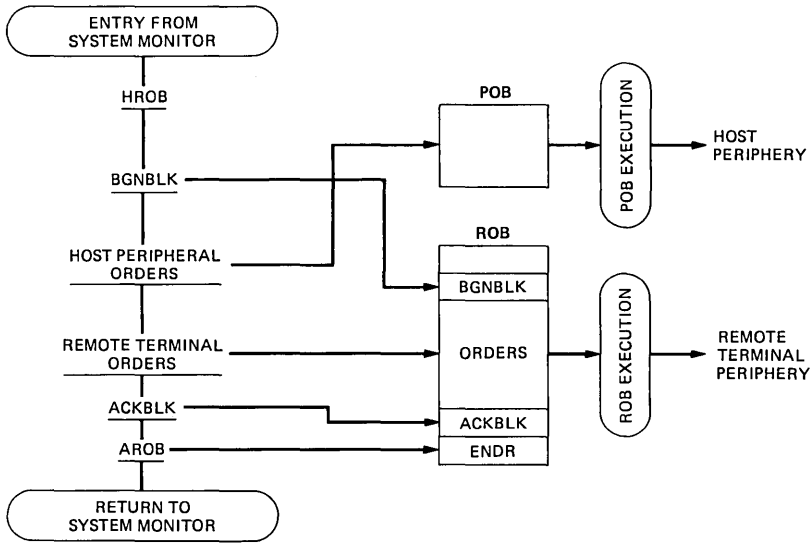

Fig. 10—Remote switching system call segment

buffered in peripheral order buffers (POBs) where they are executed by the POB execution programs, which are designed to handle the timing requirements presented by the host periphery.

A set of remote order buffers (ROBs) are provided in the host machine to buffer the peripheral orders being transmitted to the remote terminals. They are loaded and administered by the call processing programs in the same manner as the peripheral order buffers. Before a set of remote orders is generated, an ROB must be seized from a common pool provided in the host. The orders to be sent to the remote terminal are loaded in the ROB via a set of order macros which provide a high-level interface with call processing. When order loading is complete, the ROB is activated and the I/O routines transmit the orders to the remote terminal. An individual ROB may be used to send orders to any RSS. An administration macro is called before the orders are loaded to specify the identity of the remote terminal to receive the orders. The host can have any number of ROBs pending to send orders to an RSS; however, each remote terminal has a fixed set of eight ROB RECORDS that are used to store orders received from an ROB at the host (Fig. 11). The ROB RECORDS are buffers associated with the peripheral order execution program in the remote terminal that executes the orders transmitted from an ROB. Before the orders are transmitted, an idle ROB RECORD in the remote terminal must be selected by the host and the SRI in the message header must be set up to route the orders to this particular ROB RECORD.

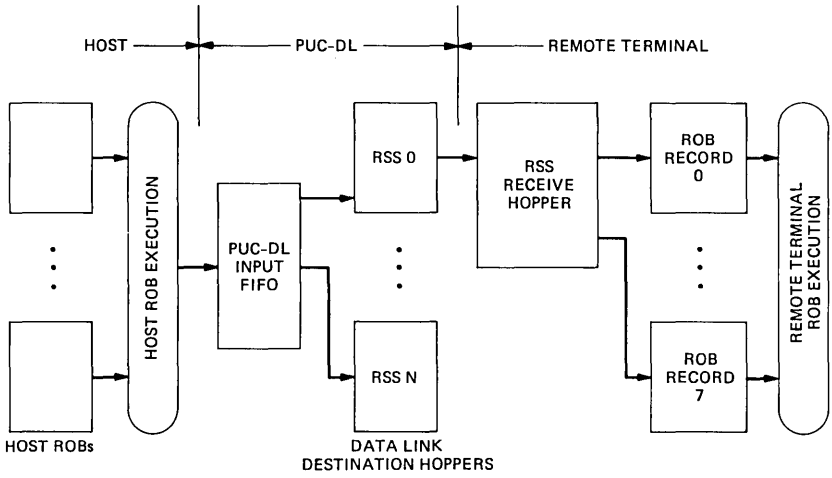

Fig. 11—Host data transmission.

5.6.1 The ROB execution protocol

A rudimentary protocol has been established to coordinate the activities of the call processing routines at the host with the execution of ROB orders at the remote terminal. Several orders will be grouped together into a single message at the host to be transmitted to the remote terminal. The orders in the message are executed at the remote terminal and upon completion an acknowledgment is returned to the host. The acknowledgment will indicate whether all the orders in the message were successfully executed or not and must be received by the host before any further actions will be permitted on this call. If the remote terminal encounters a failure in executing an order, the acknowledgment message will specify the failed order to the host and the remote terminal will suspend execution of all remaining orders in the ROB RECORD.

It is essential to receive a positive confirmation on the status of the orders for several reasons. If an order failure occurs, the host fault recovery routines can be scheduled to clear the call from the system. In addition, the acknowledgment allows the host to correctly sequence any other peripheral actions with the remote terminal orders. When the acknowledgment is received, the host can activate an associated POB or return to a call-processing program to implement the next action on the call. The restriction that additional RSS orders will not be transmitted until the acknowledgment is received also prevents the host from transmitting multiple sets of orders for the same call that would be executed in an arbitrary sequence at the remote terminal.

5.6.2 The ROB Entries

Two types of entries are loaded into an ROB. There are peripheral orders to be transmitted to the remote terminal and subroutine calls to be executed by the ROB execution program. The ROB subroutines are used to implement the message protocol and control the data transmission to the remote terminal. Figure 10 depicts the ROB loading and administration operations involved in a call segment for an RSS call. An ROB is hunted at the beginning of the segment (HROB), and a Begin-Block (BGNBLK) subroutine address is loaded in the ROB by the BGNBLK macro. When the BGNBLK routine is executed by the ROB execution program, it will identify the RSS, the subsequent ROB orders are to be sent to, and will also select an ROB RECORD at the remote terminal to receive the transmitted orders. Following BGNBLK, the set of orders to be executed at the RSS are loaded in the ROB by a set of order macros that format the order data and place it in the ROB. After the last order is loaded, an Acknowledgment-Block (ACKBLK) macro is called to terminate the loading process. This ACKBLK macro will set a flag in the last order loaded in the ROB to indicate that an acknowledgment should be returned by the remote terminal after the order is completed. In addition, an ACKBLK routine is loaded in the ROB to process the acknowledgment message when it is returned. If all orders were successfully executed, the ACKBLK routine passes control to the next entry in the ROB. If a failure is indicated, the fault recovery routines will be initiated to tear down the call. The final entry in the ROB is made when the ROB is activated for execution. The Activate-ROB macro activates the ROB to permit the ROB execution routines to process it and loads the ROB with the address of an END-ROB (ENDR) routine. Upon completion of the ROB activities, ENDR will initiate the next program segment required for the call. This may be the POB execution program or it may be a predefined call processing segment that will handle the next stage of the call.

Sequencing the execution of ROBs and POBs is necessary to control the order in which the host and remote terminal actions are carried out. This control is provided by the ENDR routines that are loaded in the POB and ROB on activation. The ENDR routines provide the capability for ROBs and POBs to be sequentially executed in either order or for the ROB and POB to be executed simultaneously. Simultaneous execution is used where it is important to minimize call setup delays and where the host and remote terminal actions can occur independently of one another. Control will be returned to the call processing client after both the ROB and POB actions have been fully completed.

VI. THE RSS CALL PROCESSING CONTROL

The RSS host call-processing software provides an ESS central office

with the capability to supply ESS features to lines served by the RSS. Since most of the call-processing functions for RSS lines are performed by the host ESS office, a full family of ESS features can be provided to the remote subscribers. The RSS call-processing software resident in the host ESS provides the means of controlling a remotely located switching system by taking advantage of existing equipment and control capability in the ESS. Firmware in the remote terminal supplements the host call-processing software appropriately. All call-processing control resides in the host ESS and any required actions at the RSS are requested via data link messages to the RSS. This permits the host to exercise total call control.

6.1 Originating call

A line originating in the RSS is first recognized during line scanning performed by the RSS microprocessor. The RSS line-scanning program in the remote terminal recognizes the line off-hook, performs timing to ensure the origination was not a transient "hit," and sends an origination request data link message to the host ESS. The host performs originating translations on the line. If service is allowed, it marks the RSS line busy and hunts an idle voice channel between the RSS and ESS. It also hunts a path through the RSS network from the originating line to the selected voice channel, and selects a customer digit receiver in the host, along with a host network path from the voice channel to the receiver. A Remote Order Buffer (ROB) is then executed to send appropriate data link messages to the remote terminal to set up the RSS network path. Messages are also sent to set the line supervision mode to repeat supervision of the originating line over the channel in the dialing (fast repeat) mode. This ensures that the dialed digits will be received properly by the host digit receiver. If the originating line is identified in translations as a two-party line or a line associated with a sleeve lead (or remote distributor point), appropriate data link messages are also included in the above ROB to perform a party test or operate the remote distributor points, respectively.

Upon successful completion of the data link orders in the remote terminal, the host then executes orders to its periphery [via a Peripheral Order Buffer (POB) mechanism] to set up the host network path between the voice channel and receiver to provide dial tone.

Processing of the call from this time on proceeds basically the same way as an origination by a host line. Digits are collected and analyzed by the same host software used to process host calls. At the completion of dialing and digit collection, a data link message is sent from the host to the remote terminal to set the line supervision mode to repeat the supervision of the originating line over the channel in the talking (slow repeat) mode to conserve remote terminal microprocessor real-time capacity.

The RSS originating call, from this point on, is routed and completed normally (excluding terminations to RSS lines) just as non-RSS line origination processing. This originating call configuration is depicted in Fig. 12 for a call that terminates in the host office. Upon answer by the called party or, for calls to other offices upon completion of outpulsing, the talking connection is established from the voice channel through the host network. In Fig. 12, this is shown by completion of the junctor (JCT) connections. The RSS answer timing, billing, traffic, and other administrative functions are all performed by the host just as for non-RSS calls. If the call terminates to an RSS line, special terminating RSS functions are performed as discussed in the following sections. When either the calling or called parties disconnect, disconnect functions are performed as discussed in Section 6.5.

6.2 Terminating call

An RSS terminating call is recognized when the host ESS performs the called number [terminating directory number (DN)] translations from digits collected from an originating host line or trunk. The RSS lines are distinguished from host lines by special RSS indicators in the terminating line translation output. After the translation is completed, special actions, as with the RSS originating call, are required to set up ringing. The host hunts an idle voice channel to the RSS, hunts a path in the RSS network between the voice channel and the terminating line, and seizes idle host ringer (whose function is explained below) and audible service circuits with associated host network paths to the voice channel and originating line or trunk, respectively. In addition,

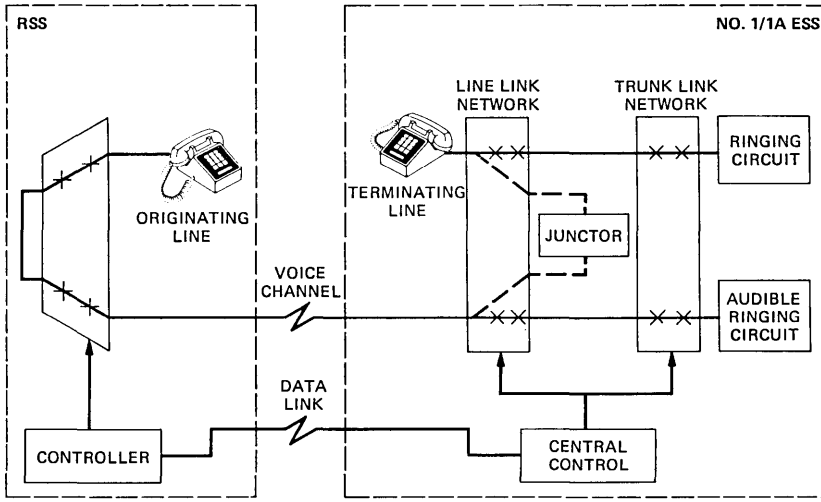

Fig. 12—Remote switching system originating call.

a talking path through the ESS network between the voice channel and the originating line or trunk is reserved.

An ROB is activated to send data link messages to the remote terminal to connect the terminating line to the voice channel and apply ringing to the line. Upon receipt of the data link orders, the remote terminal selects an idle universal service circuit (USC), along with a metallic bus and time slot to provide the type of ringing specified in the data link message. Supervision of the line is transferred across the voice channel to the host in the fast repeat mode. As with the originating call setup procedure, appropriate data link messages are included in the above ROB and sent to the remote terminal to operate sleeve leads or remote distributor points if so indicated in the output from the terminating line translations.

Upon successful execution of the ROB data link orders in the remote terminal, the host executes a POB to set up paths in the host network from the voice channel and the originating line or trunk to its associated service circuit. Power cross and low-line-resistance tests are done on the voice channel from the host ringing circuit. The host ringing circuit is then left in a state to monitor ring trip sent by the remote terminal over the voice channel to the host. Actual ringing is applied to the line by the USC at the remote terminal; the ESS host ringing circuit does not apply ringing voltage to the voice channel, but is only used to monitor for ring trip. This call configuration, as shown in Fig. 13, maximizes use of the existing terminating call sequences in the host.

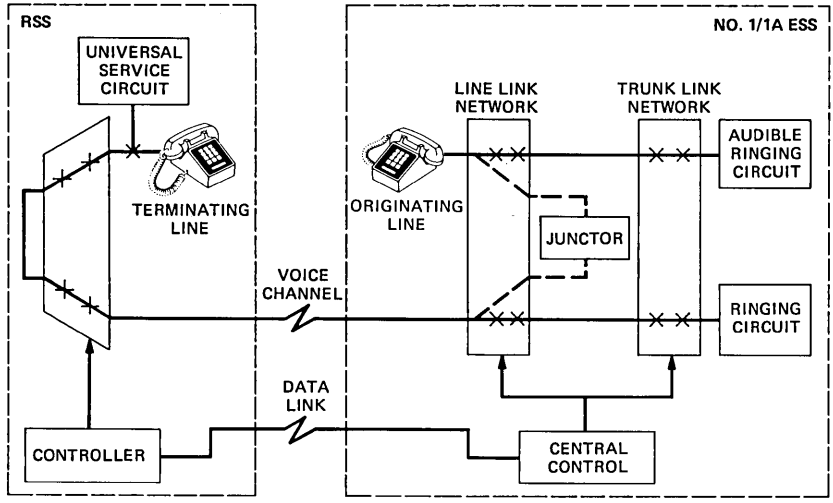

Fig. 13—Remote switching system terminating call.

When the called party answers, the remote terminal automatically releases and idles the ringing facilities (USC, metallic access bus, and time slot) and relays the ring trip report (off-hook signal) of the line across the voice channel and sets the supervisory mode to slow repeat.

The host ESS detects answer over the voice channel at the ringing service circuit, tears down the ringing and audible circuit connections in the host, and sets up the talking path that was previously reserved between the voice channel and the originating line or trunk. If the originating line in the RSS terminating call description is actually another voice channel to the same RSS as the terminating line, the call is considered an intra-RSS call and special actions are invoked as described in Section 6.4.

Disconnect actions are identical to those for the RSS originating call, except for the disconnect timing associated with the terminating versus the originating party.

6.3 The RSS reverting calls

The RSS reverting calls involving a call between two parties on a party line are handled similar to host reverting calls. However, ringing is provided similarly to the way it is applied on RSS terminating calls, with the exception that two time slots are needed in the RSS remote terminal so that ringing can be applied to both customers. Each RSS has its own ringing office option as defined in translations. This RSS ringing option, which can be either ac/dc or superimposed, is completely independent of the host ESS office ringing option, or any other RSS served by the same host. The RSS universal service circuit has the capability to provide either ringing option under firmware control.

6.4 Intra-RSS call

An intra-RSS call, where both the originating and terminating parties are served by the same RSS, is handled initially as a combination of an RSS originating call and an RSS terminating call. After answer, the host initially establishes a talking path within its network between the two voice channels. Immediately following the establishment of this talking connection, certain RSS actions are invoked to reswitch-down the call so that the talking connection resides entirely within the RSS network, thus releasing the ESS network path and voice channels for use on other calls. The call is initially set up through the host network, then followed by a reswitch-down. This two-step process maximizes the use of existing host line-to-line call setup routines and provides for a well-defined interface with the reswitch-down software module.

The reswitch-down action is initiated when the host hunts an intra-RSS network path between the originating and terminating lines. An ROB is activated to send data link orders to the remote terminal to

disconnect both line-to-channel network paths and connect the two lines through the RSS network. The supervisory mode of the RSS lines is set to scan for either a disconnect or switchhook flash, depending on the features associated with each line. Since the intra-RSS connection is entirely within the RSS, a change in supervisory state of the line must be reported over the data link to the host. The sequence of intra-RSS call configurations including reswitch-down is illustrated in Fig. 14.

If a network path in the RSS is not available, or one of the lines is an RSS coin line, the intra-RSS call is not reswitched-down and remains connected through the host ESS network. Intra-RSS calls involving coin lines are not reswitched-down in order to utilize host coin disconnect routines and thus, simplify disconnect actions.

The use of various custom calling services or other special services requires a reswitch-up of an intra-RSS call to establish a talking path between the two parties via the host network using two voice channels. This allows existing host software and equipment to be utilized to provide these customer services. The following operations require a reswitch-up operation on an intra-RSS call.

(*i*) A flash by an RSS customer to add on a third party.

(*ii*) A terminating call to one of the two parties of an intra-RSS call that has the call waiting-terminating feature.

(*iii*) A busy verification test of one of the two parties of an intra-RSS call by an operator.

When the host determines that a reswitch-up function must be performed, for any of the reasons given above, the host seizes two idle voice channels to the RSS and hunts a path between them in the host network; the host also hunts a path between the two voice channels and both lines in the remote terminal. A POB is executed in the host to set up a talking connection between the two voice channels. Following this, an ROB is executed to send data link messages to the remote terminal to disconnect the intra-RSS talking connection, connect each line to a voice channel, and set the supervisory state of each line to the talking mode (repeat supervision of the line over its respective voice channel). Once the intra-RSS call is reswitched-up to a talking connection via the host ESS network, the original service requested can be provided just as it would to a normal line-to-line connection of two host lines.

6.5 Disconnect functions

Disconnect actions for RSS calls are a function of the particular call configuration involved, i.e., intra-RSS calls or RSS calls through the host network. For call configurations involving both RSS and ESS paths, the ESS disconnect programs control the call disconnect actions. The same disconnect sequence that is performed on ESS host lines is used on RSS

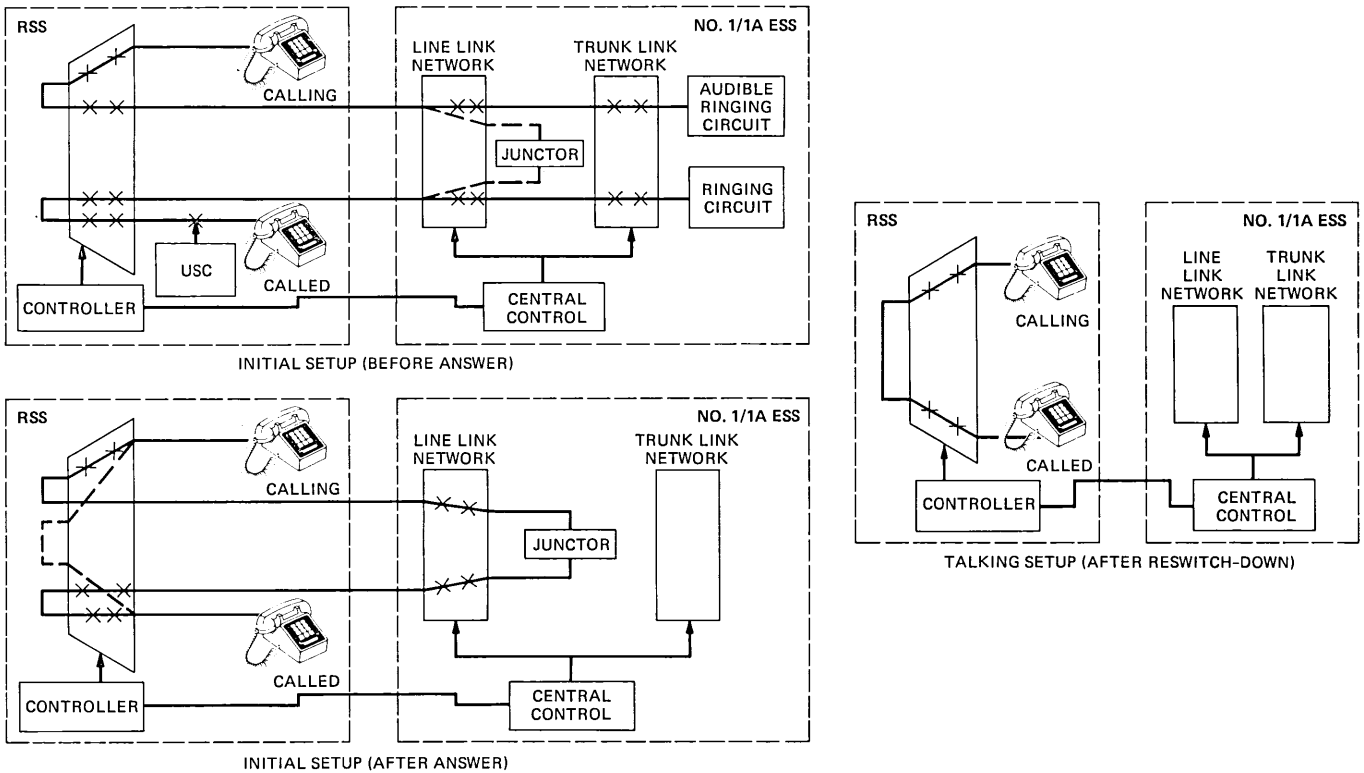

Fig. 14—Intra-RSS connection sequence.

channels that terminate on the host line network. This disconnect control strategy provides the ability to centrally recognize an RSS channel during normal host disconnect processing. This recognition occurs when ESS programs perform a restore verify action on the RSS channel (restore the channel's line ferrod to the idle state and verify that it can detect an off-hook signal). At this point in the host disconnect processing, unique host RSS disconnect modules are invoked to disconnect the RSS network path. The normal host disconnect program and RSS disconnect module then autonomously complete their respective disconnect actions. The only common resource between the two control programs is the RSS channel. The ESS host disconnect program administers the host end of the channel on its network, and the RSS host disconnect program administers the RSS end of the channel on its network. After both ends of the channel are idled, the channel is then available in the host for reallocation to a new call.

In the case of an intra-RSS call, where the call configuration involves a connection totally within the RSS network and no channels or ESS network paths are involved, the RSS lines are supervised in the 10A RSS. Hits, flashes, and on-hooks are detected by the RSS; flashes and on-hooks are reported to the ESS host via data link message. These messages are routed to unique RSS disconnect control modules in the host for proper processing. In the case of an on-hook, these programs perform the proper disconnect timing and then execute ROBs to disconnect the intra-RSS network paths and idle the lines involved. The intra-RSS call is reswitched-up on receipt of a flash message (as discussed in Section 6.4).

VII. DATABASE INTEGRITY

In an electronic switching system, the status of resources and telephone calls are recorded in temporary memory. These data can become mutilated because of program bugs, hardware errors or program design errors, resulting in the loss of resources or system degradation. The problem is further complicated in RSS because parts of the new data structures in the host ESS are duplicated in the remote terminal. The new structures are

(*i*) PMRs for lines
(*ii*) PMRs for channels
(*iii*) Network map
(*iv*) Remote order buffers (ROBs) and
(*v*) Remote miscellaneous scan point map.

The actual data stored in the two copies of these structures are not identical in all cases since the host and remote terminal do not perform identical functions. For example, the state stored in a line PMR at the remote terminal represents the supervisory state of the line (origina-

tion, repeat supervision onto a channel, high and wet, etc.), whereas the state in the host PMR represents both the status of the line (idle, busy, maintenance) and the type of path memory configuration, as discussed previously. However, there is a mapping between the two sets of states in that the host line state implies the possible supervisory states of the line. Deviations from this mapping should only be because of the time lag of the data link.

To ensure the integrity of the data structures, the first step is to prevent as many errors as possible. The RSS software applies many of the techniques that have been successfully used in other ESS projects to avoid potential causes of errors. Some of these are good documentation, standardized program interfaces, structured design, structured programming, a high-level programmer's language, and a standardized data definition language. In addition, access to the new data structures introduced into the host is limited to the administrative programs that have the responsibility for that particular database.

The second step is to make the programs as error tolerant as possible since data errors will still occur. The main technique for this is defensive programming. The degree to which a data error is propagated through the system depends upon how the programs use the data. To have a minimal effect upon the system, programs should account for bad data. Some specific types of defensive coding techniques are

(*i*) Range checks on data to prevent overindexing tables.
(*ii*) Accounting for all possible subroutine return code values.
(*iii*) Use of symbolic definitions for data values.
(*iv*) Accounting for all possible program inputs.
and
(*v*) Invalid data value checks.

Despite the preventive and defensive techniques that are employed, errors can still occur in the data. Programs are required to detect these errors and restore the facilities to the proper condition to avoid system degradation. The audit programs are responsible for detecting and correcting data errors and the initialization programs are responsible for restoring system facilities when the degradation is severe enough to cause major system degradation.

7.1 Audit programs

The integrity of the data structures is checked and corrected by a set of audit programs. Each audit program is individually tailored to a specific data structure or group of data structures and determines if the data items follow certain established rules. If the checks fail, the audit programs idle all resources (both software and hardware) associated with the particular error and print error messages on the teletypewriter. The audit programs also aid in the initialization of the data structures.

As previously discussed, the RSS system has new data structures in the host ESS that are duplicated in the remote terminal. From a call processing viewpoint, the remote terminal functions as a slave to the host, executing the various orders sent to it. The remote terminal updates its databases as a result of the orders received from the host. Orders involving lines or channels cause the remote terminal to set its PMR to the supervisory state appropriate to the order. The network map bits are set to busy or idle when it receives a setup or tear-down order, respectively. Although the host is the controlling entity, calls can be lost or service can be denied a customer if the data stored in the remote terminal are not consistent with the host data. For example, if the host has a line in the origination state and the remote terminal has supervision turned off on that line, the customer will not be able to originate since the remote terminal would never detect the off-hook. Thus, a means must be established to ensure that service or facilities cannot be lost because of differences between the two data structures. In addition, the data structures must be internally consistent within each entity independent of the synchronization problem.

The audit philosophy adopted for RSS is that each entity (host or remote terminal) will maintain the integrity of its databases independently. If the host finds a discrepancy in its database, it corrects the problem by idling all host resources involved and instructs the remote terminal to put its facilities into a known (usually idle) state. If the remote terminal finds a discrepancy in its database, it sends a message to the host and the host audit programs initiate the actions given above.

Thus there are three classes of audits associated with the RSS system:

(*i*) Host audits that maintain the internal integrity of the data structure in the host.

(*ii*) Remote terminal audits that maintain the internal integrity of the data structures in the remote terminal.

(*iii*) Audits that guarantee that the host and remote terminal data structures are consistent.

Audit classes 1 and 3 are discussed below.

7.1.1 Host audits

Existing host audits are extended to include the new data structures and new data values introduced with RSS. The main audit modifications are for the RSS path memory, the RSS network map, channels, and ROBS.

The RSS path memory and network map are audited by making the following checks:

(*i*) Point-to point-back checks are performed between PMRs and PMJs; that is, a PMJ that is pointed to by a PMR must contain the REN associated with the PRM.

(*ii*) Point-to point-back from a PMR or PMJ to a call register if linkage to a call register is indicated. In this case, a PMJ contains the REN of one of the terminals involved in the path and the call register contains an REN or LEN of the channel.

(*iii*) The junctor busy-idle bit in the network map is checked to ensure that it is idle if and only if the PMJ is idle.

(*iv*) Each of the network map bits that is marked busy is checked to guarantee that it is in a valid path.

Additional checks are performed on channels to ensure that every idle, equipped channel is on the idle link list, to ensure that the idle link list only contains equipped idle channels and that the associated host line bit for the channel is idle if the PMR is idle. The latter check requires timing since the two ends of the channel are idled autonomously, and thus the status of the two ends can be out of step for a short interval.

The ROBs are audited by periodically rebuilding the idle link list and by timing busy ROBs. If an ROB remains busy for an extensive length of time, the ROB and any associated call register are idled. All paths and circuits are also idled. The corrective action taken by the host audits is to idle facilities (hardware and software) in the host and to send orders to the remote terminal to cause the facilities at that end to be idled.

7.1.2 Synchronization between host and remote terminal

The problem of maintaining the data structures in the host and remote terminal in synchronization is greatly simplified by taking advantage of the normal system operation. The remote terminal updates its data in response to orders from the host. Bits in the remote copy of the network map are marked busy or idle in response to orders to set up or tear down network paths. Thus, no network map audit is required between the host and remote terminal since the host does the hunting and idling of paths and the remote copy will trend towards the proper state even if it does temporarily get out of step.

Similarly, ROBs are controlled from the host end and normal operation will result in the remote copy being brought back into step with the host.

The remote terminal audits check that all equipped lines have supervision turned on. Any equipped lines that are unsupervised are reported to the host via a data link message. If the host audits determine that the line state really calls for supervision to be on, the line and any associated resources are idled.

Periodically, the host sends a copy of its version of the remote scan point map to the remote terminal which overwrites its map with the host's data. If the hardware state of the scan point differs from the

map, the normal scan program will detect this as a change and report it to the host, resulting in both copies being brought back into step.

7.2 Remote terminal initialization

System initialization programs are responsible for correcting errors that prevent the system programs from cycling correctly. The initialization programs are usually executed as a consequence of errors being detected by the processor check circuits that monitor the sanity of the system operation. In the remote terminal, the primary checks for monitoring proper program operation are the system sanity timer which monitors the main program cycle time, the write protect circuitry which prevents illegal writes into program store and certain peripheral error checks which detect attempts to access unequipped areas of the periphery. If any of these errors are detected, it is indicative of an error in the system database and the method of recovery is to initialize a segment of the data and then return to the normal program cycle.

Since the initialization process inherently destroys a portion of the call-processing data, a corresponding set of calls will be lost, and it becomes a requirement for the initialization program to release the peripheral circuits associated with these calls. Any network links, channels, or service circuits employed on these calls must be idled by the initialization program before a return to normal system operation is begun. This is accomplished by releasing all the circuits that are marked idle in the initialized database.

Whenever an error is detected by a fault detection circuit, a processor interrupt is generated that executes the fault recovery programs. Various fault recovery actions are taken, depending on the type of errors detected and their frequency. As the result of a write-protect error or a sanity timer timeout, the off-line processor complex may be switched on-line and some degree of data initialization performed, depending on the number of errors that have been detected within the recent past.

The amount of data that is initialized on the first error is small. As successive errors are detected the serverity of the initialization is increased with the consequent loss of progressively greater numbers of calls. The ultimate action is to initialize the entire database and restore the system to an idle state. The goal of handling the fault recovery in stages, with increasingly more severe initializations, is to restore the system to a working mode with the loss of a minimal number of calls.

At either the remote terminal or the host, there are three fundamental levels of initialization: a minimal clear, a transient clear, and a stable clear. A minimal clear involves the initialization of the variable data associated with the active processes in the system and has the potential of disrupting at most several calls. A transient clear will

initialize all the data in the system that is related to any call in progress. All calls in the process of being established or disconnected will be lost; however, calls in a stable talking state will be preserved. The final stage of initialization is a stable clear where the entire database is reinitialized and all calls are lost.

For the RSS system, the initialization process is somewhat more involved than normal because the host and remote terminal databases are interrelated and an initialization level (phase) in one machine affects the database of the other system. Although the host machine is responsible for the control of the remote terminal on a call-related basis, the operation of the processors in the two machines is fairly autonomous with respect to their instantaneous activities. This is the situation for fault detection where the two systems are entirely independent. Each machine is responsible for initializing and carrying out is own fault recovery actions and the level of the accompanying initialization will be solely determined by the conditions within the machine that detected the error. In effect, either machine is able to initiate any level of initialization on its own database independently of the other. However, as part of the initialization procedure, the hardware and software within the two machines must be synchronized so that the databases reflect a consistent set of calls. The calls that were destroyed in one machine must be reported to the other so they can be cleared from that system also. For example, a host transient clear will destroy a number of calls that involve remote terminal lines. These calls must be cleared in the remote terminal so that periphery and call records are in agreement with those in the host.

The exact procedure for synchronizing the two machines will depend on which system has initiated the phase. Since the host is in charge of call control, its call records are regarded as the master copy and the remote terminal state is brought into agreement with its set of records. The host is, therefore, in charge of synchronizing the two machines.

Whenever a phase occurs in the host, the synchronization procedure is straightforward. The host will initialize its database and periphery and will then send initialization orders to the remote terminal to bring it into agreement with its updated records. When the remote terminal undergoes an initialization, it reports the level of the initialization to the host. In some instances, on a stable clear for example, this is sufficient information to allow the host to initialize its database. In the case of a transient clear, it is also necessary to transmit a map of the lines that are in a transient state in the remote terminal. From the data specifying the initialization level and the map of transient lines, the host is able to update its call records and periphery. Once this is accomplished, it will conduct an initialization of the remote terminal in the same manner as for a host-initiated phase.

VII. SUMMARY

The host RSS software supplies a local ESS with the capability to control a 10A RSS. The major call control resides in the host, with the 10A RSS acting as a slave in executing orders from the host.

This paper has described the major host software functions required for implementing the RSS feature on a host ESS. These major functions are RSS resource and data administration, the RSS message handling, and call processing and database integrity. The host RSS software is structured to meet system requirements to provide easy portability among local ESSs, to provide the capability of giving RSS lines the same features as host ESS lines, to minimize the effects on host capacity for non-RSS calls and to easily make new host features available to RSS lines.

IX. ACKNOWLEDGMENTS

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No. 10A Remote Switching System:

Physical Design

By C. E. JESCHKE, A. E. KRANENBORG, and B. S. THAKKAR

(Manuscript received June 9, 1980)

I. INTRODUCTION

The physical design objectives of No. 10A Remote Switching System (RSS) were to package the system into as compact a design as possible to allow for easy adaptation to both CDO and pair gain applications, to maintain an economic advantage over other alternatives, and to provide ESS service requirements. The interconnection technology was chosen to permit a 1024-line system to be contained in a single frame and to maximize the use of least-expensive interconnection techniques. Circuit partitioning and frame engineering rules were devised to minimize equipment growth, which minimizes installation cost, and to maximize plug-in apparatus growth, which keeps more costly circuit equipage at a minimum. The single (−48 volt) power requirement and low-current drain [less than the step-by-step (SXS) equivalent] allowed minimum and often reuseable battery plant requirements. The small system size resulted in reuse of existing buildings or use of a small portable modular building. The circuit partitioning and system design was implemented to ensure ESS central office service objectives. Because of the short time between manufacture and service, burn-in of electronic circuitry was instituted to minimize the impact of infant mortality on early service. Low cost was also carried into the sparing philosophy by using predicated performance data in conjunction with accepted centralized spare stocking strategies to identify a minimum spare stock which achieved required service objectives. Each aspect of the No. 10A RSS physical design taken together provides a low-cost, small-size, highly reliable electronic switch which will further extend the market coverage of electronic switching systems.

II. INTERCONNECTION TECHNOLOGY SELECTION

Two system requirements, low cost, and small size, were the driving consideration for selecting an interconnection technology. Low cost was important to maintain an economical advantage of RSS over the alternate choices. In the application of No. 10A RSS to CDOs the alternate economic choice is to maintain the existing electromechanical switching system. For pair-gain applications, the alternative is to provide cable pairs for outside plant growth. Small size was important to simplify the application of electronics to the outside plant. So, in choosing a packaging technology, size and cost were of paramount importance.

A review of the interconnection choices shows four possible levels of interconnection. The first level is within components. This, in general, provides the most dense and least-expensive method and so was chosen to be used as much as possible. The second level of interconnection is the large film circuit or the printed wiring board (PWB) which is connectorized to be pluggable for maintenance reasons. This is the second least-expensive interconnection technique providing the proper technology is selected. The third level is automatic machine wiring between connectors. Since this interconnection technique requires the use of connectors, its cost is greater than level one or two costs, and its use should be minimized. The fourth level is that of inter- and intra-frame cabling. Both are the most expensive technique for interconnection and were used as little as possible in the RSS design.

2.1 First level: components

The first level of interconnection consists mostly of integrated circuits, resistors, capacitors, and transformers. Since IC interconnection is by far the least expensive, its use was to be maximized. IGFET technology was utilized wherever possible because of its high density packaging characteristics. The nature of the circuit design is to use many discrete components other than IC. Therefore, finding the room to mount the components is a much more difficult problem than interconnecting them. To help alleviate this constraint, high-density components are required. Therefore, extensive use of R-DIPs was made which provided, at the same cost, a three-to-ten-times increase in packaging density. Also, a new family of transformers was developed using the ferrite core technology which offered a four-times increase in component density (see Fig. 1). Two custom integrated circuits (ICs) (the Battery Feed IC, and the Control Logic IC1) were developed to significantly reduce the interconnection cost of the line circuit. They, as well as the discrete version of these circuits, are shown in Fig. 2. Thus, to make maximum use of the first level of interconnection, the

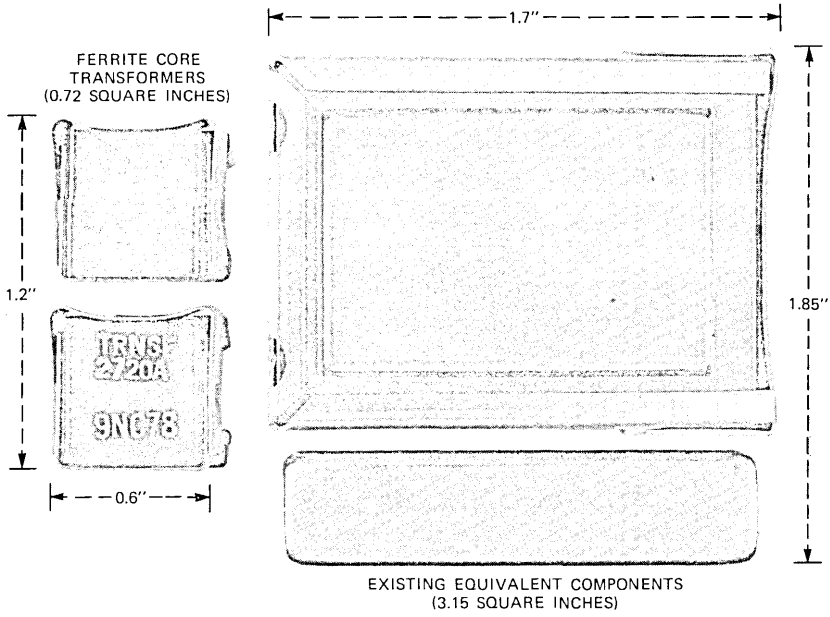


Fig. 1—Space savings of ferrite core transformers.

highest level of integration among ICs, as well as the smallest size among discrete components, was selected.

2.2 Second level: printed wiring boards

The second level of packaging required the interconnection of many discrete components, as well as ICs available in the DIP form. Therefore, PWBs, as opposed to a hybrid technology of film on ceramics, were selected as the second-level technology. An examination of the various complexities of interconnection versus cost for PWB technology is shown in Fig. 3. The interconnection complexity required for No. 10A RSS ranged from *F* through *G*, which is a relatively flat part of the curve giving increased interconnection complexity for little cost increase. Board size was reviewed to determine what effect it would have on cost of second-level interconnection. It has an almost linear relationship between size and cost so that size could be selected more on third- and fourth-level interconnection consideration than on second-level interconnection cost.

2.3 Third level: circuit pack connection system / unit wiring and backplanes

Third- and fourth-level interconnections are determined by the partitioning of circuits onto PWB which implies something about the

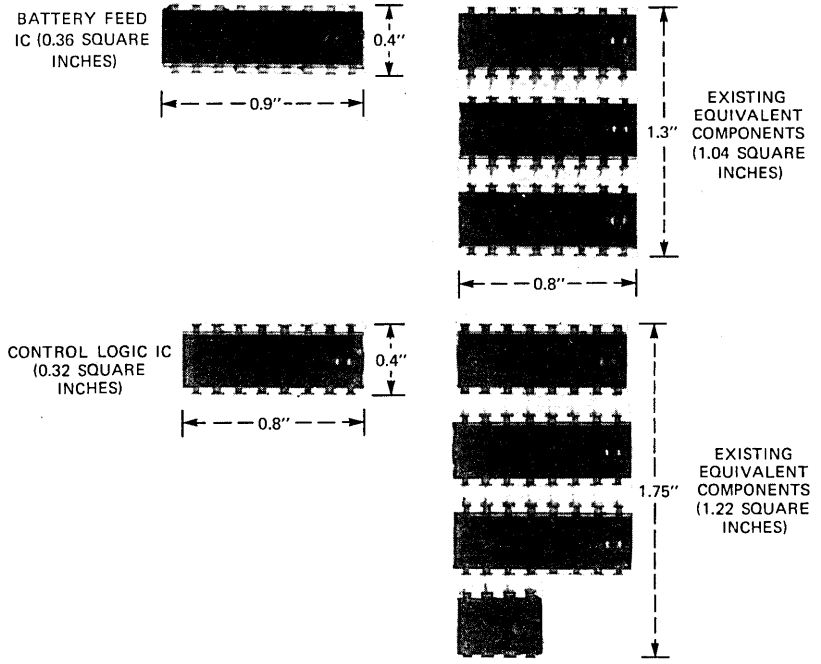


Fig. 2—Space savings of battery feed and control logic ICs.

size of the PWB and the placement of the circuit packs within the framework. The larger the PWB, the more interconnection is done at the less-expensive second level. Also the larger the PWB, the more circuitry can be placed within the physical constraint of an automatic wiring unit (20 by 39 in.). Increasing the circuitry within these automatic wiring constraints results in more interconnection being done by the less costly third level and less interconnection by the most costly fourth-level cabling interconnection. This is most dramatically shown in Fig. 4, which shows a comparison of a 1760-line RSS system partitioned onto 4- by 7-in. circuit packs for the entire system with one line circuit per circuit pack and an 8- by 13-in. circuit pack with 8-line circuits per circuit pack. Notice the significant difference in size, cost, and number of codes and packs which the two partitionings offer. The RSS utilized the 8- by 13-in. circuit packs with 8-line circuits per circuit pack. Any larger size partitioning did not offer much of a decrease in size or cost and was, therefore, not selected.

A circuit pack connector system was developed to meet the following requirements. The majority of the circuit packs (70 percent) required pin-out densities of less than 80 pins per circuit pack, while the

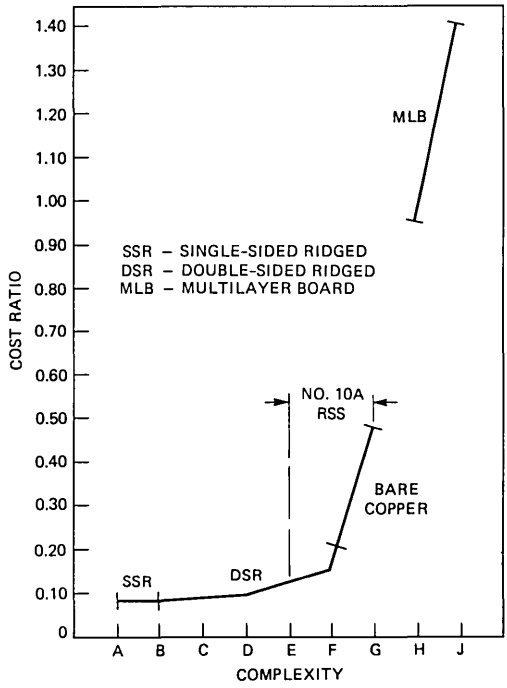
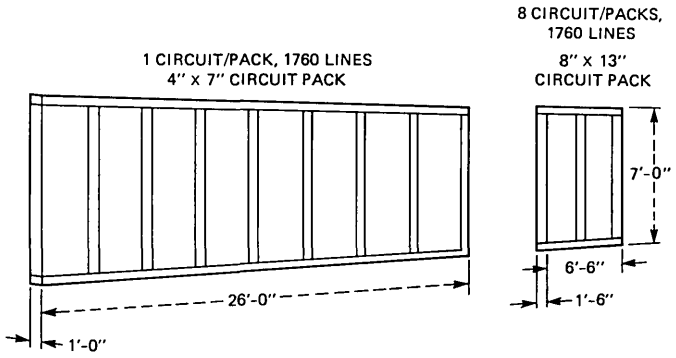


Fig. 3—Printed wiring board technology.



	RATIO	8 CIRCUITS / 1 CIRCUIT
CODES	0.4	
PACKS	0.2	
VOLUME	0.4	
LINE-UP	0.25	
COST	0.6	
FLOOR SPACE	0.3	

Fig. 4—Remote Switching System partitioning (one circuit per pack versus eight circuits per pack designs).

remaining 30 percent required pin-out densities of between 81 and 160. Thus, the connector family would have to have a low-cost member which would provide the low-density interconnection, but with a compatible member which would provide the higher density where required. To keep the third- and fourth-level interconnection cost minimized, the connector family had to be compatible with automatic wiring, PWB interconnection in the backplane, and direct connectorization to the wire wrap pins for cabling. A three-sequence connect was required to allow circuit packs to be plugged into operating frames without disrupting service. The required sequence upon circuit-pack insertion is ground, power, and signal. To meet the above requirements, new members of the 1A technology family of connectors were developed, and a ground first applique contact was developed. The connectors are shown in Fig. 5. The redesign was necessary to provide extension of the power and ground pins to ensure the proper power sequence required. The ground first contact is shown in Fig. 6. It is a solder-plated bifurcated contact which appliques to the connectors. A solder pad is designed onto the circuit pack as part of the usual artwork. The combination of the two provide a moderate resistance (less than 10 ohms) ground contact which mates with the circuit pack

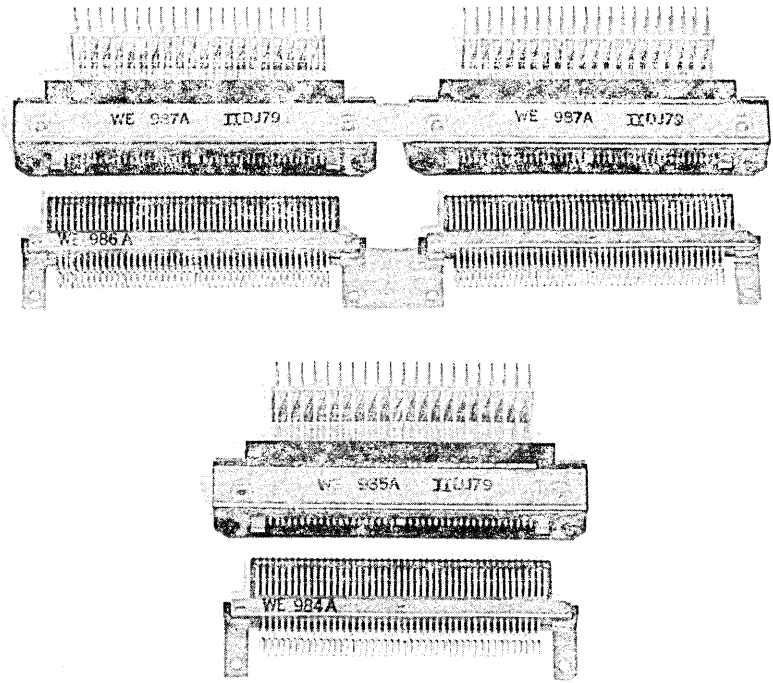


Fig. 5—Remote Switching System circuit pack connectors.

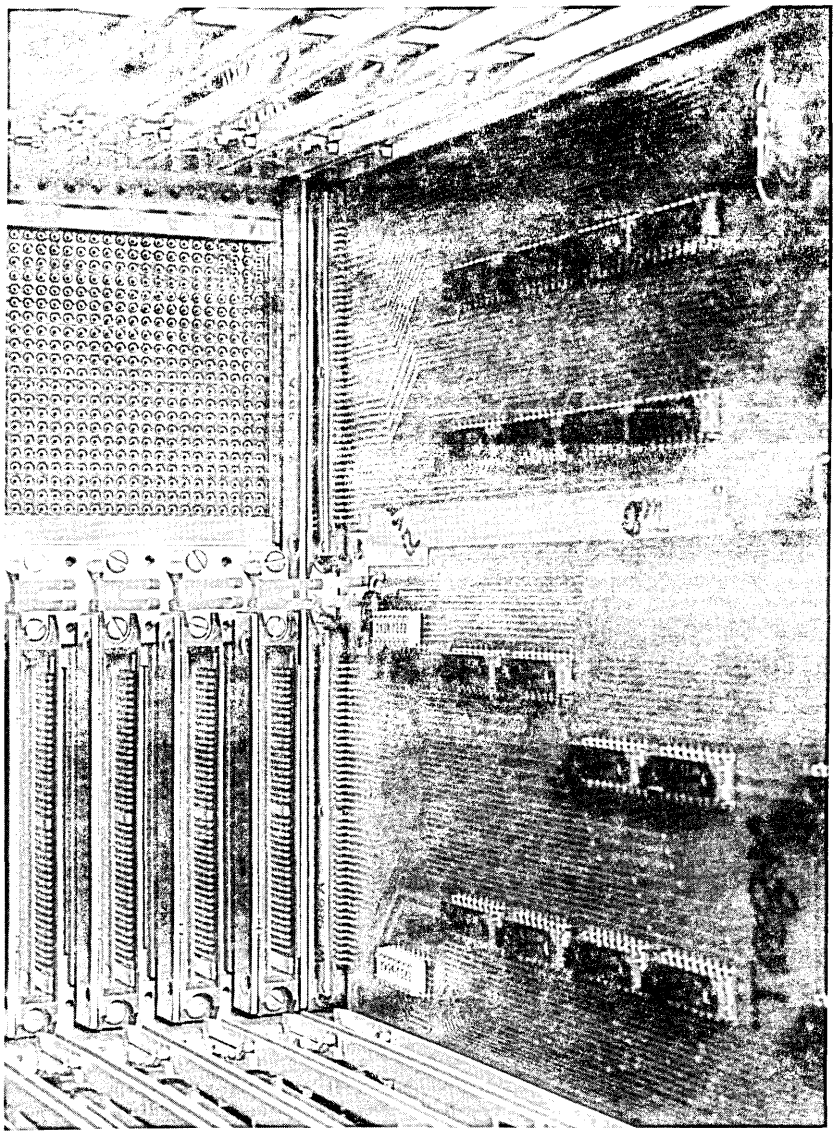


Fig. 6—Ground-first contact.

before the 980-type power contacts mate and, thus, provide the third and initial contact sequence.

The backplane interconnection is realized by a combination of printed wiring, automatic wiring, and connectorized cabling. All power and ground interconnections within a unit are realized by a double-sided PWB with solid segments of power and ground paths on both

sides (see Fig. 7). This interconnection technique is much less expensive than the alternative hand termination of large-size power wires multiplying to each connector.

2.4 Fourth level: cabling

Connectorized cables were used because they allowed easy growth

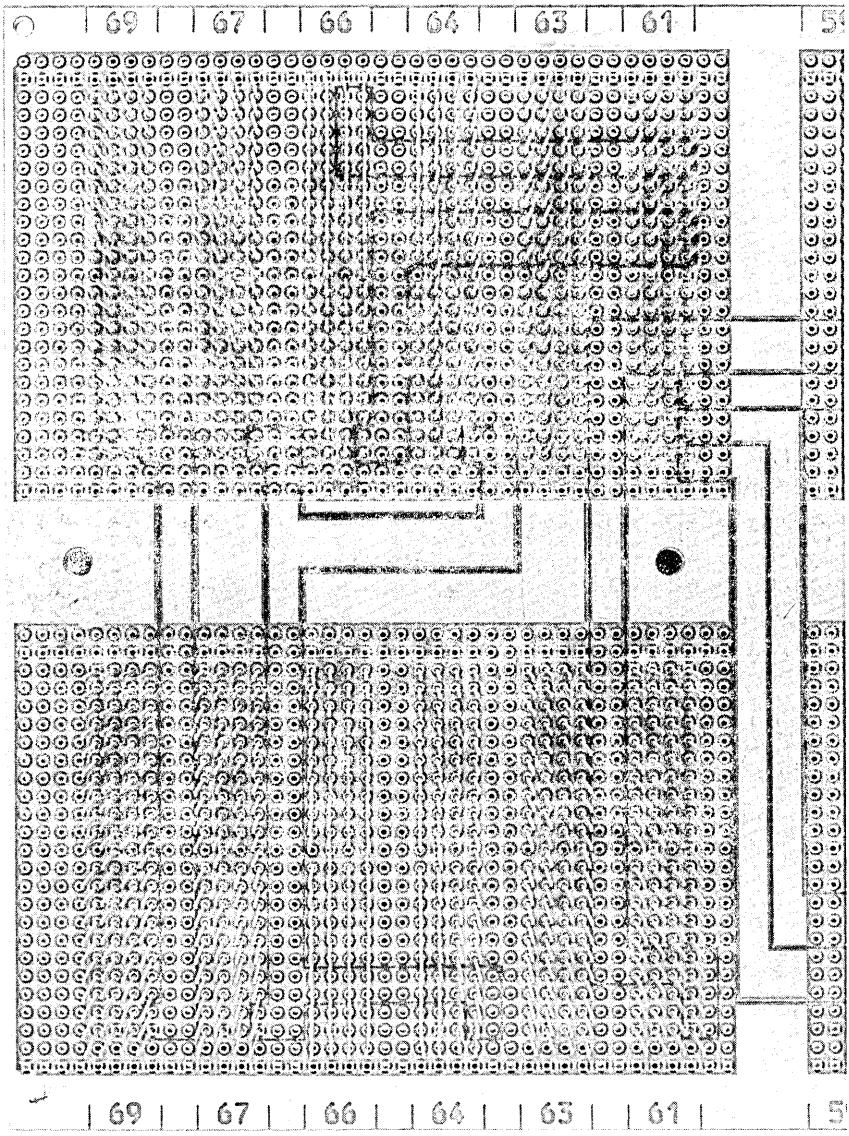


Fig. 7—Backplane printed wire power/ground segmentation.

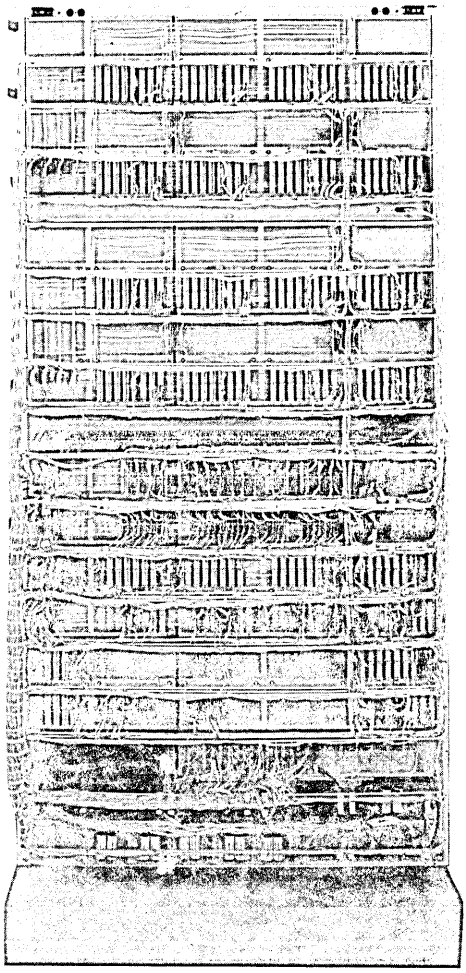


Fig. 8—Connectorized cabling.

of units in the field and a less-expensive alternative to manual termination which exhibits a resulting increase wire verification cost (see Fig. 8). All units were designed to be front removable to allow easy installation of growth units in the field and to allow easy replacement of units for maintenance reasons if the need arises.

In summary, the interconnection technology selected used high-density ICs, small-size discrete components, 8- by 13-in. PWB, the contact sequenced connectors, a ground first applique, PWB intraunit power distribution, connectorized intra- and interframe cabling, automatic wiring, and front removable units.

III. FRAME LAYOUT PARTITIONING AND GROWTH

3.1 Network topology versus frame layout

3.1.1 Introduction

The No. 10A RSS remote terminal frame (Fig. 9) utilizes a standard single-bay framework, 7 ft high by 3 ft 3 in. wide by 18 in. deep, to provide all the necessary hardware to serve up to 1024 lines. This

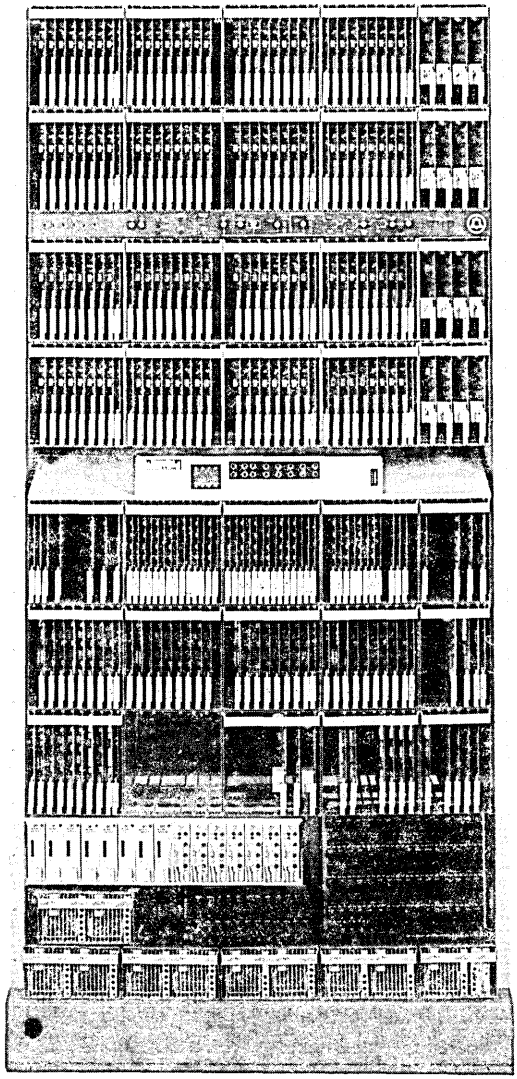


Fig. 9—No. 10A Remote Switching System (1024 lines/120 channels).

hardware includes the line interface, PNPN switching network, processor and memory, data links, transmission facility channels, and power supplies (Fig. 10). Each remote terminal can provide up to 120 channels of which two are used as dedicated channels for the data links (home frame only). For T carrier applications, these channels are provided by an integrated D bank within the RSS. When N carrier is used, N carrier channel banks and data link modems must be provided. A second RSS remote terminal frame (mate) can be added to the initial frame (home) to provide an additional 1024 lines and 120 channels. Except for certain processor, control, and test functions, the basic units are identical in the two frames.

The RSS frame hardware is physically partitioned into eight separate units (Fig. 11) based on functional grouping. The line interface unit (J4H001AA-1) provides the first-stage PNPN network, hardware interface between subscriber loop and PNPN network, fanout control, and service circuits for up to 512 lines. This unit measures 16 in. high by 36.25 in. wide and is used twice on a single frame.

The maintenance panel (J4H001AB-1) provides the craft person with several man/machine interface functions in a simple flowchart fashion. It allows the user to perform diagnostics, switch power, remove or restore service, and transfer control. It is 2 in. high by 36.25 in. wide and is only used in the home frame.

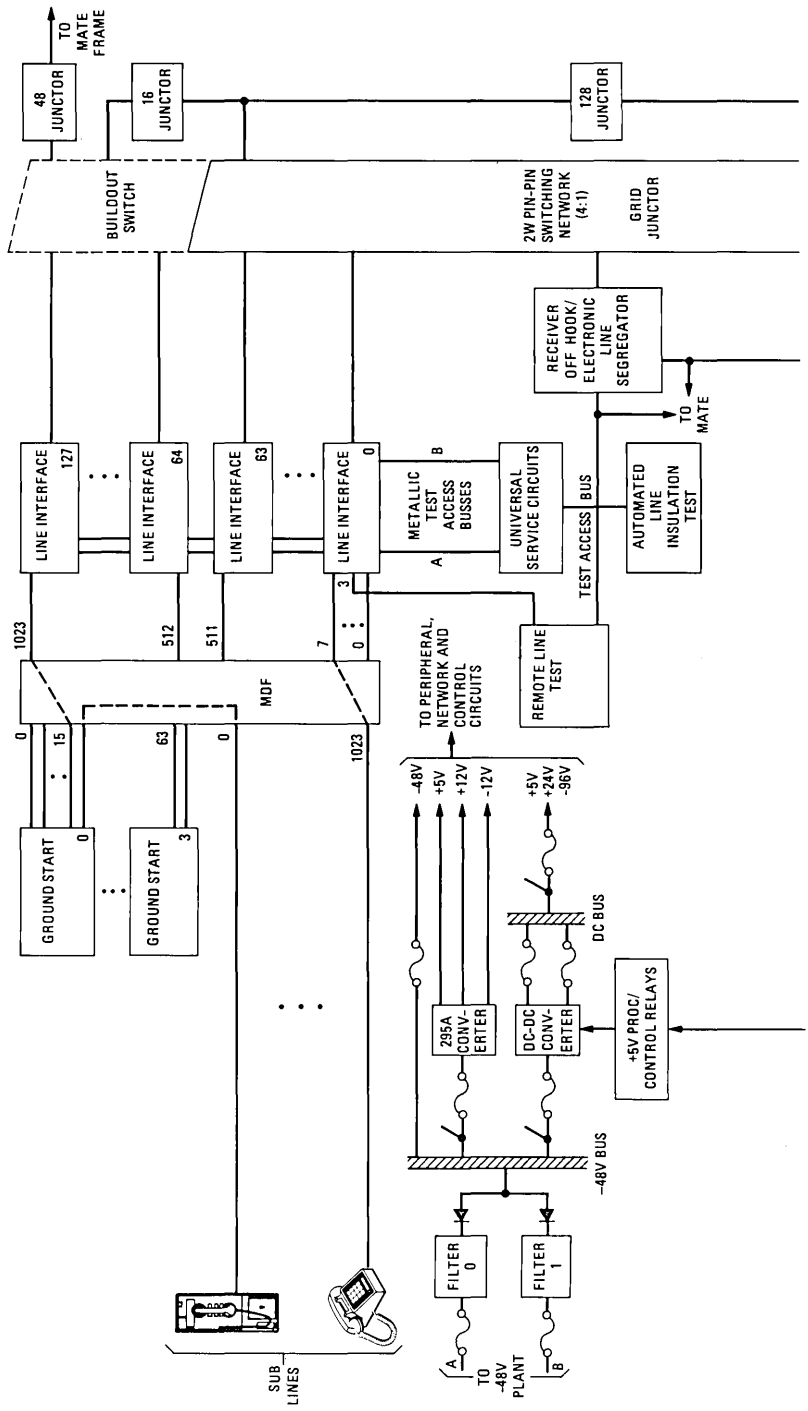
The switch and junctor, data link, and microprocessor unit (J4H001AC-1) provide the duplicated microprocessor controllers with associated memory, data link interfaces, and second-stage PNPN network. It is 8 in. high by 36.25 in. wide and provides the microprocessor and data link complex in the home frame only.

The channel interface and test unit (J4H001AD-1) provides 4 digroups with 24 channels, each for a total of 96 channels. For T carrier, each digroup includes most of the functions normally performed in the D banks to convert 24 channels to one T1 line. A power alarm monitor, receiver off-hook circuit, automatic line insulation tester, and minireponder for transmission testing are also provided in this 8-in.-high by 36.25-in.-wide unit.

The auxiliary channel interface and test unit with tone and customer digit reception backup (J4H001AE-1) provides an additional digroup with 24 channels, remote line testing functions, ground start appliques for signaling lines, such as coin and PBX trunks, *TOUCH-TONE** service receivers for stand-alone service, and scan and distribute points. This 8-in.-high by 36.25-in.-wide unit can be ordered with an· ›mbination of these functions.

The power and fuse unit with D4 special services (J4H0 AF-1)

* Registered service mark of AT&T.


TO MATE FRAME
48 JUNCTOR
16 JUNCTOR
128 JUNCTOR
BUILDOUT SWITCH
2W PIN-PIN SWITCHING NETWORK (4:1)
GRID JUNCTOR
RECEIVER OFF HOOK/ ELECTRONIC LINE SEGREGATOR
TO MATE
LINE INTERFACE 127
LINE INTERFACE 64
LINE INTERFACE 63
LINE INTERFACE 0
METALLIC TEST ACCESS BUSSES
UNIVERSAL SERVICE CIRCUITS
TEST ACCESS BUS
AUTOMATED LINE INSULATION TEST
1023
512
511
7
3
0
MDF
REMOTE LINE TEST
TO PERIPHERAL, NETWORK AND CONTROL CIRCUITS
GROUND START
-48V
+5V
+12V
-12V
+5V
+24V
-96V
DC BUS
295A CONV-ERTER
DC-DC CONV-ERTER
+5V PROC/ CONTROL RELAYS
-48V BUS
FILTER 0
FILTER 1
TO -48V PLANT
SUB LINES

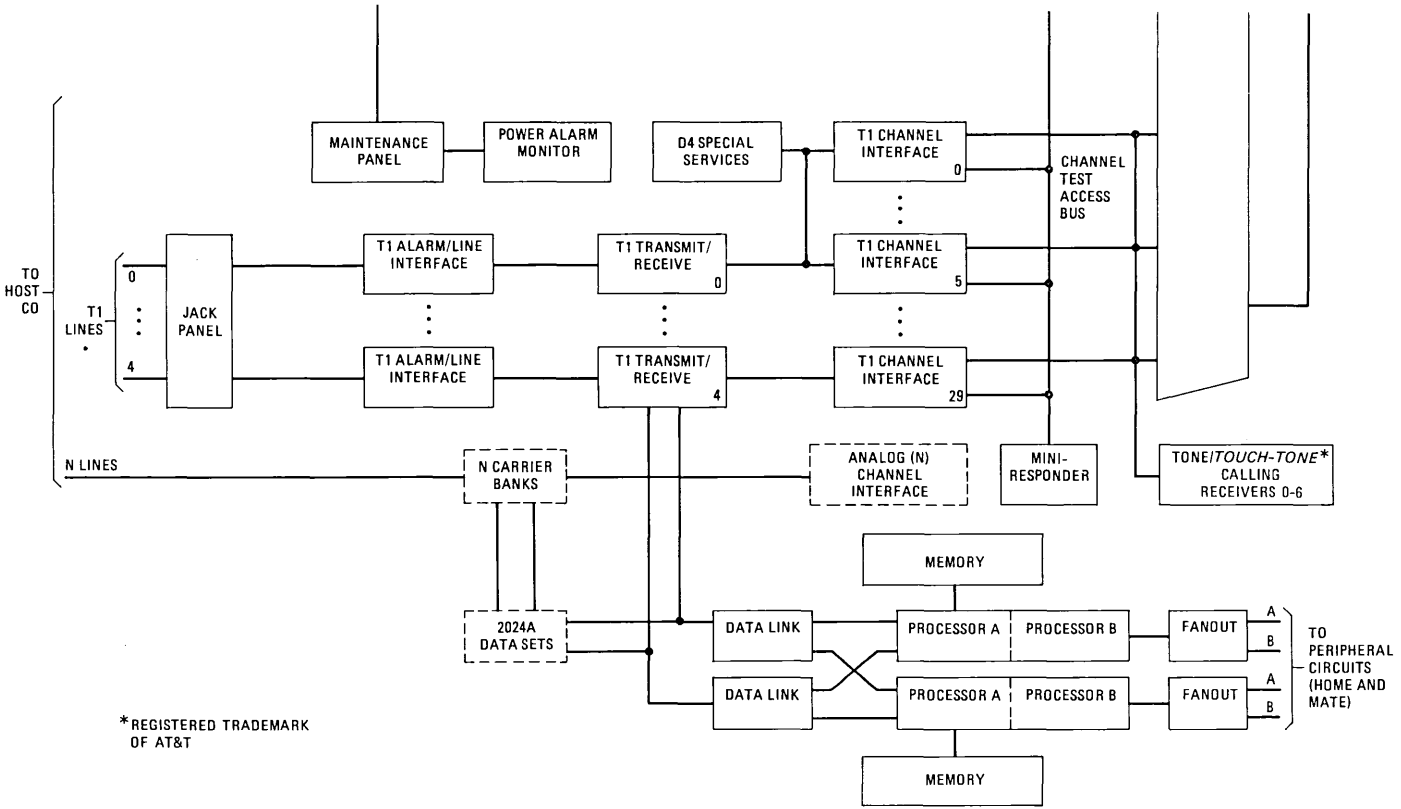
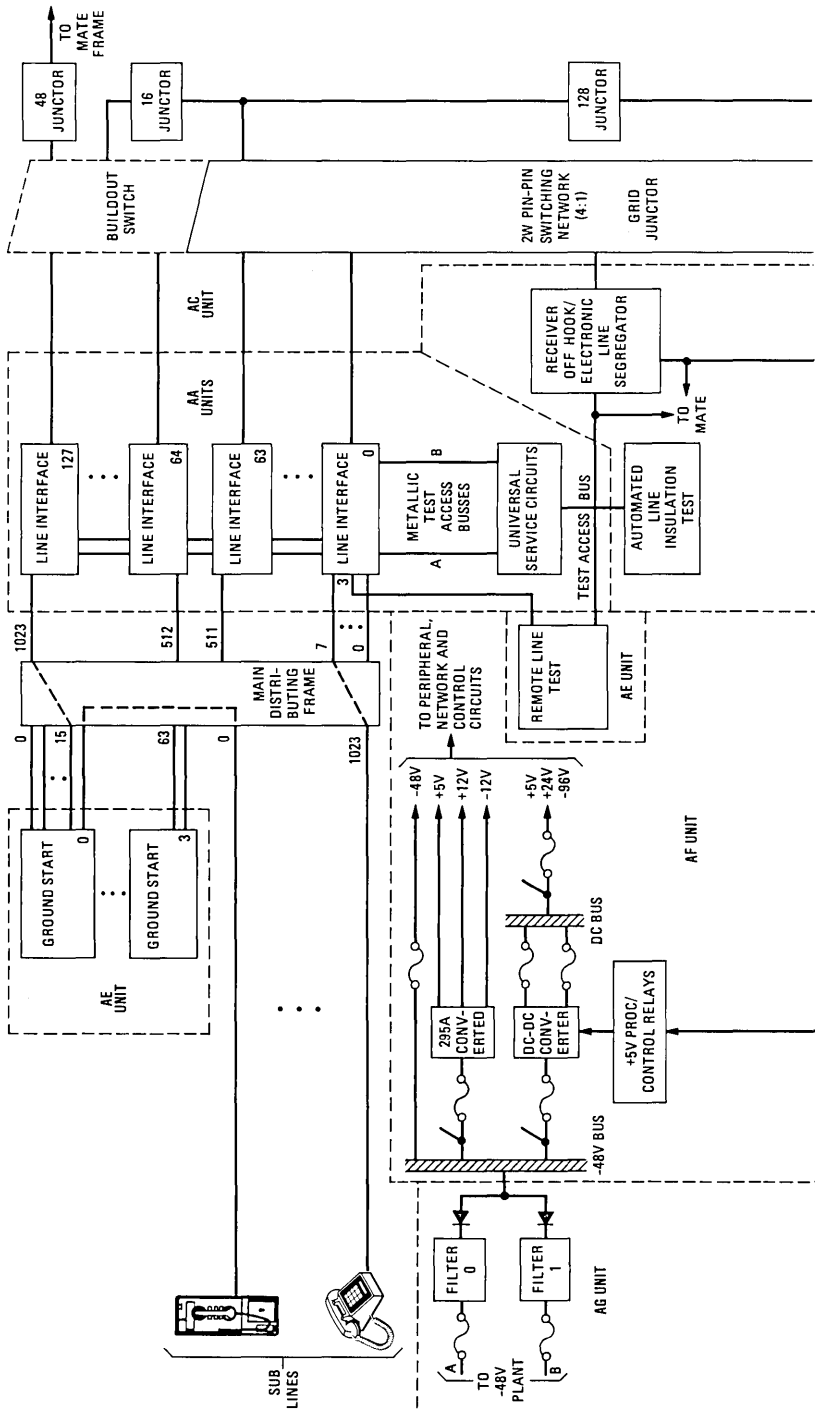


Fig. 10—No. 10A Remote Switching System block diagram.


TO MATE FRAME
48 JUNCTOR
16 JUNCTOR
128 JUNCTOR
BUILDOUT SWITCH
2W PIN-PIN SWITCHING NETWORK (4:1)
GRID JUNCTOR
AC UNIT
AA UNITS
RECEIVER OFF HOOK/ ELECTRONIC LINE SEGREGATOR
TO MATE
LINE INTERFACE 127
LINE INTERFACE 64
LINE INTERFACE 63
LINE INTERFACE 0
METALLIC TEST ACCESS BUSSES
UNIVERSAL SERVICE CIRCUITS
TEST ACCESS BUS
AUTOMATED LINE INSULATION TEST
1023
512
511
7
3
0
MAIN DISTRI-BUTING FRAME
TO PERIPHERAL, NETWORK AND CONTROL CIRCUITS
REMOTE LINE TEST
AE UNIT
0
15
63
0
1023
-48V
+5V
+12V
-12V
+5V
+24V
-96V
GROUND START 0
GROUND START 3
AE UNIT
AF UNIT
DC BUS
295A CONV-ERTED
DC-DC CONV-ERTER
+5V PROC/ CONTROL RELAYS
-48V BUS
FILTER 0
FILTER 1
AG UNIT
A
B
TO -48V PLANT
SUB LINES

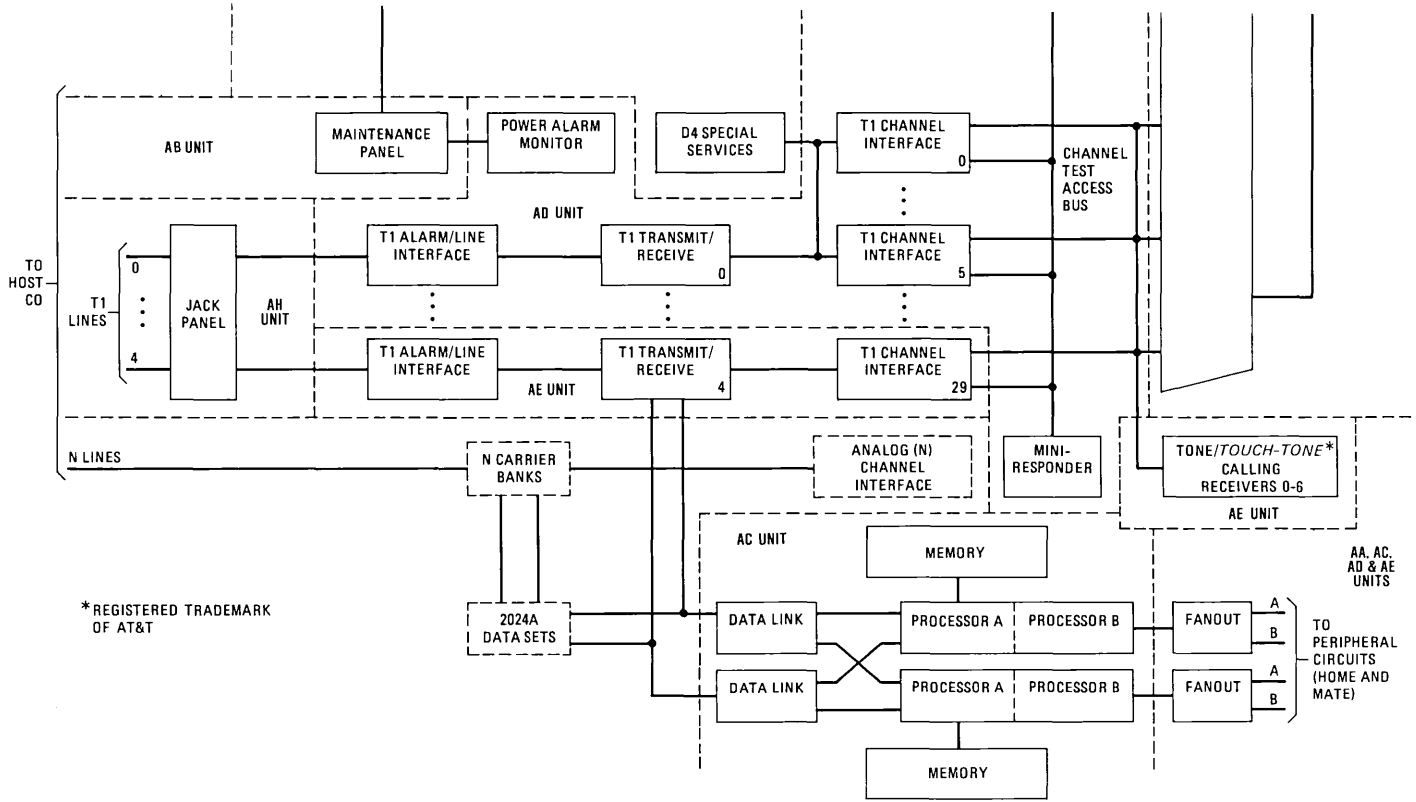


Fig. 11—No. 10A Remote Switching System block diagram (frame partitioning).

provides the power conversion and fuse indication for the entire frame. The unit is designed so that power conversion equipment can grow in relation to the number of required circuits. Provision for up to eight D4-type special services are also included in this 14-in.-high by 38.25-in.-wide unit. A 6-in.-high by 38.25-in.-wide filter unit (J4H001AG-1) is provided in the base of the frame.

The jack panel unit (J4H001AH-1) provides a means of access to the digital T1 lines for testing and monitoring purposes. This unit is 4 in. high by 36.25 in. wide and is mounted on the heat baffle in the center of the frame.

3.1.2 Line interface

The RSS line interface function is provided by the line interface circuit pack (Fig. 12) which acts as the interface between the first stage of the electronic switching network and eight customer lines. These circuit packs are located in the line interface units (J4H001AA-1) with up to 64 packs provided in each of the two units for a total of 1024 lines per frame. Each line interface pack contains eight-line circuits which provide network protection, line supervision, subscriber battery feed, and a cable anticorrosion feature.

3.1.3 The PNPN switching network

The RSS contains an analog, space division, two-wire, two-stage, folded network (Fig. 13). The network fabric is constructed using PNPN semiconductor devices. This miniaturized solid-state crosspoint re-

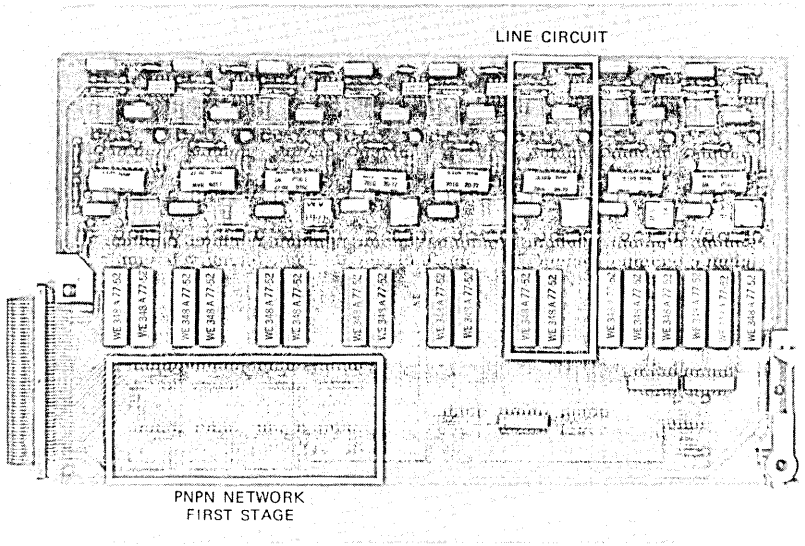


Fig. 12—Line interface circuit pack.

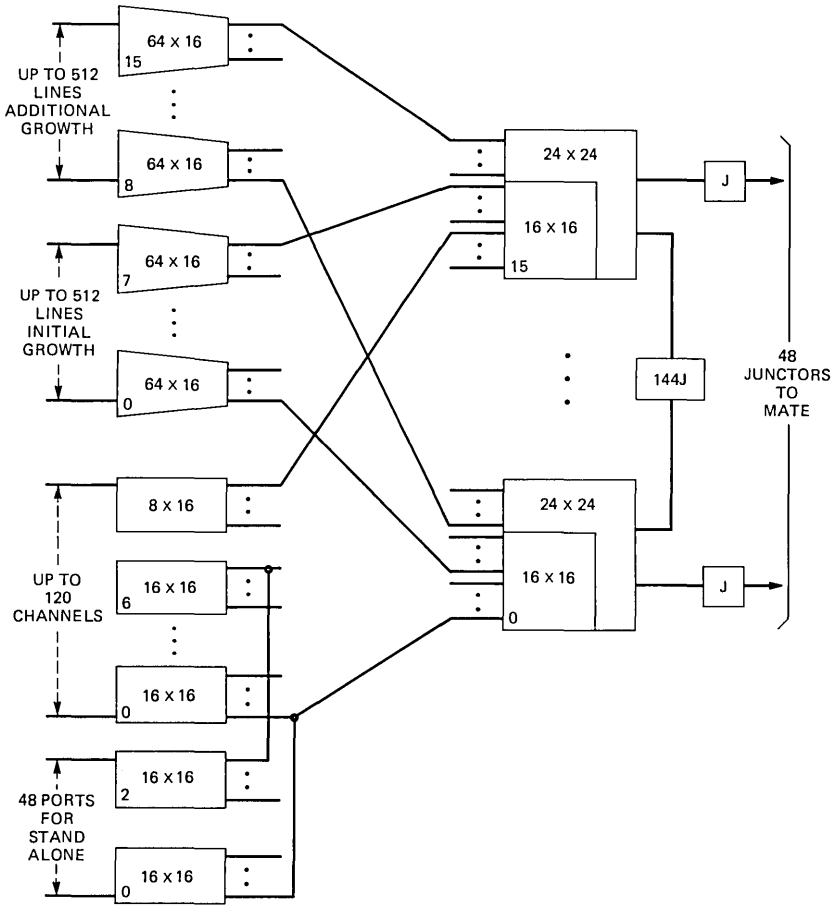


Fig. 13—Remote Switching System network.

quires very low-level signaling to activate a change in its open or closed state and results in a low-cost, compact design because of its small size.

The first stage of switching is contained on the line interface circuit pack (Fig. 12). Each pack contains an 8 by 16 matrix which allows expansion of the first-stage network as the number of lines grows, thereby reducing cost. Eight line interface packs are then combined in a single apparatus housing to form a 64- by 16-in. front-end concentrator. The line-interface pack also contains the access relays required to connect the subscriber tip and ring to the time-shared metallic network buses used for high-level signaling, such as ringing and coin control. The universal service circuits (USCs), also located in the line interface unit, provide the voltages required for this high-level signaling.

The second stage of switching is provided by the grid junctor and

build-out switch circuit packs (Fig. 14). Each grid junctor pack contains a 16 by 16 PNPN switching matrix and eight junctor circuits which provide the PNPN path-holding current sources, gain necessary to offset the PNPN device loss, and check circuitry. The build-out switch contains the 8 by 16 and 8 by 24 matrices that increase the size of the grid junctor to a 24 by 24 switch. This second-stage switch expansion occurs above a line size of 512, thereby reducing low line size network cost. Four additional junctor circuits are also added by the build-out switch providing a total of 12 junctors per second-stage switch. Of these four additional junctors, three are reserved for growth to the mate frame. The entire expanded second-stage switch, consisting of 16 grid junctor and 16 build-out switch circuit packs, is contained in less than two-thirds apparatus housings in the center of the switch and junctor, data link, and microprocessor unit (J4H001AC-1).

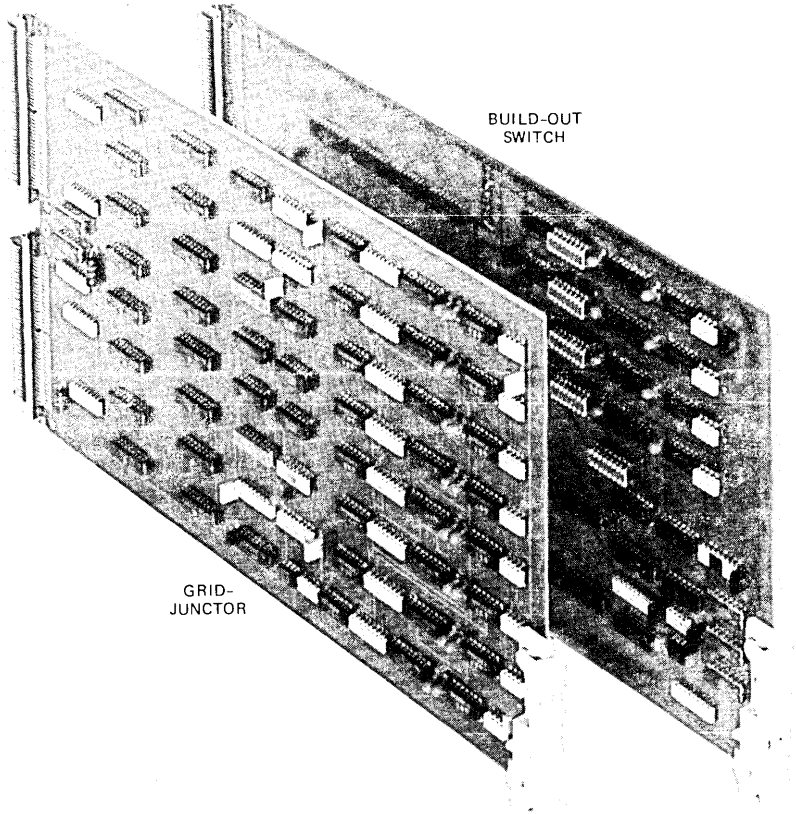


Fig. 14—PNPN network center-stage circuit packs.

The first stage of transmission switching is contained on the channel interface circuit packs (Fig. 15). Each pack provides the circuitry necessary to interface four audio channels between the remote terminal and its host ESS and provides a 4 by 16 matrix. This again minimizes cost by allowing the expansion of switching for transmission as the need for facility channels grows. A group of four-channel interface packs are combined to form a 16 by 16 switch. Each of the five-frame digroups contains one-and-a-half 16 by 16 switches on six channel interface packs for a total of 24 channels per digroup and 120 channels per frame. These channel interface packs are housed in the channel interface (J4H001AD-1) and auxiliary channel interface (J4H001AE-1) units.

3.1.4 Carrier/D4 Special Services

The RSS remote terminal provides the ability to interface with several types of facility groups. Transmission of voice circuits and data link messages to the host RSS can be routed over either T carrier or N (N2, N3, or N4) carrier at distances from 75 to 175 miles, depending on the type of carrier involved. Radio facilities are also technically feasible. These facilities may be mixed within a single RSS frame on a per-digroup basis.

Digital T carrier is intended as the primary mode of transmission for RSS, and an integrated D bank will be provided within the RSS for T carrier applications. This T carrier hardware is provided by the alarm interface, transmit/receive, and T1 channel interface circuit

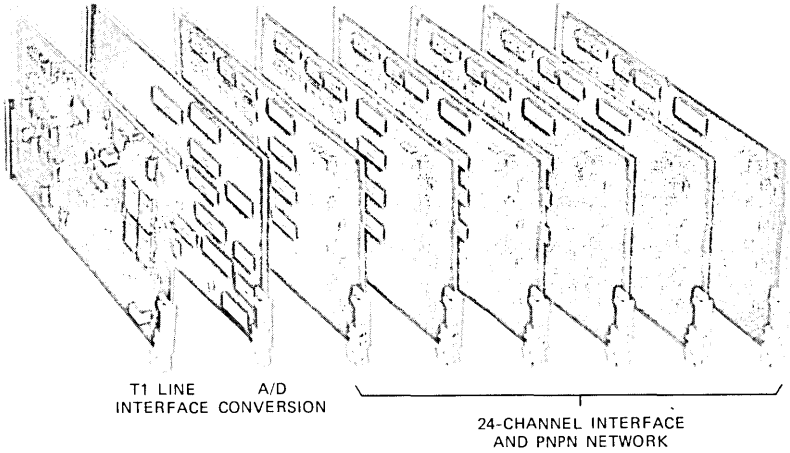


Fig. 15—Transmission and switching interface circuit packs.

packs (Fig. 15). The channel interface pack, in addition to providing the previously described first-stage network switch, acts as the interface between the electronic network and the T1 digital carrier. It provides the transmission path conditioning and the conversion from voice frequency to multiplexed pulse amplitude modulated transmission for four audio channels. When six of these packs are combined with the transmit/receive and alarm interface packs, a full T1 group of 24 channels is formed. The transmit/receive pack performs the analog-to-digital and digital-to-analog conversion functions, while the alarm interface pack acts as the direct interface between the RSS frame and the 1.544-MHz T1 line. It incorporates the required bipolar receiver, transmitter, alarm circuitry, and maintenance features to facilitate fault location.

The N carrier option is indicated by the dashed boxes in the RSS block diagram (Fig. 10). An analog channel interface circuit pack is used in place of its digital counterpart and plugs into the same frame positions. It also provides four channels per pack and performs many of the same functions as its digital equivalent. However, alarm interface and transmit/receive packs are not used. Instead, the output of the channels is cabled directly off the back of the RSS frame to the N-carrier banks. For each data link on N carrier, an external data set is required at each end of the facility link. This data set is cabled directly between the RSS frame and the N-carrier banks. The appropriate RSS frame local cable is then unplugged to remove the data link from interfacing with the T1 facility.

Provision is also made within the RSS frame in the power and fuse unit (J4H001AF-1) for up to eight built-in standard D4 special-service channel bank plug-ins for such applications as off-premise extensions, foreign-exchange lines, and private lines. Each special-service line requires the use of a channel on the carrier system. However, if the D4 special-service option is used, the last four channels of the first two digroups are reserved solely for D4 special-service use by the installation of two frame cables that tie it into the carrier system.

3.1.5 Processor/memory

The RSS frame contains duplicated microprocessor complexes which act as the controlling entity for the entire remote terminal. These processor complexes are located on each end of the switch and junctor, data link, and microprocessor unit (J4H001AC-1). Each controller consists of a *BELLMAC**-8 microprocessor with associated circuitry, memory, data link interface, and fanout interfaces located throughout the frame to communicate with peripheral systems.

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* Trademark of Western Electric.

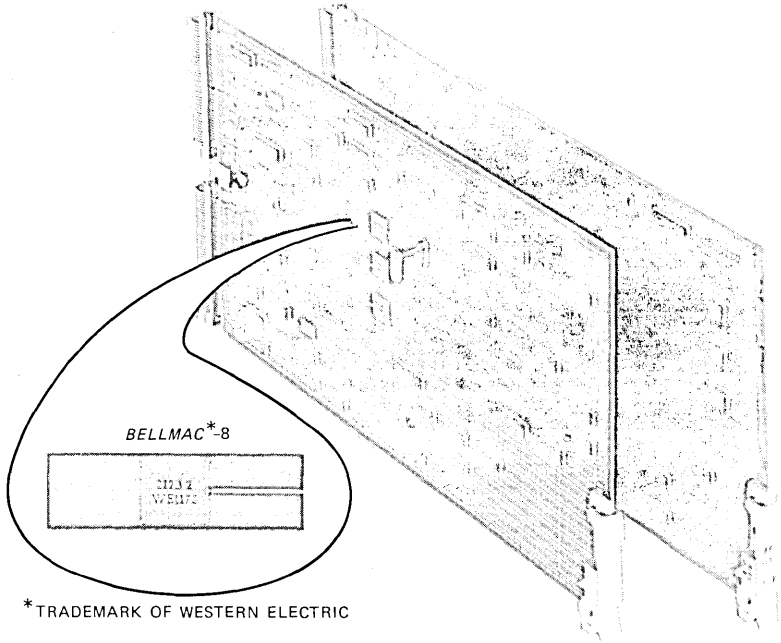


Fig. 16—Microprocessor circuit packs.

The No. 10A RSS *BELLMAC*-8 based microprocessor and associated circuitry is contained on two circuit packs (Fig. 16). This controller provides features such as extended addressing range, multiple vector interrupts, error checks, access to external circuitry, and communication with its duplicated mate. The processors are physically interconnected using tape cabling to reduce noise and communicate both through I/O ports and by a bus coupling arrangement.

The RSS memory complex contains both Random Access Memory (RAM) and Erasable Programmed Read Only Memory (EPROM) (Fig. 17). The RAM board contains 24,576 bytes of data with parity (24K by 9-bit) and is used twice in each processor complex for a total of 48K of RAM. The RAM memory utilizes a 4K by 1-bit static memory device. The EPROM board contains 63,488 bytes of data with parity (62K by 9) and is used three times in each processor complex for a total of 192K of EPROM. The EPROM board utilizes a 2K by 8-bit memory device which may be erased by exposing the board to ultraviolet (UV) light, and then programmed by applying signals to the board's edge connector. A portable apparatus called *PROMUS** reprogrammer (Fig. 18)

* Trademark of Western Electric.

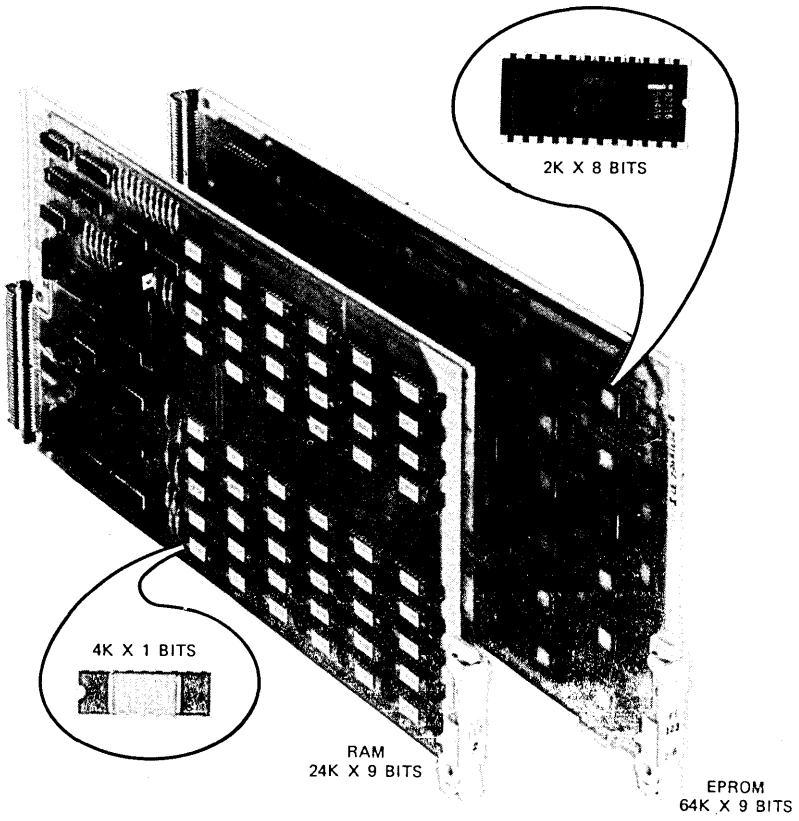


Fig. 17—Memory circuit packs.

is used to erase old data by UV light (approximately 30 minutes) and to both program and verify the new data (approximately 70 minutes), which are obtained via a dial-up link to the host computer.

The data link interface circuit pack provides the interface between the microprocessor controllers and the two voice channels assigned to perform the data link operation. The data link interface performs the implementation of signal protocol, transmission error detection, appropriate message formatting, and also allows either processor to access either data link.

The fanout circuit pack provides the interface between the duplicated processor complexes and the peripheral systems. These packs are distributed throughout the frame in close proximity to the peripheral circuits to which they interface. While a fanout pack has access to only a single processor, any peripheral circuit pack may be accessed by two fanout boards—one from each processor. This minimizes the

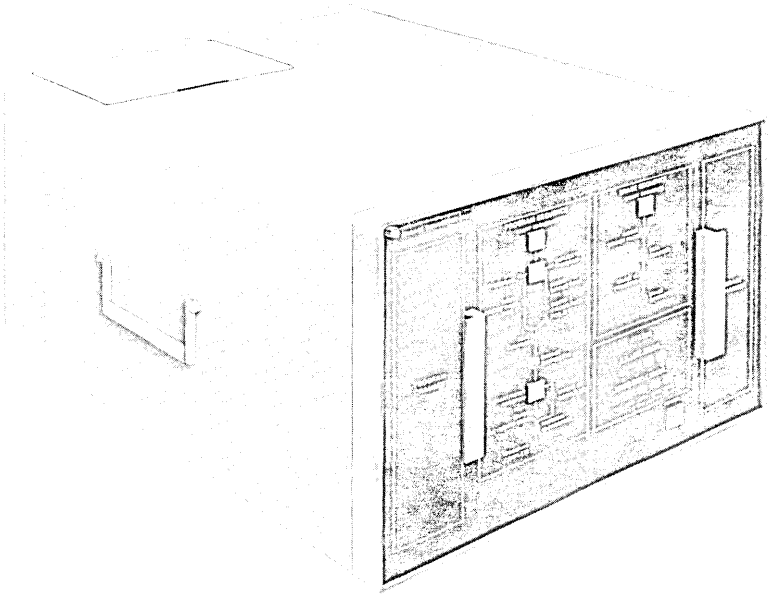


Fig. 18—*PROMUS* reprogrammer.

impact of the removal or the failure of a fanout pack. Fanout circuit packs are added as required and as the number of peripheral circuit packs increases. This reduces the cost of control for small-sized systems.

3.1.6 Power

The RSS frame provides all the power conversion and fusing for the entire system. The power complex (J4H001AF-1 and J4H001AG-1 units) is a multivoltage, multiconverter, multifuse system. It consists of 19 converters supplying 6 voltages and 180 fuses when fully equipped. It receives its input from the −48 volt office plant. Current drain for a fully equipped single frame during busy hour traffic is approximately 15 amperes.

The RSS power complex uses various types of power converters (Figs. 10 and 19). Some of these converter codes have a single output voltage (+5V:131L1A, +24V:131N1A, or −96:130L), while others are of the multivoltage type (+5V, +12V, and −12V:295A). Also, some of the converters are dedicated to certain circuit packs, while others power a common bus which is used throughout the frame. In either case, the number of converters can grow as the number of circuit packs increases, thereby reducing power equipment costs for small systems.

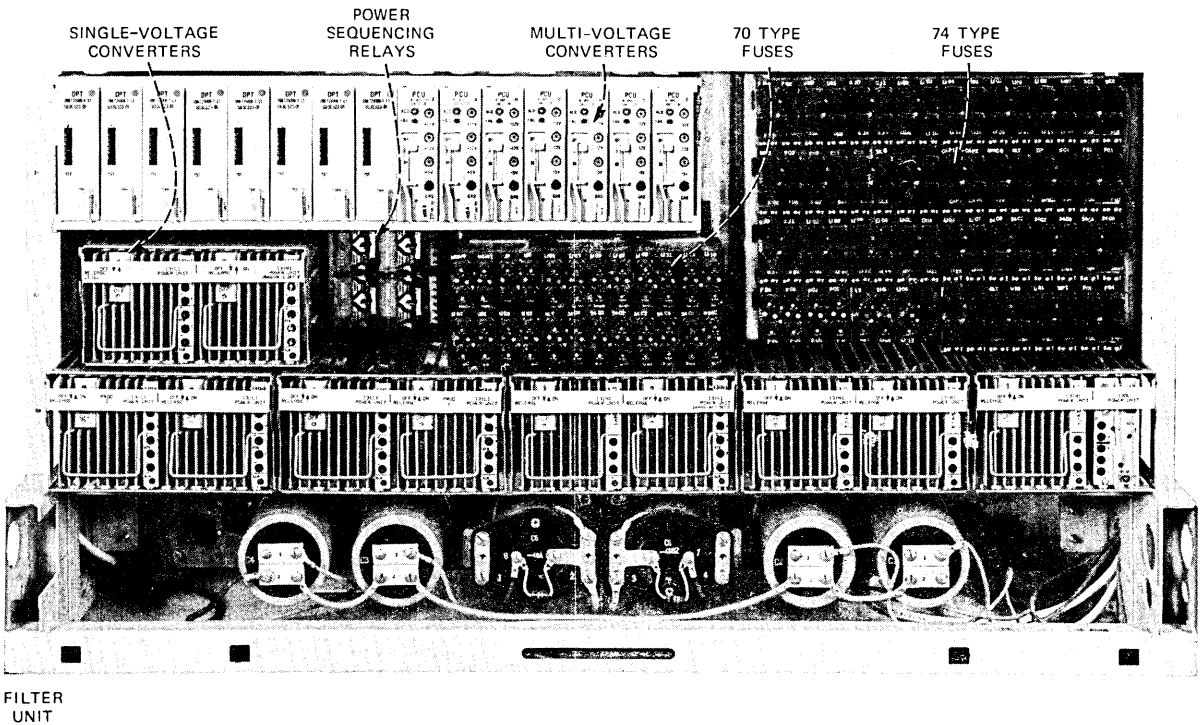


Fig. 19—Remote Switching System power complex.

Power distribution is accomplished from the converters using frame local cabling and backplane printed wiring to the required circuit packs. Circuit-pack removal from the frame is done under power with the exception of the processor complexes and their associated fanouts. These packs cannot be removed or inserted without first removing power by means of the maintenance panel. Correct power sequencing to the processor complexes is accomplished via the control relays in the power unit.

The power complex utilizes two different families of fuses. Of the 180 fuses in the frame, 64 are the 70 type, with pop-out alarm indicator, and 116 are of the 74 type, featuring fast blow time and low voltage drop to maximize protection of electronic circuitry and components. When a 70-type fuse blows, the fuse body expands lengthwise by spring action to provide visual indication and makes an electrical contact to provide an electrical indication of the alarm. The 74-type fuse does not contain an integral fuse alarm assembly, but instead uses an external Light Emitting Diode LED mounted beneath each fuse block. An alarm condition exists when a fuse's corresponding LED is illuminated.

The power alarm monitor circuit pack is the interface between the RSS processor and the frame power complex. It serves as the monitoring and controlling vehicle (via 55 scan points and 15 distribute points) by monitoring all fuses and converter output voltages, enabling the maintenance panel so that power can be removed from the processor complexes, testing fuse alarm scan points, and performing converter performance tests.

3.1.7 Miscellaneous

The RSS frame provides various specialized features which are located in the auxiliary channel interface unit (J4H001AE-1). The remote line testing feature is contained on three circuit packs and provides a modified end arrangement of the existing Western Electric remote testing system. These packs contain a *BELLMAC*-8 microprocessor to control the test circuits which provide a telemetry interface to receive host instructions, dc line test voltages, tip and ring access via the metallic access bus to the line under test, line measurements, and return of the detected results to the host.

The ground start applique circuit provides an interface between the line interface circuit packs and those loops requiring ground start supervision such as coin first, coin telephone, and PBX trunks. Each ground start circuit pack contains 16 identical circuits which can interface a like number of line interface circuits. Each frame contains provision for up to four ground start circuit packs for a maximum of 64 ground start lines per 1024-line frame.

The *TOUCH-TONE* service receiver circuit pack contains the receivers, tone circuits, and network ports via an 8- by 16-bit first-stage switch (Fig. 13) necessary for stand-alone operation. Provision for up to six receiver circuit packs exists in each frame with equipage based on the number of equipped lines.

The miscellaneous scan and distribute circuit pack provides 24 scan points and 32 distribute points required by the system for scanning and distributing capability, such as testing functions and office alarms. With provision for up to four scan and distribute boards per frame, a single frame can be equipped with 128 distribute points and 96 scan points.

3.2 Frame growth/options

The RSS frame contains 19 separate lists required for system growth and optional features. These lists are designed to provide an easy means to engineer the RSS frame equipage and can be divided into three basic categories: basic frame equipment and optional units (lists 1 to 4), apparatus required for system growth (lists 5 to 10, 13 to 16), and apparatus required for optional features (lists 17 to 21).

IV. BUILDINGS AND ENCLOSURES

4.1 Floor plans

A fully equipped RSS frame (1024 lines) weighs approximately 1100 lb, which includes 100 lb for interframe cabling and overhead cable racks. The resulting floor loading is 90.25 lb/ft^2, figured using a 2-ft operating aisle space and a 2-foot 6-inch maintenance aisle space. A second frame can be added to provide growth to 2048 subscriber lines and 240 channels. When two frames are used, the two frames must be adjacent because of lead length restrictions on common circuitry.

The compact size of the 10A RSS remote terminal frame permits a number of different enclosure options, such as the reuse of an existing building, construction of a new modular building, or an electronic hut for pair-gain applications. In many CDO applications, it will be possible to reuse the existing building, power plant, and main distributing frame, in which case floor space need only be provided for the RSS frames and a bay or two of miscellaneous equipment. Figure 20 shows a typical CDO replacement floor plan after the SXS equipment is removed.

The RSS frame has been designed to meet all central office environmental operating requirements as outlined in the New Equipment Building Systems (NEBS) building specifications. The RSS equipment design objectives require a normal operating ambient temperature of 40 to 100°F with short-term limits of 35 to 120°F for up to 72 hours.

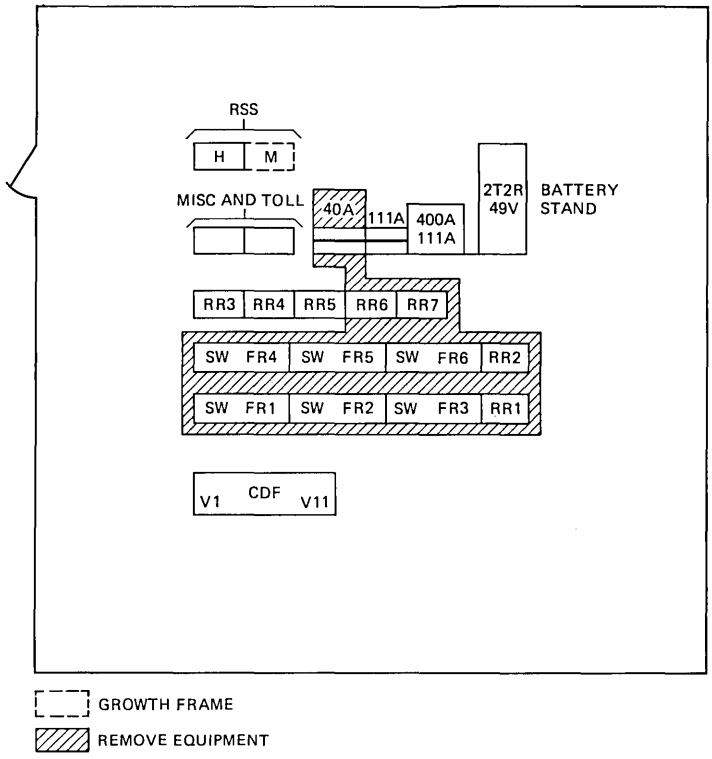


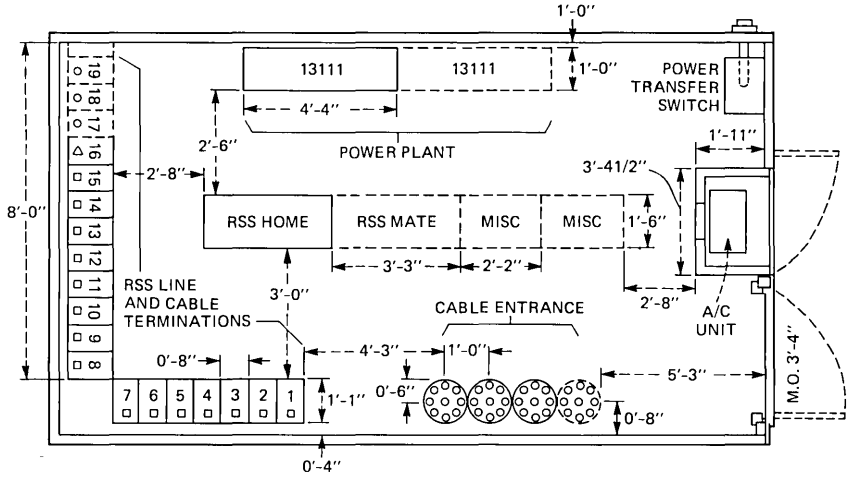
Fig. 20—Typical RSS floor plan as a CDO replacement (800 lines step-by-step office).

Relative humidity can vary from 20 percent to 55 percent, with short-term limits of 20 percent to 80 percent.

For pair-gain applications, a new enclosure called an electronic equipment enclosure will be available. This enclosure contains sufficient space for two RSS frames, two miscellaneous equipment bays, a −48 volt power plant, a main distributing frame, and a cable entrance facility. Preinstallation of equipment at a service center prior to shipment may be provided which should offer a shorter, more uniform installation with reduced shipping costs. Fig. 21 shows the floor plan for the electronic enclosure.

4.2 Electronic equipment enclosure

The electronic equipment enclosure is a building-like enclosure which can be used for both large pair-gain applications and new wire centers where no existing structure will generally be available. This shelter has floor dimensions of approximately 10 by 20 ft and can be erected with various optional architectural facade treatments, which



NOTE: 8'-3" CLEAR CEILING HEIGHT
△ T1 CARRIER PROTECTOR
□ SUBSRIBER LINE PROTECTOR
○ MISC LINE PROTECTOR

Fig. 21—Remote Switching System floor plan (electronic equipment enclosure).

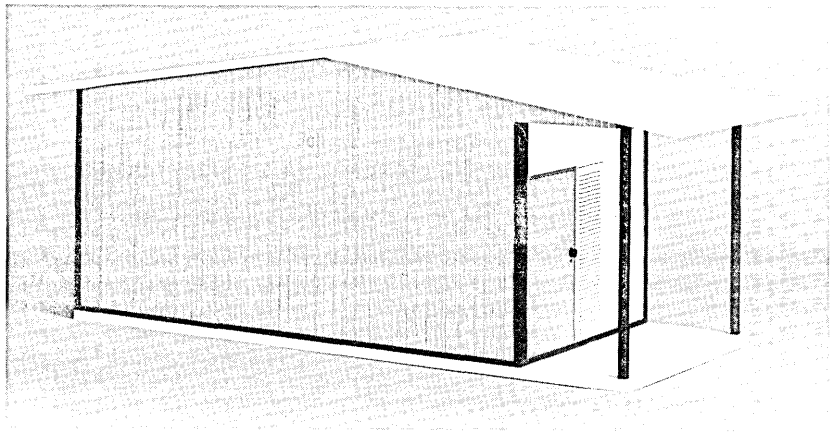


Fig. 22—Typical electronic equipment enclosure.

are expected to satisfy the aesthetic needs of most applications (Figs. 22 and 23).

The electronic equipment enclosure is capable of accommodating two RSS frames providing 1536 lines (2048 maximum). To avoid the need for traffic balancing, pair-gain applications are limited to 1536 lines. Standard central office environment (temperature between +40 and 100°F, maximum long-term relative humidity of 55 percent) is

maintained over an external ambient of −40 to 120°F by the heating and air conditioning equipment. A modular 131B power plant consisting of three 35A rectifiers, a control unit, and two high-gravity lead-calcium battery strings will provide approximately 14 hours of reserve at 32°F and 8 hours of reserve at −10°F for 2 fully loaded RSS frames.

4.3 External interfaces

Because of the compact nature of the RSS frame, a large number of external interfaces must be made via interframe cabling. All cabling is connectorized at the No. 10A RSS end to simplify field installation, testing, and unit repair by allowing front removable units to be easily replaced. External interfaces to a single RSS frame consist of:

Type	Number of Pairs
Subscriber tip and ring	1024
T carrier (in)	5
T carrier (out)	5
N carrier (in)	240
N carrier (out)	240
Scan points	96
Distribute points	128
Ground start appliques	128
D4 special services	16
Miscellaneous	13

V. RELIABILITY ASPECTS OF NO. 10A RSS

5.1 The RSS outline block diagram

In the RSS outline shown in Fig. 24, the following items are worth noting:

- The RSS is equipped with a duplicated controller group. The

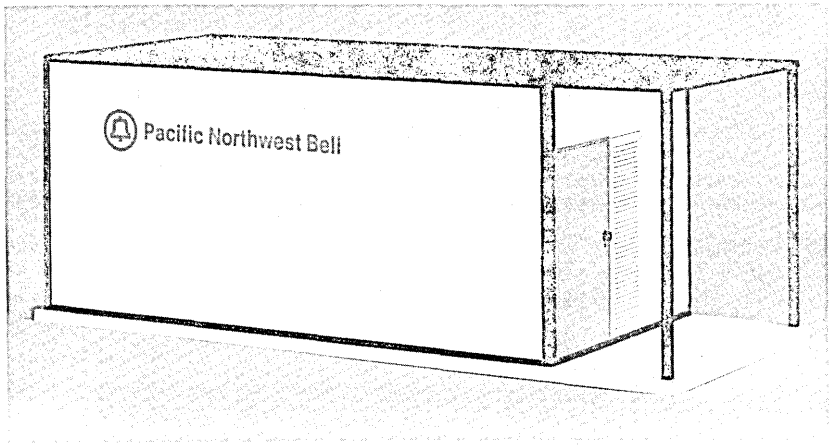


Fig. 23—Typical electronic equipment enclosure.

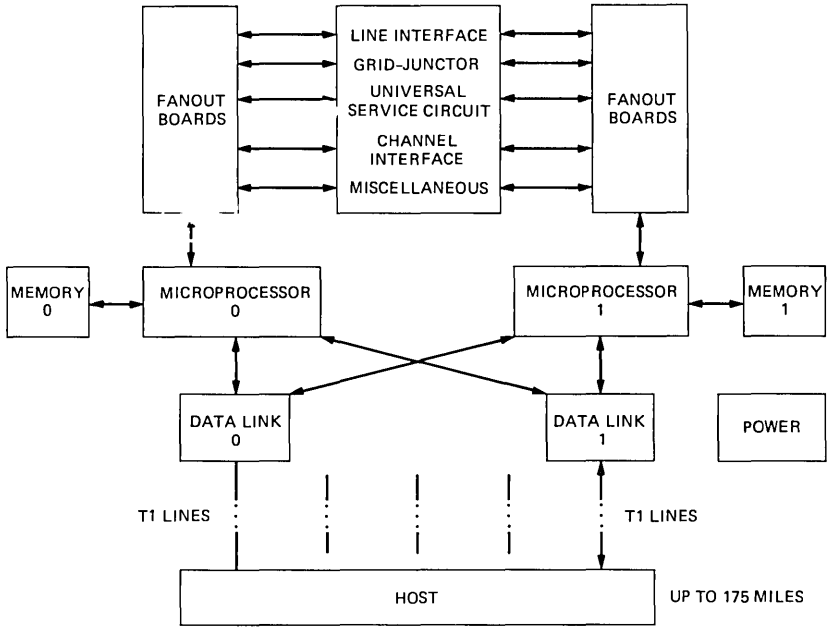


Fig. 24—Remote Switching System block diagram.

controller group consists of memory, microprocessor, and data link circuit packs. Failure of a duplicated group will affect the entire office and total service outage will occur.

- Replicated junctors, universal service circuits, fan-out circuit packs, and voice channels are provided. The failure of some of the replicated units will cause traffic problems, but customer outage will not take place. Should all replicated units fail, an entire office outage will occur, although this has a low probability of occurrence.
- Line interface circuit packs are dedicated to customers. Each circuit pack has eight circuits, each of which is dedicated to one customer. Failure of a circuit deprives one customer of service. In the event of a common circuit failure, all eight customers are affected.
- Automatic fault detection, periodic diagnostics, per-call test, and internal analysis are also provided for diagnostic purposes.

5.2 Failure modes in No. 10A RSS

Any of the following will cause total service outage:

(*i*) Simultaneous failures of both controllers and data links (DLIS).

(*ii*) Failure of all of the following circuit packs:

(a) Grid-Junctors (G-JS)

(b) Fan-Outs (FOS)

(c) Universal Service Circuits (USCs)
(d) Line Interfaces (LIs)
(e) Channel Interfaces (CIs).

(*iii*) Failure of the following items related to power:
(a) Both −48 volt office buses
(b) All +24 volt converters
(c) Both of the +5 volt converters dedicated to the microprocessors
(d) Both multivoltage converters dedicated to the DLI, FO, and CI
(e) Both +5 volt peripheral converters.

Partial service outage will occur under the following conditions:

(*i*) Greater than 10 percent service degradation

(a) Failure of two mating fan-out boards will affect 128 lines (eight LIs from each side will be affected).
(b) Failure of two mating fan-out boards will affect 512 lines (four USCs from each side will be affected).
(c) Failure of any two fan-out boards, one from each side (will bring 128 lines down if LI is affected and 512 lines down if USC is affected).

(*ii*) Greater than 1 percent service degradation

A blown fuse will affect 64 lines.

(*iii*) Greater than 0 percent service degradation

A component failure on the LI board may affect service of as many as eight customers.

5.3 Mean repair time

It is difficult to determine the repair time for various types of troubles for an unstaffed office, but, a general formulation can be made based on No. 1 ESS experience. The formulation includes the travel time required to dispatch a craft person and the degree of difficulty encountered in the repair of the trouble. From ESS experience thus far, the average repair time for staffed offices is two hours. For unstaffed offices, the calculations must include a 2-hour travel time for the craft person. Therefore, the mean repair time for No. 10A RSS was assumed to be four hours.

5.4 Failure rates for No. 10A RSS circuit packs

In evaluating the reliability of RSS, it was necessary to obtain failure rates on all components under typical office conditions. These rates were obtained from the Bell Laboratories Reliability Information Note Book, KS specifications for commercial devices, advice from various Bell Laboratories device engineers, and some field data. They did not

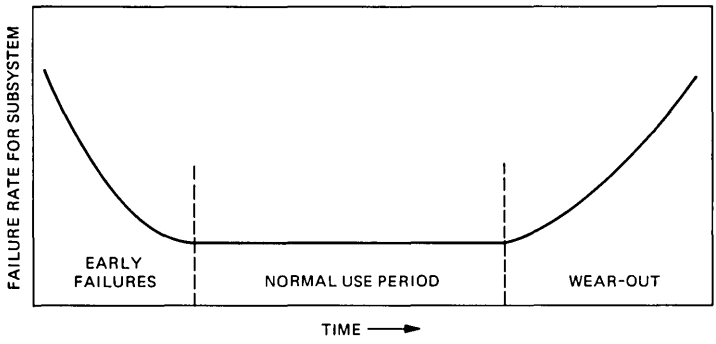


Fig. 25—Bathtub curve.

include software induced outages, errors on the part of craft persons, or unusual environmental conditions such as lightning, earthquake, fire, etc. The study concerned itself only with the electronic functioning of system components.

Mean failure rates are assumed to be constant, although they tend to decrease with an increase in time. For a long-term reliability study, the steady state portion of the bathtub curve is assumed (see Fig. 25). In this case, the components on all of the circuit packs were studied to determine the failure rate for each. The results are shown in Table I. For a 1024-line, fully equipped RSS frame, the data show that

(*i*) approximately half of the total FITS* are attributed to LI packs (FE101), which is directly related to customer line performance (every ten weeks one LI will fail),

(*ii*) about seven percent of the total system FITS come from controller groups, which are duplicated and do not seem to have serious consequences in terms of service loss to customers (they may have an impact on maintenance schedule for Bell Operating Companies),

(*iii*) fan-outs, USCs, and G-J circuit packs constitute one-third of the total system FITS (here again, the consequences are not serious), and that

(*iv*) FITS associated with automatic diagnostic features, fault detection, and internal analysis constitute about 10 percent of the total FITS.

Analyzing FITS from various components on RSS circuit packs (see Table II) shows that

(*i*) most of the failures come from integrated circuits. The controller group (FE107, FE109, FE113, FE123) shows a high usage of ICs,

* FITS = Failures in one billion hours.

Table I—Plug-in failure rates (1,024 lines, 120 channels fully equipped office)

Circuit No.	Circuit Name	No. of Circuits	Percent of System FITS	MTBF* (yrs)
FE101	LI	128	44.6	0.21
FE102	G-J	16	8.5	1.08
FE103	CI	30	5.3	1.73
FE104	FO	32	12.4	0.75
FE105	USC	16	8.7	1.06
FE106	BOS	16	3.7	2.50
FE107	DLI	2	0.4	23.30
FE108	GS	4	2.9	3.20
FE109	PROC I	2	1.6	5.65
FE110	MEM I	4	2.4	3.82
FE111	TR	5	1.0	8.93
FE112	T1-ALI	5	1.0	9.19
FE113	PROC II	2	0.8	11.57
FE114	*TOUCH-TONE* service receiver	6	1.1	8.38
FE115	ROH	1	0.2	42.18
FE116	PAB	1	0.3	34.08
FE118	RLT I	1	0.2	37.55
FE119	RLT II	1	0.2	45.53
FE120	MSD	4	2.4	3.90
FE123	MEM II	4	2.3	4.35
Steady state total FITS = 1,234,563 (MTBF* = 28 days)				

* Mean time between failures.

In terms of customer service effect, the LI boards are of most concern, since they account for about 50 percent of the total system FITS.

Table II—Percent FITS in RSS components

Components	Percent FITS
ICs	43
Capacitors	29
Relays	7
Others*	21

* Transistors, transformers, resistors, diodes, etc.

which account for approximately 90 percent of the total controller FITS,

(*ii*) the second highest number of failures comes from capacitors and in LI boards, tantalum capacitors contribute about 42 percent of total LI FITS, and that

(*iii*) the contribution of all other components, including power converters, to failures (FITS) is small.

5.5 Downtime predictions for No. 10A RSS

To determine downtime for any system, the following parameters must be studied:

Table III—Remote Switching System performance in relation to downtime

Service Outage (Percent)	Objective for Downtime (min/yr)	Expected RSS Downtime (min/yr)
100	3	0.025
$100 > x \geq 10$	10	0.107
$10 > x \geq 1$	21	1.32
$1 > x \geq 0$	53	134*

* (8 customers affected)

Table IV—Line circuit downtime

Line Circuit Spare Description	Downtime* (min/yr)	
	With Spare	Without Spare
One spare for 31 circuits	0.03	1076
One spare for 255 circuits	0.27	1076

* Note: Average repair time = 4 h.

- Failure rates of components
- Repair time for various troubles
- Status of subsystem, i.e., Simplex or Duplex, etc.

These parameters determine the availability or unavailability of the subsystem or system. The method of determining downtime is shown in the Appendix. The results of downtime calculations are shown in Table III. From the results, the following comments are pertinent:

- For the entire system, the standard of no more than three minutes per year downtime is adequately realized. The downtime, because of hardware troubles, is 0.025 minutes per year.
- Partial system downtime can be caused by simultaneous outages of fan-out boards, which is a remote possibility. However, the objectives are met for customer groups greater than ten percent.
- For less than 1 percent of the total customers, the downtime objective is met by having a switchable circuit for every 31 circuits, or 255 circuits. Downtime calculations made suggest that sparing makes downtime almost negligible. (See Table IV.)

5.6 No. 10A RSS burn-in considerations

The interval between RSS ship-date and service is much shorter (four weeks) than that for most electronic switching systems. Also, the No. 10A RSS is unstaffed and may be situated in a hut that, instead of air conditioning, merely has an exhaust fan to circulate the air and bring the ambient temperature close to the outside temperature. Therefore, it is imperative that No. 10A RSS perform near its steady state reliability objective prior to service. This can be accomplished by various burn-in procedures.

To eliminate early failures, burn-in in the factory at the circuit pack level, as well as at the frame level, appears to be the most economical approach, in which case marginal and weak components are weeded out. The following assumptions are made in order to arrive at burn-in procedures:

(*i*) The majority of circuit pack components obey the following relationship:

$$\left|\frac{\lambda}{\lambda_1}\right| = \left|\frac{t}{t_1}\right|^{-m},$$

where

λ = FITS corresponding to time t,

λ_1 = FITS corresponding to time t_1,

m = constant for components, $m = -1.2$, and

λ corresponds to the steady state failure rate, which takes place at $t_1 = 4400$ hours (6 months) of system operation.

(*ii*) Burn-in failures are the result of manufacturing errors and material defects.

To accelerate failures, temperature burn-in, heat test, and power cycling are the burn-in methods used for No. 10A RSS, and are based on other Bell System experience.

Steady-state failure rate data for No. 10A RSS plug-ins show that early failure rates can be estimated using the assumptions just described. Figure 26 shows the relationships among instantaneous failure

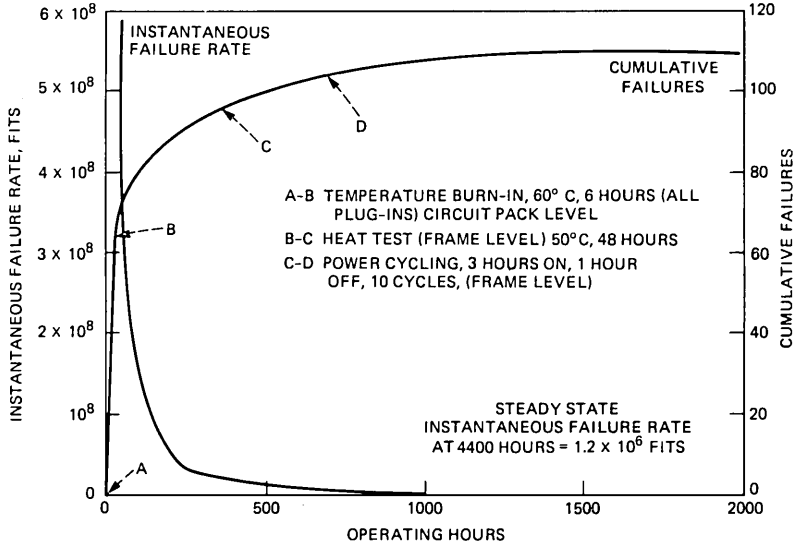


Fig. 26—Relationship between instantaneous failure rate, cumulative failures, and operating time.

rates, cumulative failures, and time of No. 10A RSS plug-ins subjected to operating stresses. The estimated number of failures for a fully equipped, 1024-line RSS frame is 115 within the first six months of operation in the field with no burn-in. Of course, some failures will be eliminated during system test and installation and before cutover. However, such failures are costly and place a burden on system test engineers and installers which, in turn, lengthens the duration of testing and installation. Based on this logic, it is assumed that the strategy of having failures occur during system test and installation for a system with no burn-in is offset by increased system test and installation interval.

The burn-in procedures for No. 10A RSS were intended to eliminate 85 percent of the failures in the factory. Table V and Fig. 26 show the burn-in procedures, acceleration factors, and failures eliminated. The economic analysis shows that a substantial net gain to the Bell System results because of the burn-in procedures.

5.7 Sparing philosophy for No. 10A RSS

As the price of plug-in modules increases with the advent of electronic systems and increased component density on plug-ins, a need for a sparing philosophy based on plug-in reliability appears to be necessary. To determine the spare requirements for RSS plug-ins, the Erlang-C traffic model is used, in which the spare requirements is a function of plug-in failure rate, turnaround time (spare replacement interval), and the service continuity objective (availability of spares when needed).

The main emphasis of the No. 10A RSS sparing philosophy is on quality of service to a customer or a group of customers and on economics. Based on these considerations, the plug-ins were divided into three classes:

Class I. Plug-in modules with frequent occurrences of failure.

Class II. Plug-in modules whose failure can cause partial or total

Table V—Factory burn-in

Burn-in Procedure	Acceleration Factor	Failures Eliminated	(See Fig. 3)
1. Temperature burn-in, all plug-ins 60°C, 6 h	3.4	64	*A* to *B*
2. Heat test RSS frame 50°C, 48 h	6.1	33	*B* to *C*
3. Power-cycling* RSS frame 3 h on, 1 h off, 10 cycles	—	7	*C* to *D*

* An acceleration factor of 8 can be estimated from data set experience at Bell Laboratories. More important, however, is that power cycling eliminates device failures that are caused by a unique mixture of thermal, electrical, and fatigue-type alternating stresses. Temperature burn-in alone may not be able to eliminate all marginal components based upon Arrhenius relationship.

service outage. This, of course, is a serious category in terms of spare requirements.

Class III. All other plug-ins whose failure would affect traffic capacity, quality of service, or system maintenance.

The classification of No. 10A RSS plug-ins, based on these definitions, are listed in Table VI.

In using the Erlang-C model for RSS, the relationship between the service continuity objective or availability and the load offered to inventory (L) is shown in Fig. 27. When the spare quantity required is less than or equal to one spare, two spares are assigned, with the additional spare acting as a "spare for a spare." When two or more spares were required, an additional spare was not provided.

The availability of the spare was taken to be 0.99, which means that once in 100 repairs there is no spare available. The failure rates and mean time between failures (MTBF) for all No. 10A RSS plug-ins, showed this availability level of 99 percent to be more than adequate for system operation. The condition of having no spares for all plug-

Table VI—Spare philosophy classification and spare requirement

Classification	FE Circuit	Circuit Name	Inventory Load*	No. of Spares
I	101	LI	1.44	6
II	104	FO	0.52	4
	107	DL	0.12	2
	108	GS	0.09	2
	109	MPA	0.051	2
	110	MEM I	0.078	2
	111	TR	0.033	2
	112	ALI	0.033	2
	113	MPB	0.027	2
	123	MEM II	0.069	4
III	102	G-J	0.276	3
	103	CI	0.180	2
	105	USC	0.282	3
	106	BOS	0.120	2
	114	TTR	0.036	2
	115	ROH	0.006	2
	116	PAB	0.009	2
	118	RLT I	0.009	2
	119	RLT II	0.006	2
	120	MSD	0.078	2
		Converters		
II		131N1	0.024	2
III		131L1	0.918	2
		J57380-C-1LI	0.036	2
		130L	0.006	2

* Inventory load = $\frac{\text{spare replacement interval}}{\text{mean time between repairs}}$

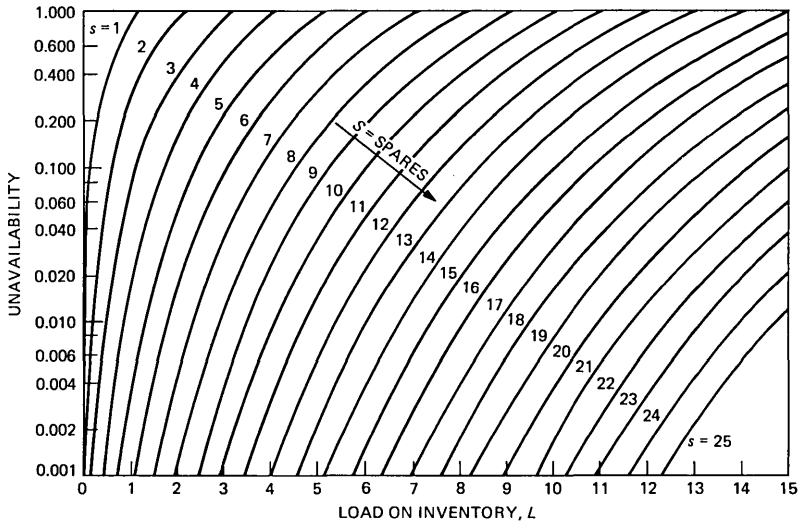


Fig. 27—Relationship between unavailability of spares and load on inventory.

ins, except the line interface (FE101) circuit pack (see Table VI), occurs less often than once every 40 years.

5.8 Sparing strategies: economic consideration

Sparing strategies depend mainly on the geographical location of the RT, on economics, and on service quality objectives. Three strategies are possible for the No. 10A RSS:

(*i*) Spares at both RT (Class I) and at host (Class II and Class III).
(*ii*) Spares at both RT (Class I) and at SCC (Class II and Class III).
(*iii*) Spares at RT (Class I), host (Class II), and at SCC (Class III).

The strategy to be selected is a judgmental matter and is a Bell Operating Company decision that is primarily based on the geographical location of the RT and on economics.

The sparing strategy (*ii*) is economically superior to (*i*) and (*iii*) and it meets the service quality objectives. The normalized price per RT for these strategies is shown in Fig. 28. With the increase in RTs per host and in hosts per SCC, the spare price per RT decreases. However, the price differences between strategies (*ii*) and (*iii*) are insignificant. Strategy (*i*) is uneconomical when there are only a few RTs, but it is an important strategy for situations where the SCC is too far from the host and the host is in the vicinity of all the RTs. Strategy (*ii*) appears to be economical and convenient to manage if the distances between the RTs and the SCC do not require craft persons to travel more than two hours to keep downtime within acceptable limits. Strategy (*iii*)

appears to be an acceptable solution if the distances involved between the RT and host are not overly significant and SCC is relatively far away from the RT and host.

5.9 Summary of reliability aspects of No. 10A RSS

(*i*) Service requirements are met in areas where the units are duplicated and replicated.

(*ii*) Burn-in in the factory must be performed to economically eliminate weak components and improve customer service. Steady-state reliability is achieved by cumulative 100-hour burn-in.

(*iii*) Spare requirements can be determined using the Erlang-C traffic model, where reliability information becomes a key parameter. Economical sparing strategy can be formulated by keeping spares at the RT, as well as at the SCC.

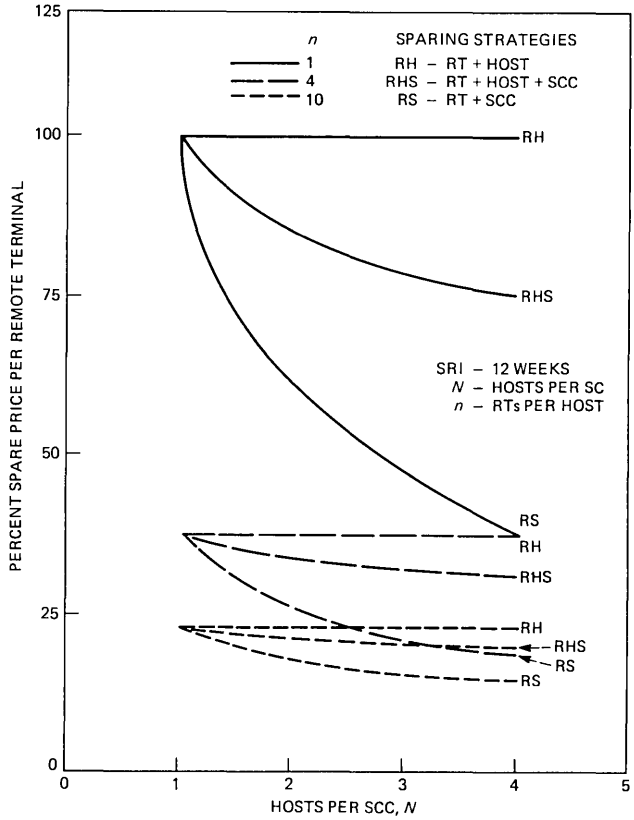


Fig. 28—Relationship between percent spare price per remote terminal and hosts per SCC for sparing strategies (SRI = 12 weeks).

VI. SUMMARY

Each aspect of the No. 10A RSS physical design serves to ultimately provide a low-cost, small-size highly reliable electronic switch. Interconnection technology selections were made to achieve low cost and small size. Frame layout partitioning and growth were devised to reduce equipment growth and to maximize plug-in apparatus, which decreases engineering and start-up cost. The resulting small equipment size maximizes the reuse of existing buildings or allows for the use of a small portable modular building. Circuit partitioning, sparing philosophy, and burn-in procedures ensure ESS central office service objectives, while providing low-cost maintenance.

APPENDIX

Downtime Calculations

A = Availability of a system.
$\bar{A}$ = Unavailability of a system.
$A + \bar{A} = 1$.
$A = \mu/\lambda + \mu$.
$\bar{A} = \lambda/\lambda + \mu$.
λ = Failure rate.
μ = Repair rate.
Expected down time
= $(\bar{A})(8760)(60)$ min/yr Simplex Model.
= $(\bar{A})^2(8760)(60)$ min/yr Duplex Model.
Expected down time in case of N duplicate units
= $(\bar{A})^N(8760)(60)$ min/yr.

Example

Consider a subsystem with 50,000 FITS, repair time = 4 h.
λ = (50,000) (10^{-9}) failures./h.
μ = 0.25 repairs/h.
Expected down time
= 105 min/yr (Simplex).
= 0.021 min/yr (Duplex).
= 0.42 by 10^{-7} min/yr (Triplex).

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No. 10A Remote Switching System:

Remote Terminal Firmware

By D. A. ANDERSON, D. R. FULLER, D. R. HANSON, and R. B. SCHMIDT

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The No. 10A RSS remote terminal (RT) is a part of a distributed telephone switching system consisting of one or more remote terminals controlled by a host ESS via data link communication. The RT is a microprocessor-based peripheral controller acting as an extension of the host network. The RT firmware contains a process-oriented operating system. Ringing and other high-power signals are supplied by universal service circuits used in a time-sharing arrangement. The RT firmware is responsible for scanning lines and reporting supervisory state changes to the host. These changes are reported over either the data link or a channel, depending on the state of the line. If data link communication fails, the RT leaves the normal master/slave mode and enters a special stand-alone mode to provide a POTS-type intra-RT service.

I. INTRODUCTION

The No. 10A RSS RT acts as an intelligent peripheral controller which follows call processing and maintenance orders sent over the data link from the host processor. In addition, the RT performs a large number of autonomous maintenance activities to ensure that all of its functions are being done correctly. In the event that data link communication with the host is lost, the RT is also designed to enter a stand-alone mode that provides simple intra-RT call service to its connected customers.

As with other telephone switching systems, high availability is also a requirement in the RT. This is achieved in part by duplication of the data link and duplication of the microprocessor controller (processor,

memory, peripheral access). The normal state is for one data link to be active and the other standby and for one microprocessor to be active and the other standby. Normally, the standby microprocessor is in a halted state that allows the active microprocessor to write simultaneously into both the active and standby memories. This keeps the standby memory up-to-date in the event that it is necessary to switch microprocessors. A certain portion of the RT firmware is devoted to the management of these duplicated units to ensure that the RT is in a working configuration and is capable of recovering from a hardware fault in one of these units.

In the development of the RT firmware, several program design techniques were used in an attempt to produce a more understandable, maintainable, and easily debugged code. These techniques included peer reviews at the program requirement, design, and code levels, extensive use of the high-level language C, and modular hierarchical program structures. Modules were coded as C functions or as assembly language subroutines using the same linkage conventions as the C compiler. Module coding standards were very important and helped the many programmers involved produce a uniformly good and understandable product. Coding standards required a comment prologue at the beginning of each module describing its purpose and inputs and outputs. Also important were the use of structured control constructs, with proper indentation, and the elimination of unnecessary "go-to's." Module sizes were normally kept to a couple of pages of program listing for understandability.

II. OPERATING SYSTEM STRUCTURE

The techniques described above are sufficient for programming a single task well. However, since in the RT many tasks must execute concurrently, the concept of an operating system becomes attractive to solve the complex problems that arise in a multitask environment. Also the local data hiding aspects of processes and the global data hiding aspects of monitors provide a good structure to limit and control interactions between tasks.

A process has a single entry point, which is called by the operating system, and returns when it is done. A process reads and writes only its own local (private) data and communicates with other processes through monitors. A monitor reads and writes global (shared) data and consists of the set of routines allowed to read or write a particular global data area. A monitor routine is passive in the sense that it only executes when called by a process. Monitors are necessary when two or more processes must communicate and perform the function of hiding the global data structure where the communication actually

takes place. Monitors are especially useful in the RT to hide the data structures necessary for seizing and releasing peripheral resources.

2.1 Scheduling mechanisms

The operating system supports three general categories of program activity: (*i*) base level, (*ii*) interrupt level, and (*iii*) reset level. Most processes execute at base level under control of the base-level scheduler. The operating system is nonpreemptive in that processes give up control voluntarily. The interrupt and reset levels are entered only as the result of a hardware interrupt. Interrupts always return to the point of interruption, whereas resets, which are caused by error conditions, may not return to the point of interruption. Each interrupt enters a separate program structure with its own stack and is overseen by a handler that performs the simple process scheduling required for that level.

The base level scheduler is actually a hierarchy consisting of a main scheduler and several subschedulers. The main scheduler provides two general forms of priority: (*i*) classed priority and (*ii*) timed priority, where priority simply means the frequency at which a process receives control. Under classed priority a process may be in one of three classes termed A, B, and C. Class A processes receive control twice as often as class B and four times as often as class C, according to the sequence ABACABA which is repeated endlessly. Under timed priority, a process receives control at fixed time intervals with a minimum period of once every 100 ms to a maximum period of once every 24 hours. The fixed time interval must be a multiple of 100 ms, 1 second, 1 minute, or 1 hour.

The class C-to-class C time interval is approximately 50 ms under no load and increases as the load increases. Timed scheduling is performed as required between the scheduling of each class with a maximum rate of once per class (or equivalently, 8 times per C-to-C cycle). When the C-to-C cycle time exceeds 800 ms, the system is in overload and some random 100-ms work cycles will be skipped. Each process when called gives up control voluntarily and is designed to keep most of its time segments under 10 ms. As protection against insane processes, a hardware sanity timer causes a reset if not restarted frequently by the operating system.

The base level scheduling algorithm has been kept fairly simple to minimize the overhead consumed by this portion of the operating system. Basic scheduling information is kept in a set of vector tables defining entry points and a set of cycle tables defining frequency of entry. These tables are built at compile time and, thus, define permanent scheduling information. This table-driven approach has the advantage of being easy to administer whenever changes are made.

Interrupt level is used to provide control for those processes that have critical timing requirements. The two normally occurring interrupts are the active data link interrupt and the 10-ms interrupt. A data link interrupt occurs each time the data link hardware is ready to transmit or has received a byte of information. Received bytes are buffered at interrupt level for later examination at base level where complete data link input messages are routed to the appropriate clients by the operating system. Data link output messages are also loaded into the active transmit buffer by the operating system at base level and sent out byte by byte at interrupt level. Of lower priority than the data link interrupt is the 10-ms interrupt which is used to control several processes that require timing more accurate than available at base level. These processes are associated with ringing telephones and surpervising lines at a fast rate.

A reset is the highest priority interrupt and in some cases is not maskable. A reset may be caused manually but in general it is caused by a check circuit sensing an error condition, such as a sanity timer timeout, parity error, write-protect violation, etc. Many of the recovery routines execute only in the event of a reset since they perform functions associated with switching microprocessors and system initialization. As in other program-controlled switching systems, the RT firmware provides several forms of initialization less severe than a complete initialization. Repeatedly occurring resets cause an automatic escalation in the severity of initialization performed, up to the point of clearing all transient telephone calls. Normally, a complete initialization can only be induced manually.

2.2 Memory management

The memory management needs of the RT are influenced by the architecture of the microprocessor used, namely, the *BELLMAC**-8. Assembly language instructions of the *BELLMAC*-8 refer to sixteen 16-bit general registers, but these registers are actually located in memory at a point determined by the address contained in a 16-bit hardware register called the rp (register pointer). The rp can be loaded with any memory address (on an 8-byte boundary) and generally points to an area called the rp stack, since the contents of the general registers can be saved and restored quickly by proper bumping and debumping of the rp. There is also a 16-bit hardware register called the sp (stack pointer) which points to an area called the sp stack. Return addresses, register contents, and other variables can be pushed, popped, or otherwise accessed on this stack. By the appropriate saving and restoring of these two hardware pointers, the context switching

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required when calling subroutines, handling interrupts, or switching processes can be made very efficient in the *BELLMAC*-8.

The *BELLMAC*-8 has 16-bit addressing capability which allows the system to access 64K bytes (where K is 1024). To control peripheral hardware, the RT uses a memory-mapped I/O scheme. The first 32K of the address spectrum addresses memory and the last 32K addresses peripheral hardware. Since 32K of memory is not nearly enough for the RT firmware, a memory-bank switching scheme has been implemented. In the same address spectrum as the periphery, several 32K banks of memory are placed. (See Fig. 1.) A bank select register, external to the *BELLMAC*-8 and under operating system control, decides which bank is selected.

The first 32K or base page of memory is always addressable. All stacks and other writable variables are located here to be accessible to programs executing in any bank. Interrupt handlers, programs that modify the bank select register, and programs that physically read and write the periphery must also be located in the first 32K.

It is important to hide from programmers the linkage required when a subroutine in one bank calls a subroutine in another bank. This linkage is provided automatically for RT firmware by a combination of an overlay link-editor and the trap handler of the operating system. When the link-editor encounters an interbank call, it replaces the call instruction with a special illegal instruction and a pointer to a transfer table entry. The transfer table built by the link-editor contains subroutine addresses for interbank calls, plus the corresponding bank numbers. When the *BELLMAC*-8 executes an illegal instruction, a reset-like interrupt occurs to the trap handler located in the first 32K of memory. If the trap is caused by the link-editor, the trap handler stacks the current return address and bank number, loads the bank number of the called routine, and makes the actual call. Upon return from the called routine, the trap handler restores the previous return address and bank and returns to the calling routine. Traps not caused by the link-editor are treated like an error reset.

Since interbank calls involve more overhead than intrabank calls, the placement of routines in banks is not done at random. Instead, an attempt is made to place related routines in the same bank. The placement policy of routines in banks is administered manually and achieves a best-guess form of optimization.

2.3 Process management

Before describing the implementation of process management in more detail, it is necessary to define the term process descriptor. A process descriptor is the block of writable memory associated with a process that defines the current state of the process. The process

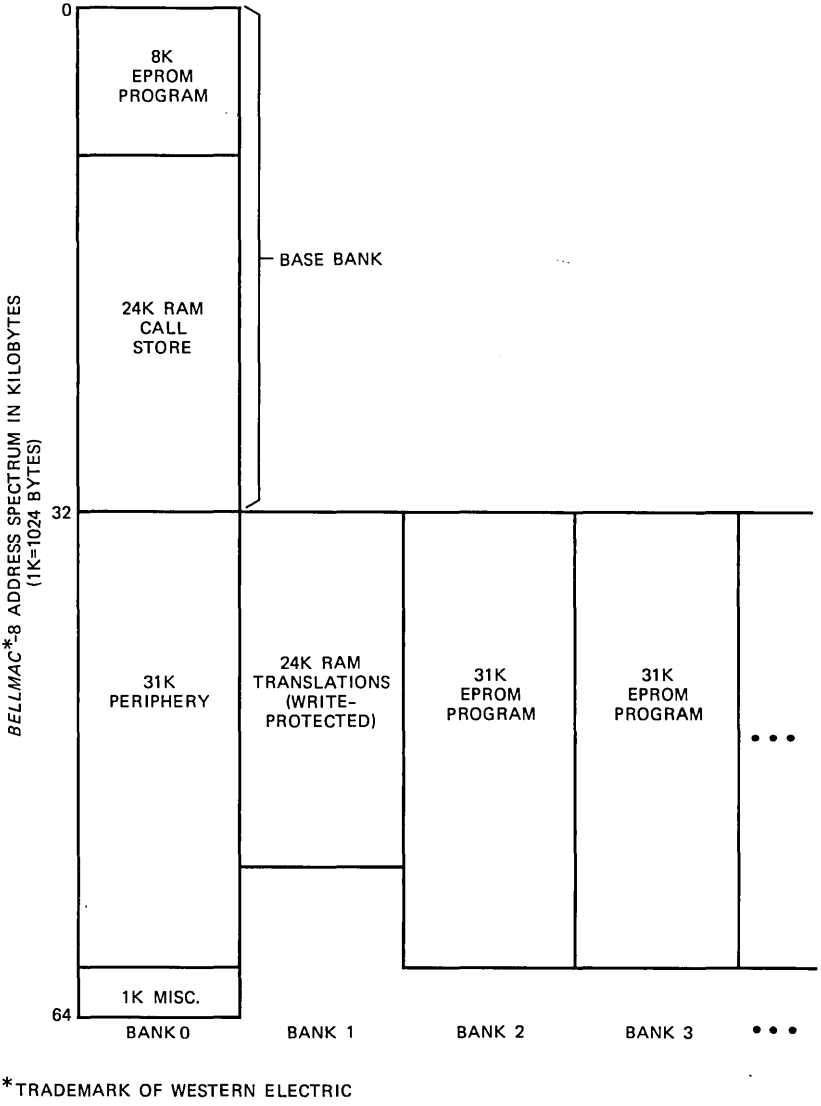

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Fig. 1—Memory bank structure.

descriptor remains unchanged, while the process takes a time break and for this reason the contents of the process descriptor is very important in determining the program structure of the process. For example, a process descriptor containing a stack allows the process to take a time break while nested several subroutine levels deep. This feature can be extremely valuable for producing an understandable hierarchical program structure.

However, process descriptors with stacks also raise some important questions. How big should the stacks be? Should stacks be dynamically allocated to conserve memory? Can enough concurrent processes be provided to meet system requirements? Is this a reasonable way to utilize memory? The remainder of this section will attempt to explain how these questions were answered for the RT firmware.

First, telephone traffic is well understood and it is possible to estimate the arrival rates and holding times of the various tasks required of the RT. Second, the stack usage conventions of the C compiler are known, and it is possible to estimate stack sizes for storing local variables and passing parameters. The results of this brief examination indicated that it would be very expensive to support each task to be done with the same general-purpose process descriptor.

The RT solution to this general problem was to break the system into several different kinds of processes and to provide a different kind of process descriptor for each. Large descriptors with more general layouts were provided for tasks with few concurrent processes and smaller descriptors with more specific layouts for tasks with many concurrent or real-time intensive processes. This approach tends to make the operating system special purpose, but it appeared to be the only way of incorporating the process concept into the RT firmware and, yet, efficiently meet the system requirements.

The seen and unforeseen complications of dynamic stack allocation were eliminated by taking a conservative approach and not providing this feature. Instead, the size and number of process descriptors is fixed at compile time. The only dynamic stack allocation done at execution time is that which occurs for the allocation of local variables within functions when they are called. Interrupt handlers also have their own dedicated stack areas so that room does not have to be provided for interrupt variables in each individual base-level stack area.

Stack sizes are an important consideration and were determined by the following methods. Initially, estimates were made based on providing a certain number of subroutine nesting levels. Later, a software tool was developed to statically examine written code and chart the nesting structure of processes to determine their deepest stack usages. Stack overflow violations were corrected by changing the code or enlarging the stack. Finally, a stack audit was incorporated into the system to dynamically look for stack violations. This audit is performed by periodically checking the last byte of each stack and making sure it always contains a zero.

2.4 Time critical processes

Time critical processes must respond quickly to call processing

inputs. The ROB (Remote Order Buffer) process is the most general time critical process at the RT. It is the primary base level workhorse and is scheduled as a class A task. In the normal host-controlled mode, ROB processes receive data link orders from the ESS host, execute these orders, and return a success or fail acknowledgment. In the stand-alone mode, these processes take over the role of handling entire telephone calls themselves, one transient telephone call per ROB.

The process descriptor for a ROB process is quite large. The rp and sp stacks account for most of this size and are estimated to provide 10 levels of C function nesting. In addition, there is a third stack in each descriptor for bank switching. The top of this third stack is located by a 16-bit pointer in memory called the Bp (bank pointer). This stack is used by the trap handler to store the current bank number and return address when an interbank call occurs. Note that it is important for the trap handler to be reentrant since other interbank calls can occur during an interrupt or during a time break.

When a ROB process takes a time break, it calls an operating system subroutine and passes it a timing parameter. This subroutine saves the current values of the rp, sp, Bp, and bank number in the process descriptor, restores their previous values, sets up the specified timing, and returns to the operating system. Later, after the specified time has passed, these pointers are restored and control is given back to the ROB process via a subroutine return. This method of context switching is very efficient since it involves little more than saving and restoring several stack pointers.

Another important time critical process is the USC (Universal Service Circuit) process which is scheduled at the 10-ms interrupt level to ensure short and accurate timing. A USC is a hardware circuit with metallic access to a group of lines. It is primarily used to ring telephones but can also perform power cross tests, party tests, and coin control functions.

In contrast to ROB processes, USC processes are designed to perform a very specific task in a very efficient manner. For example, the USC process descriptor contains a small sp stack only large enough for a few return addresses. During execution, the USC process uses a common rp stack but any information left in this stack during a time break is lost. Timing during a time break is provided by linking the USC process descriptor at the proper point for the amount of delay requested to a timing list especially designed to minimize operating system overhead. Any delay in multiples of 10 ms up to 1 second can be requested.

The remaining time critical processes are controlled by the RT operating system on a so-called one-shot basis. No time break mechanism is provided for such processes; they are called periodically, perform some quick task, and return. Any change in per-entry behavior

of such processes occurs as the result of changes in information read from the periphery or from global data structures. These one-shot processes use the same common rp, sp, and Bp stacks as the operating system. A good example of such a process is the line-scanning process which is called frequently to look for potential line originations or disconnects. This process also performs hit timing and flash timing.

2.5 Time deferrable processes

The remaining processes are referred to as time-deferrable processes because they do not handle customer affecting inputs. For this reason, they are deferrable and, during heavy load, can be given control less frequently.

The RT operating system supports three kinds of time-deferrable processes: (*i*) audit processes, (*ii*) BGT (BackGround Task) processes, and (*iii*) a special data link diagnostic process. There is one process descriptor for each of these three kinds of time-deferrable processes and hence only one process of each kind can be active at a time. These processes are all normally scheduled as class C tasks but in some cases can enter higher priority modes of execution. One case occurs when a ROB process is blocked by a resource seized by a diagnostic BGT process. At this point, the BGT process begins executing as a class A task until the resource is released. This action minimizes the amount of time the ROB process is blocked.

The purpose of an audit process is to examine global data structures to verify that they contain legitimate information. This service is necessary in continuously running systems to free resources that otherwise get lost slowly as the result of program bugs or hardware failures. In the RT, only one audit process is active at a time and, when it completes, the next audit is automatically started in a continuous audit cycle. To support time breaks, the audit process descriptor contains three stacks which are identical in function and similar in size to the ROB process stacks.

Also identical in function but much larger in size are the stacks of the BGT process descriptor. This large size is needed to support the deeper subroutine nesting structure and greater use of local variables required by certain BGT processes. There are quite a number of different BGT processes to provide the various maintenance and administrative functions needed occasionally but not simultaneously at the RT. The bulk of these processes are diagnostics to help a craft person locate and repair hardware faults.

A BGT process is normally inactive for relatively long periods of time until a request is made for its service. If another BGT process is currently active, the operating system will queue a limited number of additional requests. The BGT processes are requested either automat-

ically on a timed basis or manually on a demand basis or in some cases both ways. The BGT processes are also unique in that they can be aborted manually by host TTY input message.

The BGT processes can also execute at interrupt level by calling a special operating system subroutine and passing it a delay parameter. This subroutine uses the delay parameter to initialize a programmable timer that causes an interrupt when it times out. When the interrupt occurs, control is given back to the BGT process via a subroutine return. This form of time break can be used any number of times in sequence, effectively allowing a BGT process to raise its priority of execution above base level. Normal base-level execution is resumed by taking a standard time break. This feature is valuable when diagnostics need to delay an accurate amount of time.

To the operating system, BGT processes appear as subroutines that are called and return when done. This structure also allows one BGT process to call other BGT processes as subroutines. This hierarchical structuring ability has the valuable consequence of allowing one to build a large process from several small ones. One important use of this feature is in the routine exercise BGT process run nightly at the RT. This process calls, in a prescribed sequence, all of the diagnostic processes which are otherwise requested manually on an individual basis.

The data link diagnostic process, which performs the necessary testing at the RT end of the data link, is under control of the host. This process has its own process descriptor so that the host may diagnose the data link any time it wishes without being blocked by other activity at the RT. The data link diagnostic process also has a unique interface with the operating system. It may call a special operating system subroutine that returns control on the next off-line data link interrupt. Repeated calling of this subroutine allows this process to change its mode of execution from base level to data link interrupt level, a feature essential to completely test the data link.

III. DATA LINK MESSAGE HANDLING

Messages sent over a 2400-b/s serial data link provide the primary means of processor-to-processor communication between the RT and the host. The link is a two-way communication path with each end capable of sending and receiving concurrently. For reliability, the data link is duplicated with the normal configuration being one link in the active mode and the other link in the standby mode. Both RT microprocessors have access to both data links which allows either microprocessor to be active, independent of the data link configuration. In addition, it allows the active microprocessor to communicate over both links concurrently for testing or other purposes.

The data link interface hardware at the RT converts a serial bit stream on the link to and from (8-bit) bytes of information for the RT firmware, plus performing certain control and checking functions. The RT data link message handling firmware is completely interrupt driven by the interface hardware. Each byte received causes an interrupt at a maximum rate of 3.3 ms per byte. Similarly, at the same maximum rate, an interrupt is caused each time the hardware is ready to transmit another byte. On the data link, a limited number of data bytes are grouped together, along with certain control and checking bytes to form a frame which is transmitted according to a standard protocol. The frame protocol is designed to provide a high degree of error control. Data bytes are initially sent and ultimately received in a higher level protocol termed a message. The message protocol is designed to provide a unit of information exchange between RT and host programs and simply contains message delimiting, routing, and size information, plus data. A message may be contained in any fraction of one or more frames.

3.1 Frame protocol

The frame protocol is the standard CCITT X.25 format of the Synchronous Data Link Control (SDLC) protocol. It is a positive acknowledgment/retransmission scheme with extensive checking to provide a high degree of error control for a single data link. Configuration and state control of the duplicated data links is handled at the message protocol level. The X.25 protocol has special commands to bring up or disconnect the link. There are also special commands to turn off and restart transmitting to prevent sending data at a rate faster than it can be received.

All traffic over the link, whether it be special commands, responses, or actual message data, is transmitted in the form of frames. A frame consists of from 6 to 22 bytes in the following fixed sequence:

1 flag byte,
1 address byte,
1 control byte,
0 to 16 data bytes,
2 CRC (cyclic redundancy check) bytes, and
1 flag byte.

An idle link is marked by a continuous sequence of ones. A flag byte consists of a zero followed by six ones and a zero, (01111110) and denotes the beginning and ending of a frame. A single flag may also close one frame and open the next frame. The address byte simply distinguishes between commands and responses. The control byte distinguishes the different frame subtypes and also contains the sequence number information for the positive acknowledgment proce-

dure. Data bytes have unrestricted value and the hardware automatically inserts and deletes a zero bit after all sequences of five contiguous ones to ensure a flag is not contained in the data. The CRC bytes are also generated and checked by hardware to detect any errors introduced during the transmission of the frame.

All information frames are numbered modulo 8. Up to seven information frames may be sent before transmission must stop to wait for an acknowledgment. Frames are acknowledged by sending the sequence number n of the next expected frame, thereby acknowledging all frames with sequence numbers n-1 or less (modulo 8). All unacknowledged information frames are retransmitted after an appropriate timeout period to take care of cases where information frames or acknowledgments are lost on the link. In retransmission cases, the sequence numbers per frame are very important in distinguishing new frames from retransmitted frames to prevent accepting the same frame more than once.

3.2 Message protocol

Messages to be sent to the host are placed in a circular transmit buffer where they are extracted one byte at a time by the interrupt driven data link control program and placed in the data section of an outgoing frame. Conversely, data bytes from incoming frames are placed one byte at a time at interrupt level into a circular receive buffer where they are partitioned at class A base level into individual messages. A message is a sequence of 16-bit words with the following simple format:

1 sync word,
1 message header word, and
0 to 32 data words.

The sync word is a fixed bit pattern and is used to find the beginning of a probable message after power up or any other cause of message mutilation. The message header contains the client identity and message size information needed to properly route messages. Data words have unrestricted value.

When a complete message has been received in the data link receive buffer, the entire message, without the sync word and usually without the message header word, is moved by the RT operating system into the specified client message buffer. Each client buffer has a load and unload pointer associated with it, and these pointers are updated properly to notify the client of a new message. Each client scans its buffer for new messages at a frequency dependent on load and priority. As orders contained within the message are executed, the client buffer pointers are adjusted accordingly until the two pointers are equal signifying an empty buffer.

3.3 Link state control

The data link transmit buffer and receive buffer, plus associated pointers and protocol state variables, are organized into a single structure termed a data link record. There are actually two data link records, one always associated with the on-line (or active) data link and the other always associated with the off-line data link. The RT keeps a single flag denoting which link, 0 or 1, is associated with the on-line record.

The two data link records give the RT the capability of receiving and transmitting messages over both links concurrently. However, messages to be transmitted are normally placed in the on-line record, unless a specific request is made for the message to be placed in the off-line record. This is done only for certain test and error messages.

Configuration of the duplicated data links is entirely the responsibility of the host which informs the RT of its decision via a special data link switch message. This message specifies which link, 0 or 1, is to be associated with the on-line record. Upon receipt of such a message, if the specified link is currently associated with the on-line record, nothing is done. If not, the RT flag is toggled and the on-line record is immediately associated with the opposite link. Any loss or duplication of data caused by this switch is cleaned up by the frame protocol.

The RT firmware has extensive data link error control and recovery checks designed into it. The data link records are audited frequently by normal message and frame handling programs for protocol violations, out-of-range pointers, and other illegal states. In addition, the data link records are audited once a second at base level for deadlock conditions. Protection against hardware failures is provided by masking off invalid or too-frequent data link interrupts to prevent them from overloading the microprocessor. Either link interrupt may be independently masked. Once a second at base level, an attempt is made to reinitialize the data link hardware associated with any masked interrupt and, if successful, the interrupt is again unmasked.

As the last line of defense in helping the host reconfigure and recover the data links properly under all possible situations, three special RT-to-host messages have been implemented. The first message informs the host that the RT has received an input message with improper message protocol. Upon frequent reception of this message from the RT, the host should assume a data link hardware failure has occurred. The second special message is sent by the RT when it finds an input message in the off-line data link record for a client that always receives messages from the active link. Since this evidence suggests that the host and RT no longer agree on the active link, this message is sent via the off-line record and asks the host to send a data link switch message specifying the currently active link. The last message is sort of a "heart

beat" since it is sent every 10 seconds by the RT. Each time the host receives this message, it returns a special acknowledgment message. The absence of this handshake arrangement for a period of time indicates to both the host and the RT that one or both of the links are down. It is the responsibility of the host to initiate recovery actions in this case.

IV. METALLIC ACCESS CONTROL

Telephone switching systems exist to allow customers to talk or send data to each other. The voice and data signals are similar to each other, and are characterized by modest power levels and a frequency range of 200 to 3200 Hz. If the RT were required to carry these kinds of signals only, then the solid state voice network that it has would suffice. There is another set of signals, however, that is incompatible with this solid state network. These signals have too much power (ringing), or have too low a frequency (party test), or both (coin collect) to be carried by the voice network.

An auxiliary network is necessary to apply these signals to customer lines. Since there is much less signaling than voice traffic, this auxiliary network can be more concentrated than the voice network.

In other switching systems, the high-power signals are provided by circuits called service circuits. These service circuits are usually single-purpose circuits, such as ringing circuits or coin control circuits. The No. 10A RSS RT design has a general-purpose circuit providing ringing, party test, and coin control. This circuit also provides dc access to the customer lines for other more specialized circuits. This general purpose circuit is called the Universal Service Circuit (USC).

The Line Interface (LI) boards have A and B metallic access relays per line circuit. Each metallic access relay connects a line circuit to a bus, and each bus is wired to relays of two USCs. (See Fig. 2.) Each pair of USC's has access to eight of these buses, and there are thirty-two LI circuits wired to each bus. Thus, each group of 256 lines has access to a group of four USCs. Note that the access network has the possibility of blocking.

4.1 Universal service circuit time sharing plan

Metallic access buses are used mostly for ringing. In North America, ringing usually consists of a two-second burst of ringing followed by four seconds of silence. Note that in the four seconds of silence, a single source of ringing current could be ringing two more phones by reconfiguring the access between the ringing current source and the phones being rung.

The No. 10A RSS takes advantage of this capability to reconfigure the metallic access network every two seconds. Thus, one USC can

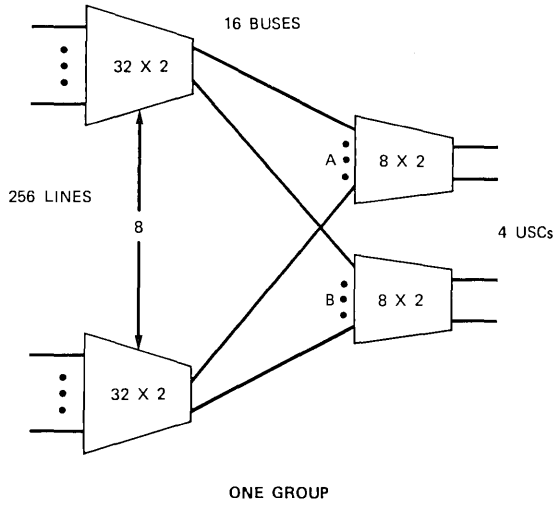

Fig. 2—Metallic access network.

supply ringing to three phones. The metallaic access control software is written to give each USC three time slots, and each time slot is two seconds long. In the case of normal ringing, a time slot is used to apply the 20-Hz ringing voltage to the line and scan for customer off-hook (ring trip). During the 4-second silent interval, no USC is connected to the line and the LI circuit is scanned for customer off-hook (ring trip). The beginning and end of each of these time slots is defined by a program entry. The program looks for work to do in a per-time slot database.

Each group of four USCs has two A metallic access bus USCs and two B metallic access bus USCs. The B USCs are delayed in time with respect to the A USCs by one-half time slot. Thus, any given line at any time has the potential of one complete time slot available starting in one second or less.

In a large RT, there may be eight groups of four USCs. The time slots corresponding to these eight groups are staggered in time. This is done because starting a time slot or ending a time slot requires many processor cycles. Spreading the group start-up periods in time spreads this processor load out in time.

There is a set of programs called the USC operating system which is driven by the 10-ms timed interrupt. These programs keep track of what time it is, start the control programs (which actually connect the USCs to the lines desired and accomplish the desired functions), provide real time breaks, and tell the USC selection routines what time it is so that the routine can select the next time slot.

4.2 Universal service circuit administration and timing

To understand how USCs are administered, it is necessary to briefly describe the USC administration databases.

There is a buffer per USC containing per-USC information and a small stack. The *BELLMAC*-8 stores return addresses on the stack. Putting a stack in each USC buffer allows the control programs for each USC to take real-time breaks easily. All that is required is for the real-time break routine to remember what the value of the sp was when the break was taken, and to restore the sp after the break is over. The control routine may resume processing, since the string of return addresses necessary to get back to the first subroutine call is intact and pointed at by the sp.

Each USC buffer contains three time-slot buffers with information pertaining to the USC function being performed in that time slot, and the necessary pointers to exchange information with other programs.

Each USC can ring three different phones at any time by using the three time slots. Thus, there must be three busy/idle bits per USC for USC selection purposes.

To select a USC time slot, it is necessary to know

(*i*) The number of complete time slots necessary to hold the function to be performed. If only a partial time slot is desired, then the length of time (in tens of milliseconds) necessary to accomplish the desired function.

(*ii*) How far ahead in time the USC selection routine is to look. This prevents long delays, i.e., instead of selecting a time slot four seconds away to do a party test, the selection routine will return a blocked indication.

(*iii*) What time is it now with respect to the time slots of the USCs that can service the line in question. This information is necessary so that the routine can select the next occurring idle time slot.

After deciding which time slot or time slots can hold the function, the USC selection routine then makes those time slots busy by marking the time slot busy/idle bits.

The USCs are normally administered independently of the host. This is necessary because USC time slots must be chosen in time order, and it would be extremely difficult to keep the host and the RT in precise synchronism.

After the time slot is chosen and seized, the time slot buffer or buffers are loaded with the information necessary to do the function. If the time slot chosen is occurring at the time it was selected, the control routine is started immediately. If, however, the time slot is due to start at a later time, the time slot is started later by the USC operating system.

The USC control routines must report the status of the function

performed to the routine that initiated the function. If the function is regular ringing, then the report occurs only if the function was started immediately. This prevents long holding times on Remote Order Buffers (ROBs) on high-runner calls. Functions other than ringing always get reports from the USC control routines.

In the control of the USC, there are occasions when waits are desired. For example, when relays are operated there will be several milliseconds between the signal that puts current through the relay coil driver and the actual closing of the contacts. The USC operating system, as mentioned above, can suspend processing by remembering the value of the sp at the point where the real-time break is requested. The USC operating system has a series of linked lists for taking real-time breaks. Each list corresponds to a different real-time break, i.e., there is a list for 10-ms breaks, one for 20 milliseconds, etc. The USC operating system links the USC buffer onto a linked list when the control program calls the real-time break routine. After the time is up, processing resumes on that USC by restoring the sp (stored in the USC buffer) and resuming processing. This scheme was adopted because it can be administered very efficiently.

4.3 Universal service circuit functions

When ringing telephones, some of the tests made in the first cycle of ringing are the following:

(*i*) A test is made to verify that no other LI circuits are connected to the metallic access bus used for this particular USC-to-LI connection. This is necessary to avoid interference between the two circuits connected to the bus.

(*ii*) There are USC and LI logic tests done to assure that the circuitry used to ring the phone is in proper working order.

(*iii*) A measurement is made to assure that there are no high voltages on the outside plant. This measurement, called a power cross test, protects the USC used to ring the line.

Subsequent ringing cycles for the same call eliminate the above tests, except for the first metallic access bus test.

Reverting ringing is used to alert the calling customer and the called customer if both parties are on the same party line. This kind of ringing requires two time slots, one for each customer. Instead of writing a special control program for reverting ringing, this kind of ringing uses two time-slot buffers, each loaded with the information to ring one of the associated parties.

There are three basic kinds of coin orders: collect, return, and presence test. Coin collect and return orders put 130 volts onto the tip conductor. The difference between the two functions is the polarity of the voltage. Coin presence tests put a positive or negative potential on

the tip conductor and test for the presence or absence of a ground by whether or not current flows.

Party test is almost exactly like the coin presence test; that is, a potential is applied to the tip conductor and the presence or absence of current is tested using the USC measurement capability.

V. LINE SUPERVISION PROCESSING

In the 10A RSS, the host system has overall control of calls, but it does not have direct access to the line supervisory states. The only call-processing circuits in the RT that can scan the line are the USCs (during ringing) and the LI (all other times).

The RT controller has the responsibility of scanning RT lines and sending the supervision states to the host. There are two paths for this information: via the channels or via the data link. If a line is connected to a channel, the supervisory state of the line must be written to the channel because the solid-state voice network will not pass dc signals. The supervisory state that is written to the channels by the RT processor is reflected by the channel circuit at the host and used to supervise the line. The data link is used for reporting supervision changes for lines that are not connected to a channel.

5.1 Off-hook and on-hook scanning

The RT has an off-hook scan program and an on-hook scan program. Each program is run every 200 ms, and the two are run 100 ms apart. Not every line is looked at by each program. For example, lines that are in the origination (idle) state are not looked at by the on-hook program, since on-hook lines in the origination state are of no interest to the host. This selective scanning is done by having a mask table for each routine. Lines in the origination state have ones in the off-hook mask table, corresponding to their equipment locations, and zeros in the on-hook mask table.

When the off-hook or on-hook scanning routine finds a line in the state for which it is looking, the routine must consult an item called a Path Memory Remote (PMR) table entry to find out what to do with the line. For example, assume that the off-hook scan routine finds an off-hook and then consults a PMR. If the PMR indicates that the line is in the origination state, the off-hook is treated as an origination. If the PMR indicates that the line is connected to a channel, the off-hook is treated as a change of state and the channel supervisory flip-flop is updated.

The functions that can be performed by the off-hook and on-hook scan routines are as follows:

(*i*) The programs pass the supervisory state of lines that are connected to channels to the channels. This is done by scanning the

lines as they go into the pass supervision state and writing the appropriate state to the channel supervisory flipflop. Then a bit is set in the opposite scan mask table so that changes of state will be discovered by the opposite routine. When the routine discovers a change of state, it updates the channel circuit supervisory flip-flop, resets the bit in its own scan mask table corresponding to the line just found, and sets the bit in the opposite table.

(*ii*) The programs perform timing by setting both of the bits in the scan mask tables and using the PMR to count time intervals. Since both bits are set, the timer is incremented every 200 ms regardless of the supervisory state of the line.

(*iii*) The programs inform the host of line supervisory changes by scanning for a given change, then sending a message to the host when it is found.

(*iv*) The programs must scan intra-RT calls for disconnect, since intra-RT calls use no channels to the host. Since one or both of the parties may have flashing privileges, the RT may have to time the length of on-hook intervals to make sure that they are not flashes.

(*v*) The programs discover originations. This is discussed in the next section.

5.2 Origination processing

After a line originates, the origination is verified by doing a rescan and making sure that the line is not back on-hook. The line is then put into a buffer called the origination hopper and an origination message is sent to the host.

After the message has been sent to the host, the line is timed. If the host does not respond in a timely manner, the origination message is sent again. Another timeout causes a special origination message to be sent to the host which can clear up some RT and host data inconsistencies which can cause lines to be ignored.

Line Load Control (LLC) is an origination restricting feature that a switching machine can invoke when the machine is overloaded with traffic. If the host machine gets into this condition, it sends a message to the RT to go into the LLC state for three minutes. When in this state, the RT scans only certain high priority lines such as fire and police numbers and one-seventh of the remaining customers. The one-seventh of customers that are scanned is changed every time through the off-hook scan routine.

The RT drops out of the LLC state if the LLC message is not received at least once every three minutes.

The RT can recognize an overload condition within itself. This occurs when regularly scheduled work is not done, and results in the RT

suspending origination scanning for a brief period of time. This is independent of the LLC condition mentioned above.

5.3 Fast passing of supervision

For lines in certain states, supervision must be passed at a faster rate than allowed by the off-hook and on-hook scanning routines. This is done by interrupt level routines that pass supervision at 10- and 20-ms intervals.

To prevent this passing from becoming a burden to the processor, very special measures must be taken. The database described below makes this passing of supervision a tolerable burden.

The *BELLMAC*-8 chip has no on-chip registers where data are held and processed, but rather uses main memory for this data storage. The area of memory being used as registers is pointed at by the rp. Register-oriented commands are really memory manipulation commands.

Since the registers are really memory, it is possible to point the rp to memory that has been loaded with the data necessary to do some function. This simple operation has the effect of loading that data into registers.

In RSS, this scheme is used to save processor cycles for the fast passing of supervision. The data necessary to pass supervision is stored in memory in the form of linked lists, i.e., each piece of data that is used to pass supervision on one call has the address of the next piece of data. Loading this address into the rp has the same effect as mentioned: the data are loaded into registers.

There are two cases where this fast supervision is necessary. When a dial pulse line is dialing, a dial pulse can shrink to as low as 11 ms in length. Thus, lines in the dialing state need passing of supervision at a 10-ms rate.

Lines that are being rung also need fast passing of supervision so that the ring trip at the RSS is processed promptly at the host. This need is not so stringent, so passing of supervision on lines being rung is done at a 20-ms rate.

The ringing pass supervision routine also must do some processing on lines that have tripped ringing. The ringing connection that is up (if the ring trip occurred in the two-second active interval of the ringing cycle) must be torn down and the USC and metallic access bus made idle. The channel must be put into the talk state, and the LI must be put into the talk state.

VI. REMOTE ORDER PROCESSING

Electronic switching systems are generally designed as call-oriented systems. A call coming into the system is assigned a memory block,

and control of the call is passed through various programs to handle particular parts of the call. However, the primary focus of the system is still the call.

The RT of the No. 10A RSS is not call oriented. Instead the central focus of the RT is the processing of remote orders from the host. The RT orders consist of operations to be performed on the RT peripheral hardware. Each order describes both an operation and a logical circuit on which to perform it. Examples include path orders, line scan orders, ring orders, and coin orders. These orders which correspond to particular parts of a call are under control of the RT, but total call control is resident in the host.

The philosophy of this control between the host and the RT is one of a master/slave relationship. The host, being the master, controls the actions of the RT on a functional basis. Orders to execute specific functions are sent to the RT over a data link. The RT, being the slave, receives these orders and executes the functions. Acknowledgments indicating the status of order execution are returned to the host.

The master/slave relationship provides a simplified view of the operation of the host and RT. The orders received from the host over the data link can cause quite different actions to be taken by the RT, depending on the state of the lines involved in the order. For example, an order to change the supervision of a line causes different hardware and firmware actions for a line in an intra-RT connection than for a line in an RSS to ESS connection. The RT responds to all data link orders as an intelligent slave and bases its actions on the current line states.

6.1 Remote order buffers

The ROBs are used for sending call-processing orders from the host to the RT. The host call-processing programs will seize an ROB and load it with one or more orders necessary to process a part of a particular call. The contents of this ROB will then be sent over the data link and stored in a corresponding ROB in the RT. Upon completion of the ROB orders, the RT returns acknowledgment messages over the data link to the host ROB. Programs in the host continue processing the call based on the acknowledgment data.

The host has a pool of ROBs used for sending orders to the individual RTs. The ROBs are not dedicated to a particular RT; they can be used to send orders to any RT. However, the number of ROB identifiers available for each RT is limited to the number of ROBs present in the RT. This prevents blockage of ROB data in individual RTs. The average holding time for an ROB is approximately 1 second. The ROB execution within the RT contributes most heavily to this holding time.

6.2 Data structures

Several data structures are required for remote order processing in addition to ROBs. Since the RT is a slave to the host, the primary data structures for call control are resident in the host. Call registers, resource memory, and equipment translators are all maintained in the host for ready access by call control. Data structures that are maintained in the RT are used primarily for maintenance and stand-alone.

Resource memory for the lines, channels, and network are kept in the host and duplicated in the RT. The state of the lines and channels is stored in PMRs and Path Memory Channel words (PMCs), respectively. Network path information is reflected in Path Memory Junctor words (PMJs) and the network map. Busy/idle status of network links is stored in the network map, while path descriptions are stored in the PMJs.

During the execution of remote orders, the RT memory for these resources is kept up to date. This allows the RT maintenance programs, which are independent of the host, to select and use idle resources. During the time the maintenance programs are using resources, the appropriate resource memory is marked diagnostic busy. The only conflict arises if the host chooses to use the same resource that maintenance is using. In this case, the remote order notes the resource conflict and requests maintenance to idle the desired resource. After a time break to allow maintenance to idle the resource, the remote order proceeds. This is an example of the master/slave relationship between the host and the RT.

The resource memory is also necessary for the entry and exit transitions from stand-alone operation. Intra-RT stable calls are maintained during the transitions through preservation of the resource memory. (See Section VII for details.)

Remote order processing also makes use of the resource memory for the metallic access network. However, full administration of this network exists in the RT so that duplicate memory and resource conflicts with the host do not exist. (See Section IV for details.)

The RT equipment translators exist primarily in the host for ready access by call control when forming remote orders. However, a few translators are also maintained at the RT to provide information required during remote order execution. These translators include:

(*i*) Line Remote Equipment Number Translator provides line transmission and ground start information for lines.

(*ii*) Ground Start Applique Translator relates lines to ground start applique circuits.

(*iii*) Remote Miscellaneous Distributor Number Translator provides distributor point information for lines.

(*iv*) Office Parameters are used to specify variable information for the RT such as ringing type and equipage of circuits.

6.3 Remote order buffer execution

Once a ROB has been loaded with orders from the data link, the RT operating system schedules execution of the ROB. The ROB execution program, which deals with the data in the ROB, can be viewed as a three-level structured program. The highest level in the structure is the executive which receives control for an active ROB from the operating system, decodes orders in the ROB, and passes control to the order execution routines. The executive also handles the acknowledgments returned to the host after the ROB orders are completed. The second level is a series of programs which carry out the order execution requested by the executive. To perform the actions requested by the orders, these routines call a third level of programs which are collections of various primitive functions that carry out specific tasks.

The operating system regularly looks for active ROBs that need to begin or continue execution. When a ROB with pending orders is found, the ROB executive begins processing by extracting the first order identifier and decoding it. Assuming a valid order is found, the executive reads the remaining data in the ROB associated with the order and passes it on to the appropriate order execution routine. Upon completion of the order, the order execution routine returns success/fail data to the executive. If the host requested acknowledgment data after the completed order, the executive returns the success/fail data to the host ROB via the data link. The executive then extracts the next order identifier in the remote ROB and repeats the process. The ROB processing continues until all orders in the ROB have been completed.

If an order should fail execution for any reason, the executive will report the failure to the host via an acknowledgment. If the acknowledgment was requested after the failing order, an immediate report is sent. However, if another order follows the failing order, that order and all succeeding orders will be skipped until an acknowledgment request is found. At that point, the failing order data are returned in an acknowledgment to the host and ROB execution terminates.

Another option that can be requested by the host for remote ROB execution is to ignore all failures during order execution. This option is used during failure recovery when the host program idles the RT hardware. Since the state of the hardware may be unknown, failures on some orders are expected. The failures are purposely ignored by always returning success acknowledgments to the host. This option simplifies the host program by eliminating the processing of ROB failure conditions.

After the executive has decoded an order identifier and extracted the data for the order, control is passed to one of many order execution routines. These routines break down the orders into a sequence of primitive functions dealing with specific tasks in firmware and hardware.

For example, the "path" order contains data specifying a set of two Remote Equipment Numbers (RENs), two network A-links, and a junctor which describe a unique network path. Additional data specify a connect or a disconnect operation and the new scan states for the two RENs. To execute this order, the path order execution routine must first translate the logical equipment numbers into peripheral hardware addresses. These addresses are in turn used in specific tasks to perform the network hardware operations. The new status of the network is recorded in the network maps and the PMJs. Similar tasks must be performed for each of the line scan states. Each one of the above functions must be completed to perform the path order. A failure in any function causes the order to fail and a failure return to the ROB executive.

Each ROB order is made up of one or more primitive functions which perform a specific task in either hardware or firmware. Several functions are used in the execution of the path order described above. One of these functions records the new status of the network in the data structures. This is accomplished by writing the path data into the PMJ for the junctor, computing the network links, and writing their new state into the network maps. This is an example of a function that depends on no other condition than the path data passed to it, and the function cannot fail.

Other primitive functions depend on the current state of the hardware. For example, setting a line to the origination scan state causes different actions when the line is in a path to the host than when it is in a path to another RSS line. In the first case, the line's supervisory state is repeated over a channel to the host. In the second case, the line's supervisory state is sent to the host as a data link supervision report. In either case, when the line disconnects, a ROB order will be received at the RT to set the line to the origination scan state. Clearly, the primitive function which handles the scan state change must first determine the old state of the line. The appropriate set of actions can then be taken to realize the desired final scan state. A success/fail return is given to the higher level routine to reflect execution status of the function. In this example, the primitive function is dependent on the line state and may fail.

Many of these primitive functions are called by several of the order execution routines. By placing the line state dependent actions in the primitive functions, the order execution routines do not require knowl-

edge of previous line states. This achieves greater code efficiency and more uniformity in handling specific tasks.

6.4 Peripheral control

Many of the primitive functions called by order execution routines perform peripheral hardware actions. However, not all peripheral circuits operate in the same amount of time. The electronic PNPN network operates at program speed and requires no firmware time breaks. Other circuits, such as the metallic access network, take longer to operate and require the firmware to delay before proceeding with additional orders. Consequently, a provision for time breaks has been included in the primitive functions to handle the slower operation. Higher level order execution routines are unaware of these delays.

Also built into the peripheral control functions is the ability to retry orders. If an order fails, it is first retried on the same microprocessor controller. If the order fails a second time, the microprocessor controllers are switched and the order is retried from the newly on-line controller. Only if this third attempt fails is the peripheral circuit considered faulty and the order aborted. This retry strategy gives the peripheral orders every chance to succeed before a failure is accepted and propagated back to the host through a ROB acknowledgment.

VII. STAND-ALONE SERVICE

The stand-alone feature of the No. 10A RSS RT provides a POTS-type intraoffice service to individual, multiparty, PBX, and coin-type lines. Typically, an RT will be located in an area where there is a community of interest. The feature has been designed to serve this community of interest during periods when both data links to the host fail.

The feature is a Bell operating company (BOC) option and is implemented by equipping the RT with an engineered quantity of special circuit boards which provide the tone digit receivers and tone sources. The stand-alone feature is always resident in the RT firmware.

7.1 Stand-alone features

The stand-alone feature was designed primarily with the CDO application in mind. It provides intraoffice services to lines which are served directly by the RT.

Local emergency service agencies in a community (e.g., fire, police, hospital, etc.) will most likely have several local telephone lines working in a multiline hunt arrangement. To continue to provide an adequate service to these agencies, a basic multiline hunt capability has been included in the stand-alone feature.

A special facility has been incorporated to reroute selected numbers such as "O" operator and "911" to a local line. This rerouting is

accomplished by the Special Directory Number Translator which can translate an "O" first digit, or any 3-digit or 7-digit number to a directory number served by the RT. If the BOC provides an entry in the special number translator to handle "O" calls, the RT can handle manual lines in the stand-alone mode by routing manual line call originations to the special "O" handling.

Coin phones may be either dial-tone-first or coin-first. Intra-RT calls will be completed but any coins deposited will be returned. For multiparty lines, all ringing options are available.

A recorded announcement port has been included on the special stand-alone circuits boards. Provision of a recorded announcement machine is optional for the BOC. Calls destined to numbers not served by the particular RT are routed to the recorded announcement on a "barge-in" basis. If one is not provided, reorder tone is substituted for the recorded announcement.

While running in the stand-alone operating mode, no connect timing is performed on calls and no record is made for charging purposes.

Special features such as call forwarding, abbreviated dialing, call waiting, specialized multiline hunt patterns, etc., are not available.

Counts of traffic activity and of calls which cannot be handled for lack of or malfunctioning of resources are maintained. These counts are sent to the host and displayed on teletypewriters (TTYs) at the time the No. 10A RSS exits from the stand-alone mode.

7.2 Entering and exiting stand-alone

The stand-alone operating mode is entered whenever a duplex data link failure occurs. This may occur as a result of the loss of frame protocol on both data links for a period of 30 seconds or as the result of the loss of the "heart-beat" for a period of about one minute. A heart-beat message on the active data link is the ultimate back-up which controls entry into stand-alone. The RT originates a data link message every 10 seconds and increments a heart-beat counter. The host on receiving this message returns an acknowledgment which, when received at the RT, causes the counter to be zeroed. If this counter gets past 6, (no heart-beat returned for about 1 minute), all call processing in the RT is stopped and the transition into stand-alone is initiated.

When entering stand-alone, all stable intra-RT calls are retained. All other calls are disconnected and the affected lines are placed into the appropriate state (origination or high and wet). Placing off-hook lines into the high and wet state helps to control the number of originations entering the system when stand-alone processing begins.

The entry into stand-alone generates a modified transient clear

which initializes the database and hardware of all transient calls and all calls involving a channel connection to the host. It is possible that the trigger to enter the stand-alone mode may not affect the RT to host channel calls. However, since the stand-alone service circuits share network appearances with the channels, it is essential that channel hardware be idled.

In the unlikely event stand-alone was triggered by other than carrier system failure, the channel idling will ensure that the host ESS will clear all of the related RSS calls. In the event of a normal outage, the host ESS is protected by the Carrier Group Alarm (CGA) conditioning capability of the host channel circuits.

The process to bring the RT out of the stand-alone operating mode is initiated by the host. This may be accomplished manually by the initialization of the data links at the host or automatically under control of host code. The exiting stand-alone process is started by a host-originated message in which the host asks the RT "Are you in Stand-Alone?" If the RT is not in stand-alone, it sends a reply which so advises the host and does nothing.

If the RT is in stand-alone, all call-processing work is suspended and the exiting stand-alone process is executed. As in the case of entering stand-alone, a transient clear is done which again initializes the database and hardware of all transient calls. All lines which are off-hook, including both those involved in transient calls and those giving a permanent signal (high and wet lines) are placed into the originating state. Stable calls remain connected.

When the database and hardware initialization work has been completed, information on stable calls is sent to the host. This information is used by the host to rebuild its database.

Finally, the RT sets up a background task to send the traffic data, which was collected while in stand-alone, to the host for printing on the host's TTY. A message is then sent to the host that says "I am out of stand-alone" and normal host-RT call processing resumes.

In the RT exiting process, lines with permanent signals are placed in the originating state. The host, after resuming control of call processing, will see these lines as call originations. With no activity on the lines, they will be given permanent signal treatment by the host and will eventually be placed into the high and wet state at the host.

7.3 Data structures

During stand-alone call processing the Stand-Alone Buffer (SAB) is the basic data structure and serves as a repository for data which are accumulated while originating or disconnecting a call. Each call origination and each disconnect requires the use of an SAB. On an originat-

ing call, the SAB is idled when the called party answers or if the calling party abandons the call. In many respects its use is similar to that of a call register in other ESS systems.

The ROBS, which are used during host mode operations, are used and redefined as SABS for stand-alone mode. Because of much longer holding times (an average of 30 seconds for an originating call) additional SABS are provided for use only in stand-alone.

While a call is in the dialing stage, a Universal Call Register (UCR) is attached to the SAB and placed on the digit collection linked list. This is a reuse of the UCR from one of its normal host mode functions.

In the RT, office translation information is stored in write-protected memory. Principal translation data structures are as follows:

(*i*) Directory Number (DN) Translator provides the information to translate a called number to the equipment location where the called party's line terminates. This translator also provides ringing information to ring the called party's line.

(*ii*) Special Directory Number (SDN) Translator is used to translate the called special emergency numbers to a DN served by the RT. A first digit of 0, or any 3- or 7-digit number can be entered into this translator (e.g., "0" or "911").

(*iii*) Line Remote Equipment Number (LREN) Translator provides information on the attributes of lines: i.e., major class of service, ground start applique usage, sleeve lead, *TOUCH-TONE** service equipped, member of a multiline hunt group, etc.

(*iv*) Multiline Hunt List contains the LREN number for lines which are members of multiline hunt groups. This list is used in connection with the multiline hunt facility.

(*v*) Remote Miscellaneous Distributor Number (RMDN) translator provides translation information for lines equipped with sleeve leads.

(*vi*) Ground Start Applique (GSA) Translator provides information on GSA equipment assigned to lines.

(*vii*) Office Parameters provide information on office equipment availability, office options, etc.

The LREN translator, GSA translator, and office parameters are used in both the stand-alone and host operating modes. The other translation data structures are used only while in the stand-alone mode.

A full translation update is made automatically by the host over the data link on a scheduled basis, or a special update can be requested manually at any time. To accommodate service order activity, recent changes entered at the host will be updated individually almost immediately at the RT.

Busy/idle maps for the network junctors and A-links are maintained

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in memory. In stand-alone mode, the maps are used to make path assignments to connect a tone to a line or to make a talking path connection. Another busy/idle map in memory maintains the status of stand-alone tone circuit assignments.

7.4 Call setup

A major objective in the design of the stand-alone call processing feature was the maximum reuse of code and functions which were developed for host mode operations. Many ROB execution functions were used "as is," except for a few that required some minor modifications to accommodate both operating modes. Line scanning and ringing functions were also reused along with many hardware control primitives.

Stand-alone call processing is carried out by a number of processes interacting with one another asynchronously and communicating through commonly accessed message areas located in the SAB.

As in the host mode, the Line Scanning process regularly scans the line interfaces for changes in the on-hook/off-hook state of the subscriber lines. When a call origination has been detected, the originating line is posted in the Origination Hopper. The Origination Hopper Unloading function, running at base level, unloads the hopper and, instead of sending a data link message, passes the LREN of the originating line to the directly coupled Originations Interface Routine. The Originations Interface seizes an SAB and spawns a process to handle the originating call.

The RT operating system regularly scans the SABs for newly spawned processes and, when one is found, the Stand-Alone Executive is called. The Executive controls the call through three main phases of the call setup process. In the first phase, the Originating Call Process Initialization, the SAB is initialized, a UCR is attached, the call is placed on the digit collection list, and the originating customer is given dial tone.

The Get Dialed Digits Process, the second phase, runs at base level and works asynchronously with the 10-ms interrupt level Digit Collection Process to receive the dialed digits from the customer, to analyze them, and to determine the equipment location of the called number. Digit analysis is performed after the first, third, and seventh dialed digits. On completion of the second phase, the called line has been checked for busy, line supervision is turned over to line scanning, the call is removed from the digit collection list, and the called line is ready to be rung. The Get Dialed Digits Process, while waiting for receipt of digits from the customer, regularly takes real-time breaks and returns control to the operating system.

The third phase, the Ring Called Line Process, builds the ring order and calls the ROB execution function which handles ring orders. This

function spawns a new process which will actually control the ringing, and the detection of answer on the called line. When the called party answers, the ringing control process posts a flag in the SAB and terminates. The Ring Called Line Process then establishes the talking path between the two customers.

This call is now in a stable state, line supervision has been turned over to line scanning, and the call is completed. The SAB is idled and the Call Setup Process terminates.

The mechanisms for detecting and handling hardware problems in the host operating mode are still active when running in the stand-alone mode. However, with the data links out of service and no way of reporting the problems, these mechanisms are of limited value. Heavy reliance is placed on the hardware and software audits to keep as much of the RT hardware available for use as practical.

To minimize the effect of a defective tone circuit on a stand-alone circuit board the various tones are assigned on a rotating basis. To avoid indefinite tie-up of any one hardware or software resource, time-out facilities have been incorporated throughout the Call Setup Process. If the preset time limits are exceeded, the customer is given appropriate tone treatment and the resource is idled.

7.5 Call disconnects

While a call is in the talking state, line scanning watches both lines for an on-hook condition. When one of the lines goes on-hook and so remains for a period of 1 second (the on-hook is not a hit or a flash), line scanning passes the information to the directly coupled Supervision Interface Routine. The Interface then searches path memory to locate the other party, seizes an SAB, and spawns a Disconnect Process. No distinction is made between the calling and called parties in processing a disconnect.

Line scanning can detect an on-hook from a reverting call disconnect or from a high and wet line going on-hook. In either of these situations, there would not be a second line and a search of path memory would fail. In these cases, the Supervision Interface will still spawn the disconnect process which will perform a "single line disconnect."

The operating system, as in the case of an originating call, finds a newly spawned process and calls the Stand-Alone Executive. The Executive determines that the SAB is for a call disconnect rather than a call origination and then passes control to the Call Disconnect Process.

On receiving control, the Call Disconnect Process first disconnects and idles any network path. For the first or only line involved, any coins which may possibly be still in the coin chute of a coin phone are returned, and the line is conditioned so that it can originate a new call.

If a second line is involved (a line-to-line connection), possible coins are returned on coin lines. A direct check of the second line's line interface is then made to determine its on-hook/off-hook status. If it is on-hook, the line is set up so that it can originate a new call. Should it still be off-hook, the line is placed into the high and wet state.

This completes processing of the call disconnect, the SAB is idled, control is returned to the Stand-Alone Executive and then to the operating system. The disconnection process then terminates.

When the second line which possibly was placed high and wet later goes on-hook, another disconnect process will be spawned. The Call Disconnect Process will then be concerned with only a single line and appropriate action will restore the line to the originating state.

VIII. SUMMARY

There is a growing trend to incorporate distributed processing in telephone switching systems. The No. 10A RSS is in the forefront of this trend and is part of a system consisting of a host ESS connected to one or more remote terminals (RTs). The host ESS and its associated RTs have a master/slave relationship via direct processor-to-processor communication over a data link. The RT is effectively an extension of the host ESS allowing it to now provide service for customers many miles away. This arrangement can increase substantially the range and utilization of an existing host ESS.

The RT processing power is supplied by the *BELLMAC*-8 microprocessor. One unique architectural feature of this microprocessor is the absence of on-chip general registers. All such temporary variables are located on two stacks in memory referenced by the rp and sp. This feature makes the context switching required when calling subroutines, handling interrupts, or switching processes very efficient since no data movement is necessary other than changing two pointers. These kinds of context switching occur very frequently in the RT firmware design.

Most of the RT firmware is coded in the high-level language C. The RT tasks performed are controlled by a process-oriented operating system in which each process descriptor contains its own stacks. The dedicated stacks keep time breaks from having a detrimental effect on the program structure of a process. The number of bytes of RT firmware code exceeded the 16-bit addressing capability of the *BELLMAC*-8 microprocessor so a memory bank switching scheme was incorporated into the RT design. Bank switching was hidden from process execution by traps to the operating system supplied by the overlay link-editor.

Ringing and other high-power signals are supplied in the RT from a general-purpose circuit termed a Universal Service Circuit (USC). A sizable portion of the RT firmware is devoted to the complex control

required by these USCs and their metallic access to customer lines. The most notable aspect of this USC control firmware is that one USC can be used to ring up to three phones via a time-sharing arrangement.

The RT firmware is responsible for periodically scanning lines and reporting any change in supervisory state to the host. If the line is connected to a channel, the supervisory state must be written to the channel because the solid state voice network will not pass dc signals. This has to be done as often as every 10 ms, while the line is in the dialing state, to properly pass dial pulses. If the line is not connected to a channel, supervisory information is passed over the data link. In these cases, the RT also performs any hit timing or flash timing necessary.

The RT is not call-oriented since total call control resides in the host. Instead, the RT focuses on executing orders sent by the host over the data link in ROBs. Several ROB execution processes can be active at any one time. If data link communication with the host fails, however, the RT enters a call oriented stand-alone mode of operation to provide customers with a POTS-type intra-RT service. In this mode, the ROBs are redefined as SABs and increased in number to support the increased holding time of their new call-oriented usage. One important aspect of the transitions into and out of stand-alone is that they have been designed to preserve all stable intra-RT calls.

IX. ACKNOWLEDGMENTS

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No. 10A Remote Switching System:

System Maintenance

By F. H. KEEVE, J. C. MARTIN, and T. L. McROBERTS

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The 10A Remote Switching System (RSS) is unlike previous electronic switching systems in that its various subsystems can be physically separated by hundreds of miles. Thus, its maintenance plan must make provisions for the day-to-day operation and repair of the separate system components by different Bell operating company craft forces. The maintenance of each of the RSS subsystems is described in this article, as well as the required overall coordination between the various craft forces charged with RSS maintenance.

I. INTRODUCTION

1.1 Maintenance objectives

Overall system requirements and objectives for the 10A Remote Switching System (RSS) are detailed in Ref. 1. From a maintenance standpoint, the objective is to provide continuous and reliable telephone service throughout the life of the system, while providing maintenance capabilities equivalent to those of other ESS systems. That is, the system must be both highly dependable and easily maintainable. The maintainability objective is to have a system in which troubles, when they occur, are easily located and sectionalized, and repair operations can be completed quickly by craft without extensive training in RSS. It is a further objective that the RSS maintenance plan be as consistent as possible with existing Bell operating company procedures for maintaining switching systems and fit the organizational structures and maintenance support systems expected to exist in the 1980s.

1.2 Overview

The No. 10A RSS maintenance plan is similar to that of other Bell System electronic switching systems in its reliance upon hardware duplication of critical system components and its use of program control for fault detection, recovery, and support of repair operations. The RSS is unique, however, in that its various subsystems can be physically separated by up to 280 miles,[2] and the maintenance plan must make provisions for the day-to-day operation and repair of separate parts of the system by different craft forces. For this reason, proper maintenance of the RSS will require considerably more coordination among various Bell operating company maintenance forces than earlier electronic switching systems.

A block diagram of the RSS is shown in Fig. 1. The three major components are

(*i*) The RSS remote terminal.

(*ii*) The data links and interconnecting channel facilities.

(*iii*) The controlling host ESS.

All of the communication (both voice and data) from the remote unit terminates on the host office, which supplies much of the overall control for the system. The communication between the remote terminal and the host ESS is over duplicated data links, controlled at the host by the Peripheral Unit Controller configured in the Data Link application (PUC/DL). The voice channels from the remote terminal connect to the host line network and, thus, present some characteristics of both lines and trunks. Detailed discussions of the software and hardware characteristics of the various RSS components are included in Refs. 1 to 7.

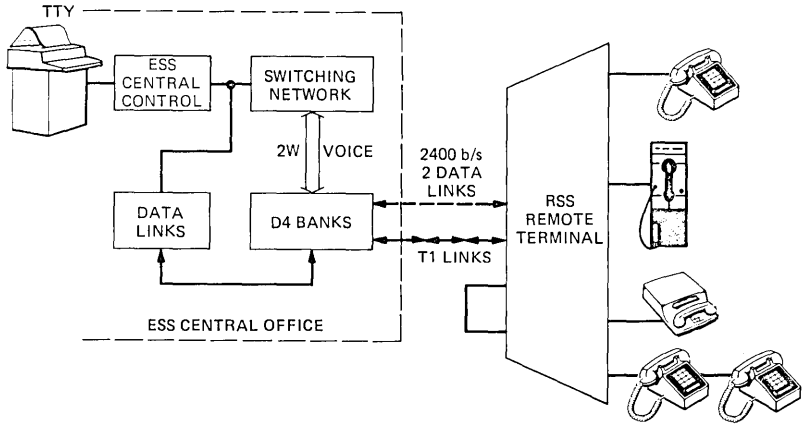


Fig. 1—Remote switching system block diagram (T carrier).

A maintenance plan for the RSS must include all of these separable subsystems and their interactions. In general, existing host maintenance procedures have been extended to include the maintenance of components of the RSS closely tied to the host ESS. Thus, the channels interconnecting the host and the remote terminal are treated, from a maintenance standpoint, much like interoffice voice trunks connected to the ESS. The PUC/DL is treated like any other piece of ESS periphery and is maintained similarly.

On the other hand, the remote terminal itself, where the hardware is distinctly separate from that of the host, is maintained, as much as possible, as a separate entity. The host maintenance teletypewriter (TTY) is the primary interface for remote terminal maintenance, but all remote terminal fault detection, diagnostic control, system state control, etc., are coordinated by the microprocessor controller at the remote terminal. In this way, most maintenance procedures for the RSS remote terminal can be kept independent of the host type (No. 1, 1A, or 2B ESS). The specific host-dependent maintenance capabilities described in this article refer to No. 1/1A ESS.

The RSS per-line circuitry is quite complex because of space, power, and network considerations,[4] while the host ESS per-line circuitry is relatively simple. Extensive loop maintenance functions, such as local test desk access and Automatic Line Insulation Tests (ALIT) exist in the host, but there are no line circuit maintenance functions applicable to the RSS per-line hardware. Host software has been modified to supervise ALIT testing, and to control line test access in the RSS. Software has been implemented in the remote terminal to provide the required per-line circuitry maintenance functions.

Section II of this paper describes the operational relationships necessary to efficiently maintain the RSS. Remote terminal maintenance is discussed in Section III, and PUC/DL maintenance is outlined in Section IV. Section V reviews the approach to RSS channel maintenance, and customer line maintenance is discussed in Section VI.

II. DIVISION OF MAINTENANCE RESPONSIBILITIES

2.1 Overall maintenance coordination

The primary responsibility for the maintenance of the RSS lies with the switching force responsible for the maintenance of the host ESS. The RSS sites are unstaffed, with all TTY messages from the various RSSs appearing on the host maintenance TTY. All alarms associated with the RSS trigger host central office audible alarms and light alarm indicators on the host Master Control Center (MCC). The sectionalization of troubles often requires detailed host office expertise because of the complex interrelationship between the host and the RSS.

The ESS switching maintenance force may be located either in the host central office or in the Switching Control Center (SCC). When the host is maintained from an SCC, the SCC is the ideal point to centralize the overall maintenance responsibility for the RSS. The SCC is normally responsible for the operation and maintenance of all ESS central office equipment within a geographic area, and its responsibility would normally extend to any RSSs served by host ESS offices in that area.

The SCC is responsible for continuous surveillance and trouble sectionalization for the RSS. Since SCC personnel would normally monitor all TTY printout and host alarms, they are responsible for sectionalizing and isolating all machine-generated trouble reports. When a fault is found in the host ESS equipment, the PUC/DL, or the RSS remote terminal, the SCC maintenance force is directly responsible for its repair. In some cases, the SCC will have direct repair responsibility for other portions of the system. In some Bell operating companies, the SCC is responsible for the maintenance of central office carrier equipment. When this is the case, SCC craft will normally be responsible for the maintenance of any host office located channel carrier equipment. In all other cases of RSS troubles, it is the responsibility of the SCC to refer other troubles (e.g., customer loop problems, carrier facility troubles, or data link modem difficulties) to the appropriate maintenance force for follow-up repair. The SCC is also responsible for tracking all RSS repair activities, independent of the specific maintenance force responsible for the repair.

2.2 Remote terminal maintenance

The repair and maintenance of the RSS remote terminal will normally be carried out by ESS switching craft dispatched from the host central office or from the SCC. In some cases, however, because of long travel times or other local problems, it may be expedient to train other available maintenance personnel in simple RSS repair procedures. In these cases, the repair operations will be performed under the direction of switching craft, either at the host or at the SCC.

2.3 Data link maintenance

All PUC/DL faults are reported on the host maintenance TTY and are treated in the same manner as a fault in any other piece of ESS periphery. After the trouble is sectionalized and isolated, the host switching craft will be responsible for the repair. If the fault is found to lie within the data sets, the trouble will be referred to the appropriate force (normally either data services or carrier repair forces) for repair. If the fault is found to lie within the carrier facilities, those normally responsible for carrier maintenance and repair will be called.

2.4 Channel maintenance

The maintenance of the voice channels between the RSS remote terminal and the host ESS is the responsibility of the same force responsible for the maintenance of the host office trunks. This function will be performed at the host trunk test panel or at the trunk maintenance work station at the SCC. This force will be responsible for monitoring the weekly scheduled automatic channel diagnostics, and providing ongoing surveillance of the maintenance TTY output in order to react to channels automatically removed from service by system-error analysis. When RSS channel troubles are detected, it is the responsibility of this force to sectionalize the trouble to either host central office equipment, host carrier equipment, carrier facilities, or remote terminal equipment. Once the fault is isolated to one of these areas, the trunk maintenance force is charged with either repairing the trouble, or referring the problem to the appropriate maintenance group.

When the host trunks are included in a Centralized Automatic Reporting On Trunk (CAROT) center, the RSS channels will normally also be included. Then, the CAROT center will routinely perform transmission measurements on the RSS channels.

2.5 Carrier equipment maintenance

The carrier equipment between the host ESS and the RSS remote terminal is the maintenance responsibility of the Bell operating company force normally charged with carrier maintenance. The switching craft responsible for the host will normally receive the first indication of carrier trouble via TTY printouts and audible alarms. The problem will then be sectionalized further to determine which specific force should carry out the repair. Trouble could lie within the RSS remote terminal frame, within the host ESS carrier equipment, or within the carrier facilities in the outside plant. In the case of T-carrier, particularly, coordination greater than the norm will often be required between the switching craft and the force responsible for carrier maintenance, because the T-carrier equipment at the remote terminal is integrated into the RSS equipment frame. When the switching craft has isolated the carrier problem to the facilities, the trouble would normally be reported to the Facility Operation Center of the T-carrier Restoration Control Center (TRCC) for repair and service restoral.

2.6 Customer loop maintenance

The responsibility for the maintenance of the customer outside plant and station equipment remains with the appropriate maintenance center. In the following, such a maintenance center will be referred to generically as a Repair Service Bureau (RSB). In the future, RSB functions may be split among several other maintenance centers.

The ability to test an RSS customer loop from the local test desk is provided either via a metallic test connection or through a modified remote test system. As with other systems, most customer complaints will be reported directly to the RSB, and it will be their responsibility to sectionalize the problem as either "in" the switching equipment or "out" in the outside plant. If the problem is found to be in the switching equipment, it is the responsibility of the RSB to notify the switching craft for further fault resolution and repair. Customer drop line, terminal equipment, and loop plant problems will be repaired by the appropriate maintenance force.

Customer loop problems that are detected by the RSS will result in TTY output messages that print on the local test desk TTY channel. It will be the responsibility of the RSB maintenance force to react to these trouble reports, sectionalize the problem to either "in" or "out" and either repair the "out" problem or alert the switching craft to problems within the RSS equipment.

III. REMOTE TERMINAL MAINTENANCE

3.1 System overview

The RSS microprocessor controller generally operates under the control of the host ESS processor. In the case of call processing, the degree of host control is large.[5] However, remote terminal maintenance activities are carried out nearly autonomously, with the host ESS acting primarily as a TTY input/output coordinator. Remote terminal hardware fault detection, error analysis, alarm scanning, and processor configuration are performed by the remote terminal microprocessor. The RSS hardware diagnostics are also resident at the remote terminal. The host exercises automatic control over remote terminal hardware diagnostics only for interface circuitry, such as channel interface hardware and data link hardware.

The desired degree of remote terminal reliability is accomplished through hardware duplication of circuitry that affects more than 64 customer lines. To ensure that no single fault will affect more than 64 lines, the RSS microprocessor controller and the data link connecting the remote terminal to the host are duplicated. A block diagram illustrating this duplication is shown in Fig. 2. A complete RSS controller consists of the microprocessor itself, along with its dedicated memory and a dedicated set of fanout boards through which the periphery is accessed. Each microprocessor controller can communicate over either data link. The host determines which data link is active, and the remote terminal decides which microprocessor controller is active.

The remote terminal microprocessor controllers have four allowable states: active, standby, out-of-service, and unavailable. In the normal

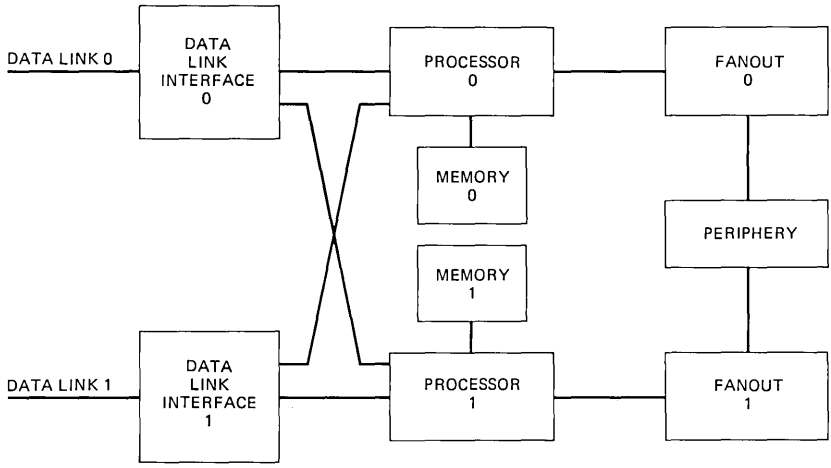


Fig. 2—Remote switching system terminal—system control.

working mode, one processor side is active with the other standby. In this mode, there is no matching between the two sides, but the standby memory is placed in a double-write mode, allowing the active processor to write into both the on-line and off-line memories simultaneously. Thus, if a fault is detected in the on-line controller, a switch can quickly be made to the standby side whose memory has been kept up to date. Any data mutilation caused by the fault will be cleaned up by initialization and audit routines after the switch.

If the off-line microprocessor complex is suspected of being faulty, or its memory is not being kept up to date, it is placed in the out-of-service state. When the off-line microprocessor is marked out-of-service, it is still available for a switch to the active state if a severe fault is detected in the on-line controller. The off-line processor is made unavailable, and a processor switch inhibited, if it has been manually forced off-line or if it has had its power removed. The RSS control complex is discussed in detail in Ref. 3.

Peripheral circuitry, such as the network links and junctors, the various service circuits, and the voice channels between the host and the remote terminal, are replicated.[4] If a malfunction occurs in one of these circuits, the faulty component is identified and removed from service. Generally, there is a sufficient number of remaining circuits to adequately handle the normal traffic with little or no degradation of service.

The primary maintenance interface with the RSS remote terminal is via the host ESS maintenance TTY. Direct TTY communication with the remote microprocessor control system is not possible. A maintenance panel is provided for on-site interaction with the remote terminal, but

its primary function is to allow for circuit-pack replacement and repair verification. The capability is provided to verify a failing circuit, remove it from service, remove power from the circuit pack if necessary, replace the pack, and then verify the replacement's correct operation. A software buffer associated with the maintenance panel must be preloaded, via the host TTY, with a list of circuit packs to be diagnosed on site.

During installation and periods when extensive repair activity is necessary at the remote site, remote access to the host maintenance TTY facility is possible. This access will generally be provided via a secure dial up connection to the SCC serving the host ESS. In this case, it is recommended that a voice-grade facility, independent of the RSS equipment, be provided. It is also possible to provide access to the host remote maintenance TTY on a direct, dedicated-facility basis.

3.2 Remote terminal fault detection

The RSS remote terminal maintenance programs detect and recover from a fault, reconfigure the system if necessary, and report pertinent information concerning the fault in a TTY output message at the host.[3,6] Normally, the message will identify the specific circuit in which the fault occurred. The detection of a fault does not automatically initiate a diagnostic of the remote terminal hardware. It is necessary for the craft person to use manual diagnostics to verify and repair the faulty circuit.

Both hardware and software checks are used to detect faults in the RSS remote terminal microprocessor controller complex.[4] There is a hardware sanity timer associated with each microprocessor. If the timer is not periodically reset, a timeout occurs, causing the associated microprocessor to begin executing code to initialize itself and establish a working mode. Repeated timeouts result in more severe initialization levels. In addition, hardware exists to detect parity errors when accessing the memory and fanout boards.

Software fault detection is performed by a set of sanity tests that are repeated approximately every 10 seconds. These tests are designed to fail when the control complex is functioning improperly.

A software check routine verifies the ability of the processors to access the RSS periphery. Peripheral faults are also detected by a number of tests each time the peripheral equipment is used. These include tests for network continuity, tests for proper operation of the logic on the line interface boards, and, on terminating calls, tests of the universal service circuit output voltage levels and logic operation. On terminating calls, proper operation of the high voltage metallic access circuitry is verified, and the ringing current on the customer loop is measured. The failure of any of these tests results in a report

to the error analysis programs. The operation of these programs is discussed in Section 3.4.

A number of tests of RSS remote terminal hardware are scheduled on a routine basis. These include a daily diagnosis of the off-line data link (discussed further in Section IV), weekly scheduled diagnostics of the voice channels between the host and the remote terminal (discussed in Section V), and periodical automatic line insulation tests (see Section VI). Remote terminal hardware diagnostics are automatically run once a day. The off-line microprocessor controller is diagnosed and switched on-line daily, and all of the peripheral hardware is diagnosed at least once every four days.

Hardware problems in the remote terminal permanent memory are detected by a memory audit that periodically examines every memory location. Data parity is checked, and the on-line and off-line data are compared. If a fault is detected, the appropriate controller is removed from service.

3.3 Fault recovery and reconfiguration

If a fault is detected in the active microprocessor controller in the RSS remote terminal, an attempt is made to automatically recover and, if necessary, to switch sides to reach a working hardware configuration. The control of this recovery action normally lies with the active processor. If it becomes too insane to initiate a switch, the sanity timer for the off-line processor will time out and initiate a recovery.[3]

Several levels of initialization are available, ranging in severity from a simple restart of the base level program cycle to a complete initialization of all data bases and a reset of all peripheral hardware. Repeated occurrences of faults will cause an automatic escalation of the initialization level up to the point where transient telephone calls are cleared. A complete initialization (which includes clearing stable calls) can normally only be requested manually.

The different initialization levels and their associated recovery actions are:

1. A Level 1 recovery requests any active background task to abort. Program execution is restarted at the beginning of the base level cycle. This level is normally the first action taken if a processor or memory fault is detected.
2. In Level 2, a minimal amount of call store is cleared, any active background task is aborted, and the processors are switched, if possible. An out-of-service processor can be switched on-line unless a switch has been inhibited by TTY request.
3. In Level 3, a minimal amount of call store is cleared, and a set of emergency audits are run. On their completion, the program cycle is restarted.
4. Initialization Level 4 clears all telephone calls in the transient

state and idles their associated peripheral hardware. Any call store memory that is not up to date is copied from the off-line side. The translation checksum is examined, and if it is not correct, a complete translation update from the host is performed. Level 4 is normally the highest automatic initialization level allowed.

5. In Level 5, all call store is cleared, except for a special "never cleared" area containing the data link buffers, traffic counts, and post-mortem information concerning the ongoing recovery action. The periphery is completely idled, and all in-progress telephone calls are lost. The translation checksum is examined, and if found to be incorrect, a complete translation update from the host is performed.

6. All clearing actions of Level 5 are executed in Level 6. The translations are unconditionally updated from the host, and the on-line/off-line roles of the processors are switched, if possible. This initialization level is entered only via a TTY request or a manual request from the reset button on the RSS frame.

When an RSS remote terminal initialization takes place, the maintenance forces at the host and at the SCC are notified via an alarmed TTY output message. This message indicates which microprocessor controller was on-line both before and after the initialization, the level of initialization, and the program address where the recovery occurred. The reason for the recovery action is also given. The reasons include various parity check errors, a sanity timer timeout, an attempt to write into write-protected memory, a request to execute an invalid program instruction, and an attempt to access an invalid peripheral address.

After a few minutes, when it is clear that further recovery action is not going to occur, a "post mortem" message is printed, giving detailed information relative to the recovery. Information is printed about both the first initialization in the current series, and from the most recent initialization. Normally, the initialization process is carried to completion by the RSS remote terminal programs, and no craft intervention is required. If the controller gets in a state where it is continually initializing itself, a manually requested Level 6 initialization may become necessary.

When the periodically executed processor sanity tests fail, the recovery mechanism differs from the multilevel initialization process just described. The failure of one of these tests normally indicates a hardware fault in the on-line microprocessor controller, and the recovery consists of an attempt to switch to the standby side. If the off-line controller is marked out of service, it may or may not be switched on-line, depending on the severity of the fault and its potential effect on the system. If a processor switch is not completed, the original controller remains active, with the processor marked faulty. In this state, the discovery of new processor faults will not be reported via TTY output, unless they are severe enough to cause a processor switch.

Memory faults discovered by the memory audits also result in a processor switch, if possible. A switch will not take place if the off-line controller is out of service.

As with sanity test failures, peripheral faults are also handled outside the multilevel initialization procedure, since they normally result from peripheral hardware problems. If a fault is detected while attempting to execute a peripheral order, one of three problems is assumed to exist. The fanout board involved could be faulty, the particular peripheral hardware being accessed could be faulty, or a transient hardware failure could have occurred in either the fanout board or the periphery.

When a peripheral order fails, it is first retried without altering the system state. If the retry succeeds, a transient hardware fault is assumed and a transient error counter for the on-line side is incremented. If the number of transient errors exceeds a threshold, the system will switch sides, if possible.

If the peripheral order retry fails, the system attempts to switch sides. The peripheral order is then retried from the new controller complex. If it succeeds, the original fanout board is assumed faulty. The off-line controller is then removed from service, with that particular fanout marked bad. If the peripheral order fails on the new side, a peripheral hardware failure is indicated. The now off-line microprocessor controller is left in the standby state, and the faulty portion of the periphery is marked bad so further access problems with the suspected hardware will not result in a processor switch or TTY output.

When two successive peripheral orders fail and a processor controller switch is not allowed, it is not possible for the system to differentiate between fanout and peripheral hardware faults. In this case, the on-line fanout board involved is marked faulty.

3.4 Error analysis and peripheral circuit disposition

When a fault is detected in the peripheral hardware, either through the mechanism described in the previous section or the various per-call tests, the hardware involved is reported to the RSS error analysis programs located in the remote terminal. The circuits analyzed by these programs include network A-links and junctors, Receiver Off-Hook (ROH) tone circuits, metallic access buses, and Universal Service Circuits (USCs). Channels and lines receive modified treatment, as described in Sections V and VI, respectively.

The error analysis programs make use of two techniques for analyzing and pinpointing faulty hardware—peer group analysis and quick check. A peer group analysis program compares the error rate of a particular member of a group of circuits to the error rate of the entire group. The circuits are compared on the basis of a particular error type, and any circuitry that shows a high rate of failure relative to the

other members of the group is reported to the circuit disposition programs for possible removal from service.

The second technique used for peripheral hardware error analysis is a success/fail comparison called quick check. The quick check program looks for three successive failures from the same circuit. When a particular circuit fails three times in a row, an attempt is made to automatically remove it from service.

When a per-call failure is detected by either the peer analysis or quick check technique, a TTY output message is generated. This message details the particular circuit which failed and the failure type.

The circuit disposition program, located primarily in the host, is responsible for acting on requests to remove or restore peripheral circuits to and from service. Removal requests can be automatically generated by the error analysis programs as just outlined, or they can be the result of a manual request from the RSS maintenance panel or from the host maintenance TTY. Restoral to service requests can only be made manually.

When a request is received to remove a circuit from service, it may be removed immediately, the request may be denied, or, if the circuit is busy, it may be camped on and removed when it becomes idle. A removal request can be denied if a predefined out-of-service limit has been reached. In this case, a manual request can be made from the TTY to override this limit and unconditionally remove the circuit from service. The camp-on mechanism will not monitor the circuit indefinitely. After a period of time, the program will time out, and it will be necessary to re-request the circuit removal.

In all cases, the action taken by the circuit disposition programs is reported to the craft by host maintenance TTY output messages. The success or failure of a removal or restoral request is indicated. If a removal request failed, the reason for failure is specified. When an automatic request from error analysis results in the removal of a circuit from service, the error type or types is specified, and the reason for removal, either peer analysis or quick check, is given.

The circuit disposition program also formats and outputs information about the status of RSS remote terminal peripheral hardware. Out-of-service lists for network A-links and junctors, metallic access buses, and USCs are output by this program. The current state of any individual line can also be determined and printed via the circuit disposition program.

3.5 RSS remote terminal diagnostics and fault repair

In the RSS remote terminal the circuit pack is generally the smallest replaceable entity. For this reason, the diagnostics for the remote terminal hardware are designed on a per-circuit-pack basis. Each diagnostic tests a complete circuit pack, which often contains many

individual circuits. For example, the line interface board contains line access circuitry for eight lines, the first stage of the switching network for these lines, and the metallic interface network between the customer loop and the USC which supplies high voltage control, such as ringing and coin control.

The primary requirement for the design of these diagnostics is testing completeness rather than fault resolution. Thus, the diagnostics are designed to determine which portion of the system (to the circuit pack level) contains a fault, not which specific circuit is faulty. In most cases, a failing diagnostic pinpoints the faulty board, or at most a few suspected faulty boards.

The TTY output message associated with a diagnostic failure will usually include enough information to either determine the faulty board or suggest further diagnostics that should be run. If a more detailed analysis of the failure is necessary, the output message will contain raw data that, when used in conjunction with the diagnostic program listings, will enable this examination to be done.

All diagnostics can be requested manually from the maintenance TTY. The microprocessor controller diagnostics are automatically run daily, and all peripheral hardware is routinely diagnosed on a 4-day cycle. Except for the channel and data link diagnostics, discussed later in this paper, RSS remote terminal diagnostics are not run automatically as the result of a detected failure. Also, a failing diagnostic will not remove circuitry from service because of the lack of failure resolution to the circuit level.

The RSS processor, memory, and fanout diagnostics run on the off-line controller only, but diagnostics for the peripheral circuitry will run whether the equipment is in service or out-of-service. If a diagnostic is run on a circuit pack containing traffic busy circuitry, the tests for that portion of the board are skipped. Thus, there are three possible results for a peripheral circuit-pack diagnostic. It can pass all tests, it can fail some tests, or it can pass every test run, with some tests skipped. Each of these cases is detailed with a TTY output message, with an indication of the number of skipped orders when all tests were not run.

The diagnostics can be run in one of three modes. In the normal mode, the diagnostic is run only to the point where a failure is detected. At that point, the diagnostic is terminated and the failure is reported. The daily routine diagnostics are run in this mode. An unconditional mode exists for cases where the fault resolution of the normal mode is inadequate. In this mode, every diagnostic test is run and every failure is reported. The third diagnostic mode is the repeat mode. The diagnostic, or a portion of the diagnostic, is repeated continually until manually aborted. In this mode, the result of the first run through the diagnostic, either pass or fail, is reported. On subsequent runs, only changes in diagnostic results are reported. This mode is useful when

an intermittent failure exists, or when it becomes necessary to use external test equipment to monitor the operation of a portion of the RSS circuitry.

In addition to using the diagnostics for fault detection, they are also useful for fault isolation. In some cases, a diagnostic failure implicates only one circuit pack, but in other cases, the failing diagnostic will implicate other boards. By diagnosing these circuit packs, the particular board that is faulty can usually be identified. In some cases, it may be necessary to use the information in the diagnostic program listings for a description of the test situation and a detailed analysis, using the raw data contained in the diagnostic failure message.

When a fault has been isolated to one or a few suspected faulty boards, a craft person must be dispatched to repair the problem. The RSS maintenance panel is the normal field interface between the system and the craft. Identification numbers of the suspected faulty boards must be preloaded in the maintenance panel repair buffer from the host maintenance TTY. In the field, the craft person can then use the panel to sequentially examine each circuit pack. First, the board is removed from service and diagnosed. If it fails, it is replaced and rediagnosed for repair verification. If it passes, the pack is restored to service. If the diagnostic continues to fail, the fault probably lies on one of the other suspected faulty packs. In this case, the original board can be replaced, and the second suspected circuit pack investigated. This procedure is repeated until every circuit pack stored in the maintenance panel repair buffer passes its diagnostic.

IV. PERIPHERAL UNIT CONTROLLER/DATA LINK MAINTENANCE

4.1 Peripheral hardware

A Peripheral Unit Controller (PUC) is a microprocessor-based, intelligent No. 1/1A ESS peripheral. It communicates with the No. 1/1A ESS through the peripheral unit bus, the scanner answer bus, a central pulse distributor, and a master scanner (see Fig. 3).

Since the PUC is a general-purpose controller used in No. 1/1A ESS for such features as Digital Carrier Trunk, and Electronic Tandem Switching, as well as the Remote Switching System, PUC maintenance considerations will not be specifically discussed. The RSS requires a PUC data link (PUC/DL); that is, a PUC with additional hardware and an additional firmware package that allows it to provide an interface with up to 16 data links. Because of the dependence of RSS on its data links, the PUC/DL maintenance considerations will be discussed. Other aspects of RSS data link operation are covered in Refs. 3, 5, and 6.

Since an RSS can serve up to 2000 customers, its communication link to the host is duplicated for reliability. The two links are operated in an active-standby configuration at a 2400-b/s data rate using the CCITT

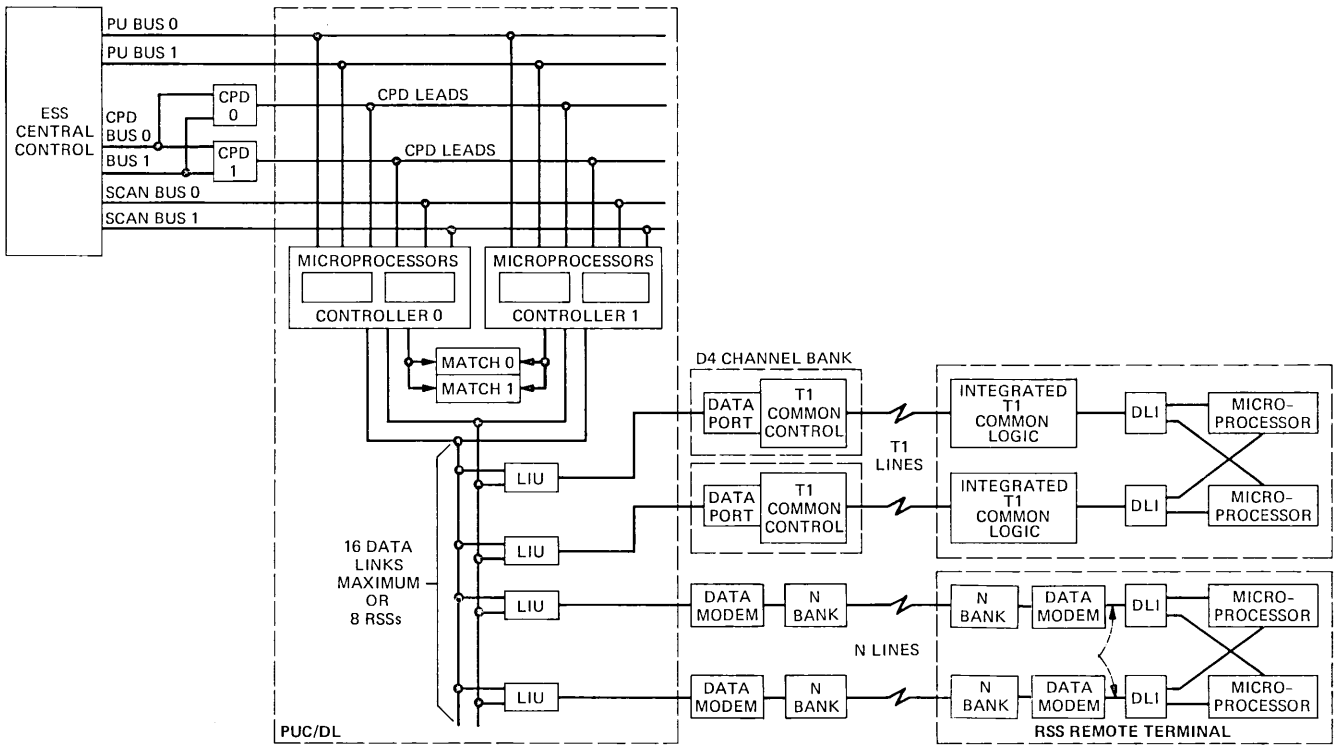


Fig. 3—Remote switching system data links.

X.25 link-level protocol. A PUC/DL frame can support up to eight RSSs. Each link connects the host to the Remote Terminal via either T1 or N-carrier. If T1 carrier is used, the link consists of the following:

(*i*) Line Interface Unit (LIU) in the PUC.
(*ii*) Special D4 channel bank data port plug-in.
(*iii*) Standard interface between the LIU and the data port.
(*iv*) T1 voice channel.
(*v*) Data Link Interface (DLI) board in the RT.

If N-carrier is used the link consists of the following:

(*i*) Line Interface Unit in the PUC.
(*ii*) Standard 2400-baud, full-duplex data set.
(*iii*) Standard interface between the LIU and the data set.
(*iv*) N-carrier voice channel.
(*v*) Matching data set at the RT.
(*vi*) Data Link Interface board.
(*vii*) Standard interface between the modem and the DLI.

It is the task of PUC/DL maintenance to detect link-affecting problems in any of these components, reconfigure appropriately, and to provide diagnostic resolution sufficient to sectionalize the problem.

4.2 Data link trouble detection and recovery

Trouble in the data link can be detected by the host[3] or the remote terminal[3,6] when a carrier failure, a protocol response failure, or an excessive error rate is encountered. When the remote terminal detects a problem before the host, it simply stops responding to the received data, causing the host to detect a protocol response failure. In any case, the host attempts to establish a working configuration using the standby link. The faulty link is then diagnosed and reported to the craft person by a host TTY message. If both links to the RSS are faulty, the remote terminal will go into a stand-alone mode. Host recovery programs continue to periodically diagnose the links and will automatically bring the data links back on-line when the trouble clears.

Faults requiring manual intervention require additional software tools. The TTY messages are provided to request the data link status, restore a data link to service, remove an active link from service, and diagnose a data link. In rare cases, TTY messages can be used to force a link active or detain a link out-of-service; thus, overriding the system checks and forcing the system to use or not use a specified link.

4.3 Data link diagnostic

A data link diagnostic can be requested manually or automatically. It is composed of seven phases which test the various sections of the data link by looping signals at different interfaces, applying enough load to stress the system, and observing the results (see Fig. 4). The

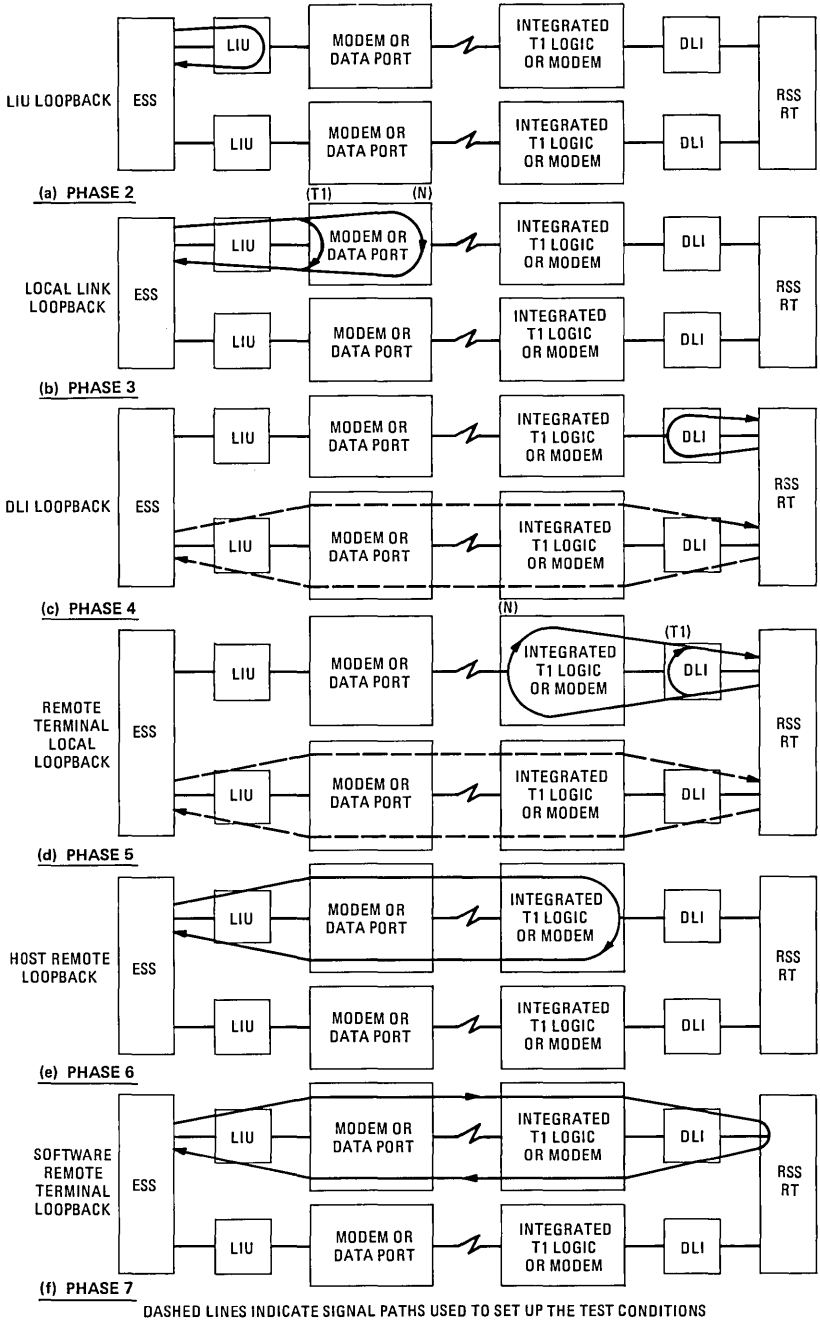


Fig. 4—Data link loop tests.

diagnostic can print in the normal or raw data modes. It can run all phases, begin and end at a specific phase, or loop on a particular phase. Phase 1 tests host access to the LIU. Phase 2 loops the host signal at the LIU. Phase 3 loops the host signal at the host modem or data port. Phases 4 and 5 consist of tests run at the RT. Phase 4 verifies proper operation of the DLI board and performs a local loopback from the remote terminal controller to the DLI. Phase 5 remotely loops the signal at the remote terminal T1 interface or modem, depending on the facility. Phase 6 is a hardware end-to-end loop consisting of 1000 frames of data; fewer than 10 errors is considered as an All-Tests-Pass (ATP), fewer than 100 errors is characterized as a degraded link, and more than 100 errors is considered a failure. Phase 7 attempts end-to-end communication by sending a message to the remote terminal controller, and waiting for a response. This phase fails if a response is not obtained within a reasonable period of time.

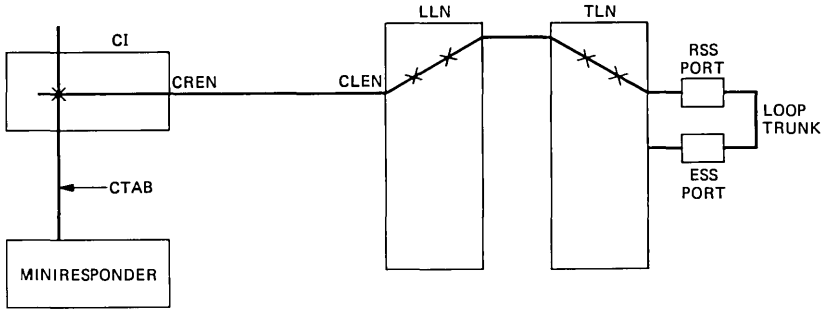
V. REMOTE SWITCHING SYSTEM CHANNEL MAINTENANCE

5.1 Channel maintenance overview

A channel is a Special Service Circuit, similar to a voice trunk, connecting the RT to a line appearance on the host No. 1/1A ESS. A channel looks like a line to call processing programs, enabling most No. 1/1A ESS line features to be readily available to any RSS customer when connected to a channel. In the areas of maintenance and traffic usage, however, channels more closely resemble trunks. With a traffic usage of up to 25 CCS/channel, a faulty channel can potentially affect many customers; therefore, weekly diagnostics, per-call-failure tests, error analysis, and manual access arrangements are required to maintain them adequately.

At least a part of every normal RSS call involves a link from the RSS to the ESS consisting of an RSS line circuit, an RSS network connection, and an RSS channel. Since this link did not exist when the Direct Distance Dialing (DDD) transmission allocation plan was developed, it was not given any loss allocation. This link must then have a nominal 0-db loss characteristic. This requirement led to the transmission plan detailed in Ref. 2. This plan requires tight control of the channel transmission characteristics. Automated monitoring of RSS channel transmission performance is provided by the Centralized Automatic Reporting On Trunks (CAROT) system.

Since the RSS is simply a remote extension of the host ESS, the maintenance of both ends of the channel becomes the natural responsibility of the host. This allows the automatic testing of channels to be superior to that provided for most trunks.



CI CHANNEL INTERFACE
CLEN CHANNEL LINE EQUIPMENT NUMBER
CREN CHANNEL REMOTE EQUIPMENT NUMBER
CTAB CHANNEL TEST ACCESS BUS
LLN LINE LINK NETWORK
TLN TRUNK LINK NETWORK

Fig. 5—Remote switching system channel maintenance terminology.

5.2 Design approach

Because of the similarity between channels and trunks, the possibility of using the existing No. 1/1A ESS trunk maintenance programs was appealing. Connecting the host line appearance of an RSS channel to one port of a loop-around trunk allows the unconnected port (and, therefore, the channel) to be treated like a trunk (see Fig. 5). Two criteria were considered vital in the implementation of the design. The first: minimize the differences between RSS channel maintenance and No. 1/1A ESS trunk maintenance so that it is unnecessary for the craft person to learn new and radically different procedures. The second: minimize software changes by making the RSS channel look as much like a trunk as possible.

5.3 Channel maintenance functions

Channel maintenance functions can be divided into two major categories: automatically initiated testing and manually initiated testing.

5.3.1 Automatic maintenance functions

The following six automatic maintenance functions are provided for channels:

(*i*) Per-call failure processing
(*ii*) Audit failure processing
(*iii*) Automatic progression testing
(*iv*) Error analysis
(*v*) Transmission testing
(*vi*) Software state control.

Per-call failure processing refers to the action taken by the channel maintenance programs when call processing suspects a channel fault. Even though a faulty channel can potentially affect many customers, real-time considerations prevent all channels from being fully diagnosed more than once a week. It, therefore, becomes the responsibility of call processing to inform maintenance when a faulty channel is suspected. Examples of per-call tests include testing if off-hook supervision can be successfully transferred over a channel from an RSS line, and a host network continuity test from the channel to a trunk circuit. When such tests fail, call processing programs attempt to place the channel on the Channel Maintenance List (CML). The CML is a queue of channels that are awaiting a system diagnostic. If the diagnostic fails, the channel is retested after a 5-second delay. If the channel fails both diagnostics, it is removed from service (i.e., locked out) as long as the Automatic Maintenance Limit (AML) has not been exceeded. In any case, two messages are printed on all failures to inform the craft person of both the failure and the disposition of the channel. If either test passes, RT error analysis is informed and the channel is returned to the traffic-idle, maintenance in-service state.

Audit failure processing takes place when system audits find a channel in an invalid state. The channel is placed on the Channel Maintenance List for Audits (CMLA). The CMLA is a queue of channels that are awaiting a blind-idle of their hardware. After the channel is hardware idled, the control program attempts to place the channel on the CML.

Automatic progression testing is the primary vehicle used to allow channel maintenance to detect and remove faulty channels before they are used by call processing, and cause calls to be lost. Beginning at 1:00 a.m. every Monday morning, channel automatic progression testing begins at the first idle channel in the first-assigned RSS. The diagnostic, software state control, and printing are exactly as described for the CML. When all channels in the RSS have been tested, testing continues with the first idle channel in the next RSS. Testing continues until all idle channels in all assigned RSSs are tested, or until 6:00 a.m. If testing has not been completed at that point, it is resumed each morning thereafter between 1:00 a.m. and 6:00 a.m. until all idle channels have been tested.

Error analysis for channels is carried out in much the same manner as described in Section 3.4 for the RT. All channel error analysis counts are kept in the RT. A data link message is sent to the RT every time a channel passes a CML diagnostic sequence in the host. In addition, the RT records every time a channel is involved in a half-path continuity, a half-path cross, or a CI board failure. If an individual channel fails in three consecutive usages (quick check failure) or performs poorly in

relation to other channels (peer analysis failure), a data link message is sent to the host resulting in the channel being removed from service if the AML is not exceeded.

Automatic routine transmission testing is provided using a CAROT system. Software modifications were necessary to allow:

(*i*) A line equipment number to be substituted for a trunk network number as the circuit identifier for CAROT testing.

(*ii*) A channel modifier digit specifying the state of the balance network and 2-dB pad instead of a trunk modifier digit specifying the trunk state.

The CAROT system interfaces with a Remote Office Test Line (ROTL) in the host machine and a miniresponder[4] in the RT. (The RT miniresponder is a miniaturized single-board version of the 52A responder used in the ROTL.) All appropriate CAROT capabilities that are available on No. 1/1A ESS trunks have been provided for RSS channels. The Processor Controlled Interrogator (PCI) allows the use of the ROTL equipment from the local office or an SCC without the aid of CAROT. The PCI is used primarily to verify that problems reported by CAROT have been corrected.

Software state control refers to the automatic administration of RSS channel maintenance states. Although one of these states is usually related to a hardware state, it is strictly a software construct. This software state, which may be permanent or transitory, is encoded in per-channel memory. The following maintenance states have been provided for RSS channels:

(*i*) ACTIVE—Available for use by both call processing and maintenance.

(*ii*) HIGH AND WET—Host side of the channel is off-hook and not involved in a connection. A channel in the high and wet state is unavailable to call processing. Channels are automatically removed from this state when they go on-hook. The most likely reason for the channel being in the high and wet state is a carrier failure.

(*iii*) CHANNEL MAINTENANCE LIST—Queued for a deferred channel diagnostic and temporarily unavailable to call processing.

(*iv*) LOCKED OUT—Out-of-service and permanently unavailable to call processing without manual intervention. Channels can be locked out by error analysis, automatic progression, or CML processing and manual requests from the TTY or one of the trunk test panels.

(*v*) CHANNEL MAINTENANCE LIST FOR AUDITS—Queue of channels found in an invalid state by the system audits and waiting to be blind-idled. Temporarily unavailable to call processing.

5.3.2 Manual channel maintenance functions

Manual channel maintenance functions can be requested from the

ESS maintenance TTYs, as well as from the ESS trunk test panels. Remote control from the SCC is also possible.

Single-channel diagnostics can be executed in one of two modes: normal and raw. A normal mode diagnostic indicates the general area of the fault. A raw diagnostic printout, with the help of the RSS channel trouble location manual, can be used to localize specific channel faults.

A single-channel transmission test can be requested using the RT miniresponder as a 102-type Far-End Test Line (FETL) for a 1-way (RSS to ESS) loss measurement, a 100-type FETL for a 1-way (RSS to ESS) loss and noise measurement, or a 105-type FETL for 2-way loss, noise, noise with tone, and gainslope measurements. During any of these tests, the switchable transmission components at the remote terminal end of the channel (described in Ref. 7) can be placed in most of their allowed states.

In addition to the single-channel maintenance functions, three types of multiple channel test requests are provided: group tests, repeat tests, and diagnosis of all out-of-service channels. These functions are provided to increase the efficiency of a craft person in localizing a transient fault or a single fault which affects multiple channels. Group tests allow the craft person to request a diagnostic or transmission test on all channels associated with the specified RSS. A repeat test allows the craft person to diagnose a channel 32 times in a row and print only the failures. A diagnosis of all out-of-service channels allows the craft person to quickly verify that these channels are still faulty.

In addition to the automatic software state control discussed earlier, channels can be manually locked out or made active. Manual state changes are not subject to the AML. If manual actions cause this limit to be exceeded, the craft person will be so informed.

Access to channels from manual test positions is provided to permit initial channel alignment and testing, and manual testing when system diagnostics provide insufficient trouble localization. The following functions are provided:

(*i*) DC access from the panel to the channel facility.

(*ii*) DC voltage measurements.

(*iii*) Connection from the panel to the channel to a 102-type FETL.

(*iv*) Monitoring or measuring of ac tones.

(*v*) Connection from the panel to the channel to a 100-type FETL.

(*iv*) Noise measurements.

(*vii*) The ability to send an ac tone from the panel and detect it at the RT.

(*viii*) The ability to control the 2-dB pad, the state of the hybrid balance network, and the off-hook/on-hook state of a channel connected to the panel.

The following channel list functions are provided:

(*i*) A list of all out-of-service channels.

(*ii*) A list of all high and wet channels.

(*iii*) A list of all idle channels in a specified RSS.

(*iv*) A list of all RSSs with the number of out-of-service channels exceeding the AML.

(*v*) A list of all channels in a specified RSS and their overriding maintenance state.

The ability to request the traffic and maintenance state of a single channel is also provided.

5.4 Channel diagnostic tests description

The approach taken by the channel diagnostic is to emulate all operations performed on a channel during a call, verifying in each instance that the channel performs satisfactorily. The hardware components that make up an RSS channel are described in Ref. 4.

The following nine channel tests are performed:

(*i*) Power Cross—A check to detect commercial power crosses at a channel's host line appearance.

(*ii*) False Cross and Ground—A check for path crosses or grounds in the portion of the ESS network involving a channel.

(*iii*) Supervision—A check that the on-hook and off-hook state of a channel can be passed from the RT to the host.

(*iv*) Restore Verify—A check that the line ferrod can be connected and disconnected via the line cut-off relay on the host line link network.

(*v*) Low Line Resistance—A check of the resistance across tip and ring at the host to detect a condition where this resistance is so low that an on-hook channel would erroneously trip ringing and cause false billing.

(*vi*) Showering Line—A check of the resistance across tip and ring at the host to detect a condition where the on-hook and off-hook status of a channel varies depending on whether the channel is supervised at the line ferrod or at a service circuit.

(*vii*) Dial Pulse—A check of the ability of a channel to successfully transmit a dial pulse zero (10 pulses) to a host dial pulse receiver.

(*viii*) AC Far-To-Near—A check of the ability of a channel to successfully transmit an ac tone from the RT to the host.

(*ix*) AC Near-To-Far—A check of the ability of a channel to successfully transmit an ac tone from the host to the RT.

It may be noted that this diagnostic does not provide any test of that portion of the RT network physically located on the CI board. This network testing function is performed by the RSS-controlled CI board diagnostic. This has the disadvantage that complete testing of a newly replaced CI board requires that one CI board and four individual channel diagnostics be requested. The overriding advantage of this

approach is that it permits a host controlled end-to-end functional test of the channel without creating an unacceptable resource contention problem with the RSS.

VI. REMOTE SWITCHING SYSTEM LINE MAINTENANCE

6.1 Line maintenance overview

The overall approach to RSS line maintenance is to extend from the host ESS all existing line maintenance features and to implement within the RT any maintenance feature uniquely required for RSS lines. Standard line maintenance features are normally divided, both functionally and administratively, into two types:

(*i*) Testing of the metallic customer loop and associated station set.

(*ii*) Testing of the central office per-line circuitry.

While RSS requires no changes to a properly designed outside plant,[2] the RSS per-line circuitry[4] is considerably more complex than the per-line circuitry in the ESS.[8] Both systems have line circuits that provide the basic functions of switching network protection, line attending, and voice network access. However, the RSS's nonmetallic voice-switching network requires that its line circuits provide dial pulse reconstruction, talking battery, and test access, all of which are provided by service circuits in the host ESS. The RSS line circuit must also provide metallic access to its shared service circuits for such functions as ringing and coin control. In addition, space and power considerations require a constant current loop-feed design, which in turn requires special line circuit provisions for anticorrosion biasing, detection of ground start originations, and switchable line feed states.

Therefore, traditional outside plant functions like Automatic Line Insulation Tests (ALIT) and Local Test Desk (LTD) have been implemented by providing new RT hardware[4] with the necessary dc access, and generalizing the host programs to control the new hardware via the data link, whereas new per-line circuit functions, such as diagnostics and error analysis, have been implemented in the RT.

6.2 Line maintenance functions

The maintenance functions provided for RSS loops include:

(*i*) Per-call loop tests, performed automatically by the system.

(*ii*) Automatic line insulation tests, normally performed on a routine, scheduled basis.

(*iii*) Manual testing from the local test desk, normally performed only when trouble is suspected.

(*iv*) Station ringer and *TOUCH-TONE** dialing tests, normally initiated from the customer premises when a station set is installed.

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* Registered service mark of AT&T.

Maintenance functions provided for RSS line circuits include:

(*i*) Per-call tests of various line circuit functions.

(*ii*) Routine exercises, which provide, on a scheduled basis, a complete diagnosis of the line circuit.

Each of these functions is described in more detail in the following paragraphs.

6.2.1 Loop maintenance functions

The number of per-call loop tests that can be made are restricted by considerations of call setup time and processor capacity. As a result, these tests are limited to those which establish that the line can safely be placed in a connection, and that the subsequent call disposition can be monitored. These tests are as follows:

(*i*) Power Cross Test—Before a metallic connection is set up to apply ringing, a test is made for voltages on the loop which may damage the ringing circuit.

(*ii*) Ringing Continuity Test—Shortly after ringing voltage is applied to a line, a current measurement is made to establish that a ringer is actually connected to the loop.

(*iii*) Showering Line Test—The RSS line circuit is more sensitive to dc loop current in the idle state than in the talking state. This can cause some leaky lines to "shower" (that is, continually appear to originate and then immediately hang up when put in a dialing connection). To prevent this, the line is scanned with the line circuit in both the idle and the talking states when an origination is detected.

When any of these three tests fail, an immediate report is made on a host TTY, identifying the line and the nature of the failure. This immediate reporting, which differs from the usual RSS error-analysis approach, is necessitated by the immediate customer service impact of these failures. Also, in the showering line case, the system must take defensive action (placing the line high and wet) to avoid being flooded with origination reports.

Permanent Signal and Partial Dial (PSPD) timing is another per-call loop "test," but one requiring much different treatment. Although faulty customer loops sometimes evidence themselves this way, PSPD failures are more often induced by customer actions. A PSPD timeout occurs when a line originates but does not dial at all (permanent signal) or does not dial successive digits (partial dial) within 20 seconds. As a result, the line is connected successively to an appropriate recorded announcement, receiver-off-hook tone, and finally an operator. If none of these actions results in the line going on-hook, the line is placed high and wet. After an additional timing interval specified by the Bell operating company, the line is reported on a host TTY. A summary list of all high and wet lines (both host ESS and RSS) is available by manual TTY request.

The Automatic Line Insulation Test (ALIT) provides automatic, routine surveillance of customer loops for insulation breaks in wire, cable sheath, and cable terminals. The RSS lines are tested under the control of the host ESS, using measuring circuitry in the RT. On a schedule established by the Bell operating company, the host ALIT control program sequences through all testable host and RSS lines in order of telephone number. For each RSS line, a data link message is sent, identifying the line and requesting an ALIT test. The RT performs the test, returning the results to the host. Failing results are reported on the appropriate host TTY.

There is one respect in which ALIT failures on RSS lines require special interpretation and screening. The anticorrosion biasing arrangement may be ineffective on lines with localized, very low resistance leakage paths to ground. The ALIT failure reports in this category provide the only automatic indication of an RSS line subject to corrosion.

In addition to performing routine testing, the ALIT circuit in the RSS may be used in the "demand" mode, via host TTY request. These tests may select different test types or ranges from those used for routine testing. Either a single line or all testable idle lines in a particular RSS may be tested via a single TTY request.

The RSS lines are accessible for testing from standard Local Test Desk (LTD) No. 14, or No. 16. Access arrangements depend on the distance from the test desk, through the host ESS, to the RSS. When this distance is within metallic testing range, a metallic access arrangement is provided. In this case, mechanized loop testing (MLT) access is also supported. Otherwise, access is via a modified version of the LTD Remote Test System (LTDRTS). From a user's point of view, both arrangements duplicate the majority of existing LTD functions. Certain functions (e.g., operation of the no test vertical key) do not apply because the RSS testing configuration is different. Other functions, like verifying that a ground start line can originate, cannot be performed because of design limitations. (The required ground start applique is automatically placed in the bypass state and the line is "tested" as a loop-start line.) When an LTDRTS is required, additional differences occur. To use a standard system at the LTD, nonstandard arrangements are provided in the host and the RT. The host must be able to detect a limited set of control oriented test requests (e.g., origination, disconnect, line ferrod), while test configuration requests are detected and acted upon at the remote terminal. This new hardware requires the LTD to use a different test trunk or test trunk group to obtain access to RSS lines than that used to access host ESS lines. It also requires a connection to an RSS line before RTS test battery voltages can be checked. (Existing systems require only a connection to the CDO.) A

complete description of the RSS line test hardware is included in Ref. 4.

All customer trouble reports are received at the Repair Service Bureau (RSB) which has primary responsibility for maintaining satisfactory service to customers. The RSB performs tests to determine if the trouble is internal or external to the RSS. Since the RSS line circuitry is more complex than the per-line circuitry of most existing switching systems, and because the RSS line circuit cannot readily be isolated from the customer loop, the internal-external decision is more complicated for RSS lines. In some cases, RSS line and ground start applique diagnostics will be needed to help localize the problem. Therefore, RSS line testing requires more coordination between the RSB and the SCC.

When a telephone set is installed, or repaired, the Station Ringer and *TOUCH-TONE* dialing test equipment can be accessed via a telephone company assigned directory number to perform any of the following tests:

(*i*) *TOUCH-TONE* Dialing Test—A verification that a predetermined digit sequence can be correctly dialed from a 10- or 12-button telephone set.

(*ii*) Automatic *TOUCH-TONE* Dialing Test—A verification that a predetermined digit sequence is dialed at the correct rate from a 12-button automatic dialer set.

(*iii*) Party Ground Identification Test—An off-hook resistance measurement from simplex tip and ring-to-ground.

(*iv*) Leakage Test—An on-hook resistance measurement from simplex tip and ring-to-ground.

(*v*) Ringing Test—A test of the ability to ring the customer phone.

For Station Ringer and *TOUCH-TONE* dialing testing of RSS lines, no special circuits are required at the RT. An RSS line accesses the host ESS Station Ringer and *TOUCH-TONE* dialing test circuit via a channel, and the host circuit is used for the *TOUCH-TONE* dialing tests and for all tone signaling to the line. Party ground identification and leakage tests are performed by the RSS upon host data link request. The results are returned to the host which, in turn, conditions the Station Ringer and *TOUCH-TONE* dialing test circuit to signal the appropriate test result tone. The ringing test is performed by the RSS in a similar manner.

6.2.2 Line circuit maintenance functions

Generally, each time the RSS firmware accesses a line circuit to perform a function, a test is made to ensure that the action is successful. This approach is supported by comprehensive test access and by the fact that the tests can be made quickly (i.e., with an acceptable penalty to call setup time and processor capacity). Among the per-call tests performed on a line circuit are the ability of the circuit to

(*i*) Place the loop feed in the talking (high power) state.

(*ii*) Provide a path for network holding current.

(*iii*) Operate and release relays which provide access to the metallic network.

(*iv*) Place the loop feed in the idle (low power) state.

(*v*) Open the path for network holding current.

Failure of any of these tests is reported on the host maintenance TTY and also analyzed by standard RSS error analysis. If the failures exceed the error analysis threshold a high priority trouble message is printed on the host TTY. Some of these failures are subject to additional processing by the RSS firmware. For example, loss of power to a line circuit causes the line to appear to originate. Therefore, when the attempt to place a line in the talking state fails after an origination is detected, further tests are made and, if appropriate, the failure is reported at the host ESS specifically as a "no power" condition.

All assigned RSS line circuits are diagnosed as part of the RSS routine exercise program. Both the scheduling control and the diagnostic logic reside entirely within the remote terminal. In addition, any single RSS diagnostic may be requested via a TTY at the host ESS. When manually requested, the diagnostic may be performed in any of the three modes described in Section 3.5.

The remote terminal diagnostics are partitioned to permit complete testing of a single plug-in circuit board with a single request. For most customer lines, this partitioning allows all diagnosable circuitry associated with a single line to be tested via a single request for a line interface board diagnosis. Certain lines, however, such as ground start, and coin lines, require an additional request to diagnose the associated ground start applique.

VII. SUMMARY

The RSS maintenance plan has been made as consistent as possible with existing Bell operating company switching system procedures, but the geographical separation of the various system components has required modifications and additions to these procedures. In addition to the switching craft charged with RSS maintenance responsibility, several other craft forces (e.g., outside plant, data services, LTD, carrier, trunk maintenance, etc.) will become involved in the maintenance of various portions of the RSS. The required coordination of these different craft forces will make new Bell operating company maintenance procedures necessary.

The maintenance of each major portion of the RSS has been discussed in detail. Remote terminal maintenance activities are carried out nearly autonomously, with little interaction required between the host ESS and the RT. Both hardware and software checks are utilized to

detect system faults, and automatic recovery, circuit removal, and fault reporting are utilized when a fault is detected. Manual diagnostics are available for detailed fault location and repair.

The PUC/DL is a direct peripheral unit of the host ESS. Its maintenance is coordinated closely with that of the host.

The RSS channel maintenance has been made to look as much like ESS trunk maintenance as possible. Per-call-failure tests, error analysis, and manual maintenance access arrangements, similar to those existing for trunks, have been provided.

Numerous existing line maintenance features (e.g., ALIT, LTD access, etc.) have been extended to RSS customer loops from the host ESS. In addition, the increased complexity of the RSS per-line circuitry has made new maintenance functions necessary.

VIII. ACKNOWLEDGMENTS

The design and implementation of the various portions of the RSS maintenance plan, and their integration into existing Bell operating company maintenance procedures have required the cooperation and assistance of everyone associated with the RSS project. It is not possible to acknowledge individually everyone who helped with this plan. Many of their contributions are discussed in greater detail in other papers included in this issue of *The Bell System Technical Journal.* The authors would like to especially acknowledge the help of D. A. Anderson, F. R. Fromm, G. T. Kresan, R. W. Sevcik, and S. R. Staak.

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No. 10A Remote Switching System:

Transmission Plan

By P. N. BURGESS, J. L. NEIGH, and R. G. SPARBER

(Manuscript received May 15, 1980)

The transmission properties of a switching system always play an important role in the design of any switching system. This was particularly true in the design of the 10A Remote Switching System which has an architecture that raises new transmission problems. This paper describes these new problems and details the methods by which they were solved.

I. INTRODUCTION

The design of the 10A Remote Switching System (RSS) has involved the interaction of many disciplines and required the solving of many old and new problems. One of these traditional questions concerned the transmission performance of the switching path. It must be assured that the switching path contributes little to the transmission impairments of the overall end-to-end talking connection. While the design of the RSS must continue to meet this requirement, the question must be answered in a new light since RSS is an "extension" of its controlling host RSS and located some distance from it. This paper addresses the transmission issues associated with the host-RSS link, spelling out the objectives and requirements, detailing the actual plan, describing the methods of analyzing and evaluating the plan, and defining its characteristics.

II. OBJECTIVES AND REQUIREMENTS

In this section, we describe various aspects of the design of RSS which had an impact on the development of the transmission plan. For a more detailed description of the RSS, see Ref. 1.

2.1 Extension of its host

The RSS, by design, is considered an extension of the host which controls it and on which it homes. This implies that lines served by the RSS be given the same kind of service as those lines served by the host directly. A customer served by the RSS should experience about the same transmission grade of service as would be experienced by a customer served directly by the host. This is an *absolute requirement* when RSS replaces a class 5 Community Dial Office (CDO). In this case, the loops on the CDO could have been designed to the limits of a conventional class 5 office, and the link between the CDO replacement and the class 5 host should not add additional impairments which might affect DDD transmission. This transparency characteristic is *desirable* for pair-gain applications because, even though the transmission link replaces designed loss in the loop, significant savings can be obtained using finer gauge cable than would be required if the RSS subscribers were served directly by the host.

2.2 Choice of host class

As a way of assuring wide deployment of the RSS, it is important that the transmission plan be designed so that the RSS can be hosted from any local electronic switching system. In other words, the plan should not require that the RSS be hosted only by class 4 or combined class 4/5 offices.

2.3 Singing and echo performance

By forcing the transmission link to be transparent from a loss point of view, some form of amplifying equipment is needed. This gain can be supplied by unidirectional or bidirectional amplifiers. In either case, instability is a potential problem.

One choice of carrier facilities could be unidirectional amplifiers, commonly known as a 4-wire facility. Since both ends of the link are 2-wire (the subscriber end and the host end), standard methods of converting between 2- and 4-wire facilities using hybrids are required. Raising the gain in each direction to satisfy the transparency requirement mentioned earlier increases the probability that the connection will oscillate or sound hollow because of the feedback mechanisms of the 2- to 4-wire conversions, unless corrective measures are taken. The transmission plan must provide these corrective measures so that the transmission paths exhibit adequate echo performance.

2.4 Distance objectives

For this system to be economically viable, any restraints imposed by the transmission plan must be generous enough to allow the RSS to be *at least* 50 miles from its host.

2.5 Type of facilities

As indicated in a companion paper,[1] RSS will be deployed in various applications, e.g., as a replacement for CDOs and as an economic alternative to cable (pair gain). As a result, the RSS should be able to be served by as many different types of carrier facilities as possible, including both digital (e.g., T1) and analog (e.g., N) types, particularly to take advantage of in-place plant.

2.6 Interface with real loops

The plan must be workable and provide adequate performance even in the face of a real loop plant which does not conform exactly to design rules for a variety of reasons, including economic and maintenance. Design rules for loop plant include constraints on resistance, load coil spacing and deployment, and constraints on allowable bridge taps. As the loop plant is reconfigured to satisfy customer requirements, variation from the design rules can occur.

2.7 Ease of administration and maintenance

The plan must be straightforward and use simple methods for administration and maintenance. The ultimate goal should be that the RSS satisfy its own needs for information (e.g., condition or type of subscriber loop) rather than relying on manual methods, and use maintenance methods that are triggered and executed automatically.

III. THE RESULTING PLAN

3.1 Zero-dB link

The RSS transmission plan centers around 0-dB links from the line appearance at the RSS to the ESS line link network appearance of the channel. (See Fig. 1.) From a transmission loss standpoint, the RSS line effectively appears as a line at the ESS.

3.2 Improved impedance match

Previous implementations of 0-dB plans have often had problems because the resulting 2- to 4- to 2-wire paths were frequently poor transmission links. Connections using these links might be graded as poor by customers because they would sound "hollow"* or, even worse, they might be unstable and oscillate or squeal in the customer's ear. This condition results from the fact that signals starting at *A* (see Fig. 2) and arriving at the input of the 4-wire port of hybrid 1 would "leak across" the hybrid and return via its transmit port back to hybrid 2. If

* Hollowness on telephone connections is typically referred to as listener echo. Loss in the closed loop formed by the 2- to 4- to 2-wire path is defined as listener echo path loss.

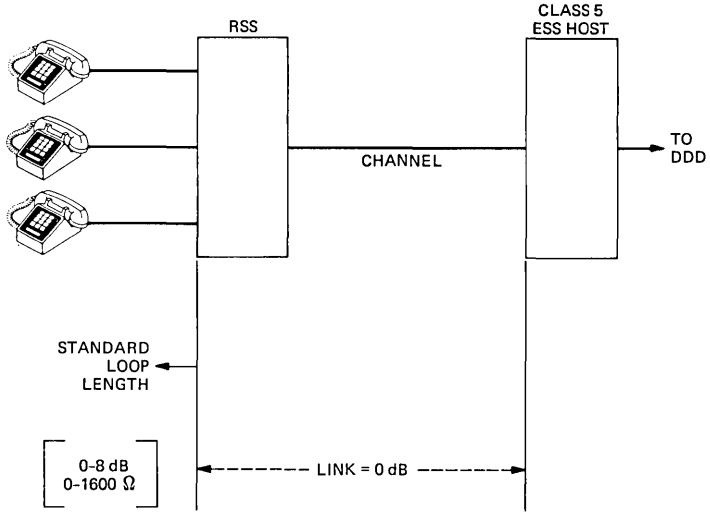

Fig. 1—Remote switching system transmission plan basic objective.

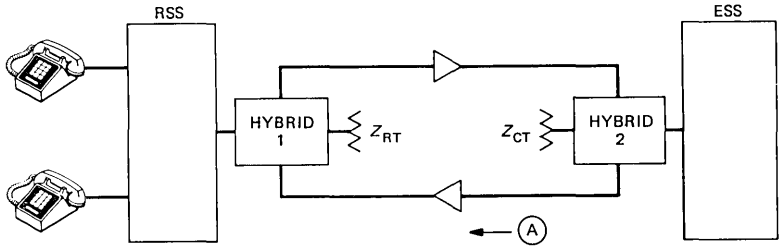

Fig. 2—Remote switching system transmission link.

the signal also leaks across hybrid 2 such that it returns to *A* at the same or greater energy than it began, oscillation (or singing) can occur. Oscillation can be prevented by decreasing the gain in either (or both) directions, or by increasing the loss across one (or both) hybrids. Because we must keep the loss from one end to the other at 0 dB, we are not free to decrease the gain of either amplifier. Therefore, techniques for increasing the transhybrid loss at the 2- to 4-wire interfaces were established. The most straightforward approach is to choose a better impedance compromise network for the overall loop population. It has been determined[2] that a single, parallel resistor-capacitor compromise network provides a better impedance match to the overall Bell System loop population than does the standard 900 ohm in series with 2.16-μF network. In addition, it has also been determined that further improvements in impedance matching and, hence, return loss can be gained by using separate parallel RC balance networks for

loaded and nonloaded loops. The use of separate balance networks for loaded and nonloaded loops is generally called loop segregation.

To improve stability and listener echo performance on the RSS-host channel, the RSS has adopted the improved balance networks. The channel units at the remote end of the RSS-host channel are equipped with switchable balance networks for loaded and nonloaded loops. The appropriate balance network is inserted on a per-call basis. The loaded-nonloaded decision is made automatically by a new circuit called the Electronic Loop Segregator (ELS). See Section 3.3 and the Appendix for more details.

At the host end of the channel, it is impractical to implement a device like the ELS in existing analog offices since there is no convenient place in the host network topology to place the loop segregator circuit and minimize per-call usage of host resources. Therefore, a single compromise network is used to match all types of terminations. The most difficult to match impedances at the host office are the lines served by the host. Therefore, the RSS channel unit at the host uses an impedance compromise network. This results in an improvement in return loss for connections to host lines and provides adequate return loss for connections to direct and toll connecting trunks.

3.3 Electronic Loop Segregator

The separation of loops into the two categories of loaded and nonloaded loops is done by the RSS system using the ELS. This circuit is used in the following way:

(*i*) At least once a day, a measurement of the ac impedance of each on-hook line is made. The real part of this impedance is compared to a threshold. The result of this comparison is stored in RSS memory with 1 bit per line.

(*ii*) When the line goes off-hook on a terminating or originating call, the proper balance network is chosen for the RSS end based on the above measurement. If the real part of the impedance is above the threshold, the loop is assumed to be loaded, and the loaded network is selected. If the real part of the impedance is below the threshold, the loop is assumed to be nonloaded, and the nonloaded network is selected. (If the loop is misdesigned, ELS usually chooses the best match.)

3.4 Maintenance aspects

To retain the improved transmission performance that the modified balance networks provide, all the parameters of the elements in the transmission paths must be chosen to have a minimal variation. This has been guaranteed for each end of the link by choosing components with minimal variation and by assuring that the variations in the gains

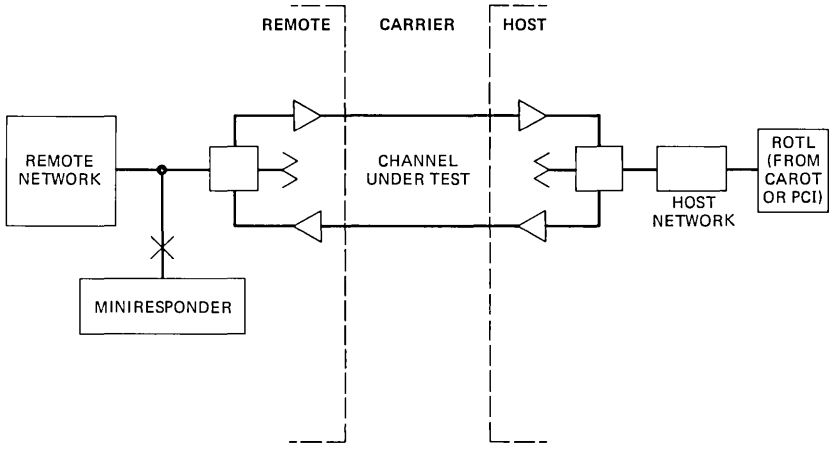

Fig. 3—Remote switching system channel testing.

of the amplifiers be limited. For this plan, we have required this variation to be limited to ±1 dB.

The maintenance of the channels from both an operational and transmission perspective is done from the host, and uses techniques similar to those used to maintain operational and transmission performance on trunks. Included in the RSS frame is a miniresponder circuit which has metallic access to the network side of each channel. (See Fig. 3.) The host, under control of automated transmission test systems [centralized automatic reporting on trunks (CAROT) or program controlled interrogator (PCI)], will establish a test call to the responder from the ESS and will use the channel under test. Conventional loss and noise measurements will be made in each direction. The $Q1$ level (the gain/loss band outside of which a report is made to the maintenance craft) is about 0.7 dB, and the $Q2$ level (the gain/loss band outside of which the channel is removed from service) is about 0.9 dB. The choice of these values is influenced by the measurement accuracy of the test equipment which is ±0.1 dB.

3.5 Provisions for trouble loops

As will be shown later in this paper, the above plan works well even in the face of most real loops that do not necessarily meet the conventional resistance design requirements. As a backup measure, however, a feature has been included to allow the RSS to work temporarily with a loop that is grossly different from the design requirement. Loops with this characteristic need to be repaired, but can be made to work temporarily until maintenance craft can be routinely dispatched. On a temporary basis, the RSS has the capability of

inserting 2-dB loss in each direction of a channel connected to a loop. The system will perform this loss function if a specified bit per line is set. The bit is set (or cleared) by a TTY message initiated by a craft person. The bit is not controlled autonomously by the system. This loss state will be temporary; ultimately, the problem loop must be fixed.

IV. EVALUATION AND ANALYSIS METHODS

When the plan was designed, it was clear that the various aspects of the plan provided improvements to the transmission quality, but it was not clear whether enough improvement was achieved. This section describes the various methods used to analyze and evaluate the plan.

4.1 Subjective testing

A zero loss 2- to 4- to 2-wire connection has the potential of singing if the energy circling around the 4-wire path is sufficiently high to sustain oscillations. However, even if a connection is not singing but is close to singing, the transmission performance would not generally be considered acceptable to most customers. This characteristic is called "near singing distortion" or "listener echo." Objectively, near singing creates ripples in the net 2- to 2-wire response of the system. The ripples can be characterized by the magnitude and frequency shape of the loss in the feedback path, plus the round-trip delay in the 4-wire portion of the system. Subjectively, near singing manifests itself as an unnatural or hollow effect which can, in some cases, make a conversation sound as if it is being conducted in a drainage pipe.

To quantify the effects of near-singing distortion, subjective tests were conducted (Ref. 3). The tests independently varied listener echo path loss, round-trip delay, and frequency response of the 4-wire path. As a result of these tests, a new measure of subjective quality has been defined: Weighted Echo Path Loss (WEPL). The WEPL provides a more accurate view of connection quality than does singing margin. The WEPL concept is demonstrated in Fig. 4. The measure is based on an average (versus frequency) of the loss around the closed loop (listener echo) path. Because of the averaging, WEPL provides a less conservative view of connection quality than singing margin. Use of WEPL for judging subjective quality allows more meaningful objectives for the control of listener echo to be established.

One of the most important parameters when evaluating performance is the round-trip delay of the system. Listener echo becomes increasingly objectionable with increasing delay. Correspondingly, the value of WEPL required to provide adequate connection quality increases with increasing delay. Thus, current WEPL objectives are stated as a function of round-trip delay in the 4-wire path. A comparison of the

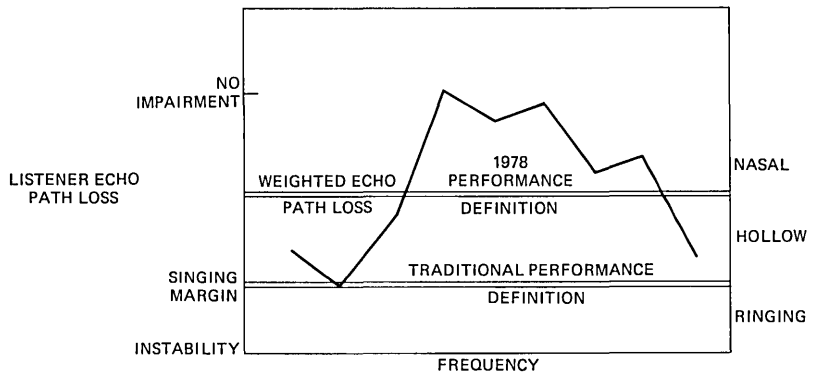

Fig. 4—Singing margin and weighted listener echo path loss.

WEPL objectives and the predicted WEPL performance for a distribution of connections can be used to establish the allowable delay in the system. For example, the WEPL objectives for a distribution of connections with round-trip delays of 4 and 7 ms are shown in Fig. 5. For a system with a 4-ms round-trip delay to provide acceptable listener echo performance, the WEPL performance for a distribution of connections made over the system must exceed (i.e., be to the right of) the 4-ms WEPL objective. Similarly, the 7-ms distribution must be met or exceeded by connections with a 7-ms round-trip delay. Recommended distributions of WEPL performance for other delays have also been established (Ref. 3).

Knowledge of the allowable round-trip delay can be used to form limits on signal processing delays and to set length restrictions for remote-host transmission lengths. The remote-host length restrictions for the RSS system are discussed in Section V.

4.2 Evaluation using various loop populations

Once the subjective tests had been used to establish transmission objectives for achieving customer satisfaction, it was necessary to determine how the RSS performed with its transmission plan. This was done by performing a computer simulation based on a model of the RSS transmission characteristics and a data base which contained the impedance of the subscriber loops. The model included the transmission characteristics of the switched path from the line appearance of the subscriber on the RSS to the 2-wire channel appearance at the host ESS. The model was more complex than models of previous ESS systems because the RSS contains more components affecting the transmission paths than earlier systems. With the model created (together with the expected worst-case tolerance of each part), the performance of RSS

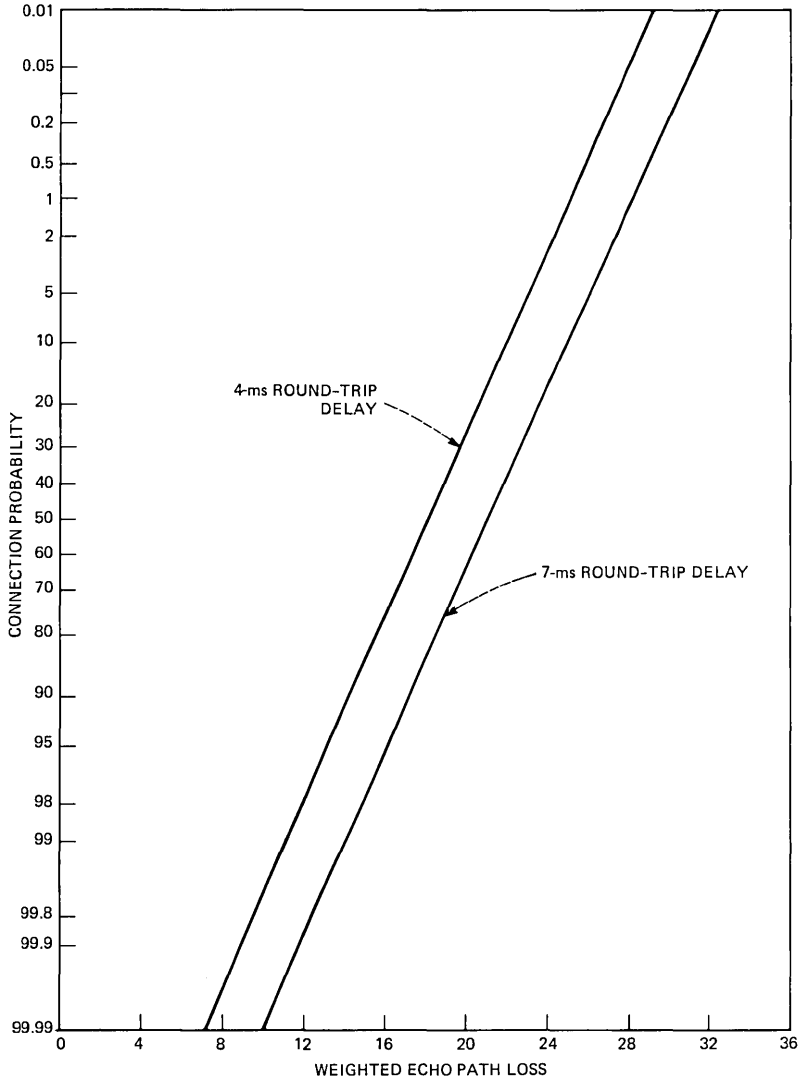

Fig. 5—Weighted echo path loss objectives for 4- and 7-ms round-trip delay.

for loss and WEPL was determined by simulating connections where terminations at the 2-wire points were real loop impedances. The simulation involved choosing two loops from the population, placing one at each end of the connection, and calculating loss and WEPL for that connection. This process was repeated for all possible connections involving all loops in the data base. Cumulative distribution functions of WEPL performance were then generated and compared with the requirements.

The evaluation of WEPL performance for the RSS was completed using two different data bases of customer loops. The first data base came from the 1973 survey of Bell System loops (Ref. 4). This data base contained 1098 loops sampled from all varieties of real loops on working switching systems. These survey data were based on paper records only. The second data base came from a 100-percent sample of the loops served by one of the first RSSs placed in service. This data base contained 625 loops, and was generated by using paper records

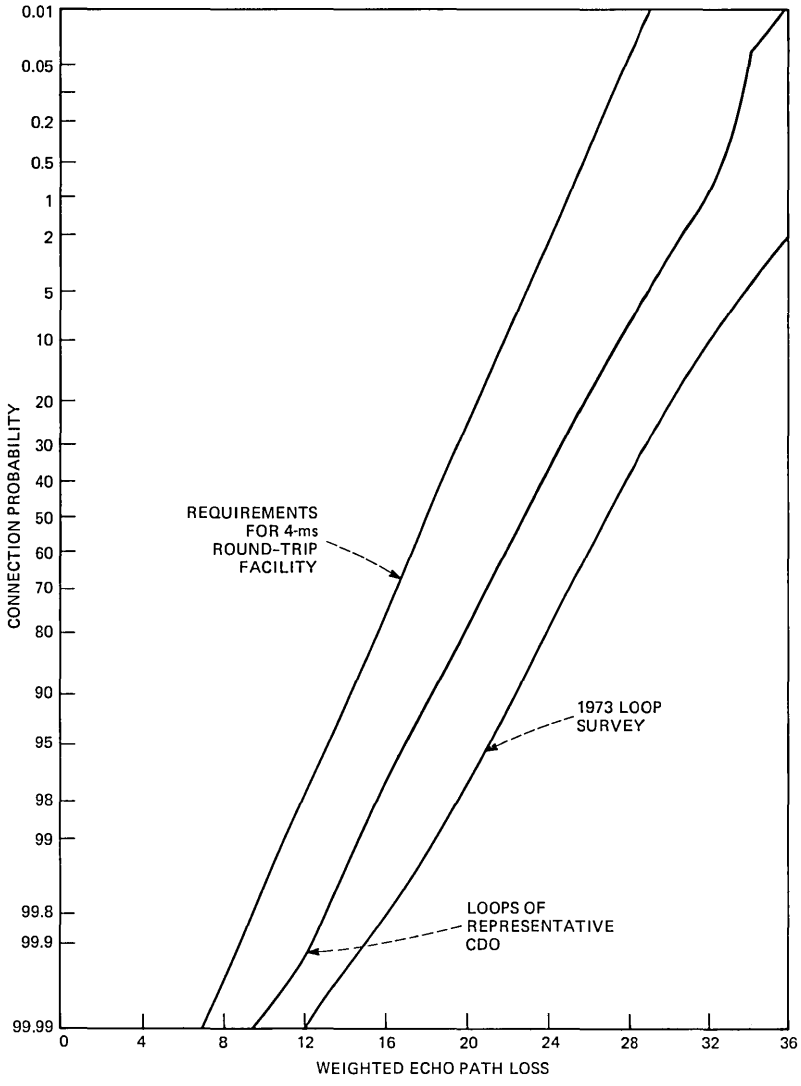

Fig. 6—Weighted performance with RSS.

and electrical testing of each loop. It is expected that this office is typical of many Bell System CDOs.

The WEPL performance using the CDO data base was not as good as the performance using the 1973 survey data base. (See Fig. 6.) However, performance for both surveys met the WEPL requirements for a system with 4-ms round-trip delay. This level of performance of a CDO population is significant because the CDO data base contained a large number of loops that did not strictly adhere to resistance design rules. This WEPL performance level implies that wholesale changes are *not* required when an RSS is placed into service, even though there are a number of other reasons that loop plant should be improved, independent of the installation of the RSS.

V. CHARACTERISTICS

5.1 Limitations on facility types

Because of the requirement (in Section 3.4) that the variation of gains be limited to ±1 dB, only the more modern carrier types are compatible with RSS. Specifically, RSS will be able to interface with T1 digital lines, N2, N3, and N4 analog lines, and analog radio facilities that use A5 or A6 banks. The A-banks must be equipped with compandors to assure quality signal-to-noise performance.

5.2 Distance limitations

As is shown in Section 4.2, the transmission link is limited in distance by the round-trip delay of the facility. This round-trip delay is limited to 4 ms (averaged over the frequency band). All components that contribute to the delay must be accounted for, including the multiplexing terminals at each end, as well as the propagation delay over the transmission medium. These parameters vary with facility types. The following lists the distance limitations by facility type:

T carrier via repeatered metallic lines	175 miles
T carrier via digital radio	260 miles
N2 carrier via repeatered metallic lines	150 miles
N2 carrier via analog radio	280 miles
N3, N4 carrier via repeatered metallic lines	75 miles
N3, N4 carrier via analog radio	140 miles
A5, A6 banks with compandors via radio	140 miles

VI. SUMMARY

The RSS is now providing service to customers in Clarksville, New York, as well as in over 50 other locations around the country. Performance from both a switching and transmission perspective has

been very satisfactory. The transmission plan that has been presented above has met all the goals and objectives that were set forth.

VII. ACKNOWLEDGMENTS

The evaluation of the 10A RSS transmission plan has involved the work and advice of many people in Bell Laboratories and AT&T. We would like to acknowledge the contributions of W. L. Ross, J. R. Rosenberger, III, R. W. Hatch, J. L. Sullivan, A. M. Lessman, G. M. Cofer, and D. L. Whitney.

APPENDIX

Techniques for Loop Segregation Using ELS

A scheme for improving singing margin and echo performance through the use of loop segregation is meaningless unless a simple means of distinguishing between loaded and nonloaded loops is available. Separating loaded from nonloaded loops can either be done on paper (through office records), or by an electrical measurement. The paper approach is hazardous because using office records is not as accurate as electrical measurements and could commonly lead to the wrong choice for a compromise network. The most common electrical measurement which can distinguish between loaded and nonloaded loops is the level trace meter. However, there are other simpler measures which can be employed. These measures are based on the fact that one of the most significant electrical differences between loaded and nonloaded loops is in the real part of the loop impedance near the upper band edge. These differences occur for both on-hook and off-hook measurements. However, the customer may be bothered by measurements on the loop while the telephone receiver is at the customer's ear. Also, off-hook measurements may experience difficulties because of interference from the customer's voice or ambient noise at the subscriber location. Therefore, the RSS has adopted an algorithm for loop segregation based on an electrical measurement of the on-hook impedance. Fig. 7 shows a scatter diagram of on-hook loop driving point impedance at 3200 Hz for loops from the 1973 Bell System customer loop survey. Different symbols have been used for loaded and nonloaded loops. Note that there are differences between the two populations which can be exploited. Table I shows the result of a search for a loaded-nonloaded decision criterion based on the real part of the on-hook impedance. A threshold setting between 400 and 540 ohms results in a loaded-nonloaded accuracy of 98.7 percent. Almost all of the mistakes are loaded loops matched with nonloaded balance networks. They are primarily short single-load coil loops which should not have been loaded.

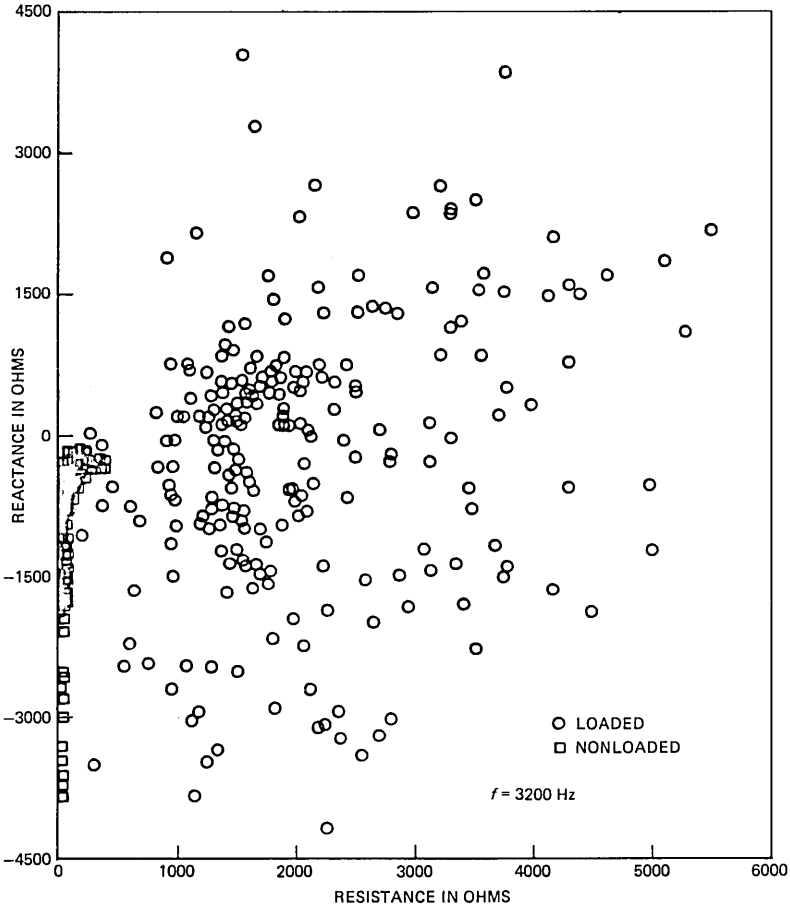

Fig. 7—Bell System loop survey—loop driving point impedance (3200 Hz) on-hook 500 set.

The following paragraphs give an overview of the circuit arrangements to do this segregation. The standard way to measure an unknown impedance (such as that of the loop which we wish to characterize) is shown in Fig. 8. A current of known level and frequency is applied, and the resulting voltage is measured. This works well if the unknown impedance (Z_x) is passive. However, any noise from the unknown impedance shows up in this voltage. The obvious solution is to filter V at the same frequency as the current source. (See Fig. 9.)

This will block the noise unless the noise falls in the pass band of the filter. As we boost the Q of the filter, less noise can pass. This works well as long as the current source frequency remains in the filter's pass band. One can see that as the bandwidth gets smaller, the alignment of the oscillator and the filter becomes critical.

Table I—Threshold values for loaded-nonloaded segregation based on real part of 3200-Hz on-hook impedance

Real Impedance	Number Mistakes	Number Loaded Assumed Nonloaded	Number Nonloaded Assumed Loaded
300	178	9	169
320	138	11	127
340	106	11	95
360	68	11	57
380	40	13	27
400	14	13	1
420	13	13	0
440	13	13	0
460	14	14	0
480	14	14	0
500	14	14	0
520	14	14	0
540	14	14	0
560	15	15	0
580	15	15	0
600	15	15	0
620	17	17	0
640	18	18	0
660	18	18	0
680	18	18	0

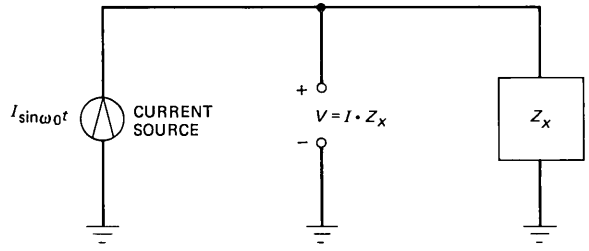

Fig. 8—Standard impedance measurement technique.

Fig. 10 shows the details of the problem. Here, one Band Pass Filter (BPF) is used as an oscillator and another one is used to filter the current related to the unknown impedance. Ideally, the two filters should be identical. One way to keep the two filters close is to build them from crystals. This could be done, but at 3200 Hz, it would be difficult and expensive. Besides, what is needed is not a precise frequency—only tracking filters.

The best way of making two filters track is to make them one filter. If the same filter can be used to generate the oscillations and filter the resulting voltage, the filter's Q can be made very large.

Figure 11 displays the circuit configuration using only one filter. There are three functions present. First there is the high Q, two-pole,

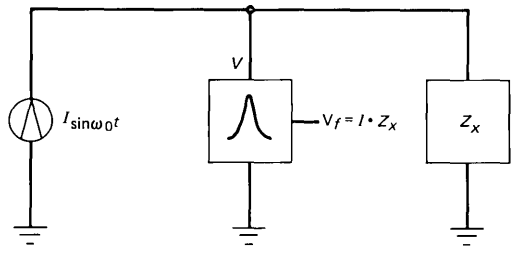

Fig. 9—Impedance measurement which reduces effects of noise.

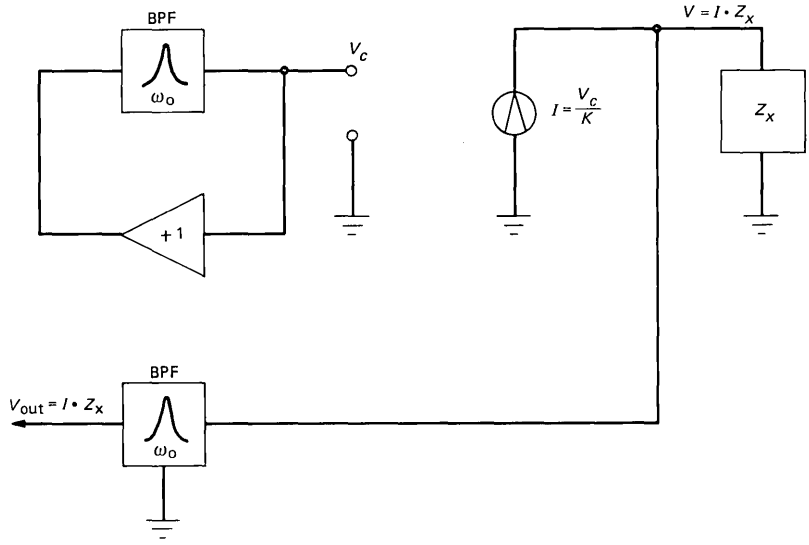

Fig. 10—One form of implementing Fig. 9.

BPF. Added to this is the Voltage Controlled Circuit Source (VCCS). The comparator completes the circuit.

If we assume that the BPFs output voltage, V_{out}, is a sine wave at a given frequency, then the output of the comparator, V_c, will also be at the same frequency. Furthermore, it will be in phase with V_{out}. The VCCS will also be in phase with V_{out}.

The test current out of the VCCS is applied to the unknown impedance Z_x. The resulting voltage is applied to the filter. It is at the same frequency and out of phase with the test current by the phase angle of Z_x. The input voltage to the filter is equal to the test current times the unknown impedance. Note that a phase difference has been forced across the filter. V_{out} is, by definition, 0 degrees; V_{in} is determined by

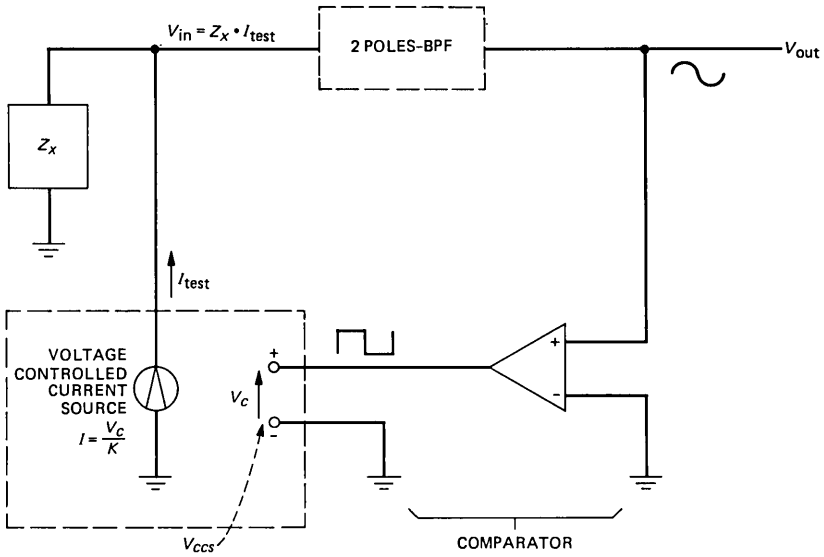

Fig. 11—Improved way of implementing Fig. 9 using single filter.

Z_x's phase. The BPF is forced to exhibit a phase difference equal but opposite to the unknown's phase. Once this occurs, the sum of the phases around the signal path become 0 degrees. The frequency of oscillation adjusts itself to satisfy this condition.

In the above discussion, it was assumed that all voltages and currents were sine waves. Note that the comparator's output is really a square wave. This forces the test current to also be a square wave. A square wave contains odd harmonics, as well as the fundamental. However, only the fundamental frequency passes through the high-Q BPF. It is, therefore, valid to treat all signals as pure sine waves.

The circuit will oscillate as long as the sum of the phases equals zero. The two-pole BPF can exhibit phases from −90 degrees to +90 degrees. This means an unknown impedance must not exceed ±90 degrees. All telephone loops satisfy this condition.

It can be shown that the magnitude of V_{out} of Fig. 11 is proportional to the real part of the unknown impedance, Z_x.

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ACRONYMS AND ABBREVIATIONS

ACI	analog carrier interface
ACKBLK	acknowledgment-block
ALIT	automatic line insulation test
AML	automatic maintenance limit
AROB	activate remote order buffer
ATP	all-tests-pass
AUD	audible circuit
BGNBLK	begin-block
BGT	background task
Bp	bank pointer
BPF	band pass filter
BOC	Bell Operating Company
BOS	build-out switch
CAROT	centralized automatic reporting on trunks
CARSEL	carrier select input
CC	central control
CCIS	common-channel interoffice signaling
CCITT	Comite Consultatif International Telegraphique et Telephonique
CCS	hundred call seconds
CDO	community dial office
CGA	carrier group alarm
CI	carrier interface
CLKOUT	clock out
CODEC	coder-decoder
CML	channel maintenance list
CMLA	channel maintenance list for audits
CNTL	control
CPD	central pulse distributor
CRC	cyclic redundancy check
CRC-CCITT	cyclic redundancy check-Comite Consultatif International Telegraphique et Telephonique
DAC	digital-to-analog converter
DDD	direct distance dialing
DDS	digital data system
DIGROUP	digital carrier group (twenty-four channels)
DIP	dual in-line package
DLENA	data link enable A
DLENB	data link enable B
DLI	data link interface
DN	directory number

DSU	data service unit
DSU-DP	data service unit-data port
EIA	Electronics Industries Association
ELS	electronic loop segregator
ENDR	end-ROB
EPROM	erasable programmable read-only memory
ESS	electronic switching system
FETL	far-end test line
FITS	failures in one billion hours
FO	fan out
G-J	grid-junctor
GS	ground start
GSA	ground start applique
HLSC	high-level service circuit (same as USC)
HROB	high-priority ROB
IC	integrated circuit
IGFET	insulated gate field effect transistor
IHA	hold current—side A
IHB	hold current—side B
I^2L	integrated injection logic
INHIB	inhibit signal
INT	interrupt signal
I/O	input/output
IT	talk current
JCT	junctor
JFET	junction field effect transistor
LED	light-emitting diode
LEN	line equipment number
LI	line interface
LIU	line interface unit
LLC	line load control
LLN	line link network
LREN	line remote equipment number
LSI	large-scale integration
LTD	local test desk
LTDA	local test desk applique
LTDRTS	local test desk remote test system
MCC	maintenance control center
MCEN	memory chip enable
MDAC	multiplying digital-to-analog converter
MLAP	metallic line access port
MLT	mechanized loop testing
MRDY	memory ready
MSD	miscellaneous scan and distribute

MSI	medium-scale integration
MTBF	mean time between failures
MTTF	mean time to failure
MWRT	memory write
NEBS	New Equipment Building Systems
nMOS	n-channel metal oxide semiconductor
OIU	office interface unit
PA	power alarm
PAB	peripheral address bus
PAM	pulse-amplitude modulation
PBX	private branch exchange
PCI	processor controlled interrogator
PCM	pulse-code modulation
PMC	path memory channel
PMJ	path memory junctor
PMR	path memory remote
PNPN	semiconductor crosspoints, described by the four layers in the device
POB	peripheral order buffer
POTS	plain old telephone service
PSPD	permanent signal and partial dial
PU	peripheral unit
PWC	pulse-width controlled
PWB	printed wiring board
PUC/DL	peripheral unit controller/data link
PUC DL/DCT	peripheral unit controller data link/digital carrier terminal
RAM	random access memory
R-DIPs	resistor-DIPs, used for level adjustments in channels
RCLK	receive clock
RE	read enable
REN	remote equipment number
RLT	remote line test
RMDN	remote miscellaneous distributor number
RMSN	remote miscellaneous scan number
RNDIS	receive not disable
RNPCM	receive not pulse-code modulation
ROB	remote order buffer
ROH	receiver off-hook
ROTL	remote office test line
rp	register pointer
RSB	repair service bureau
RSCO	remote switching system central office end (D4 unit)
RSS	remote switching system

RT	remote terminal
RTS	remote test system
RWD	receive window
SAB	stand-alone buffer
SCC	switching control center
SCR	silicon controlled rectifier
SDN	special directory number
SDLC	synchronous data link control
SF	single frequency
sp	stack pointer
SRI	client buffer identifier
SSI	small-scale integration
SXS	step-by-step
SYSRD	system read
TAB	test access bus
TCI	T-carrier channel interface
TDCLK	transmit data clock
TLN	trunk link network
TNDATA	transmit not data
TR	transmit-receive
TRCC	T-carrier restoration control center
TTL	transistor-transistor logic
TTY	teletypewriter
TWD	transmit window
UCR	universal call register
USC	universal service circuit (same as HLSC)
UV	ultraviolet
VCCS	voltage controlled current source
WE	write enable
WEPL	weighted echo path loss
WPBLK	write-protect block

CONTRIBUTORS TO THIS ISSUE

Nadine B. Abbott, B.S., 1971, and M.S., 1973 (Applied Mathematics and Computer Science), Washington University at St. Louis; Advanced Computation Laboratory, 1973–1975; Bell Laboratories, 1975—. Ms. Abbott's initial assignments at the Laboratories were to provide systems engineering support for rural and suburban local switching developments including No. 3 ESS and the No. 10A RSS. Since 1979, she has been engaged in the evaluation of various strategies for improving the efficiency of the network. Currently, she is participating in studies to define new interfaces between the network and customer premises equipment.

J. Mark Adrian, B.S. (Electrical Engineering), 1969, Iowa State University; M.S., 1971 (Electrical Engineering), Northwestern University; Northwestern Bell Telephone Company, 1968–1969; Bell Laboratories, 1969—. Early in his career at Bell Laboratories, Mr. Adrian performed exploratory work that led to the No. 3 ESS, as well as other exploratory work in electronic switching networks. Later, he was involved in several areas of the No. 10A RSS, such as line interface, network, and carrier interface. Presently, he is supervisor of the No. 5 ESS Line Interface Group. Member, IEEE, Tau Beta Pi, Eta Kappa Nu, Phi Kappa Phi.

Douglas A. Anderson, B.S. (Electrical Engineering), 1965, University of Colorado; M.S. (Electrical Engineering), 1966, Purdue University; Ph.D. (Electrical Engineering), 1971, University of Illinois; Bell Laboratories, 1965—. After joining Bell Laboratories, Mr. Anderson helped develop a number of electronic switching systems, including No. 2 ESS, No. 3 ESS, RSS, and currently, No. 5 ESS. Presently, he is supervisor of a software development group. His interests include real-time operating systems, programming methodologies, fault-tolerant computing, and self-checking designs. Member, IEEE.

Donald W. Brown, B.S.E.E., 1962, University of Louisville; M.S.E.E., 1964, New York University; Bell Laboratories 1962—. Mr. Brown has been engaged in the system design of proposed Signal Transfer Points for the CCIS network. Since 1976, he has worked on system and program design for the RSS. He was past supervisor of the RSS, Remote Terminal Maintenance Group and is now supervisor of the Cell Maintenance Group for the Advanced Mobile Phone Service system.

Paul N. Burgess, B.S.E.E., 1963, University of Wisconsin; MSEE, 1965, Ohio State University; Bell Laboratories, 1963—. Mr. Burgess has worked in a variety of switching development projects. He first designed maintenance circuitry for No. 5 crossbar, and participated in switching and transmission development of *PICTUREPHONE*® service for No. 5 crossbar. He then supervised groups responsible for trunk and service circuit design for No. 3 ESS, and for circuit design and system planning for the No. 10A Remote Switching System. For the latter, he participated in the development of line maintenance features and an overall transmission plan. He is now supervising a group that is responsible for peripheral circuit diagnostics for No. 5 ESS.

Kanwar J. S. Chadha, B.E. (Honors), 1967, Punjabi University; M.A.Sc. (Control Systems), 1969, University of Toronto; Ph.D. (Systems Engineering), 1973, Case Western Reserve University; Bell Laboratories, 1973—. Mr. Chadha initially worked on the development of system requirements of AMPS. He later worked on the design and implementation of the call processing software for AMPS in the mobile telephone switching office. He supervised the group responsible for designing call processing features in No. 1/1A/2B ESS for the Remote Switching System. In 1980, he was named Head of the Mobile System Software Design Department. He is currently Head, Small Business Systems Software Design Department.

John J. Driscoll, B.S.E.E., 1964, Clarkson College of Technology; M.S.E.E., 1966, Stevens Institute of Technology; Bell Laboratories, 1964—. Mr. Driscoll has been engaged in various aspects of electronic switching system development. Initially, he worked on maintenance and call processing software development for No. 2 ESS, and later he worked on exploratory studies and call processing software development for the Advanced Mobile Phone Service. He was involved with call processing and administrative software development on the No. 1 ESS and the No. 2B ESS RSS systems. Presently, he is working on No. 5 ESS performance evaluation and capacity improvement.

Laimons Freimanis, B.S.E.E., 1951, M.S.E.E., 1952, Michigan State University; Bell Laboratories, 1952–1980. Mr. Freimanis was engaged in peripheral unit development for the ESS trials at Morris, Illinois. For the No. 1 ESS, he designed the central pulse distributor, and worked on the development of the integrated circuit peripheral decoder for No. 2 ESS. In 1975, as a member of the Advanced Switching Technology Department, he was involved in exploratory studies of

line interface circuits and alerting arrangements. More recently, Mr. Freimanis had responsibility for the design and development of a floating line interface for the 10A RSS. Member, Tau Beta Pi, Eta Kappa Nu, Sigma Pi Sigma.

David R. Fuller, B.S. (Electrical Engineering), 1966, University of Wisconsin; M.S. (Electrical Engineering), 1967, University of California at Berkeley; Bell Laboratories, 1966—. At Bell Laboratories, Mr. Fuller has worked on the software and hardware design of a minicomputer-based test system for mobile telephones systems. He has also worked on crosstalk reduction and cable studies and on the design of electronic remote line concentrators. Member, Phi Eta Sigma, Tau Beta Pi.

Dennis R. Hanson, B.S., 1972, Iowa State University; M.S.E.E., 1973, University of Michigan; Bell Laboratories, 1972—. Mr. Hanson was first engaged in the development and field support of the No. 2B ESS system. More recently, he has worked on the call processing and system integration of the No. 10A Remote Switching System. He presently supervises a group responsible for the system integration of the Advanced Mobile Phone Service. Member, Phi Kappa Phi.

Charles E. Jeschke, B.S.E.E., 1966, University of Illinois, M.S.E.E., 1967, University of Michigan; Bell Laboratories 1966—. Since joining Bell Laboratories, Mr. Jeschke has been involved in the physical design of No. 101 ESS, No. 2 ESS, 3A Central Control, No. 10A RSS, and No. 5 ESS. He is currently head of the No. 5 ESS Physical Design Department. Member Eta Kappa Nu, Tau Beta Pi.

Frederick H. Keeve, B.S.E.E., 1967, M.S.E.E., 1968, University of Missouri at Rolla; Bell Laboratories, 1968—. Early in his career at Bell Laboratories, Mr. Keeve worked on the No. 1 ESS, and No. 10A RSS. Currently, he is a member of the technical staff of the Software Recovery Detection and Initialization Group.

Andrew E. Kranenborg, B.S.E., 1976, Calvin College; B.S.M.E., 1976, University of Michigan; M.S.M.E., 1977, University of Michigan; Bell Laboratories, 1977—. Mr. Kranenborg has worked on the physical design of the new remreed networks for Nos. 1, 2, and 3 ESS, including grid and frame designs and also the physical design of the No. 10A Remote Switching System. He is currently responsible for the design of software integrity monitors in the No. 5 ESS. Member, Tau Beta Pi.

Frederick M. Lax, B.S.E.E., 1974, University of Notre Dame; M.S.E.E., 1975, Massachusetts Institute of Technology; Bell Laboratories, 1974—. From 1975 to 1979, Mr. Lax was engaged in software development for No. 11A ESS call processing and No. 10A Remote Switching System (RSS) feature design. In 1979, he was named supervisor of the RSS First Application/General Availability Features Group and subsequently supervisor of the No. 5 ESS Audit Systems Group. He is presently Head of the No. 5 ESS Software Recovery Department.

Jeffrey C. Martin, B.S.E.E., 1971, M.S., (Electrical Engineering), 1972, University of Florida; Bell Laboratories, 1972—. At the beginning of Mr. Martin's Bell Laboratories career, he was engaged in software development for the No. 1 ESS input/output programs. He then worked for several years on a variety of trunk maintenance features, prior to his involvement with maintenance arrangements for the No. 10A RSS. Presently, he is a member of a group responsible for the No. 1A ESS processor maintenance development and evaluation.

Thomas L. McRoberts, B.S. (Electrical Engineering), 1965, M.S., 1968, Ph.D., 1973, Iowa State University; Bell Laboratories, 1973—. Early in his career at Bell Laboratories, Mr. McRoberts was engaged in the characterization of crosstalk coupling in digital and analog circuits. Later, he was involved in early application studies of the RSS, particularly as a pair-gain vehicle. He worked on RSS maintenance system design, including the craft TTY interface, and served as coordinator for the first RSS installation in Clarksville, New York. Presently, he is involved in maintenance design and development for the Advanced Mobile Phone Service. Member, IEEE, Phi Eta Sigma, Eta Kappa Nu, Tau Beta Pi, Phi Kappa Phi, Sigma Xi.

James L. Neigh, B.S. (Electrical Engineering), 1973, University of Pittsburgh; M.Eng. (E.E.), 1974, Cornell University; Bell Laboratories, 1973—. Mr. Neigh has participated in several studies related to transmission planning for the introduction of digital technology in the local network. He currently has responsiblity for digital transmission, synchronization, and signaling requirement in the Customer Switching Systems area.

Robert K. Nichols, B.E.E. (Electrical Engineering), 1967, M.E. (Electrical Engineering), 1969, Rensselaer Polytechnic Institute; Bell Laboratories, 1968—. Mr. Nichols has worked on circuit analysis and testing and is presently engaged in work related to digital switching systems. Member, Eta Kappa Nu.

Robert B. Schmidt, B.S.E.E., 1941, University of Illinois; M.S.E.E., 1964, Northwestern University; U.S. Army Signal Corps and Air Corps, 1941–46; Illinois Bell Telephone Co, 1946–51; Bell Laboratories, 1951–52; Illinois Bell Telephone Co., 1952–67; Bell Laboratories, 1967—. While with Illinois Bell, Mr. Schmidt was involved in Engineering of Electrical Coordination, Protection, and Transmission Maintenance of telephone plant, the design and provision of toll, special services, video and telegraph facilities, and with the preparation of the capital construction program and computerization of its administration. With Bell Laboratories in 1951–1952, he was involved with the M33 antiaircraft radar project. Since 1967, Mr. Schmidt has been involved in the LAMP and ESS loader projects. On the 10A ESS, he developed the stand-alone feature. Currently, he is involved with the *PROMUS** reprogrammer and with the No. 5 ESS projects.

D. Paul Smith, B.S. (Electrical Engineering), 1967, Brigham Young University—; M.S., 1968, Ph.D. (Electrical Engineering), 1972, Stanford University; Bell Laboratories, 1967—. Early in his career at Bell Laboratories, Mr. Smith was engaged in work involving memories and switching network for No. 2 ESS. Later, he was named supervisor of RSS Hardware Development. Currently, he is Head, Line Interface Department.

Richard G. Sparber, B.S., 1973, Union College; M.S., 1974, University of California at Berkeley; Bell Laboratories, 1973—. Mr. Sparber's early work involved transmission, signaling, and diagnostic circuits for No. 3 ESS. He is presently working on the No. 5 ESS line interface unit. Currently, Mr. Sparber holds five patents in the areas of transmission and measurement. Member, Tau Beta Pi, Sigma Xi, Eta Kappa Nu.

Thomas J. J. Starr, B.S. (Computer Engineering), 1974, M.S. (Computer Science), 1976, University of Illinois, Champaign-Urbana; Bell Laboratories, 1976—. After joining Bell Laboratories, Mr. Starr became involved in circuit design of the data link and memory for the 10A Remote Switching System. He joined the *PROMUS** unit development group in 1977. He is presently in the Advanced Switching Technology Department, concentrating on the No. 5 ESS and on combining data-voice capabilities for local switching systems.

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* Trademark of Western Electric.

Bharat S. Thakkar, B.E. (Mechanical Engineering), 1963, University of Baroda, Baroda, India; M.S. (Mechanical Engineering), 1967, Ph.D. (Mechanical Engineering), 1976, Illinois Institute of Technology; Bell Laboratories, 1977—. Prior to joining Bell Laboratories, Mr. Thakkar was engaged in product/process R&D projects for container and packaging metal working industries. At Bell Laboratories, he studied reliability aspects of No. 10A RSS, PUC/DL, PUC/DCT, *PROMUS**, and No. 5 ESS from 1977 through 1979. Simultaneously, he also investigated silicone contamination of relays used in No. 1 ESS. From 1979 through 1981, he was project leader on physical design of No. 5 ESS subsystems. Currently, he is working on assembly technologies to be used in high-density electronic packages designed for 3BX processor. Member, ASME, ASM, and SPE.

Timothy F. Wickham, B.S.E.E., 1962, Polytechnic Institute of N.Y.; M.S. (Electrical Engineering), 1964, Rutgers University; Bell Laboratories 1962—. Mr. Wickham worked on the initial call processing design of the No. 1 ESS. From 1971 to 1976, he supervised the development of major call processing additions to the No. 1 ESS including CAMA, 2/4 wire local toll capability, and various centrex features. In 1977, he assumed responsibility for the call processing development of the 10A RSS. Mr. Wickham currently supervises a group responsible for the system performance and integrity of the 1/1A ESS. Member IEEE, Eta Kappa Nu, Tau Beta Pi, Sigma Ki.

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