

MICROCOMPUTER DIGEST

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NATIONAL'S NEW SINGLE CHIP 16-BIT CPU

Industry's first 16-bit, single-chip micro-processor has been announced by National Semiconductor of Santa Clara, CA. Called PACE (for Processing And Control Element), the new low-cost microprocessor provides all of the advantages of a 16-bit instruction set and 16-bit address processing. The devices offer the option of either an 8-bit or 16-bit data processing on a single, monolithic chip.

Included on the CPU chip are all control logic, a stack, 4 accumulators, and interrupt control circuitry. By using a single chip, support components were reduced to simply a clock driver and some buffering circuits.

The general purpose microprocessor has a typical instruction time of 10 us and provides the user with a compact instruction set of 45 instruction types (or 337 individual instructions). National says the CPU is powerful enough to allow considerably more efficient program coding than most microprocessors today and compares favorably with many minicomputers.

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INSIDE THIS ISSUE

TEXAS INSTRUMENTS announces second family of microcomputers. Story on page 4.

4K RAM RACE continues as several companies announce 16 and 18-pin versions. Story on page 6.

FROST & SULLIVAN study concludes microcomputer sales to reach \$877 million by 1983. Story on page 13.

COURSES--Upcoming Microcomputer Courses and Seminars for Jan., Feb., March and April on page 16.

SMS INTRODUCES BIPOLAR MICROCONTROLLER

Scientific Micro Systems, Inc. of Mt. View, CA has announced they have completed development of a microcomputer system that they say is 10 to 20 times faster than any microcomputer now on the market. Preliminary applications of the "MicroController" system will be in controlling industrial machinery and processes, instrument systems, and computer peripherals. Other uses will be in the data communications and telecommunications fields for data switching and concentration.

James H. Geers, SMS vice-president of marketing, said the MicroController can execute a complete instruction in 300 ns. Each system includes a central processor, ROM, PROM, RAM memory and direct register input/output interface with variable field address capability.

Program storage for the first four MicroController systems varies from 512 to 4096 16-bit words, and input/output ranges from 32 to 224 points. Read/write data storage, called "Working Storage", is available as a 256-byte option.

(cont'd on page 4)

ROCKWELL CANCELS SOS μ C

Rockwell International Corp. has shelved their commercial SOS device activity resulting in General Automation scrubbing its new generation of microcomputers. GA had depended on Rockwell to deliver silicon-on-sapphire microprocessor ships for its LSI 12/16 and LSI 16 minicomputers.

GA, in a letter to customers, said it may take six months to a year to find an LSI alternate to the SOS microcomputer.

(cont'd on page 3)



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READER'S FORUM:

uC: HISTORY'S FULCRUM?

Sir

I recently attended a large microprocessor conference and was appalled at the attitudes reflected in the presentations made by representative of the semiconductor industry. I do not wish to belittle the professionalism of the speakers, nor do I wish to minimize the importance of the development of the microprocessor. I do wish to let these people know that the zeal they display for their product makes them appear arrogant and insensitive to the needs of their potential customers.

Specifically:

- *The microprocessor is not the single most important development in the history of mankind.
- *The microprocessor and associated electronics are not the single items on the critical path of an overall development program.
- *The average I.Q. of an engineer is not below 100, and he should be able to learn to use software if it is properly documented and decent training courses are offered.
- *Reliability issues cannot be dismissed on the simple premise that one device replaces many devices - in reality several state of the art devices replace proven products.
- *Not all users need to buy more capability than a task requires to accommodate future product enhancements which may serve to obsolete the original product.

If microprocessors are to produce the anticipated benefits, it will take a concerted effort on the part of both customer and vendor. What we need is a meaningful communication and not the platitudinous ponderosities (in these days of sexual equality we can no longer call them motherhood statements) we are hearing.

Neil Kleinman
Electronic Memories & Magnetics Corporation



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NATIONAL'S NEW SINGLE CHIP 16-BIT CPU

(from page 1)

Because PACE can operate on either 8- or 16-bit data, the designer can avoid the double precision software operations and the extra hardware required when an 8-bit processor is used in 16-bit applications and he can avoid the byte packing required when a 16-bit processor is used in an 8-bit application.

National chose the P-channel silicon gate process for PACE because it not only meets speed and density requirements, but P-channel is a highly predictable and well-established process that has been used successfully on a number of products of comparable complexity. An additional factor is that the P-channel requires only two standard power supplies, +5V and +12V, instead of three for the N-channel, +5V, +12V, and -9V.

National reports that the 10 us instruction execution time, the 16-bit word length, efficient architecture, and powerful instruction set gives PACE a throughput that rivals or surpasses announced N-channel microprocessor products, even though some have minimum instruction execution times as low as 2 us.

Another major feature of PACE is its internal multi-level priority interrupt system. National says PACE's interrupt system can save considerable hardware and software in applications where alarm or transient conditions must be serviced immediately, such as in automobile, process and machine tool controls. They eliminate the program overhead and performance penalties associated with software-pollled processor systems.

Since PACE is highly compatible with the IMP-16 series introduced by National last year, a designer can work with both processors and still have common software and peripheral hardware. National claims PACE is the most powerful and cost-effective processor ever offered on a single chip. They say it represents a substantial advance in microprocessor technology and should be the answer to requirements for a powerful, yet compact microprocessor.

PACE has reduced costs not only because it integrates into one chip the five MOS/LSI cir-

cuits used in the IMP-16, but also because it integrates into the same chip most of the functions that were performed with TTL circuits in the IMP-16 system. Functions include control flags, the jump condition multiplexer, multi-level interrupts, and the multi-phase clock generator.

The compatibility of the microprogrammable multi-chip IMP-16 and the single chip PACE microprocessor allows the choice of multi-chip flexibility or single-chip economy and the ability to switch from one to the other without the need for software or hardware redesign.

The new PACE chip is priced at \$161 in 100-up quantities. Sample units will be available to users for sampling during the first quarter of 1975.

ROCKWELL CANCELS SOS uC

(from page 1)

Although they had discontinued all commercial work, Rockwell says they will continue to develop the SOS technology for the military market. Donn L. Williams, president of Rockwell's electronics operations, said the commercial projects were stopped as "other projects have to take higher priority."

It has been reported for the past six months that Rockwell was experiencing yield difficulties. Another supplier for the SOS circuit, a small unnamed spinoff from Rockwell, is also experiencing the same yield problems. The company, however, plans to continue to develop the microprocessor in order to improve process and yield problems.

Fortunately, General Automation did not cast all her eggs into one nest. GA had begun a parallel operation several months back for a substitute CPU for the LSI 12/16 computer. The CPU uses high speed MSI TTL technology and has the same identical logic as its SOS counterpart. But, it still may take six months to a year before GA can begin shipments.

Despite uncertainties of the SOS future, responses from other SOS and MOS manufacturers indicate they believe SOS, in time, will become a very productive process. However, the technology is not feasible for all circuits and probably will never capture more than 10 per cent of the MOS market.



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SMS INTRODUCES BIPOLAR MICROCONTROLLER

(from page 1)

Supplementing the MicroController system are the SMS MicroController Simulator (MCSIM) and the SMS MicroController Machine Compiler (MCMAC). MCSIM is a real-time, on-line replica of the MicroController system with front panel controls for program modification and program control during de-bugging. Like the MicroController, the MCSIM plugs into the user's system and has an identical input/output structure. MCMAC, a symbolic program language, enables programming with an assembler level instruction set and generates the software needed to create firmware for the MicroController system.

Geers emphasized that the MicroController combines the speed inherent in the bipolar Schottky process with a highly efficient input/output architecture. The result, he says, is a microcomputer performance/cost ratio that far exceeds that of other available systems.

"The MicroController system presents a formidable performance/cost challenge to minicomputer manufacturers attempting to penetrate the microcomputer market; the same applies to semiconductor manufacturers who offer sets of LSI devices, but leave microcomputer implementation to their customers," added Geers.

SMS entered the emerging microcomputer market in 1970 by combining LSI technology with innovative computer architecture. The company concentrated its early effort on designing and developing advanced LSI semiconductor components and introduced the first bipolar Schottky 4096-bit ROM and 256-bit RAM devices.

It subsequently introduced the ROM Simulator, its first microsystem, which simulates most ROM and PROM devices on the market.

In quantities of 100, the price of the MicroController ranges for \$370 to \$1460, depending on size. MicroController system prototypes along with MCSIM and MCMAC are currently available and production quantities will be ready early in 1975.

#

Ed's Note: Six month subscriptions are now beginning to expire. Please check to make sure you have renewed yours!

TECHNOLOGY:

TI DELIVERS ENCORE AFTER BIPOLAR μ C

Not content with just one family of microprocessors, Texas Instruments has announced another family of microcomputers for the lower end of the performance scale.

The p-channel MOS system construction set is comparable to Intel's 4004; however, the chip architecture should undercut system cost. The microprocessor chip ALU contains a 256-bit RAM for data storage and an 8,192-bit ROM for program storage.

The microcomputer will offer a wide range of applications including appliance controls, point-of-sale terminals, flow meters, automotive control instruments, consumer arcade games, intelligent instruments, telephone dialers, and controllers for serial or parallel printers.

Instruction execution time is 12 μ s and the 8K ROM will accept up to 1,024 8-bit instructions. TI has a basic instruction set of 43 instructions that provides conditional branching capabilities and one level of subroutine nesting.

TI is currently using the microprocessor in TI's own SR-16 slide rule calculator. Prices for the TMS 1000 start at \$20 and range down to \$10 in 10,000 piece quantities.

ENGLAND ANNOUNCES TWO CHIPPER

Advance Electronics Ltd., England, has announced a two chip microcomputer system aimed at the POS, process/machine control, and business machine market.

Spokesmen for the company said the new system was not the fastest, or the biggest, but that Advance felt it was the least expensive microprocessor available.

The system is based on two devices that the company had previously designed for its calculator line three years ago.

The microcomputer has a powerful instruction set, 384 instructions. Advance said the addition of two 16-digit numbers can be accomplished within one instruction.

Advance is also studying designs for microprocessor usage in taximeters, computer term-

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inals, electronic cash registers, price-computing weighing machines, liquid dispensing/pricing machines and money changers.

The chips are being manufactured by General Instrument's Glenrothes, Scotland plant. Advance guarantees to supply devices programmed to users' specific requirements within six months after receipt of an order.

JAPAN ENTERS 16-BIT UC FOR HOME MARKET

Nippon Electric Co. of Tokyo, Japan has introduced a 16-bit n-channel, silicon gate MOS microcomputer with an instruction-execution time of 1 us.

The microcomputer, Model Mucom-16, will be initially used for minicomputer emulators and data terminals.

The 6-chip system consists of one control chip, an arithmetic/logic and register chip (RALU), and four 1024 x 8 ROM chips.

Features include direct memory addressing up to 64 words, wide range mapping capability, multiprocessor capability, 15 general purpose registers, status register, interrupt capabilities, TTL-compatible interface and power supplies of +12 V, +5 V and -5 V.

The system is presently available in sample quantities as \$1000 each. Quantity production is scheduled for the first quarter and sources say NEC is interested in the overseas market, but that no plans have yet been established.

MICROCOMPUTER-BASED PRODUCTS:

NEW NORWEGIAN FIRM ENTERS μ C MARKET

Data Industri, a newly formed Norwegian company, has started assigning, manufacturing, and selling a new microcomputer system based on Intel's 8080 system. Called MYCRO-1, the microcomputer system consists of a series of modules starting with a DIM-1001 processor module which combines an 8080, teletype, asynchronous interface, 2K byte PROM, 2K byte ROM and 1K byte RAM on a single 16 x 23 cm card.

The Oslo based company has developed a one-pass assembler which processes the standard Intel assembly language source format residing in PROMs in less than 3K bytes. The assembler is interactive and makes it possible for the user to program the MYCRO-1 RAM memory without any intermediate state of paper tape.

The company also plans to market a memory

module with sockets for relocatable ROM library programs, making their use in the low-cost mask program ROM memories feasible for the first time. The company reports that a number of systems have already been delivered.

MICROCOMPUTER DIGEST will feature the MYCRO-1 in an upcoming issue.

TTL & MOS JOIN HANDS IN NEW YORK

A new CRT terminal for use in hotel/motel environments has been unveiled at the recently held Hotel/Motel Exposition held in New York.

The intelligent peripheral contains three separate logic processors. An Intel 8008 is the host microcomputer, while two TTL/MSI outboard processors perform high speed general I/O functions such as disc or tape storage, display operations and keyboard monitoring.

The outboard processors have a much simpler instruction set than the 8008 and are responsible for basic operations like arithmetic, loading and storing, bit rotation, and jump return after task completion.

The system has 16K RAM memory and can be user programmed. The outboard processors access 8008 memory by "cycle stealing". Thus the microcomputer will never be loaded down more than 10 per cent of the time.

The new terminal will be used by NCR in its hotel reservation system. Applications also include inventory, ticketing, sales and typesetting.

The OP-1 terminal system is priced at \$2,285 in 100 quantities. Delivery is 90 to 120 days ARO.

MICROTROL--HEART OF CONTROL SYSTEM

A new customized process control system has been introduced by Avco's Systems division. At the heart of the new Microtrol system will be Digital Equipment Corp.'s line of MPS microcomputers and software.

Microcomputers were chosen so that customers could automate their plants one step at a time. As customers gain confidence, they can easily expand their system.

The system allows stand-alone control of each process and several systems can be linked to a single PDP-11/45 minicomputer. The soft-

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ware used for the system will be the same as that used in Avco's Avmots line of automatic test systems.

It is estimated by the company that the Microtrol line could yield \$10 million by 1978. According to L. Everett Karels, manager of automatic test and control systems, the present market for digital control equipment for the process control industry exceeds \$1 billion with a large growth predicted for the next 10 years.

SUPERMARKET CHAIN CHOOSES DATACHECKER

Fazio's Supermarket has opened a 36,000 square foot store in Fountain Valley, CA. The addition, Fazio's first store on the west coast, is equipped with a 12-terminal Data-checker checkout system.

Pete Sodini, Administrative vice president for the chain, disclosed that "because it was our first totally new store in the area, we felt the time was right to install electronic checkout." He added that they chose the Data-checker system since it was "best suited to the needs of this marketing area. It supplies the scheduling and record-keeping capabilities we were looking for, and it has front-end capabilities compatible with a bulk produce operation."

National Semiconductor Corp. of Santa Clara, CA manufactures the Datachecker, a microcomputer-based POS system for supermarkets.

CARD DATA PROCESSOR GAINS UC

The new Series 8000 intelligent card reader uses an internal microprocessor to initiate subsequent actions once the unit reads optically marked cards.

The reader, manufactured by Bourns Management Systems, edits on or off line into stackers under microprocessor command, or external program control.

The microprocessor controls character suppression, accuracy checks and card classification based on program card and output formatting. Both sides of the card are read and stored in a 160-character buffer.

Prices begin at \$6,500 with delivery in 60 days.

COMPANY'S 1ST UC PERIPHERAL

Interdata Corp. has announced their second peripheral product, a microprocessor controlled computer-output printer. The company plans to introduce the printer for the OEM market this month.

The microprocessor is built into the controller and is used to control the printing element, monitor communication lines, and control transfer to and from the computer memory. A stepping motor is used instead of a servo to drive the printing element. Interdata says the new printer design will reduce misalignment and character blurring caused by recent servo-controller designs.

OPTICAL READER CAN VERIFY PAGE

A new optical page reader manufactured by Datatype Corp. is being offered with or without a microprocessor. The Model 500 uses a microprocessor to provide flexibility and reread typed lines to correct for parity errors that exist on the OCR document.

The reader also features 110 chars/sec reading speed, no mechanical adjustments, two electronic adjustments, front-of-unit paper-return, and has no mechanical clutches or brakes for advancing the paper through the machines.

MEMORIES AND PERIPHERALS:

PACKAGE PIN DUEL MOUNTS

Motorola and Intel have both recently announced they will second source Mostek's 16-pin 4K RAM, making it as a possible industry standard.

Intel is expected to begin prototype production in this quarter with full production sometime next quarter. Motorola is also planning to be in full production of the NMOS memory device by June.

Until recently, Mostek had been the only company producing the 16-pin device. With the two second source announcements, the 16-pin 4K RAM could be an industry standard shortly.

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Further proof is a recent contract in which National Cash Register (NCR) selected Mostek's 16-pin device for use in future systems. Donald E. Eckdahl, vice president for manufacturing operations for NCR, confirmed the contract, but declined to comment on the amount of units or price agreed upon. He also declined to comment on which NCR facility would incorporate the 4K RAMs.

Mostek officials said the increased savings in space provided by the 16-pin device over the 22-pin unit can amount to as much as 56 to 80 per cent savings in printed-circuit board space.

Mostek did reveal that they were experiencing some yield difficulties, but that they were continuing engineering efforts. L. J. Sevin, Mostek president, said that he does not believe the yield problem will last longer than a few months. He indicated that major expansion of the 4K RAM market will be shifted from mid-1975 to 1976.

On another front, National Semiconductor has launched itself into the middle of the 4K RAM race by introducing both a 22-pin and an 18-pin version. National has chosen the 18-pin package over the 16-pin as it "offers both good board density and high speed without needing the multiplexing circuitry required of 16-pin packages."

Not to be left behind, Texas Instruments has confirmed that they will also market two versions of the 18-pin 4K RAM. Sources say their memory circuit would be rated at guaranteed maximum access time of 200 ns and maximum cycle time of 400 ns. TI claims the 18-pin package will offer 70 to 100 per cent better board density than the 22-pin circuit.

EM&M AND GI ANNOUNCE 2ND SOURCE PACT

Electronic Memories & Magnetics and General Instruments have announced a cross-licensing agreement for N/MOS semiconductor parts.

GI will second-source four of EM&M's 1K static RAMs and their new 4K static RAM. EM&M will in turn second-source GI's GIANT-II line of five static ROMs and RAMs. The agreement also included GI products still under development, such as a 16K static ROM, character generators and a single chip microprocessor.

The companies felt the benefit of second-

sourcing would be an attractive feature for potential customers. Each company will provide the other with masks, process technology and test information for the devices.

MOTOROLA'S NEW 64 x 4 RAM

Motorola Semiconductor has announced a new static 64 x 4 CMOS RAM, the MCM14552. Three chip-enable inputs allow the RAM to be expanded into a 2048-bit memory system with no additional address decoding.

Tri-state outputs permit bus-organized operation; in addition, on-chip output data latches can be used to hold data during a write mode. Under static operation, the MCM 14552 may be controlled by dc levels with no maximum pulse width restrictions. Also quiescent power dissipation (typically 10 uW/package @ $V_{DD} = 10V$) is low enough to consider these devices for use in long term, battery-backed, non-volatile RAM systems. Due to the static operating characteristics, the need for refresh circuitry is not required, resulting in a simple RAM system design.

Access time, during a read operation, is typically 700 ns. The RAM is housed in a 24-pin DIP and is currently available. Single unit prices begin at \$29.

RCA INTRODUCES FIRST NMOS RAM

The latest entry in the NMOS semiconductor memory market is RCA's high speed 1024 x 1 static RAM, the MW7001ID.

Features of the LSI device include a 60 ns max. access time, 180 ns max. cycle time, TTL-compatible inputs, 0.5 uW/bit max. standby power dissipation, 640 uW/bit max. operating power dissipation and a ceramic, hermetic 22-lead DIP.

The 1024 RAM is the first in a series of solid state NMOS memories to be introduced by RCA. The next device will be a 4096-bit dynamic RAM which is expected sometime early in 1975.

The MW7001ID is available from stock at both the RCA Solid State Division in Somerville, NJ and its distributors. It is priced at \$10.50 each for quantities of 1,000.



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HIGH PERFORMANCE RAM FAMILY UNVEILED

A new family of modular and high-performance n-channel static RAMs has been introduced by Intel Corp. Totalling 21 new types of 2101, 2111, 2112, and 2102A series of silicon-gate n-channel MOS static RAM circuits, the introductions expand the popular 2102 1K static RAM series into the industry's first complete family of 256 x 4 and 1024 x 1 TTL-compatible static MOS RAMs.

All the RAMs use a single +5 volt supply and operate at TTL logic levels, have tri-state outputs and are fully static.

Including the 2102 series, the family now comprises 24 types in four configurations and seven speed ranges. Intel plans to announce further additions to the family soon.

The 256 x 4 devices are more applicable to small systems and modularly expandable memory organizations than the 2102's standard 1K configuration. They are available in the same speed ranges as the 2102; 500 ns, 650 ns and 1 μ s. Those speeds are for both maximum access time and minimum cycle time, which are identical in 2102-class RAMs, and are specified as worst-case over the 0° to 70° temperature range. Typical power dissipation is 150 mw.

The 2102A series retains the standard 1K configuration, that is, it has 16 pins, separate input data and output data lines, and one chip-enable input, as well as address and read/write control inputs.

The three new 256 x 4 devices include the 2101, which is a 22-pin RAM with separate input and output data lines (four each), output disable and two chip-enable inputs. The 2111 has 18 pins, with four common I/O lines, output disable and two chip-enable inputs. The 2112 RAM has 16 pins with four common I/O lines and one chip-enable input.

The output disable function is used to control the state of a common I/O bus. It makes the use of bidirectional logic unnecessary in common I/O system buses. The 2102 may be used with either independent or common I/O buses, while the 2111 and 2112 are designed primarily for use in higher-density, common I/O memory systems.

The 256 x 4 configurations minimize package

counts at system or module storage capacities of 256 or 512 words, while the standard 1K configuration minimizes package counts only at 1024 words.

Since small modules are rarely practical with 1024 x 1 RAMs, the 256 x 4 configuration is expected to prompt the development of incrementally expandable memory systems for product lines requiring a variety of memory capacities. Such products include TTL-based data terminals, portable data-collection recorders, industrial controls, microcomputer systems, programmable calculators, business machines and other small systems.

One major 2101 application will be "add-on" modules providing intermediate storage capacities in 2102-based memory systems. For example, the 2102 may be used to minimize cost and maximize storage density of 1024-word modules while the 2101 minimizes package counts and, thus, costs of 256-word or 512-word modules.

As a result, system capacities such as 1-1/4 kilowords or 2-1/2 kilowords can be built at optimum costs and density. The 2102 and 2101 RAMs can both be connected to the same buses since both have independent I/O lines. Also, the 2101's logical controls minimize the amount of system logic required to select add-on modules.

The new family devices are now in stock at Intel distributors and prices begin at \$7.45 in 100-up quantities. Special speed selections can also be ordered from Intel.

1ST QUARTER--1K RAM TARGET DATE

A 1K silicon-on-sapphire RAM will be introduced by RCA's Solid State division early in 1975. The new device's design has been predicated on trade-offs involving speed, power, ease of use, and chip size. Trade-off decisions resulted in a RAM requiring only a single power supply and a chip select input that may also be used as an additional address to accommodate memory expansion.

To increase speed, the chip has nine address lines to address two cells, one from each of two 512-word blocks. The tenth address selects the desired block. This row decoded, therefore, is only one of 16 rather than the conventional one of 32.

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Access time will be approximately 120 ns at 10 V, with cycle times of 150 ns. Operating dissipation will be about 20 mw at 1 MHz and 10 V.

First samples of the device are expected in February with production quantities to be stocked during the third quarter of 1975.

MCM UPGRADES TEST CENTER

The Electronic Test Center Division of MCM Industries has upgraded its semiconductor environmental testing capability with the purchase of a Sentry 610 test system from the System Technology Division of Fairchild Camera & Instrument Corp.

The Sentry 610 will perform high-speed tests on gates, flip-flops, shift registers, RAMs, ROMs, calculator chips, microprocessors and other custom bipolar and MOS products for MCM customers.

The four-year old Electronic Test Center Division of MCM Industries operates test laboratories in Anaheim and Santa Clara, CA and in Waltham, MA.

BIPOLAR MEMORY LINE GAINS TWO UNITS

National Semiconductor has announced two additions to its line of bipolar memories for use with microprogramming and code converter applications. The new items--the DM7577/DM8577 and DM7578/DM8578 are field-programmable, 256-bit read-only memories.

Both units are identical except the DM8577 has open-collector outputs, while the DM8578 has Tri-State outputs. They are organized as 8-bit words, and have fully-decoded buffered inputs with easily expandable outputs, are pin compatible with the SN 74188A and with most other TTL and DTL circuits and have access times of 50 ns.

The PROMs are electronically programmable for use in custom and prototype memory applications to determine a suitable memory pattern. The PROMs are available in 16-pin packages and prices begin at \$6.70 in lots of 100.

###

Ed's Note: Six month subscriptions are now beginning to expire. Please make sure you have reviewed yours.

ONE MICRO UNDER GLASS, PLEASE!

A totally new look in tie tacks and cuff-links is now available from Xenia. They're using microprocessor chips mounted behind clear lenses and black chrome-plated brass cases set off the intricate silicon chip with its gold leads. The chip tacks and cuff-links are designed especially for engineers, salesmen and executives in the electronic industries as well as for students and professionals in related fields.

Available separately or as a matched set the cuff-links sell for \$11.90, and the tie tacks for \$5.95. The entire set is priced at \$16.00. Quantity discounts are available to companies for promotion uses. The jewelry is not limited to microprocessor ships but can be made with most microcircuits.

4096 BITS IN AN 18-LEAD PACKAGE

National Semiconductor has entered the 4K RAM marketplace with its MM5270 Read/Write memory that has a unique design concept called Tri-Share which allows a single lead to serve as Read/Write, Logical Chip Select and V_{CC} , and another lead is a common input/output lead.

The combination of Tri-Share design with a single I/O lead reduces the package lead count for 4096-bits of memory from 22 leads (which is what most users have had to deal with) to only 18 leads on the MM5270.

The MM5270 thus allows users to achieve a PC-card memory density nearly twice as great as that possible with 22 lead 4K RAMs.

The new 4096 x 1 RAM is fully decoded, and uses n-channel silicon gate technology. The MM5270 also features TTL-compatible inputs (except for Chip Enable) and on-chip registers for address and Chip Select. Access time is 200 ns, and cycle time is 400 ns.

The new RAM will be available in production quantities by mid-1975, in both ceramic and molded DIPs.

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Ed's Note: The staff of MICROCOMPUTER DIGEST is most interested in your views and opinions. We welcome all comments. Address your letter to the Reader's Forum Department.



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MANNY LEMAS, Applications Technical Advisor.

DRO AVAILABLE WITH μ C TESTER

A new Digital Readout Option (DRO) has been announced by the Systems Technology Division of Fairchild Camera & Instrument Corp. for its Qualifier 901 integrated-circuit test system.

The DRO measures voltage and current and then displays failed test parameters on a 3-1/2 inch display panel meter after measurement mode, range, and device pin selections have been made. The system uses a microprocessor to automatically identify the bias (VCC) pin, ground pin, and input/output pins of the Device Under Test (DUT).

When a DUT fails in the normal Stop-On-Fail mode of the tester, the operator dials the failing pin number, and the measurement mode and range to obtain the digitized voltage or current measurement.

The Qualifier option is capable of monitoring the internal DC power supplies used to provide current analog reference and pin-driver circuitry of the system. The option does not inhibit test speed when the tester is operating in normal high throughput modes.

SIGNETICS ADDS 2K & 4K PROM TO LINE

Two high speed bipolar PROMs have been designed and developed by Signetics Corp. One, the Model 82S114, is a 2,048 PROM organized into 256 x 8 words, and the other, the Model 82S115, is a 4096-bit PROM organized into 512 x 8 words.

Both devices are field-programmable and are suitable for use in bus-organized data systems. Applications include microprograms, hardware algorithms, character generation, control store, and sequential control.

Other features include buffered address lines, on-chip decoding, on-chip storage latches, tri-state outputs, and input current less than 100 μ A.

The PROMs are Shottky diode-clamped and incorporate data output registers on their chips. A D-type latch is used to enable the tri-state output drivers.

In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while the strobe line is held high. In this mode, the bit drivers are

controlled solely by two chip-enable lines.

The Latched Read mode begins with an application of the desired address and an enabling of both chip enable lines. Data then enters the output latches after the positive transition of the strobe line.

The data lines are locked into their last valid state, following the negative transition of the strobe. The latches remain set and the outputs are enabled until the chip is disabled and the strobe is brought high.

Large quantities of the new PROMs are now available from the Signetics Bipolar Memories Division and from franchised distributors. When ordered in lots of 100, the PROMs sell for \$65 each. Factory programming is available at \$12/pattern and 50¢/PROM.

PEOPLE, LITERATURE AND EVENTS:

TELECOM HIGHLIGHTS MICROS

Microprocessors gained the spotlight at last month's IEEE's National Telecommunications Conference in San Diego, CA.

Users stated that the transition to micros was not always easy. They felt that one had to be well prepared and realize that every microprocessor's architecture, software and I/O is unique. This meant each user must carefully examine each model and undergo a substantial self-teaching effort, especially for newly-introduced microprocessors in which software and hardware support was lacking.

Attendees at the meeting were told that they would realize circuit requirements with few microprocessor chips, and that design changes were a factor of reprogramming one's ROMs. Hardware design efforts would mostly involve interfacing.

Exhibits included modems and Caesar Castro of the Naval Electronics Laboratory Center in San Diego gave a presentation of high speed microprocessors for real-time processing of communication data.

SYMPOSIUM SLATED FOR APRIL

The "1975 International Symposium on Military and Industrial Microprocessor Systems" will be sponsored by AH Systems. Held at the
(cont'd next page)



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new Marriott Hotel at the Los Angeles International Airport, the symposium will run from April 29 to May 1, 1975.

The symposium will host key speakers from major microprocessor manufacturers, support service companies, and AH Systems Technical staff. The moderator for the conference is Dr. Gary Nelson of AH Systems.

The program's 18 sessions will include descriptions of current LSI microprocessors, projections for the technological and economic environment for the 1980's, and analysis of technological development. Systems architectures, software, reliability and design will be featured along with tutorial sessions on comparisons of microprocessor chip sets in systems, radiation hardening of microprocessors, and benchmark programming.

The registration fee for the three day symposium is \$395. Further information can be obtained by contacting Art Cohen, vice president/director of programs, AH Systems, Inc.

FIRST MICROPROCESSOR CONFERENCE

Nearly 175 participants from the United States and abroad heard 15 speakers consider the economics, applications, and technology of microprocessors at the First National Microprocessor Conference held on December 2 and 3 at the Sheraton in Boston, MA. Sponsored by Arthur D. Little, Inc., a research and consulting firm, presentations were combined with discussions in which speakers and conference attendees exchanged views on the potential of microprocessors.

Underlying the conference was the question of the current economic recession's impact on the microprocessor market. But the overall consensus indicated a growing number of small volume customers well into next year. Lincoln Young, marketing manager at Motorola, estimates that by 1980 there will be 16 million microcomputers in use. He broke the number down to 4.8 million in computers, 8.4 million in industry, 2 million in consumer products and 1 million in Federal systems.

Norman Zimbel, a consultant for ADL and conference co-moderator, said the next five years should see a tremendous growth with a total market value of between \$280 million and \$475 million.

Young sees 80 to 90 per cent of the market to be composed of chip sets rather than individual devices. The future should see larger, more cost effective packages of standard building blocks.

David F. Millet, also of ADL, looks for more effective I/O devices which will accept and enter data with timing and levels matched to the requirements of the CPU. He sees the present number of support chips used as a hindrance in keeping the cost of microcomputer based products down.

In opening the conference, Zimbel said, "The application of microprocessor technology represents an evolutionary development for the computer industry and a revolutionary development for other classes of products." He said that the market for microcomputer components could grow over \$280 million by the end of the decade with a significant fraction of that volume being accounted for by new markets.

Several companies indicated that research and development on microprocessor products had been put aside until the present economic situation clears later this year. However, several representatives indicated that their companies were still pushing forward, as microprocessors offered the precise savings they would need to weather the business crunch. Others indicated second sourcing, software and inability of the microprocessors to handle their applications as reasons for their company's delay in entering the microcomputer market.

For some the answer was definite, while others were delaying for better economic times. But the direction is definitely positive, the microcomputer will be a leader in the seventies.

AUERBACH A LA CARTE

Auerbach Publishers Inc. is offering a new low-price computer service, Auerbach A La Carte, which allows subscribers to choose only those subjects that fit their needs. The new service will be derived from the company's Computer Technology Reports.

Four specific categories are being offered: (1) minicomputers, small business computers and intelligent terminals; (2) general purpose (cont'd next page)



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computer systems; (3) software: processing, data retrieval and monitoring; and (4) data communications and peripherals.

Prices begin at \$79.50; however, all reports are free with a one year subscription to the Auerbach Subscriber Newsletter.

TWO NEW BROCHURES OFFERED BY PCS

PCS Inc. has prepared and is now offering two free pieces of literature describing two of the company's new microcomputers.

The first, entitled "The World's First Complete Microcomputer Development System", describes the new PCS MicroPac 80, a desktop microcomputer designed to incorporate the Intel 8080 micro CPU into a complete and flexible configuration of memory and communications process input/output modules.

The second brochure, entitled "PCS Brings the Microcomputer to OEM Control Systems", describes the workings and options of the PCS MicroPac OEM, a special configuration of the MicroPac computer which is custom designed from standard off-the-shelf modules for large OEM users.

GROVE WINS J. J. EBERS AWARD

Dr. Andrew S. Grove, vice president and director of operations of Intel Corp. has won the 1974 J. J. Ebers award for his "outstanding technical contributions to electron devices."

The award, presented by the Electron Devices Group of IEEE at its recent international meeting in Washington, D.C., consists of a certificate and \$500.

Dr. Grove, fourth recipient of the award, was cited for his work in contributing to the understanding and control of the surface properties of silicon, particularly as used in MOS devices.

The award is presented in honor of the late Jewell James Ebers, a pioneer in the early development of the transistor.

Dr. Grove's most significant contribution was in the understanding and control of surface properties of silicon, which has had a major impact in the stability of MOS devices and on high-voltage bipolar devices. He also holds several patents pertaining to surface

controlled semiconductor devices and has written over 40 technical articles on semiconductor devices and technology.

Dr. Grove is a member of the group which helped found Intel Corp. in 1968. He will become executive vice president of Intel in April.

NATIONAL NAMES NEW ADMINISTRATOR

Donald J. Watson has been named Product Administrator for National Semiconductor's Datachecker microcomputer-based electronic cash registers and in-store processing system for supermarkets.

Watson comes to NS Datachecker from the Electronic Cash Register Division of Digital Computer Controls, Inc., where he was National Sales Manager and, more recently, vice president of marketing.

In the newly-created position at National, Watson will be responsible for product marketing for Datachecker's microcomputer-based multi-terminal, computer-linked system and for the T3000 series stand-alone microcomputer cash register.

INTEL TO REALIGN MANAGEMENT

A new management reshuffle proposed by Dr. Robert Noyce, president and chief executive, will promote Dr. Gordon Moore, executive vice president as the new Intel president. Dr. Noyce would become chairman, and continue to take an active management role.

Dr. Andrew Grove, operations vice president would replace Moore as executive vice president. Arthur Rock, Intel's chairman, would become vice chairman of the board of directors and chairman of the executive committee.

Dr. Noyce said the proposed shuffle was a result of "evolutionary change of management as the company is growing." Dr. Noyce said the company's earning performance was not a factor, and that earlier earning projections are still holding.

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Ed's Note: Don't miss a single exciting issue of MICROCOMPUTER DIGEST. Check to make sure you have renewed your subscription.



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FROST & SULLIVAN μ C MARKET STUDY

In 1971, the Intel Corp. introduced the world's first microprocessor chip, the gut component of a microcomputer. That event triggered what will become one of the most glamorous product areas in the annals of American industry. Already, in 1973, sales of microcomputers to the industrial market came to \$8 million, and they will multiply 100-fold, to reach \$877 million by 1983, according to projections by market research specialists, Frost & Sullivan, Inc.

The study projects that sales of microprocessor chips alone will rise from \$3.4 million in 1973 to \$406 million in 1983. Similarly, it projects that the market for microcomputer add-on memories will increase from \$2.2 million in 1973 to \$221 million by 1983; for input/output interface equipment it will soar from \$1.5 million to \$225 million. (All of these projections apply only to industrial applications, the study notes, and since they assume no technological surprises, "they are conservative.")

The industrial market--defined as those sectors which produce materials, other physical products, and also electric power--already is a heavy user of dedicated computer systems, the report acknowledges. But microcomputer technology offers the potential for "true dedicated processing--which the minicomputer has never quite realized," it says. As a result, by 1982, the dollar volume of microcomputer sales for industrial purposes will surpass that of microcomputer sales, the report concludes.

Some of the biggest microcomputer application areas will include:

- o Programmable-Controllers: "Microcomputers should move easily into this area," the report says. Another major use will be in numerical control systems.
- o Process Instrumentation: Microcomputers will become an important OEM component, especially within control mechanisms.
- o Petroleum Industry: Here, microcomputers will initially be focused on refinery operations; computerized drilling will become common by the 1980's.
- o Transportation Equipment: This category includes automotive, aerospace, and

agricultural vehicles and, taken all together, it will be the single largest industrial user of microcomputers.

- o Plastic Fabrication: Microcomputers will expedite the production of small extrusion and molding operations.

The foregoing represents only a sprinkling of application areas, and already a French company, the study has found, has become one of the world's first, and major, microsystems suppliers. It has developed a product line based on Intel's 8008 chip, and the company claims 800 installations, all in Europe. Because of the product, the firm's sales for 1974 will hit \$3 million, up from \$200,000 in 1971.

Several companies are vying for a dominant position in supplying these lucrative markets with microcomputers. In 1974, the four leading producers will account for 63% of the total market share (Intel Corp. alone captured 25%). But by 1977 and beyond, "no firm will hold more than a 20% share."

N-channel MOS technology, which is just starting to be commercialized, will dominate the microprocessor market, the study notes. This will be so despite the difficulty encountered in manufacturing n-channel chips. It is nearly 3 times as fast as p-channel technology, and will enable microprocessors to attain minicomputer speeds.

Microcomputers will be in worldwide demand. U.S. consumption, in fact, which accounted for approximately 50% of global use in 1973, will decline to a 39% share by 1979 despite a rapid absolute increase in usage. Altogether, microcomputer sales abroad, for industrial applications alone, will increase from \$2.6 million in 1974, or 14% of the total market, to \$270 million by 1983, or 30%.

RECENT LITERATURE

Improve Interrupt-Handling Capability of Microprocessor with a Few ICs

By Tom Pittman

Electronic Design, November 22, 1974

This article explains how, by adding six standard TTL ICs, the interrupt handling flaw of the 8008 microprocessor can be eliminated. The article stated that the basic problem is
(cont'd next page)



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that the microprocessor does not automatically save and later restore either the contents of the CPU registers or the condition of the status flags.

The author suggests adding two SN7489, (64-bit RAM), SN74193 (4-bit up/down counter), SN7432 (NAND gates), SN7475 (4-bit latch), SN7404 (Hex Inverter) that will provide the CPU with an external push-down or last-in, first-out stack with a total overhead time of only 480 ns.

Two "push" operations will be needed to save the processor state for an interrupt-service routine. The first saves the contents of the accumulator and status flags, the second saves half the contents of the memory-address accumulator and latched status flags in the register. To save additional registers and/or flags, additional "push" operations can be used.

To retrieve the processor state, a 16 word table translates the saved flags and register contents into the processor conditions. The table can be placed at the end of the program memory pages.

4K RAMs: Increased Densities Bring Difficult Testing Problems

James E. Fischer, Tektronix Inc.

EDN November 20, 1974

An enlightening discussion of several techniques in screening 4K RAMs. Since 4Ks are rather expensive throw-away devices, it is worth the extra effort to screen them 100 per cent.

The author described several methods for testing:

- o that each cell exists and is capable of storing both ones and zeroes,
- o sense amplifiers for capability of shifting to opposite data state after a long series of like data,
- o volatility,
- o internal address multiplexing (16-pin devices),
- o split cycle timing,
- o tri-state conditions,
- o dc parameters: IOL, IOH, input leakage, breakdown, power dissipation, etc.

Since 4K RAM testing is time consuming, Fischer suggests the following sequence for maximum time utilization.

First tests are dc, followed by functional verifications that all cells can store ones and zeroes properly.

The address complement routing does not result in erroneous write recovery time.

Then verify memory operation for read cycle, write cycle and read/modify/write cycles. After this test, the RAM should undergo a volatility test.

All tests should be performed at the maximum specified temperature.

A Very Complete Chip Set Joins the Great Microprocessor Race

Robert H. Cushman, Special Features Editor

EDN November 20, 1974

An excellent article describing Motorola's first entry into the microcomputer arena. Although the M6800 runs about half the speed of the Intel 8080, benchmark programs revealed that they were running neck to neck in program execution time. Under favorable conditions, the M6800 was decisively faster. The M6800 will be complimented by a large family of support chips to make it adaptable to numerous applications.

An excellent description of the M6800 family is presented. The article is highly recommended for those interested in Motorola's venture, or thought that all you had to know about microcomputers was Intel.

Comm Systems In 1980 Will Provide "Smart" Functions in Every Terminal

George King, Western Editor

Digital Design November 1974

This article is a description of present day use of microprocessors in communication systems and probable evolution paths to the end of this decade. Contending MOS to be the leader in LSI technology today, it is reported that 1980 could see bipolar LSI and CCD devices as the foremost running semiconductor technology.

AH System's Vice President, H. Dean McKay sees "That within ten years, an entire communication system will consist of a single LSI chip and a keyboard."

Forecasts for 1980 show a phase-out for PMOS and TTL but large production quantities for I²L and CCD. Chip sizes will range upward to 500 mils. (cont'd next page)



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As microprocessors infiltrate communication systems, they, along with associated memories, will be located at the user's end of the system.

Several typical applications are discussed along with device descriptions and what to expect in a microcomputer.

Brake Tester Takes Microprocessor for a Ride
Walt Palstone, Managing Editor
EDN November 20, 1974

A report from GM on microprocessor usage in testing automobile braking. GM engineers have upgraded their brake testing instrumentation as a result of the U.S. government federal Motor Vehicle Safety Standard 105. This measure specifies rigid standards of braking efforts from minimum distant stops to spikes or panic stops. Tests must be monitored and records taken to include data on brake fade and recover.

The basis of the system is an Intel MCS-4 microcomputer. The instrument controls the sequential operation of the test, records, and then processes data. A digital display mounted on the dashboard provides the driver/operator with real time information. Two hardcopy data outputs are used, a digital printer and chart recorder.

The test system basically recognizes when the system is ready to go, executes braking sequence, controls the procedure, records test parameters and then processes data for output.

An excellent article describing an Intel 4-bit microcomputer application.

Microprocessors and Microcomputers: What Will the Future Bring?
Jerry Weth, EDN Research and Roy Forsberg, Editor
EDN November 20, 1974

A summary of the report conducted by Cahners Research and Creative Strategies to determine who is using microprocessors, how and what they are expecting to receive.

The basic conclusion of the report is "microprocessors will be used by nearly everyone. Moreover, they'll be used, or at least have the potential to be used, in nearly every electronic design application. In addition, 40% of the applications involve

areas not currently served by electronics. The potential for this device is staggering-- and we've just scratched the surface."

The study was taken from a survey of 1511 engineers and EDN readers. Results were tabulated by Creative Strategies. Following is a summary of the results.

- o Most survey respondents (70%) have one or two microprocessor applications under development. Within one year, up to 22% will have five or more.
- o 60% of microprocessor applications will be hardwired logic replacements. 40% will be new product applications.
- o Evaluation of memory requirements yielded two conclusions. "First, microprocessor applications will be very dedicated, thus large special-purpose instruction sets are in the planning stage. Second, many applications are in the planning stage. This latter point, coupled with hardware designer's unfamiliarity with programming results in a basic 'I don't know for sure, but I'll take a guess' approach" to future memory requirements.
- o Memory types:
 - 90% Semiconductor memory
 - 8% Core memory
 - 2% Plated wire
- o Three peripherals or input/output devices would be required.
- o 1975 should be the first year for a "wave" of microprocessor products to hit the market. Based on those surveyed, 6% now had a microprocessor product in production and 64% were planning one for introduction in the next 12 to 18 months.
- o Programming costs range between \$1000-\$5000.
- o Microprocessor characteristics considered most important:

Availability	57%
Supplier reputation	43%
Software support	37%
Size of instruction set	31%
Speed	28%
Architecture	27%
Second sources	26%
Memory size	21%
Package count	20%
Number of power supplies	16%
Power consumption	16%



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EDUCATION:January

- Arr. Motorola Microprocessors \$375
3 day course Phoenix, AZ Motorola Semiconductor
- Arr. Microprocessor Architecture: Intel
8080 New York, NY IEEE Computer Society
- Arr. Microprocessor Programming: National
IMP-16 New York, NY IEEE Computer Society
- 6- 8 Intel MCS80 Workshop \$350 Boston, MA and San Jose, CA Intel Corp.
- 7 Control Structures Palo Alto, CA SIGPLAN
- 7- 9 Microprocessors/Microcomputers \$410
Washington, DC Integrated Computer Systems, Inc.
- 7-10 Minicomputers/Microcomputers \$425
Zurich, Switzerland Integrated Computer Systems, Inc.
- 8-10 Microprocessors and Systems Applications
\$350 Bridgeport, CN Automata Information Services
- 13 Designing with Microcomputers Univ.
of Santa Clara Santa Clara, CA
- 13 Microprocessor Software Univ. of
Santa Clara Santa Clara, CA
- 13-15 Microprocessor Product Survey \$395
Washington, DC Microcomputer Technique, Inc.
- 13-15 Intel PL/M Workshop \$395 Boston, MA
and San Jose, CA Intel Corp.
- 14-17 Minicomputers/Microcomputers \$425
Orlando, FL Integrated Computer Systems Inc.
- 15-17 Microprocessors/Microcomputers \$410
Salt Lake City, UT Integrated Computer Systems, Inc.

- 15-17 Microprocessor Product Survey \$395
Anaheim, CA Microcomputer Technique Inc.
- 20-22 Second Annual Symposium on Computer
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- 20-22 How to Design Systems with Micro-
Processors \$425 Washington, DC and
Anaheim, CA Microcomputer Technique Inc.
- 20-22 Intel MCS40 Workshop \$350 Boston, MA
and San Jose, CA Intel Corp.
- 22-24 Microprocessors/Microcomputers \$410
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- 22-24 Microprocessors and Systems Applica-
tions \$350 Syracuse, NY Automata Information Services
- 23-24 How to Program Microprocessors \$275
Washington, DC Microcomputer Technique Inc.
- 23-25 How to Program Microprocessors \$275
Anaheim, CA Microcomputer Technique Inc.
- 27-29 Micro, Mini & Midicomputer Systems
Structure, Implementation and Application
San Francisco, CA AIIE Seminars
- 28-30 Microprocessors/Microcomputers \$410
Ottawa, Ontario Integrated Computer Systems, Inc.
- 28-31 Minicomputers/Microcomputers \$425
Washington, DC Integrated Computer Systems, Inc.
- 28-31 Minicomputers/Microprocessors \$395
Houston, TX Technology Service Corp.

February

- 3- 5 Microprocessors and Systems Applica-
tions \$350 Saddlebrook, NJ Auto-
mata Information Services



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- 3- 5 Intel MCS80 Workshop \$350 Boston, MA and San Jose, CA Intel Corp.
- 4- 7 Minicomputers/Microcomputers \$425 Dallas, TX Integrated Computer Systems, Inc.
- 10-12 Intel PL/M Workshop \$395 Boston, MA and San Jose, CA Intel Corp.
- 12-14 Microprocessor Product Survey \$395 San Francisco, CA and New York, NY Microcomputer Technique, Inc.
- 12-14 International Solid-State Circuits Conference Philadelphia, PA SSC Council
- 12-14 Microprocessors and Systems Applications \$350 Philadelphia, PA Automata Information Services
- 17-19 Intel MCS40 Workshop \$350 Boston, MA and San Jose, CA Intel Corp.
- 18-20 Computer Science Conference 1975 Washington, DC ACM Contact William F. Atchison
- 24-26 How to Design Systems with Microprocessors \$425 New York, NY and San Francisco, CA Microcomputer Technique, Inc.
- 24-27 Minicomputers and Microprocessors \$395 Zurich, Switzerland Technology Service Corp.
- 25-27 COMPCON SPRING San Francisco, CA Contact Compata, Inc., L.D. Amdahl
- 27-28 How to Program Microprocessors \$275 New York, NY and San Francisco, CA Microcomputer Technique, Inc.

March

- 3- 5 Intel MCS80 Workshop \$350 Boston, MA and San Jose, CA Intel Corp.
- 11-12 Microprocessor Applications in Industry

Philadelphia, PA IECI

- 10-12 Intel PL/M Workshop \$395 Boston, MA and San Jose, CA Intel Corp.
- 12-14 Microprocessor Product Survey \$395 Boston, MA and Chicago, IL Microcomputer Technique, Inc.
- 17-19 Intel MCS40 Workshop \$350 Boston, MA and San Jose, CA Intel Corp.
- 17-19 How to Design Systems with Microprocessors \$425 Boston, MA and Chicago, IL Microcomputer Technique Inc.
- 17-19 Micro, Mini & Midicomputer Systems Structure, Implementation and Application Washington, DC AIIE Seminars
- 20-21 How to Program Microprocessors \$275 Boston, MA and Chicago, IL Microcomputer Technique, Inc.

April

- 7- 9 Micro, Mini & Midicomputer Systems Structure, Implementation and Application New York, NY AIIE Seminars
- 21-23 Micro, Mini & Midicomputer Systems Structure, Implementation and Application Chicago, IL AIIE Seminars
- 22-24 The Society for Information Display International Symposia Washington, DC

SPONSORING ORGANIZATIONS AND CONTACTS

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AIIE Seminars, Dept. K, P. O. Box 25116 Los Angeles, CA 90025 (213) 826-7572

AUTOMATA Information Services, AUTOMATA Systems Corp., 254-10 Northern Blvd., Little Neck, NY 11363 (212) 423-7149



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Ed's Note: MICROCOMPUTER DIGEST publishes, at no cost, the listing of courses, seminars and meetings for four months in advance. If your organization is not listed, please contact the Education Department.

FINANCIAL:

EARNINGS

<u>Adv. Memory Sys.</u>	<u>1974</u>	<u>1973</u>	<u>%</u>
Sept. 30 Earnings	2.1M	56.6K	
Sales	7.5M	8.2M	-8.2
Year Earnings	-2.1M	-196K	
Sales	32.4M	31.4M	+3.1
 <u>Microdata</u>	 <u>1974</u>	 <u>1973</u>	 <u>%</u>
Year Share Earnings	\$.41	\$.34	+20.6
Earnings	641K	525K	+22.2
Sales	13.8M	8.7M	+58.1

ZENTEC SIGNS µC TERMINAL PACT

Zentec Corporation has announced that it will supply its 9002 intelligent microcomputer system to Trans-A-File Systems Co.

Under terms of the agreement, Trans-A-File will use the 9002 terminal with their automated digital document storage and retrieval system. Zentec is an OEM supplier of CRT intelligent programmable terminals utilizing microcomputer technology.

UDC MERGES WITH TYMSHARE

Tymshare, Inc. and United Data Centers, Inc. have jointly announced the consumation of the merger of UDC into a subsidiary of Tymshare. Tymshare will issue approximately 652,000 shares of its common stock to former shareholders of UDC pursuant to the transaction, rising its total outstanding shares to approximately 3,652,000.

Tymshare provides remote access computer services which include microcomputer support software through its international data communications network.

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COMPANY INDEX:

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Auerbach, 121 N. Broad St., Philadelphia, PA 19107 (215) 491-8200

Avco Systems, 210 Lowell, Wilmington, MA 01887 (617) 657-5111

Bourns Management Systems, 6600 Jurupa Ave., Riverside, CA 92504 (714) 687-7220

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Xenia, 3090 Stelling Dr., Palo Alto, CA 94303 (415) 327-2308

PUBLICATION INDEX:

Industrial Market for Microcomputers \$445
Lucy Hendry, Frost & Sullivan, Inc., 106
Fulton St., New York, NY 10038 (212) 223-1080
Reference Report #295

Microcomputer Design, Systems and Hardware
For the 8008, 8080 \$100 Martin Research Ltd.,
1825 S. Halsted St., Chicago, IL 60608
(312) 829-6932

Microprocessor Field Survey & Data Book \$495
for first copy, \$55 each additional copy.
Microprocessor-Based Communications Systems--
Market Analysis Report \$195 for first copy,
\$40 each additional copy. AH Systems Inc.,
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Ed's Note: We apologize for the delay we've caused in your receiving January's Issue. However, we do believe that the new format will greatly enhance your monthly reading. We would appreciate hearing from you concerning the format and any possible suggestions you might have.

January also marks the first month in which several subscriptions expire. Please be sure to renew your subscription.



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