

PRELIMINARY

ARCHIVE CORPORATION  
SC-499 TAPE CONTROLLER  
Information Guide

This information Guide may be filed in  
your IBM PC manual binder for future use.

*exc write  
for more details  
exc*

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## SC-499 TAPE CONTROLLER

### Information Guide

#### 1.1 INTRODUCTION

The SC-499 Tape Controller (Figure 1-1) is designed to interface streaming 1/4-inch cartridge tape drives to the IBM Personal Computer (PC), XT, AT and compatible systems.

The SC-499 is compatible with the IBM PC XT/AT I/O structure, uses DMA for data transfer, and responds to the standard QIC-02 command set. Controller interface with the tape drive is through the QIC-36 industry interface standard. The SC-499 also supports the QIC-24 tape format standard. (Both QIC-36 and QIC-24 are standard features of Archive Fastape and Scorpion tape drives). Operation with 4 or 9 track drives is jumper-selectable.

The tape controller consists of a single printed circuit board which plugs directly into the PC expansion board. Two drive interface connectors on the controller board provide the option of mounting the tape drive internally or externally to the IBM PC System Unit.

The following paragraphs provide the SC-499 unpacking and handling instructions, jumper-selectable options, installation instructions, and interface information.

#### 1.2 HANDLING

Industry standard procedures for the handling of electronic equipment are sufficient for handling the SC-499. The user should ensure that the board and its components are not subjected to physical shock or damage, and to excessive handling which may cause component damage from electrostatic discharge (ESD).

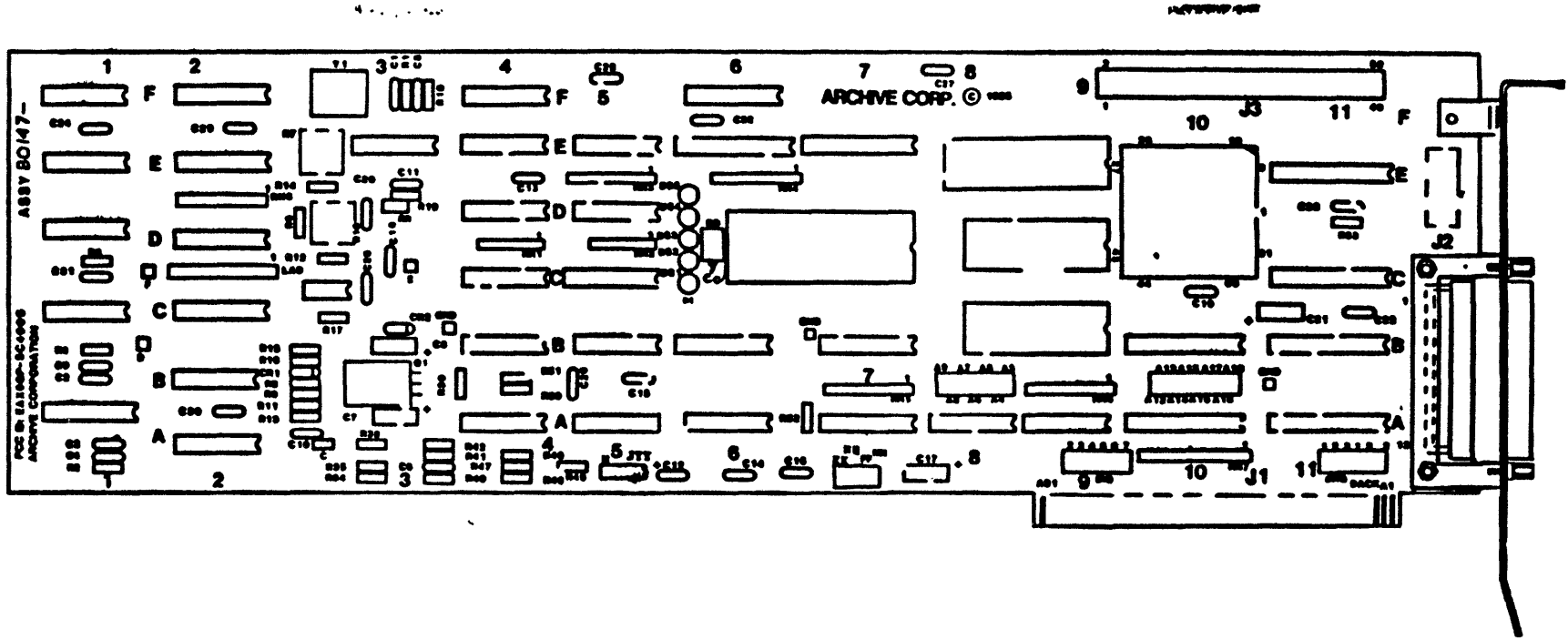


Figure 1.1 SC-499 Tape Controller PCB Assembly

### 1.3 UNPACKING AND INSPECTION

The SC-499 has been packaged for maximum protection from shipping damage. Still, an inspection of the board and components should be performed upon receipt to assure that no damage has occurred. If damage is detected notify the manufacturer and the common carrier immediately. If practical, save all containers and packing materials for reshipment or storage.

### 1.4 JUMPER-SELECTABLE OPTIONS

The jumper-selectable options given in Table 1-1 are available on the SC-499.

TABLE 1-1. JUMPER-SELECTABLE OPTIONS

DESCRIPTION	JUMPER LOCATION	OPTION
Tape format	CC	IN = QIC-24* OUT = QIC-11
Tape Speed	DD	OUT (90IPS)* For Archive use only
Number of Tracks	Y	IN = 9 Tracks OUT = 4 Tracks
Power-On Confidence Test	KK	IN = Test at Power-ON or Reset OUT = Test Disabled
I/O Register Base Address**	A3 thru A9	IN = Address Bit TRUE OUT = Address Bit FALSE NOTE: Base Address is selectable from 0 to 3F8 HEX on 8-byte boundaries.
DMA Priority Level (Select one pair)	DRQ1, DACK1 DRQ2, DACK2 DRQ3, DACK3	Both IN = Priority Level 1* Both IN = Priority Level 2 Both IN = Priority Level 3
Interrupt Priority	IRQ2	IN = Priority Level 2*
	IRQ3	IN = Priority Level 3
	IRQ4	IN = Priority Level 4
	IRQ5	IN = Priority Level 5
	IRQ6	IN = Priority Level 6
	IRQ7	IN = Priority Level 7
	Loop on Error Maintenance	FF C
Test Configuration	HH	OUT* (For Archive use only)
No Description	NN, RR	OUT* (For Archive use only)

\* As-shipped configuration

\*\* As-shipped configuration = A9 Jumper IN (200 HEX).

choosing At bus address

\*

## 15. JUMPER CONFIGURATION

The tape controller jumpers are installed at the factory and the I/O board connectors are shown in Figure 1-2.

NOTE: Jumper location Y is open on the 4-track controller.

### 1.5.1 Contention

The as-shipped configuration (Base Address = 200 HEX, DMA Channel = 1, Interrupt Priority = 2) of the SC-499 provides contentionless operation for the majority of the system users, though a contention problem can arise between the tape controller and certain other options if both are installed.

NOTE: Be advised that most IBM PC models use DMA Channel 2 for the floppy disk drive and DMA Channel 3 for the hard disk drive. However, the AT does not use DMA Channel 3 for the hard disk drive. It is handled through I/O.

Dowe?

CONNECTOR J3 IS I/O FOR INTERNALLY-LOCATED TAPE DRIVE

DIAGNOSTIC INDICATORS

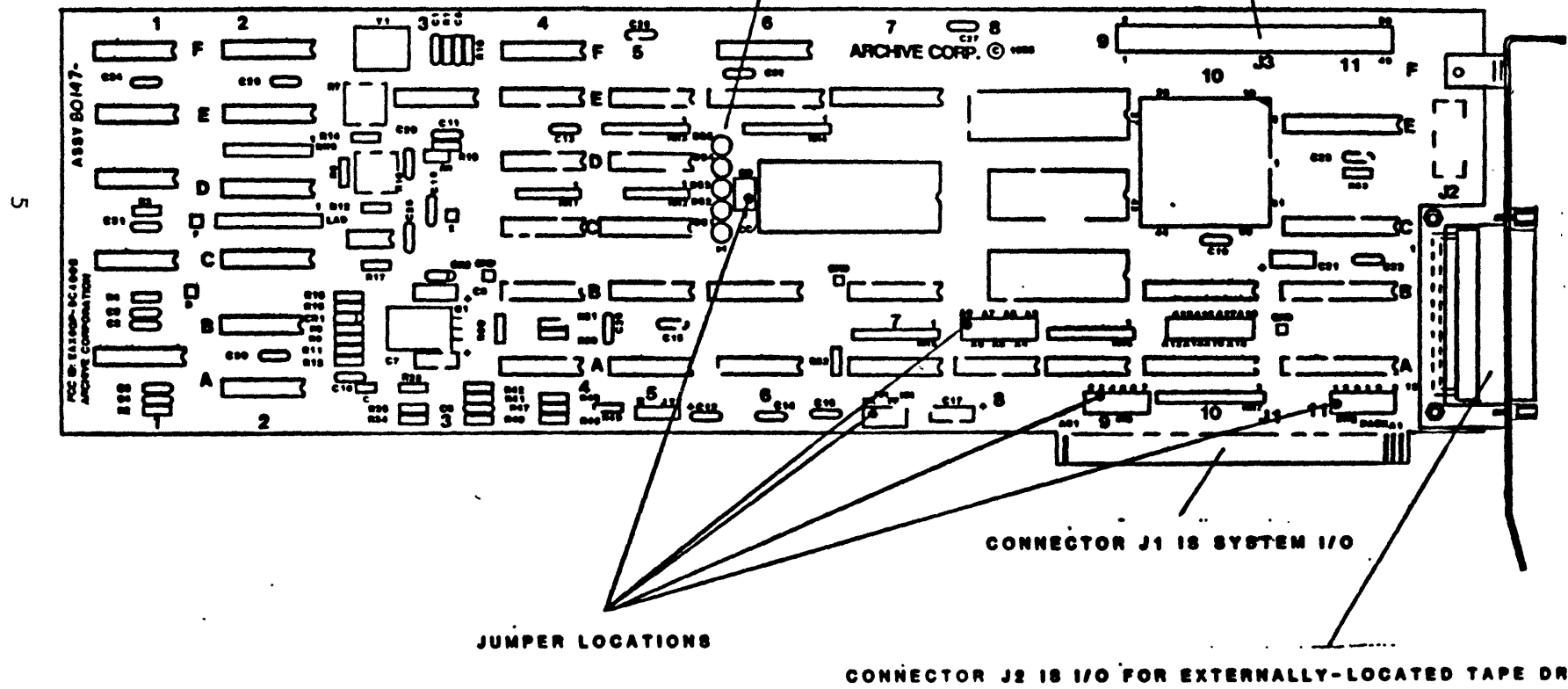


Figure 1.2 SC-499 Jumpers, indicator, and connector locations



## 1.6 ELECTRICAL SIGNAL DESCRIPTION

All voltage measurements are taken at the controller connector (J2 or J3) with terminators installed. Standard TTL levels are used on signal lines to the drive as follows:

FALSE - Logic 0 (HIGH) = 2.4 to 5.25 VDC  
TRUE - Logic 1 (LOW) = 0.0 to 0.55 VDC

Standard TTL levels are required on signal lines to the controller as follows:

FALSE - Logic 0 (HIGH) = 2.0 to 5.25 VDC  
TRUE - Logic 1 (LOW) = 0.0 to 0.80 VDC

## 1.7 INTERFACE CONNECTIONS

The SC-499 pin assignments and signal descriptions for the IBM PC bus interface connector, J1, are listed in Table 1-2.

Table 1-3 lists pin assignments and signal descriptions for both drive-interface connectors, J2 and J3. At the external interface connector J2, pins 3, 4, 8, 15 and 19 are signal returns connected to signal ground at the controller. The cable shield connects to the connector housing only. At the internal interface connector J3, all odd-numbered pins are signal returns connected to signal ground at the drive

TABLE 1-2 CONNECTOR J1 PIN ASSIGNMENTS/SIGNAL DESCRIPTION

PIN	NAME	DESCRIPTION
A02	DB7	DATA BUS BIT 7
A03	DB6	DATA BUS BIT 6
A04	DB5	DATA BUS BIT 5
A05	DB4	DATA BUS BIT 4
A06	DB3	DATA BUS BIT 3
A07	DB2	DATA BUS BIT 2
A08	DB1	DATA BUS BIT 1
A09	DB0	DATA BUS BIT 0
A12 THRU A31	A19 THRU A00	SYSTEM ADDRESS BUS
B02	RESET DRV	RESET DRIVE
B18	DRQ1	DMA REQUEST Priority Level 1
B06	DRQ2	DMA REQUEST Priority Level 2
B16	DRQ3	DMA REQUEST Priority Level 3
B17	/DACK1	DMA ACKNOWLEDGE Priority Level 1
B26	/DACK2	DMA ACKNOWLEDGE Priority Level 2
B15	/DACK3	DMA ACKNOWLEDGE Priority Level 3
B13	/IOW	I/O WRITE
B14	/IOR	I/O READ
B25	IRQ3	INTERRUPT REQUEST Priority Level 3
B24	IRQ4	INTERRUPT REQUEST Priority Level 4
B23	IRQ5	INTERRUPT REQUEST Priority Level 5
B22	IRQ6	INTERRUPT REQUEST Priority Level 6
B21	IRQ7	INTERRUPT REQUEST Priority Level 7
B27	T/C	TERMINAL COUNT
B30	OSC	OSCILLATOR (14.31818 MHz Clock)

TABLE 1-3 CONNECTOR J2/J3 PIN ASSIGNMENTS/SIGNAL DESCRIPTIONS

PIN		NAME	TO*	DESCRIPTION
J2	J3			
13	02	GO-	D	GO. Motion Control for capstan servo.
25	04	REV-	D	REVERSE. Direction control for capstan servo.
12	06	TR3-	D	TRACK SELECT Bit 3 (MSB).
24	08	TR2-	D	TRACK SELECT Bit 2.
11	10	TR1-	D	TRACK SELECT Bit 1.
23	12	TRO-	D	TRACK SELECT Bit 0 (LSB).
10	14	RST-	D	RESET. Cause drive to perform initialization and head recalibration.
22	22	DSO-	D	DRIVE SELECT
09	24	HC-	D	HIGH CURRENT. Enables operation with alternate tape type (DC600A).
21	26	RDP-	C	READ DATA PULSE. Read data is present at the drive interface.
20	28	UTH-	C	UPPER TAPE HOLE.
07	30	LTH-	C	LOWER TAPE HOLE.
06	34	CIN-	C	CARTRIDGE IN. Tape cartridge in place.
18	36	USF-	C	UNSAFE. Safe plug on cartridge is in the unsafe position, i.e. writing is enabled.
05	38	TCH-	C	TACHOMETER. Capstan tachometer pulses.
17	40	WDA-	D	WRITE DATA.
16	42	WDA+	D	Inverse of WRITE DATA signal.
02	46	HSD-	D	HIGH SPEED DRIVE. Tape speed = 90 ips.
14	48	WEN-	D	WRITE ENABLE.
01	50	EEN-	D	ERASE ENABLE.

\*C = Controller  
D = Drive

## 1.8 INSTALLATION

The SC-499 fits and functions in any expansion slot in the IBM PC System Unit except slots 7 and 8. Power requirements from the System Unit are given in Table 1-4.

TABLE 1-4. SC-499 POWER REQUIREMENTS

VOLTAGE	CURRENT	MAXIMUM RIPPLE
+5V+/-5% including ripple	1.0A (typ) 1.25A (max)	100 mv
+12+/-5% including ripple	65ma (typ) 125ma (max)	500 mv to 10KHz; 200 mv beyond 10KHz

To install controller:

1. Set all external power switches to OFF, and unplug the external power cord(s) from their power source.

### NOTE

Steps 2 thru 7 are for mounting the SC-499 in a System Unit expansion slot.

2. Disconnect any interface cabling which may obstruct cover removal. Remove the System Unit cover (Figure 1-3) to gain access to the interior (see Figure 1-4).
3. Connect the tape drive interface cable to controller connector J3 (see Figure 1-2), which is a 50-pin (male) header connector.

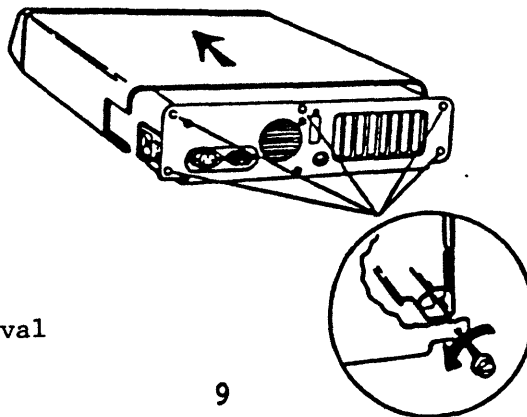


Figure 1.3

PC Cover Removal

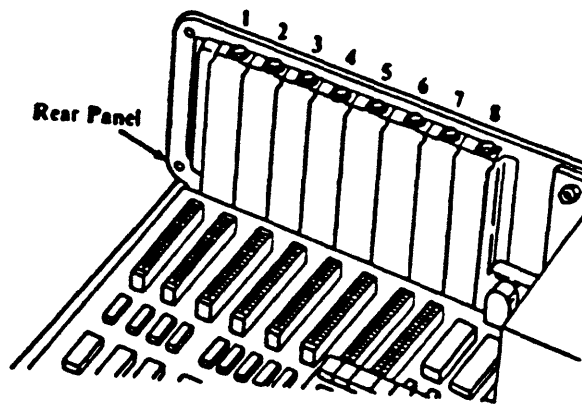


FIGURE 1-4. PC Expansion Slots

4. Choose any available expansion slot (except 7 and 8) and remove the cover plate from the rear panel access to that slot. Save the retaining screw and cover.

CAUTION

The tape controller PCB may be shorted to the IBM PC system speaker if the controller is used in expansion slot 1.

5. Carefully, but firmly, press the controller board into the slot.
6. Align the hole in the board's retaining bracket with the hole in the System Unit rear panel, and replace the retaining screw.
7. Replace the System Unit cover and reconnect all cables.
8. If the tape drive is mounted outside of the System Unit, connect the tape drive interface cable to controller connector J2 (see Figure 1-2), which is a 25-pin (female) D-type, subminiature connector. J2 is accessible from the System Unit rear panel.

NOTE: Interface cable length should not exceed 72 inches (1.8 meters).

9. Installation is now complete and power may be restored.

### 1.8.1 Power-On Confidence (POC) Test

A POC test occurs automatically when power is applied or when a reset command is issued. This test includes sub-tests of the following:

- \*Microprocessor internal RAM and basic instructions

- \*LSI controller operation

- \*16K RAM IC

- \*Data separator logic (discrete)

Successful completion of the above tests are reported to the host by the assertion of EXC-within five seconds. If EXC- is not asserted within this time a failure is indicated.

on reset timer  
5sec

Each logic group except the microprocessor has an associated LED diagnostic indicator as follows:

- \*DS1-LS1 controller chip

- \*DS2-16K RAM buffer logic

- \*DS4,DS5 - not used

Successful completion of all tests is indicated by a single blink of all five LED's following the off period during which the tests are performed. Each time a test fails the associated LED blinks and the test is repeated; hence, a blinking indicator is a visual indication of the area of failure. If the microprocessor fails the results are unpredictable.

## 1.9 I/O STRUCTURE

The SC-499 is fully compatible with the IBM PC I/O structure. The I/O registers occupy eight adjacent locations in the IBM PC I/O address map. Only four of the address locations are used by the SC-499.

NOTE: Jumper-selectable BASE ADDRESS is factory-set at 200 HEX.

1. BASE ADDRESS +0 (200 HEX): Data/Command Register (Read or Write).  
*INDICATE CMD*
2. BASE ADDRESS +1 (201 HEX): Control Register (Write Only). Status Register (Read Only).

### CONTROL REGISTER DESCRIPTION (Write) *only when doing*

BIT 7	1 = RSTSAC	Reset controller microprocessor
BIT 6	1 = REQ	Request to LSI chip
BIT 5	1 = IEN	Enables interrupts IEN = 0, masks interrupts
BIT 4	1 = DNIEN	Enables DONE interrupt DNIEN = 0, masks DONE interrupt.

*All true when request*

(BITS 0-3 Not Used)

### STATUS REGISTER DESCRIPTION (Read) *only after op perform*

BIT 7	0 = IRQF	Interrupt Request Flag, ORing of RDY AND EXC, and DONE if DNIEN is set.
BIT 6	0 = RDY	Ready, from LSI chip.
BIT 5	0 = EXC	Exception, from LSI chip.
BIT 4	1 = DONE	Done, from DMA logic.
BIT 3	1 = DIRC	Direction, indicates direction of bus is from controller to IBM PC.

*0 0 0 0 1 K*

(BITS 0-2 Not Used)

3. BASE ADDRESS +2 (202 HEX): Start DMA (DMAGO). Any write to this register will cause DMAGO to be active.
4. BASE ADDRESS +3 (203 HEX): Reset DMA (RSTDMA). Any write to this register will cause RSTDMA to be active.

## 1.10 INTERRUPTS

The SC-499 interrupt priority level is jumper-selectable (see Table 1-1). Each interrupt source bit, RDY, EXC, and DONE (see Status Register Description), can be read through the Status Register regardless of the state of the interrupt masks: IEN = 0, DNIEN = 0, (see Control Register Description). The IRQ line is tri-stated when IEN is cleared. This allows other IBM PC options the use of that interrupt line when the tape controller is not using it. Therefore, the IBM PC 8259 interrupt controller should be programmed to respond to the tape controller's IRQ only after IRQ has been enabled by setting IEN.

## 1.11 DMA

The tape controller uses the IBM PC 8237 DMA controller to transfer data to and from the IBM PC main memory. The DMA channel is also jumper-selectable (see Table 1-1).

The tape-controller DMA logic can be initialized by writing to address location BASE+3 (RSTDMA). RSTDMA initializes the DMA sequencer, clears all Control Register bits to 0, and sets DONE to 1 (power-on reset from the IBM PC performs the same functions). The following sequence may be used to start DMA transfer:

1. Issue a transfer command to the tape controller.
2. Set up the 8237 DMA controller's register (but leave the mast bit set).
3. Write (any value) to the tape controller register at BASE ADDRESS+2 (DMAGO).
4. Clear the mask bit in the 8237 DMA controller.
5. Repeat above from step 2 for each subsequent block.

## 1.12 RESETS

Four reset signals (two DMA resets, and two microprocessor/tape drive resets) are available on the SC-499.

### 1. DMA Resets:

- \* RSTDMA. (RSTDMA is discussed in the DMA paragraph above).
- \* RESET DRV. This is the power-on reset from the IBM PC power supply, and performs the same functions as RSTDMA.

### 2. Microprocessor and Tape Drive Resets:

- \* Microprocessor RESET. Reset the controller microprocessor when any of the following conditions occur:
  - a. The +5V supply drops below 4.6V.
  - b. The +12V supply drops below 9V.
  - c. RSTSAC is set.

### NOTE

Microprocessor RESET will also cause a tape drive reset.

\*RSTSAC. Activated by writing a 1 to Control Register Bit 7. RSTSAC must be set, held for more than 25 usec, then cleared by either writing a 0 to Control Register Bit 7 or by a RSTDMA.

*block length  
can be  
1024 - (page)*

*for each blk*



Doesnt list select command for drive 2 3 or 4 are they avail?

### 1.13 PROGRAMMING SECTION \* (Technically Oriented)

The SC-499 controller is designed to accept the QIC-02 command set. The SC-499 shall utilize the QIC-02 standard command set as follows:

lead to use to set light on get correct in use

SELECT, SOFT LOCK OFF	H'01'
SELECT, SOFT LOCK ON	H'11'
BOT	H'21'
ERASE	H'22'
RETENSION	H'24'
SELECT Q11 FORMAT	H'26'
SELECT Q24 FORMAT	H'27'
WRITE	H'40'
WRITE FILE MARK (WFM)	H'60'
READ	H'80'
READ FILE MARK (RFM)	H'A0'
READ STATUS	H'CO'

H'01' ←  
H'11'  
H'21'  
H'22'  
H'24'  
H'26'  
H'27'  
H'40'  
H'60'  
H'80'  
H'A0'  
H'CO'

indicated in 0000 0001  
Look AT Achieve Spc pg 13 of 67

The SC-499 shall discriminate between DC300XL and DC600A cartridges by measurement of BOT to LOAD POINT distance and shall select appropriate basic drive write current.

#### 1.13.1 STANDARD COMMAND DESCRIPTIONS

STAD 1) SELECT, SOFT LOCK OFF (0000 0001)

The SELECT command selects the tape drive. The drive shall remain selected until changed by another SELECT command or RESET.

OPT 2) SELECT, SOFT LOCK ON (0001 0001) This is optional cmd

This command is identical in function to the SELECT, SOFT LOCK OFF command and additionally provides a SOFT LOCK on the cartridge. Execution of the SELECT command or RESET unlocks the cartridge.

STAD 3) BOT COMMAND (0010 0001)

The BOT command positions the tape in the cartridge in the selected device to BOT (beginning of tape).

STAD 4) RETENSION COMMAND (0010 0100) = initialization cmd in 0160

The RETENSION command shall be used in accordance with cartridge tape manufacturer's instructions. The RETENSION command moves the tape in the device to BOT, then to EOT and then back to BOT.

STAD 5) ERASE COMMAND (0010 0010)

The ERASE command completely erases the tape in the selected drive. The ERASE command moves the tape in the device to BOT, activates the erase head and moves to EOT, deactivates the erase head

\*Users should familiarize themselves with the QIC-02 REVD intelligent interface STANDARD manual.

write in file mark

and moves the tape back to BOT. The ERASE command also fulfills the requirements of initialization.

*STD* 6) WRITE COMMAND (0100 0000)

When the WRITE command is issued the device requests and transfers data. The READY line is activated when the device is ready for a data block transfer. When the READY line is active, the host terminates transfer of write data by issuing a WRITE-FILE-MARK command. NOTE: A write command following cartridge insertion or RESET shall commence recording at BOT end of tape, otherwise, recording shall commence at the current tape position. NOTE: If the host starts transfer between blocks before READY is asserted, READY may not be asserted when the early warning hole of the last track is detected by the device, thus the device ceases to transfer additional data blocks from the host. The device terminates the WRITE command and reports END OF MEDIA by means of an EXCEPTION and READ STATUS.

*STD* 7) READ COMMAND (1000 0000)

When the READ command is issued the device transfers data. The READY line is activated when the device is ready for a data block transfer. The READ command shall be terminated by the device if a file mark is detected. The host is informed by means of an EXCEPTION and a READ STATUS sequence. When READY is true, the host may alternatively terminate the READ command by issuing a READ-FILE-MARK command. If a READ command is issued, the command is accepted and the drive continues reading. NOTE: A READ command following cartridge insertion or RESET shall commence at BOT, otherwise the read command commences from the current tape position. NOTE; If the host starts transfer between blocks before READY is asserted, READY MAY NOT BE ASSERTED.

*STD* 8) WRITE-FILE-MARK COMMAND (0110 0000)

The WRITE-FILE-MARK (WFM) command causes a file mark to be written on the tape in the selected drive. NOTE: a WFM command following cartridge insertion or RESET shall commence recording at BOT end of tape, otherwise, recording shall commence at the current tape position.

*STD* 9) READ-FILE-MARK COMMAND (1010 0000)

The READ-FILE-MARK (RFM) command causes the tape in the selected drive to be moved to the next FILE MARK. NOTE: A RFM command following cartridge insertion or RESET shall commence reading at the BOT, otherwise, reading shall commence at the current tape position.

*STD* 10) READ STATUS COMMAND (1100 0000)

The READ status command provides the host with information about the selected device. The host issues the READ STATUS command. The device transfers the standard six bytes to the host.

*Vendor  
approved*

11) SELECT Q11 FORMAT COMMAND (0010 0110)

The SELECT Q11 format command selects the Q11 format as the current format.

12) SELECT Q24 FORMAT COMMAND (0010 0111)

The SELECT Q24 format command selects the Q24 format as the current format.

1.13.2 INTERFACE TIMING

Timing specifications are defined at the driven end. Requirements involving deskew shall be the responsibility of the receiving end. Interface signal timing shall be outlined in the following diagrams.

FIGURE

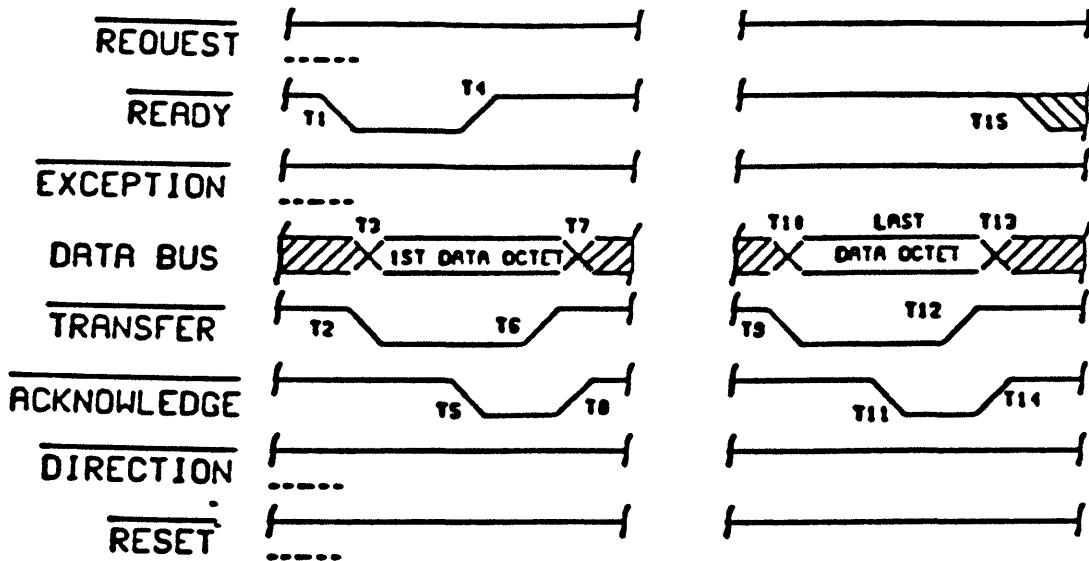
DATA TRANSFER

Write Operation.....	1-5
Read Operation.....	1-6

COMMAND TRANSFER

Ready Asserted.....	1-7
Exception Asserted.....	1-8
Direction Deasserted.....	1-9

STATUS BYTE TRANSFER .....	1-10
----------------------------	------



**Activity**

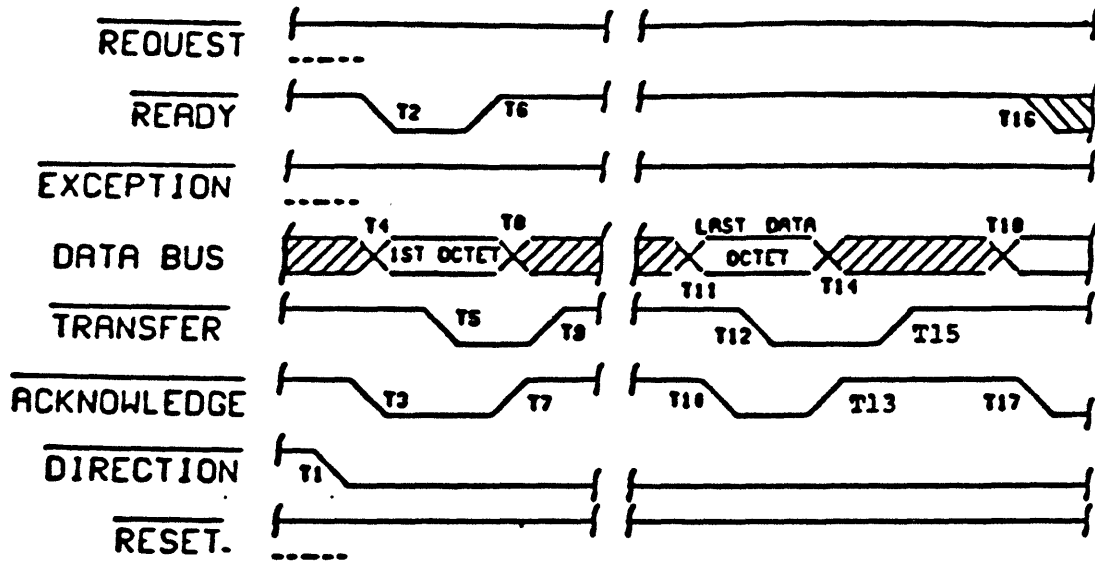
- T1-Device Asserts READY  
(Device READY for First Data Block)
- T2-Controller Asserts TRANSFER
- T3-Data Bus Valid
- T4-Device Deasserts READY
- T5-Device Asserts ACKNOWLEDGE
- T6-Controller Deasserts TRANSFER
- T7-Bus Data Invalid
- T8-Device Deasserts ACKNOWLEDGE
- T9-Controller Asserts TRANSFER
- T10-Data Bus Valid
- T11-Device Asserts ACKNOWLEDGE
- T12-Controller Deasserts TRANSFER
- T13-Bus Data Invalid
- T14-Device Deasserts ACKNOWLEDGE
- T15-Device Asserts READY  
(Device READY For Next Data Block)

**Timing**

- 0 us. < T1---->T2
- T2---->T3 < 40 ns.
- 0 us. < T2---->T4 < 1 us.
- 0.5 us. < T2---->T5 <100 us.
- 0 us. < T5---->T6
- 0 us. < T5---->T7
- 0 us. < T6---->T8 < 3 us.
- 0 us. < T8---->T9
- T9---->T10 < 40 ns.
- 0.5 us. < T9---->T11 <100 us.
- 0 us. < T11--->T12
- 0 us. < T11--->T13
- 0 us. < T12--->T14 < 3 us.
- 100 us. < T14--->T15

\*Note: If the Controller asserts TRANSFER before the device asserts READY, then the behavior of READY is device dependent. READY shall not be asserted for an EXCEPTION condition.

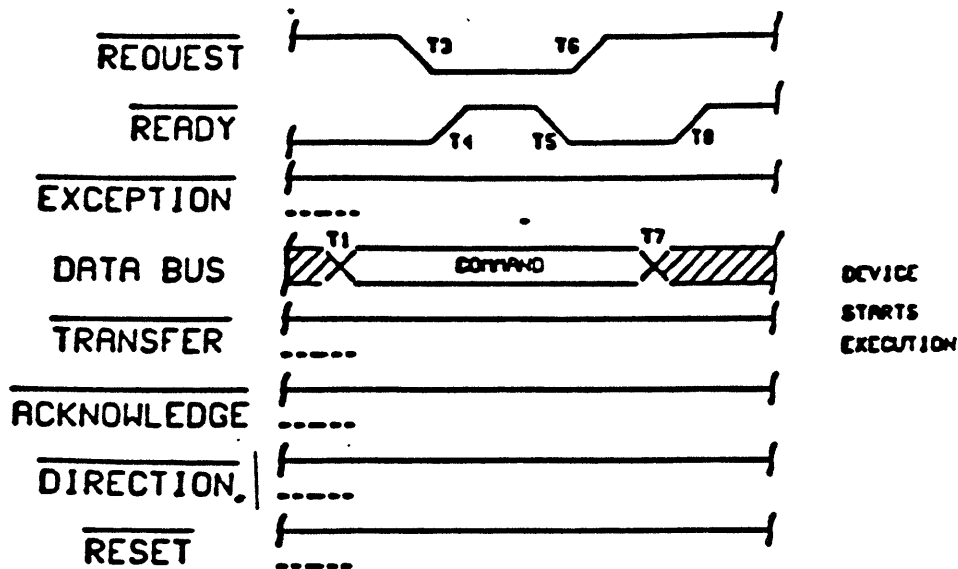
**Figure 1-5 Data Transfer,  
Write Operation**



T1-Device Changes DIRECTION	
T2-Device Asserts READY	
T3-Device Asserts ACKNOWLEDGE	
T4-Bus Data Valid	T3---->T4 < 40 us.
T5-Controller Asserts TRANSFER	0 us. < T1---->T4
T6-Device Deasserts READY	0 us. < T4---->T5
T7-Device Deasserts ACKNOWLEDGE	0 us. < T5---->T6 < 1 us.
T8-Bus Data Invalid	0.5 us. < T5---->T7 < 3 us.
T9-Controller Deasserts TRANSFER	0 us. < T5---->T8
T10-Device Asserts ACKNOWLEDGE	0 us. < T7---->T9
T11-Bus Data Invalid	T10---->T11 < 40 ns.
T12-Controller Asserts TRANSFER	0 us. < T11--->T12
T13-Device Deasserts ACKNOWLEDGE	0.5 us. < T12--->T13 < 3 us.
T14-Bus Data Invalid	0 us. < T12--->T14
T15-Controller Deasserts TRANSFER	0 us. < T13--->T15
T16-Device Asserts READY	
T17-Device Asserts ACKNOWLEDGE	
T18-Bus Data Valid	T17--->T18 < 40 ns.

\*Note: If the Controller asserts TRANSFER before the device asserts READY, then the behavior of READY is device dependent. READY shall not be asserted for an EXCEPTION condition.

Figure 1-6 Data Transfer,  
Read Operation



**Activity**

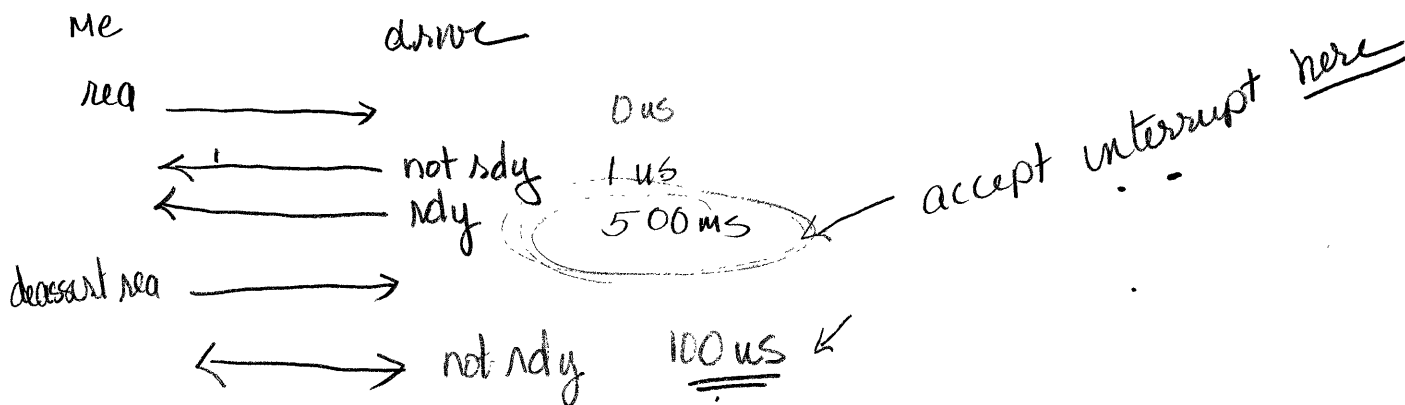
T1-Bus Data Valid

- T3-Controller Asserts REQUEST
- T4-Device Deasserts READY
- T5-Device Asserts READY
- T6-Controller Deasserts REQUEST
- T7-Bus Data Invalid
- T8-Device Deasserts READY

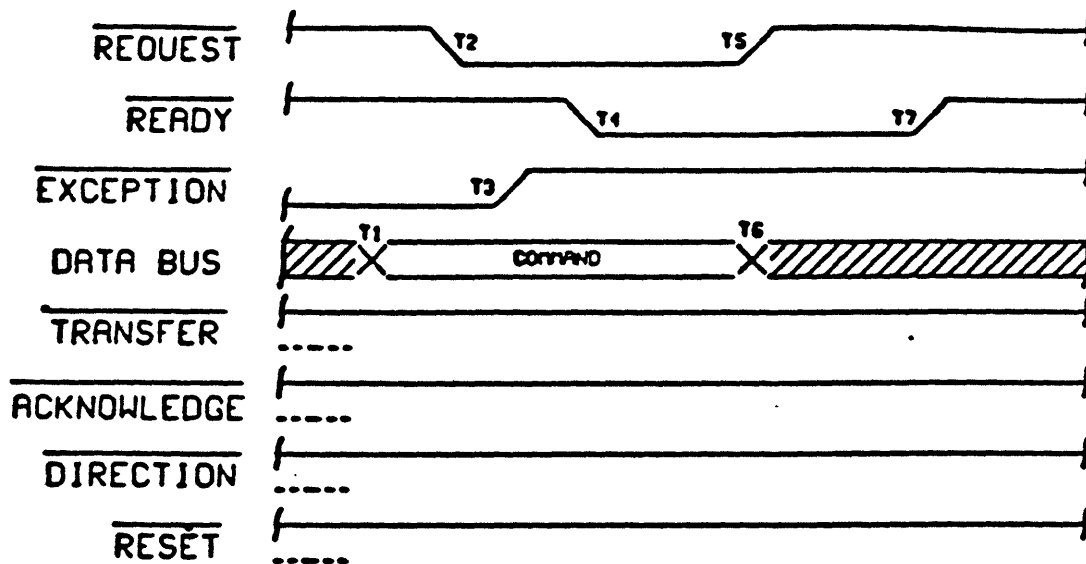
**Timing**

- 0 us. < T1 ---> T3
- 0 us. < T3 ---> T4 < 1 us.
- T4 ---> T5 < 500 ns.
- 0 us. < T5 ---> T6
- 0 us. < T6 ---> T7
- 20 us. < T6 ---> T8 < 100 us.

**Figure 1-7 Command Transfer, READY Asserted**

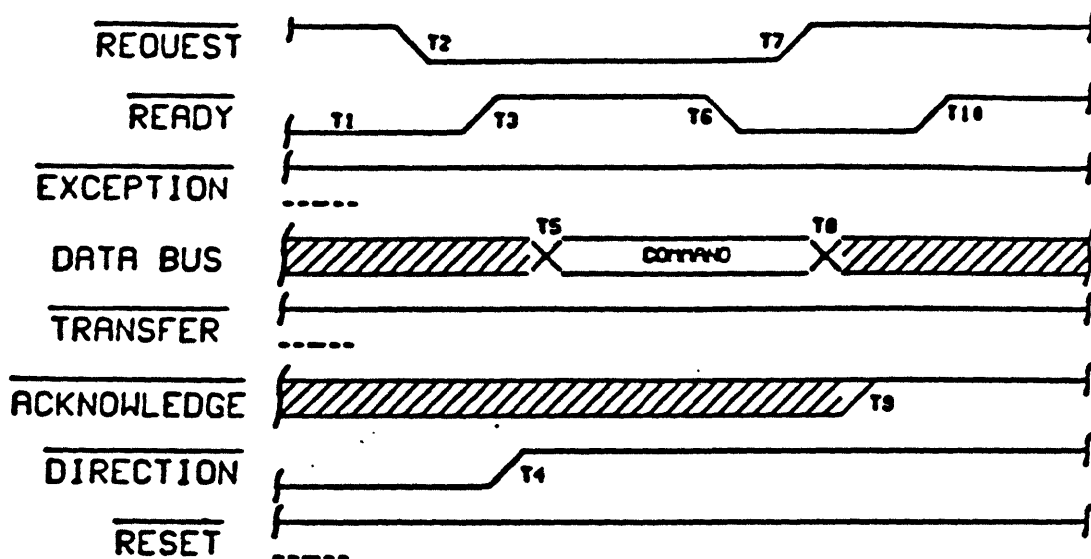


1793



T1-Bus Data Valid	
T2-Controller Asserts REQUEST	0 us. < T1--->T2
T3-Device Deasserts EXCEPTION	0 us. < T2--->T3
T4-Device Asserts READY	10 us. < T3--->T4
T5-Controller Deasserts REQUEST	0 us. < T4--->T5
T6-Bus Data Invalid	0 us. < T5--->T6
T7-Device Deasserts READY	20 us. < T5--->T7 < 100 us.

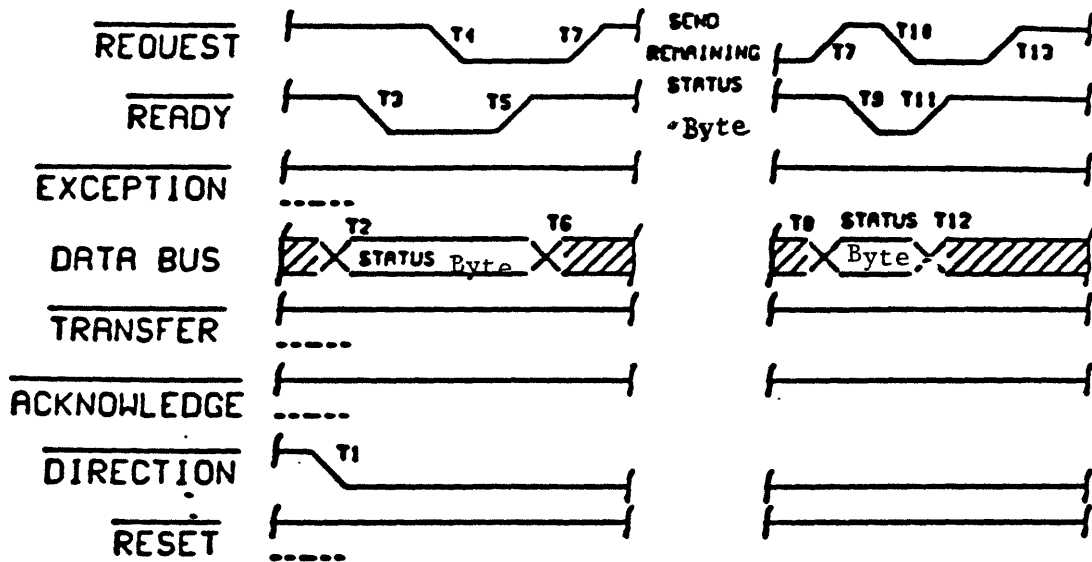
Figure 1-8 Command Transfer,  
EXCEPTION Asserted



Activity	Timing
T1-READY Asserted	
T2-Controller Asserts REQUEST	0 us. < T1--->T2
T3-Device Deasserts READY	0 us. T2--->T3
T4-Device Deasserts DIRECTION	0 us. < T3--->T4 < 150 us.
T5-Bus Data Valid	T4--->T5 < 1 us.
T6-Device A Asserts READY	T4--->T6 < 500 us.
T7-Controller Deasserts REQUEST	0 us. < T6--->T7
T8-Bus Data Invalid	0 us. < T7--->T8
T9-Device Deasserts ACKNOWLEDGE	0 us. < T9--->T10
T10-Device Deasserts READY	20 us. < T7--->T10 < 100 us.

Figure 1-9 Command Transfer,  
DIRECTION Deasserted





**Activity**

- T1-Device Changes Bus DIRECTION
- T2-Bus Data Valid
- T3-Device Asserts READY
- T4-Controller Asserts REQUEST
- T5-Device Deasserts READY
- T6-Bus Data Invalid
- T7-Controller Deasserts REQUEST
- T8-Bus Data Valid
- T9-Device Asserts READY
- T10-Controller Asserts REQUEST
- T11-Device Deasserts READY
- T12-Bus Data Invalid
- T13-Controller Deasserts REQUEST

**Timing**

- 0 us. < T1---->T2
- 0 us. < T2---->T3
- 0 us. < T3---->T4
- 0 us. < T4---->T5 < 1 us.
- 0 us. < T5---->T6
- 20 us. < T4---->T7
- 0 us. < T7---->T8
- 20 us. < T7---->T9
- 0 us. < T9---->T10
- 0 us. < T10---->T11 < 1 us.
- 0 us. < T10---->T12
- 20 us. < T10---->T13

**Figure 1-10 Status Byte Transfer**

### 1.13.3 PROGRAMMING FLOW CHART

The following diagrams depict the flow of the command structures. These flow charts are helpful for any software engineer who is designing a software driver. The flow charts shall be specified in the following diagrams.

DESCRIPTION	FIGURE
✓ READ NTH FILE FLOW DIAGRAM.....	1-11
✓ READ FILE WITH SPECIFIC 1st BLOCK ID FLOW DIAGRAM.....	1-12
✓ APPEND FILE FLOW DIAGRAM.....	1-13
✓ READ FILE FLOW DIAGRAM.....	1-14
✓ WRITE FILE FLOW DIAGRAM.....	1-15
✓ READ FILE MARK FLOW DIAGRAM.....	1-16
✓ WRITE FILE MARK FLOW DIAGRAM.....	1-17
✓ ERASE COMMAND FLOW DIAGRAM.....	1-18
✓ INITIALIZE CARTRIDGE COMMAND FLOW DIAGRAM.....	1-19
✓ BOT COMMAND FLOW DIAGRAM.....	1-20
✓ SELECT, SOFT LOCK COMMAND FLOW DIAGRAM.....	1-21
○ SELECT FORMAT COMMAND FLOW DIAGRAM.....	1-22
✓ RESET FLOW DIAGRAM.....	1-23
DONE FLOW DIAGRAM.....	1-24
✓ READ STATUS FLOW DIAGRAM.....	1-25
SEND COMMAND FLOW DIAGRAM.....	1-26

READ NTH FILE FLOW DIAGRAM

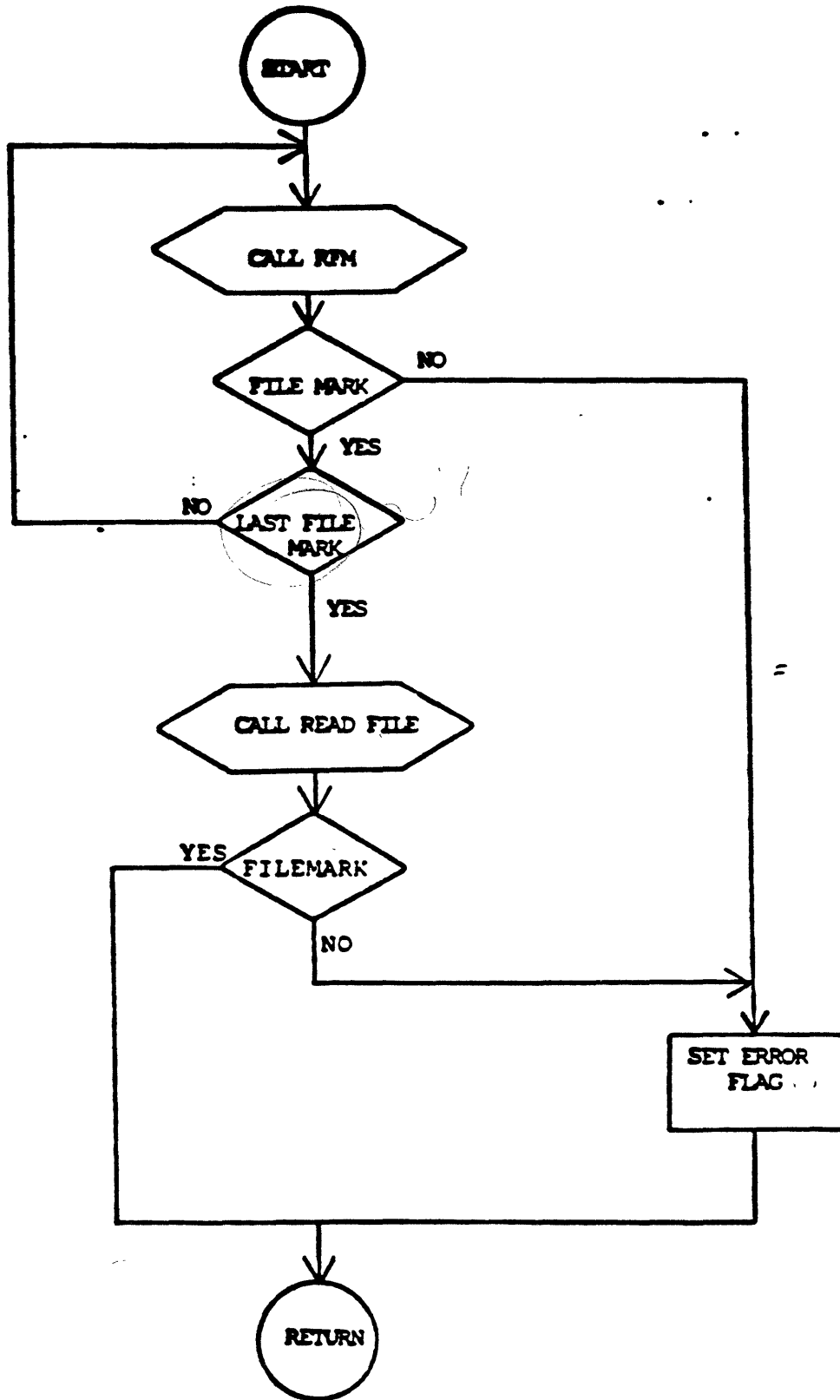
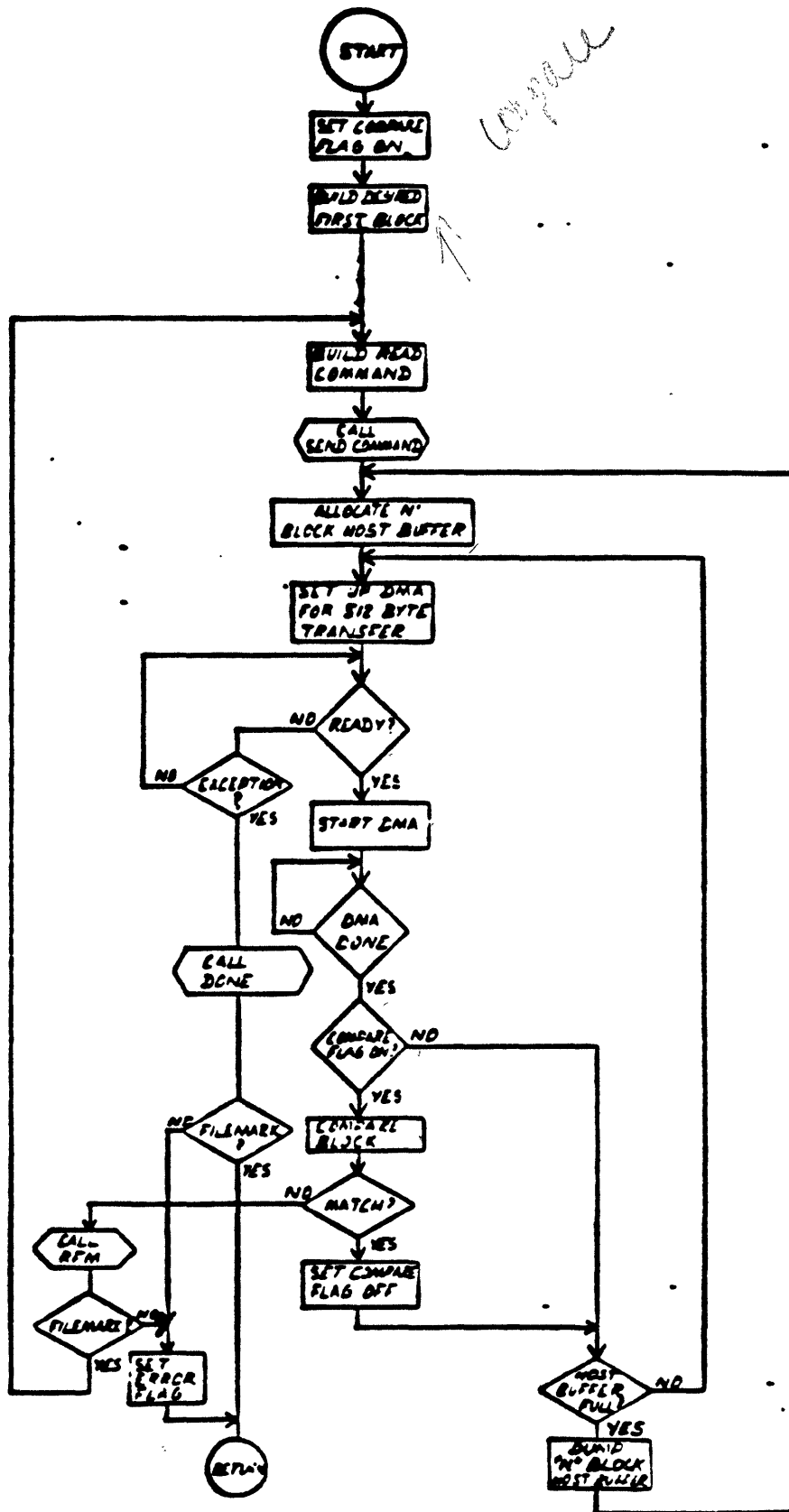


Figure 1-11

READ FILE WITH SPECIFIC 1ST BLOCK ID FLOW DIAGRAM



*Compare*

*Can't read*

*blk 3/12  
6.30.2*

Figure 1-12

APPEND FILE FLOW DIAGRAM

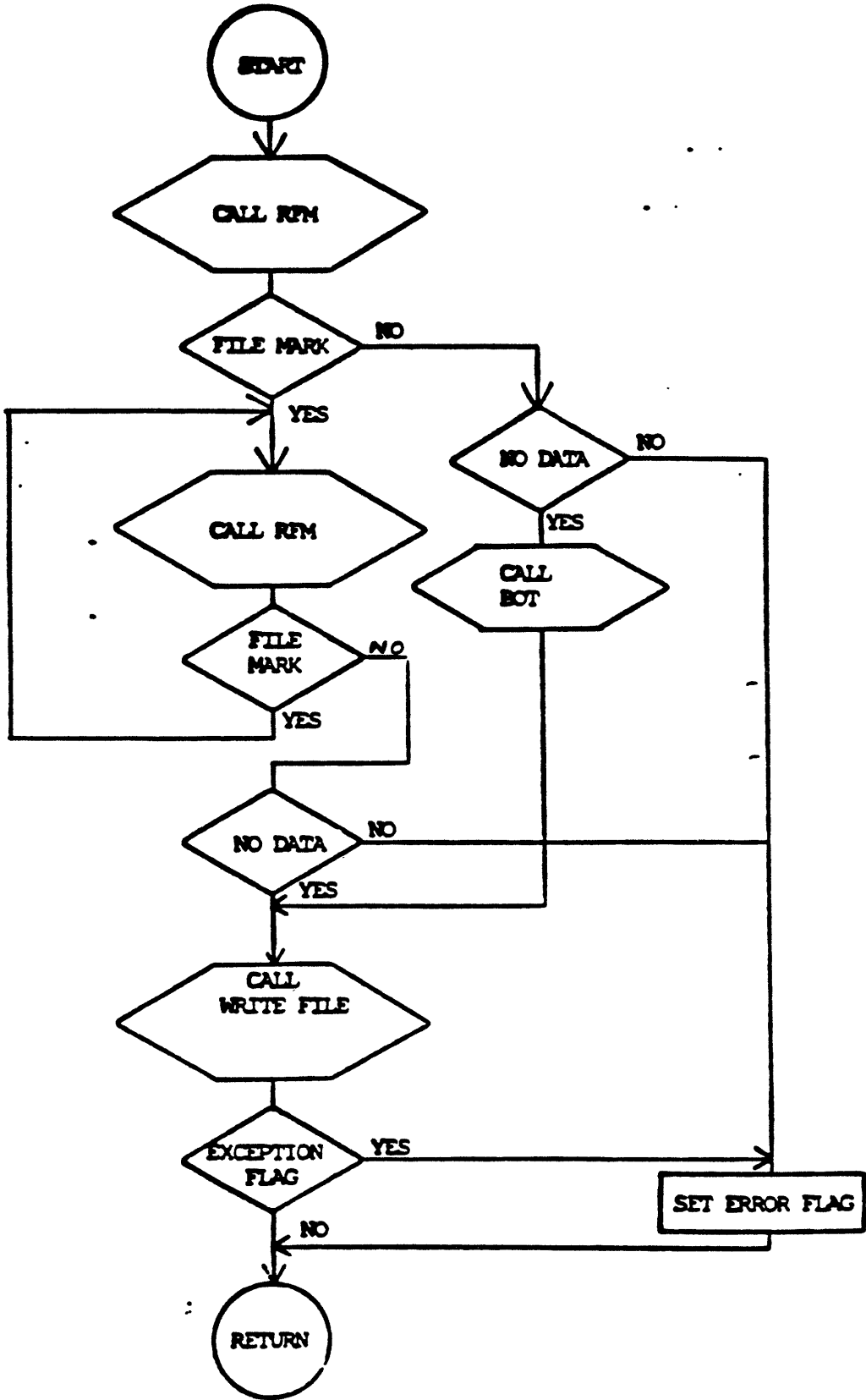


Figure 1-13

Read  
Fills buffers (3)

READ FILE FLOW DIAGRAM

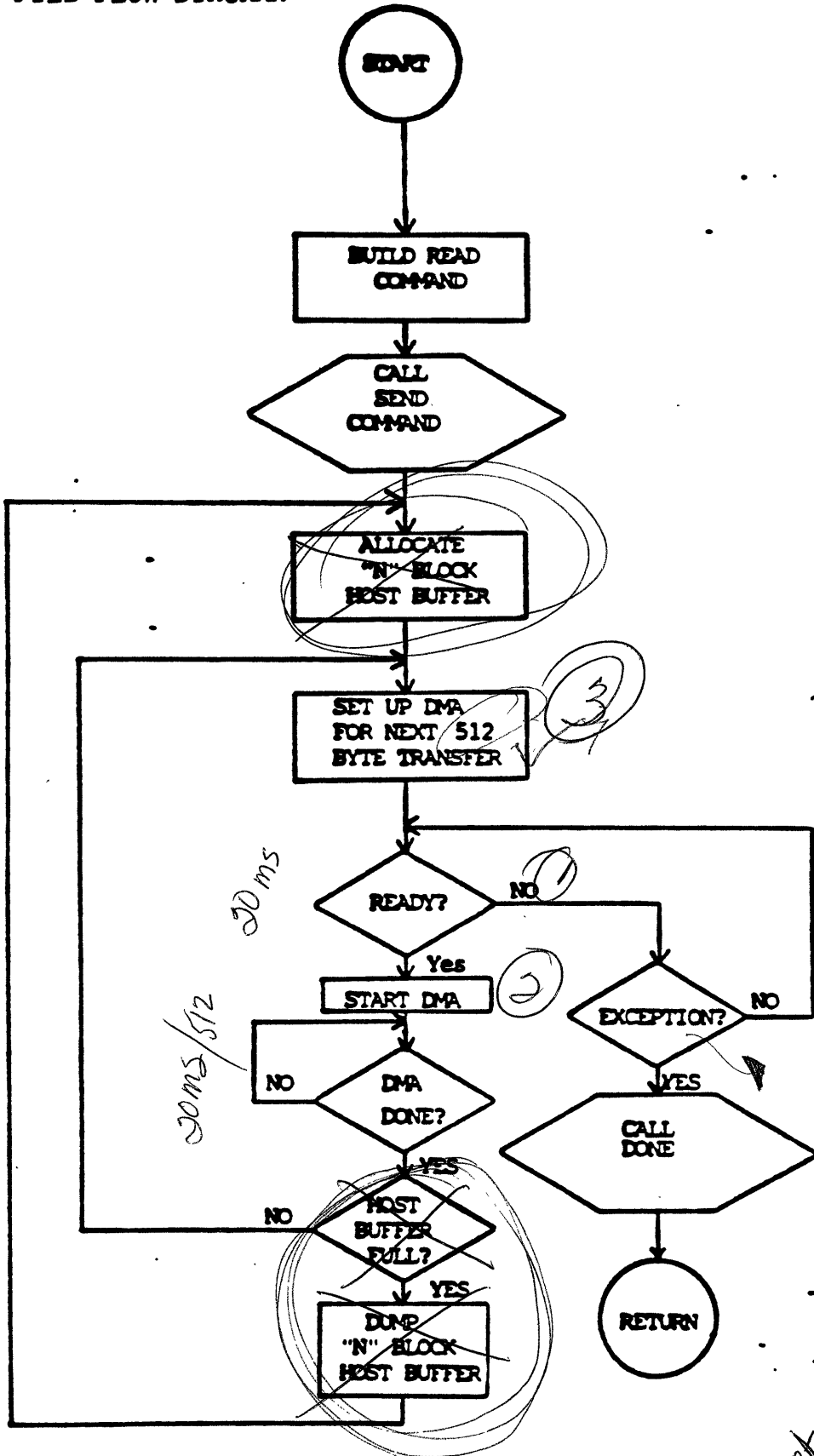


Figure 1-14

WRITE FILE FLOW DIAGRAM

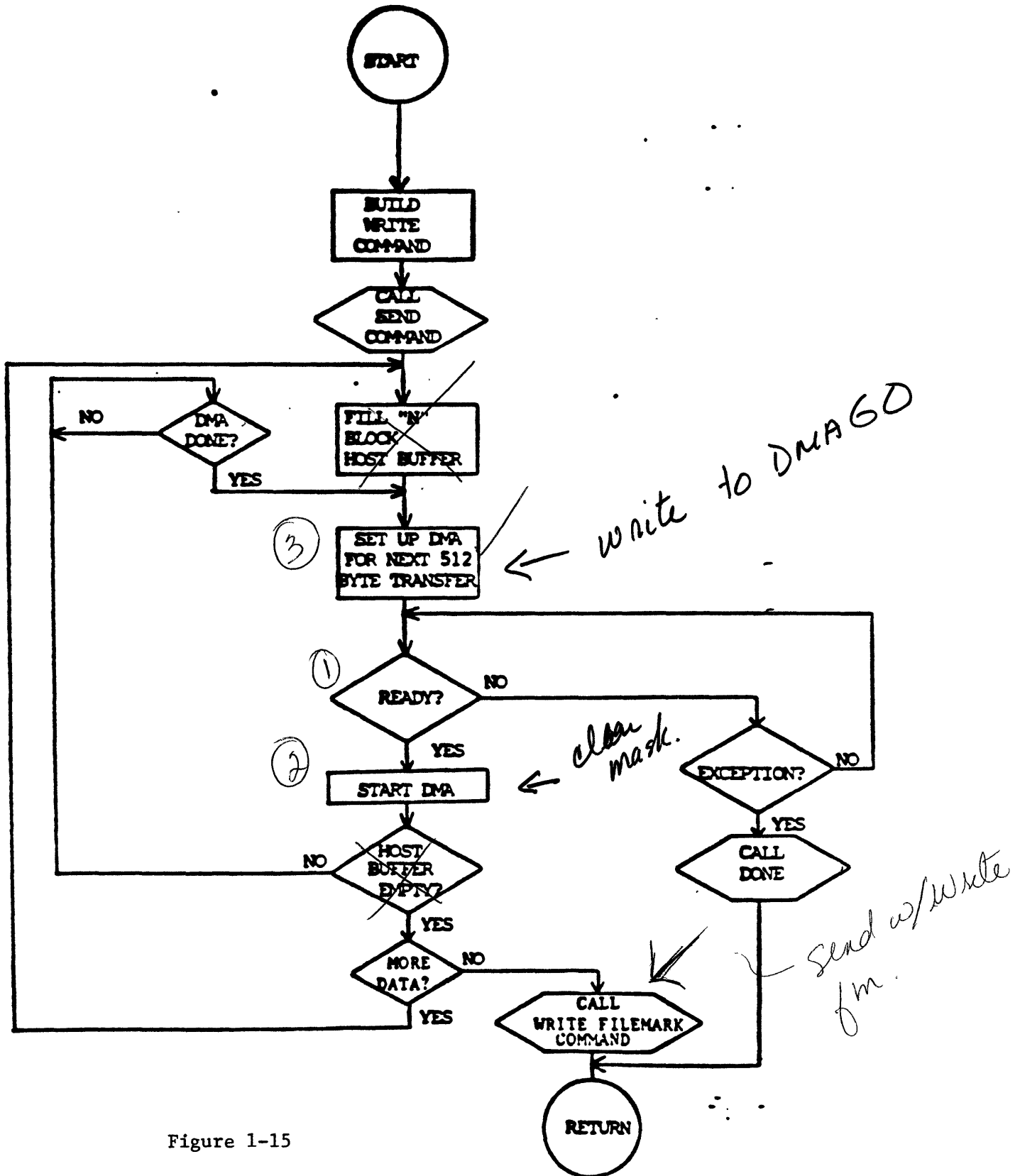


Figure 1-15

READ FILE MARK FLOW DIAGRAM

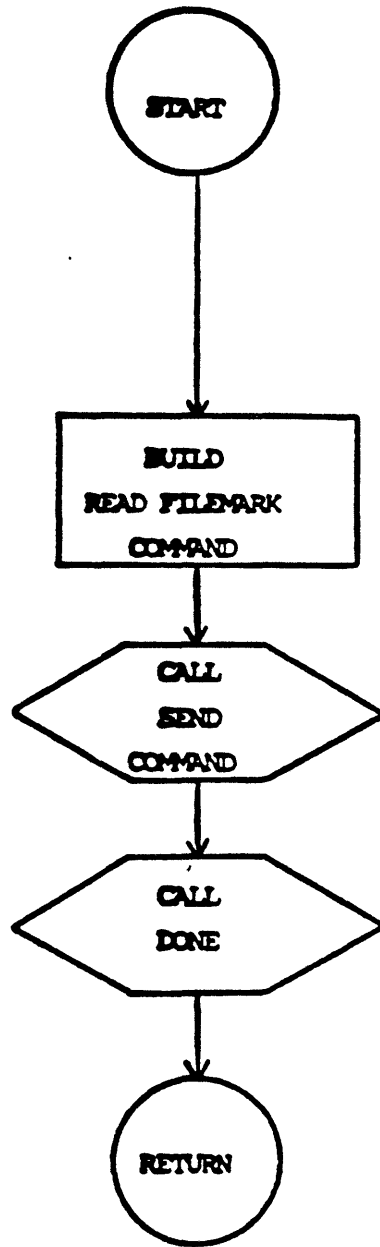


Figure 1-16



WRITE FILE MARK FLOW DIAGRAM

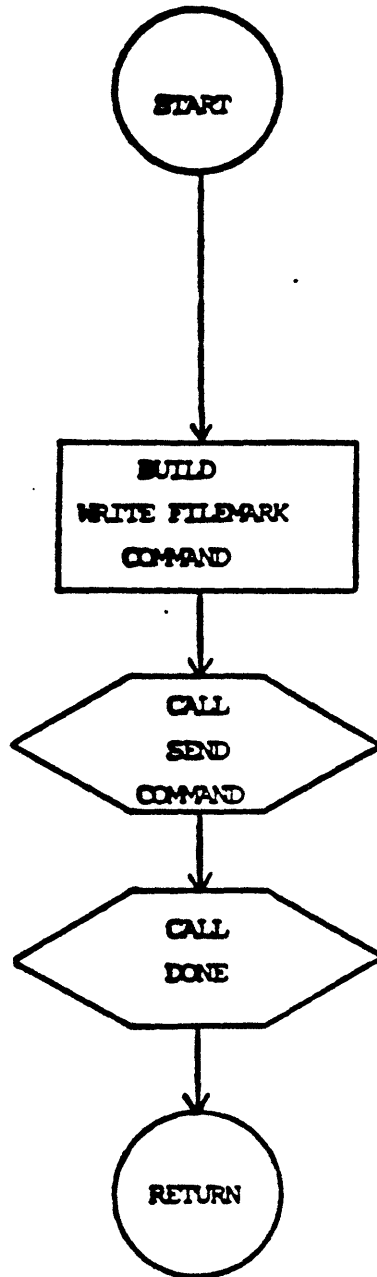


Figure 1-17

**ERASE COMMAND FLOW DIAGRAM**

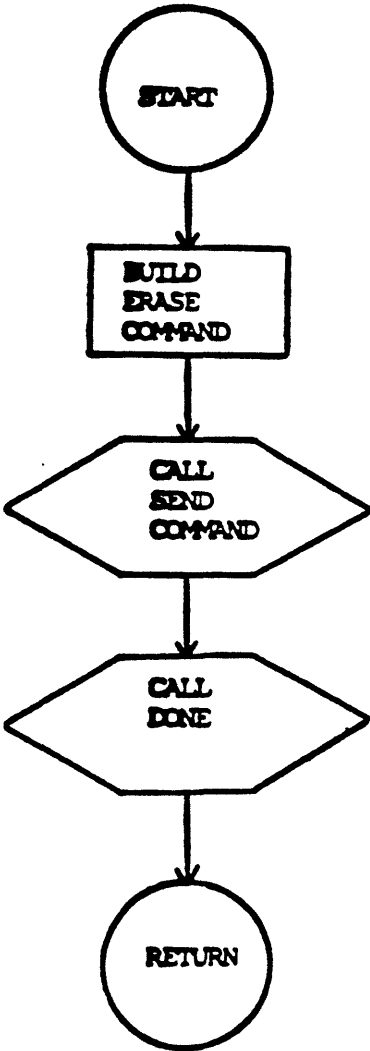


Figure 1-18

**INITIALIZE CARTRIDGE COMMAND FLOW DIAGRAM**

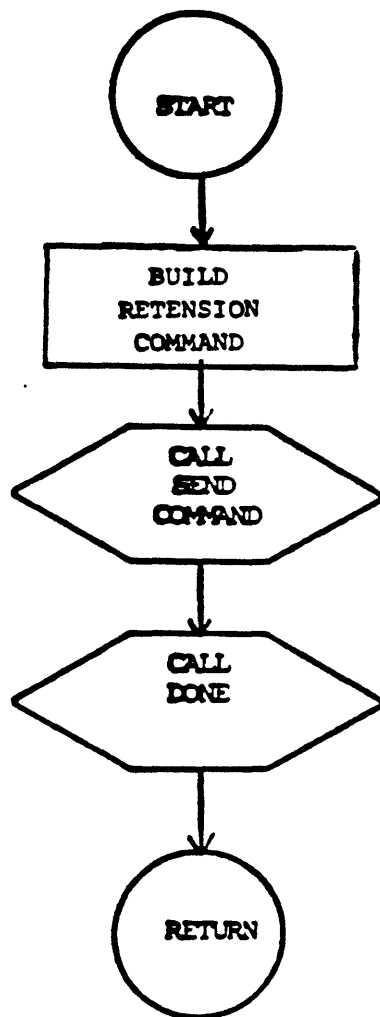


Figure 1-19

**BOT COMMAND FLOW DIAGRAM**

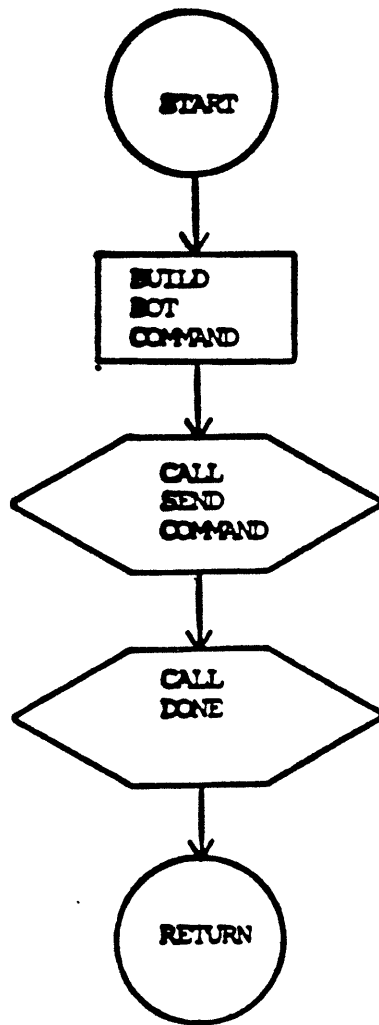


Figure 1-20

**SELECT, SOFT LOCK COMMAND FLOW DIAGRAM**

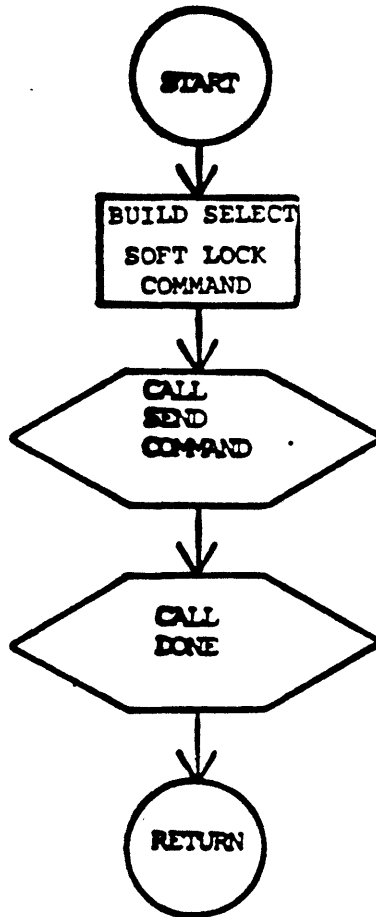


Figure 1-21

**SELECT FORMAT COMMAND FLOW DIAGRAM**

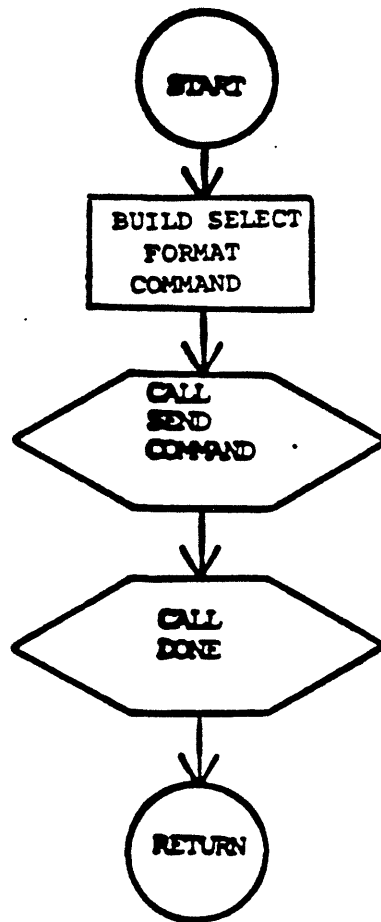


Figure 1-22

RESET FLOW DIAGRAM

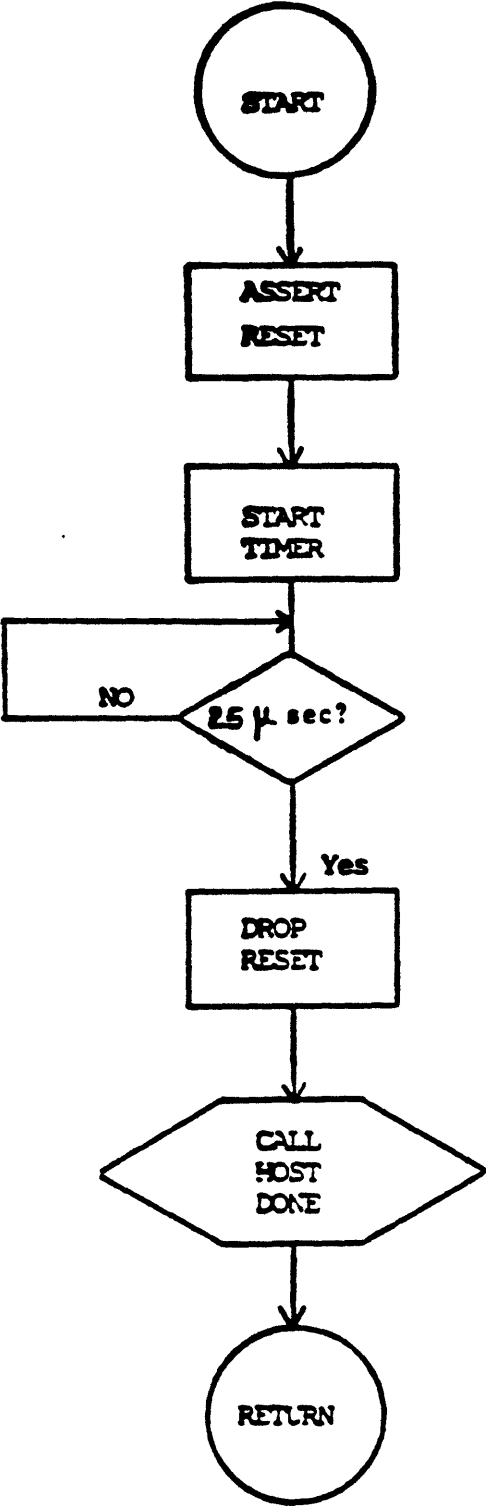


Figure 1-23

DONE FLOW DIAGRAM

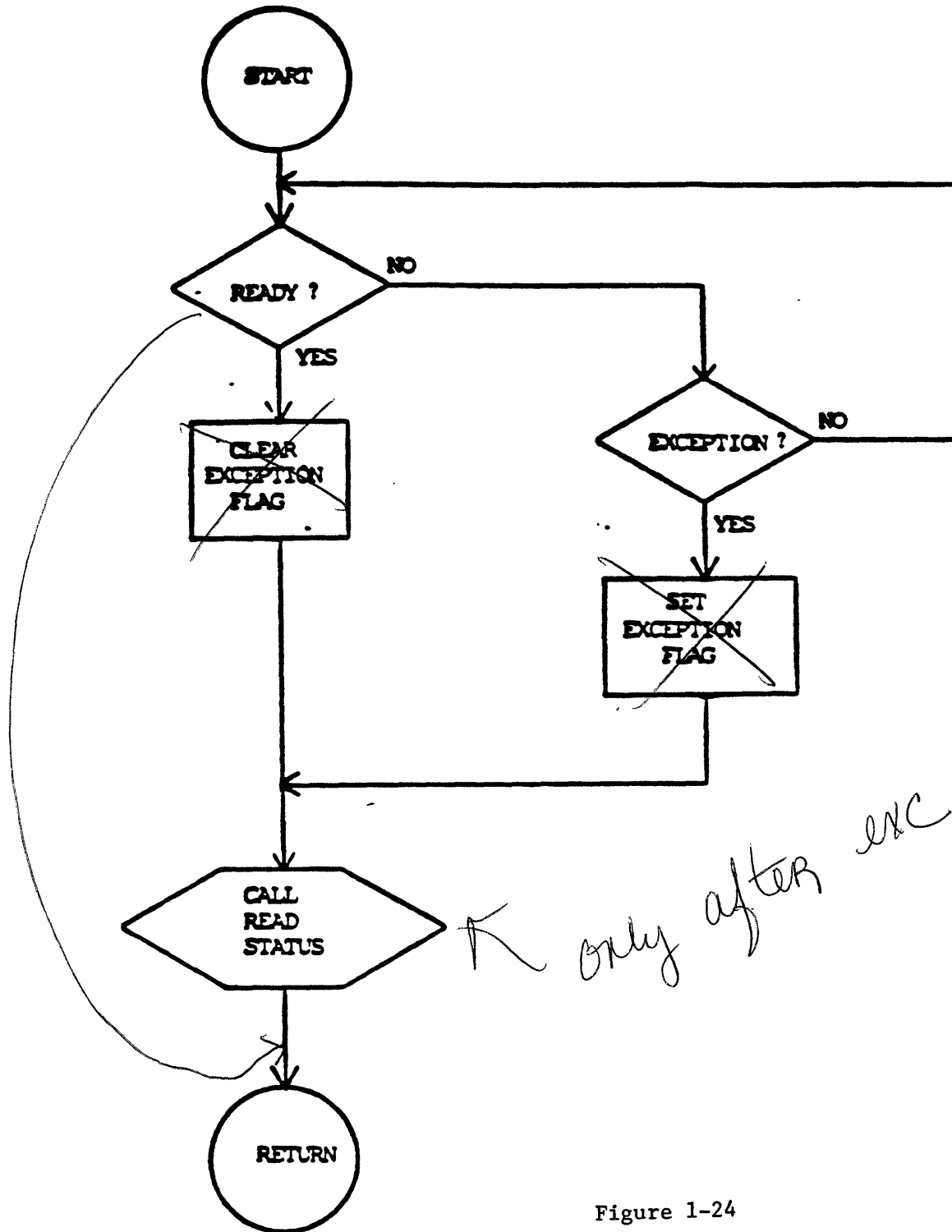


Figure 1-24



READ STATUS FLOW DIAGRAM

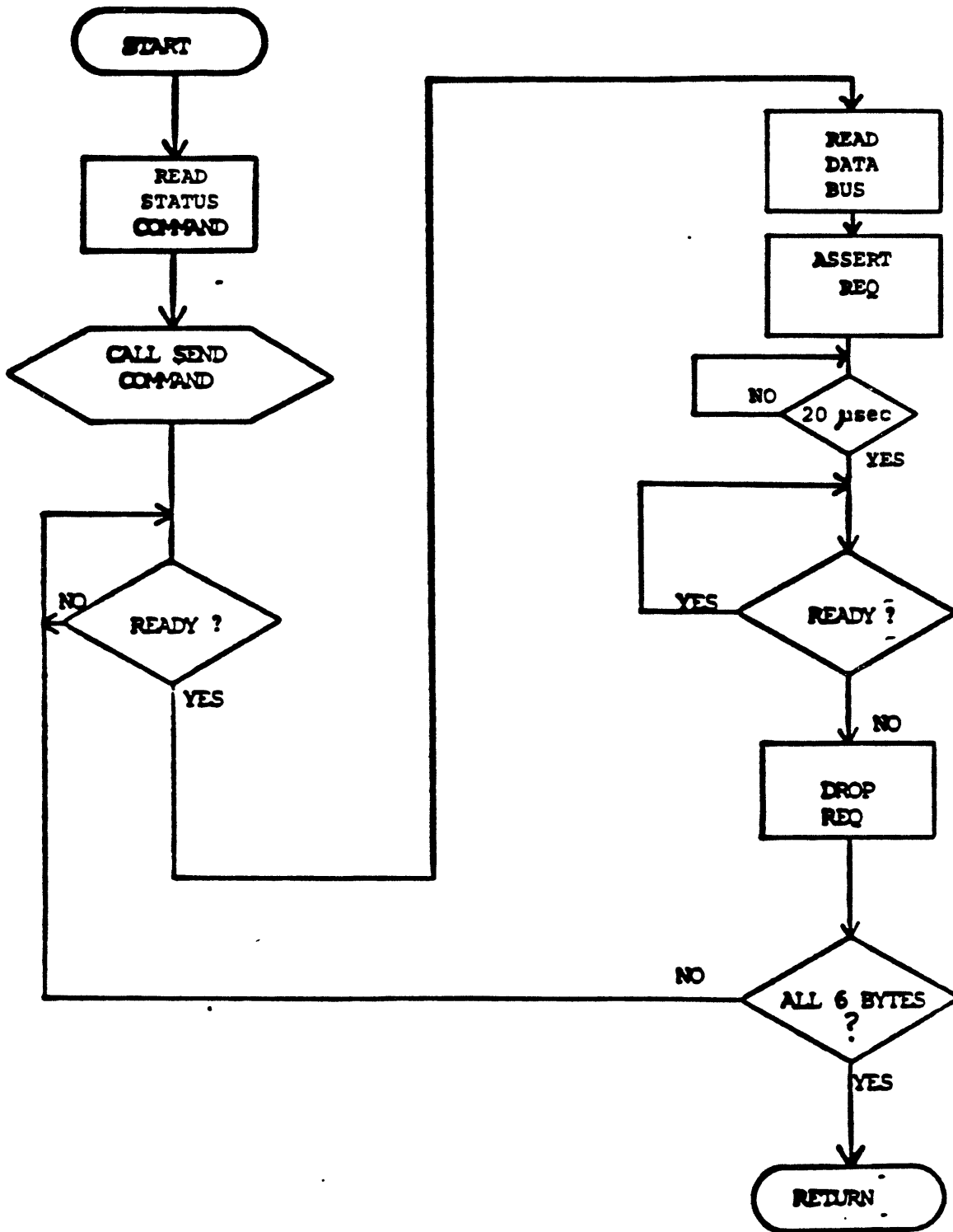
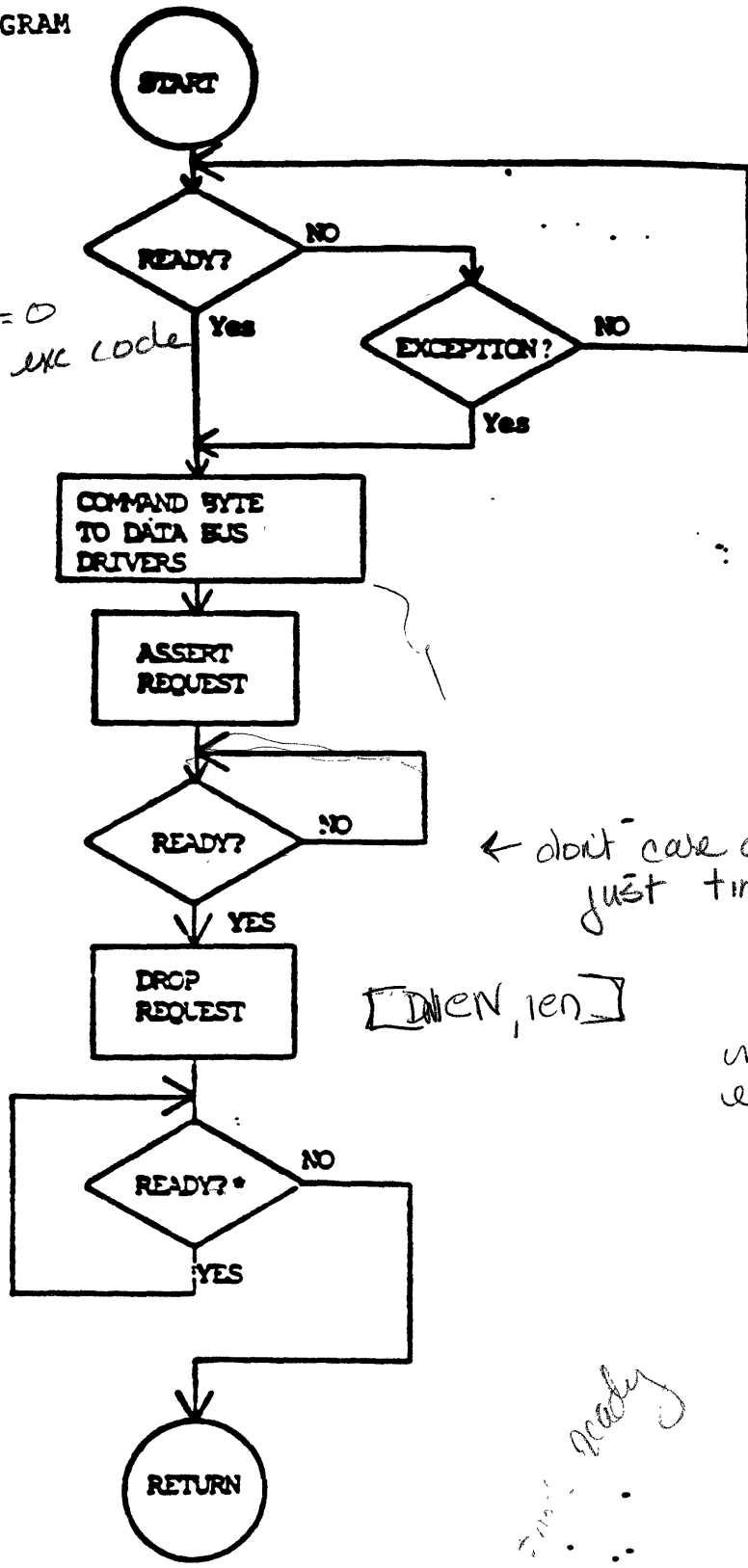


Figure 1-25

SEND COMMAND FLOW DIAGRAM

et.wait  
 ↓  
 return STATUS AIL = 0  
 or STATUS. ALL = exc code



← don't care about exc just timeout

[DLEN, LEN]

initialize pic enable cpu

et.wait ready

\*20 µsec loop max., see timing

Figure 1-26