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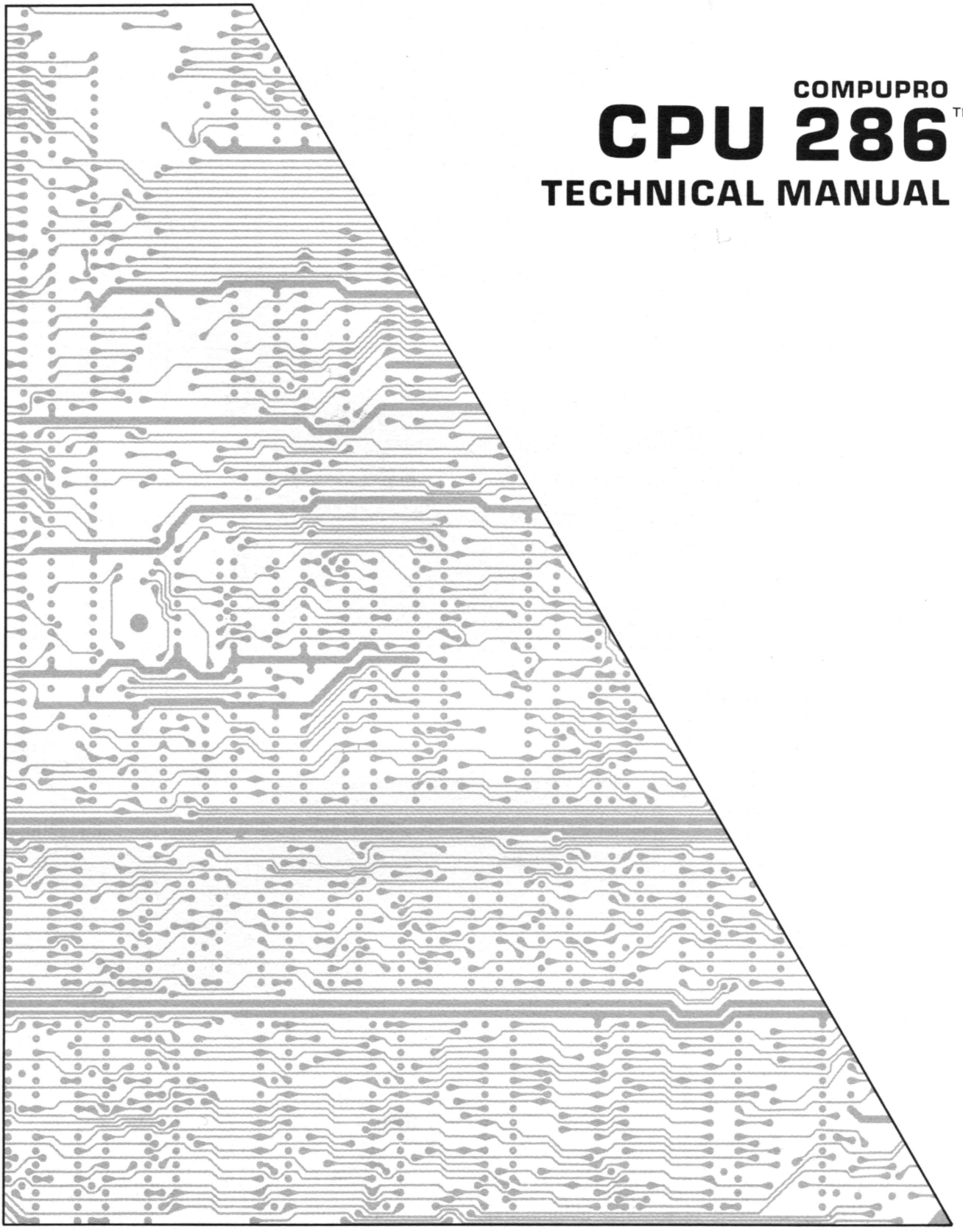

COMPUPRO

CPU 286™

TECHNICAL MANUAL

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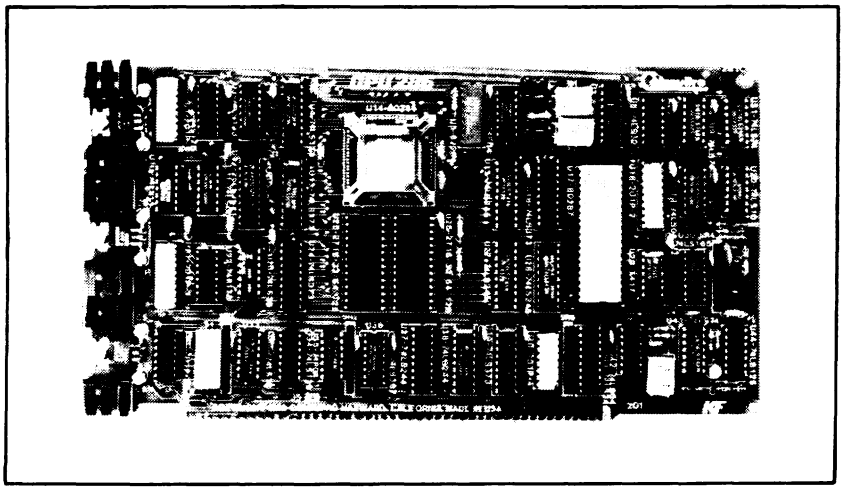
CPU 286
Technical Manual



HIGH PERFORMANCE 16 BIT 80286
80287 NUMERIC PROCESSOR EXTENSION
EPROM SOCKETS FOR UP TO 32K

CPU 286 TECHNICAL MANUAL

Hayward, CA 94545

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CONTENTS

HOW TO GET YOUR CPU 286 UP AND RUNNING WITHOUT READING THE MANUAL

Eager to get your new CPU 286 running? This section is for those of you who are running this CPU board in a standard CompuPro configuration and do not intend to deviate from that standard configuration. You should be able to set the switches and jumpers as shown below and never have to change them again (unless you change your system configuration).

If you want to know all the details about what these switches and jumpers do, you will have to read the rest of this manual.

CPU 286 INSTALLATION PROCEDURES

STEP 1. UNPACK CPU 286 BOARD.

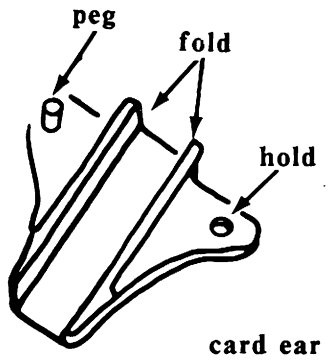
Along with the board, you will find two card ears in the plastic bag.

STEP 2. INSTALL CARD EARS.

a) Hold the board so the component side is toward you. (See diagram below.)

b) Insert the peg on the card ear into the hole in the right corner of the board. Fold the ear over the board's edge until the ear's hole snaps over the peg (make sure the long edge of the ear is along the top edge of the board.)

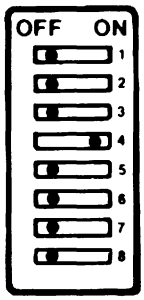
c) Repeat for left ear.



STEP 3. SET SWITCHES. Check the CPU 286 switch settings (see figure below for location of S1).

The black dot (●) shows which side of the switch should be down.

SWITCH 1:



POSITION	SET IT
1	OFF
2	OFF
3	OFF
4	ON
5	OFF
6	OFF
7	OFF
8	OFF

NOTE: SWITCH SETTINGS FOR OTHER COMPUPRO BOARDS

Follow the switch settings in the Disk 1 manual for the CPU 86/87, with the following exception: If you have an "F" revision Disk 1 (part number 171F) or later, move the shorting plug at jumper location J17 from the "A" position (which is the way it was probably shipped from the factory) to the "B" position. J17 is located just to the right of the EPROM. (See your Disk 1 technical manual if you need help locating J17.)

If you have an "E" revision Disk 1 (part number 171E) or earlier, contact your CompuPro System Center or dealer for an upgraded EPROM that contains the 8086/286 boot code.

On the DISK 1A, use the CPU 8086-CPU 286 switch settings outlined in DISK 1A manual.

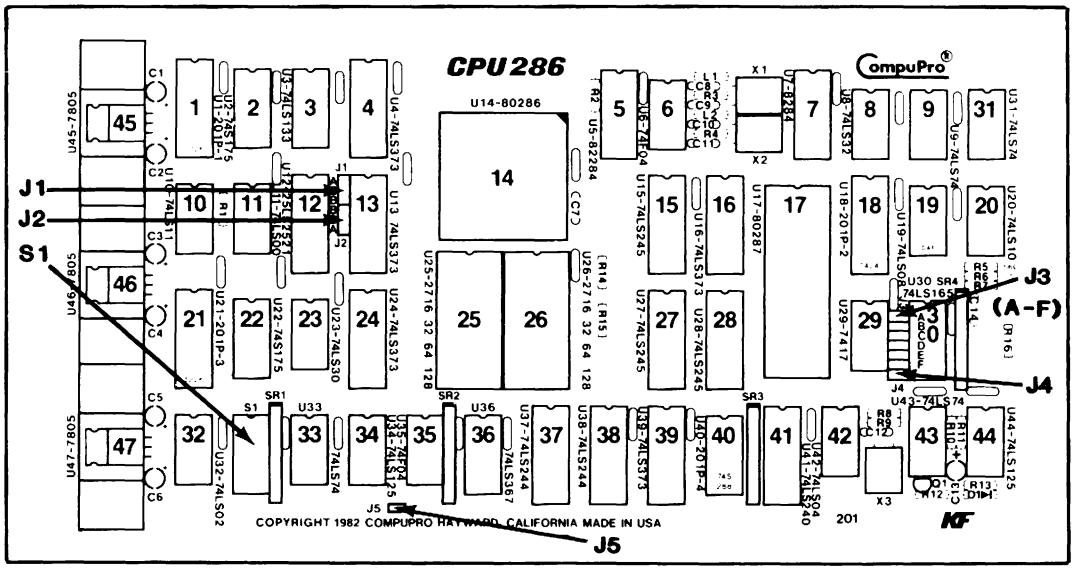
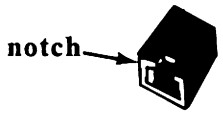


Figure 2. CPU 286 (jumper and switch location)

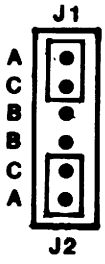
STEP 4. CHECK JUMPER SHUNT CONNECTORS

Make sure the jumper shunts are installed as listed below. (See Figure 2 for location of jumper connectors labeled J1, J2, J3 and J4).

JUMPER SHUNTS

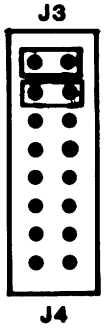


A jumper shunt is a small plastic part used to connect two pins on the jumper connector. Jumper shunts should be installed notch side down.



J1 should be connected from A-C.

J2 should be connected from A-C.



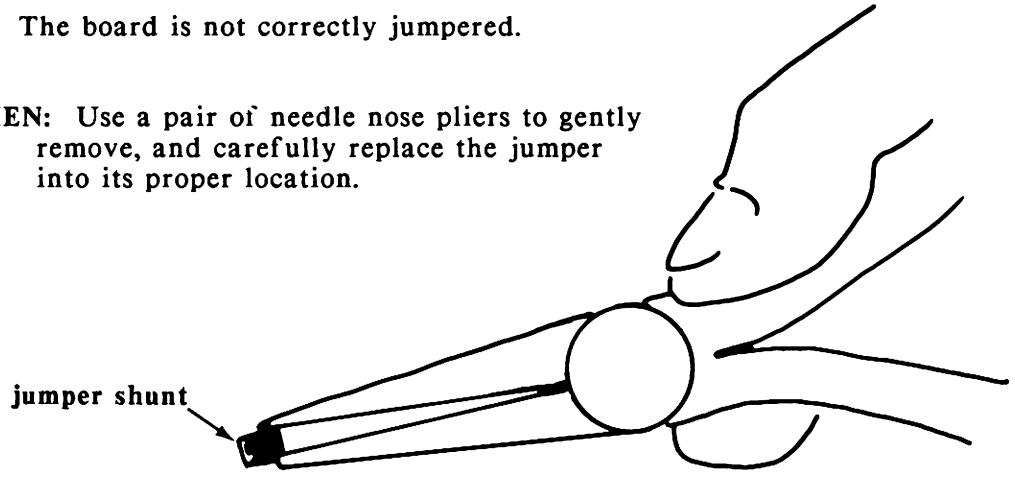
J3 should have shunts in position A and B (the top two locations).

J4 should not have a shunt.

Leave J5 as it came from the factory.

IF: The board is not correctly jumpered.

THEN: Use a pair of needle nose pliers to gently remove, and carefully replace the jumper into its proper location.



BOOTING UP THE SYSTEM

If all the switches and jumpers in the system are set correctly (make sure your drives are jumpered per the Disk 1 or 1A manual if they are other than CompuPro drives), you should be ready to boot up the system. Make sure that all the boards are plugged squarely into the motherboard, replace the enclosure's cover, and turn on the power to the computer, terminal and disk drives. The light on your "A" drive should be flashing about twice per second. If it is not flashing, stop! Read the Disk 1 or 1A manual's troubleshooting section and correct the problem before proceeding. If the light is flashing, insert the single-user or multiuser operating diskette into the A drive and close the drive door. Your system should sign on.

The diskette you should be trying to boot should be an 8086/80286 operating system. A diskette for the CPU 8085/88 will not work. You may return a CPU 8085/88 diskette to CompuPro for upgrading.

HARDWARE SECTION

ABOUT THE CPU 286

The CPU 286 from CompuPro is one of the most advanced 16-bit processors available for the IEEE 696/S-100 bus. Based on Intel's high performance iAPX 286 16-bit processor, it includes sockets for on board EPROM and Intel's 80287 High Speed Numeric Processor Extension. In the real address mode, the 80286 will run all software written for the 8086 (see "Software Considerations" for a discussion). In addition, the 80287 appears to the software just like an 8087. In the protected virtual address mode, the 80286 has integrated Memory Management and Four Level Memory Protection for operating systems employing virtual memory. The address space in the protected virtual address mode extends to 16 Megabytes of physical addressing (24 bits), and a full gigabyte (30 bits) of virtual addressing per task.

The CPU 286 includes circuitry that allows it to handle 8-bit and and 16-bit memory and I/O devices that conform to the IEEE 696/S-100 standard for 8 and 16-bit transfers. Both 8 and 16-bit types may be mixed in a system; the CPU 286/287 will dynamically adjust itself to the proper bus width. The CPU 286/287 is fully compatible with DMA devices that adhere to the IEEE 696/S-100 standard (like the DISK 1, DISK 1A, DISK 2, DISK 3, MPX-1 etc.).

The CPU 286 currently operates with a 6 MHz clock, but is designed to accommodate faster clocks as they are introduced.

A special clock switching circuit allows the use of specially designed slave processors to share the bus with the CPU 286. Use of an 8-bit slave CPU would provide equivalent operation to our CPU 8085/88 dual processor board, thus providing a simple way to execute libraries of existing 8-bit software, as well as CompuPro's proprietary CP/M 8-16 , MP/M or Concurrent DOS 8-1wshp

When you couple high speed operation with the power of the 80286, the CPU 286 is truly a processor board for advanced computing systems. Thank you for choosing a CompuPro product.

SWITCH SETTINGS AND OPTION SELECTION

This section gives you a detailed description of all the switch and jumper settings for the CPU 286. To set the board up for use in a standard CompuPro system configuration, see the first section of this manual: "How to Get Your CPU 286 Up and Running Without Reading the Manual".

DIP SWITCH S1

On dip switch S1, only paddles 2,4,7, and 8 are used. The remaining should all be switched OFF.

S1	Paddle	Function	Normal Setting
	1	Not Used	OFF
	2	ϕDSB* Enable (ON enables feature)	OFF
	3	Not Used	OFF
	4	EPROM ENABLE* (ON disables EPROM sockets)	ON
	5	Not Used	OFF
	6	Not Used	OFF
	7	EPROM SIZE SELECT high bit	OFF
	8	EPROM SIZE SELECT low bit	OFF

Paddle 2 - ϕDSB* Enable: This paddle turned ON allows the master bus clock (ϕ) to be disabled by a temporary bus master asserting the ϕDSB* signal on bus line 21. When this paddle is turned OFF, this feature is disabled. This new S-100 bus line has been defined by CompuPro for use with our slave processor boards or special DMA peripherals. For now, leave this paddle OFF. The manual supplied with a board that utilizes this line will instruct you to turn on the paddle. For a description of how the ϕDSB* line is implemented, see the "Theory Of Operation" section of this manual.

Paddle 4 - When this paddle is turned ON, the two on-board EPROM sockets are disabled. To enable the sockets, turn this paddle to the OFF position. When EPROMs are going to be used, make sure that jumpers J1 and J2 are properly placed, and paddles 7 and 8 are in the right position. Note that both sockets are enabled or disabled simultaneously; the board requires the EPROM to be 16 bits wide since the byte-swapper will not work on the EPROM.

Paddles 7 and 8 - These paddles determine the size of the address space that will select the on-board EPROM sockets. The EPROM address space ends at FFFFFFH and starts between 4K and 32K bytes (2K and 16K words) below the top of the 16 Megabyte address space. Therefore, when using two 2716 2Kx8 EPROMs, flipping both paddles ON would choose a 4K byte address space and EPROM would appear from FFE000H to FFFFFFH. For a discussion of how to use the EPROM effectively in either real address normal or protected address mode, see "Software Considerations".

Size	2Kx16	4Kx16	8Kx16	16Kx16
EPROMs used (2)	2716	2732	2764	27128
P7 position	ON	ON	OFF	OFF
P8 position	ON	OFF	ON	OFF

JUMPERS

There are five jumpers on the CPU 286. Jumpers J1 and J2 are located next to U13, and are three pins each. J1 is labeled A-C-B from the top, and J2 is labeled B-C-A from the top. Jumper J3 is next to U30 and is a set of 6 two pin pairs (A at the top through F at the bottom, right above J4). Jumper J4 is a single two pin pair located below J3. Do not mistake J4 for the bottom of J3. Jumper J5 is also a single 2 pin pair located near the edge connector below U35.

J	Position	Function
1		EPROM SIZE SELECT (A14)
2		EPROM SIZE SELECT (A12)
3	A	1 MEMORY WAIT STATE (MINIMUM)
	B	1 I/O WAIT STATE (MINIMUM)
	C	2 MEMORY WAIT STATES
	D	2 I/O WAIT STATES
	E	2 ON-BOARD EPROM WAIT STATES
	F	4 ON-BOARD EPROM WAIT STATES
4		TWO CYCLE MEMORY FETCH DIAGNOSTIC MODE (Should never be installed by user)
5		MWRITE GENERATION BY CPU 286

Jumpers J1 and J2 - These jumpers select the proper pinout for the various EPROMs that can be installed in the on-board sockets. The standard CompuPro configuration mentioned in the first section of this manual (both shunts A to C) is for 2716 type EPROMs. The positions for other types is shown below:

EPROM Type		2716	2732	2764	27128
Jumper	J1	A-C	A-C	A-C	B-C
	J2	A-C	B-C	B-C	B-C

Jumper J3 - This jumper has 6 positions: A through F. To select how many wait states the given space (I/O, Memory, ROM) has, install a jumper in the proper location. A space without a jumper will insert seven wait states whenever that space is accessed. Therefore, since all systems access both memory and I/O space, install at least two jumpers to minimize wait time. When ROM is installed in the on-board sockets, one more shunt will be necessary.

One or two wait states should be quite adequate for most memory or peripherals to respond (either with results or by asserting a RDY line), but if it becomes necessary to increase the on-board waits for either memory or I/O, please call CompuPro's Technical Support for help.

If more than one shunt is placed for waits in a given space, i.e.: both 1 and 2 memory wait state shunts are installed, the least number will be used, that is, 1.

The standard CompuPro configuration is to install the top two shunts, positions A and B. This gives plenty of time for all CompuPro memory and peripherals to respond.

Jumper J4 - This jumper is used at CompuPro as a diagnostic tool. If this jumper is installed, the CPU 286 executes illegal S-100 bus cycles and does not conform to the IEEE 696/S-100 standard. It should never be installed by a user in a working system.

Jumper J5 - This jumper has no pins. It is a normally closed connection that allows the CPU 286 to drive the MWRT signal onto the S-100 bus pin 68. In older IMSAI type systems, MWRT was often generated by the front panel and needed to be disconnected on the CPU. If it is ever necessary to use this feature to disable MWRT, the trace under J5 can be cut and pins installed to reconnect it when necessary. Pin 3 on buffer U34 can also be removed from the socket to achieve the same result. Systems using only CompuPro boards will never need this modification and should leave J5 as it was shipped.

INSTALLING AN 80287 NUMERIC PROCESSOR EXTENSION

The CPU 286 is designed to accept the 80287 Numeric Processor Extension (NPX) chip made by Intel. Unlike the 86/87 pair, the 80287 can run at any speed with respect to the 80286. The crystal oscillator is set to run the 80287 at 5 MHz. The price paid for this flexibility is the loss of some I/O ports to the 80287. Ports 00F8H through 00FFH are decoded on the CPU 286 and cannot be used on the S-100 bus. See "Software Considerations" for further discussion.

The socket for the 80287 has been fully tested by CompuPro and is ready to accept a 5 MHz 80287. To install the 80287, plug the part into the 40 pin socket labeled U17. No board modifications are necessary. Once installed, the 80286/80287 pair become object code compatible with the 8086/8087.

If you are not familiar with hardware or have never inserted a large IC into a socket, the time to learn is not with a several hundred dollar part; it is too easy to break a pin and ruin the IC. Return your board to CompuPro for an upgrade, and we will run a complete test on the board and numeric processor.

THEORY OF OPERATION

This section of the manual will explain, in general, how the circuitry on the CPU 286 works. In the following discussion, it will be helpful to refer to the schematic diagrams in the appendix.

The CPU 286 is based on the Intel 80286 CPU. The clock for the CPU is generated by the 82284 clock generator IC (U5). It uses an external oscillator consisting of two inverters, crystal X2, capacitors C10 and C11, inductor L2, and resistor R4. The crystal is a fundamental type, and is twice the desired processor frequency. For example, to run the CPU at 6 MHz, a 12 MHz crystal would be used. If the crystal value is changed, the value of C11 must also be changed.

The clock output of the 82284 is double the actual processor clock speed, and is divided by two inside the 80286 to get to the processor clock. The CLK and CLK* signals are used by 80287 to give it a sampling edge for its processor signals (HLDA, S1*, S0*, etc.) and by the S-100 bus controller unit to synchronize it with the 80286. An actual processor speed clock (PCLK) is generated by the 82284, but its worst case performance is unacceptable for an S-100 bus ϕ. Therefore PCLK from the 82284 is reconditioned by U11 and U22 to form a clean PCLK and Bϕ. Bϕ is buffered by U34 to get S-100 Bus ϕ. The TRI-STATE enable of this buffer is driven by the inverting output of flip flop U33b. The D and CLR inputs to this flip-flop are driven by the CompuPro defined bus line ϕDSB* on pin 21 of the S-100 bus. This line will be driven low by a temporary master coincident with the CDSB* signal (which is just after the rising edge of the clock). This will immediately cause the bus clock to be TRI-STATEd. Pull-up SR2 makes sure that it floats to the high state, but the temporary master should be driving the clock now anyway. When the temporary master relinquishes the bus, it will drive CDSB* high and float its clock high. Flip-flop U33b will then be free to enable the CPU 286's clock, but not until after the next rising edge of it. This ensures that there are no slices on the clock line.

The 80286 (U14) and the 80287 (U17) communicate via eight I/O mapped ports, the PEREQ and PEACK* (peripheral request and acknowledge), BUSY* and ERROR*, and several processor status signals (S1*, S0*, HLDA, C/I*, READY*, and CLK). When the 80286 sees an ESC instruction dealing with the 80287, it should check the status of BUSY*, and if the 80287 is not currently busy, instruct the NPX to execute a command. When the 80287 requires data from memory, it can assert PEREQ at which time the 80286 will perform the transfer. Intel has defined the 80287 I/O ports to reside at 00F8H to 00FFH. Comparator U12 and NAND gate U23 decode these I/O ports and feed the NPS1* and NPS2 inputs of the 80287. With this circuitry, the I/O ports the 80287 occupies are excluded on the S-100 bus.

The two 74F175 D flip-flops (U2 and U22) along with their respective 12L6 PALS (U1 and U21) generate the synchronization timing between the 80286 and S-100 bus. PAL 201P-3 (U1) and D flip-flop (U2) produce strobes DBIN and WR* for the S-100 bus, and I/ORD* and I/OWR* for the 80287 NPX. The HLDA strobe is produced directly by the 80286; the STVAL* strobe falling edge is produced on the rising edge of CLK during SYNC by U33a; the SYNC strobe is produced in PAL 201P-2 (U21) and synchronized through D flip-flop U22. PAL 201P-2 (U21) also produces ALE to gate the three address latches (U4, U13, and U24) which are then buffered to the S-100 bus by TRI-STATE drivers U37 and U38. All of the strobes are buffered by a 74LS367 (U36) to the S-100 bus.

PAL 201P-2 (U21) includes the WAIT state logic necessary to handle both onecycle and twocycle fetches. A onecycle fetch is when the processor requests either 8 or 16 bits from memory and the memory is able to handle the transfer in one S-100 bus cycle. A twocycle fetch is when the processor requests 16 bits from the memory but the memory is only able to transfer 8 bits, forcing the internal finite state machine to complete two S-100 bus cycles to fetch two bytes before allowing the 80286 to complete its cycle. A twocycle fetch is also called a byte serial fetch. The decision to execute either a onecycle transfer or twocycle transfer is controlled by the S-100 signals sXTRQ* and SIXTN*.

The sXTRQ* line is generated by the latched OR of the signals BHE* and A0. If BHE* and A0 are low, and it's not an interrupt acknowledge cycle, a sixteen request will be generated. If SIXTN* goes low, indicating that a 16-bit transfer can occur, the output of U20 (pin 12) will go high, causing the ONECYCLE signal to be true. This signal tells the CPU to complete the 16-bit transfer at full speed. If the SIXTN* signal stays high, U20's output (pin 12) will be low causing the ONECYCLE signal to be false. This starts a process whereby the CPU 286/287 will halt the 80286 and read or write two bytes serially.

The twocycle is performed by the state machine consisting of U9, U19, U20, U31b, and part of PAL U21, which generates the signals STBINH, TWOCYCLE, END, RDY, and FLIP. These are used to sequence the logic on the board to run the two bus cycles. STBINH* is produced by PAL U21 during the last cycle that strobes are to be asserted, and is fed to PAL U1 to cause the strobes to fall. It is also used to generate END during the second half of a twocycle. TWOCYCLE is asserted by U9b when the first SYNC* falls and the external memory has not yet produced SIXTN*. RDY is generated on PCLK when the S-100 and internal wait state generator are ready (U10 pin 8 high), and is used to terminate the first half of a twocycle without ending the 80286 wait state. FLIP signals the start of the second half of a twocycle, and is produced by U9a when strobes fall and TWOCYCLE is asserted. Finally, the signal CA0 (corrected A0 to the S-100 bus) is fed directly from LA0 to the S-100 bus like the rest of the address lines during a onecycle, but is asserted high by FLIP during the second half of a twocycle to enable access of the high address.

The data bus is buffered, multiplexed and latched (depending on what is required) by U15, 16, 27, and 28. The control of these buffers and latches is performed by a 14L4 PAL 201P-1 (U18). LS1* determines the direction of data (transmit or receive) and goes to the direction inputs of the the main data bus buffers (U27 and U28). The signal DEN* coming from PAL U21 determines when data can be put on the CPU 286's internal bus or the S-100's data bus. The rest of the inputs to the PAL control which of the various buffers are enabled. The LA0, LBHE* and LS1* signals control the basic 16-bit cycles, while the FLIP and TWOCYCLE signals control the buffers during a byte serial transfer. The INTAK signal routes the byte data correctly during interrupt acknowledge cycles. Note that 8 bits are latched by U16 on the falling edge of DBIN during the first half of a twocycle fetch, and are asserted onto the D0-D7 bus during the second half.

The S-100 status lines are generated by a 74S288 bipolar PROM. The four status lines from the CPU (S0*, S1*, C/I*, M/IO*) are latched by U39. The outputs of U39 go to four of the address inputs of the PROM. The PROM then decodes the proper status and puts it out on its data output lines O1-7. Data output O8 is used to generate 1 wait state in the shift register U30, and should be high at all times. Since the 80286 without wait states would complete the bus access in 2 CLK cycles producing an illegal S-100 bus cycle, 1 wait state must be added to every S-100 access. To eliminate this wait state bring WAIT1 low in memory accesses only and generate an illegal S-100 bus cycle. To do this, pull the PROM address A4 low. The S-100 status lines are buffered by U41.

The internal wait state generator is controlled by the 8-bit shift register U30. When the strobes are unasserted, the register is loaded with the data presented at its inputs. This data should be all high except for a low in A and another low in either D, F, or G. When the strobes are asserted, the register clocks out states with Bϕ until a low is found. When it is found, WAIT* goes high and the cycle ends. By selecting the proper status to feed to the shift register, different wait states can be selected for different spaces (memory, I/O, ROM). If no status is presented, then every 7cycle will have to wait until A is shifted down to QH*, causing wait states.

A bug in some of the early steppings (B1 and before) of the iAPX 286 caused bizarre results if a HOLD was requested and acknowledged in between the two INTAK cycles that the 80286 performs in response to INTR. D flip-flop U31a and NOR gate U32 simply exclude HOLD on the S-100 bus from reaching the 80286 from the first INTAK bus read until a memory write occurs (MWRS*). This will always occur when the 80286 pushes the PC on the stack. In later steppings with the bug fix, U31a pin 6 could be removed from the socket and U32 pin 2 tied low.

The on-board EPROM sockets are decoded by a 13 input NAND gate (U3) and 2 OR gates (U8). This places the EPROMs in high memory. Switch S1 position 4 disables the EPROM sockets by pulling one input of the NAND gate low. Position 7 and 8 decide whether LA13

and/or LA14 are decoded by the EPROMs or are required to be high for access. Jumpers J1 and J2 select the pinouts for the sockets. 2716s require Vcc to pin 23 of the socket, and 27128s require LA14 to pin 26 of the socket.

Three sections of U42, buffer U44, one section of U43 (the D flop-flop) and crystal X3 (4 MHz), provide a 2 MHz clock for the S-100 CLOCK signal on pin 49. A separate oscillator was used so that CLOCK will always be 2 MHz independent of the CPU frequency.

The power fail circuit causes a POC* to be issued upon the rising edge of PWRFAIL*. This insures that the system will recover just as if the power had come on for the first time, and prevents problems that might occur if the power dips for a short period causing PWRFAIL* to be asserted, but the power doesn't actually go away.

This completes the "Theory of Operation" section of this manual.

SOFTWARE CONSIDERATIONS

The iAPX 286 software is upward compatible with the iAPX 8086 and iAPX 8088. This feature makes the iAPX 286 very attractive to users who have an investment in 8086/8088 code and who need a higher performance processor. While we were able to bring up 99% of our existing 8086/8088 software with the 80286, several problems did emerge.

First, the 80286 is substantially faster than the 8086, and due to the optimization of the pre-fetch queue, often executes bus cycles in a different order than the 8086. To see where this is a problem, consider initializing a part such as Intel's 8259A interrupt controller. While the 8086 executes the 3 byte initialization sequence as such:

1. Fetch first operand
2. Output first operand
3. Fetch second operand
4. Output second operand
5. Fetch third operand
6. Output third operand

the 80286 executes this:

1. Fetch first operand
2. Fetch second operand
3. Output first operand
4. Fetch third operand
5. Output second operand
6. Output third operand.

Although the actual order that the 8259A receives the bytes is the same for both (as it must be), the minimum time between outputs is reduced since no bus cycle is run between the second and third output. The 8259A requires a minimum time between command bytes, and with the faster 80286, this time is not met. One solution to this problem is to force the 80286 to run a bus cycle between every output. The above example used immediate operands as initialization bytes, allowing the 80286 to pre-fetch and use them quickly. By putting the initialization bytes into a small table and fetching them individually for every output, the 80286 will be forced to run at least one bus cycle (the operand fetch) between every output. This will easily satisfy the 8259A minimum.

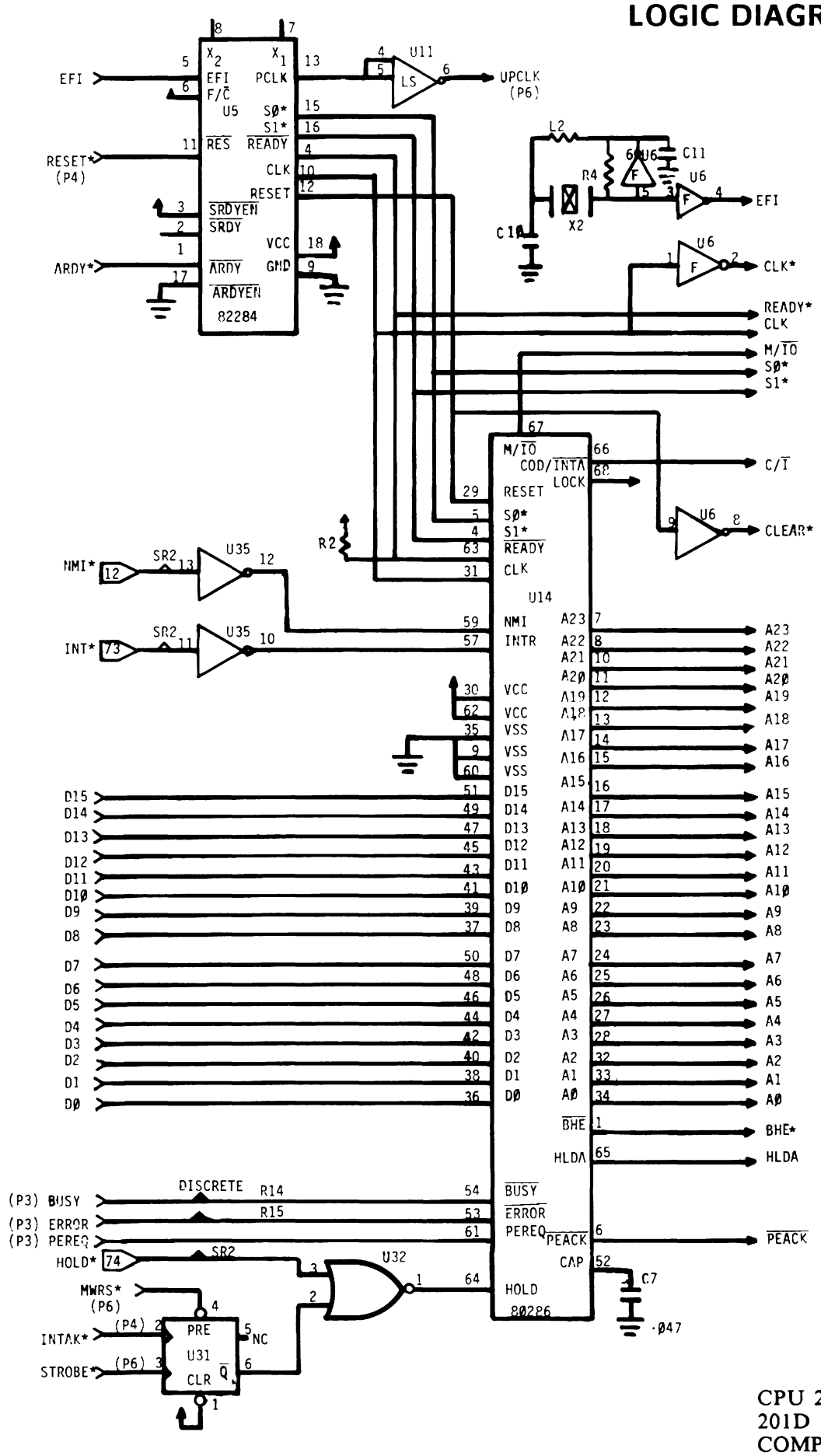
The second difficulty is with Intel's decision to I/O map the 80287 Numeric Processor Extension into ports 00F8H to 00FFH. From a hardware standpoint, this was a logical thing to do, as it allowed the NPX and CPU to run at different speeds. The problem is that any software that accesses these ports will both mess up the 80287 and not be mapped onto the S-100 bus. The best solution is to relocate the conflicting S-100 boards in the system to a different location. This is the only solution if the NPX is to be used. If it is

completely impossible to relocate these ports, and the 80287 will never be used, a last resort hardware modification is required.

Finally, the 80286 initializes and starts execution at location FFFFF0H. Notice that this is a 24 bit address, not a 20 bit address, as the 8086/8088 produces. This is not a problem in complete CompuPro systems, as the boot EPROM on the DISK1/1A appears in every 64K page while PHANTOM* is asserted during boot up. Second, while in real address mode, since the 80286 does not know what to do with the most significant 4 bits (A20-A23), it leaves them high on boot until a LONG JUMP is executed, i.e. one that loads the CODE SEGMENT, at which time it sets the 4 bits low. Note that if the boot code is in the on-board EPROM, that code can not execute any long jumps, or it will jump right out of the EPROM's address space. Also note that once out of the EPROM, the program can never get back until going into the protected address mode.

This completes the "Software Considerations" section of this manual.

LOGIC DIAGRAM 1 of 6



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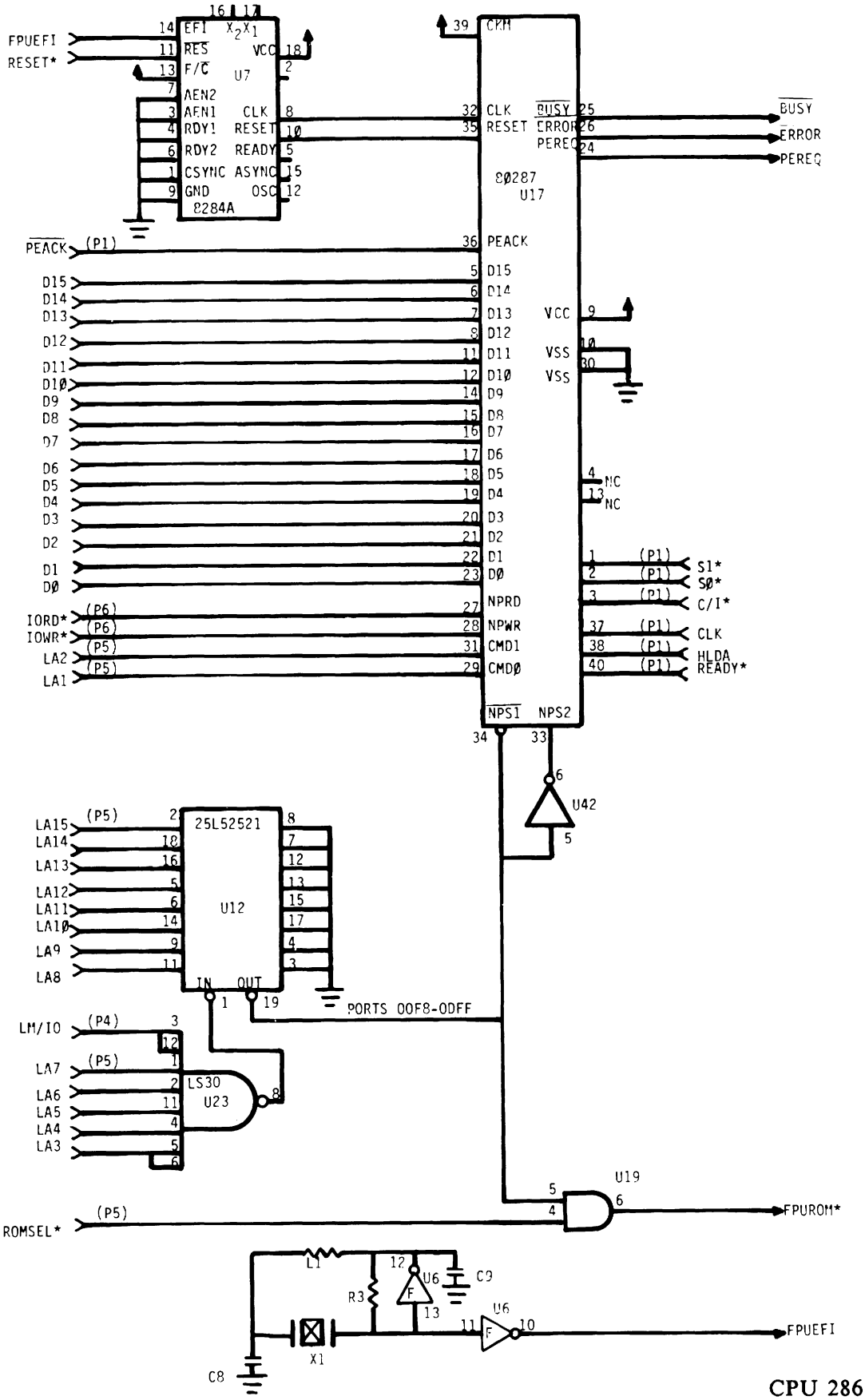

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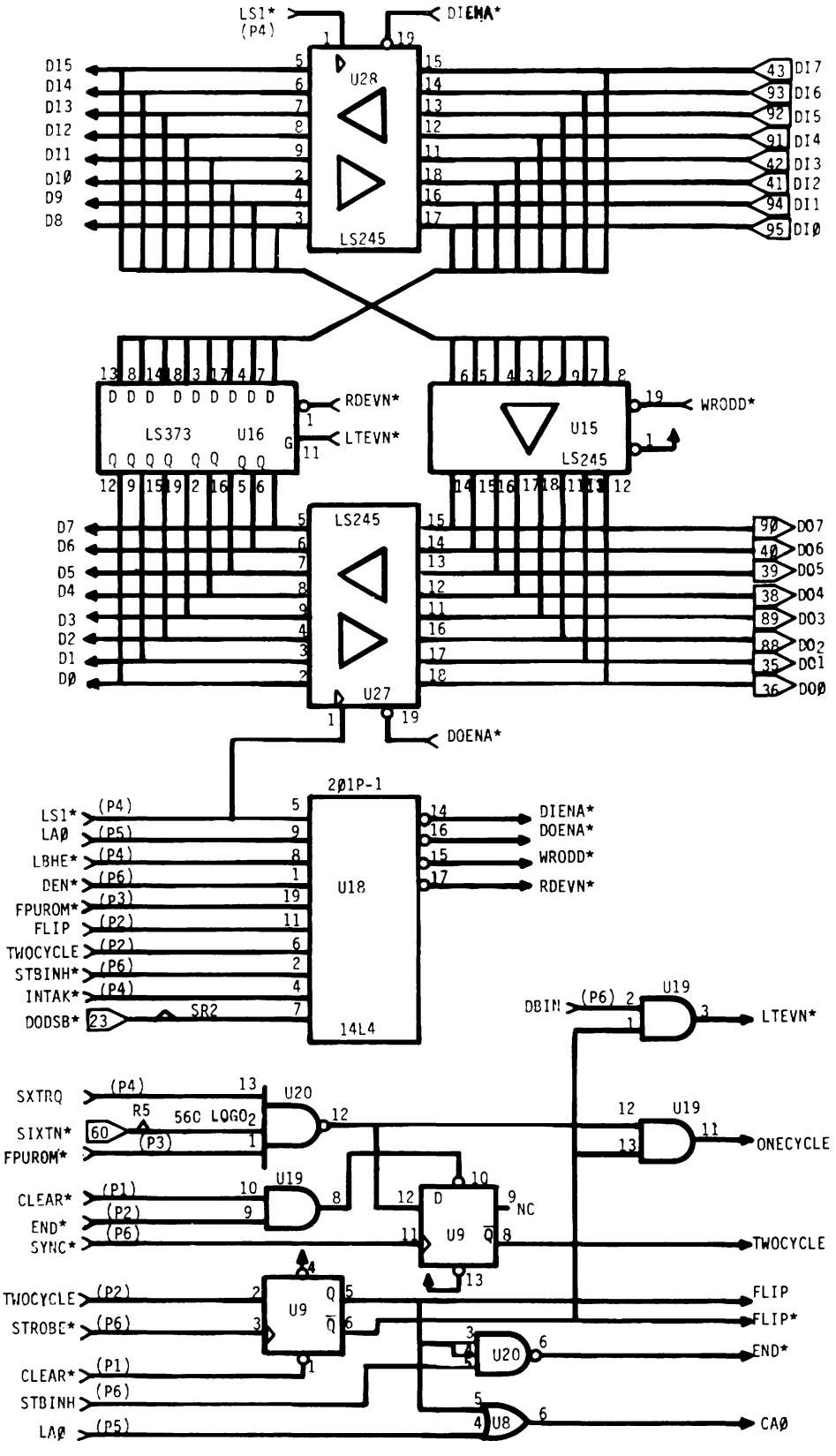

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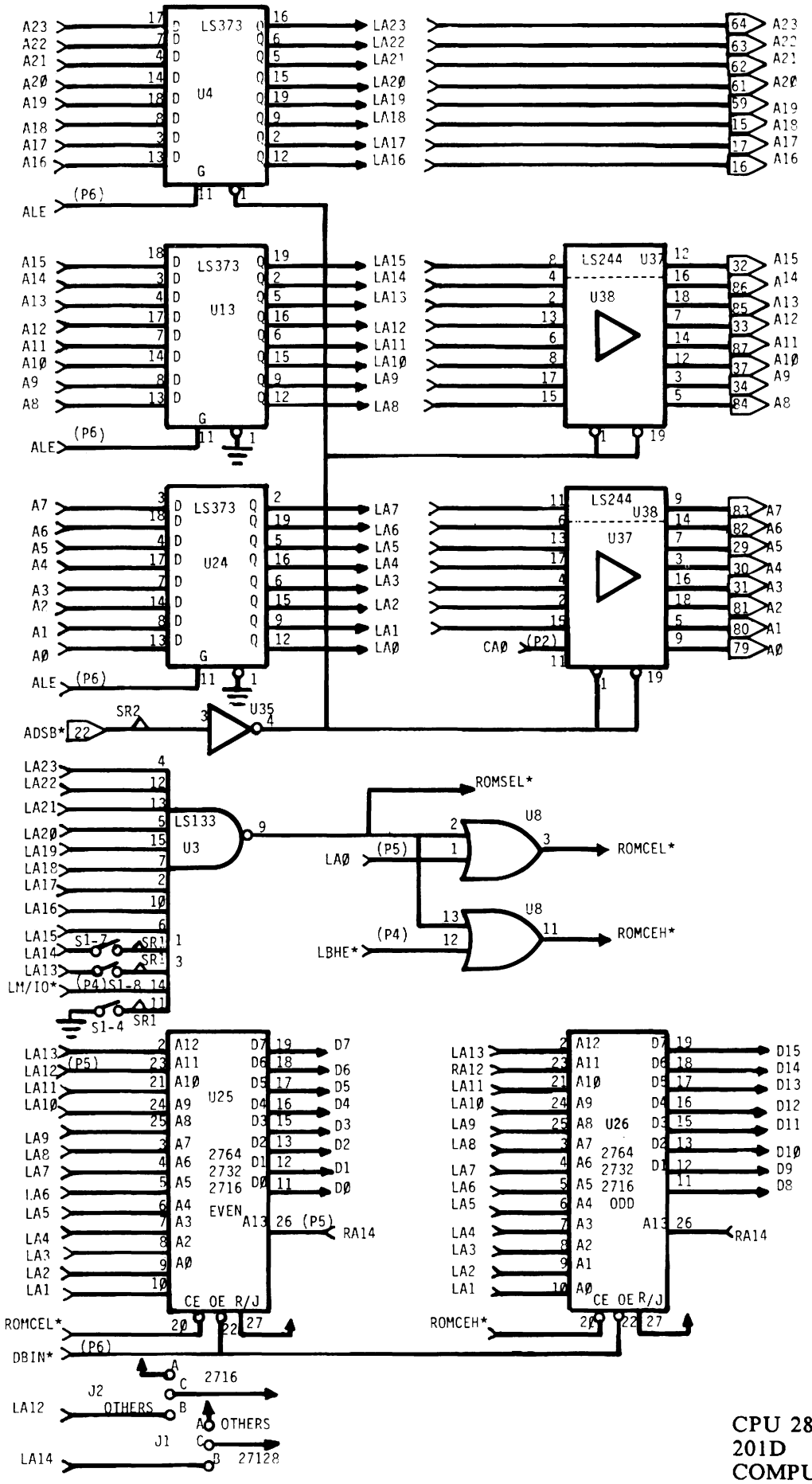

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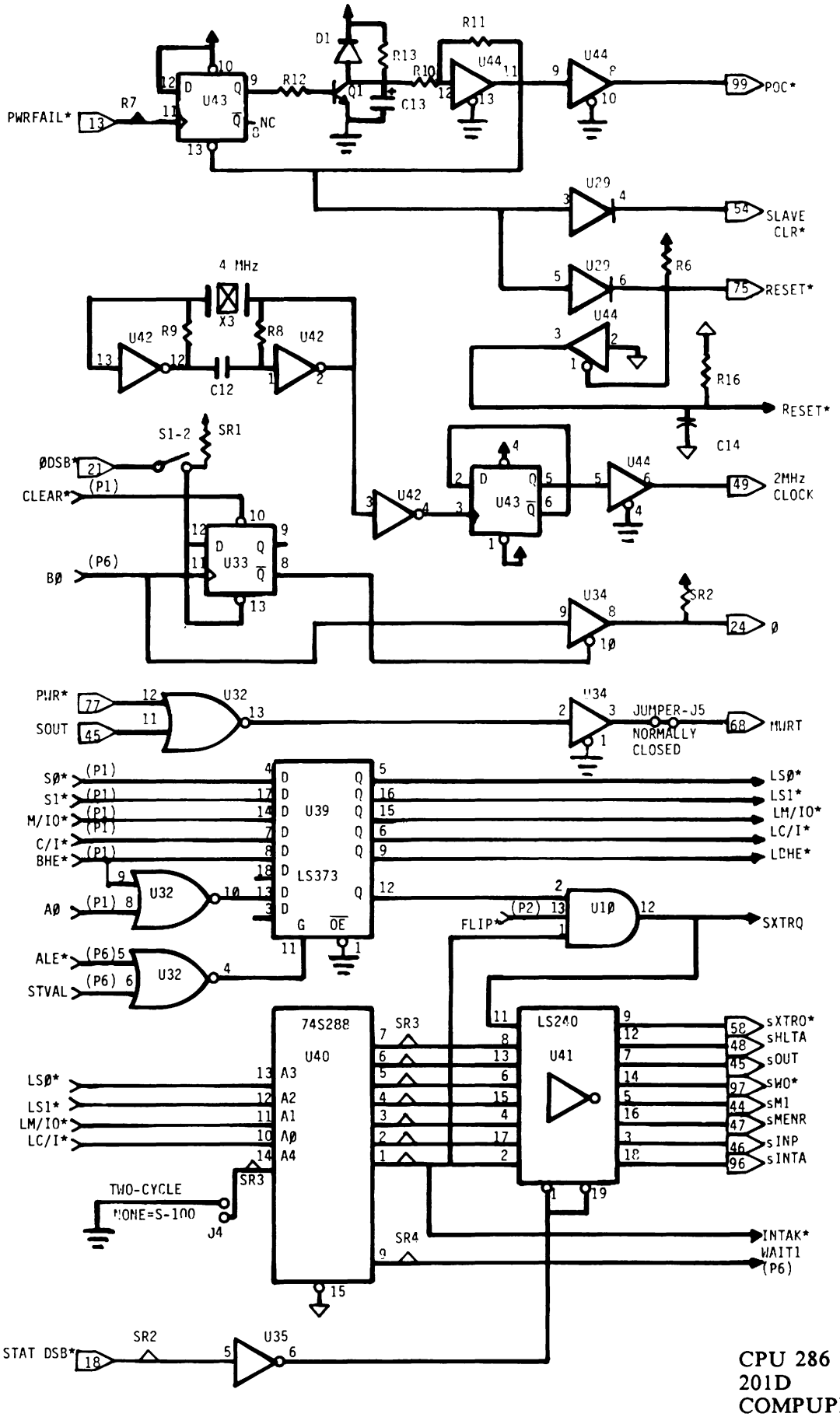

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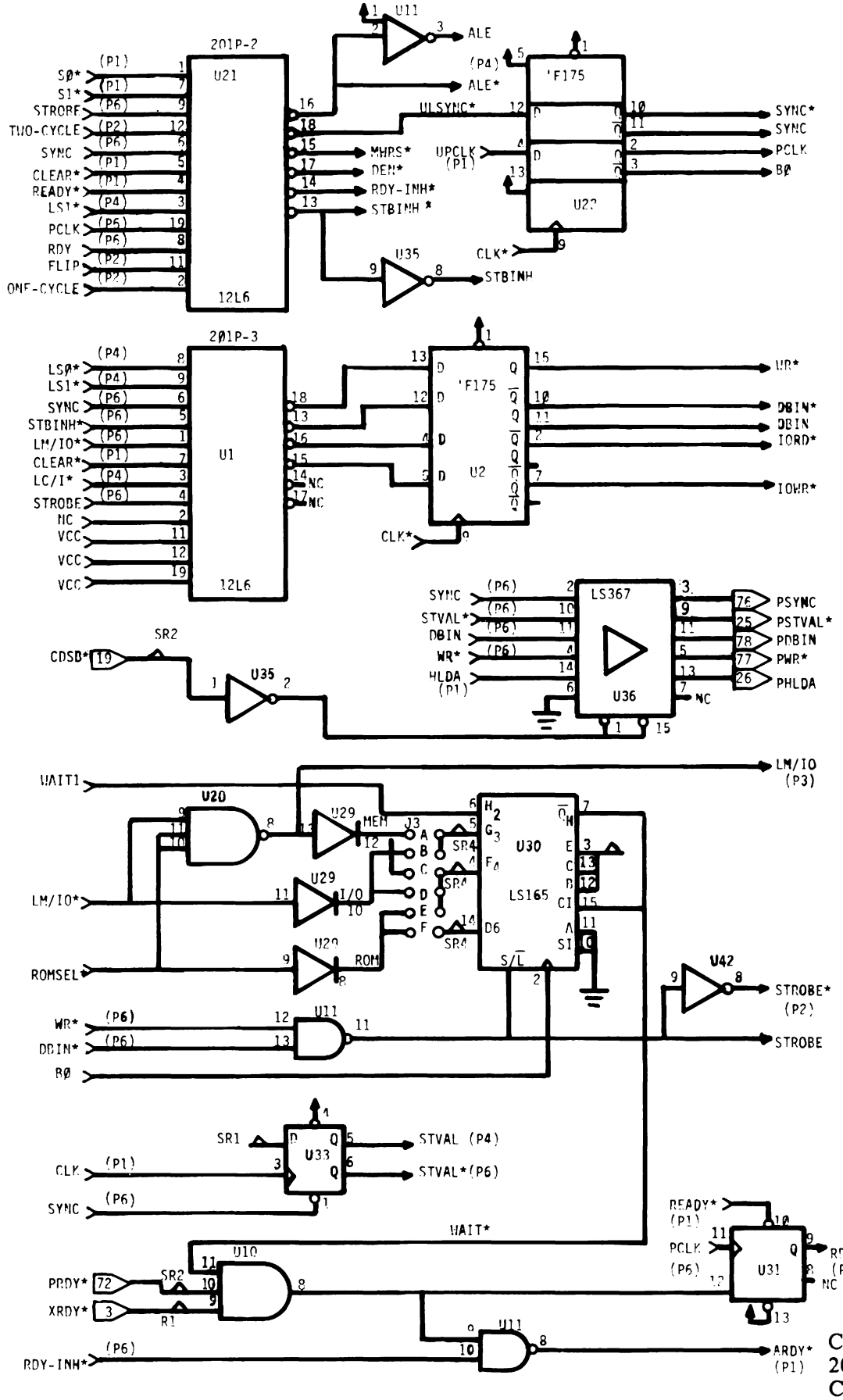

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PARTS LIST

Integrated Circuits

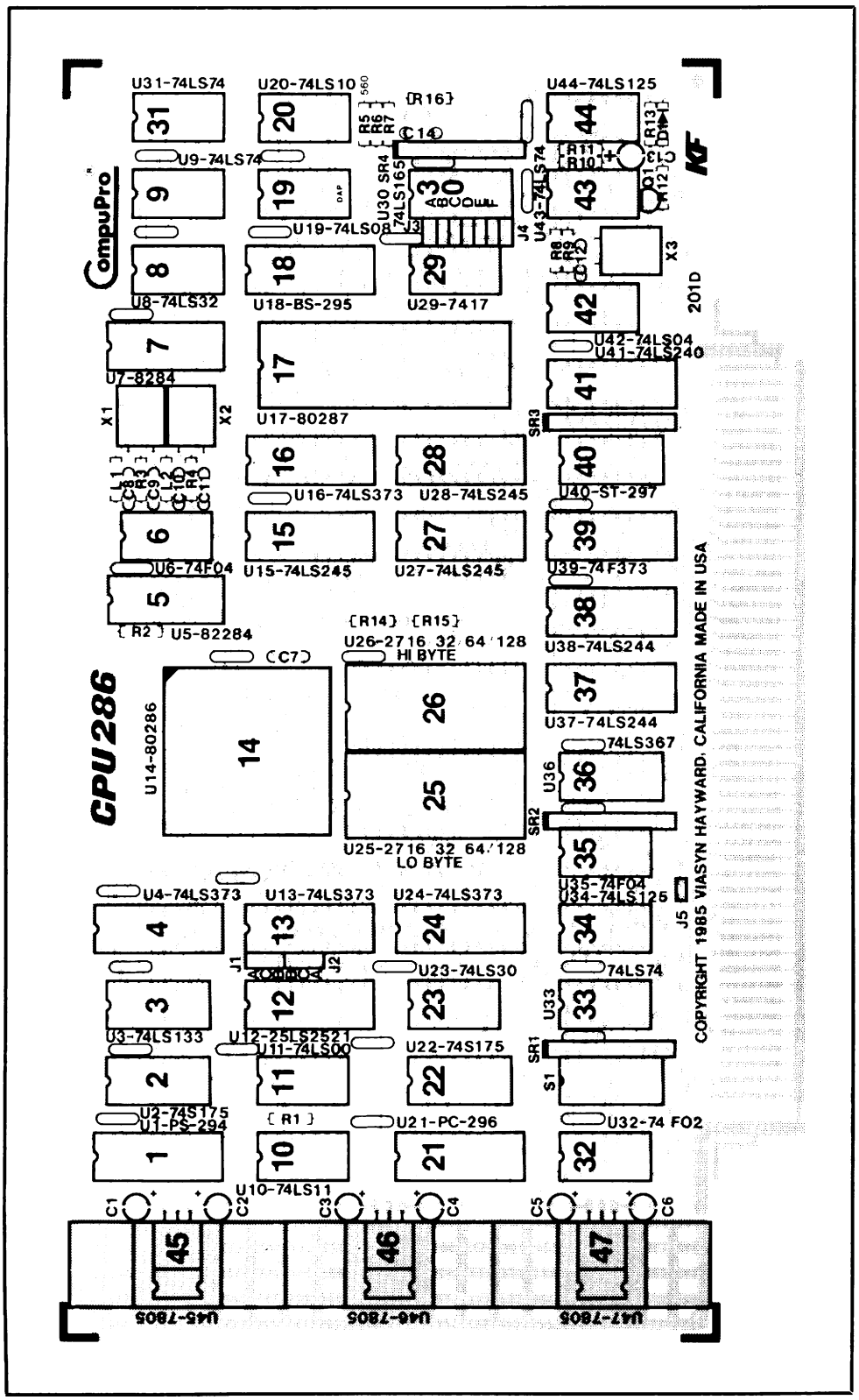
QTY	DESCRIPTION	
1	74LS00	Quad 2 input NAND (U11)
1	74F02	Quad 2 input NOR (U32)
1	74LS04	Hex inverter (U42)
2	74F04	Hex inverter, fast (U6,U35)
1	74LS08	Quad 2 input AND (U19)
1	74LS10	Triple 3 input NAND (U20)
1	74LS11	Triple 3 input AND (U10)
1	7417	Hex buffer O.C. (U29)
1	74LS30	Eight input NAND (U23)
1	74LS32	Quad 2 input OR (U8)
4	74LS74	Dual D flip-flop (U9,U31,U33,U43)
2	74LS125A	Quad TRI-STATE buffer (U34,U44)
1	74LS133	13 input NAND (U3)
1	74LS165	8 Bit shift register (U30)
2	74LS175	Quad latch, fast (U2,U22)
1	74LS240	Octal TRI-STATE inverter (U41)
2	74LS244	Octal TRI-STATE buffer (U37,U38)
3	74LS245	Octal transceiver (U15,U27,U28)
1	74LS367A	Hex TRI-STATE buffer (U36)
5	74LS373	Octal transparent latch(U4,U13,U16,U24,)
1	25LS2521	Octal comparator (U12)
1	74F373	(U39)
1	80286	High performance 16 bit processor (U14)
1	80287	Numeric Processor Extension(U17)(Optional)
1	82284	iAPX 286 clock generator (U5)
1	8284A	Clock generator (U7)
2	12L6	12 In, 6 Out PAL (U1,U21)
1	14L4	14 In, 4 Out PAL (U18)
1	74S288	32x8 bipolar PROM G201x (U40)
2	2716/128	2K to 16K x8 EPROM (U25,26) (Optional)
3	7805	Positive 5 volt regulator (U45,U46,U47)

Other Electrical Components

2	Sip resistor 4.7 or 5.1K ohms (SR1,SR3)
2	Sip resistor 1.5K ohms (SR2,SR4)
1	270 ohm resistor (R10)
1	300 ohm resistor (R2)
1	560 ohm resistor (R5)
4	1K ohm resistor (R3,R4,R8,R9)
3	1.5K ohm resistor (R1,R6,R7)
1	2.7K ohm resistor (R11)
1	4.7K ohm resistor (R13)
1	10K ohm resistor (R12)
2	22K ohm resistor (R14,R15)
6	>3.3 mfd tantalum radial cap 10v (C1-6)
1	>10 mfd tantalum radial cap 10v(C13)
1	.047 mfd ceramic disc cap (C7)
1	.01 mfd ceramic disc cap (C12)
28	bypass cap (all unmarked)
2	220 pF silver mica cap (C8,C9)
1	270 pF silver mica cap (C11)
1	390 pF silver mica cap (C10)
1	1 uH inductor (L1)
1	0.47 uH inductor (L2)
1	4 MHz crystal (X3)
1	15 MHz NPX speed x3 crystal (X1)
1	CPUx2 processor crystal (X2)
1	1N914 or equivalent diode (D1)
1	2N3904 transistor (Q1)

Mechanical Components

17	14 pin sockets
6	16 pin sockets
2	18 pin sockets
15	20 pin sockets
2	28 pin sockets
1	40 pin socket
1	68 pin leadless socket
1	8 position dip switch (S1)
1	7 Long Double row pins (J3,J4)
1	6 Long Single row pins (J1,J2)
3	Heatsinks
3	6-32 x 3/8" screws
3	6-32 hex nut
3	6-32 lock washer
1	PCB #201
2	card ejectors
1	technical manual



COMPONENT LAYOUT

(The CompuPro People)

12014/4 3506 Breakwater Court, Hayward, CA 94545 (415) 786-0909 135300D