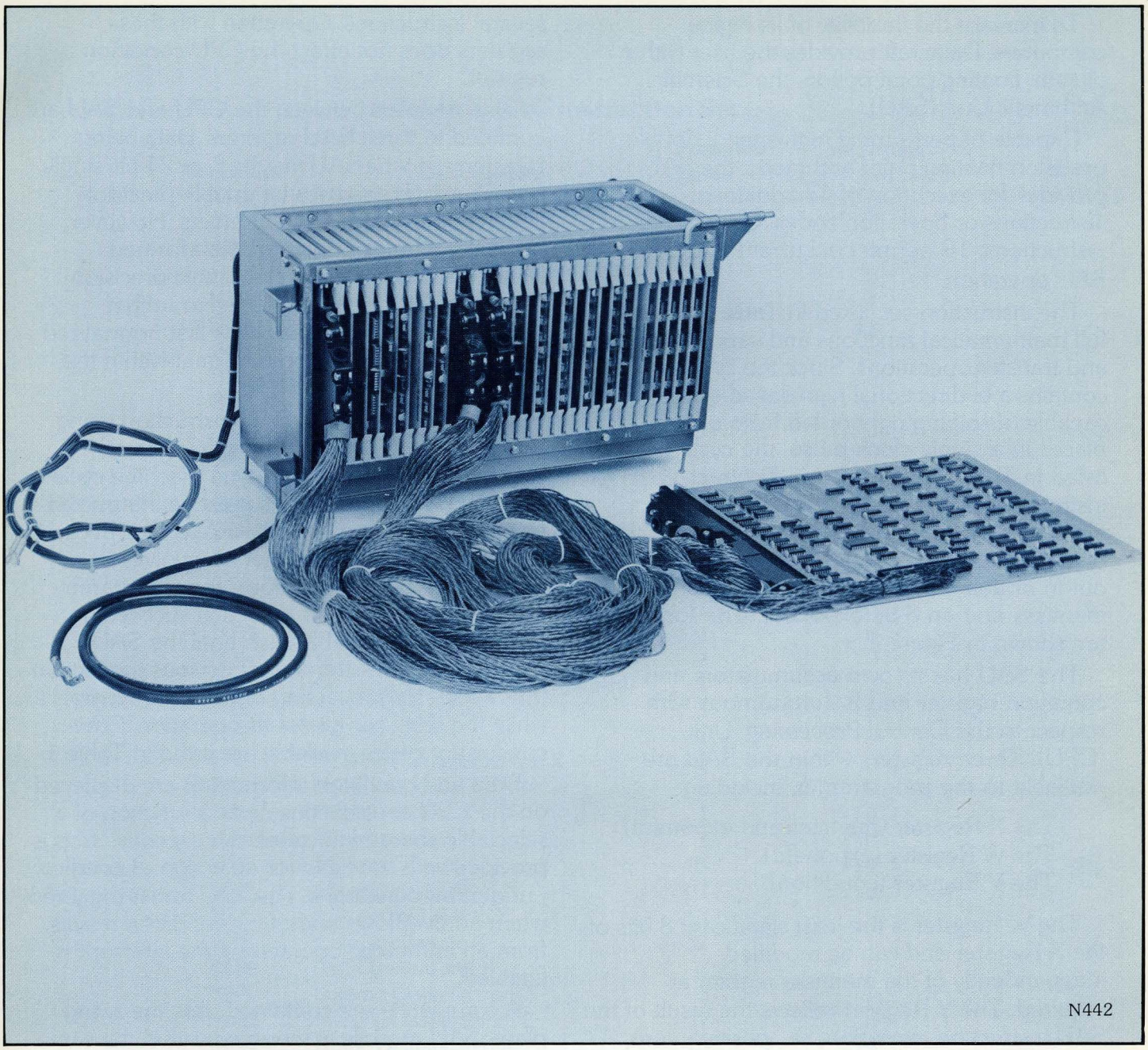

SCIENTIFIC ARITHMETIC UNIT

PRODUCT BULLETIN

FEATURES

- **47 Individual Operations**
- **Super-fast Double Precision**
- **Compact Package**
- **Simple Interface**

Datacraft®

To increase the flexibility of its digital computers, Datacraft provides the user with a plug-in, floating-point option, the Scientific Arithmetic Unit (SAU).

Capable of performing high-speed, double-precision floating point arithmetic, the SAU provides for execution of 47 additional instructions or operation codes. Of these 47 instructions, 19 permit concurrent computer/SAU operation.

The instruction set, listed in Table 1, includes full mathematical functions and various branch and transfer operations. Since the SAU contains a bi-directional high-speed scaler capable of shifting right or left from one to 38 places in a single clock pulse, the cycle times listed in Table 1 for Add and Subtract instructions are absolute (no extra cycles for alignment of exponent or normalizing the result). All arithmetic operations are carried out in double precision format to yield a 39-bit mantissa and an 8-bit exponent. The formats are shown in Figure 1.

The SAU has its own accumulators and condition register and is autonomous with respect to the Central Processing Unit (CPU). Three registers within the SAU are available to the programmer, including:

The X Register (mantissa and exponent).
The W Register (exponent).
The Y Register (condition).

The W Register is the least significant 8 bits of the X Register and can be modified independently of the mantissa register as required. The Y Register reflects the result of the SAU instruction execution, i.e., positive, zero, negative and/or overflow. General instructions set the overflow bit as well as one or more of the remaining bits if an error occurs. The A and D register of the CPU are available to the SAU via several instructions. Operation with these registers does not effect the CPU condition register.

Data transfers between the CPU and SAU are confined to three SAU registers. Data being transferred to the SAU may be 8- or 24-bit, single-precision integers or 48-bit double-precision floating-point normalized numbers. However, since all arithmetic operations performed within the SAU are done in double-precision floating-point format, any integer number transferred for arithmetic use is first normalized and placed in floating-point format within the SAU.

Depending upon the SAU instruction being executed, the SAU and CPU can operate concurrently for more than one machine cycle. CPU and SAU instructions must be intermixed to take advantage of the available cycles. In cases where the instruction sequence involves consecutive SAU instructions, the mainframe will convert the second and each succeeding instruction into a self-branch until the SAU completes processing of the previous instruction (this allows for processing of priority interrupts while the SAU completes its operation). The concurrent cycles available are listed in Table 1.

Data and condition information are displayed on the CPU control console as a function of selectable shared indicators. An executive trap is provided with the SAU for detection of overflow/underflow conditions. The SAU trap is triggered when an overflow/underflow condition results from an arithmetic operation if the interrupt is enabled.

A completely self-contained unit, the swing plane SAU module is mounted within the same rack assembly as the CPU. Since the Datacraft CPU's are prewired for SAU operation, the add-on may be performed on site as the user requires.

Table 1. SAU Instruction Set

Mnemonic	Description	Mainframe Cycles	Concurrent Cycles Available
TMX	Transfer Memory to X	3	0
TXM	Transfer X to Memory	3	0
AMX	Add Memory to X	3	0
SMX	Subtract Memory from X	3	0
MMX	Multiply Memory by X	7	4
DMX	Divide Memory into X	16	13
BOX	Branch on SAU Ready	1	0
BNR	Branch on Negative Reset	1	0
BNS	Branch on Negative Set	1	0
BZR	Branch on Zero Reset	1	0
BZS	Branch on Zero Set	1	0
BPR	Branch on Positive Reset	1	0
BPS	Branch on Positive Set	1	0
BOR	Branch on Overflow Reset	1	0
BOS	Branch on Overflow Set	1	0
TYA	Transfer Y to A	1	0
TOY	Transfer Operand to Y	1	0
TOW	Transfer Operand to W	1	0
AOW	Add Operand to W (Exponent)	1	0
COW	Compare Operand to W (Exponent)	1	0
HSI	Hold SAU Interrupt	1	0
RSI	Release SAU Interrupt	1	0
FAX	Floating Normalize of A to X	1	0
PXX	Positive of X to X	1	0
NXX	Negative of X to X	1	0
TZX	Transfer Zero to X	1	0
INX	Inverse of X to X	15	14
SEX	Square of X to X	7	6
SRX	Square Root of X to X	13	12
CZX	Compare Zero to X	2	1
AOX	Add Operand and X	2	1
SOX	Subtract Operand from X	2	1
MOX	Multiply Operand and X	7	6
DOX	Divide Operand into X	15	14
AAX	Add A and X	2	1
SAX	Subtract A from X	2	1
MAX	Multiply A and X	7	6
DAX	Divide A into X	15	14
ADX	Add D and X	2	1
SDX	Subtract D from X	2	1
MDX	Multiply D and X	7	6
DDX	Divide D into X	15	14
IDX	Interchange D and X	2	0
CDX	Compare D and X	2	1
FXA	Fix of X to A	2	0
TDX	Transfer D to X	1	0
TXD	Transfer X to D	2	0

Specificiations subject to change without written notice

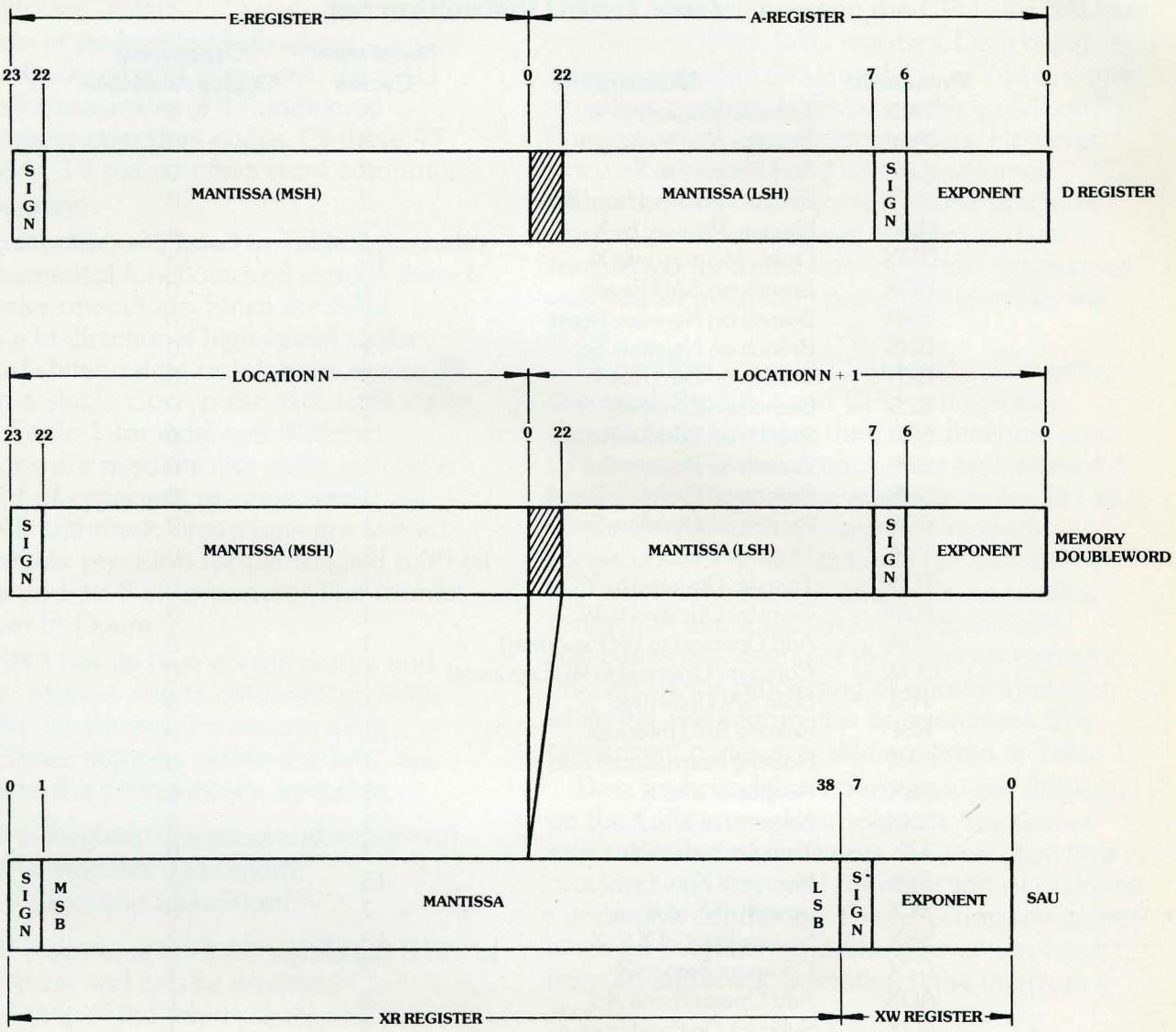

Figure 1 Floating-Point Formats MI1226-673

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