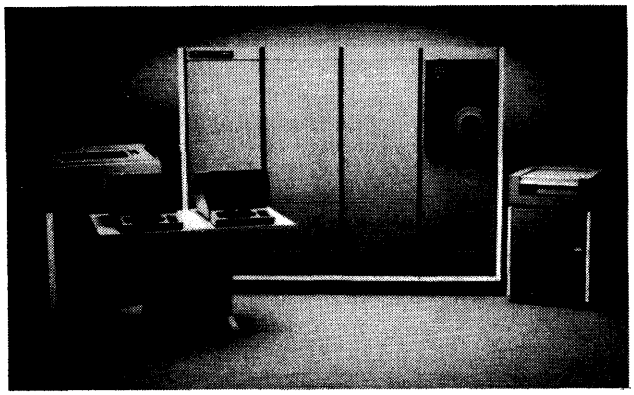
# Harris H800



The Harris 800 system above includes (left to right) a Model 4130 900-lpm printer, an operator console and MAP terminals, the H800 CPU with memory and I/O expansion cabinets, a Model 6890 nine-track magnetic tape drive, and a Model 5650 300-megabyte disk storage module.

**The H800, the most powerful member of the Harris family of virtual memory computers, features 48-bit architecture, over three megabytes of real memory, over twelve megabytes of virtual memory, and a 6K-byte cache memory. The basic system costs $165,900 with monthly maintenance priced at $1,095.**

**MAIN MEMORY: 384K to 3,072K bytes.**
**DISK CAPACITY: Resource dependent**
**WORKSTATIONS: Up to 128**
**PRINTERS: 240 to 1,200 lpm**
**OTHER I/O: Magnetic tape, punched card, paper tape**

## MANAGEMENT SUMMARY

Harris Corporation's Computer Systems Division came into being in January 1974 when Harris acquired the Datacraft Corporation, a minicomputer manufacturer. Harris continued to market Datacraft's Slash Series and introduced the Series 100 and 200 virtual memory systems, based on the Slash 4, Slash 6, and Slash 7 central processors.

Harris now offers three basic systems, the 100, 500, and 800. Each has a CPU, basic memory, and software. The systems were restructured and prices were reduced in 1979, primarily because of new memory prices reflecting Harris' use of 16K memory chips and the planned early use of 64K chips on the same memory boards.

The Harris 100, 500, and 800 systems form a series of compatible data processing systems and include a family of central processors, peripheral devices, and programming support systems. The processors share a common code structure and instruction formats, differing primarily in memory capacity, computational speed, numbers of instrucitons, and input-output throughput. The 800 is upwardly compatible from the 100 or 500, and the 800's instructions, character codes, interrupt facilities, and programming features are functionally identical to corresponding features on 100 and 500 processors. The three systems use the same operating system, making it possible to run on an 800 jobs which were originally designed for a 100 or 500. Users' programs for 100 and 500 systems can also be run on the 800.

The H800, the top of the line in the Harris family of virtual memory computers, features 48-bit pipeline architecture, a system bus which transfers data at a maximum 19-megabyte-per-second rate, over three megabytes of directly addressable real memory and over twelve ➢

## CHARACTERISTICS

**MANUFACTURER: Harris Corporation, Computer Systems Division, 2101 West Cypress Creek Road, Fort Lauderdale, Florida 33309. Telephone (305) 974-1700.**

**Founded in 1895 as a manufacturer of automatic printing presses, Harris Corporation is now a high-technology company supplying a broad range of equipment and services for communications and information handling. The Computer Systems Division came into being in 1974 when Harris acquired Datacraft Corporation, a minicomputer manufacturer.**

**MODEL: H800.**

**DATE ANNOUNCED: June 1979.**

**DATE OF FIRST DELIVERY: March 1980.**

**NUMBER INSTALLED TO DATE: Approximately ten have been shipped, but some are not yet completely installed.**

### DATA FORMATS

**BASIC UNIT: 8-bit byte or 6-byte word.**

**FIXED-POINT OPERANDS: 48-bit words. Data is represented in two's complement binary notation. Decimal arithmetic is performed on data in packed format with two decimal digits in each byte.**

**FLOATING-POINT OPERANDS: Double-precision (48-bit) floating-point operations employ a 39-bit mantissa and an 8-bit exponent. Quad-precision operations employ a 70-bit mantissa and a 24-bit exponent.**

**INSTRUCTIONS: Most instructions of the H800's set are a half-word in length. Direct addressing to 96K bytes, direct addressing to 192K bytes through long-address instructions, and indirect addressing to 768K bytes (data only) are provided in the Compatibility Mode. Direct, indirect, and indexed addressing to 3 million bytes are provided in the Address Extension Mode.**

**H800 systems use the same standard instruction set used by Harris' H100 and H500 systems. Operation codes are usually ➢**

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megabytes of virtual memory, a 6K-byte bipolar cache memory, integrated hardware floating-point mathematics, and support for up to 128 interactive terminals.

Harris claims that in final testing the H800 computed 1.8 times as fast as the 500. This ratio proved consistent through a multi-use mix of compiles and executes of FORTRAN, APL, BASIC, COBOL, and RPG II programs, all of which operated concurrently under Harris' virtual memory system, VULCAN.

The H800's main memory is expandable to over three megabytes in 192K-byte modules. Each memory module has its own timing and control logic and reads or writes forty-eight bits plus error-correcting bits in one memory cycle. The virtual memory system makes over twelve megabytes of logical address space available for application program use regardless of the actual physical memory available, and also provides hardware and software memory protection. The H800's 6K-byte cache memory allocates 3K bytes each to operands and to instructions. The cache reads or writes 48-bit data fields in one cache memory cycle. Although the effectiveness of cache memory depends on the nature of the executing programs, Harris claims that the typical cache hit ratio will be 90% or better. An optional Shared Memory System is available for multiple-processor configurations requiring rapid access to common data. Up to six ports are available, allowing as many as six processors to be connected to over three megabytes of memory. The combined main and shared memory available to any single computer is three megabytes.

Memory is accessed at the 48-bit, 24-bit, 8-bit, and single bit levels, and operations are performed on, and from, 48- and 24-bit data and instruction words. In addition, the H800 is capable of selective byte manipulation and performs Boolean functions on single, selected bits. Two's complement arithmetic is performed on parallel, binary, fixed-point, or floating-point operands. Fixed-point capabilities include hardware multiply, divide, and square root functions as well as 48-bit add and subtract operations.

The VULCAN operating system is a priority-structured, demand-paged, multi-programming, multi-lingual virtual memory operating system which supports concurrent operation of multi-stream batch processing, interactive time-sharing, data base management, remote job entry, remote job hosting, and real-time processing. VULCAN supports the Harris Macro Assembler, COBOL, SNOBOL, FORGO, Harris' multi-pass FORTRAN 77, a multi-user APL language, the TOTAL data base management system, the T-ask information retrieval system, an interactive BASIC language, and five remote job entry and two remote batch terminal packages. VULCAN also works in conjunction with the paging hardware to monitor and direct memory allocation. VULCAN's virtual memory operation is totally transparent to the user. VULCAN's prerequisites include a disk subsystem with at least a 40-megabyte capacity and a magnetic tape subsystem.

six or twelve bits in length, and instruction formats vary widely. There are eleven distinct field arrangements within the 24-bit instruction word. However, within these eleven arrangements there are multiple field uses that greatly expand the number of format descriptions. The following three representative format descriptions by no means exhaust the possibilities.

Memory reference instructions are of two basic types. The standard memory reference uses the six high-order bits for the operation code, the next bit for an indirect addressing indicator, the next two bits for indexing, and fifteen bits for the address field. The second format is the long branch: the six high-order bits are the operation code, the next bit is an indirect addressing indicator, the next is an operation code extension, and the last sixteen bits form an address field. Another significant format is for register-to-register instructions: the operation code occupies the twelve high-order bits with the last twelve bits divided equally to designate two registers. Memory beyond three megabytes is accessible through the virtual memory addressing system.

INTERNAL CODE: ASCII.

### MAIN STORAGE

TYPE: NMOS with single-bit error correction.

CYCLE TIME: 400 nanoseconds (48 bits). If a desired instruction is already in cache memory, it can be accessed in 70 nanoseconds (48 bits). Cache memory has two 3K-byte partitions, one for instructions and one for operands, each of which is searched in parallel. Harris claims that the cache "hit" ratio is 90% or better.

CAPACITY: 384K bytes to 3 million bytes in 192K-byte increments. A Memory Expansion Unit is required if memory is to be increased beyond 1,344K bytes.

CHECKING: Single-bit error correction is employed using a 5-bit Hamming code for each 24-bit data word. All single-bit main memory errors are detected and corrected. The five parity bits are generated for each word as the word is written into memory and recomputed when the word is read.

STORAGE PROTECTION: The H800's virtual memory system provides hardware and software memory protection. Every 3,072-byte program page in memory is protected against access or inadvertent destruction by another concurrently executing program. In addition, pages containing instructions and constants (as opposed to variable data) are hardware write-protected even within the same program.

RESERVED STORAGE: The H800 reserves from sixteen to seventy-two memory addresses for external interrupt handling. Sixteen external interrupt levels are standard, and up to fifty-six additional external interrupt levels are optional. Eight internal interrupts, called executive traps, are reserved for internal CPU functions. Each executive trap level is associated with specific functions.

A 6K-byte cache memory and an optional shared memory system are also available with the H800. The shared memory is configured using the basic 192K-byte MOS memory modules. A single CPU can interface with up to four shared memories. Maximum memory available to a single CPU is 3,072K bytes, which includes a combination of main memory and shared memory.

### CENTRAL PROCESSOR

GENERAL: The H800 central processing units feature 48-bit architecture with pipeline and parallel processing. Three separate processors—the Instruction Processor, the

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## PERIPHERALS/TERMINALS

| DEVICE | DESCRIPTION AND SPEED | MANUFACTURER |
|---|---|---|
| MAGNETIC TAPE | | |
| 6630, 6631 | Seven-track, 556/800 bpi, 45 ips, tension arm | Wangco |
| 6700 | Nine-track, 1600/6250, 75 ips | Pertec |
| 6840-1, -2 | Nine-track, 800 bpi, 45 ips, tension arm | Pertec |
| 6850-1, -2 | Nine-track, 800/1600 bpi, 45 ips, tension arm | Pertec |
| 6890-1, -2 | Nine-track, 800/1600 bpi, 75 ips, vacuum column | Pertec |
| 6720, -21 | Nine-track, 1600/6250 bpi, 75 ips | STC |
| LINE PRINTERS | | |
| 4415 | 180-cps serial printer | Centronics |
| 4110 | 300-lpm, drum type, 64-char. set, 136 positions | Dataproducts |
| 4115 | 240-lpm, drum type, 96-char. set, 136 positions | Dataproducts |
| 4120 | 600-lpm, drum type, 64-char. set, 136 positions | Dataproducts |
| 4125 | 436-lpm, drum type, 96-char. set, 136 positions | Dataproducts |
| 4130 | 900-lpm, drum type, 64-char. set, 136 positions | Dataproducts |
| 4135 | 660-lpm, drum type, 96-char. set, 136 positions | Dataproducts |
| 4260-1, -2 | 1200-lpm, chain, 64-char. set, 132 or 136 positions | Data Printer |
| 4270-1, -2 | 900-lpm, chain, 96-char. set, 132 or 136 positions | Data Printer |
| CARD EQUIPMENT | | |
| 3010 | 300-cpm reader, 550-card I/O stackers, 80-column | Documation MXXXL |
| 3020 | 600-cpm reader, 1000-card I/O stackers, 80-column | Documation MXXXL |
| 3030 | 1000-cpm reader, 1000-card I/O stackers, 80-column | Documation MXXXL |
| 3110 | 300-cpm reader, 500-card I/O stackers, 80-column | Documation MXXXL |
| 3120 | 600-cpm reader, 1000-card I/O stackers, 80-column | Documation MXXXL |
| 3130 | 1000-cpm reader, 1000-card I/O stackers, 80-column | Documation MXXXL |
| PAPER TAPE EQUIPMENT | | |
| 2030/2035 | 300-cps reader/75-cps punch (2035 is for fanfold tape) | Remex |
| 2040 | 300-cps reader/spooler | Remex |
| 2050 | 2040 with 7.25-inch reel | Remex |
| 2060 | 75-cps punch/spooler | Remex |
| 2095 | Paper tape spooler | Remex |
| TERMINALS | | |
| 2110, 2130 | Modified ASR-33; 10 cps | Teletype |
| 2140 | Modified KSR-33; 10 cps | Teletype |
| 2150 | Modified ASR-35; 10 cps | Teletype |
| 2160 | Modified KSR-35; 10 cps | Teletype |
| 2310, 8610, 8630 | Interactive CRT; 24 lines x 80 char., 9600 bps; 8610 is a remote terminal; 8630 has RS-232 interface | Tec |
| 2350 | Teleprinter replacement CRT; 24 lines x 80 chars., with keyboard | Infoton |
| 8680 | Interactive CRT; 24 lines x 80 char., with keyboard | Beehive |

Optional hardware items available with a basic H800 include 100 kHz real-time clock, additional Programmed Input/Output Channels, External Block Channels, Integral Block Channels, additional Buffered Block Channels, additional Direct Memory Access Communications Processor Channels, 56 additional priority interrupt levels, Memory Expansion Unit (required for memory above 1,344K bytes), and Shared Memory Unit.

Harris services its equipment on a maintenance contract basis, with field service personnel operating out of ten sales offices in the United States. Offices are located in major metropolitan areas near large installation sites.

**Execution Processor, and the Maintenance Aid Processor—operate independently, asynchronously, and in parallel with each other. Included in the CPU are several general- and special-purpose registers, and arithmetic section, timing and control logic, memory interface logic, and I/O channel interface circuits. Special paging registers and control logic are provided for virtual memory operation.**

**Instruction execution sequences are established and directed by the timing and control logic associated with the Instruction Unit. This logic includes a crystal-controlled clock generator that provides precise timing for all instruction functions. Instruction words of twenty-four or forty-eight bits are prefetched and retained in an instruction buffer. As many as four instructions may be prefetched and stored in the buffer. The control logic decodes these instruction words and**

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Services offered by Harris include consultation for design and testing of applications software, interface software, and system software as well as in-house or field training on the processor, peripherals, and software for user system programmers and maintenance personnel.

## USER REACTION

Because of the small number of H800's which Harris has shipped and installed and the short time that any of these systems has been in use, Datapro feels that a user reaction survey would not be meaningful at this time.□

provides the internal commands necessary for execution. In the User Mode of operation, the paging control logic operates in conjunction with the basic CPU timing to implement address translation and demand paging techniques.

The Maintenance Aid Processor (MAP) and the terminal connected to the MAP replace the conventional computer control panel. The MAP and terminal provide an intelligent interface between the operator and the computer. Normal operator functions provided by the MAP terminal include facilities for starting and halting operations manually, entering data into memory and various registers, and selecting memory and registers for display. System status and other functions can be displayed via the MAP and its terminal. Master clear and initial program load (bootstrap) functions are also provided. In addition to the normal operator functions, the MAP provides special maintenance functions. Special support hardware operates in conjunction with the MAP to provide selective monitoring and control of the computer logic. A maintenance bus provides access to all essential internal computer hardware not otherwise accessible. Maintenance functions include the capability to perform a limited master clear, to step through instructions and microinstructions, to control the CPU clock, and to read/write nonprogrammable CPU registers. I/O channel read and write control, program and memory address compare breakpoint control, and power supply voltage monitoring are additional functions performed by the MAP.

CPU-to-memory interface circuits consist of address- and data-handling buses and registers and parity generation/checking or error checking and correction logic. Memory interface circuits include a 48-bit data register that retains both the read and write data, a 20-bit address register to define the location to be accessed in up to 3,072K bytes of physical memory, data multiplexing logic to control read and write data handling, and address multiplexing and control logic for selecting the proper memory segment and a location within that segment. Data to be written in memory is applied via the 48-bit system data bus. Address inputs are applied to the memory interface via the system address bus. The address source may be the CPU, one of the block transfer channels, communications processor, or, in the User Mode of operation, the paging logic addressing circuits.

The arithmetic section consists primarily of a 48-bit arithmetic logic unit (ALU) and several buses to permit data manipulation between the various registers and the ALU. Arithmetic functions performed include addition, subtraction, multiplication, division, and square root computation. The Execution Unit provides floating-point arithmetic capability. A special repertoire of instructions is provided for performing floating-point computations. The E Unit contains the X, XW, and Y registers for manipulating 48-bit quantities and for reporting arithmetic status (condition) after the operation has been completed. Data and condition information may be displayed on the MAP terminal. An executive trap is provided with the E Unit for the detection of overflow-underflow conditions.

Communications between the CPU and the I/O channels are conducted via the channel interface logic in the CPU. This logic makes use of the system buses and one of the general-purpose registers in order to implement data and address flow between the CPU and the I/O channels. Although an I/O channel conducts channel-to-unit communications independently and asynchronously, input/output operations such as channel and unit selection and activation, function commands, and status testing are initiated under program control.

CONTROL STORAGE: None.

REGISTERS: Five general-purpose registers are included in the basic CPU and are used in logical, arithmetic, and manipulative operations such as register-to-memory, memory-to-register, and register-to-register instructions. Three of the general-purpose registers can be used as index registers in memory addressing functions, and one register serves as the I/O communication register during input/output operations. A 48-bit register is formed by combining two general-purpose registers, and a byte register is created by using the eight least-significant bits of one general-purpose register. With the Interval Timer included in the CPU, the Timer (T) Register becomes a sixth general-purpose register in the Monitor Mode of operation. In the User Mode, the T-Register can be read but cannot be loaded. Among the special-purpose registers are those associated with integral CPU functions such as addressing, instruction decoding, and temporary storage during data manipulation. Additional special-purpose registers are those supplied with the bit (Boolean) processor, with the Interval Time (T-Register) for timing applications, and with the Address Trap.

ADDRESSING MODES: Memory can be accessed at the 48-bit, the 24-bit, the 8-bit (byte), and the bit levels by the standard instruction set. Memory is partitioned into thirty-two 96K-byte sections, Map 0 through Map 31. If the system is in the Compatibility Mode, up to 96K bytes per section can be addressed directly and up to 768K bytes can be accessed by indirect and indexed addresses. Executable code is restricted to 192K bytes at any given time. In the Address Extension Mode, up to three megabytes of memory can be accessed directly and executable code can be located anywhere in memory and is unlimited in size.

When virtual memory is enabled, two addressing modes are employed: User and Monitor. Addresses generated in the User Mode (logical addresses) are translated to the physical address by selecting the appropriate 3K-byte physical "page" and the offset within that page. The division of main memory into physical pages allows a program to be located in noncontiguous areas of memory and to be transferred in page increments between memory and an external mass storage device under system control. When the virtual memory hardware detects a reference to a page not currently resident in main memory, a page fault occurs. This supports a demand-page technique which allows portions of a program to be absent from memory while the program is running. The occurrence of a page fault initiates a system process which transfers the referenced page to physical memory. The paging logic is disabled in the Monitor Mode; thus addresses generated in the Monitor Mode are used directly as physical main memory addresses.

INSTRUCTION REPERTOIRE: In addition to the same standard set of instructions used by Harris' H100 and H500 systems, the H800 also has a decimal feature which includes pack, unpack, decimal add, and decimal subtract instructions. The scientific instruction set executes floating-point operations on 48-bit operands with a 39-bit mantissa and an 8-bit exponent. For greater precision, extended floating-point operations use 70-bit mantissas and 24-bit exponents.

The standard instruction set is grouped into instruction types:

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| Instruction Type | Number of Instructions |
|---|---|
| Arithmetic | 42 |
| Branch | 14 |
| Compare | 11 |
| Input/Output | 7 |
| Logical | 9 |
| Priority Interrupt | 30 |
| Shift | 12 |
| Transfers | 35 |
| Miscellaneous | 11 |
| Bit processing | 17 |
| Byte processing | 23 |
| Scientific Arithmetic Unit | 47 |
| Virtual Memory | 13 |

INSTRUCTION TIMINGS: The following are minimum timings (in microseconds) for full-word fixed-point operands in register-to-register operations:

| | |
|---|---|
| Add/Subtract | 0.390/0.390 |
| Multiply/Divide | 1.700/3.510 |
| Compare | 0.390 |

INTERRUPTS: Four priority groups (0, 1, 2, and 3) are available. Group 0 is reserved for internal CPU functions and consists of eight executive trap interrupt levels. All executive tray levels are associated with specific functions.

Groups 1, 2, and 3 are reserved for external interrupts. Each group may have up to twenty-four levels. A basic system has sixteen external interrupt levels, and an additional fifty-six external levels are available. External interrupts may be individually armed, disarmed, enabled, inhibited, or triggered under program control.

PHYSICAL SPECIFICATIONS: The H800 is housed in two equipment cabinets. Overall dimensions are 71" high, 48.75" wide, and 30.75" deep. It can operate within a non-condensing relative humidity range of from 20% to 80% and within a temperature range of 50° F. to 113° F. Power requirements are 120/208, 120/240 VAC, single-phase, 4-wire at either 60 or 50 Hz ±2 Hz. Maximum current drawn is 46 amperes, and the heat dissipation is 17,000 BTU per hour. The weight of the system is approximately 1,000 pounds. Cooling is by forced air provided by internal fans on each chassis.

## INPUT/OUTPUT CONTROL

I/O CHANNELS: Programmed and direct memory access (DMA) data transfers are supported. All such operations are initiated under program control and are conducted asynchronously by an I/O or communications processor channel. All channels in the system can be active simultaneously, and each channel can communicate with up to sixteen controllers. However, only one device can transfer data at one time. The H800 has several types of input/output channels which interface the central bus system to the device controllers. Each channel is designed for a particular input/output data transfer application. The system supports up to thirty-one logical I/O channels, and multiple channels of a given type may be used as the application requires.

The Programmed Input/Output Channel (PIOC) is capable of implementing a single-word, eight-bit, parallel data transfer between the CPU and slow-speed devices. The PIOC has provisions for installing up to four unit interface controllers on the I/O circuit board. The PIOC can also drive up to twelve additional remote device controllers. This board also contains a Programmable Interrupt Generator which can be used in multiprocessor installations. One or two real-time clocks may be installed on the board. Units which may be interfaced to the PIOC include teletypes (with or without cassette), line printers, CRT terminals, RS-232 asynchronous controllers, and communications multiplexers. Input/output to these devices proceeds under program control through a CPU register.

The Buffered Block Channel (BBC) performs and controls automatic data transfers between main memory and any of up to sixteen external high-speed peripheral controllers. Data is transferred between main memory and the BBC in a 48-bit parallel word format and between the BBC and peripheral controllers in a 24-bit parallel word format. Data transfers between the BBC and a peripheral controller can be performed simultaneously with transfers between the BBC and memory. Data and command chaining is supported as well as programmed input/output transfers. After a block of data has been transferred, the data chaining capability permits a subsequent data block to be transferred automatically without program intervention. Command chaining enables the channel to access memory automatically for a command word upon completion of the current block transfer. A new block of data is then transferred under new command restraints.

The BBC can also perform a reverse read operation, eliminating the need for rewinding magnetic tapes. The 24-bit input data words from the peripheral controller are assembled in reverse order by the BBC and are then transferred to memory in 48-bit parallel format.

A large internal buffer, forty-eight bits wide by sixteen words deep, in the BBC allows peripheral transfer rates to be maintained even during periods when the CPU inhibits memory access by the channel. The internal buffer and a dual priority scheme cause most BBC memory requests to occur in groups. This enhances CPU performance by increasing the effective bandwidth.

A special function enables the BBC to generate odd parity on command and data transfers to designated controllers and to check for odd parity on data transfers from these units. Parity errors occurring during block or programmed word transfers are reported with a status word.

Once initiated, all BBC DMA operations proceed automatically.

The Direct Memory Access Communications Processor (DMACP) is a multiport communications processor channel dedicated to serial data communications. The DMACP-16 provides direct access to memory for up to sixteen devices, which can be asynchronous or synchronous.

Programmed data transfers or block data transfers of twenty-four bits are performed between the DMACP and CPU. Programmed word transfers are used for status check, initialization, and control of the DMACP. Block mode operations are used for data transfers between main memory and communication devices attached to the ports. These transfers are under the control of the microprocessor installed on the DMACP board and require no intervention by the CPU. Transfers between the DMACP and main memory are in the form of 24-bit words, while transfers between the DMACP and communication devices are in the form of 8-bit bytes. Standard interfaces available with the DMACP-16 are RS-232C, 20 ma current loop, and Harris Differential. Asynchronous devices supported are Harris Standard CRT terminals, interactive CRTs, teletypewriters, Bell asynchronous modems, and Bell compatible modems up to 19.2K bits per second. Synchronous devices supported are Bell synchronous RS-232C modems and Bell compatible synchronous modems with transfer rates up to 56K bits per second.

The External Block Channel (XBC) provides for direct memory access operations between memory and up to eight user-designed and developed external controllers and

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devices. Any one of the eight controllers connected to the XBC may initiate memory transfer sequences. Since controllers may be self-starting, no CPU commands are required to perform DMA transfers. If required, however, controllers can be activated by generating input/output commands to the XBC. Parameters required for block transfers such as block length and memory transfer address may be furnished by either the controller or the CPU. Once a controller has been activated for memory transfer operations, the controller initiates word transfer sequences and controls the operational parameters. Data transfers between main memory and controllers are in a 24-bit parallel word format.

The Integral Block Channel (IBC) provides automatic data transfer between main memory and one self-contained controller. The controller is dedicated to a block mode card reader. The IBC is initialized by the CPU to perform DMA transfers under self-control. Data chaining provides for the transfer of subsequent blocks of data without program intervention. Data transfers between memory and the controller are in a 24-bit parallel word format.

Available as an option, the Input/Output Expansion Unit increases the input/output capacity of a system. The maximum number of I/O channels supported by a system is thirty-one. I/O expansion is implemented by adding a cabinet assembly to the basic system. The cabinet contains a power distribution unit, power supplies, and a 22-slot chassis assembly. A pair of PC boards plus cables is also provided to connect the expansion unit to the basic system. The I/O Expansion Unit can be used to expand the I/O capabilities of computer systems located in the field.

The Interprocessor Communication Facility (ICF) provides direct communications capability between interconnected computers in a dual-computer installation. Memory-to-memory transfers are made under the control of a DMA channel installed in each CPU. Either channel in the link may control the transfer. Such a link is particularly useful in real-time control applications involving more than one computer. Two H800 CPUs may be linked, or an H800 CPU may be connected to a CPU in either an H100 or an H500 system. The ICF is implemented with two dedicated Buffered Block Channels, link cables, and four Priority Interrupt Generators. The linked systems may be up to 120 feet apart. Software interrupts generated by the Priority Interrupt Generators are normally used to initialize link operations. This option is not supported by the VULCAN operating system except for the priority interrupt structure. Establishment of control must be user-implemented and requires user code.

SIMULTANEOUS OPERATIONS: All channels in the system can be active simultaneously. In addition, Harris' pipelining technique provides simultaneous instruction execution, address processing, and instruction and operand fetches. Both operands and instructions are prefetched, and several instructions are processed simultaneously. When conditional branch instructions are executed, instructions for both decision paths are prefetched and preprocessed so that minimal time is lost after a decision has been made. Interfaces such as multiple batch operations, interactive terminals, remote job entry, and direct connection to instrumentation or control apparatus can be engaged simultaneously with precedence and priority being assigned by the user.

## CONFIGURATION RULES

Memory for the H800 can be expanded from 384K bytes to 3,072K bytes (three megabytes) in 192K-byte increments. A Memory Expansion Unit is required if memory is to go above 1,344K. The 12-megabyte virtual memory and the 6K-byte cache memory are standard equipment. A system can support up to thirty-one logical I/O channels, and each channel can communicate with up to sixteen controllers. The number of peripherals is limited only by the number of I/O channels and the maximum number of peripheral controllers which each type of channel can control. Multiple channels of a given type may be used. A disk subsystem with a capacity of at least forty megabytes and a magnetic tape subsystem are prerequisites for the VULCAN operating system.

WORKSTATIONS: The system will support up to 128 interactive workstations. Two local data terminals are provided with each system. A similar data terminal is used for remote diagnostic operations. All terminals are console type, consisting of a CRT and a keyboard. One of the local terminals is dedicated to operator communications, and the other is used as a Maintenance Aid Processor terminal.

DISK STORAGE: The cartridge disk system will support four drives per controller. The 40-, 80-, 300-, and 675-megabyte disks are controlled by the Universal Disk Controller (UDC), which can handle up to eight drives in any mix of the four sizes. Typically, only one UDC would be attached to a Buffered Block Channel (although multiple BBCs can be attached to an H800). For practical purposes, Harris considers ten UDCs to be the maximum.

MAGNETIC TAPE UNITS: Each magnetic tape drive controller can support a maximum of four tape drives. Tape drives attached to a given controller must be the same type. There is no practical limit to the number of tape controllers which can be supported by an H800.

PRINTERS: Printers are controlled by the Programmed Input/Output Channel. Multiple PIOCs can be attached to an H800, and each PIOC will accept four plug-in device controllers. A practical maximum of about four printers can be supported by an H800.

## MASS STORAGE

5200 CARTRIDGE DISK SYSTEM: Provides storage for 10.8 megabytes on double platters. The controller can handle up to four disk units. Data transfer rate is 300,000 bytes per second. Average head positioning time is 35 milliseconds, and average rotational delay is 12.5 milliseconds. The 5200 is manufactured by Control Data.

5610, -30, -50 DISK STORAGE MODULES: Provide 40, 80, or 300 megabytes of storage on a single drive. The drives are under the control of the Universal Disk Controller, which handles eight drives in any mix. Transfer rates are up to 1.2 megabytes per second. Average head positioning time is 30 milliseconds, and average rotational delay is 8.3 milliseconds. The units are manufactured by Control Data.

5560 FIXED STORAGE MODULE: Provides 675 megabytes of storage on a single drive. The drive is controlled by the Universal Disk Controller and can be mixed with 5610, -30, and -50 drives on the same controller. Transfer rate is 1.2 megabytes per second, and average rotational delay is 8.3 milliseconds. The average head positioning time is not yet available. The 5660 is manufactured by Control Data Corporation.

## INPUT/OUTPUT UNITS

See Peripherals/Terminals table.

## COMMUNICATIONS CONTROL

The 8100 Series Asynchronous/Synchronous Controllers operate at up to 9600 bps, and most operating parameters are set by program.

# Harris H800

The 8310 Communications Multiplexer provides a common logic chassis for up to eight channel boards. Each board can handle a synchronous line interface or a dual asynchronous line interface of the 83XX type.

The 8450 Direct Memory Access Communications Processor (DMACP) is dedicated to serial data communications with up to sixteen asynchronous and synchronous devices. Available interfaces include RS-232C, 20 ma current loop, and Harris differential. Single 24-bit control words or data blocks are passed between the DMACP and the CPU. A microprocessor included in the DMACP board controls the transfers independent of the CPU.

COMMUNICATIONS SOFTWARE: A Remote Job Entry subsystem supported by VULCAN provides the capability for communications with certain host computers concurrently with other processing. All standard terminal features are supported for communication with the following systems: as a Univac 1004 with the Univac 1100 Series computers; as a Control Data 200 User Terminal with the CDC 6000/7000 Series; as an IBM 2780/3780 with the IBM 360/370 series; and as an IBM HASP II workstation with the IBM 360/370 series. Any VULCAN interactive terminal, either CRT or teletypewriter, may serve the RJE subsystem. Message transmission and reception use the host system's protocol. I/O spooling is an integral part of the system.

## SOFTWARE

The basic software supplied as standard with each system is the operating system, VULCAN.

Also available are APL interpreter, a FORTRAN IV compiler, COBOL compiler, Interactive BASIC compiler, SNOBOL 4, RPG II, Harris MACRO Assembler, Diagnostic FORTRAN compiler (FORGO), FORTRAN 77, Sort/Merge, Indexed Sequential File Handler, post mortem dump, Utility Package, Cross Reference, Symbolic Debugger, Link Loader, and a complete set of diagnostics for the mainframe, memory, and peripherals.

OPERATING SYSTEM: VULCAN occupies 120K to 300K bytes of memory. System size depends on several factors, including the number of concurrently active user programs, system table sizes, and the number of nonresident handlers loaded at a given time. According to Harris, the system will generally occupy less than 288K bytes of memory. VULCAN requires a disk subsystem with at least 40-megabyte capacity and a magnetic tape subsystem.

VULCAN's features include disk file security on a multi-level basis, re-entrant processors and libraries which minimize the additional memory required by multiple users, re-entrant code generation (which implies separation of program space into code and data sections), spooling of input and output of either the data or jobstream type for local or remote terminals, interprogram communications either by message or parameter, integral systems accounting, and a Remote Job Entry (RJE) subsystem for emulation of several different terminal types.

The Remote Job Entry subsystem provides the capability for communication with certain host computers concurrently with other processing. All standard terminal features are supported for communication with the following systems: as a Univac 1004 with the Univac 1100 Series computers; as a CDC 200 User Terminal with the CDC 6000/7000 Series; as an IBM 2780/3780 with the IBM 360/370 Series; and as an IBM HASP II workstation with the IBM 360/370 Series.

Any interactive terminal, either CRT or teletypewriter, may serve the RJE subsystem. Message transmission and reception use the host system's protocol.

LANGUAGES: Eight languages are currently being offered for use on the H800.

*APL* is a conversational language that is particularly well suited for operating on numeric and character array-structured data. Using APL, variables can be shared and also examined and changed, and program action can be readily traced. Features of APL include dynamically variable user's workspace size, chaining of APL programs to previously prepared run-time programs, multiple statement lines, standard H800 file-naming formats, and extended single operators which allow the user to fully evaluate character strings and write user-defined functions to perform output formatting and function editing. The language is built around a set of unique symbols, each of which represents a desired operation. The nature of the language is such that complex expressions are easily constructed by the programmer. According to Harris, APL produces concise code.

*FORTRAN IV* is based on but exceeds ANSI X3.9-1966. Harris-supported extensions include random-access I/O; indexed sequential file operations; memory-to-memory data conversion through encode/decode statements; double-buffered and overlapped I/O capabilities through asynchronous I/O statements, which include processing of variable-length and arbitrary-format records in both input and output; free-format I/O, allowing for basic I/O without using FORMAT statements; control functions for end-of-file and I/O or FORMAT errors in all I/O statements; a DATA statement extension for arrays; octal and literal constants; recursive subprograms; in-line assembly code for statements and variables or constants; implied DO loops in DATA statements; program-controlled loading of program overlay segments which have been separately compiled; pseudo-random number generations; services in real-time digital and analog I/O functions; and bit manipulation functions. A diagnostic FORTRAN compiler (FORGO) serves as a companion to Harris extended FORTRAN IV.

*FORTRAN 77* is based on the full language definition of ANSI FORTRAN X3.9-1978. This standard defines a number of added capabilities not included in the 1966 standard. These include structured programming support with IF-THEN-ELSE statements; character data types; array enhancements including up to seven dimensional arrays, adjustable dimensions, negative subscripts, and subscript range specification; multiple RETURN definition; IMPLICIT statement; ENTRY statement; INTRINSIC statement to permit use of the symbolic name of an intrinsic function; enhanced I/O capabilities including direct access and list-directed I/O, OPEN, CLOSE, and INQUIRE statements, internal files, I/O statement keyword parameters, and FORMAT statement extensions; PARAMETER statement; and new format editing descriptors. In addition, Harris FORTRAN 77 provides capabilities not included in the 1977 standard such as additional structured programming features including FOR, LOOP, WHILE, and DO-UNTIL blocks; indentation of structured programs listings; in-line assembly code; support for large software systems through use of MONITOR COMMON and DATAPOOL; additional data types; symbol names of up to 63 characters; support for lower-case characters in symbol names; continuation lines not limited to 19; asynchronous I/O (BUFFER IN/BUFFER OUT); additional logical operators including exclusive OR, logical shift, and logical rotate; support for Hollerith as well as character data; formatted direct access I/O and indexed sequential I/O; in-line compiler control statements; extensive subroutine libraries; and conditional compilation of DEBUG statement. Harris FORTRAN 77 provides upward compatibility with Harris FORTRAN IV. Compile-time options are provided to accept source files created using IBM 026 character code and to cause character constants to be processed as Hollerith constants. Harris FORTRAN 77 has been validated by the Federal Compiler Testing Center.

# Harris H800

*Interactive BASIC* contains 54 statements and language enhancements for string manipulation, extended Boolean operators and IF statements, logical I/O and picture format facilities, and editing for input. Built-in real-time capabilities allow for use of external interrupts, initiation of programs, parameter passing from other programs regardless of language, and operator communications. A compiler mode that produces linkable code is included in Harris' BASIC, as well as a conventional interpreter mode.

*RPG II* as implemented by Harris allows for interchange of files between itself and FORTRAN IV or assembly-language programs, as well as creation of these files by programs coded in any of the three languages. Harris RPG II language extensions include array and table equivalencing, main program execution initiation, array element manipulation, source library use, and one- to six-byte binary numeric fields. Sequential, indexed sequential, and direct access files are also supported.

The *MACRO Assembler* is a two-pass system that supports over 700 mnemonic operation codes and a range of pseudo-operations which can, among other things, create eleven different constant types. The assembler features nested and recursive macro capabilities.

*COBOL* conforms to ANSI X3.23-1974. As with FORTRAN, the COBOL compiler generates re-entrant code. It features 44 verbs and modifications, 49 levels of qualification, arbitrary deeply nested conditional statements, 32-digit accuracy in intermediate calculations, facilities for using CORRESPONDING, and standard debugging tools. Harris' COBOL has been validated by the Federal Compiler Testing Center.

*TOTAL* is a host-language data base management system implemented much along the same lines of the CODASYL Data Base Task Group Report, except that the user can use other host languages as well as COBOL. TOTAL provides an effective means for organizing and managing diverse data to make it both efficient and convenient for application programmers to maintain and retrieve the data for processing. It was developed by Cincom Systems, Inc., and is widely used with large computer systems. It has been well received and highly rated by users.

TOTAL can manage virtually an unlimited number of data sets on an "integrated, non-redundant" basis and provides for association of each of these data sets with other data sets to form an integrated data base. TOTAL allows the user to relate data across many functional and/or departmental boundaries, permitting the data processing applications to mirror the system of management within an organization.

TOTAL permits the establishment of two types of records: a single-entry or master record and a variable-entry record. Each group of records, of either type, forms a file (data set). Linkages can be set up that permit automatic retrieval of all variable-entry records associated with a particular single-entry record based on the linkage. A variable-entry record can be part of many linkage paths or chains.

A TOTAL data base is composed of multiple data sets or files. Linkages can exist between any master file and any variable-entry file. Multiple-file data bases can be established. A particular master file or variable-entry file can be part of more than one data base. The multiple paths of access allowed by such a structure, called a network structure, simplify the logic of application programs using the data. In the case of TOTAL, they also reduce the amount of disk storage required to hold information by eliminating duplicate fields or records.

A randomizing algorithm is used by TOTAL to calculate master record physical addresses based on the value of the control field. If duplicate addresses are calculated, a pointer is used in that record to show where the "duplicate" or synonym record is stored. Thus, the complete disk space allocated can be used. Once all space is used up, the data file must be reloaded with new parameters. Cincom provides a utility to handle such occurrences.

Access to TOTAL files is provided through the CALL statement for application programs written in COBOL, FORTRAN, or assembly language. The applications programmer cannot establish new data sets or alter existing linkages among data items; this function is accomplished separately through a generator program using a special data base definition language.

Harris' TOTAL Data Base Management System is complemented by the Harris T-ask Information Retrieval System, which is available under TOTAL on any Harris processor supporting the VULCAN operating system. T-ask allows nonprogrammers to extract information from the TOTAL data base by means of a simple, English-like, nonprocedural information retrieval language. Frequently used inquiries may also be saved (catalogued) for re-use at a later time.

UTILITIES: Other software includes an indexed sequential disk access method callable by FORTRAN IV or assembly-language programs; a sort/merge package callable by FORTRAN IV, RPG II, or assembly language; and a macro cross-assembler written in FORTRAN IV.

APPLICATIONS: Harris does not supply application packages.

## PRICING

POLICY: Harris offers its systems primarily for purchase, although third-party leasing (one-year term) is available on a negotiated basis. Some software costs are bundled in the system prices, except for items such as the remote batch terminal emulation software, which is priced at $5,000; TOTAL Central, priced at $12,800; and T-ask, priced at $10,000; and some utilities.

Special considerations apply for volume purchases of virtual memory systems. When the first purchase of an H800 system is made by an OEM or volume-purchase end-user, no OEM, CPU, peripheral, or business volume discounts apply. Any additions or upgrades to a system, however, will be eligible for appropriate CPU/peripheral discounts. CPU's purchased in H800 systems will count toward CPU and peripheral totals for other OEM purchases, and the final "dollar total" on the systems will apply to total business volume for other purchases.

SUPPORT: Maintenance is performed by service personnel working out of Harris CSD service offices in the U.S. Maintenance contracts are developed on the basis of local or remote service areas. A local service area is defined as the area within a 50-mile radius of a Harris CSD service office. All other areas are considered remote. For non-contract maintenance, prime-time hourly rates are $60 and $66 per man-hour; minimum billing for these customers is four hours for local service and eight hours for remote service. Remote service area customers, whether on contract or not, are billable at actual cost for tourist-class air travel or at $0.20 per mile for automobile usage and for meals and lodging.

Under contract, maintenance is available for 9 prime-shift hours from 7 am to 6 pm, Monday through Friday. Additional maintenance hours are available by negotiation with Harris at prime monthly rates plus an extra charge.

# Harris H800

**End users are not charged for the installation of a basic system; however, there are installation charges for subsequent add-ons. Programming and maintenance training are separately priced and are available either at the installation site or at Harris' Fort Lauderdale facility. Training courses are offered in maintenance for the processors, Scientific Arithmetic Unit, and peripherals. A software course on VULCAN is currently being offered.**

**EQUIPMENT: Harris does not offer packaged configurations based on the H800. Prices of the basic processor and peripheral equipment are shown in the following Equipment Prices.**

## EQUIPMENT PRICES*

| | | Purchase Price | Monthly Maint. |
|---|---|---|---|
| **PROCESSOR** | | | |
| H800 | Computer system: includes 384K-byte error-correcting MOS memory, 12-megabyte virtual memory, hardware floating-point processor, Maintenance Aid Processor and MAP terminal, console CRT, 16 priority interrupts, cache memory, Integral Scientific Arithmetic Unit (SAU), hardware multiply/divide/square root, VULCAN operating system and software (MACRO assembler, text editor, and support libraries), and two 19-inch cabinets<br>Note: VULCAN requires a disk subsystem with at least 40-megabyte capacity and a magnetic tape subsystem. | $165,900 | $1,095 |
| **MEMORY** | | | |
| 001A | 192K-byte error-correcting MOS memory | 7,300 | 60 |
| 001B | 384K-byte error-correcting MOS memory | 12,000 | 120 |
| 001C | 768K-byte error-correcting MOS memory | 18,000 | 240 |
| 001D | 960K-byte error-correcting MOS memory | 19,400 | 300 |
| 001E | 1,920K-byte error-correcting MOS memory | 31,300 | 600 |
| **PROCESSOR OPTIONS** | | | |
| 015B | Scientific Arithmetic Unit (SAU) | 10,395 | 55 |
| 022 | 100 kHz real-time clock | 1,750 | 10 |
| 051 | Priority interrupt expander with 32 priority interrupts | 3,675 | 40 |
| 052 | Priority interrupt expander with 24 priority interrupts | 3,150 | 30 |
| 045 | Programmed I/O Channel (PIOC) | 1,260 | 10 |
| 046 | Buffered Block Channel (BBC) | 2,700 | 20 |
| 048 | External Block Channel (XBC) | 2,100 | 15 |
| 049 | Integral Block Channel (IBC) | 2,100 | 10 |
| 072 | Expansion pack; including 22-slot I/O chassis and power supplies | 8,500 | 20 |
| 073 | Memory expansion chassis for up to 9 memory modules | 7,500 | 20 |
| 074 | Extended Memory kit; interface module for 073 | 2,000 | — |
| 075 | Shared Memory kit with one port | 2,000 | — |
| 076 | Slot Enable kit; includes 4 slots for shared memory ports and 3 slots for additional memory modules | 1,000 | — |
| 077 | Additional Slot Enable kit; includes 4 slots for additional memory modules | 1,000 | — |
| **MASS STORAGE** | | | |
| 5260-A | 10.8-megabyte double-platter cartridge disk drive and controller | 17,200 | 140 |
| 5261-A | 10.8-megabyte add-on double-platter cartridge disk drive | 11,600 | 110 |
| 5265 | Cartridge disk platter | 500 | — |
| 5610 | 40-megabyte storage module drive and Universal Disk Controller (UDC) | 23,300 | 255 |
| 5611 | 40-megabyte add-on storage module drive | 15,900 | 175 |
| 5515 | Disk pack for 40-megabyte drives | 1,000 | — |
| 5630 | 80-megabyte storage module drive and UDC | 26,900 | 300 |
| 5631 | 80-megabyte add-on storage module drive | 20,500 | 225 |
| 5535 | Disk pack for 80-megabyte drives | 1,000 | — |
| 5650 | 300-megabyte storage module drive and UDC | 43,650 | 450 |
| 5651 | 300-megabyte add-on storage module drive | 34,250 | 400 |
| 5555 | Disk pack for 300-megabyte drives | 2,500 | — |
| 5660 | 675-megabyte fixed module drive and UDC | 71,260 | 490 |
| 5661 | 675-megabyte add-on fixed module drive | 61,860 | 440 |
| **MAGNETIC TAPE** | | | |
| 6630-B | Seven-track, 556/800-bpi, 45-ips tension arm drive and controller, 4 drives maximum | 13,500 | 115 |
| 6631 | Seven-track, 556/800-bpi, 45-ips add-on drive | 11,400 | 95 |
| 6840-B | Nine-track, 800-bpi, 45-ips tension arm drive and controller, 4 drives maximum | 13,700 | 115 |
| 6841-1 | Nine-track, 800-bpi, 45-ips add-on drive, with upper mounting kit | 11,900 | 95 |
| 6841-2 | Same as 6841-1 with lower mounting kit | 11,900 | 95 |
| 6850-B | Nine-track, 800/1600-bpi, 45-ips tension arm drive and controller; 4 drives maximum | 20,100 | 155 |
| 6851-1 | Nine-track, 800/1600-bpi, 45-ips add-on drive, with upper mounting kit | 12,800 | 105 |
| 6851-2 | Same as 6851-1 with lower mounting kit | 12,800 | 105 |
| 6720 | Nine-track, 1600/6250-bpi, 75-ips, auto-load, formatter/controller; 4 drives maximum | 39,900 | 450 |
| 6721 | Nine-track, auto-load, 1600/6250-bpi, 75-ips add-on drive | 26,600 | 210 |

*These prices became effective on August 15, 1980.

# Harris H800

## EQUIPMENT PRICES*

| | | Purchase Price | Monthly Maint. |
|---|---|---|---|
| **MAGNETIC TAPE (Cont'd)** | | | |
| 6890-B | Nine-track, 800/16090/bpi, 75-ips vacuum column drive and controller; 4 drives maximum | 24,600 | 190 |
| 6891-1 | Nine-track, 800/1600-bpi, 75-ips add-on drive, with upper mounting kit | 14,900 | 140 |
| 6891-2 | Same as 6891-1 with lower mounting kit | 14,900 | 140 |
| **LINE PRINTERS** | | | |
| 4110 | 300-lpm printer, 64-character, with controller | 12,600 | 135 |
| 4115 | 240-lpm printer, 96-character, with controller | 14,200 | 145 |
| 4120 | 600-lpm printer, 64-character, with controller | 20,200 | 175 |
| 4125 | 436-lpm printer, 96-character, with controller | 22,100 | 195 |
| 4130 | 900-lpm printer, 64-character, with controller | 26,100 | 250 |
| 4135 | 660-lpm printer, 96-character, with controller | 28,800 | 270 |
| 4260-1 | 1200-lpm chain printer, 64-character, 132 cols., with controller | 39,900 | 265 |
| 4260-2 | 1200-lpm chain printer, 64-character, 136 cols., with controller | 40,800 | 265 |
| 4270-1 | 900-lpm chain printer, 96-character, 132 cols., with controller | 40,900 | 285 |
| 4270-2 | 900-lpm chain printer, 96-character, 136 cols., with controller | 41,800 | 285 |
| 4415 | 180-cps serial printer | 3,950 | 50 |
| **CARD EQUIPMENT** | | | |
| 3010 | 300-cpm reader and controller | 10,500 | 55 |
| 3020 | 600-cpm reader and controller | 12,600 | 80 |
| 3030 | 1000-cpm reader and controller | 14,175 | 100 |
| 3110 | 300-cpm reader with DMA controller | 5,410 | 55 |
| 3120 | 600-cpm reader with DMA controller | 7,330 | 70 |
| 3130 | 1000-cpm reader with DMA controller | 10,500 | 100 |
| **PAPER TAPE EQUIPMENT** | | | |
| 2030 | 300-cps reader/75-cps punch and controller | 6,565 | 60 |
| 2035 | 2030 for fanfold tape | 7,090 | 65 |
| 2040 | 300-cps reader/spooler and controller | 4,095 | 35 |
| 2050 | 2040 with 7¼-inch reel | 4,620 | 40 |
| 2060 | 75-cps punch/spooler and controller | 5,250 | 45 |
| **TELETYPEWRITERS** | | | |
| 2105 | Teletype modification kit | 370 | — |
| 2110 | ASR-33 teletypewriter with controller | 2,890 | 55 |
| 2115 | Serial teletypewriter controller | 790 | 10 |
| 2130 | Modified ASR-33 teletypewriter | 2,415 | 50 |
| 2140 | Modified KSR-33 teletypewriter | 2,205 | 40 |
| 2150 | Modified ASR-35 teletypewriter | 7,195 | 85 |
| 2160 | Modified KSR-35 teletypewriter | 4,620 | 55 |
| **CONSOLE DEVICES** | | | |
| 2310 | Interactive CRT; 24 x 80 with keyboard, interface, and controller | 5,775 | 80 |
| 2350 | Teleprinter replacement CRT; 24 x 80 with keyboard, interface, and controller | 2,575 | 25 |
| **REMOTE KEYBOARD TERMINALS** | | | |
| 8610 | Interactive CRT, Harris interface | 3,520 | 35 |
| 8630 | Interactive CRT for EIA RS-232C terminal interface | 3,360 | 35 |
| 8680A-1 | Interactive CRT with Harris differential interface | 2,200 | 20 |
| 8680A-2 | Interactive CRT with EIA RS-232C interface and current loop interface | 1,950 | 20 |
| **COMMUNICATIONS** | | | |
| 8110 | Synchronous controller for RS-232C modem; up to 9600 bps | 2,890 | 30 |
| 8121-1 | Asynchronous controller for RS-232C terminal; up to 9600 bps | 1,315 | 15 |
| 8121-2 | Same for RS-232C modem | 1,315 | 15 |
| 8121-3 | Same for 8660 CRT terminal | 1,315 | 15 |
| 8121-4 | Same for Model 4415 printer | 1,315 | 15 |
| 8130-1 | Asynchronous controller for RS-232C terminal on 8-bit IOC; up to 9600 bps; stand-alone | 2,625 | 25 |
| 8130-2 | Same for RS-232C modem | 2,625 | 25 |
| 8310 | Communications multiplexer for up to 16 asynchronous or 8 synchronous lines | 3,150 | 30 |
| 8330 | Synchronous line interface unit for RS-232C modem connection to multiplexer | 1,260 | 15 |
| 8340-1 | Dual asynchronous line interface unit for RS-232C terminal connection to multiplexer | 790 | 10 |
| 8340-2 | Same for RS-232C modem | 895 | 10 |
| 8340-3 | Same for 8660 CRT terminal | 790 | 10 |

*These prices became effective on August 15, 1980.

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## EQUIPMENT PRICES*

| | | Purchase Price | Monthly Maint. |
|---|---|---|---|
| **COMMUNICATIONS (Cont'd)** | | | |
| 8340-4 | Same for 8680A-2 CRT terminal | 790 | 10 |
| 8340-5 | Same for Model 4415 printer | 790 | 10 |
| 8350-1, -2 | Dual asynchronous line interface unit for 33 or 35 TTY | 790 | 10 |
| 8360-1, -2 | Dual asynchronous line interface unit for 8600 series CRT | 790 | 10 |
| 8370-1 | Dual asynchronous line interface unit for 8700 series terminal | 790 | 10 |
| 8370-2 | Dual asynchronous line interfce unit for 8700 series modem | 895 | 10 |
| 8430 | DMA Communications Processor for up to four twin asynchronous ports or one synchronous and two twin asynchronous ports | 3,465 | 30 |
| 8435 | ISODMACP; includes two ports for graphics terminals or plotters | 6,195 | 70 |
| 8441/5 | Twin asynchronous ports for 8430 | 685 | 10 |
| 8447 | Synchronous port; up to 19,200 bps | 1,260 | 15 |
| 8450 | DMA Communications Processor (DMACP-16 can accommodate up to 8 twin synchronous or twin asynchronous ports) | 3,500 | 30 |
| 8461 | Twin asynchronous ports for two 20 mA current loop terminals, up to 9600 bps | 540 | 10 |
| 8462 | RS-232C connection; accommodates 2 asynchronous terminals up to 19.2K bps, 2 synchronous devices with software CRC, single synchronous device with hardware CRC, or single asynchronous and single synchronous device with software CRC | 540 | 10 |
| 8463 | Twin asynchronous Harris Differential ports for two Model 8680 A-1 CRT terminals, up to 19.2K bps | 570 | 10 |

*These prices became effective on August 15, 1980.

## SOFTWARE PRICES

| | License Fees | | |
|---|---|---|---|
| | Object Code Only | Source & Object Code | Annual Maint. |
| VULCAN Operating System; includes MACRO assembler, Cross Reference, DEBUG, FORTRAN and COBOL libraries, and Symbolic Debugger | $ N/C | $ 3,000 | $1,200 |
| Harris Transaction Processor | 15,000 | N/A | 1,500 |
| 3270 Emulator | 1,000 | 2,500 | 100 |
| DMACP-16 Microcode, includes assembler and cataloger | N/C | 7,500 | N/A |
| SORT/MERGE | 300 | 1,200 | 30 |
| FORTRAN IV | N/C | 2,000 | N/A |
| FORTRAN 77 | 7,500 | N/A | 500 |
| FORGO | 500 | 1,000 | N/A |
| COBOL | 9,000 | 13,500 | 500 |
| BASIC | N/C | 2,000 | N/A |
| Extended BASIC | 5,000 | 9,500 | 420 |
| RPG II | 2,500 | 5,000 | 240 |
| SNOBOL | N/C | N/A | N/A |
| APL | 7,500 | N/A | 1,200 |
| TOTAL | 12,800 | N/A | 600 |
| T-ask | 10,000 | N/A | 500 |
| RJE 2780 Emulation, RJE 3780 Emulation, RJE HASP Workstation Emulation, RJE CDC 200UT Emulation, RJE UNIVAC 1004 Emulation, RJE HOST 2780, RJE HOST HASP Workstation (each) | N/A | 2,600 | 200 |
| FORMAT | 250 | 1,000 | 25 |
| TX Text Editor | 250 | 1,000 | 25 |
| AZ7 | 9,500 | N/A | 760 |
| AZ7/TOTAL Interface | 1,500 | N/A | 180 |

N/A = Not available
N/C = No charge