INSTRUCTION MANUAL

DATUM MODEL 5091

NRZI MAGNETIC TAPE FORMATTER

Publication No. 1800

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SECTION I

GENERAL DESCRIPTION AND SPECIFICATIONS

1.1   FUNCTIONAL DESCRIPTION

The DATUM NRZI Formatter provides for writing and reading IBM or USASCII compatible 9 track 800 BPI and/or 7 track 800/556/200 BPI magnetic tapes.

The NRZI Formatter provides a simplified computer oriented interface to minimize the task of interfacing to a digital computer. All major operations are performed automatically under control of the Formatter.

Individual selection and operation with up to four "Daisy Chained" tape transports is provided.

The transports can be a mixture of 7 and 9 track, any two tape speeds, Read/Write (single stack head) or Read-After-Write (dual stack head) configurations.

Tape transport motion control, CRCC and LRCC generation, and checking, LRCC checking, inter-record gap generation and status reporting are included. All write clocks and delay times are derived from a crystal controlled oscillator. No "one shots" or RC delays are utilized.

The NRZI Formatter is provided with a selection capability such that two formatters (NRZI or 1600 CPI phase encoded) can be "Daisy Chained" to one computer adaptor. This feature provides the capability of mixing 9 track 1600 CPI phase encoded, 9 track 800 BPI and 7 track 800/556/200 BPI tape units or providing up to eight tape units via one computer adaptor.

Card space and excess +5V power is available for computer adaptor (may be wire-wrapped) in the Formatter.

"On the Fly" operation (continuous read or write at maximum tape speed without stopping in each inter-record gap) is provided.

Writes the IBM compatible file mark (7 or 9 track formats) and recognizes file marks.

Provides for the "Edit" feature (allows a record anywhere on a previously recorded tape to be replaced with an updated record).

No calibration or adjustment potentiometers in the Formatter. All timing derived from crystal oscillator.

Compatible to entire 12.5 to 75 ips tape speed range without even changing crystals. Single field changeable jumper selects the frequencies needed for the tape speed.

Special low threshold data recovery feature provided for.

Controls and indicator lamps are provided to allow:

1. Switchable assignment of any tape unit number (0, 1, 2 or 3) to any of the four tape units.
2. Lamp indication of Formatter selection
3. Lamp indication of tape unit selection
4. Lamp indication of high or low density selection (7 track tape units only)
5. Lamp indication of odd or even parity selection (7 track tape units only)
6. Remote or Manual control over density and parity selection (7 track tape units only)
7. Power on/off.

1.2   PHYSICAL DESCRIPTION

The DATUM Model 5091 NRZI Formatter is designed to be mounted in a standard 19" EIA rack. The Formatter has 5.25" front panel height and is 21" deep (allow 2" more for I/O cable service loop).

Top and bottom covers may be easily removed for access to integrated circuits.

Input/output cable connections are made at the rear of the Formatter utilizing printed circuit edge connectors into which printed circuit cable termination cards can be plugged.

Figure 1-1 illustrates the connectors for interfacing the NRZI Formatter to an external or an internal computer adaptor and to the tape units. There is room for a third card to plug into the basic chassis to allow for the 1600 CPI Formatter which requires two card slots.

1.3   CONTROLS AND INDICATORS

The Front Panel controls and indicators are illustrated in Figure 1-2.
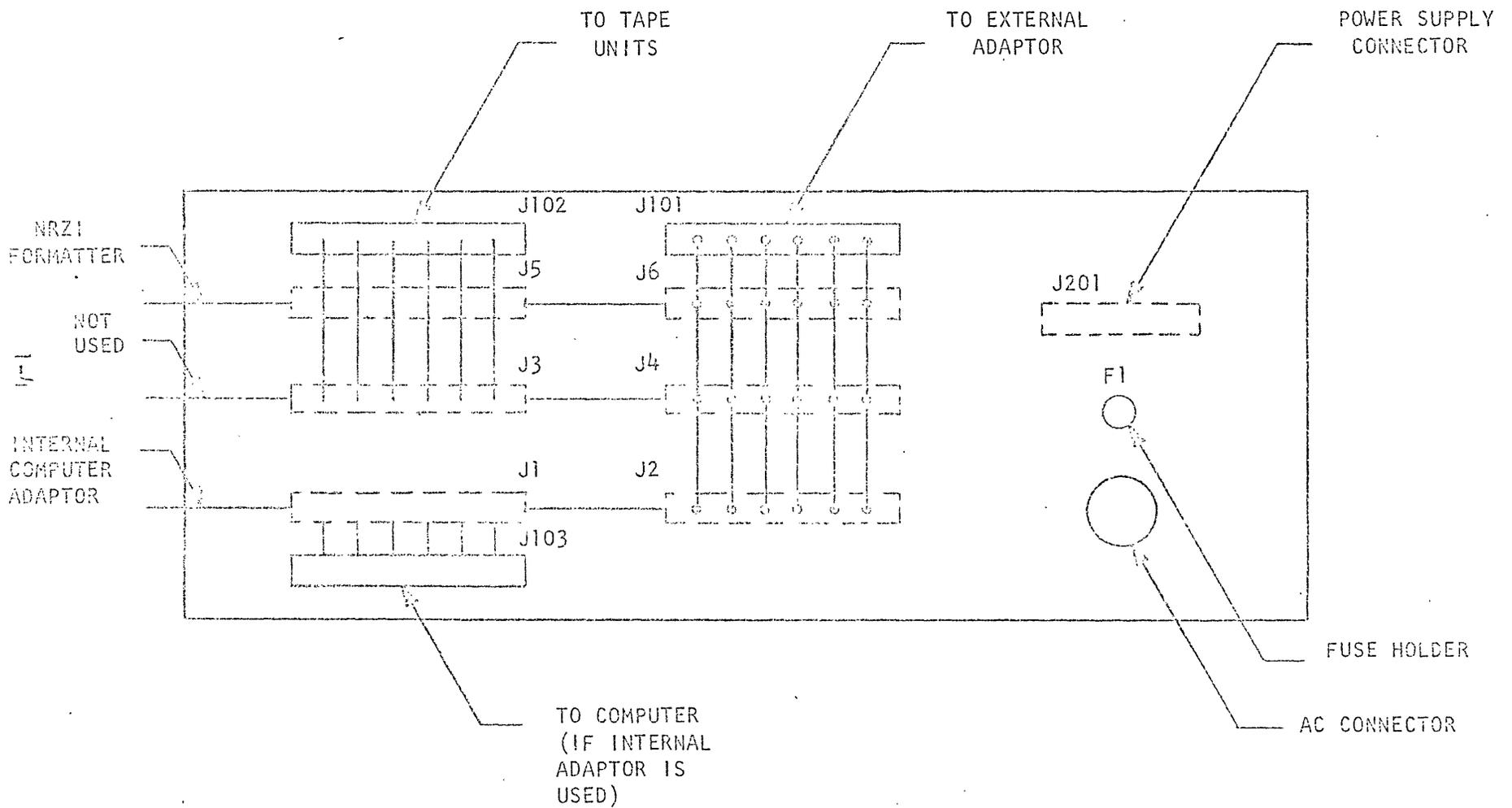
Figure 1-1. Rear View Formatter Connectors

PARITY INDICATOR
LAMPS

DENSITY INDICATOR
LAMPS

PARITY

MODE

DENSIT

1-5

REMOTE ⊂ ⊃ MANUAL

0 1 2 3   ODD   EVEN   0 1 2 3   FORMATTER   SELECTED   0 1 2 3   HI   LOW   0 1 2 3

A   B   C   D

PARITY
SELECT
SWITCH

MODE
SELECT
SWITCH

UNIT
SELECT
INDICATOR
LAMPS

UNIT
SELECT
SWITCHES

FORMATTER
SELECTED
INDICATOR
LAMP

DENSITY
SELECT
SWITCH
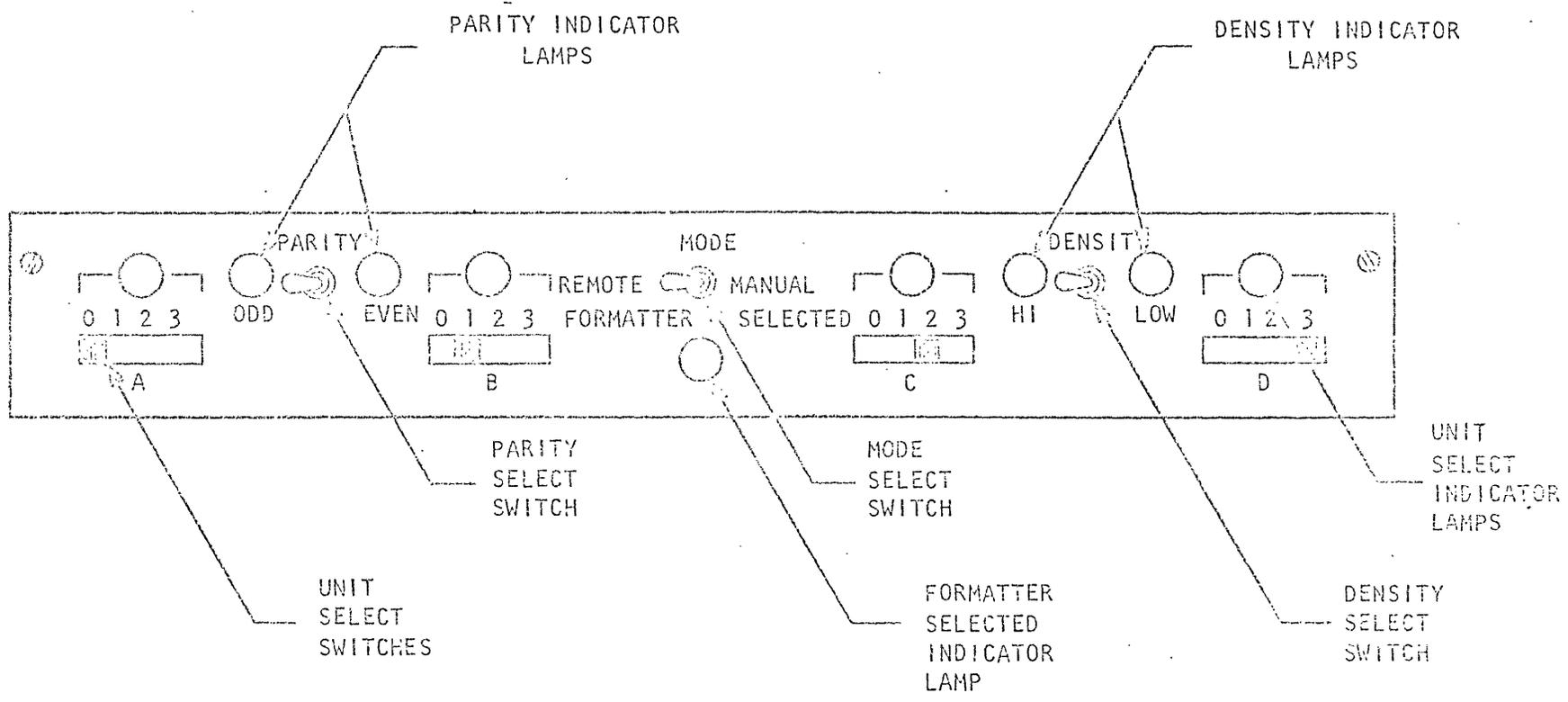
Figure 1-2.   Front Panel

POWER   The power switch controls main power to the Formatter.

FORMATTER SELECT   Lamp indicates when the computer has selected the
                            Formatter.

UNIT SELECT   The four slide switches allow any unit number (0, 1,
                            2, 3) to be assigned to any physical tape unit (tape
                            unit A, B, C, or D). Only one tape unit should be
                            assigned to a particular unit number.

UNIT SELECT
INDICATOR LAMPS   Indicate which tape unit is selected.

MODE   Allows selection of density and parity for 7 track
                            tape units to be under computer control (REMOTE) or
                            under operator switch selectable control (MANUAL).

DENSITY   When the Formatter is in MANUAL MODE, the DENSITY
                            switch controls the write/read density for 7 track tape
                            units. 7 track tape units can be any pair of densities
                            selected from 800/556/200 bits per inch. HI position
                            selects the higher density of the pair, LOW selects
                            the lower density of the pair. The indicator lamps
                            give visual indication of the selected density whether
                            under REMOTE or MANUAL control. The lamps are dark for
                            9 track tape units.

PARITY   When the Formatter is in MANUAL MODE, the PARITY switch
                            controls the selection of ODD or EVEN character parity
                            for 7 track tape units. The indicator lamps indicate
                            the selected parity whether under REMOTE or MANUAL con-
                            trol. The lamps are dark for 9 track tape units.

1.4   SPECIFICATIONS

Inter-record gap (7 track)	.75 inch nominal (.69 inch minimum)
Inter-record gap (9 track)	.6 inch nominal (.54 inch minimum)
Dimensions	Height - 5.25 inches
	Width - 19 inches
	Depth - 21 inches
Weight	25 pound maximum
Mounting	Standard 19" EIA Rack
Power	115 VAC ±10%
	230 VAC ±10%
	160 watts maximum
	48-400 Hz frequency
Circuits	All silicon
Operating Temperature	0° to 50°C
Storage Temperature	-40° to +70°C
Altitude	0 to 20,000 feet
Relative Humidity	10 to 95% (non-condensing)
Interface Voltages (DTL 900 series or TTL 7400 series compatible)	low = 0V ±.4V
	high = 3.9V ± 1.5V

The interface is designed such that an open circuit is interpreted as a "high" signal.

Figure 1-3 illustrates the configuration for which the interface has been designed.

1.5   MAGNETIC TAPE FORMATS

Figures 1-4 and 1-5 illustrate the IBM and USASCII magnetic tape formats for 7 track and 9 track tapes respectively.

CABLE DRIVER

CABLE TERMINATION +5V

2200

CABLE RECEIVER

DTL 844 or TTL 7416, 7437,
7438, 7440 or equivalent

DTL 8XX Series; TTL 74XX Series
or equivalent
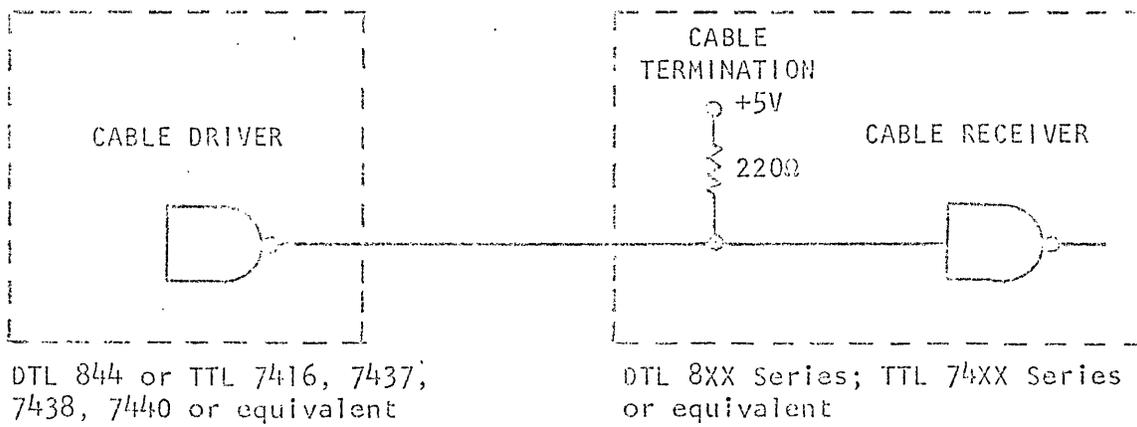
Figure 1-3.   Interface Circuits

Figure 1-4. 7-Track Format
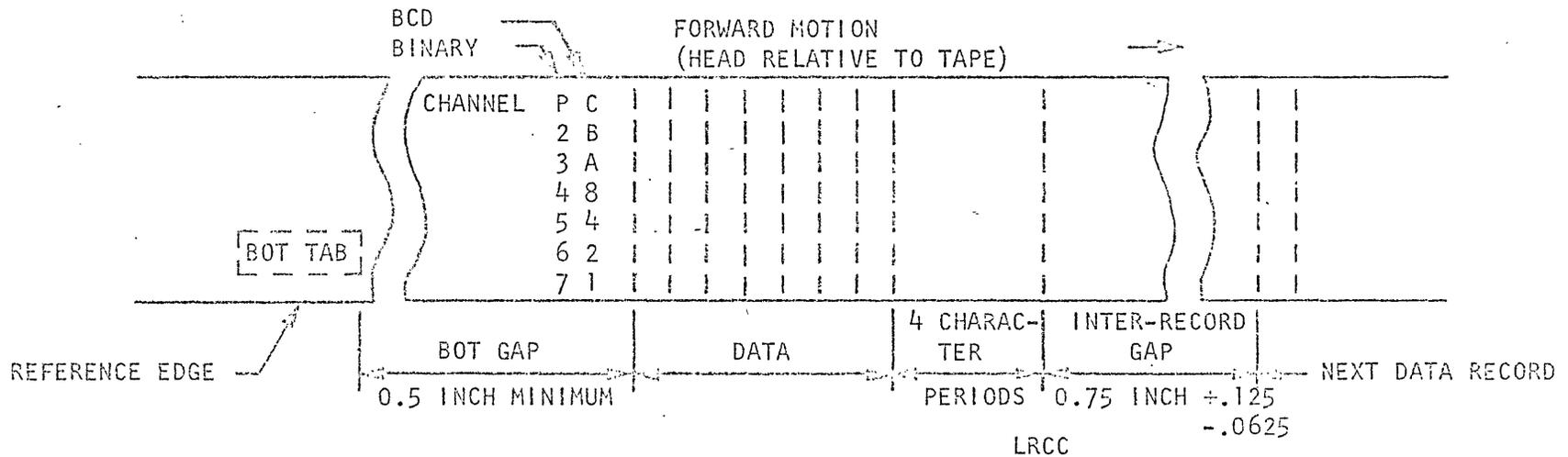
NOTES

1. TAPE SHOWN WITH OXIDE SIDE UP.

2. CHANNELS 2 THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.

3. CHANNEL P (PARITY) CONTAINS ODD DATA PARITY FOR BINARY TAPES, OR EVEN PARITY FOR BCD TAPES.

4. EACH BIT OF THE LRCC IS SUCH THAT THE TOTAL NUMBER OF "1" BITS IN THAT TRACK (INCLUDING THE LRCC) IS EVEN. IT IS POSSIBLE IN THE 7-TRACK FORMAT FOR THIS CHARACTER TO BE ALL ZEROES, IN WHICH CASE A READ DATA STROBE WILL NOT BE GENERATED.

5. A FILE MARK IS A SINGLE CHARACTER RECORD HAVING "1" BITS IN CHANNELS 4, 5, 6 AND 7 FOR BOTH THE DATA CHARACTER AND THE LRCC. THE FILE MARK IS SEPARATED BY NORMAL IRG's (.75 INCH) FROM THE PREVIOUS AND FOLLOWING RECORDS. OPTIONALLY, A 3.5 INCH GAP CAN BE ERASED PRIOR TO WRITING THE FILE MARK.

6. DATA PACKING DENSITY MAY BE 200, 556, or 800 BITS PER INCH.

←———⟶ FORWARD MOTION (HEAD RELATIVE TO TAPE)————⟶

CHANNEL 4
6
0
1
2
P
3
7
5

BOT TAB

REFERENCE EDGE

BOT GAP

0.5 INCH MINIMUM

DATA

4 CHARAC-TER

4 CHARAC-TER

PERIODS | PERIODS | INTER-RECORD GAP

0.6 INCH +.15 −.10

NEXT DATA RECORD

CRCC   LRCC   1071
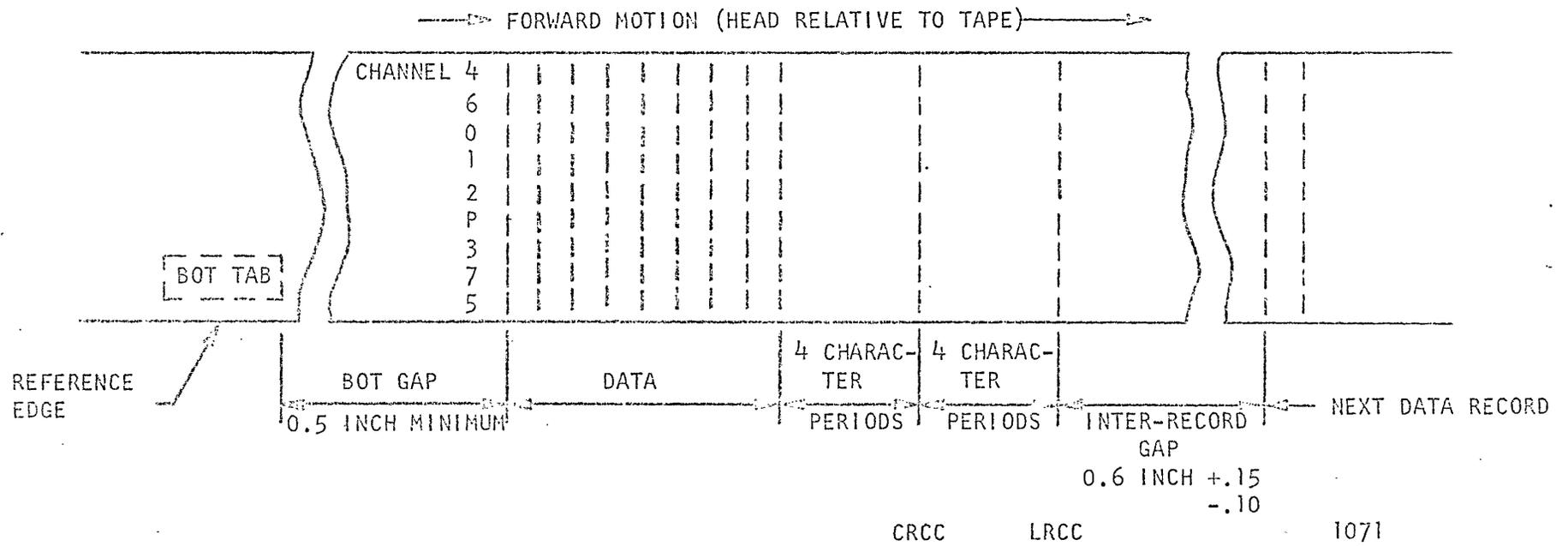
NOTES·

1. TAPE SHOWN WITH OXIDE SIDE UP.

2. CHANNELS 0 THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.

3. CHANNEL P (PARITY) ALWAYS CONTAINS ODD DATA PARITY.

4. EACH BIT OF THE LRCC IS SUCH THAT THE TOTAL NUMBER OF "1" BITS IN THAT TRACK (INCLUDING THE CRCC AND THE LRCC) IS EVEN. IN THE 9-TRACK FORMAT THE LRCC WILL NEVER BE AN ALL-ZEROES CHARACTER.

5. IT IS POSSIBLE FOR THIS CRCC CHARACTER TO BE ALL ZEROES, IN WHICH CASE A READ DATA STROBE WILL NOT BE GENERATED.

6. A FILE MARK IS A SINGLE CHARACTER RECORD HAVING "1" BITS IN CHANNELS 3, 6, AND 7 FOR BOTH THE DATA CHARACTER AND THE LRCC. THE CRCC CONTAINS ALL ZEROES. THE FILE MARK IS SEPARATED BY NORMAL IRG's (.6 INCH) FROM THE PREVIOUS AND FOLLOWING RECORDS. OPTIONALLY, A 3.5 INCH GAP CAN BE ERASED PRIOR TO WRITING A FILE MARK.

Figure 1-5. 9-Track Format

SECTION II

INTERFACE

2.1   INTRODUCTION

There are two interfaces to the Formatter, one to the computer
adaptor (J101 for external adaptor or J2 for internal adaptor) and one
to the tape units(J102). (See Figure 1-1, page 1-4.)

If the internal adaptor is utilized, then connector J103 is
available to interface the adaptor to the computer. Datum printed circuit
board #170189 is available for constructing the adaptor internally. The
P. C. Board can accept up to 196 14 or 16 pin wire wrap sockets.

The interface connectors are 100 pin Amp 583485-3 printed cir-
cuit edge connectors which mate to DATUM part number 170192 cable termin-
ator printed circuit plug-in board.

Individual stranded twisted pair wires should be used of 22 to
26 AWG. Maximum length should be 6' for the computer adaptor interface
and 20' (total) for the tape unit "Daisy Chain" bus.

The twisted pair wire should have at least one twist per inch
and minimum insulation thickness of .01 inch.

The ground wire of each twisted pair should be terminated to
ground as close to the origin or destination of the signal as possible
(within 6 inches maximum) to minimize ground loop currents "crosstalk"
effects.

The interfaces are listed in Tables 2-1 and 2-2. The terms
with a "bar" over them are "low" (0V) when active and the terms without
a bar are "high" (+5V) when active.

2.2 FORMATTER/TRANSPORT(S) INTERFACE

Table 2-1 lists the signals and the pins on which the signals appear.

Table 2-1. Formatter/Transport(s) Interface

J102 Pin	Formatter to Transport		J102 Pin	Transport to Formatter	
60	$\overline{\text{SLCTA}}$	Transport Address	64	$\overline{\text{RDY}}$	Status
53	$\overline{\text{SLCTB}}$		66	$\overline{\text{ONL}}$	
58	$\overline{\text{SLCTC}}$		62	$\overline{\text{RWD}}$	
54	$\overline{\text{SLCTD}}$		70	$\overline{\text{FPT}}$	
			57	$\overline{\text{LDP}}$	
34	$\overline{\text{SFC}}$		41	$\overline{\text{EOT}}$	
56	$\overline{\text{SRC}}$		76	$\overline{\text{NRZ/PE TRANSPORT}}$	
36	$\overline{\text{RWC}}$		78	$\overline{\text{SINGLE/DUAL HEAD}}$	
55	$\overline{\text{OFC}}$		80	$\overline{\text{LOW/HIGH SPEED}}$	
44	$\overline{\text{SWS}}$	Control	72	$\overline{\text{7 TRK/9 TRK}}$	
8	$\overline{\text{OVW}}$		74	$\overline{\text{DDI}}$	
94	$\overline{\text{RTH1}}$		24	$\overline{\text{RDP}}$	Read Data
92	$\overline{\text{RTH2}}$		14	$\overline{\text{RD0}}$	
43	$\overline{\text{WARS}}$		32	$\overline{\text{RD1}}$	
46	$\overline{\text{DDS}}$		18	$\overline{\text{RD2}}$	
			20	$\overline{\text{RD3}}$	
45	$\overline{\text{WDS}}$	Write Data Strobe	28	$\overline{\text{RD4}}$	
48	$\overline{\text{WD0}}$	Not Used for	30	$\overline{\text{RD5}}$	
50	$\overline{\text{WD1}}$	7 Track NRZI	10	$\overline{\text{RD6}}$	
51	$\overline{\text{WD2}}$		12	$\overline{\text{RD7}}$	
49	$\overline{\text{WD3}}$				
52	$\overline{\text{WD4}}$	Write Data	6	$\overline{\text{RDS}}$ (1)	Read Strobe
37	$\overline{\text{WD5}}$				
38	$\overline{\text{WD6}}$				
42	$\overline{\text{WD7}}$				
40	$\overline{\text{WDP}}$				
	Total = 24			Total = 21	

Notes: (1) NRZI Formatter Only

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2.2.1   Formatter to Transport

2.2.1.1   Transport Address

$\overline{\text{SLCTO}}$ through $\overline{\text{SLCT3}}$ - Transport Select Lines. Four select lines gated with the Formatter Address signal to select one of the "daisy chained" transports.   Developed by decoding the S1 and S2 address lines from the computer adaptor.

2.2.1.2   Control

The control lines activate the selected transport when it is "READY" and "ON LINE".

$\overline{\text{SFC}}$ - Synchronous Forward Command. A level which, when low, causes the selected transport to "ramp" up to speed and drive forward at the rated speed until the level goes back high. When switched to the high level, the transport "ramps" down to halt.

$\overline{\text{SRC}}$ - Synchronous Reverse Command. A level which, when low, causes the same action as $\overline{\text{SFC}}$ except in reverse tape motion.

$\overline{\text{RWC}}$ - Rewind Command. A negative going pulse which causes the selected transport to rewind to load point.

$\overline{\text{OFC}}$ - Offline Command. A negative going pulse which causes the selected transport to revert to manual control. Transport must be manually placed "ON LINE" before it can again be operated.

The offline command can be transmitted to a tape transport that is rewinding (even though the transport status indicates NOT READY).

$\overline{\text{SWS}}$ - Set Write Status. The level of this signal is inspected within 20 microseconds after a SFC or SRC command is initiated to set the

selected transport to the write or read mode. This mode is maintained until the next SFC or SRC command is initiated.

The write mode within the transport is also switched to read mode if:

a) A RWC or OFC command is received.

b) Loss of interlock occurs.

c) The transport is manually switched offline.

$\overline{OVW}$ - Over Write. This signal is a level which causes the transport write current enable/disable to "ramp" on and off to minimize rate of change of recorded inter block gap magnetism when rewriting a record in the EDIT mode.

This signal level also causes the write current and DC erase head current to be turned off immediately after rewriting the new record (to keep from erasing the beginning of the next record).

$\overline{RTH1}$ - Read Threshold 1. This level selects a high threshold for marginal checking of written records when utilizing a single stack head. This is usually accomplished by backspacing over a newly written record and then reading forward in the high threshold mode to perform a parity check.

$\overline{RTH2}$ - Read Threshold 2. This level selects an extra low threshold for recovery of very low quality signals (on transports so equipped).

$\overline{WARS}$ - Write Amplifiers Reset. This signal controls the early turn off of write and erase currents after rewriting a record in the EDIT mode.

The negative going transition of this signal initiates the write current turn off. In NRZI transports, this signal also generates the LRC character.

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$\overline{DDS}$ - Select high density. Low = select high density (for NRZI Formatter only) for 7 track transport.

2.2.1.3   Write Data

$\overline{WDS}$ - Write Data Strobe. This is a clock utilized to copy the write data ($\overline{WDP}$ and $\overline{WDO}$ through $\overline{WD7}$) in to the selected transport write flip-flops. The data levels <u>must</u> be static during $\overline{WDS}$ and the trailing edge (positive going) of $\overline{WDS}$ is used to clock the flip-flops. The clock rate is <u>twice</u> the character rate for 1600 CPI and <u>at</u> the character rate for NRZI.

$\overline{WDP}$, $\overline{WDO}$ through $\overline{WD7}$ - Write data. $\overline{WDP}$ is the odd parity bit, $\overline{WDO}$ is the most significant bit, and $\overline{WD7}$ is the least significant bit. $\overline{WDO}$ and $\overline{WD1}$ are not used for 7 track NRZI operation.

These signals are presented to the selected transport along with the $\overline{WDS}$ clock. For the 1600 CPI Formatter, the first negative going transition (in writing a record) is the "zero bit" of the preamble. The write data is presented in phase encoded form. For the NRZI Formatter, the write data is presented in logic level form (low = logic 1, high = logic 0).

2.2.2   <u>Transport to Formatter</u>

2.2.2.1   Status lines.

$\overline{RDY}$ - Ready. A level that is low only when the selected transport is:
   a)   Interlocked.
   b)   Through the initial load or rewind to load point sequence.
   c)   On line.
   d)   Not rewinding.
   Note: A transport will go NOT Ready for approximately .5 second after reversing into load point and does not go Ready until approximately .5 second after termination of a Rewind.

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$\overline{\text{ONL}}$ - On line. A level that is low when the selected transport is manually switched on line (to place it under remote control).

$\overline{\text{RWD}}$ - Rewinding. A level which is low while the selected transport is rewinding. The level remains low until the transport completes the automatic "return to load point" sequence but the transport does not become Ready until approximately .5 second after the $\overline{\text{RWD}}$ signal terminates.

$\overline{\text{FPT}}$ - File Protect. A level which is low when the selected transport has a supply reel of tape mounted which does not have a write enable ring installed.

$\overline{\text{LDP}}$ - Load Point. A level which is low when the selected transport's beginning of tape reflector is located under the photo sensor, interlocks are made, and the initial load or rewind sequence is completed.

$\overline{\text{EOT}}$ - End of Tape. A level which is low when the end of tape reflector is under the photo sensor in the selected transport. This signal is not staticised and neither the positive or negative going transition is "clean".

$\overline{\text{NRZ}}$/PE - Non Return to Zero/Phase Encoded. A level which reports the selected transport type. Low for NRZ type, High for PE type.

$\overline{\text{SINGLE}}$/DUAL - Head Stack. A level which reports the selected transport head type. Low for single stack, High for dual stack "read while writing".

$\overline{\text{Low}}$/High - Transport Speed. A level which reports the selected transport tape motion speed.

Low = low speed

High = high speed

$\overline{7\ TRK}/9\ TRK$ - Transport Type.

        Low = 7 track

        High = 9 track

$\overline{DDI}$ - Data Density Indicator

        Low = High Density Selected

        High = Low Density Selected

2.2.2.2   Read Data & Read Clock

$\overline{RDP}$, $\overline{RD0}$ through $\overline{RD7}$ - Read Data.

a) 1600 CPI Formatter:

Read Data from the selected transport is identical to the
Write data wave forms supplied to the transport. There is
no read strobe.

The Phase Encoded signals are high during an Inter Block Gap
or when the tape is not in motion. In the forward direction
the first negative going transition is the zero bit of a
preamble. In the reverse direction the first negative going
transition is the last "phase" transition of the postamble
hence the zero bit transition will be a positive going
transition in read reverse.

b) NRZI Formatter:

Read Data is in logic level form (low = logic 1, high =
logic 0) and is presented along with a negative going read
strobe $(\overline{RDS})$.

2.3   FORMATTER/COMPUTER ADAPTOR INTERFACE

2.3.1   General

Table 2-2 lists the signals and pins for the Formatter/computer
adaptor interface.

All signals from the Formatter to the Computer Adaptor may be "daisy chained" to a second Formatter such that one of the two Formatters may be addressed to operate with the Computer Adaptor. In order to accomplish this, all such signals are "low active" open collector cable driver integrated circuits capable of sinking 25 ma. This allows all such signals to be terminated with resistors to +5V at the Computer Adaptor.

2.3.2   Formatter to Computer Adaptor

2.3.2.1   Status

Most of the status signals are generated by latch flip-flops that retain the occurrence of the status until the next command is accepted by the Formatter (or the Formatter is deselected).

Some of the status signals are levels from the Formatter or from the selected transport that are gated with the Formatter address line hence are not reset by the command clock. These status signals are marked by note 1 in Table 2.

$\overline{EOTS}$ - End of Tape Staticised. When low, the $\overline{EOTS}$ level indicates selected tape transport is on or has passed over (in the forward direction) the EOT reflective tab. The $\overline{EOTS}$ signal remains low until a "reverse direction" command (such as rewind, backspace or read reverse) is accepted by the Formatter. Thus the program only need check for $\overline{EOT}$ after completion of writing each record.

$\overline{EOTS}$ is also reset by power on, or the EXT RESET signal from the Computer Adaptor.

$\overline{REJECT}$ - Rejected Command Status. Goes low when the command accompanying the command clock (STROBEC) is rejected by the Formatter.

Table 2-2. Formatter/Computer Adaptor Interface

J101/J2 Pins		Formatter to Computer Adaptor		J101/J2 Pins		Computer Adaptor to Formatter	
59		EOTS		71		FAD1	Addressing
80		REJECT		91		S1	
73	1) 5)	7 TRK		84		S2	
24	1)	NRZ					
22	1)	SINGLE		5		STROBEC	Command Clock
20	1)	LOW					
87		TMER		92		EXT RJCT	
93		PARITY ER	Status	90		SET REV	
70		FM		32		SET WCC	
95	1)	RDY		55		SET WFM	
9	1)	RWDG		57		SET GAP	Commands
43	1)	FPT		89		SET FSR	
47	1)	LDP		58		SET RCC	
31		WCC		64		SET CLR	
38		RCC		68		SET REW	
	4)	IDENTS		61		SET OFL	
	4)	CERS					
				66	3)	GEN ODD PARITY	
19		RP		77	3)	HI DENSITY	
15		R0		6		THR1	
26		R1		8		THR2	Modes
17		R2		85		EDIT	
25		R3	Read Data & Clock	63	3)	TRD	
11		R4		75		STOP SPACE	
30		R5		29	3)	CD	
13		R6					
28		R7		37		B0	
21		RSTROBE		62		B1	
				39		B2	
94		CBUSY		42		B3	
65		DBY		45		B4	Write Data
78	2)	RCAS		52		B5	
82		DATA FLAG	Data Transfer Flag	46		B6	
69		WRMSB	Write Most Signif. Byte	49		B7	
76		RJCT	Reject Pulse				
79		CK WD CNT	Check Word Count Pulse	7		W/R ACK Data Transfer Acknowledge	Control
34		CLK	Clock	72		HALT Last Word Transferred	
88		WRP	Write Clock Precede	67		EXT RESET	
		Total = 36				Total = 33	

1) Status levels not reset by acceptance of new command.

2) Always 1 when 1600 Formatter is addressed.

3) Not used by 1600 Formatter.

4) Always 0 (open circuit) from NRZI Formatter.

5) Always 0 (open circuit) from 1600 Formatter.

The reject status is needed to keep the computer program from "hanging up" when it issues a command that the Formatter can't perform. Normally the computer adaptor is designed to interrupt the program when the commanded function terminates (based on the Formatter returning to the NOT busy state). If the Formatter can't perform the commanded function, the $\overline{RJCT}$ pulse can be utilized to set the interrupt. When interrupted, the $\overline{REJECT}$ status line can be inspected by the program (before going on to the next function) to ascertain if the command was accepted.

The following conditions cause a reject:

a) Formatter busy with transport motion or selected transport busy and any command other than a clear is issued.

b) Reverse motion command issued while at BOT.

c) Write command issued while no write ring is installed on selected transport.

d) Any "external reject" condition exists in the computer adaptor (a typical use is detection of a non-valid command code).

$\overline{7\ TRK}$ - Seven Track Tape Transport Selected. Available only if tape unit is equipped to supply this status.

             Low = 7 track transport is selected.
             High = 9 track transport is selected.

$\overline{NRZ}$ - Non Return to Zero Tape Transport Selected. Available only if tape unit is equipped to supply this status.

             Low = NRZI transport selected.
             High = 1600 PE transport selected.

$\overline{SINGLE}$ - Single Gap Head Transport Selected. Available only if tape unit is equipped to supply this status.

             Low = Single Gap Head (Read/Write).
             High = Dual Gap Head (Read while writing).

$\overline{\text{LOW}}$ -·Low Speed Tape Unit Selected. Available only if tape unit
is equipped to supply this status.

> Low = Low Speed.
>
> High = High Speed.

$\overline{\text{TMER}}$ - Data Transfer Timing Error Status.

> Low = Error.
>
> High = No Error.

Level that indicates detection of computer adaptor failure to
transfer a character before the next character transfer is required. This
check is performed both in write and read modes.

$\overline{\text{Parity ER}}$ - Parity Error Status.

> Low = Error

Level that indicates error condition was detected on last operation.

a) 1600 CPI Formatter:
   1. Correctable error occurred (CERS will be low also).
   ·2. Uncorrectable error occurred (CERS will· be high).
   3. False preamble or postamble was detected.
   4. Skew error.
   5. Multi track dropout.

For an error condition consisting of a vertical parity error
without a corresponding single track dropout the $\overline{\text{PARITY/ER}}$ line will be
pulsed low during Read Clock (RSTROBE) time to tag the character in question.

b) NRZI Formatter:
   1. LRC error occurred.
   2. VRC error occurred.

$\overline{\text{FM}}$ - File Mark Status.

> Low = File mark detected.
>
> High = No file mark detected.

$\overline{\text{RDY}}$ - Ready Status.

> Low = Selected transport is ready.
>
> High = Selected transport is not ready.

$\overline{\text{RWDG}}$ - Rewinding Status.

> Low = The selected transport is rewinding or is not
> ready yet after a rewind.
>
> High = The selected transport is not rewinding.

The $\overline{\text{RWDG}}$ status flip-flop doesn't indicate termination of rewind until the transport also indicates READY (if a _single_ transport is commanded to rewind and the Formatter waits until the rewind terminates). In multiple transport systems it is possible to initiate rewind on one transport, select and operate another transport, and then re-select the first transport and find that it is _not_ reporting the rewinding condition, yet isn't ready (because it _stays_ not ready for approximately .5 second after termination of rewind). For this reason, the computer program should always check for ready status as well as "done rewinding" before proceeding after any rewind on multiple tape systems.

$\overline{\text{FPT}}$ - File Protect Status.

> Low = Selected transport is protected against writing
> (no write ring installed on supply reel).
>
> High = Writing is enabled.

$\overline{\text{LDP}}$ - Load Point (see $\overline{\text{LDP}}$ under section 2.2.2.1)

> Low = Selected transport is at BOT.
>
> High = Not at BOT.

$\overline{\text{WCC}}$ - Write Mode. Level that indicates when the Formatter is writing a record.

> Low = Writing.
>
> High = Not writing.

Typically used with "unpack" signal $\overline{\text{WRMSB}}$ to control the computer data requests and computer adaptor to Formatter write strobes ($\overline{\text{W/R ACK}}$) when unpacking a computer word into two tape characters.

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$\overline{RCC}$ - Read Mode. Level that indicates the Formatter is performing a read operation.

$$Low = Reading$$
$$High = Not\ reading$$

Typically used to indicate "data transfer direction" to the computer and to disable detection of read mode record length error logic (on the computer adaptor) when not reading. Also disables the read mode control of the computer adaptor data transfer control logic even though read strobes are received for "read while write" operations.

$\overline{IDENTS}$ - 1600 CPI Identification Status.

$$Low = 1600\ CPI\ tape\ identified\ at\ BOT.$$

Signals detection of 1600 CPI "Burst" when selected tape is commanded to move off BOT. (1600 CPI Formatter only)

$\overline{CERS}$ - Corrected Error Status.

Low = Single track error was corrected by the 1600 Formatter in the last record. Always logic 0 (open circuit) from NRZI Formatter.

2.3.2.2   Read Data & Clock

The read data is completely "buffered" in a special register (supplied on the Formatter) such that no external register in the computer adaptor is required. The data is allowed to change just before the leading edge of the read strobe pulse ($\overline{RSTROBE}$) and is static throughout $\overline{RSTROBE}$ and until the leading edge of the next $\overline{RSTROBE}$ pulse.

The $\overline{RSTROBE}$ pulse actually isn't needed for simple 8 bit single character interfaces to computers but is included to allow more sophisticated computer adaptors to be built which "pack" successive pairs of tape character into a 16 bit word for computer entry. In this case, at least 8 bits must be stored on the computer adaptor.

The $\overline{\text{DATA FLAG}}$ Control signal goes low at the trailing edge of the $\overline{\text{RSTROBE}}$ pulse to signal that read data is ready for output from the Formatter. The computer adaptor must respond with $\overline{\text{W/R ACK}}$ before the next RSTROBE pulse occurs or the data transfer timing error ($\overline{\text{TMER}}$) will latch.

$\overline{\text{RSTROBE}}$ - Read Strobe Clock. Negative going pulse that can be utilized to clock the levels present on the data lines into an external register. Normally also used by the computer adaptor to detect read record lengths that are longer than expected by gating with a signal that indicates all the characters asked for by the computer program have been input. If more $\overline{\text{RSTROBE}}$'s occur, after this signal indicates that the record length asked for has been input, then the record is longer than expected.

2.2.2.3   Control

$\overline{\text{CBUSY}}$ - Controller Busy.

　　　　　Low = Controller busy.

　　　　　High = Controller not busy.

Goes low at the leading edge of the STROBEC command clock when a new command is accepted and remains low until the operation has finished and all tape motion has ceased.

The offline command does not cause the controller to go to the busy state and the rewind command can be jumper selected to not cause the controller to go to the busy state.

The computer adaptor normally makes use of $\overline{\text{CBUSY}}$ to inhibit new commands. However, for continuing with writing or reading "on-the-fly", the computer adaptor logic can ignore the $\overline{\text{CBUSY}}$ level and initiate the next command when the $\overline{\text{DBY}}$ (data busy) signal terminates at the beginning of the IRG (inter-record gap).

$\overline{\text{DBY}}$ - Data Busy

> Low = Data write or read portion of operation is in process.

The $\overline{\text{DBY}}$ does not occur for offline, rewind, or clear & select type commands.

The $\overline{\text{DBY}}$ signal begins after the initial "Up to Speed" delay transpires and remains low until the motion command line (SFC or SRC) to the selected transport is terminated. At this time the transport begins deceleration to stop in the inter-record gap. If continuous "on-the-fly" operation is desired (to halve the amount of time required to traverse the IRG) then the computer adaptor can initiate the next command immediately after $\overline{\text{DBY}}$ terminates rather than waiting until $\overline{\text{CBUSY}}$ terminates. The only restrictions are that the next command must be the same type and direction as the preceding command.

The computer adaptor is usually designed to notify the computer program when $\overline{\text{DBY}}$ terminates and it is left up to the computer program to read status (to determine if the last command terminated correctly, check that the new command is of the same type and direction as the old, and issue the new command).

Commands are "typed" as to whether they are read or write commands as follows:

Command Types

Read	Write
Space Forward	Erase 3" Gap
Space Reverse	Write File Mark
Read Record Forward	Write 1 Record
Read Record Reverse	
Test Read Forward	

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$\overline{RCAS}$ – Read Clock Activity Sensor. Used in NRZI Formatter to separate the CRC/LRC characters from the data character in a read forward operation. In NRZI Formatter, low = data portion of record. In read reverse operations, $\overline{RCAS}$ does not separate the CRC/LRC characters from the data hence the program must expect one or two more characters to be input than in the read forward mode and must discard the CRC/LRC characters. This may be done for the 9 track case by setting the record length to two characters more than in the forward mode. Since the CRCC may be all zero, program would have to test the record length error status to find out whether to discard: 1. The first character only (LRCC) if record is too short. 2. The first two characters (LRCC & CRCC) when the record is the expected two characters longer than in the forward mode. In the 7 track case the record length must be set to one extra character (only LRCC is generated for 7 track) and the record length error status inspected to determine whether to discard the first character or not. If the record is the expected one character longer, the first character (LRCC) must be discarded. If the record indicates that it is too short, then the LRC character must have been zero hence the first character is data and should be retained.

For 1600 CPI Formatter, the signal is switched low and held there as long as the 1600 CPI Formatter is addressed.

$\overline{DATA}$ $\overline{FLAG}$ – Data Transfer Request Flag.
Low = transfer request active.
The data flag is utilized for both write and read functions. It is cleared by the leading edge of the $\overline{W/R\ ACK}$ pulse from the computer adaptor.

In the case of writing, the data flag is set one character time before the character is needed hence the amount of time allowed before the $\overline{W/R\ ACK}$ pulse must be received is dependent solely upon the tape speed. If the $\overline{W/R\ ACK}$ pulse is not received in time, the $\overline{TMER}$ (data transfer error) status latch is set.

In the case of reading, the data flag is set at the trailing edge of the read strobe ($\overline{\text{RSTROBE}}$) pulse. Due to tape speed variations and bit crowding effects, the worst case time allowed may be as short as one-half the character time but is also directly dependent upon the tape speed. If the $\overline{\text{W/R ACK}}$ pulse is not received before the next $\overline{\text{RSTROBE}}$ is generated then the $\overline{\text{TMER}}$ latch is set.

$\overline{\text{WRMSB}}$ - Write Most Significant Byte.

Low = Odd characters

High = Even characters

Flip-flop that toggles to the opposite state for each character to be written on tape to allow 16 bit computer words to be easily "unpacked" into two 8 bit tape characters by the computer adaptor.

Not needed for simple 8 bit transfer modes of operation.

$\overline{\text{WRMSB}}$ is switched shortly before $\overline{\text{DATA}}$ $\overline{\text{FLAG}}$ is set and is static throughout $\overline{\text{DATA}}$ $\overline{\text{FLAG}}$ time hence can be gated with $\overline{\text{DATA}}$ $\overline{\text{FLAG}}$ to determine whether to set the computer data request flag or to generate the $\overline{\text{W/R ACK}}$ signal back to the Formatter when "unpacking".

$\overline{\text{RJCT}}$ - Reject Pulse. Negative going pulse which sets the $\overline{\text{REJECT}}$ status flip-flop.

This pulse can be utilized by the computer adaptor to trigger the interrupt normally set by the $\overline{\text{DBY}}$ or $\overline{\text{CBUSY}}$ termination.

The computer program should always check status after a command operation signals completion to determine if the command was accepted & performed correctly or if the command was rejected.

$\overline{\text{CK WD CNT}}$ - Check Word Count Pulse. Negative going pulse at the end of each record which is usually used by the computer adaptor to

set a "record length error" status bit if the record read is shorter
than expected.

Usually gated with signal in computer adaptor that signifies
that the record length expected by the computer program has been input.
If this signal isn't set when $\overline{\text{CK WD CNT}}$ pulse occurs then the record must
have been shorter than expected.

$\overline{\text{CLK}}$ - Clock. Clock derived from crystal oscillator on formatter.

$\overline{\text{WRP}}$ - Write Pulse Precede. Pulse that precedes write flag (DATA
FLAG) which may be utilized to test for data transfer complete before the
next one is initiated.

2.3.3   Computer Adaptor to Formatter

General

The computer adaptor driver circuits to the Formatter should be
capable of sinking 30 milliamps when at the low level. They need not sup-
ply any current when at the high level since resistor termination's to +5V
are supplied within the Formatter. The drivers are not required to be
"open collector" types however (since no "wired or" function is utilized).

2.3.3.1   Addressing

$\overline{\text{FAD1}}$ - Formatter Address
            Low = Formatter #1 addressed.
            High = Formatter #Ø addressed.
This level must remain static throughout execution of any command.
The Formatters have capability of jumper specifying whether their address
is Ø or 1.

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S1, S2 - Transport Select Address Lines. These levels are decoded by the Formatter to select one of the four transports. The levels must remain static throughout any operations except Rewind. A transport can be commanded to rewind and a different transport selected immediately.

S1	S2	Tape Unit Selected
Low	Low	0
High	Low	1
Low	High	2
High	High	3

2.3.3.2 Commands & Command Clock

General

The commands are stored in the Formatter by the command clock pulse if the command is not "rejected" by the Formatter.

$\overline{CBUSY}$ is set at the trailing edge of the command if the command is accepted. When the $\overline{CBUSY}$ signal terminates, the operation has been completed by the Formatter and the Formatter is ready to accept another command.

Commands - The offline command never causes $\overline{CBUSY}$ to set and $\overline{CBUSY}$ set upon rewind command acceptance is jumper selectable.

The command signals must be static from 100 nanoseconds before the leading edge to 100 nanoseconds after the trailing edge of the command clock.

Table 2-3. illustrates the valid Formatter functions and the corresponding command lines that are required to be "high" in order to

initiate the associated function. All other command lines must be "low" with the exception of EXT RJCT which over-rides all other commands.

Command Clock. The command clock (STROBEC) must be a positive going pulse of 100 nanoseconds (or more) pulse width.

Table 2-3. Commands

Formatter Function	Command Signals "High"
1) Write File Mark	SET WFM
Erase 3" Gap then Write File Mark	SET WFM/SET GAP
1) Write Record	SET WCC
Erase 3" Gap then Write Record	SET WCC/SET GAP
2) 3) Space Forward	SET FSR
1) 2) 3) Space Reverse	SET REV
3) 4) Read Forward	SET RCC
3) Read Reverse	SET RCC/SET REV
Erase 3" Gap	SET GAP
Reject	5) EXT RJCT
Clear	SET CLR
Rewind	SET REW
Offline	SET OFL

5) overrides all other commands.

4) can be in either normal or test read mode.

3) can be read in various read threshold modes.

2) can be multiple record spacing under control of STOP SPACE mode.

NOTES: 1) can be in edit or normal modes.

2.3.3.3   Modes

The mode lines are levels which are <u>not</u> stored in the Formatter by the command clock hence must be stored by the computer adaptor. They

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must all remain static (with the exception of STOP SPACE) throughout execution of a command by the Formatter.

GEN ODD PARITY - Generate Odd Parity. This line is ignored by the 1600 CPI Formatter. The NRZI Formatter uses it to control parity generation for 7 track tapes (if in the REMOTE parity control mode). Low = even parity, high = odd parity.

HI DENSITY - Select High Density Write Mode. The 1600 CPI Formatter ignores this line. The NRZI Formatter utilizes the line to control High/Low write density selection for 7 track tape transports (if in the REMOTE density select mode) high = low density, low = high density.

THR1 - Select Read Threshold One. Used for single track head transports to enable a marginal read amplitude check to be made immediately after writing each record (by backspacing then reading forward) to determine whether that section of tape should be erased and the record re-written further down the tape.

Low = Marginal threshold (high threshold).
High = Normal threshold.

THR2 - Select Read Threshold Two. Used for transports equipped with the extra low read threshold capability for recovery of low amplitude data.

Low = Extra low threshold.
High = Normal threshold.

EDIT - Edit Mode. Enables records to be replaced with equal length records anywhere on a tape.

Low = Edit mode.
High = Normal mode.

The record to be replaced must first be backspaced over in the edit mode (to position the write head correctly) then rewritten in the edit mode (to cause the erase head and write current to be turned off

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immediately at the end of the record before the erase head erases into the following record).

$\overline{\text{TRD}}$ - Test Read Mode.

> Low = Normal mode.
>
> High = Test read mode.

Not used by 1600 CPI Formatter. The NRZI Formatter utilizes the line to control access to the CRC/LRC characters (when reading forward) for diagnostic and maintenance purposes. In test read mode, the data flag is allowed to trigger for the CRC/LRC characters.

STOP SPACE - Stop Forward or Backspacing.

> High = Normal (Formatter spaces 1 record for each
> command).
>
> Low = Continuous spacing.

The $\overline{\text{DBY}}$ signal can be used by the computer adaptor to count the number of records spaced over to determine when to switch STOP SPACE high to terminate multiple record spacing. The leading edge of $\overline{\text{DBY}}$ should be used to count·records and switch STOP SPACE.

$\overline{\text{CD}}$ - Core Dump Mode.

> Low = Core dump mode.
>
> High = Normal mode.

Ignored by 1600 CPI Formatters. The NRZI Formatter utilizes this line to operate 9 track tape machines in a 7 track mode where in 7 track type file marks are written and detected. This mode is necessary for compatibility with some computer systems in the field.

2.3.3.4 Write Data

The write data consists of eight lines which must be stable during the $\overline{\text{W/R ACK}}$ pulse transmitted from the·computer adaptor to the Formatter. Odd parity is generated in the Formatter for recording.

A write data storage register is included in the Formatter so that none is required in the computer adaptor.

$\overline{B0}$ through $\overline{B7}$ are the write data lines. $\overline{B0}$ is the most significant bit. (low = logic 1, high = logic 0).

2.3.3.5   Control

$\overline{W/R\ ACK}$ - Write/Read Acknowledge. This negative going pulse is used to acknowledge the $\overline{DATA\ FLAG}$ request for data transfer in both read and write operations. The pulse must be at least 100 nanoseconds wide.

In the write operation the $\overline{W/R\ ACK}$ pulse is used to clock the levels present on the $\overline{B0}$ through $\overline{B7}$ lines into the Formatter write storage register and to reset the $\overline{DATA\ FLAG}$ flip-flop.

In the read operation the $\overline{W/R\ ACK}$ pulse is merely used to reset the $\overline{DATA\ FLAG}$ flip-flop.

The leading edge of the $\overline{W/R\ ACK}$ signal is delayed in the Formatter and utilized to reset the DATA FLAG flip-flop such that the Formatter $\overline{DATA\ FLAG}$ signal can itself be gated at alternate character times onto the $\overline{W/R\ ACK}$ line to reset itself (in "Pack/Unpack" modes of operation). This is useful since actual data transfers with the computer must take place only for every other tape character time yet the Formatter data transfer requests must be serviced for every 8 bit tape character (since it only provides storage for one 8 bit tape character).

Halt - Halt data transfer.

The signal is used to initiate termination of writing a record or to terminate data transfer requests ($\overline{DATA\ FLAG}$) from the Formatter when

reading a record. The signal is normally low and should go high after the last $\overline{\text{W/RACK}}$ pulse to signal termination of the record. Must remain high until the next command is issued.

In the write operation, the 1600 CPI postamble (or the NRZI CRC/LRC character) are written and a portion of the inter-record gap is erased before the tape transport begins to decelerate to halt in the IRG.

In the read operation, the Formatter continues on until the true end-of-record is detected before initiating the halt in IRG process.

$\overline{\text{EXT}}$ $\overline{\text{RESET}}$ - External Reset. The external reset line allows the Formatter to be cleared to initial conditions from such signals as the computer "start" button etc.

Low = Reset

High = Normal

SECTION III

THEORY OF OPERATION

3.1   INTRODUCTION

This section contains information on the operation of the Model 5091 NRZI Magnetic Tape Formatter.

The information in this section is divided into two major topics. A discussion of the block diagram (Figure 3-1) is presented first, to provide an overall functional description and to illustrate the relationship between the Formatter, the tape transports, and the computer adaptor. A discussion of the command execution, illustrated by timing diagrams, describes operation of the Formatter circuitry during execution of computer-originated instructions.

The Formatter performs three basic functions. These are:

1. Control
2. Write
3. Read

The Formatter provides control over the selected tape unit including all timing necessary to automatically perform all write, read, rewind, space forward or backward, and rewind commands.

Upon completion of the commanded operation, status is provided so that the computer can ascertain whether the operation was performed correctly.

The Formatter performs all the write functions for erasing tape, writing a file mark or writing a record of data. A 3.5 inch gap
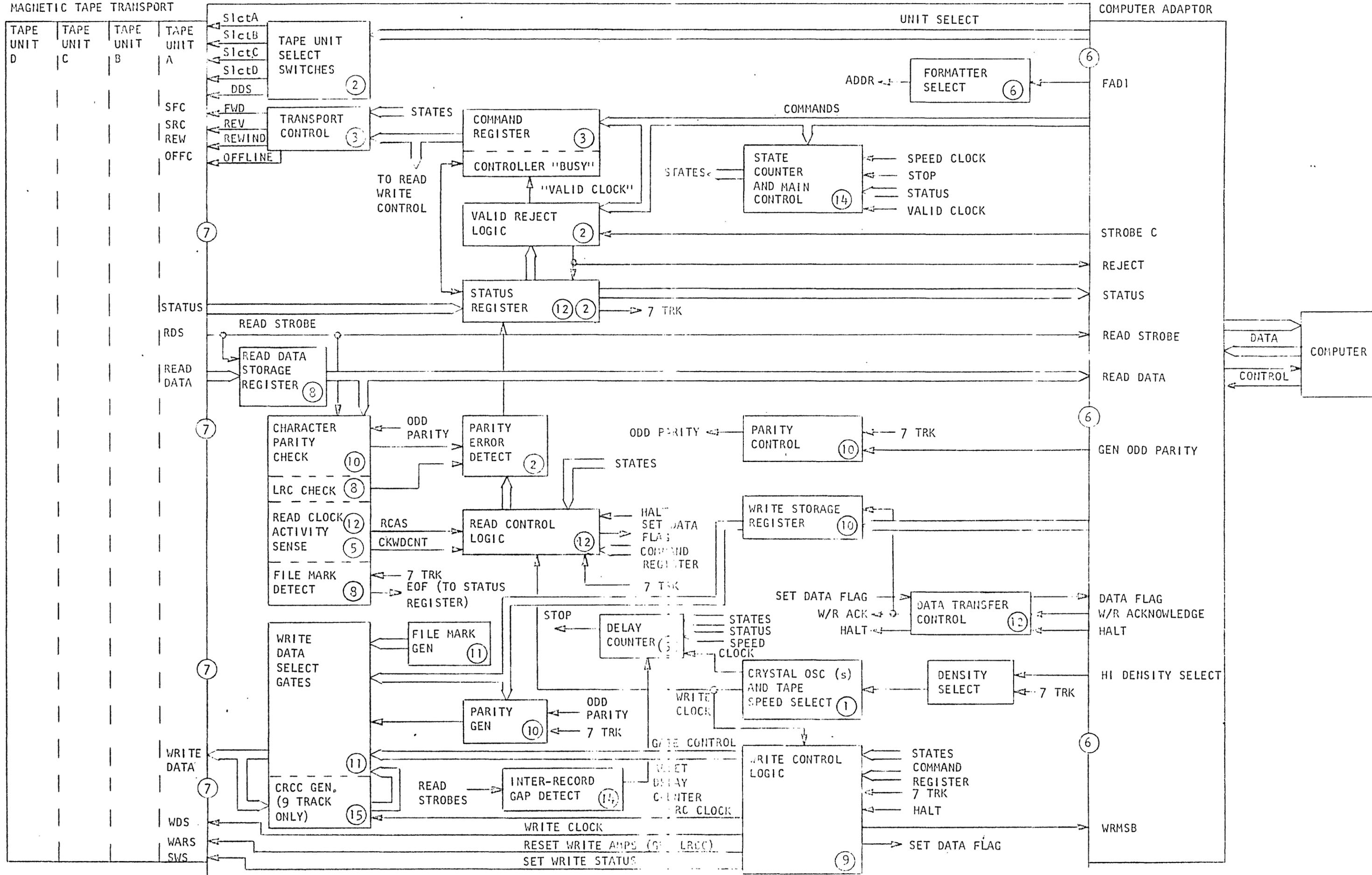
Figure 3-1. NRZI Formatter Block Diagram

is automatically erased before the first record when starting from beginning of tape (BOT). The correct timing delays for erasing the inter-record gap (IRG) is provided and the file mark code is developed by the Formatter.

The task of writing is reduced to mere transfer of the characters on a demand-response basis for the computer adaptor logic.

The Formatter also reduces the reading and spacing operations to a minimum by performing all parity checks and positioning of the head in the IRG's automatically. The task of reading is reduced to transfer of the characters on a demand-response basis.

The Formatter can accommodate as many as four magnetic tape transport units simultaneously. All input/output signal lines are daisy chained to the multiple tape transports, while a single select line is wired to each individual tape transport. Only the selected tape transport unit will respond to the Formatter commands.

3.2   BLOCK DIAGRAM

A simplified block diagram of the NRZI Formatter is shown on Figure 3-1. The block diagram illustrates the various functions performed by the standard 7-track, 9-track NRZI Formatter and shows the relationship between the Formatter, the tape transport units, and the computer adaptor.

The circled numbers refer to the "Logic Diagram Number" on which the indication function is drawn in detail. This number is located in the lower right hand corner of the detailed logic drawings.

3.2.1 Command Register & Valid/Reject Logic

When a command is output from the computer, the command
and a strobe pulse are delivered from the computer adaptor to the
Formatter valid command detect logic. If the command is acceptable,
a valid clock is generated to enable the command to be loaded into the
command register. If the command is not valid, a "reject" pulse is
returned to the computer adaptor. Each valid clock initiates a system
reset (SRS) pulse, which is, in turn, used to reset the Formatter to
initial conditions.

3.2.2 CBUSY

The valid clock also sets the controller busy flip-flop.
The controller busy flip-flop normally is used by the computer adaptor
to signal termination of all commands. The transport control logic resets
the controller busy flip-flop after all tape motion has ceased for the
commanded function. If "on-the-fly" writing or reading is desired, the
Data Busy status must be utilized by the computer to initiate the next
command as soon as Data Busy terminates.

3.2.3 Transport Control

The transport control logic develops the forward, reverse,
rewind and offline commands to the selected tape transport unit under
control of the command register and the state counter.

3.2.4 Formatter Select

The Formatter select logic allows a Formatter to be assigned
the number zero or one so that two Formatters can be "Daisy Chain" con-
nected to one computer adaptor to provide up to eight transports or a
mixture of NRZI and 1600 CPI Phase Encoded Transports.

3.2.5   Tape Unit Select

The Tape Unit Select switches allow the operator to assign unit numbers 0, 1, 2 or 3 to any of the four tape units. This allows physical tape units to be switched without requiring changes to the computer program. Indicator lamps give visual indication of which tape unit is selected.

3.2.6   State Counter and Main Control

The State Counter breaks the major operations (such as write and read) down into successive sub "states" that are sequentially stepped through to perform the operation. These states are:

State Count	Function
0	Rest
1	Predelay (not BOT and not 3 inch gap)
2	Predelay (BOT or 3 inch gap)
3	Write or Read execution
4	Postdelay
5	Forward Motion Halt time out
6	Reverse Motion Halt time out
7	Rewind or Clear execution

The "delay" and "time out" states all use the Delay Counter to determine when the state count should terminate and the next state count entered. These delay count times vary dependent on factors such as:

1. Tape speed

2. Single or dual stack head

3. Edit or normal mode

4. Reverse or Forward motion

5. Seven or nine track tape unit selected

The pre and post delays are utilized to erase the inter-record gaps (IRG) and to halt the head in the correct position in the IRG when reading.

State 0 (the "rest" state) is the state the Formatter enters after completing an operation.

State 1 (Predelay) is used to wait for the tape unit to get up to speed and to erase part of the IRG when writing. State 1 is used for predelay when not starting from BOT or not erasing a 3 inch gap.

State 2 (Predelay) is similar to State 1 except a longer delay is implemented to handle the 3 inch gap erased automatically at BOT and for the erase 3 inch gap command.

State 3 (Write or Read Execution) is the State during which the record is written or read. When reading, State 3 is terminated when no more read strobes occur (indicating the IRG has been reached).

IRG detection is also used to terminate State 3 for write operations when utilizing a dual stack read-after-write tape unit (so that the written record can be checked for correct parity). For single stack writes, State 3 is terminated as soon as the LRC character is written at the end of the record.

State 4 (Postdelay) is utilized to halt the head in the correct position in the IRG when reading. When writing, State 4 postdelay erases a portion of the IRG.

State 5 (forward motion halt time out) retains memory of the forward direction of motion during the time interval after the tape unit has been commanded to stop until the unit actually stops (to delay termination of the CBUSY signal until the tape unit has completely halted in the IRG).

The DBUSY status terminates when State 5 is entered so that successive "writes" or successive "reads" may be executed on the fly without stopping in the IRG's.

State 6 (reverse motion halt time out) is similar to State 5 except for reverse motion commands. When performing on-the-fly operations, successive commands issued after DBUSY terminates but before CBUSY terminates must be of the same type. A read cannot follow a write and a forward motion command cannot follow a reverse motion command (or vice versa). There is, of course, no such restriction if the commands are not issued until after CBUSY terminates.

State 7 (Rewind or Clear) is entered upon issuance of a rewind or clear command by the computer. The State is terminated when the tape unit finishes rewinding.

3.2.7   Status Register

The Status Register stores both tape unit and Formatter status so that the computer can inspect the results of an operation after the operation is completed to find out whether the operation was completed correctly or some other action needs to be taken.

The status of the selected tape unit and the Formatter are available for access by the computer at any time.

3.2.8   Parity Control

The Parity Control logic provides manual or program control over selection of odd or even parity for 7 track tape units. Odd parity is automatically selected for 9 track tape units. The output (odd parity) is used by the parity Generator and check logic.

3.2.9   Parity Error Detect

        The Parity Error Detect logic searchs for one or more parity
errors in each tape record. Any detected errors causes the Parity Error
Status bit to be set.

        The read control logic utilizes the Read Clock Actitity
Sense logic(RCAS)output to enable the Parity Error Detect logic to in-
spect the Character Parity Check output only during the data portion of
a record (since CRCC (9 track) and LRCC (7 track) can exhibit either
odd or even parity).

        The output of the LRC Check logic is inspected only after
the entire record (including CRCC and LRCC) has been read.

3.2.10   Character Parity Check

        The Character Parity Check logic checks each character read
from tape for either odd or even parity under control of the Parity Control
Logic.

3.2.11   LRC Check

        The longitudinal Redundancy Character Check logic checks for
an even number of 1's for each individual track down the length of the
record including the CRC and LRC characters.

3.2.12   Read Data Storage Register

        The Read Data Storage Register stores each tape character at
the leading edge of the Read Strobe in such a manner that the Read Data is
static to the computer adaptor interface throughout the entire period until
the leading edge of the next read strobe occurs. This deletes the require-

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ment for a storage register on the computer adaptor which would other-
wise be required to retain the data for the _maximum_ possible time after
the Data Flag is set to give the computer the maximum amount of time to
accomplish the data transfer.

The outputs of the Read Data Storage Register are routed
to the rest of the logic where read data is utilized on the Formatter.

3.2.13   Read Clock Activity Sense

The Read Clock Activity Sense logic is utilized to seperate
the data portion of each record from the CRC and/or LRC characters in the
forward direction. Thus the Set Data Flag (in the Read Control logic)
is allowed to operate only for the data portion of the record which
"strips" off the CRC and/or LRC characters.

The check word count (CKWDCNT) pulse occurs just after the
last data character _but_ _before_ the CRC or LRC character's Read Strobe
destroys the contents of the Read Data Storage Register. The CKWDCNT
pulse is delivered to the Computer Adaptor interface where it may be
utilized to create an _extra_ data transfer request to the computer for the
case where an odd number of characters were read from tape and the "Pack"
mode of operation is being utilized. The CKWDCNT pulse is also typically
utilized on the Computer Adaptor to determine .if the expected number of
characters were read from tape to create status bits which can inform the
computer that the record was too long, too short and/or contained an odd
number of tape characters.

3.2.14   File Mark Detect

The File Mark Detect logic checks for 7 track or 9 track file
marks dependent on which type of tape is selected. The EOF status bit is
developed if a file work is detected in a forwards or backwords direction.

3.2.15   Read Control Logic

The Read Control Logic controls data transfer during State 3 until the IRG is detected at which time the Postdelay (State 4) or one of the Halt delays (State 5 or 6) is entered.

The Set Data Flag signal is generated for each Read Strobe that occurs as long as RCAS indicates that the data portion of the record is present and the Halt signal hasn't occurred.

When the IRG is detected or the computer generates the Halt signal (to indicate it doesn't want any more data) there are no more Data Flag signals generated even though there may be more data in the record.

When reading backwards, the CRC and/or LRC characters are not stripped from the data portion of the record but are included as the first one or two characters read and so must be accounted for and stripped off by the program. The program accounts for these extra characters by setting the expected record length to 2 characters greater for 9 track and 1 character greater for 7 track. The program can strip off the extra characters by noting whether the record was shorter than expected.

For 9 track, if the record was the expected 2 characters longer, then the first 2 characters are the LRC and CRC characters and can be discarded. If the record is not 2 characters longer then the CRC character was all zeros (no read strobe occurs) hence only the first character (LRC) need be discarded.

For 7 track, if the record was the expected 1 character longer, the first character is the LRC character and may be discarded. If the record is not 1 character longer then the LRC character must have been all zeros hence no character needs to be discarded.

The Read Control Logic also controls the forwards and reverse space operations. These operations are identical to reading forward or reverse except the Data Flag is not set for data transfer requests. All parity checks are valid for the spacing operations as well as the reading operations and for read-after-write operations when a dual stack head is employed on the selected tape unit.

Special read modes may also be utilized:

1. Test read
2. Read threshold high
3. Read threshold extra low

In the Test Read mode the CRC and/or LRC characters are not seperated from the data in the forward read operation. This is employed to check the CRC and LRC generator logic by diagnostic programs.

The Read Threshold High mode may be used with single-stack read/write tape units to enable a marginal parity check to be performed on each record immediately after it is written by back spacing over the record and spacing or reading forward over the record in the Read Threshold High mode then checking for parity error status. This marginal check function is automatically performed by dual stack read-after-write tape units since they automatically select the high threshold when in the write mode so that the read-after-write parity checks may be performed while writing.

The Read Threshold Extra Low mode allows tape units equipped with this option to recover low amplitude signals on poor quality tapes.

3.2.16   Write Storage Register

The Write Storage Register is provided so that no register is needed on the Computer Adaptor to store output data from the computer. The Data Transfer logic operates on a request/response basis via the Data

Flag and Write/Read Acknowledge (W/R ACK) signals such that each character is requested a full write clock period before it is needed and the computer can respond any time within this period with a W/R ACK strobe pulse to load the Write Data into the Write Storage Register.

3.2.17   Parity Generator

The Parity Generator creates odd or even parity for each character presented from the Write Storage Register and sends the parity bit to the Write Data Select Gates. The Parity Control logic determines whether odd or even parity is generated.

3.2.18   Write Data Select Gates

The Write Data Select Gates consist of three sets of gates that are enabled by the Write Control Logic to gate the write data (and parity bit) or the File Mark code or the CRC Character onto the write data bus to the tape units.

3.2.19   File Mark Generator

The File Mark Generator generates the appropriate file mark code dependent on whether a normal 9 track file mark, a special 9 track file mark or a 7 track file mark is to be written. The Write Control Logic gates the file mark code onto the write data bus at the appropriate time and generates a Write Clock to write the file mark.

The special 9 track file mark is an option that writes the 7 track file mark code to provide compatibility with some computer manufacturer's hardware and software when writing in the "unpack" mode on a 9 track tape.

3.2.20   CRCC Generator

The Cyclic Redundancy Check Character (CRCC) Generator calculates the CRC Character while writing each record as each data character appears on the write data bus.

At the end of the record (9 track only) the Write Control Logic gates the CRCC onto the bus and geneates a write clock pulse to write the CRC Character. The LRC Character is then written to finish the record. The CRCC may be all zeros and may exhibit odd or even parity.

3.2.21   Write Control Logic

The Write Control Logic operates during State 3 for write, erase and write file mark operations. The Write Control Logic controls the Data Transfer Logic for write operations by developing the Set Data Flag pulse to request each character to be written until the write operation is terminated by the Halt signal from the Computer Adaptor.

Upon receiving the Halt signal, the CRC and/or LRC character is automatically appended to the record and part of the IRG is then erased. If a single stack (read/write) tape unit is selected, the Write Control Logic triggers the State Counter to the State 4 postdelay when it finished writing the LRC character at the end of the record. If a dual stack (read after write) tape unit is selected, the Inter-Record Gap Detect logic is utilized to exit State 3 to State 4 Post delay in order to allow all of the record to be read-after-write parity checked.

The data rate is developed from the write clock frequency from the Crystal Oscillators and tape speed select logic.

The Write Control Logic also sends the Write Most Signifi-
cant Byte (WRMSB) signal to the Computer Adaptor to enable the odd/even
characters to be seperated when "unpacking" a computer word into two
sequential tape characters.

3.2.22   Crystal Oscillators and Tape Speed Select

The Crystal Oscillators provide stable precision clock fre-
quencies for 800/556/200 bits per inch packing dnesities. The Tape
Speed Select and Density Select logic divide down the clock rates to the
appropriate frequencies and select the write clock frequency dependent on
tape speed and packing density.

One set of crystals covers the standard tape speeds from
12.5 to 75 ips.

The Speed Clock signal is utilized by the Delay Counter to
provide all the precise time delays for the Formatter.

The Speed Clock is dependent only on tape speed.

3.2.23   Density Select

The Density Select logic provides control over selection of
Hi or Low density for 7 track tape units. 9 track tape units are auto-
matically operated at only 800 BPI. The Density Selection is normally con-
trolled by the computer program via the Hi Density Select signal but can
be over-ridden by front panel switches.

Different pairs of densities can be accomodated on multiple
7 track tape units, i.e., one unit can be an 800/556 while a second unit
is a 556/200 and a third is an 800/200.

3.2.24   Data Transfer Control

The Data Transfer Control operates in conjunction with the
Read or Write Control logic dependent on whether a Read or Write opera-
tion is active.

The Read or Write Control logic generates the Set Data Flag
pulse to signal that read data is ready for input or to request a write
data character. The Computer Adaptor returns the W/R ACK signal which
clears the Data Flag and is used to strobe the write data into the Write
Storage Register for write operations. When the Computer Adaptor desires
to halt data transfer it generates the HALT signal and the Data Flag sig-
nal is disabled.

3.2.25   Delay Counter

The Delay Counter is a flip-flop divider chain that counts
the Speed Clock pulses to provide precise time intervals for Pre and Post
delays as well as Halt delays. The time interval is defined by the inter-
val from the time the counter is allowed to start counting (from a reset
condition) until the STOP signal is generated by a set of gates that decode
various counts from the Delay Counter. The gate selected for a particular
time interval is dependent on which State the Formatter is in as well as
the configuration of the Formatter and the selected tape unit (provided
by the STATUS signals to the Delay Counter).

3.2.26   Inter Record Gap Detector

The IRG Detector is used to trigger the Formatter from State
3 to the Post Delay State 4, or Halt Delay State 5 or 6 when completing
any read or space operation or any write operation with a dual stack
read-after-write tape unit. The IRG Detector resets the Delay Counter with
each read strobe. After the read strobes quit, the Delay Counter is allowed

to count for a prescribed interval until the STOP time is reached at which time State 3 is terminated.

3.3   COMMANDS

3.3.1   Basic Commands

Basic Commands provided by the Formatter are:

1. Read (one record)
2. Write (one record)
3. Space
4. Write File Mark
5. Erase 3 inch gap
6. Rewind
7. Offline
8. Clear

3.3.1.1   Read and Space

The Read and Space operations can be in the forward or reverse direction in one of three possible modes (normal, read threshold high or read threshold low). In addition, a read forward may be performed in a "Test Read" mode in which the CRC and LRC characters are input to allow diagnostic programs to check the CRC and LRC generator circuits. The Read Threshold High mode is utilized with single stack head (read/write) tape units to allow marginal checking of each record immediately after it is written by backspacing over the record and reading or spacing forward in the Read Threshold High mode and checking for no parity errors. The Read Threshold Low mode provides the ability to recover low amplitude data from poor quality tapes (if the tape unit is equipped with this option.

The space operations can be a single or multiple record under control of the STOP SPACE Computer Adaptor signal. In addition, the backspace operation can be conducted in the EDIT mode to position the write head correctly in the IRG preceeding a record that is to be replaced with an equal length but updated record. BOT will halt back spacing automatically.

3.3.1.2   Write, Erase 3 Inch Gap and Write File Mark

The Erase 3 Inch Gap command can be performed by itself or combined with the Write or Write File Mark commands to cause a 3 inch gap to be erased prior to writing the record or file mark. A write command can be performed in the Edit mode (if the record to be replaced has first been backspaced over in the Edit mode to position the head correctly) to replace a record with an equal length record of updated information.

3.3.1.3   Rewind and Offline

The Rewind command causes the selected tape unit to rewind to Load Point (Beginning of Tape). The Formatter can optionally go "Busy" until the rewind is terminated (to provide a means of interrupting the computer upon termination of the operation) or not.

The Offline command never sets the Formatter to the "Busy" state and may be sent to a selected tape unit even if the tape unit is "Not Ready" because it is performing a rewind operation.

3.3.1.4   Clear

The Clear command can be utilized to clear the status register and set the Formatter to initial conditions even if the Formatter is "Busy". After the clear command is generated, the Formatter will return to the "Not Busy" status.

3.3.2 .   Command and Mode Combinations

The list of possible commands executable by the Formatter, depends on the "mode" lines and are listed in table 3-1.

The Command signals are strobed into a command storage register in the Formatter by the Command Clock (STROBEC) hence can be changed immediately after the termination of the STROBEC pulse. The MODE lines must be held static throughout each operation as no storage is provided in the Formatter.

TABLE 3-1 COMMAND & MODE COMBINATIONS

FORMATTER OPERATION	REV	WCC	WFM	GAP	FSR	RCC	CLR	REW	OFL	GEN ODD PARITY	HI DENSITY	THR1	THR2	EDIT	TRD	STOP SPACE	CD
1. Test Read Forward						X				1	1	2	3		X		5
2. Read Forward						X				1	1	2	3				5
3. Read Reverse	X					X				1	1	2	3				5
4. Write 1 Record (normal)		X								1	1						
5. Write 1 Record (Edit)		X								1	1			X			
6. Space Forward 1 record					X					1	1	2	3				5
7. Space Forward "n" records					X					1	1	2	3			4	5
8. Space Reverse 1 record	X									1	1	2	3				5
9. Space Reverse "n" records	X									1	1	2	3			4	5
10. Space Reverse (Edit mode)	X									1	1	2	3	X			5
11. Write File Mark			X							1	1			6			5
12. Erase 3 Inch Gap				X													
13. Erase 3" then Write File Mark			X	X													
14. Erase 3" then Write 1 record		X		X						1	1						
15. Rewind								X									
16. Off-line									X								
17. Initiate Rewind then Offline								X	X								
18. Clear							X										

SEE NEXT PAGE FOR NOTES 1-6

NOTE 1   The GEN ODD PARITY and HI DENSITY mode lines are ignored
          for 9 track tape units or if the MANUAL mode is selected
          so that the front panel over-ride switches can be used.
          If the REMOTE mode is selected at the front panel and a 7
          track tape unit is selected, the GEN ODD PARITY line
          controls whether odd or even parity is written or checked
          for. The HI DENSITY line controls the written character
          packing density and the period of time allowed between
          read strobes in the Read Clock Activity Sensor Circuits.

NOTE 2   The THR1 mode (Read Threshold High) has no effect except
          when reading with single stack head (read/write) tape units
          equipped with this feature allows for marginal checking of
          written records by backspacing then marginal checking during
          a read or space forward operation.

NOTE 3   The THR2 mode (Read Threshold Low) has no effect unless the
          selected tape unit is equipped with this feature. Allows
          recovery of low amplitude data from poor quality tapes.

NOTE 4   The STOP SPACE signal is used only for continuous spacing
          over multiple records. The DBY signal can be used by the
          Computer Adaptor to count records to determine when the
          required number of records has been traversed.

NOTE 5   The CD signal (Core Dump) is ignored in 7 track but can be
          used to write 7 track type file marks and to check for 7
          track file marks on a 9 track tape unit, i.e., an octal 17
          with even parity is written (and decoded as a file mark when
          reading) instead of the normal octal 23 with odd parity.

          This provides compatibility with some existing computer
          manufacturer's software.

NOTE 6   The Edit mode can be used to rewrite a file mark if the
           file mark is first backspaced over in the Edit mode.

3.4   STATE FLOW

           Figure 3-2 illustrates the State Counts that the Formatter
sequences through in simplified form.   Figure 3-3 illustrates the State
Flow in detail.

3.4.1   Simplified State Flow (See Figure 3-2)

           The Formatter is in the "Rest" State 0 at initial conditions.
The strobe C command clock is rejected if the command is not a "valid"
one.   If CBUSY is not set by a valid command then the command must be:

           1. Offline
           2. Rewind (with no interrupt)
In this event, the command is executed but the Formatter remains in State 0.

           If CBUSY is set then a rewind or clear command causes the
Formatter to enter State 7 until the rewinding status signal is false at
which time CBUSY is cleared and State 0 is re-entered. For a clear com-
mand (since the rewind status bit never is true) CBUSY is cleared almost
immediately.

           Any other command causes one of the two Predelay States to
be entered.   State 1 is normally used but State 2 is used when the For-
matter is at BOT or a 3 inch Gap Command is executed.   The appropriate
motion signal (SFC for forward motion, SRC for reverse motion) is activated
at this time.

           The predelays are utilized to erase a 3 inch gap or part of the
IRG when writing and to allow sufficient time for the tape unit to get"up
to speed".
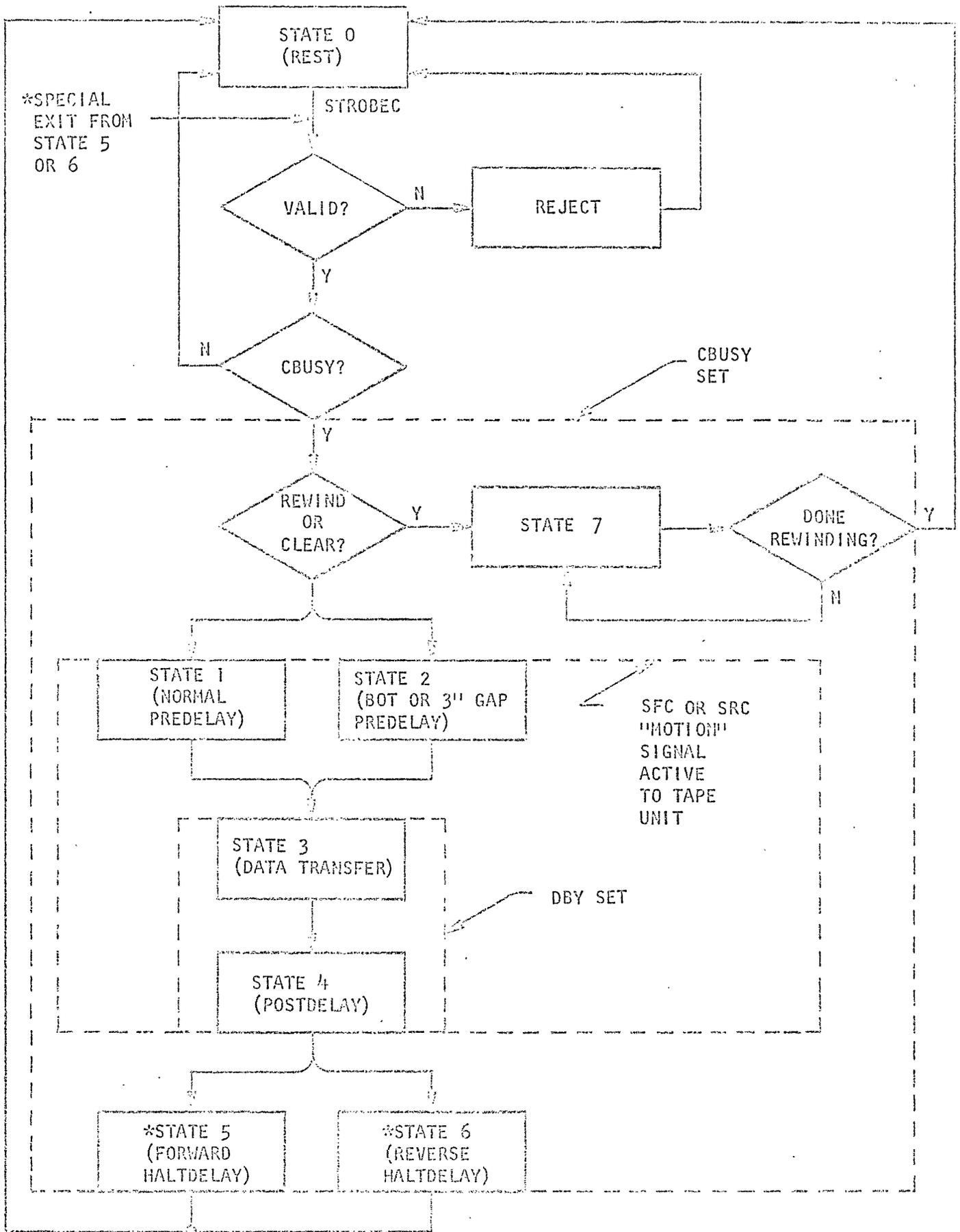
Figure 3-2. Simplified State Flow

The State 3 data transfer then takes place. For writing, the data is written until the HALT signal from the Computer Adaptor terminates the record. For "Erase" no data transfer is needed so State 3 is terminated immediately and State 4 is entered. For "Write File Mark" no data transfer actually occurs but the Formatter writes the file mark and the LRC character and then enters State 4.

For dual gap (read-after-write) tape units, the transition from State 3 to State 4 is delayed until the read head detects the end of the record (the beginning of the IRG) to allow the full record to be checked for no parity errors. State 4 Postdelay (in conjunction with the .2 inch distance the tape moves after the motion command terminates) is utilized to erase the first part of the IRG.

For Reading or Spacing operation, State 3 is maintained until the end of the record and the IRG is reached. For reading, the Computer Adaptor HALT signal terminates actual data exchange. For reading or spacing, the State 4 Postdelay (in conjunction with the fixed .2 inch distance the tape moves when halting after the motion command terminates) is utilized to position the head in the correct position in the IRG to allow for a subsequent write or read operation.

Note that the Data Busy (DBY) signal is active only during States 3 and 4 while the "motion" signals to the tape unit is active from the beginning of the Predelay State through the Postdelay State.

After the Postdelay occurs, one of the forward/reverse HALT delay (State 5 or 6) is entered (to insure that the tape is allowed sufficient time to come to a halt in the IRG.

At the termination of the Halt Delay signal CBUSY is cleared (to signal the computer that the next command can now be executed) and the Rest State 0 is entered.

The "Special Exit" from State 5 or 6 allows continuous writing or reading without stopping in the inter-record gap to optimize data transfer effeciency.

Since the Start/Stop characteristics of the tape units are "ramp" like, the gap traverse time is twice as long (as it would be at full speed) when the next command is delayed until the tape has completely halted.

This "special exit" allows a write or read command to terminate the Halt delay State and initiate the Predelay State without getting "rejected" even though the CBUSY signal is active.

In any other State, with CBUSY active, a command (other than clear) is rejected.

The computer can accomplish "on-the-fly" writing or reading by initiating the next command when DBY terminates at the end of State 4 rather than waiting until CBUSY terminates.

However, there are certain restrictions on this type of operation:

1. The next command must not switch from a write or write file mark to a space or read (or vice versa).
2. The next command must not switch direction of motion.
3. The next command must not be a rewind or offline if the previous one was a write, or write file mark type.

It is the computer program's responsibility to make sure these restrictions are followed.

The Delay Counter is utilized in States 1, 2, 4, 5 and 6 to generate the prescribed delay times.
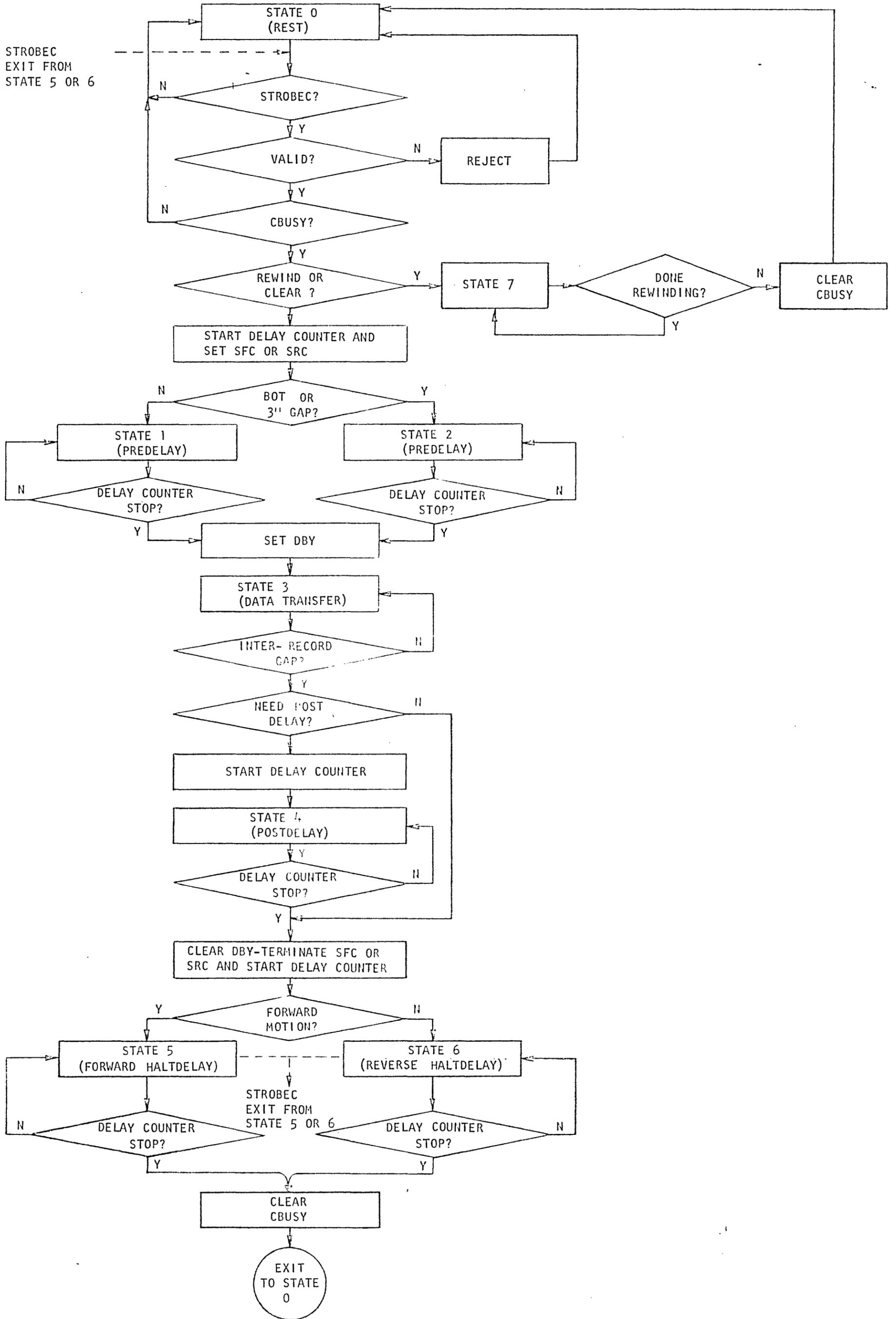
Figure 3-3. Detailed State Flow

3.4.2.   Detailed State Flow (See Figure 3-3)

The Detailed State Flow chart shows the control over signals DBY, CBUSY and the motion commands SFC, SRC as well as the use of the Delay Counter. Otherwise the flow chart is like figure 3-2.

In addition, the IRG detection exit from State 3 is detailed as is the detour around State 4 Postdelay (to achieve minimum Postdelay) in certain cases.

3.5   COMMAND EXECUTION AND TIMING

The main commands are discussed step-by-step and an illustrative timing diagrm is included for each command.

The main commands are:

1. Clear
2. Rewind (with interrupt)
3. Write file mark (7 track)
4. Write file mark (9 track)
5. Forward Space 1 record
6. Back space 1 record
7. Write 1 record (7 track)
8. Write 1 record (9 track)
9. Read 1 record (7 track)
10. Read 1 record (9 track)
11. Erase 3 inch gap.

3.5.1   Clear

The Clear function will terminate any motion command and reset the Formatter to initial conditions. CBUSY will set and then reset after the Clear command is complete to signify that the Formatter is ready for the next command.

6 - SET CLR

6 - STROBE C

2 - VLD

3 - SRS

6 - C̄ B̄ŪS̄Ȳ*
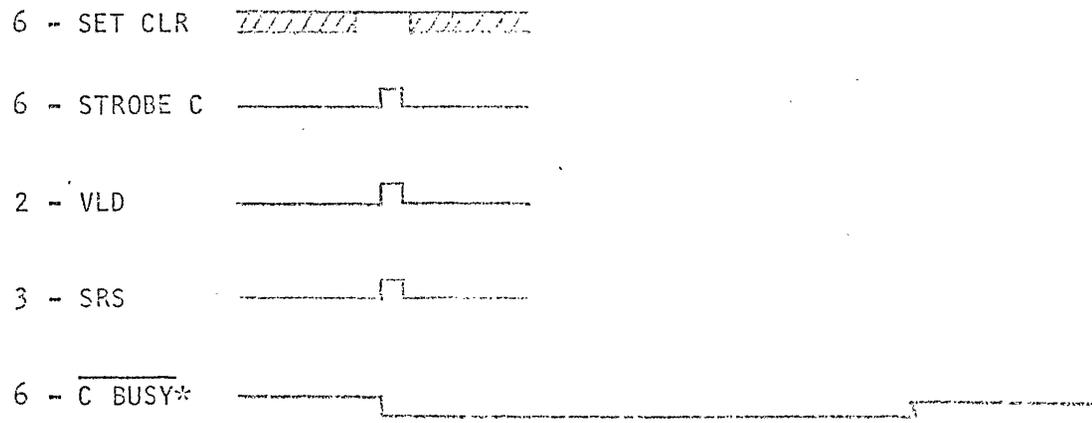
Figure 3.5.1. "Clear" Timing Diagram

The Clear command is included mainly to allow diagnostic programs control over a faulty Formatter that doesn't halt the tape unit. This command must <u>not</u> be used to halt any write or read operation since the head will not be halted at the correct point in the IRG and the CRC/LRC characters won't be written or read.

The System Reset 3-SRS pulse resets the Status register.

3.5.2   Rewind (With Interrupt)

The offline command doesn't set CBUSY and neither does the Rewind command if the Rewind Interrupt (see option 3.7.7) is jumpered out. In this event, the commands are passed on to the selected tape unit as a pulse.

If jumper E1 to E2 is in on the main Formatter board (assy. #76135) then CBUSY is set for a rewind command and resets when the rewind command is completed to signal the computer that the next command can be accepted by the tape unit.

Figure 3.5.2 illustrates the timing.

When the computer adapter generates the 6-STROBEC pulse while 6-SETREW is high and the Formatter isn't busy, the command is accepted and the 2-VLD pulse is generated.

The 3-REW flip-flop is set to store the rewind command. When the 6-STROBEC clock pulse terminates, the rewind command is generated to the selected tape unit (signal 3-$\overline{RWC}$). When the tape unit responds that it is rewinding (signal 7-REWINDING) the 3-REW flip-flop is reset and the Formatter 6-$\overline{RWDG}$ status bit is set. The tape unit goes "not ready" (7-$\overline{RDY}$) during a rewind. Since the tape unit rewind terminates before the tape unit returns to load point and becomes "Ready" again, the 6-$\overline{RWDG}$ status bit is interlocked to wait until the tape unit <u>goes</u> ready (7-$\overline{RDY}$).
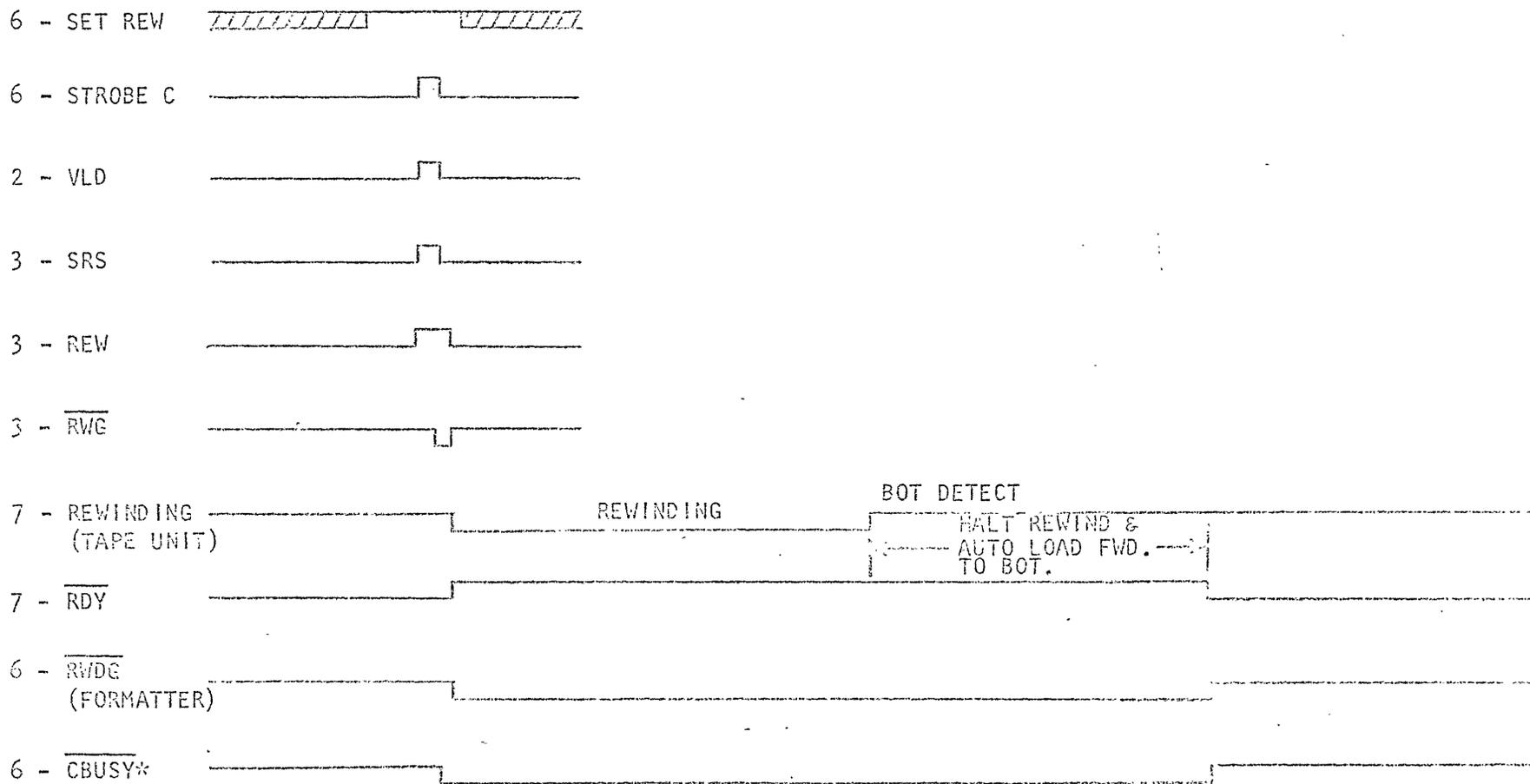
Figure 3.5.2. Rewind Timing Diagram

The 3-SRS (system visit) pulse clears the status register.

At this time 6-CBUSY* resets to signal that the operation is complete.

3.5.3 Write File Mark (7 Track)

When signal 6-SET WFM is high during the 6-STROBE C clock pulse, the 3-WFM command registerflip-flop is set to initiate a write-file-mark command. The 2-SRS pulse is also generated to reset the Formatter to initial conditions. The 3-CBUSY flip-flop is set by the 2-VLD clock, and the 7-$\overline{SFC}$ command is activated to start the tape moving in the forward direction. The selected tape unit write amplifiers are enabled as the 7-$\overline{WARS}$* signal is high. Command register flip-flop 3-WFM also sets the selected tape transport unit to the write mode via signal 7-$\overline{SWS}$. The Predelay signal delays writing of the file mark character until the tape transport unit is up-to-speed and has generated a portion of the required inter-record gap. If the tape transport unit is at the beginning of tape when the write file mark instruction is generated, the Predelay is longer to cause a 3-inch gap to be erased before the file mark is written. The enable write data request flip-flop (9-EWDR) is set upon the termination of the Predelay signal. The write data clock flip-flop (9-WDCL) is set one write clock period later and is gated to set the enable blank character counter (9-EBCC) flip-flop. The 9-EWDR flip-flop is immediately reset, which causes flip-flop 9-WDCL to be reset one write clock period later. Thus, only one write data strobe is generated to the selected tape transport unit. The command register flip-flop 3-WFM gates the file mark code onto the write data bus.

The blank character counter (comprised of flip-flops 9-CC1, 9-CC2 and 9-CC4) begin counting from the occurrence of the write file mark clock to cause the 9-WARS flip-flop to be set to reset the tape unit write amplifier flip-flops to cause the LRC character to be written. The tape transport unit continues running in the forward direction until the file mark passes under the read head so that the file mark and LRCC character can be checked for vertical parity and longitudinal parity. The time interval

3-30
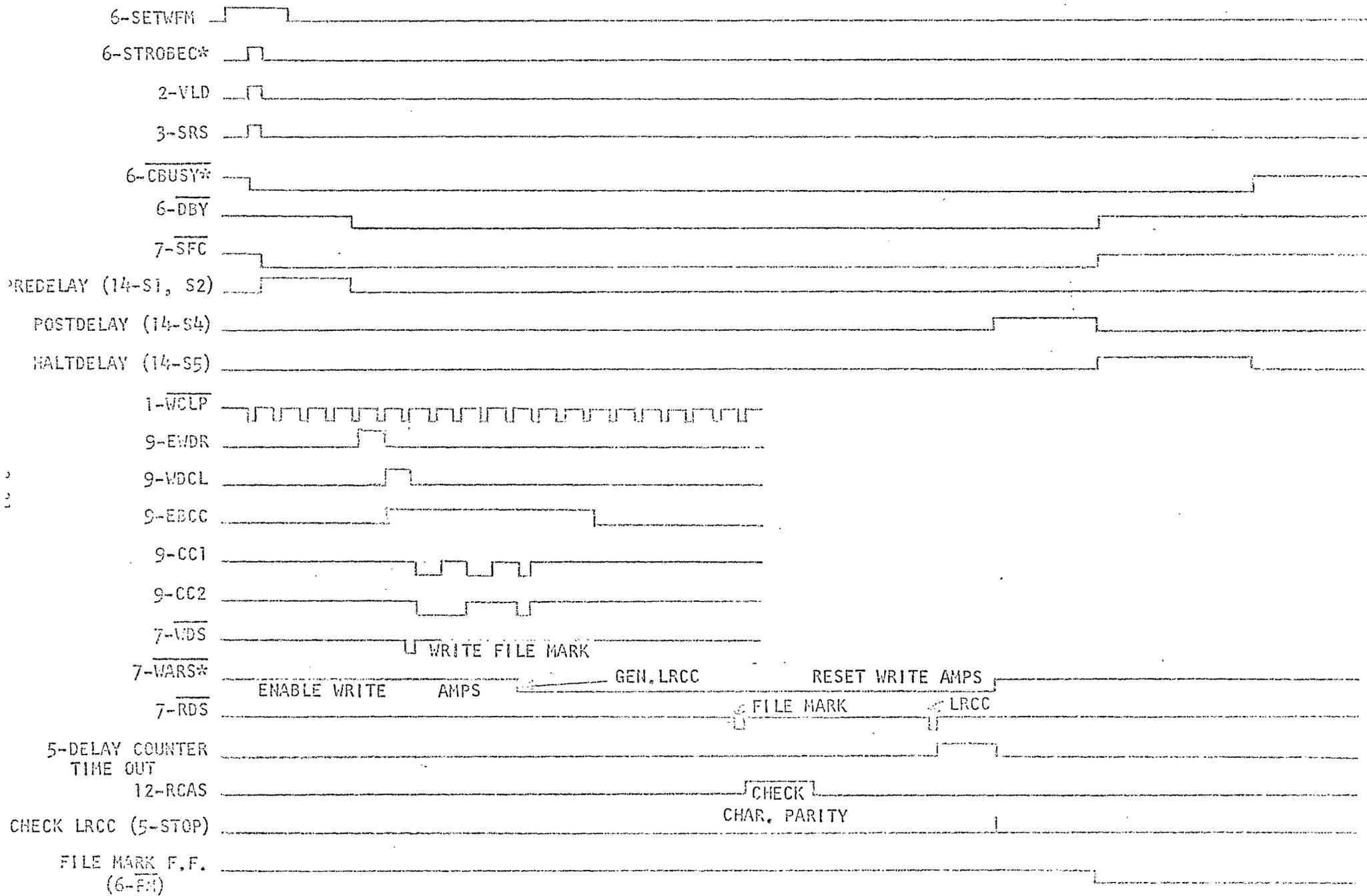
Figure 3.5.3. Write File Mark Timing Diagram (7-Track Mode)

in milliseconds, between writing the file mark and reading back the file mark character, is equal to 150 divided by the tape speed in inches-per-second. As the timing diagram illustrates, the read data strobe (7-$\overline{\text{RDS}}$) will occur, and 8 character times later (for 9-track), the LRC character read strobe will occur. The LRC character occurs 4 character times later for 7-track. The read clock activity sensor (12-RCAS) is set upon detection of the first 7-$\overline{\text{RDS}}$ pulse and times out 2 or 3 clock periods later. While the 12-RCAS circuit is active, the character parity is checked.

The Delay Counter is reset by each read strobe and then times out a delay interval after the last read strobe. Thus, the Delay Counter performs the task of IRG detection. Upon termination of the Delay Counter time out, the 5-STOP pulse is generated and utilized to check for an LRCC error in the previous record. The 5-STOP pulse is also utilized to trigger the state 4 Post Delay circuits (14-S4). When the Post Delay terminates the 7-$\overline{\text{SFC}}$ signal is terminated, and the State 5_Halt Delay is entered. The Halt Delay insures that the tape transport unit is guaranteed to have ceased all motion in the inter-record gap. If the next command is to be a write type command, then the IRG can be erased "on the fly" at full tape speed (without stopping in the IRG) by issuing the command after the signal 6-$\overline{\text{DBY}}$ terminates rather than waiting until 6-$\overline{\text{CBUSY}}$ terminates. Status is valid after the 6-DBY signal terminates, hence the status can be checked before issuance of the next command.

3.5.4   Write File Mark (9 Track)

Writing a File Mark in 9 track mode is similar to the 7 track mode except that 8 character times separate the file mark and the LRC character. Note that there is effectively an "all zeros" CRC characters since for data records the CRCC occurs at the 4th character time then 4 character times later the LRCC is written.

3.5.5   Forward Space/Record

When term 6-SET FSR is high with the 6-STROBEC, the 7-$\overline{\text{SFC}}$
signal is activated to move tape forward. The 2-VLD and 3-SRS pulses are
generated to reset the formatter and initiate the space forward operation.

NOTE   The Space Forward Command results in spacing over ONE record
if signal 6-STOP SPACE is "open circuit" or at the High level.
If multiple records are to be spaced over, 6-STOP SPACE must
be held low until the leading edge of signal 6-$\overline{\text{DBY}}$ occurs for
the last record. The signal 6-$\overline{\text{DBY}}$ may be used to count records to
determine when the last record to be spaced over is reached, but
the leading edge should be used to provide control over signal
STOP SPACE as indicated. The 6-$\overline{\text{FM}}$ status signal and 6-$\overline{\text{EOTS}}$
status signal may also be utilized to switch STOP SPACE "high"
so that a file mark or the end of tape will halt the multiple
record spacing operation.

Note that 6-$\overline{\text{CBUSY}}$ remains low (for multiple spacing operations)
until the final record has been passed.

The Predelay allows the tape unit to get up to speed before
allowing read strobes to be accepted. The read strobes activate the Read
Clock Activity Sensor (12-RCAS) to enable parity checks to be made while
spacing. When the record is past, the Delay Counter times out to detect
the IRG and the LRCC check is made. After the Signal 6-$\overline{\text{DBY}}$ terminates,
status can be checked and the next command can be issued (if a read or
space forward) to accomplish non-stop operation.

If no new command is issued at this time, the normal Halt
Delay sequence is entered.

6-SET FSR

6-STROBEC

7-$\overline{\text{SFC}}$

2-VLD

2-SRS

PREDELAY (14-S1)

POSTDELAY (14-S4)

HALTDELAY (14-S5)

(7-$\overline{\text{RDS}}$) READ STROBE

CRCC   LRCC

READ CLOCK ACTIVITY SENSE
(12-RCAS)

CHECK CHAR
PARITY

DELAY COUNTER TIME OUT

(5-STOP) CHECK LRCC

6-$\overline{\text{CBUSY}}$

6-$\overline{\text{DBY}}$
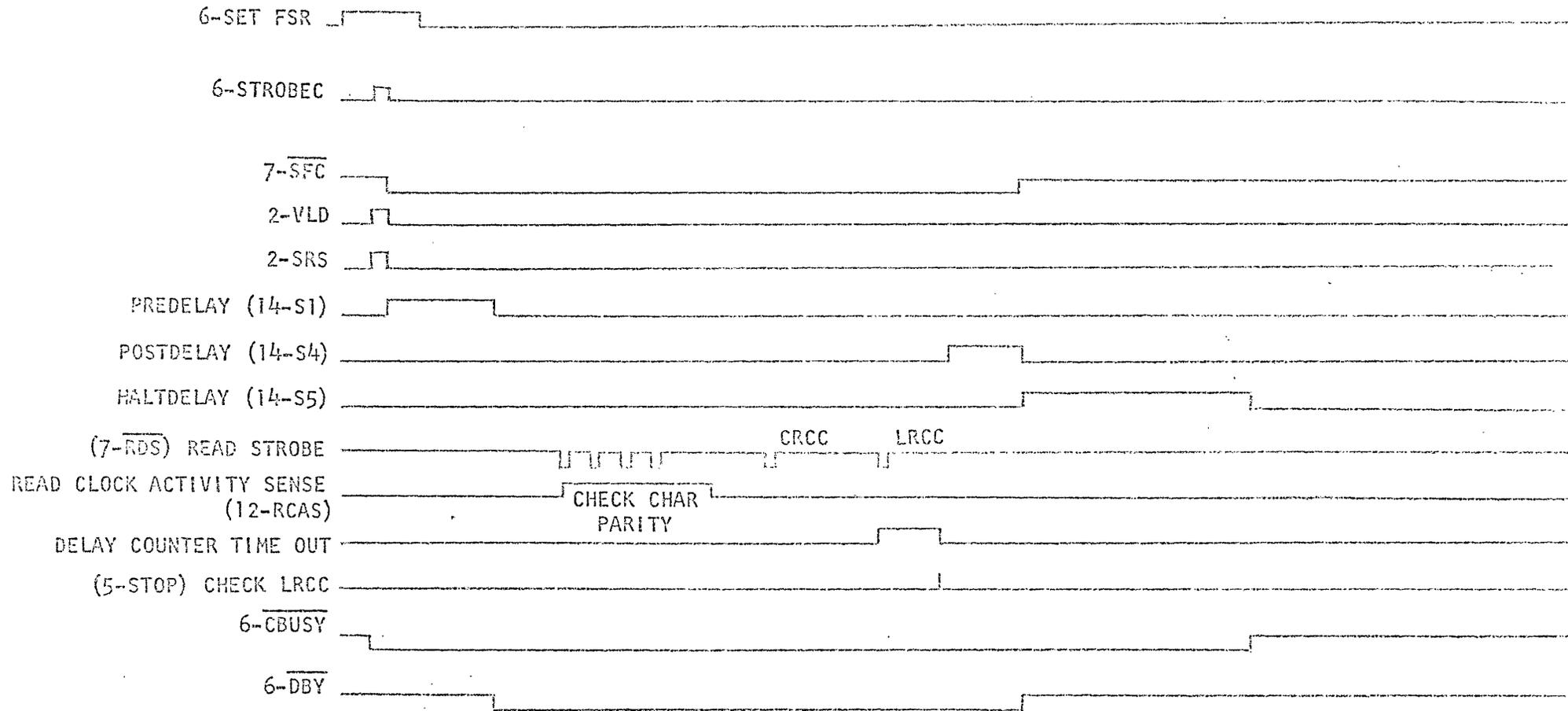
1. CRCC MAY BE MISSING FOR 9 TRACK AND IS ABSENT ON 7 TRACK.

Figure 3.5.5. Forward Space One Record Timing Diagram

3.5.6   Backspace/Record

Backspace is similar to Forward space except the LRC/CRC characters occur first.

3.5.7   Write-One-Record (7 Track)

The write-one-record instruction causes the tape transport unit to turn on the write current, enable the write amplifiers, get up to speed, generate a portion of the inter-record gap, then request output data transfers from the computer adaptor. The requested data characters are written on tape until a HALT signal is generated by the computer adaptor logic. The HALT signal terminates the record by writing the CRC character (9-track only) followed by the LRC character. The tape transport unit read-after-write head enables parity checks to be performed upon the record that has just been written. After the parity checks are completed, the tape transport unit erases a portion of the next inter-record gap and is then commanded to halt. After sufficient time has elapsed to ensure that the tape has completely stopped moving, the completion of the write-one-record operation is signaled when 6-$\overline{\text{CBUSY}}$ terminates. "On-the-fly" generation of the IRG without signal stopping may be accomplished by checking status at the termination of signal 6-$\overline{\text{DBY}}$ and issuing the next write, erase or write file mark command immediately. The write mode is set by the command clock (2-VLD) to initiate the write-one-record instruction. The system reset pulse (3-SRS) is also generated by the valid command clock to reset the tape transport controller to initial conditions. The controller busy flip-flop (6-$\overline{\text{CBUSY}}$) is set by the command clock to initiate the write-one-record instruction. The synchronous forward signal (7-$\overline{\text{SFC}}$) is sent to the tape unit to initiate forward motion.

After the Predelay (14-S1, S2) times out, the enable write data request flip-flop (9-EWDR) is clocked set to begin the writing of the record. The Predelay erases the last portion of the inter-record gap as

6-SETWCC

6-STROBEC

2-VLD

3-SRS

6-$\overline{CBUSY}$

6-$\overline{DBY}$

7-$\overline{SFC}$

PREDELAY
(14-S1, S2)

POSTDELAY (14-S4)

HALTDELAY (14-S5)

1-$\overline{WCLP}$

9-EWDR

9-WDCL

12-DATA FLAG

6-$\overline{WRMSB}$

6-$\overline{W/RACK}$

6-HALT

9-EBCC

9-CC1

9-CC2

7-$\overline{WDS}$

7-$\overline{WARSW}$ (ENABLES WRITE AMPS TO TRIGGER   GEN. LRCC   (RESETS WRITE AMPS)
FROM WRITE STROBE

7-$\overline{RDS}$ LRCC

5-DELAY COUNTER
TIME OUT

12-RCAS   CHECK CHAR.
PARITY

5-STOP
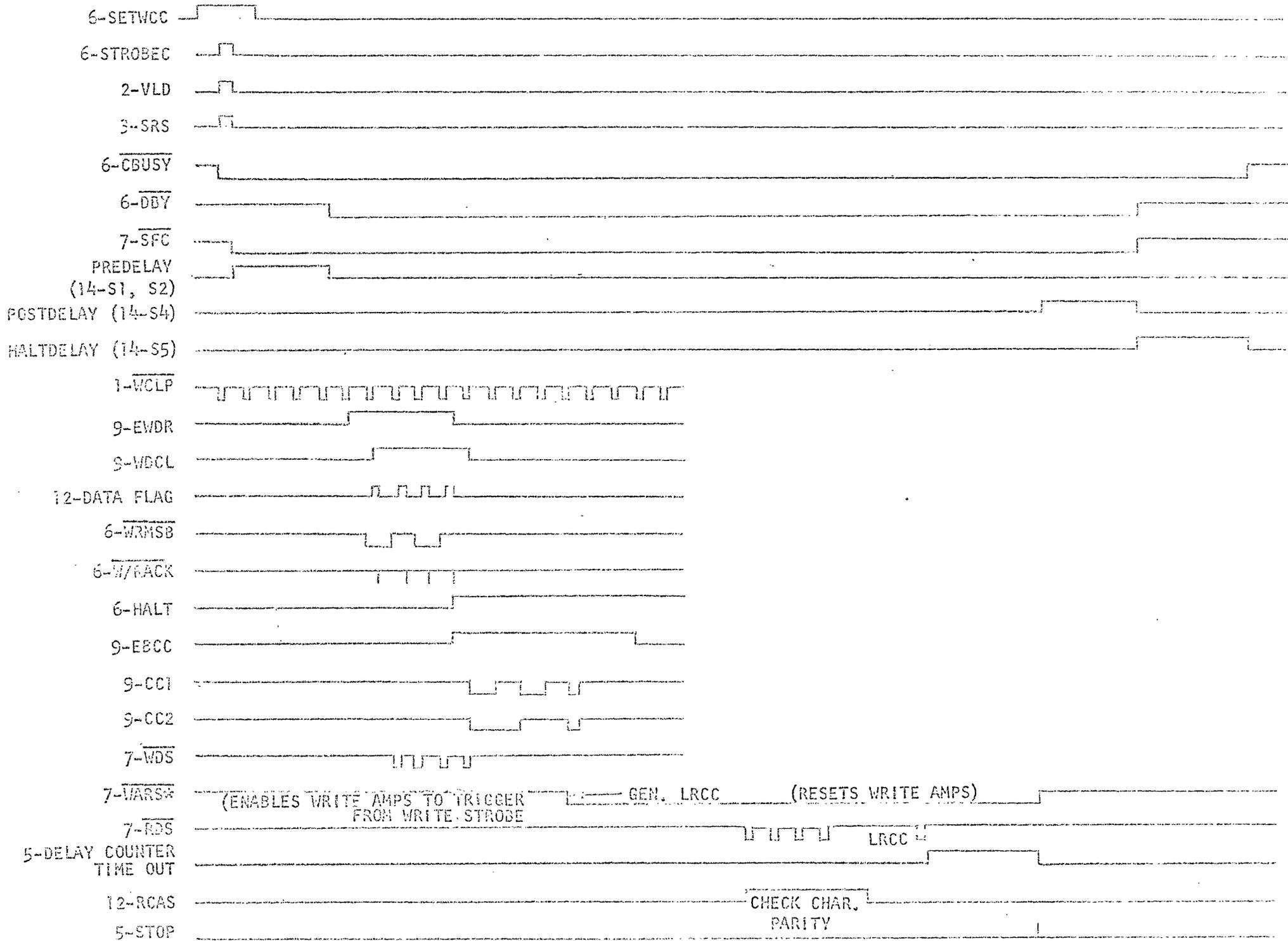
the write current is on for this period. The write data clock flip-flop (9-WDCL) is clocked set one clock time after the 9-EDWR flip-flop to enable write strobes to be generated to the tape unit.

The first Data Flag signal is sent to the computer adaptor. When the Computer Adaptor has the first character ready to transfer it generates the 6-W/$\overline{\text{RACK}}$ pulse which stores the first output character in the Formatter Write Data Register and clears the Data Flag. The first write data strobe (7-$\overline{\text{WDS}}$) is then generated by the next write clock pulse (1-$\overline{\text{WCLP}}$) in order to clock the character stored in the write data storage register onto the magnetic tape. At the trailing edge of the write data strobe, the Data Flag is set to request the next character from the Computer Adaptor.

The write data strobe (7-$\overline{\text{WDS}}$) is OR'ed with an extra CRC clock generation signal to clock the CRC generator register on logic diagram 15, to begin calculation of the CRC character. The CRC generator register is initially reset. The CRC generator register then monitors the write data output bus to generate a check character that is unique for the data characters written on tape.

If the output data character is not transferred to the tape controller before the next write data strobe is to occur, a "timing error" status bit will be set. The sequence of Data Flag-W/R ACK-Write Strobe continues until the HALT signal is generated by the Computer Adaptor to terminate the writing. The HALT signal sets the enable-blank-character-counter (9-EBCC) flip-flop. Flip-flop 9-EBCC enables the Blank Character Counter (CC1, 2, 4), disables the write control flip-flops, and resets the write most significant Byte (WRMSB) flip-flop.

The Blank Character Counter controls the generation of the CRC and LRC characters to generate the end of the record.

The character counter is decoded in the 9-track mode to create an extra CRC clock and to gate the contents of the CRC generator onto the write data bus. The character counter is also decoded in order to set the 9-WARS flip-flop to reset the write amplifiers via signals 7-$\overline{\text{WARS}}$ (in order to generate the LRC character).

The tape transport unit continues motion in the forward direction so that the read-after-write head can check parity of the entire record. The read clocks (7-$\overline{\text{RDS}}$) trigger the read clock activity sensor circuit (12-RCAS), which defines the characters that are to be checked for vertical parity. Two or three clock periods after the last character in the record, the 12-RCAS signal terminates and vertical parity checking is disabled. The Delay Counter times out after the LRC character is detected at the end of the record to provide detection of the IRG. The 5-STOP pulse is then utilized to check for an LRC error. The Post Delay time out interval ensures that a sufficient portion of inter-record gap is erased in the forward direction after a record is written such that the tape transport unit can start in the reverse direction and get up to speed for a backspace read. At the end of the Post Delay, the synchronous forward command terminates, and the Halt Delay begins timing out to ensure that the tape has come to a complete halt before the 6-$\overline{\text{CBUSY}}$ signal terminates.

For continuous writing (no stopping in the IRG) the status can be inspected after 6-$\overline{\text{DBY}}$ signal terminates and a write, erase or write file mark command can be issued immediately.

3.5.8   Write/Record (9 Track)

Writing in 9 track mode is similar to 7 track except that there is a Cyclic Redundancy Check Character (CRCC) written 4 character times after the end of the record followed by the Longitudinal Redundancy Check Character (LRCC) 4 more character times later.

3.5.9   Read One Record (7 Track)

The read one record command is initiated when signal 6-SET RCC
is high and the 6-STROBEC pulse occurs. The valid command pulse (2-VLD)
clocks the 3-RCC flip-flop set in the command register. The system reset
pulse (3-SRS) is generated by the 2-VLD clock to reset the Formatter to
initial conditions. The synchronous forward command (7-$\overline{SFC}$) and the
6-$\overline{CBUSY}$ signal are activated at the same time. After a Predelay interval
(to allow the tape to get "up to speed") read strobes are enabled to the
read logic. The first read strobe that occurs sets the data gate flip-
flop (12-DGATE) and triggers the read clock activity sensor (12-RCAS).
The trailing edge of the first read strobe sets the first character
detect flip-flop (12-1st CH), which, in turn, disables any further read
strobes from setting the 12-DGATE flip-flop. When the end of the record
is reached, the 12-RCAS circuit times out two or three character times
later, resetting the 12-DGATE flip-flop if the computer hasn't terminated
data transfer (via the HALT signal) already.

During the interval when the 12-DGATE flip-flop is set, the
data transfer takes place. During the time that 12-RCAS is set the charac-
ters are checked for parity. The CRC/LRC characters are not checked for
parity. If the HALT signal occurs before the end of the record, the 12-
DGATE flip-flop is reset to terminate Data Flag requests. (The dashed
line signals annotated with Note 1 illustrate that if the HALT signal is
missing, the 5th tape character shown on the timing diagram is input to the
computer and the 12-DGATE flip-flop does not reset until the 12-RCAS
circuit times out at the end of the record. The dashed waveforms annotated
with Note 2 indicate that the Data Flag operates for the CRC and LRC
characters when the record is read in the test read mode.) The test read
mode is provided so that the CRC/LRC characters can be read into the com-
puter for diagnostic purposes. Regardless of whether the read one record
instruction is terminated by a HALT or not, the tape continues motion until
the inter-record gap is reached, at which time Delay Counter begins timing
out. When the IRG is indicated by the Delay Counter time out, the LRC

6-SETRCC

6-STROBEC

2-VLD

3-SRS

FORWARD COMMAND
7-SFC

PREDELAY

POSTDELAY (14-S4)

HALTDELAY (14-S5)

6-RSTROBE

9-DATA FLAG

6-W/RACK

6-HALT

READ CLOCK ACTIVITY
SENSE (12-RCAS)

FIRST CHARACTER
DETECT (12-1st CH.)

DATA GATE (12-DGATE)

5-DELAY COUNTER
TIME OUT

CHECK LRCC (5-STOP)

(6-CBUSY)

DATA BUSY (6-DBY)

LRCC

CHECK CHAR.
PARITY

3-40
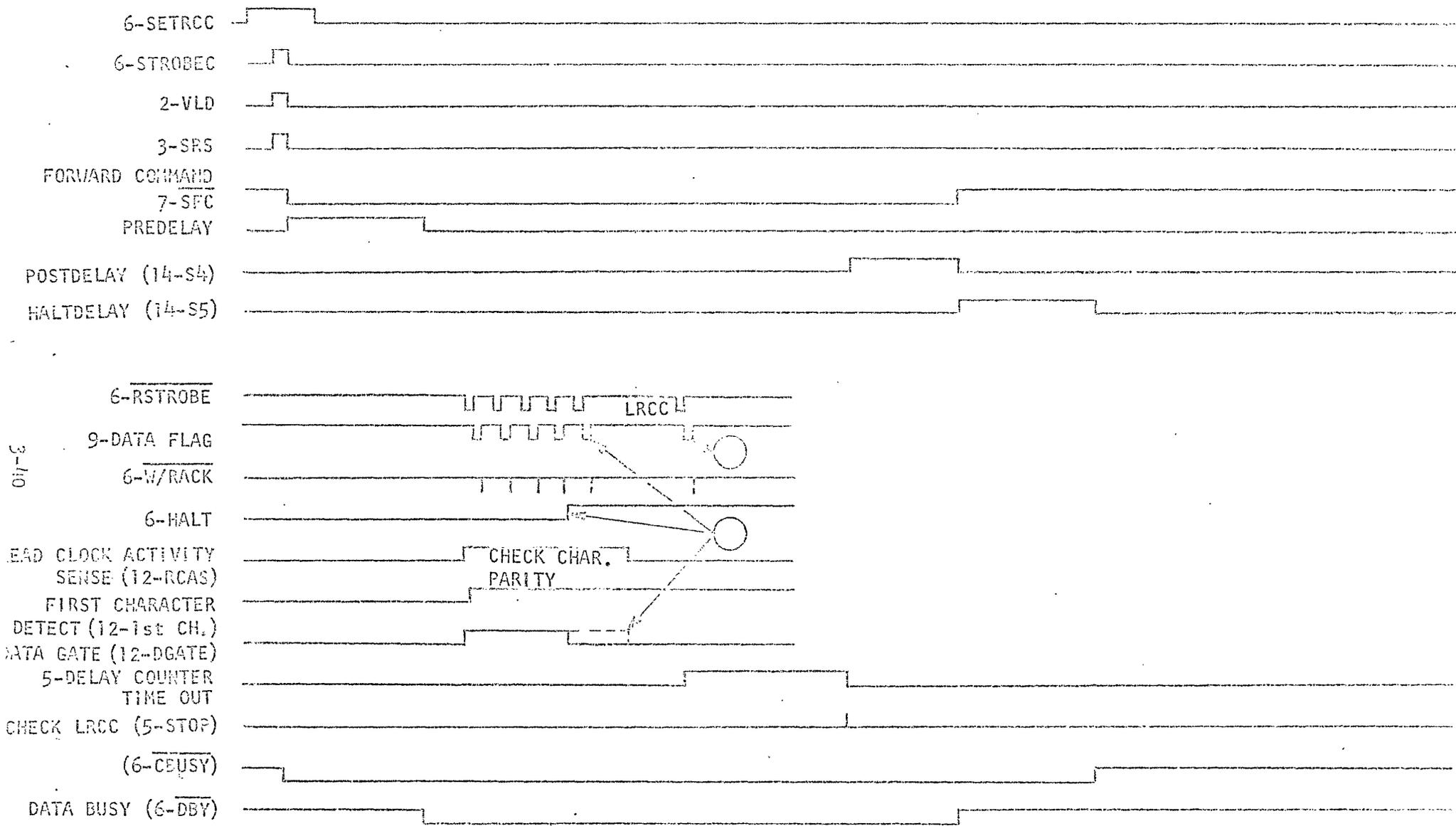
NOTES

2. IF "TEST READ MODE", THE DATA FLAG ALSO OPERATES
FOR THE LRC CHARACTER TO INPUT IT TO THE COMPUTER.

1. IF "HALT" DOESN'T OCCUR BEFORE END OF RECORD, THE
DATA GATE WILL REMAIN SET AND THE DATA FLAG WILL
CONTINUE OPERATION.

Figure 3.5.9. Read One Record Timing Diagram (7-Track Mode)

check logic is strobed by the 5-STOP pulse and causes the parity error status flip-flop to set if an LRC error exists. The Post Delay interval is then entered (14-S4) at the end of which the 7-$\overline{\text{SFC}}$ Synchronous Forward Command is terminated to the tape unit. The halt delay (14-S5) then begins timing out to delay reset of the 6-$\overline{\text{CBUSY}}$ signal until the tape transport unit is guaranteed to have halted all motion. If continuous read (no stopping in the IRG) is desired then the termination of signal 6-$\overline{\text{DBY}}$ can be utilized to signal that status is ready to be checked so that, if the next command is a read or space (in the same direction) it can be issued immediately.

The data transfer signals sequence is:

1. Pulse 6-$\overline{\text{RSTROBE}}$ indicates read data is being stored in the Formatter Read Data Register. The read data will be settled by the end of the pulse. At the trailing edge of the pulse, the Data Flag is set.

2. When the 6-$\overline{\text{DATA FLAG}}$ signal goes low, a data transfer is requested.

3. After the computer has accepted the data, pulse 6-$\overline{\text{W/RACK}}$ must be issued to clear the Data Flag.

4. The 6-HALT signal (or the detection of the IRG) resets 12-DATA GATE to terminate transfer requests. 6-HALT should be presented with the last 6-$\overline{\text{W/RACK}}$ pulse (or shortly thereafter).

The 6-$\overline{\text{DATA FLAG}}$ signal reset has a "built in" delay from the 6-$\overline{\text{W/RACK}}$ pulse such that the 6-$\overline{\text{DATA FLAG}}$ signal can be gated to form the 6-$\overline{\text{W/RACK}}$ pulse, when designing a computer adaptor that "Packs" 2 tape characters into one computer word. Normally a pulse from the computer is utilized to generate the 6-$\overline{\text{W/RACK}}$ signal.

The leading edge of the 6-$\overline{\text{RSTROBE}}$ pulse may be used to toggle a binary flip-flop on the computer adaptor to determine whether the tape character is an "odd" or "even" one for "Packing" purposes. By using the leading edge, the toggle flip-flop can be gated with 6-$\overline{\text{DATA FLAG}}$ to form the 6-$\overline{\text{W/RACK}}$ pulse on the odd characters while storing the odd characters in a computer adaptor register.

The toggle flip-flop can then be checked at pulse 6-$\overline{\text{CKWDCNT}}$ time to detect an odd number of characters in the record (to "force" a data transfer to the computer for the extra "odd" character since "Packing" logic normally expects an even number of characters so that a data transfer to the computer normally occurs after every even character).

3.5.10   Read One Record (9 Track)

Similar to Reading 7 track except there can be a CRC character as well as a LRC character. The CRC character can be "all zeros" but there is always a LRC character.

3.5.11   Erase 3 Inch Gap

The erase 3 inch Gap timing is similar to the Write File mark timing except 14-S2 generates the Predelay and no writing occurs.

3.6   CONTINUOUS WRITE OR READ

Continuous Write allows the IRG to be generated at full rated tape speed. If successive write commands are based upon the termination of the CBUSY command (as is normal) then the tape comes to a full stop in the IRG.

Similarly, continuous read (or space) allows the IRG to be traversed at full rated tape speed.

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This mode of operation optimizes the usage of the tape units by minimizing the amount of "dead time" where in data transfer cannot take place in the IRG. In order to obtain continuous "on-the-fly" operation, the DBY signal may be used (instead of the CBUSY signal) as long as certain restrictions are met:

1. The next command may not switch from a read to a write mode (or vice versa).

2. The next command may not switch tape direction.

3. A rewind or offline command may not follow a write or write file mark command.

A write or write file mark command can follow a write or write fie mark command as soon as signal DBY terminates rather than waiting until signal DBY terminates.

Similarly, a read or space forwards command can follow the same type command upon termination of DBY.

A read or space reverse command can follow the same type command upon termination of DBY.

3.7   OPTIONS

The following field changeable options are provided for in the Formatter:

1. Selection of tape speed.

2. Selection of 7 track dual density pair.

3. Definition of which tape units are single stack (read/write) and which ones are dual stack (read-after-write).

4. BCD 10 to zero conversion (when reading 7 track tapes
    in even parity mode).

5. 7 track file mark code write and read on 9 track tape units.

6. No interrupt for Rewind command.

7. Formatter Address Select

8. No Parity Error with file mark.

3.7.1   Tape Speed

The tape speed selection option provides control over the
"Speed Clock" and the "Write Clock" divider chains that operate from the
crystal oscillators. There can be two different tape speeds selected.
The selection is accomplished by controlling the division modulo of a
flip-flop divider chain by loading the negative 2's complement of the
desired (divisor-1) whereupon the counter counts up to zero to recycle.

Chip position F5 on card assembly number 76134 is provided
as a plug-in wire wrap socket for this purpose. Input Pins 1, 2, 3 and 4
represent the four tape units A, B, C and D respectively. All tape units
at speed #1 must have their "input" pins bussed together (call this
BUS #1) and all tape units at speed #2 must have their input pins bussed
together (call this BUS #2).

Bus #1 must then be jumpered to Field #1 pins 5, 6, 7, 8 and 9
as indicated in table 3-7 to obtain the desired division ratio. Similarly,
Bus #2 must be jumpered to Field #2 pins 11, 12, 13, 14, and 15 as indicated
in table 3-7 to obtain the second desired division ratio.

All pins in Fields #1 and #3 remaining must be jumpered to pin 16
to disable them. Note in the table that column 5 gives the frequency of
the "Speed Clock" utilized by the delay counter for time interval calculation.
Note also that columns 6, 7 and 8 give the write clock frequency for the
standard tape speeds dependent on the bit packing density of the selected
tape unit.

TABLE 3-7 TAPE SPEED SELECTION

Col 1	Col 2	Col 3	Col 4					Col 5	Col 6	Col 7	Col 8
Tape Speed	Division Ratio	NEG. 2's Complement	16 / 9 / 15	8 / 8 / 14	4 / 7 / 13	2 / 6 / 12	1 / 5 / 11 ← BINARY BIT WT. / FIELD #1 PINS (F5) / FIELD #2 PINS (F5)	SPDCLK FREQ KHz (PIN D5-11)	WRITE CLOCK FREQ, KHz (PIN D5-5)		
									800 BPI	556 BPI	200 BPI
112.5	2	-1	0	1	1	1	1	22.5	90	62.55	22.5
75	3	-2	0	1	1	1	0	15	60	41.7	15
56.25	4	-3	0	1	1	0	1				
45	5	-4	0	1	1	0	0	9	36	25.02	9
37.5	6	-5	0	1	0	1	1	7.5	30	20.85	7.5
32.14	7	-6	0	1	0	1	0				
28.125	8	-7	0	1	0	0	1				
25	9	-8	0	1	0	0	0	5	20	13.9	5
22.5	10	-9	0	0	1	1	1				
20.45	11	-10	0	0	1	1	0				
18.75	12	-11	0	0	1	0	1				
17.3	13	-12	0	0	1	0	0				
16.07	14	-13	0	0	0	1	1				
15.0	15	-14	0	0	0	1	0				
14.06	16	-15	0	0	0	0	1				
13.23	17	-16	0	0	0	0	0				
12.5	18	-17	1	1	1	1	1	2.5	10	6.95	2.5
11.84	19	-18	1	1	1	1	0				
11.25	20	-19	1	1	1	0	1				
10.7	21	-20	1	1	1	0	0				
10.22	22	-21	1	1	0	1	1				
9.7	23	-22	1	1	0	1	0				
9.38	24	-23	1	1	0	0	1				
9.0	25	-24	1	1	0	0	0				
8.6	26	-25	1	0	1	1	1				
8.3	27	-26	1	0	1	1	0				
8.03	28	-27	1	0	1	0	1				
7.77	29	-28	1	0	1	0	0				
7.5	30	-29	1	0	0	1	1				
7.2	31	-30	1	0	0	1	0				
7.03	32	-31	1	0	0	0	1				

NOTES:

1. In Col 4, pins marked "0" must be jumpered to Bus #1 or #2, pins marked "1" must be jumpered to Pin F5-16 to enable.

2. Standard tape speeds are underlined

F5
PIN

TERM

1 — A ⎫
2 — B ⎬ INPUT TAPE UNITS
3 — C ⎪
4 — D ⎭

5 — 1 ⎫
6 — 2 ⎪
7 — 4 ⎬ FIELD #1
8 — 8 ⎪
9 — 16 ⎭

10 — NOT USED

11 — 1 ⎫
12 — 2 ⎪
13 — 4 ⎬ FIELD #2
14 — 8 ⎪
15 — 16 ⎭

16 — DISABLE

BUS NO. 1

ENABLE
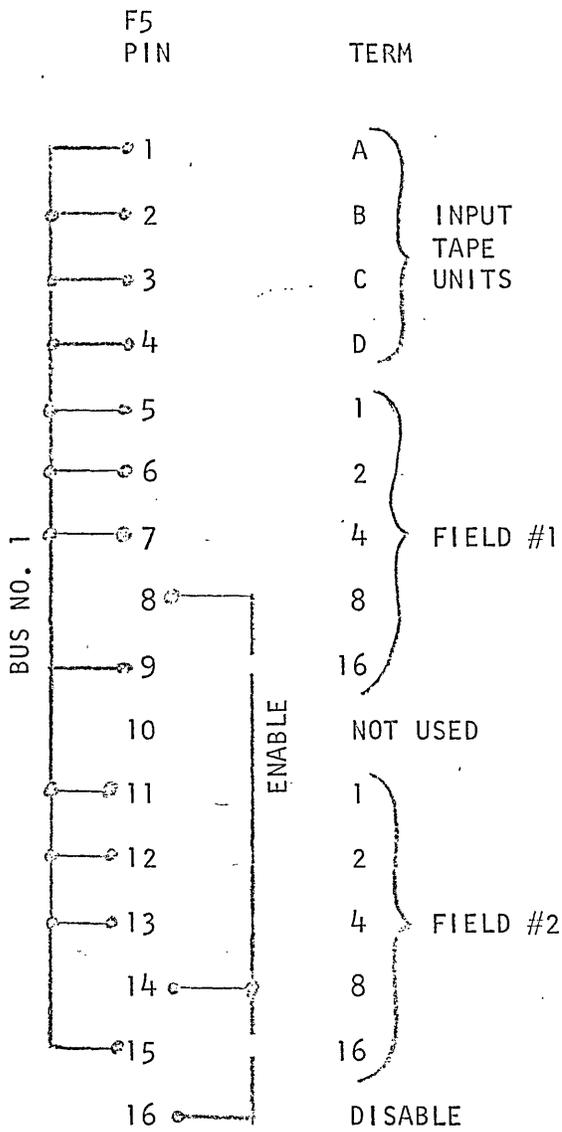
EXAMPLE #1 - ALL TAPE UNITS 25 ips

F5
PIN

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16

BUS NO. 1

BUS NO. 2

ENABLE
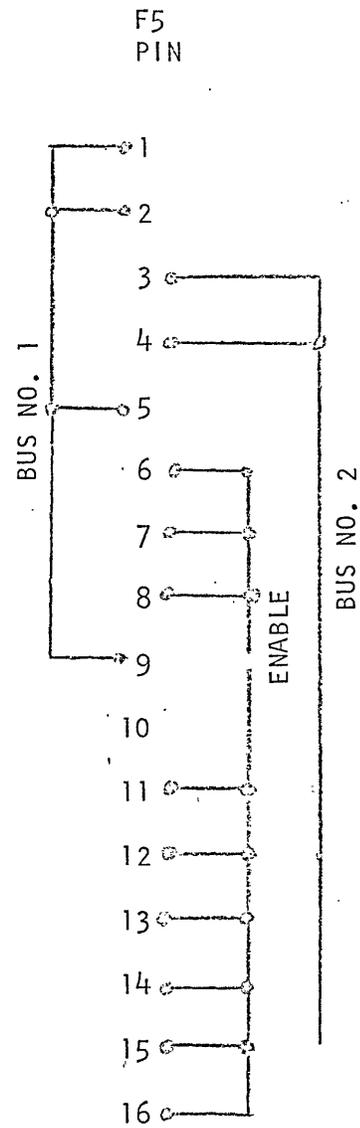
EXAMPLE #2 - TAPE UNITS A, B ARE
75 ips

TAPE UNITS C, D ARE
12.5 ips

FIG. 3-8   EXAMPLE TAPE SPEED SELECTION

Figure 3-8 illustrates two examples of jumper wiring of socket F5 to achieve the desired tape speeds.

3.7.2   Dual Densities

The Formatter is configured to operate at 800 BPI with no jumpers in the Density Field on card 76134 or when a 9 track tape unit is selected. Different pairs of densities can be selected for different tape units, i.e., tape unit A can be 800/556, B = 556/200, C = 800/200 etc.

The "H" pin for each 7 track tape unit must be jumpered to the "556" bus if the higher density of the pair is 556BPI. The H pin can be ignored if the higher density is 800.

The "L" pin for each 7 track tape unit must be jumpered to the "556" or the "200" bus depending on what the lower density is of the pair.

Figure 3-9 is an example of the wiring for the following configuration:

        TAPE UNIT A = 9 Track 800 BPI
        TAPE UNIT B = 7 Track 800/556 BPI
        TAPE UNIT C = 7 Track 556/200 BPI
        TAPE UNIT D = 7 Track 800/200 BPI
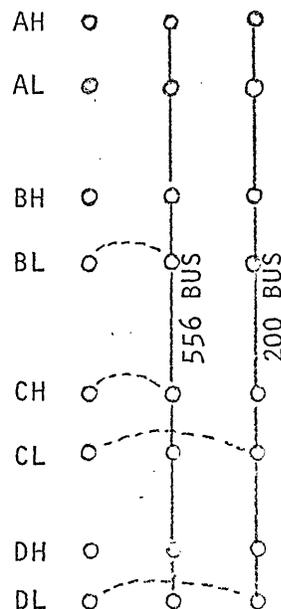
FIG 3-9   DENSITY SELECTION

3.7.3 Single/Dual Stack Head Selection

The formatter is configured so that if no jumpers are used in the SS/DS Head Selection Field then Dual Stack (read-after-write) is assumed.

Jumpers must be used only for the tape units A, B, C or D that are single stack head units.

The SS/DS Head Selection Field is located on the main board assembly number 76135 near chip position G7. Bus "E3" must be jumpered to points A, B, C or D for single stack tape units A, B, C or D.

3.7.4 BCD 10 to Zero Converter

The Formatter is configured to convert BCD 10 (Octal 12) to zero when reading 7 track tapes in the even parity mode if no jumper is inserted between E4 and E5 on the main board assembly number 76135 (near position K12).

Insertion of the jumper causes the BCD 10 to be read without conversion to the computer adaptor. The BCD 10 code is equivalent to a 1 bit on lines $\overline{R4}$ and $\overline{R6}$ with $\overline{R2}$, $\overline{R3}$, $\overline{R5}$, $\overline{R7}$ and $\overline{RP}$ all 0 bits.

The all zeros code is automatically converted to the BCD 10 code when writing on a 7 track tape unit in the even parity mode so that there will be at least one track with a 1 bit in it to generate a read strobe when reading back. Therefore, the BCD 10 code is FORBIDDEN as an industry standard when writing on 7 track tapes in the even parity mode unless the program is constructed to handle the following items.

A) Conversion of BCD 10's written to zero upon reading (no jumper).

B) Conversion of zero written to BCD 10 upon reading (with jumper).

3.7.5   7 Track File Mark Code Write/Read on 9 Track Unit

The Formatter is configured to write/read normal (Octal 23) file marks with 9 track tape units when no jumper is installed between E8 and E9 near position K12 on the main board assembly 76135.

With the jumper installed, an octal 17 file mark is written and checked for ("dummy" 7 track code) to provide compatibility with existing computer manufacturer's software.

3.7.6   NO Parity Error for File Marks

The Formatter is configured to indicate a parity error when reading a 7 track file mark in the odd parity mode or a "dummy" 7 track file mark on a 9 track unit (with no jumper installed between E6 and E7).

With the jumper installed (located near K10 on main board, assembly #76135) the parity error indication is disabled.

3.7.7   Rewind Interrupt

The Formatter is configured to set CBUSY when the rewind command is issued if no jumper is present between E1 and E2. CBUSY resets when the rewind is complete to provide a signal to the computer to indicate that the next command can be accepted.

If jumper E1 to E2 (next to position G7) is present, CBUSY will not set for a rewind command.

3.7.8 . Formatter Address Select

The Formatter is configured to always be selected if no jumper is placed in the Formatter Address Select area near F4 (E10, E11 and E12). Thus, if a single Formatter is utilized, no jumper need be used.

Table 3.7.8 illustrates the jumper connection required for the two addresses.

Table 3.7.8   Formatter Address Selection

Formatter Address	Signal $\overline{FAD1}$	Jumper
0	High	E11 to E12
1	Low	E10 to E12

3.8 Delay Times

There are three main delay times:

1. Predelay

2. Postdelay

3. Halt Delay

The Pre/Post delays are used to erase portions of the Inter-record gap (when writing) or to erase tape. When reading they are used to position the head correctly in the IRG so that the following record can be either a read or a write.

The Halt delay is also used to erase part of the IRG when writing and provides sufficient time to insure that the tape unit is completely stopped (after the motion signal is terminated).

There are many factors that enter into the various delays:

1. 7 track/9 track

2. Tape speed

3. Single/dual stack head

4. Forward/reverse motion

5. BOT/$\overline{BOT}$

6. Write/read command

7. EDIT/$\overline{EDIT}$ mode.

Table 3-9 through 3-13 give the delay times for a 9 track tape unit selected at the standard speeds of 75, 45, 37.5, 25, and 12.5 ips. Tables 3-14 through 3-18 give the same information for 7 track.

Table 3-9. NINE TRACK PRE/POST DELAYS (75 ips)

		PREDELAY			Time Interval Milliseconds	POSTDELAY		Time Interval Millisecor
		FROM		TO		FROM	TO	
		Signal	Pin	Signal	Pin			
Single Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	3.66	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	1.67
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	12.0	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	1.67
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	3.66	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	0
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	3.66	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	.33
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	53.6	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	2.66
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	5.66	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	2.66
Dual Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	3.66	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	0
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	12.0	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	0
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	3.66	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	1.67
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	3.66	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	2.33
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	53.6	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	.33
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	5.66	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	.33

HALTDELAY		
FROM	TO	
$\overline{DBY}$(1) J101-65	CBUSY(1) J101-94	5.66

NOTES

3. (transition) = 0 means from +5V to 0V, = 1 means from 0V to +5V

2. Write   = Write 1 record or write file mark

1. Read   = Read 1 record or space

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		PREDELAY				Time Interval Milliseconds	POSTDELAY		Time Interval Millisecond
		FROM		TO			FROM	TO.	
		Signal	Pin	Signal	Pin				
Single Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65		$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65		$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65		$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65		$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65		$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65		$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	
Dual Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65		$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65		$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65		$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65		$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65		$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65		$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	

HALTDELAY	
FROM	TO
$\overline{DBY}$(1) J101-65	CBUSY(1) J101-94

NOTES

3. (transition) = 0 means from +5V to 0V, = 1 means from 0V to +5V

2. Write   = Write 1 record or write file mark

1. Read   = Read 1 record or space

Table 3-10. NINE TRACK PRE/POST DELAYS (45 ips)

		PREDELAY			Time Interval Milliseconds	POSTDELAY		Time Interval Milliseconds
		FROM		TO		FROM	TO	
		Signal	Pin	Signal	Pin			
Single Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	6.08	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	2.78
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	19.9	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	2.78
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	6.08	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	0
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	6.08	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	.54
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	89.0	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	4.4
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	9.4	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	4.4
Dual Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	6.08	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	0
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	19.9	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	0
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	6.08	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	2.78
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	6.08	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	3.86
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	89.0	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	.54
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	9.4	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	.54

HALTDELAY		
FROM	TO	
$\overline{DBY}$(1) J101-65	CBUSY(1) J101-94	9.4

NOTES

3. (transition) = 0 means from +5V to 0V, = 1 means from 0V to +5V

2. Write   = Write 1 record or write file mark

1. Read   = Read 1 record or space

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Table 3-11. NINE TRACK PRE/POST DELAYS (37.5 ips)

| | | PREDELAY | | | Time Interval Milliseconds | POSTDELAY | | Time Interval Millisecon |
| | | FROM | | TO | | FROM | TO | |
		Signal	Pin	Signal	Pin				
Single Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	7.3	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	3.34
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	24.0	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	3.34
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	7.3	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	0
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	7.3	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	.66
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	107.3	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	5.3
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	11.3	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	5.3
Dual Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	7.3	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	0
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	24.0	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	0
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	7.3	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	3.34
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	7.3	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	4.64
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	107.3	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	.66
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	11.3	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	.66

| HALTDELAY | | |
FROM	TO	
$\overline{DBY}$(1) J101-65	CBUSY(1) J101-94	11.3

NOTES

3. (transition) = 0 means from +5V to 0V, = 1 means from 0V to +5V

2. Write = Write 1 record or write file mark

1. Read = Read 1 record or space

Table 3-12. NINE TRACK PRE/POST DELAYS (25 ips)

		PREDELAY			Time Interval Milliseconds	POSTDELAY		Time Interval Milliseconds
		FROM		TO		FROM	TO	
		Signal	Pin	Signal	Pin			
Single Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	11	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	5
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	36	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	5
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	11	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	0
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	11	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	1
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	161	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	8
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	17	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	8
Dual Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	11	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	0
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	36	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	0
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	11	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	5
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	11	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	7
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	161	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	1
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	17	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	1

HALTDELAY		
FROM	TO	
$\overline{DBY}$(1) J101-65	CBUSY(1) J101-94	17

NOTES

3. (transition) = 0 means from +5V to 0V, = 1 means from 0V to +5V

2. Write   = Write 1 record or write file mark

1. Read   = Read 1 record or space

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Table 3-13. NINE TRACK PRE/POST DELAYS (12.5 ips)

| | PREDELAY | | | | Time Interval Milliseconds | POSTDELAY | | Time Interval Millisec |
| | FROM | | TO | | | FROM | TO | |
	Signal	Pin	Signal	Pin				
Single Stack Head								
Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	22	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	10
Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	72	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	10
Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	22	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	0
Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	22	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	2
Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	322	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	16
Write	STROBEC(0)	J101-5	DBY(0)	J101-65	34	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	16
Dual Stack Head								
Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	22	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	0
Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	72	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	0
Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	22	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	10
Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	22	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	14
Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	322	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	2
Write	STROBEC(0)	J101-5	DBY(0)	J101-65	34	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	2

| HALTDELAY | | |
FROM	TO	
$\overline{DBY}$(1) J101-65	CBUSY(1) J101-94	34

NOTES

3. (transition) = 0 means from +5V to 0V, = 1 means from 0V to +5V

2. Write = Write 1 record or write file mark

1. Read = Read 1 record or space

Table 3-14. SEVEN TRACK PRE/POST DELAYS (75 ips)

		PREDELAY			Time Interval Milliseconds	POSTDELAY		Time Interval Milliseconds
		FROM		TO			FROM	TO	
		Signal	Pin	Signal	Pin		FROM	TO	
Single Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	3.66	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	3.63
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	12.0	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	3.63
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	3.66	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	0
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	3.66	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	.33
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	53.6	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	4.62
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	5.66	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	4.62
Dual Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	3.66	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	1.67
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	12.0	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	1.67
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	3.66	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	1.67
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	3.66	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	2.33
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	53.6	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	2.33
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	5.66	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	2.33

HALTDELAY		
FROM	TO	
$\overline{DBY}$(1)　　　J101-65	CBUSY(1) J101-94	5.66

NOTES

3. (transition) = 0 means from +5V to 0V, = 1 means from 0V to +5V

2. Write = Write 1 record or write file mark

1. Read = Read 1 record or space

Table 3-15. SEVEN TRACK PRE/POST DELAYS (45 ips)

		PREDELAY				Time Interval Milliseconds	POSTDELAY			Time interva Milliseco
		FROM		TO			FROM		TO	
		Signal	Pin	Signal	Pin					
Single Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	6.08	$\overline{S3}$(1) Cathode CR4		$\overline{DBY}$(1) J101-65	6.0
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	19.9	$\overline{S3}$(1) Cathode CR4		$\overline{DBY}$(1) J101-65	6.0
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	6.08	$\overline{S3}$(1) Cathode CR4		$\overline{DBY}$(1) J101-65	0
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	6.08	$\overline{S3}$(1) Cathode CR4		$\overline{DBY}$(1) J101-65	.54
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	89.0	$\overline{S3}$(1) Cathode CR4		$\overline{DBY}$(1) J101-65	7.56
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	9.4	$\overline{S3}$(1) Cathode CR4		$\overline{DBY}$(1) J101-65	7.56
Dual Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	6.08	$\overline{S3}$(1) Cathode CR4		$\overline{DBY}$(1) J101-65	2.78
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	19.9	$\overline{S3}$(1) Cathode CR4		$\overline{DBY}$(1) J101-65	2.78
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	6.08	$\overline{S3}$(1) Cathode CR4		$\overline{DBY}$(1) J101-65	2.78
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	6.08	$\overline{S3}$(1) Cathode CR4		$\overline{DBY}$(1) J101-65	3.86
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	89.0	$\overline{S3}$(1) Cathode CR4		$\overline{DBY}$(1) J101-65	3.86
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	9.4	$\overline{S3}$(1) Cathode CR4		$\overline{DBY}$(1) J101-65	3.86

HALTDELAY		
FROM	TO	
$\overline{DBY}$(1)　　J101-65	CBUSY(1) J101-94	9.4

NOTES

3. (transition) = 0 means from +5V to 0V, = 1 means from 0V to +5V

2. Write = Write 1 record or write file mark

1. Read = Read 1 record or space

Table 3-16. SEVEN TRACK PRE/POST DELAYS (37.5 ips)

		PREDELAY				Time Interval Milliseconds	POSTDELAY		Time Interval Milliseco
		FROM		TO			FROM	TO	
		Signal	Pin	Signal	Pin				
Single Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	7.3	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	7.14
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	24.0	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	7.14
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	7.3	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	0
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	7.3	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	.66
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	107.3	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	9.1
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	11.3	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	9.1
Dual Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	7.3	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	3.34
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	24.0	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	3.34
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	7.3	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	3.34
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	7.3	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	4.64
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	107.3	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	4.64
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	11.3	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	4.64

HALTDELAY		
FROM	TO	
$\overline{DBY}$(1) J101-65	CBUSY(1) J101-94	11.3

NOTES

3. (transition) = 0 means from +5V to 0V, = 1 means from 0V to +5V

2. Write   = Write 1 record or write file mark

1. Read   = Read 1 record or space

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Table 3-17. SEVEN TRACK PRE/POST DELAYS (25 ips)

		PREDELAY			Time Interval Milliseconds	POSTDELAY		Time Interval Milliseconds
		FROM		TO		FROM	TO	
		Signal	Pin	Signal	Pin			
Single Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	11	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	11
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	36	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	11
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	11	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	0
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	11	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	1
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	161	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	14
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	17	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	14
Dual Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	11	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	5
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	36	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	5
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	11	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	5
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	11	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	7
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	161	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	7
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	17	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	7

HALTDELAY		
FROM	TO	
$\overline{DBY}$(1) J101-65	CBUSY(1) J101-94	17

3. (transition) = 0 means from +5V to 0V, = 1 means from 0V to +5V

2. Write = Write 1 record or write file mark

NOTES 1. Read = Read 1 record or space

Table 3-18.   SEVEN TRACK PRE/POST DELAYS (12.5 ips)

		PREDELAY			Time Interval Milliseconds	POSTDELAY		Time Interval Milliseconds
		FROM		TO		FROM	TO	
		Signal	Pin	Signal	Pin				

		Signal	Pin	Signal	Pin	Time Interval Milliseconds	FROM	TO	Time Interval Milliseconds
Single Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	22	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	22
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	72	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	22
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	22	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	0
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	22	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	2
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	322	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	28
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	34	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	28
Dual Stack Head	Read forward	STROBEC(0)	J101-5	DBY(0)	J101-65	22	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	10
	Read forward (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	72	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	10
	Read Reverse	STROBEC(0)	J101-5	DBY(0)	J101-65	22	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	10
	Read Reverse (EDIT)	STROBEC(0)	J101-5	DBY(0)	J101-65	22	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	14
	Gap or Write (BOT)	$\overline{LDP}$(1)	J101-47	DBY(0)	J101-65	322	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	14
	Write	STROBEC(0)	J101-5	DBY(0)	J101-65	34	$\overline{S3}$(1) Cathode CR4	$\overline{DBY}$(1) J101-65	14

HALTDELAY		
FROM	TO	
$\overline{DBY}$(1) J101-65	CBUSY(1) J101-94	34

3. (transition) = 0 means from +5V to 0V, = 1 means from 0V to +5V

2. Write   = Write 1 record or write file mark

NOTES   1. Read   = Read 1 record or space