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DOUBLE DENSITY DISC CONTROLLER SYSTEM MANUAL

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THE DIGITAL GROUP

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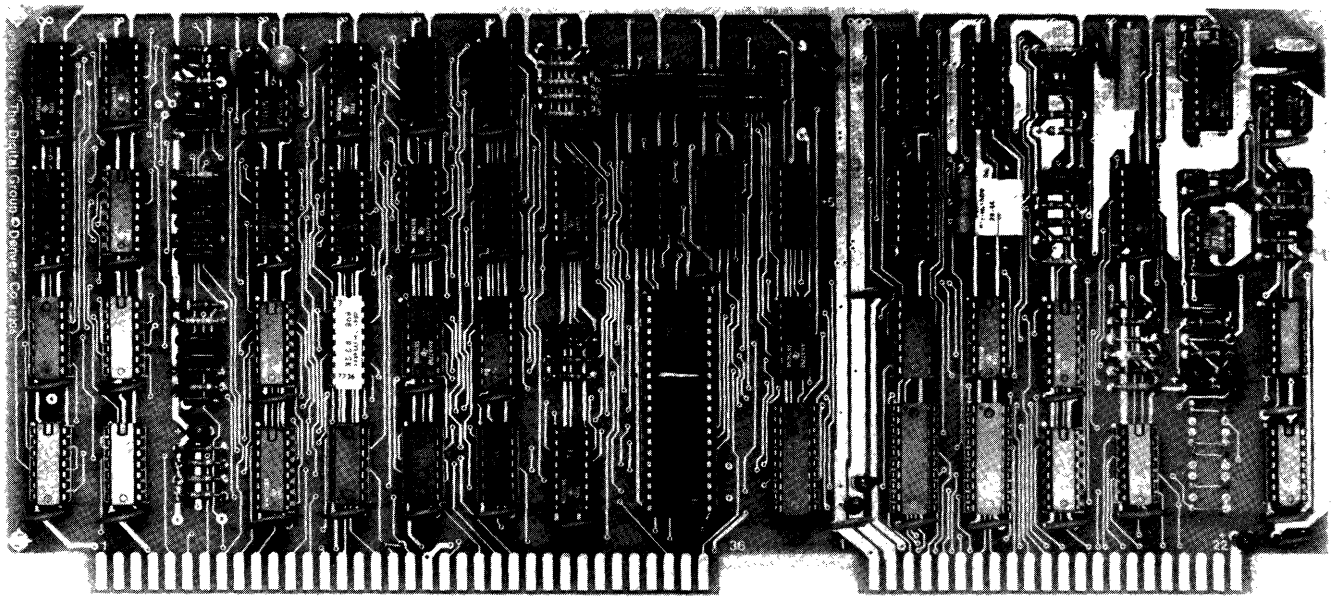
INTRODUCTION



The DIGITAL GROUP DOUBLE DENSITY CONTROLLER MANUAL is a comprehensive set of documentation that allows the user to Assemble, Test, Troubleshoot, and Install the Board in his system. Each section of the manual contains ordered concise instructions for getting the user up fast and reliably.

An Installation Manual is included for the user who bought the board assembled. All he needs to do is consult the Installation Manual for getting the board up.

For the kit builder, the Assembly and Testing sections are provided. Along with the Installation Manual, the kit builder will find the Controller board easy to build.

Also included in the documentation is the Hardware Monitor Manual and Cassette. This Monitor is very powerful in aiding the user to Test and Diagnose problems that might occur in assembly and testing. The Assembled Board purchaser might wish to perform some of the Diagnostics provided in HMON to continue to monitor the reliability of the System. You might think of the Diagnostics in HMON as a "Memory Test" for the Controller.

CHAPTER 2

ASSEMBLING THE CONTROLLER

2.1 INTRODUCTION

Estimated Construction Time: 4-8 Hours

To build the Digital Group Dual Density Floppy Card, you will need the following tools and equipment:

Fine tipped low wattage soldering iron (25 watt is ideal)
Solder 60/40 RESIN core wire solder, 20-30 gauge
DO NOT USE ACID CORE SOLDER (SEE OUR WARRANTY POLICY)
Diagonal cutters, small micro-shear preferred
Long-nosed pliers
flux remover or Alcohol
small brush

Volt-Ohmmeter (20K Ohms per VOLT or better)
15 Mhz Dual Trace Triggered Sweep Oscilloscope

Before you start to assemble the board, take a little time to inspect the P.C. board. Check to see if there are any shorts on the top side of the board under where the Integrated Circuit sockets will be placed. Once the Sockets are in place, it will be very difficult to find shorts in this area. Also, read through the entire assembly procedure before starting to familiarize yourself with the proceedure.

2.2 PRELIMINARY INSPECTION

( ) Remove all parts from their bags and plastic rails.

( ) Sort the components into individual values. (cupcake trays are good for this)

( ) Verify that all parts are there by checking them off of the PARTS LIST in APPENDIX A

( ) Remove the Parts Placement Diagram from APPENDIX I and place it conveniently in front of you.

2.3 RESISTOR INSTALLATION

NOTE: All resistors are mounted on .4 inch centers.
(If you have a lead bender, by all means use it.)

(✓) Insert the following Resistors into the board:

( )	R42	47 Ohm	(yel-vio-blk)
( )	R30,R31	120 Ohm	(brn-red-brn)
( )	R12,R13,R14	150 Ohm	(brn-grn-brn)
( )	R15,R17	150 Ohm	
( )	R22	270 Ohm	(red-vio-brn)
( )	R25	330 Ohm	(org-org-brn)

( ) Turn the board over at this time and solder in these Resistors.

(✓) Insert the following Resistors into the board:

( )	R33,R37	470 Ohm	(yel-vio-brn)
( )	R49,R50	470 Ohm	
( )	R28,R36	1k Ohm	(brn-blk-red)
( )	R38	1K Ohm	
( )	R9,R18,R19	2.2K Ohm	(red-red-red)
( )	R20,R21	2.2K Ohm	

( ) Turn the board over at this time and solder in these Resistors.

(✓) Insert the following Resistors into the board:

( )	R27,R34,R39	2.2K Ohm	(red-red-red)
( )	R7	2.7K Ohm	(red-vio-red)
( )	R44,R45	3.3K Ohm	(org-org-red)
( )	R29	3.9K Ohm	(org-whi-red)

( ) R43 4.7K Ohm (yel-vio-red)

( ) R46 5.6K Ohm (grn-blu-red)

( ) R6,R10 6.8K Ohm (blu-gry-red)

( ) R4 7.5K Ohm (vio-grn-red)

( ) R8 9.1K Ohm (whi-brn-red)

( ) Turn the board over at this time and solder in these Resistors.

(/) Insert the following Resistors into the board:

( ) R23,R24,R32 10K Ohm (brn-blk-org)

( ) R40,R41,R47 10K Ohm

( ) R48 10K Ohm

( ) R5 11K Ohm (brn-brn-org)

( ) R2 15K Ohm (brn-grn-org)

( ) R11 27K Ohm (red-vio-org)

( ) R1 33K Ohm (org-org-org)

( ) R3 820K Ohm (gry-red-yel)

( ) Turn the board over at this time and solder in these Resistors.

2.4 INTEGRATED CIRCUIT SOCKET INSTALLATION

If you received SAE sockets with your kit, DO NOT REMOVE the white strips located on the bottom of the socket.

(/) Install the following IC Sockets at this time by inserting the socket and SLIGHTLY bending two diagonally opposing corner pins outwards to hold the socket onto the board.

( ) IC3,IC9,IC22 8 Pin Socket

( ) IC50,51,52 8 Pin Socket

( ) IC53 8 Pin Socket

(✓) Turn the board over at this time and solder in the 8 Pin Sockets.

(✓) Install the following IC Sockets at this time by inserting the socket and SLIGHTLY bending two diagonally opposing corner pins outwards to hold the socket onto the board.

( ) IC2,IC5,IC6,IC7 14 Pin Socket

( ) IC14,IC15,IC16 14 Pin Socket

( ) IC17,IC18,IC19 14 Pin Socket

( ) IC20,IC21,IC23 14 Pin Socket

( ) IC24,IC27,IC30 14 Pin Socket

( ) IC31,IC32,IC34 14 Pin Socket

( ) IC35,IC36,IC38 14 Pin Socket

( ) IC39,IC40,IC46 14 Pin Socket

( ) IC48,49 14 Pin Socket

( ) Turn the board over at this time and solder in the 14 Pin Sockets.

(✓) Install the following IC Sockets at this time by inserting the socket and SLIGHTLY bending two diagonally opposing corner pins outwards to hold the socket onto the board.

( ) IC1,IC4,IC8 16 Pin Sockets

( ) IC10,IC11,IC12 16 Pin Sockets

( ) IC13,IC25,IC26 16 Pin Sockets

( ) IC28,IC33,IC37 16 Pin Sockets

( ) IC41,IC45 16 Pin Sockets

( ) Turn the board over at this time and solder in the 16 Pin Sockets.

(✓) Install the following IC Sockets at this time by inserting the socket and SLIGHTLY bending two diagonally opposing corner pins outwards to hold the socket onto the board.

( ) IC42,IC43,IC44 20 Pin Sockets

NOTE: No 20 Pin Socket will be installed in IC Position 47.

( ) IC29 40 Pin Socket

(✓) Turn the board over at this time and solder in the 20 and 40 Pin Sockets.

2.5 CAPACITOR INSTALLATION

Insert the following Capacitors into the board and then bending the leads slightly enough to hold the Capacitor in place.

( ) Insert the following Capacitors into the board:

( ) C10,C11,C12 50pf Silver Mica

( ) C13,C14,C34 50pf Silver Mica

(✓) C53 36pf Silver Mica

(✓) C66 180pf Silver Mica (could be marked 181)

(✓) C52,C74 220pf Silver Mica (could be marked 221)

(✓) C65 680pf Silver Mica (could be marked 681)

(✓) C32,C54 1000pf Silver Mica (could be marked 102)

(✓) Turn the board over at this time and solder in these Capacitors.

(✓) Insert the following Capacitors into the board:

(✓) C70,C73 .01 Disc Ceramic

(✓) C49,C50 .01 10% Mylar

(✓) C48 .022 10% Mylar

(✓) C15 .022 10% Disc Ceramic

(✓) Turn the board over at this time and solder in these Capacitors.

( ) Insert the following Capacitors into the board. Be sure to check the Parts Placement Diagram and PC board for the correct orientation of the + end of the capacitors.

( )	C40,C42,C43	4.7uf Tantalum (Observe Polarity)
( )	C68	4.7uf Tantalum (Observe Polarity)
( )	C9,C61,C62	10uf Tantalum (Observe Polarity)
( )	C71	10uf Tantalum (Observe Polarity)
( )	C16,C39	22uf Tantalum (Observe Polarity)
( )	C72	100uf Tantalum (Observe Polarity)

( ) Turn the board over at this time and solder in these Capacitors.

( ) Insert the following Capacitors into the board:

( )	C1-C8	.1uf Disc Ceramic
( )	C17-C31	.1uf Disc Ceramic

( ) Turn the board over at this time and solder in these Capacitors.

( ) Insert the following Capacitors into the board:

( )	C33,C35-C38	.1uf Disc Ceramic
( )	C41,C44-47	.1uf Disc Ceramic
( )	C51,C55-C60	.1uf Disc Ceramic
( )	C63,C64,C67	.1uf Disc Ceramic
( )	C69,C75	.1uf Disc Ceramic

( ) Turn the board over at this time and solder in these Capacitors.

2.6 REMAINING COMPONENT INSTALLATION

( ) Insert the remaining components into the board:

( ) D1,D3,D4 1N4148 Diode (save the leads for later)

( ) D2 1N4731A Zener Diode (.5 in. Centers)

( ) L1 22uh Choke (red-red-blk) looks like 2W resistor

( ) R35 5K Ohm 10 Turn Trim-Pot

( ) X1 4.000 Mhz Crystal

( ) Turn the board over at this time and solder in the last of the components. Be sure to solder the crystal as quickly as possible to minimize heat buildup.

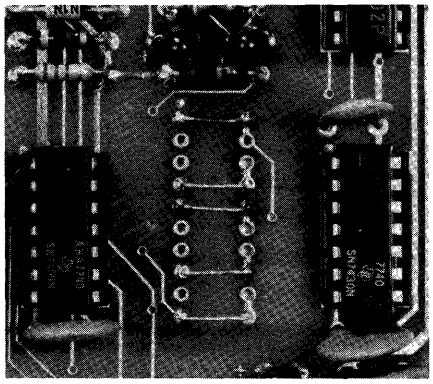
LEFT TO DO
1. (IC 48 SOCKET)
2. (6-50pf MICA C10-14 C34)
3. (L1 22uh CHOKE)
4. (D$_A$ PIN 36 WAIT LINE)

2.7 BOARD ADDRESS JUMPER INSTALLATION

( ) Using the leads saved from the 1N4148 Diodes:

( ) Form five jumper wires bent on .3 in. spacing.

( ) Install the Port Addressing jumpers into the jumper pads at IC Position 47 as follows:



( ) Pin 1 to Pin 20

( ) Pin 4 to Pin 17

( ) Pin 5 to Pin 16

( ) Pin 8 to Pin 13

( ) Pin 10 to Pin 11

( ) Solder in these jumpers and trim the excess leads.

2.8 HEAD LOAD MOTOR-ON JUMPER

If you intend to use the Disc Controller on Mini Drives with the DSM-INT1 cabling installed OR you intend to run both Mini and Standard drives with the DSS-INT1 cabling, install the following:

( ) Install a small jumper wire between the pads near the 36 Pin edge connector pins 18 and 19.

2.9 FINAL INSPECTION AND CLEANING

All components that are to be soldered onto the board have been soldered in. The only parts that should be left over at this time should be the Integrated Circuits and 7 1N4148 Diodes. These parts will be installed during testing. You should now look over your work and check for obvious shorts, solder splashes and unsoldered pins. After you are satisfied that no glaring shorts or opens exist, clean the board in commercial board cleaner or alcohol.

( ) Inspect the board for obvious solder shorts, solder splashes, and unsoldered pins.

( ) Clean the board in commercial board cleaner or alcohol.

( ) Re-inspect the board for shorts and unsoldered pins again.

( ) Be sure that all solder joints are clean and SHINY.

( ) RE-SOLDER any joints that appear dull in finish.

( ) Reclean the board if joints needed retouching.

You have completed the assembly phase of construction. Go to the Installation Manual now and perform any CPU modifications that are required. If you presently have a single density Controller (DSS-INT1 or DSM-INT1) and you have a spare slot on the I/O Bus, you should parallel the connections on Pins 34 and 36 of the 36 Pin edge connector to this spare slot. Some of the testing could be done with your old controller installed along with the new Double Density Controller. If this is the first Disc Controller to be installed in your system, perform all required cabling at this time. You don't need to parallel a slot if this is your first disc system. After you have installed all required modifications and cabling you should take a break. The next thing we will do is test the Double Density Controller. Proceed to the next chapter.

CHAPTER 3

TESTING/TROUBLESHOOTING

3.1 INTRODUCTION

The Double Density Disc Controller is not a difficult board to troubleshoot. The board was designed to be modular. The following tests check out each section to the degree that the section should work. Each test will also give the user the ability to check further into the circuitry should the test results be negative.

In general, if there is a problem in one section, the user should consult the theory of operation for that section to get a better idea as to where the problem lies.

3.2 GENERAL- POWER SUPPLIES AND CAPACITORS

Before power is applied to the disc controller board all of the power supply traces should be tested. This is to ensure that shorts or reversed Tantalum capacitors will not destroy the computers power supplies. NO integrated circuits should be installed on the disc controller board for this test.

(1). With an Ohmmeter, check the +5, +12, and -5 volt power supplies with respect to ground and the other supplies. There should be no direct shorts (resistance less than 25 Ohms) to ground or any other supply. Be sure to check these measurements by reversing the leads of the Ohmmeter.

(2). If the above test was successful, recheck the polarity of all Tantalum and Electrolytic capacitors. If there was a short between any power supply and ground or between any supply find the cause of this short before proceeding.

(3). Insert the disc controller (less Integrated Circuits) into the computer and apply power. Check to see that there are no power supply failures. Now, just leave the disc controller inserted and the power on for about five minutes. If a capacitor was installed incorrectly it will probabily fail in this time period (it's better for it to fail now rather than when all the Integrated Circuits are installed).

3.3 THE POWER-ON RESET AND LOW VOLTAGE CIRCUIT

The Power-on reset circuit will now be tested. This circuit holds the 1791 IC and the write gate inactive during power up and during a power loss. If this circuit fails to operate the controller board will not function at all. The controller board may be inserted into any I/O slot for this test.

(1). Install the following IC: IC34 (LM3302). Insert the disc controller board in the computer and apply power. Adjust the Computer +5 Volt supply for +5 Volts at the top of the Disc Controller card. The tolerance is + or - 5%. Do NOT use the extender cards for this setting.

(2). Now, place the disc controller up on extender boards if you have them. Apply power again and see if the output of IC34 pins 1 and 2 are high. If not, check the +12 volt power supply and then recheck the +5 volt supply. If the +12 volt supply failed (crow-barred) check all components associated with that supply. If the +5 volt supply was low, readjust that supply and start the test all over again. Correct polarity of diodes D1 through D4 are critical to the operation of this circuit. Check to see if these diodes are installed correctly.

(3). Observe the output of IC34 pins 1 and 2 with an oscilloscope. During powerup, IC34 pin 2 will hold low for approximately 50 milliseconds. If this level is not present, check for shorts or bad polarity of capacitor C62. Also, the LM3302 could be bad.

(4). Now with the oscilloscope in place reduce the computer +5 volt supply until IC34 pin 1 goes low. Note that this voltage should be arround 4.3 volts. If this voltage is above 4.3 volts replace Zener D2 or Diode D1. If the voltage is below 4.3 volts, check or replace the Zener D2 , or the LM3302. Retest if necessary. (above or below means 10% either way)

(5). Readjust the computer +5 Volt power supply to +5 volts as in Step 1. Now, attach one probe to the +5 Volt supply and the other to IC34 Pins 1 or 2, then cycle the AC power on and off. AC trigger the scope to when the +5 Volt supply starts to go low. Observe that the output of IC34 Pins 1 and 2 go low prior to the total loss of the +5 volt power supply. (Note that IC34 Pins 1 and 2 output goes low when the +5 Volt supply passes through 4.3 Volts.)

(6). Now, place one scope probe on the +12 Volt power supply. Place the other on the +12 Volt supply Pin 3 of IC34. Cycle the AC power again and note that the +12 Volt "storage" circuit comprised of C61, R42 and D4 remains charged after the standard +12 Volt supply discharges. then remove the scope probe from the +12 Volt supply and place it on the +5

Volt supply. Note also that while cycling the AC power the +5 Volt supply discharges to 0 while the voltage on IC34 Pin 3 is still above +5 Volts. The +5 Volt supply discharge rate is a function of the load of your particular system, but it should discharge in less than one second. If this is not the case, check the polarity of D4 and C61. Also be sure that the value of R42 is correct.

3.4 USING HMON/2 FOR TESTING

Most of the following tests will use the HMON/2 Hardware monitor for exercising the controller board. The user should read the HMON/2 Manual and familiarize himself with the operation of this monitor. HMON/2 has been used to adjust all the sections of the Dual Density Controller board. The only secton that the monitor can't diagnose is the Phase locked loop. It should be noted that using the INP-<port>:CON function, the user can generate a single repetitive pulse train that any "good" scope can sync to. These pulses occur at approximately a 10 millisecond rate. Use of the DELay function can extend these pulses to allow the user to trigger all of the timing elements on the board. In one of the sections we will use this technique to check all the controller to disc buffers and timing elements. When an example is given there will be no explanation of the command or how to terminate it. The user should read the rest of the test procedure and then go back to the HMON/2 Manual and reread the functions used exclusively for testing. Be sure that you know how to STOP any function that we will be using.

We will be reloading the HMON/2 cassette three or four times. If you presently have a Single density disc system or a Phideck system, you may want to load in HMON/2 at this time and save it on disk or cassette. The Double Density Controller board may be tested in the slot next to the intended slot for most of the tests. This can be accomplished by installing temporary motherboard jumpers from the intended slot to this new slot for both the Int and Wait lines. Remember, you can load HMON/2 through any operating system except for the last test, which requires you to connect the Double Density Controller to the actual disc drives.

3.5 BOARD SELECT AND GATING CIRCUITS

In this section we will test all of the address gating and port select logic. We will also test the wait logic here. The first test will check to see if any shorts exist in the output data enable and the wait enable lines. If there is a problem here, the computer will not function as the controller board will either interfear with the computers I/O bus or the Wait line. Should the user have dynamic memory, the holding of the Wait line will cause memory loss. We will next test the Input/Output gating logic to see if the

board can be accessed. Then, the wait logic will be tested to see if the wait timeout timer and the entire wait circuit functions properly.

(1). Install all IC's EXCEPT the following: IC8, IC9, IC22, IC29, IC37, and IC44.

(2). Insert the disc controller and apply power. Check to see that all of the power supplies are operating and that no IC is getting excessively hot to the touch.

(3). With either a scope or a voltmeter, check the following:

(a). Pins 1 and 19 of IC44 are at a constant high level.

(b). Pin 15 of IC37 is also at a constant high level.

If either of these signals is low, there is a problem in the address select or wait logic. At this point the user should start back tracking from these pins to find the source of the problem.

(4). Now remove power from the system and install IC's 37 and 44. (Be sure that the Wait jumper and Int jumper on the motherboard are in place)

(5). Read in the disc diagnostic tape using the "ZE" ROM and execute the HMON/2 with option 6.

The following tests will establish whether the address decoding and wait generation logic are functioning properly.

Most of the tests will have visual outputs to the screen. You should stop with the testing and start scoping the board when your outputs do not agree with the examples.

(6). First we will see if the board responds to the computer. Execute the following program:

```
:OUT-54,0:INP-54:OUT-54,377:INP-54 (cr)
```

The computer should respond with:

```
INPUT PORT 054 = 304
INPUT PORT 054 = 307
```

If this is the result you received, go on to step 7. If both inputs resulted in a 000, the board was not selected. Check IC's 16, 31, 33, 45. This test should have generated the strobe pulse labeled RE4 on the schematic. To aid in testing this section, re-execute the above test but place a "CON" statement at the end. This will cause the test to be repeated

at speeds a scope will sync to. If the result of the test was not 000 but something else, check the problem bits in IC's 30, 41, 42, 43 and 44.

(7). Now we'll see if the wait logic is operable. Temporarily short pins 38 and 39 of the IC29 to ground. (Jumper IC29-39 to IC29-3 and IC29-38 to IC29-20.) (Use the hookup wire supplied.) Then try the following:

```
:SET-.10000 (cr)
:OUT-57,0:NEX:MES-/DONE/ (cr)

Time the length of the second line above.(app 25 sec) Th

:SET-.10000 (cr)
:OUT-53,0:NEX:MES-/DONE/ (cr)
```

The second test should execute about 1.5 seconds faster. If this was true proceed to step 8. If the tests ran at the same speed, there is a problem with the wait logic. Check to see if the CPU mods have been installed and their associated jumpers on the motherboard are there. If this is not the problem then read the theory of operation of the wait logic and check IC's 2, 7, 15, 17, 25, 36.

(8). We apparently have some communication with the controller board at this time. Remove power and insert all the IC's EXCEPT IC29, the 1791.

3.6 DEVICE ATTRIBUTE, VCO AND CLOCK CIRCUITS

In this section we will check out the Attribute selection circuts, the Phase locked loop and the Basic 1791 clock circuit. The attribute circuit will also test some of the input/output buffer lines. Any shorts on these lines could cause problems for the 1791 IC. We will also set the free running frequency of the Phase locked loop. This adjustment is the most critical adjustment to be made and should be done carefully. Once the adjustment has been made, we will change the attributes for device 0 and check the switching of different sections of the loop. If a problem arises in this circuit, a careful examination of the rest of this circuit is in order. Finally, we will check the Basic clock frequency of the 1791 and check to see if it switches properly for each attribute.

(1). Install the controller board on its extender boards again and reload HMON/2.

(2). Get two of the 1N4148 diodes that were supplied and bend the leads to fit the .3" spaced socket.

(3). Please refer to APPENDIX C on DEVICE ATTRIBUTES for the

following:

(a). Start HMON/2 with option 6.

(b). The following program will be run for all 4 drives. This is done by replacing the word "DATA" in the OUT-54,"DATA" with the following: 0, 1, 2, 3. In each case the user should place a diode in each of the 4 possible positions for that drive and observe the results on the screen.

(c). Run the following program for each drive:

:OUT-54,DATA:INP-54:CON (cr)

The results obtained should conform to the following table:

DATA	POSITION 1	POSITION 2	POSITION 3	POSITION 4
0	300	344	324	314
1	301	345	325	315
2	302	346	326	316
3	303	347	327	317

If any of the above results were incorrect, study the data pattern for all tests and check the associated bits on the controller board.

Now we will set and check out the VCO basic free running frequency.

(2). The VCO free running frequency is set as follows:

(a). Place a diode in the Single/Double density position for device 0.

(b). Select this device by executing a OUT-54,0 (cr) instruction.

(c). Observe the clock period at IC29 Pin 26 with an oscilloscope.

(d). Adjust Pot R35 for a square wave with a period of 2 usec high and 2 usec low. Tolerance is: +5% -0%.

(e). With a voltmeter, measure the DC voltage at Pin 3 of

IC8. Make a note of this voltage on the schematic for later reference.

(3). Now we will check the operation of the loop.

(a). Remove the diode installed in the Single/Double density position for device 0. Observe that the clock period at IC29 Pin 26 just halved. (1 usec high and 1 usec low)

(b). Now install the diode in the Mini/Standard position for device 0. Observe that the period doubled to 2 usec high and 2 usec low.

(c). Install the second diode in the Single/Double density position for device 0. Observe that the clock period doubled again to 4 usec high and 4 usec low.

If any of the above observations didn't occur, back track from IC29 Pin 26 to where the problem exists.

(3). We will now test the fixed clock frequency for the 1791 IC. This is either a 1 Mhz or 2Mhz clock applied to Pin 24 of IC29.

(a). With the 2 diodes still installed from the above test, observe that the period of the clock on IC29 Pin 24 is 500 nsec high and 500 nsec low.

(b). Now remove the 2 diodes and observe that the period of the clock on Pin 24 of IC29 just halved to 250 nsec high and 250 nsec low.

If you didn't observe the 2 different periods as above, check IC's 19, 20 and 49.

3.7 TIMING ELEMENT AND DISC I/O BUFFER CIRCUITS

In the following section we will check to see that all the timing elements are operating properly. For example, if the drive change one-shot fails to function, all disc copying may fail due to improper settle time. Other timing element failures could cause: loss of input data, improper write timing, no motor startup delay or excessive wait states. We will use the strobe feature mentioned above to "fire" the timing elements and also to see if a clear path exists for other Disc I/O Buffers.

(1). For all the tests we will use the input strobe of IC29 Pin 4. Use the hookup wire supplied to form jumpers for these

tests. If any of these tests fail, trace through the logic from IC29 Pin 4 to the source of the problem. Now let's generate the repeatable strobe by executing the following:

```
OUT-54,0 (cr)
INP-50:CON (cr)
```

(2). First let's test the lines to the disc:

(a). Jumper IC29 Pins 4 and 15.

(b). Observe that the signal at IC40 Pin 5 Is the same as IC29 Pin 15.

(c). Now jumper IC29 Pins 4 and 16.

(d). Observe that the signal at IC40 Pin 2 is the same as IC29 Pin 16.

(e). Jumper IC29 Pins 4 and 28.

(f). Observe that the signal at IC39 Pin 5 is the same as the signal on IC29 Pin 28.

(g). Observe that the signal at IC38 Pin 13 is the same as the signal on IC29 Pin 28.

(h). Jumper IC29 Pins 4 and 30.

(i). Observe that the signal at IC38 Pin 2 is the same as The signal on IC29 Pin 30.

(3). Next we will test the head load delay timer. There are two ways this timer may be fired, we will test both.

(a). Reinstall the jumper from IC29 Pins 4 and 28.

(b). Stop the program presently running and type the following:

```
INP-50:DEL-.100:CON (cr)
```

(c). Observe that the negative going pulse at IC4 Pin 4 is between 35 and 45 milliseconds.

(d). Now Stop the program that is executing and type the following:

```
OUT-54,20:DEL-.100:CON (cr)
```

(e). Jumper IC29 Pins 28 and 39.

(f). Observe that the pulse on IC4 Pin 4 is the same as in (c).

(4). We will now check the wait timeout timer. ~~This may be done without the use of jumpers.~~ Jumper IC-29 pins 38 and 39 to ground.

(a). Stop the program that is presently running and type the following:

INP-57:CON (cr)

(b). Observe that there is a positive going 160 to 170 micro second pulse on IC37 PIN 13.

(5). The next timer to check out is the mini motor startup timer.

(a). Install a diode in the Mini/Standard position for device 0.

(b). Temporarily remove IC3 and jumper IC3 Pins 2 and 3.

(c). Stop the program that is presently running and type the following:

OUT-50,0:DEL-.1500:CON (cr)

(d). Observe that the negative going pulse at IC4 Pin 12 is low for about .8 to 1.1 seconds. (Sweep: .2sec/cm, Trigger: negative DC, normal trigger, not auto.)

(e). Remove the jumper on IC3 and reinstall IC3.

(6). The mini motor timeout timer is easy to test. Try the following:

(a). Place a scope probe on IC38 Pin 10.

(b). Stop the present program.

(c). Type in the following:

OUT-50

(d). Use a stopwatch or sweep hand on your non-digital watch and:

(e). Wait for a convenient time then depress (cr).

(f). The signal on IC38 Pin 2 should go high. Measure the time it takes for the signal to return low. This time

should be in the range of 10 seconds.

(g). Retime this signal a few times to be sure it is consistant. If the time varies by more that 20%, check to see if capacitor C72 is installed correctly.

(7). The last timer test is to see if the write precompensation circuit functions properly. There are 3 timers associated with this circuit that generate the compensation and one that generates the actual write data pulse. If your oscilloscope does not have the 15Mhz bandwidth to measure the following pulses accurately, just observe their presence for now.

(a). Jumper the following on IC29:

(1). Pin 4 to Pin 31.

(2). Pin 18 to 20.

(3). Pin 17 to 3.

(b). Type in the following:

INP-50:CON (cr)

(c). Observe the following:

(1). IC13 Pin 4 has 300 nanosecond negative pulse.

(2). IC13 Pin 12 is always high.

(3). IC12 Pin 4 is always high.

(4). IC12 Pin 5 has 250 nanosecond positive pulse.

(d). Jumper IC29 Pins 17 and 39 then observe the following:

(1). IC 13 Pin 4 is always high

(2). IC13 Pin 12 has 150 nanosecond negative pulse.

(3). IC12 Pin 4 is always high.

(4). IC12 Pin 5 has 250 nanosecond positive pulse.

(e). Jumper IC29 Pins 17 to 3 and 18 to 38. Then observe the following:

(1). IC13 Pin 4 is always high.

(2). IC13 Pin 12 is always high.

(3). IC12 Pin 4 has 450 nanosecond negative pulse.

(4). IC12 Pin 5 has 250 nanosecond positive pulse.

(f). Remove all jumpers installed on socket IC29.

(8). The last Disc I/O Buffers to be checked are the disc status lines. To do this test we will need a shorting wire. Each of the input disc signals should be shorted to ground at the 36 Pin edge cnnector while the user observes the voltage level at IC29. To enable the READY line one jumper must be used on IC29. The diode installed for the motor tests is to be removed.

(a). Remove the diode installed in the Mini/Standard position for device 0.

(b). Jumper IC29 Pins 28 and 39.

(c). Observe the following:

(1). When Pin 9 of the edge is shorted IC29 Pin 36 goes low.

(2). When Pin 5 of the edge is shorted IC29 Pin 35 goes low.

(3). When Pin 12 of the edge is shorted IC29 Pin 34 goes low.

(4). When Pin 8 of the edge is shorted IC29 Pin 32 goes HIGH.

(5). When Pin 17 of the edge is shorted IC25 Pin 9 goes low.

3.8 BRINGING UP THE 1791 IC

The last item to be tested is the 1791 itself. The previous tests have given us a 99% chance that the board will now work. We have checked all the circuitry associated with the 1791 IC except the operation of the Phase locked loop and the data lines. This will be done in this last section.

If you have been loading HMON/2 with the old Disc controller board, you will now have to load it a last time using the audio cassette.

At this time the user should go to the INSTALLATION portion of the manual to connect a drive to the Controller board. Be sure that all the proper

terminators have been installed at the disc drive.

(1). Remove the controller board from the system and check to see that Pin 1 of IC29 is NOT SHORTED to anything else.

(2). Reinstall the controller board and check to see if:

(a). Pin 21 of IC29 has +5 Volts to it.

(b). Pin 40 of IC29 has +12 Volts to it.

(c). Pin 20 of IC29 is at ground potential.

NOTE: IF THE 1791 IC IS INSTALLED UPSIDE DOWN, THE CHIP WILL BE DESTROYED. WE WILL TEST THE IC AT THE FACTORY AND NO WARRANTY REPLACEMENT WILL BE ALLOWED IF THIS HAS HAPPENED.

(3). Install the 1791 IC WITH PIN 1 AWAY FROM THE EDGE CONNECTORS.

Note: We will test the drive in the single density mode. If you wish, you may retest the drive in the double density mode using the procedures in this section.

(4). Place a Diode in the following positions:

(a). The select position for DS0.

(b). The single density position for DS0.

(c). If you have a Mini drive Install a diode in the mini position for DS0.

(5). Install the controller board into the computer in the slot assigned it.

(6). Reload HMON/2 .

(7). Begin execution at Option ~~6~~. ~~5~~ ok to use 6 here.

(8). Select device 0 by executing the following:

:OUT-54,0 (cr)

(9). Now see if the data lines are ok. Try:

:OUT-51,0:INP-51:OUT-51,377:INP-51 (cr)

The computer should respond with:

```
PORT 051 = 000
PORT 051 = 377
```

If your results are not the same, you have a shorted or open data line to/from the 1791 IC.

(10). Let's try to get the head over track 0. First, manually position the drive read/write head to the center of the disc by turning the shaft at the end of the steper lead screw by hand. Do not install the media at this time. But, close the door. Now try:

:LOA-0 (cr)

the computer responds with the prompt:

Enter Macro Instruction >

Now enter:

INP-51:CON (cr)

OUT-50,013:MAC-0 (cr)

The user should hear the drive step to track 0 while the screen displays a desending sequence of numbers from 377 to 000.

If you did not get these results, first be sure the device select light on the drive came on. If it did, again, manually spin the stepper motor shaft to force the head to the center of the disc. Try the test again. If the numbers do appear desending on the screen but the drive does not step, check all lines corresponding to DIR STEP TK00 DS0 and HLOAD. If the numbers are not decending on the screen, check the TK00 line first. If this line is low while the device select light is on, we still don't have good communication with the 1791 IC. Check IC29 Pin 24 for a 2Mhz signal if Standard drive or a 1Mhz signal for a Mini drive. If the clock line is ok then the problem is still in the data or port select logic. Remove the drive from the system and then remove the 1791 IC and return to the addressing section of this manual.

(11). Assuming that all is well so far, its time to format a diskette.

(a). Place an "expendable" diskette in the drive and close the door.

(b). Carefully place a scope probe on Pin 2 of IC38. (Write Gate)

(c). By now the drive select light should have gone out. If it hasn't, check the INDEX line for problems.
(d.) Start H-mon at option 5 (FOR- will not work on option 6.)
(e). Here we GO ! Type the following:

FOR-0 (cr)

The head should have loaded and the drive should be stepping. If there was no responce, check the HLT logic and its associated IC's.

If the drive IS stepping, check to see that the signal on IC 38 Pin 2 Is a square wave of 166/200 ms up 166/200 ms down (std/mini). If that is so, we're probably formatting the disc. To be sure:

(e). Wait for the format to finish and the head to unload.

(f). Carefully place the scope probe on Pin 5 of IC38. (Write Data)

(g). Retype the FOR-0 (cr) instruction.

See that the signal on Pin 5 of IC38 is a series of 250ns pulses occuring at a 2/4us rate (std/mini). If these pulses are absent check the Write Precompensation circuit, IC's 12, 13, 14, 16 and 30.

(12). Seems we can format. let's see if the controller can read.

(a). Type the following command:

RAT-3:RET (cr)

(b). You are now back in the Suding Operating System.

(c). Now enter HMON/2 at Option 5.

(d). You should hear the drive restore to track 0 and see the introduction message.

(e). Let's see if it can read. Type:

GED-0,1 (cr)

(f). The system should respond with a screen (128 bytes) full of 345's.

If the system went away, check the Interrupt lines you installed on the CPU and Motherboard plus the wait logic. If the system came back with an error (CRC RNF IDF), check the data separator in the following way:

Issue the following command:

TRK-0 (cr)

Place one scope lead on IC25 Pin 12 and the other on IC29 Pin 26. Trigger on the IC25 pin first. You should see a series of 200ns pulses on IC25 separated by 2/4us (std/mini). The other trace should be a overlapping square wave 180 Degrees out of phase with the pulses. There is a 250ns allowable "jitter" in the Square wave with respect to the pulses. Now switch triggering and see that the square wave stops overlapping and measures 2/4us up and 2/4us down (std/mini). There is an allowable error here but the timing should be within 5%. If the square wave has a severe "accordian" appearance to it the loop is not locking. Remove the diskette and readjust the VCO Free Running Frequency, (as done before in Sec 1.7-(2)), if incorrect. Tolerance is +5% and -0%. Reinstall the diskette and see if the problem clears itself. If not, there is a problem in some part of the loop. Go read the theory of operation of the VCO Phase locked loop and check IC's 6, 7, 8, 9, 10, 11, 15, 17 21, 24, 35 and 25.

(13). If you received a screen full of 345's, it looks as if the controller reads. But, let's be sure. Type:

RES:VER (cr)

Allow the drive to step through all tracks and return with:

DONE

Now type:

DEC:ERA:STA (cr)

The screen should erase and the Disc Status Table should be displayed. There should be 01001/00720 (std/mini) reads with no errors logged.

(14). The last test will be to see if the controller can read and write successfully. Type the following:

RES:ERA:RND (cr)

HMON/2 will now do 100 random read/writes. Wait for:

DONE

Now let's look at the Disc Log Table again by typing:

ERA:STA (cr)

The table should now show 100 reads and 100 writes with no errors.

If the above tests were successfull, The Board is in operating condition and you should read the Theory of Operation and the rest of the documentation. You might want to test the board further at this time. Read the tests available in the HMON/2 Manual and try some of them. The Disc Log Table

will keep track of the performance of the hardware and signals can be examined as these tests execute.

CHAPTER 4

THEORY OF OPERATION

4.1 INTRODUCTION

The Theory of Operation is broken into 13 sections, each covering a different portion of the circuitry. There is a partial schematic next to each section so that the user may view that section as he reads the theory.

As far as terminology is concerned, points on the schematic that are labelled with a signal name, will be called by that name. For points on the schematic that are not labelled, the IC and its associated pin number will be used (IC29 Pin 4 will be written as IC29-4). If an IC has more than one function the IC will be broken into parts, ie, IC13a.

There are many inputs and outputs of gates that require pullups. When a pullup resistor in used to pull up gates in different areas on the schematic, that pullup resistor appears in both areas. Don't be confused when you see numerous resisitor numbers repeated. Also, all resistors in the RPACK labeled IC26 are called out on the schematic as R26-(Pin Number).

4.2 PORT LABEL DEFINITIONS

The controller occupies eight consecutive I/O addresses. Of these, six are used. The base address must start on an address that is a multiple of eight. There are 32 such locations that the controller board can occupy. For the Theory of Operation and for the Software Listings, we will fix this base address as 050Q or 028H. All references to these ports could be either numeric or by their software label. The following table should aid the user in determining the ports.

PORT	INPUT DESCRIPTION	OUTPUT DESCRIPTION
050	STAT- 1791 STATUS	CMND- 1791 COMMAND
051	TRACK- CURRENT TRACK	TRACK- CURRENT TRACK
052	SECTOR- DESIRED SECTOR	SECTOR- DESIRED SECTOR
053	AVAIL BUT NOT USED	DATA- SEEK DATA
054	SEL- NUMEROUS FLAGS	SEL- DEVICE SELECT
055	NOT USED	NOT USED
056	NOT USED	NOT USED
057	WAIT- USER DATA PORT	WAIT- USER DATA PORT

FIGURE 1.

4.3 POWER-ON RESET AND LOW VOLTAGE CIRCUIT

The Power-On Reset and Low Voltage Circuit monitors the computer's +5 Volt line. It forces the 1791 into Master Reset on powerup and during any other time that the +5 Volt line decays below +4.3 Volts.

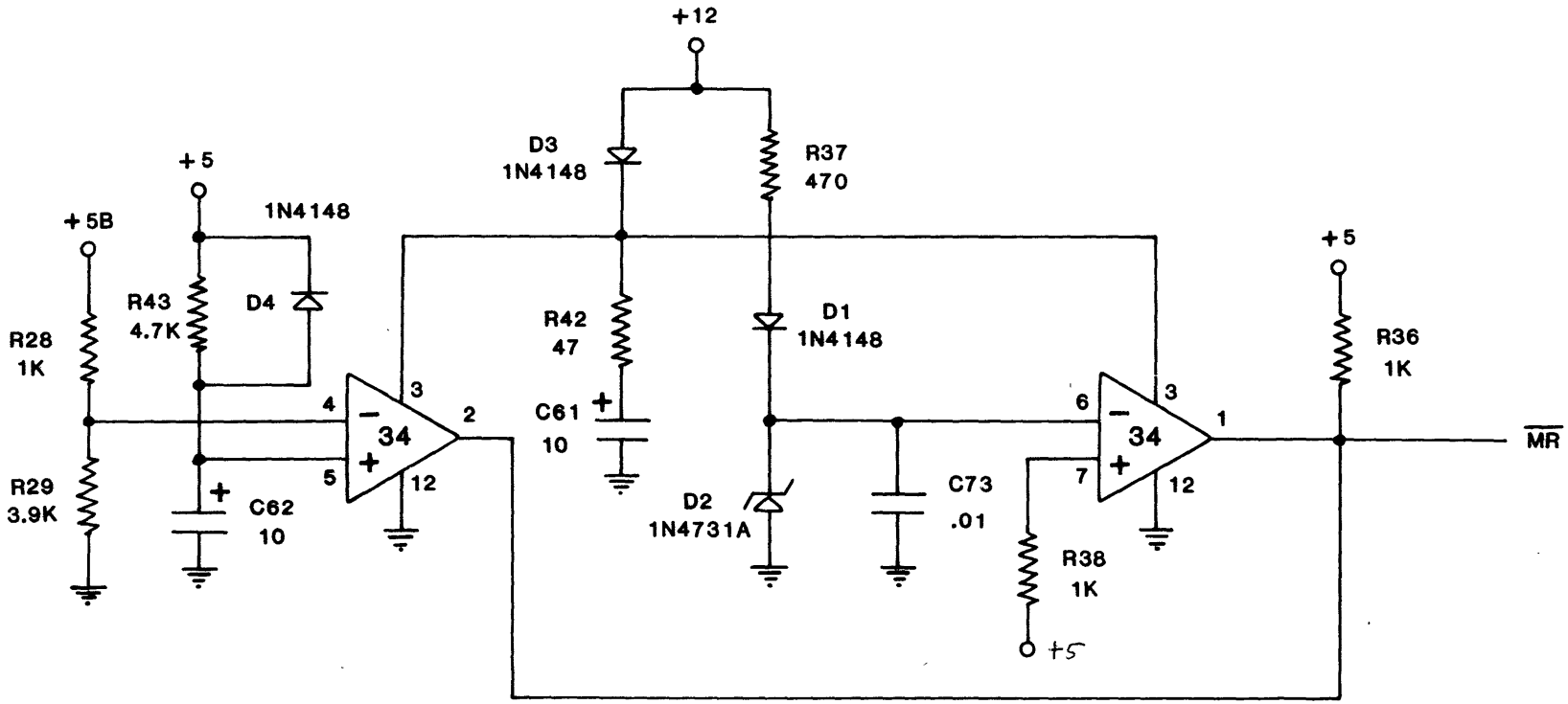
This circuitry also inhibits Write Gate during these occasions. This prevents the controller from accidentally writing over portions of the diskette.

This circuit consists of IC34, a Quad Comparator (2 used), and its associated resistors, capacitors and diodes.

During powerup the output IC34-2 has control of the circuit. The sequence of events are as follows: D54 has allowed C62 to discharge rapidly, insuring that on the initial (or subsequent) powerup, C62 will be discharged. When power is applied, C62 begins to charge through R37. At this time IC34-5 (the positive input) tracks the capacitor. R28 and R29 form a voltage divider that sets the negative compare voltage at approximately 4.0 Volts. Until this voltage is exceeded on the positive input IC34-5, the output IC34-2 remains low. The Capacitor, C62 takes approximately 50 milliseconds to charge to a voltage above 4.0 Volts. This keeps the output IC34-2 low for this time which forces a Master Reset into the 1791 IC. It also keeps the Write gate IC38-3 inactive.

During a voltage fluctuation on the +5 Volt supply that falls below +4.3 Volts, comparator output IC34-1 becomes active. The sequence of events is as follows: The positive input of the comparator IC34-7 tracks the +5 volt supply through R38. The negative comparator input, IC34-6, Has a fixed reference voltage of +4.3 Volts set by the Zener diode D3. R37 provides constant current through the Zener. When +12 Volts is lost, blocking diode D2, along with capacitor C73, temporarily provide the current for the reference Zener, D3. When the +5 Volt supply drops below the reference voltage on IC34-6, the comparator output IC34-1 goes low, again forcing the 1791 IC into Master Reset and inhibiting the Write Gate.

To insure that the outputs of the comparators remain active during a normal system power down, capacitor C61, along with blocking diode, D4, combine to supply the voltage and current for IC34. Resistor R42 insures a constant charging rate for C61.



POWER-ON RESET AND LOW VOLTAGE CIRCUIT

FIGURE 2

4.4 ADDRESS DECODE AND CPU I/O BUFFERS

The Address Decode and I/O Buffer circuit enables the computer to pass information to and from the Double Density Disc Controller board.

In order for the board to be accessed, the following conditions must be met:

1. The upper five address lines must match the selected base address.
2. The three lower address lines must be in the range of 0 through 4 or 7.
3. Either I/O READ or I/O WRITE must be active low.

When these conditions are met the board can be accessed for read or write.

ADDRESS GATING

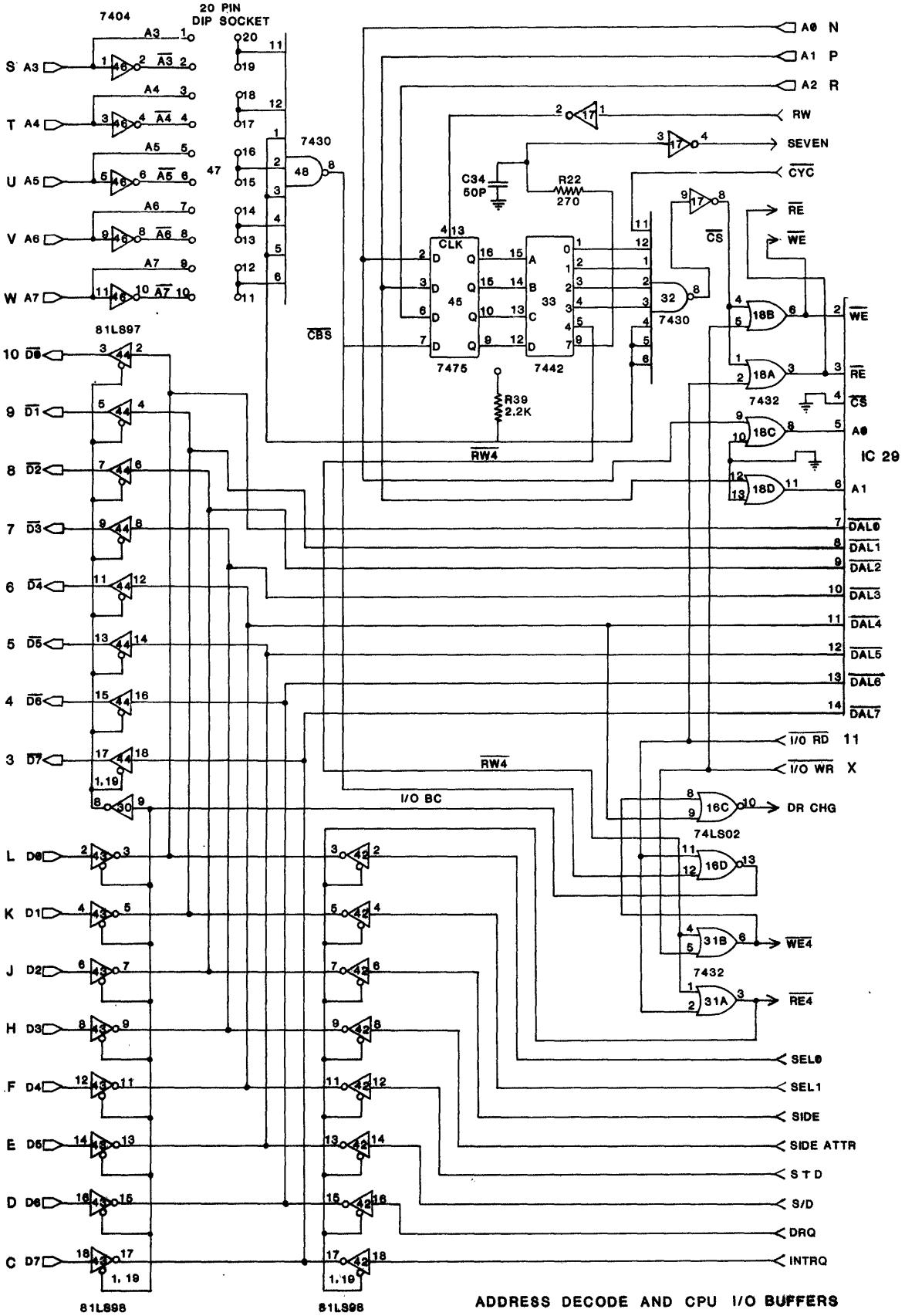
The addressing operation happens as follows: The upper five address lines are presented to IC46 where the user selects which section in the I/O address space he wishes the board to occupy. This is done by selectively inverting the proper lines in IC46. Once this has been done, when the computer sends this address to the board, IC48-8 will go low. This line is the Conditional Board Select (CBS) signal and is gated to the following: 1. To the I/O Buffer Control Gate IC16-12. 2. To the enable input of IC33, the Port Select Decoder. The lower three addresses are presented to the port decoder through Latch IC45. Also the lower two address lines are buffered in IC18c,d and presented to the Controller IC29. IC33 generates all the conditional port select gating. If the lower three address lines are between 0 and 3, IC33 gates on IC32-8 which in turn is inverted in IC17. This inverted Controller Select(CS) signal partially enables IC's 18a and 18b. If the lower three address lines were decoded in IC33 to be equal to 4, The RW4 signal is generated which partially enables IC's 31a and 31b. If the lower three address lines were decoded to be 7, The SEVEN signal is generated. This SEVEN signal is passed to the Wait logic.

We have at the present selected one of three things. We have generated the CS signal or the RW4 signal or the SEVEN signal. We have also partially enabled the I/O buffer control gate.

I/O READ

Now, if this is a I/O READ operation, the computer will lower the I/O READ line. This line is presented to four gates. First it will fully enable the I/O buffer control gate IC16-13 which will cause the input buffer IC43 to turn off and then the output buffer IC44 to turn on. Second it is combined with RW4 in IC31a. Third, it will combine with CS in IC18a.

If the RW4 signal was active, I/O READ combines with RW4 to generate the RE4 signal at the output of IC31a. This signal enables octal buffer IC42 onto the I/O bus allowing the computer to read the data in the D Latches IC41, the drive attribute bits, and the two status signals from the



ADDRESS DECODE AND CPU I/O BUFFERS

FIGURE 3

controller IC29.

If the CS signal was active, I/O READ combines with CS to form RE at the output of IC18a, which when generated, will gate the controller register, selected by the lower two address lines, onto the I/O data bus for the computer to read.

The I/O READ signal is also presented to IC19a, to be gated with the SEVEN signal, but this is in the Wait logic and will be discussed later.

I/O WRITE

Now, if this is an I/O WRITE operation, the computer will lower the I/O WRITE line. This line is presented to three gates. First, it is combined with RW4 in IC31b. Second, it is combined with CS in IC18b.

If the RW4 signal was active, I/O WRITE combines to form WE4 at the output of IC31b. This signal provides the strobe pulse to the Device Select, Side Select, and Interrupt Enable D type Latch IC41. It also conditionally enables the Drive Change signal(DR CHG) at IC16c. If Data bit 4 is low true at the time, the DR CHG signal is generated at the output of IC16c.

If the CS line was active, I/O Write combines to form WE at the output of IC18b. This signal enables the Controller register, selected by the lower two address lines, to be written into by the computer.

The I/O WRITE signal is also presented to IC19a, to be gated with the SEVEN signal. This is in the Wait circuit and will be discussed later.

I/O BUFFERS

The computer data interface to the controller is through three Octal buffer IC's 42, 43, 44. The controller's internal data bus is a low true bidirectional bus. When the board is not being accessed, the normal state of the internal bus is recieve. This normal state only changes to transmit when the computer has presented the proper port address and the I/O READ signal is active low. Since the computer I/O input bus is inverted, the Octal buffer IC44 is noninverting so that the controllers internal low true bus is gated to the computers low true I/O input bus. Octal buffer IC42 converts the high true data on its inputs to low true data for the controllers low true data bus.

4.5 WAIT LOGIC

The Wait logic enables the computer to wait for the data coming from the disc without the fear of waiting "forever". This is accomplished by the wait timeout timer.

If data is already present when the computer enters wait, a maximum of two extra wait states is added to the I/O cycle.

The Wait logic is conditioned by three signals. These are, I/O READ, I/O WRITE and SEVEN. When the computer executes an I/O instruction, either I/O READ or I/O WRITE will become active low. This Combination is NANDed in IC19a and then filtered by the RC network of R25 and C32. This cleaned up signal is used to latch the Conditional Board Select signal(CBS) and the lower three address lines in Latch IC44. If the decoder IC33 detects a 7, this signal is filtered by RC network of R22 and C34. The SEVEN signal removes the CLEAR input to IC7a and allows the ANDed signals of SEVEN and RW to clock IC7-11 through IC15-8. The SEVEN signal also triggers (or retriggers) the wait timeout timer, IC25a, at this time. Once IC7a has been clocked it should not be clocked again until the wait cycle finishes. The $\overline{Q}$ output of IC7a now goes low, enabling the Three state Gate IC37a to become active. The Q output of IC7a also removes the PRESET of IC2a,b. This allows IC2 to function. IC2-5 places a high on the input of IC37a forcing the computer into the Wait State.

To remove the wait, one of three events occur. First, the wait timeout timer can timeout. This causes a high level to be presented to IC36-13. Second, a Completion Interrupt can occur from the controller IC29. This causes a high level on IC36-1. Third and most common, a Data Request could be generated by the Controller IC29. This causes IC36-2 to go high. Any of these High levels at IC36a will cause the output IC36-12 to go low. Since we just removed the PRESET from IC2, the output of IC2-5 is high. This, along with the former high of IC36a, kept IC23-11 high. Now that IC36-12 is low, IC23-11 will go low. At the next 2Mhz clock rising edge, the Q output IC2-5 will go low. This signal now enables one input to IC32 (CYC) and causes the CS signal to be generated. This along with the lower two address lines being one, causes the fourth register in the controller to either be read or written. The signal from IC2-5 also disables the D input to itself through IC15-12. This forces the Q output IC2-5 to remain low until IC7a is CLEARed.

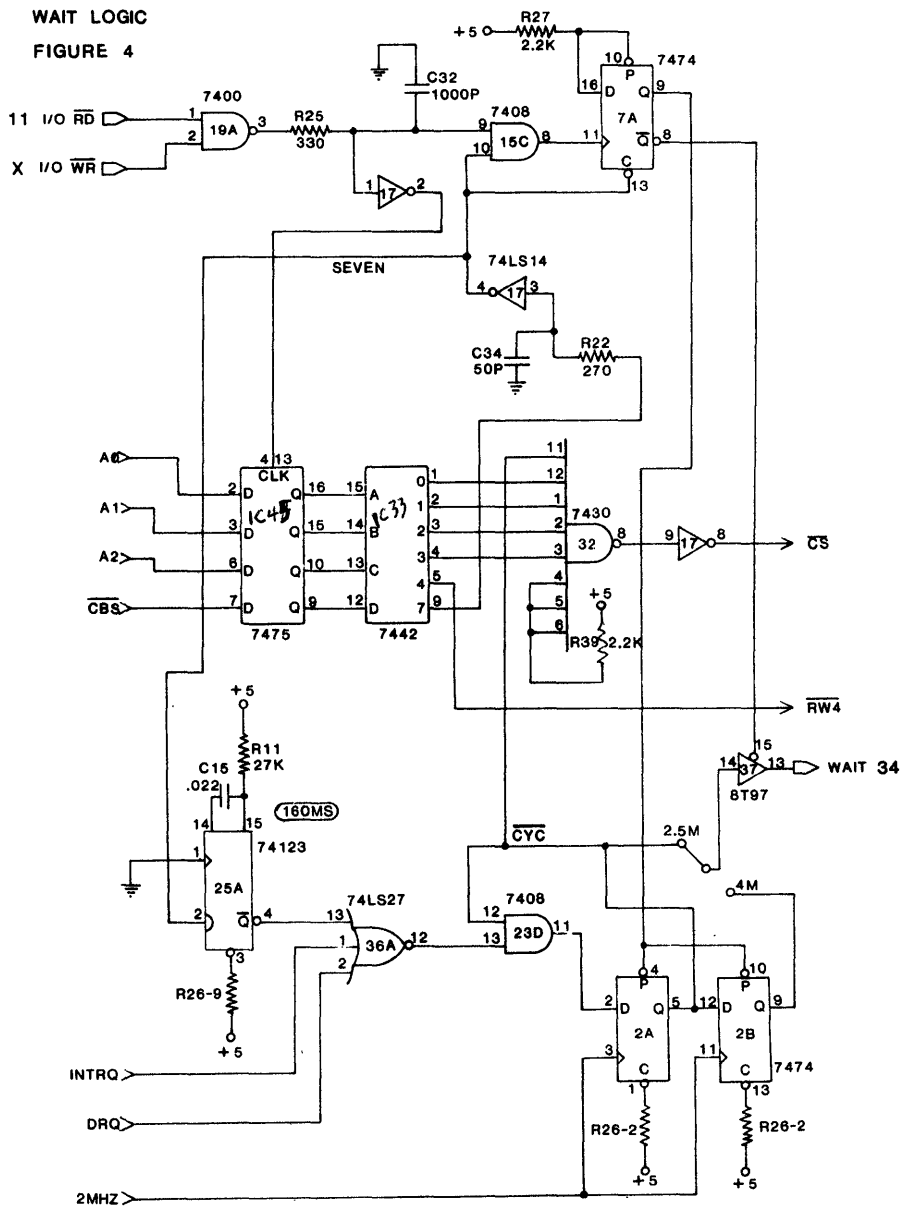
The controller IC29 was selected and we are still in wait. When the next 2Mhz rising edge comes along, the low at the D input IC2-12 is clocked to the Q output. This signal is gated to the CPU through IC37-13 and removes the wait request. Now we are waiting on the CPU to release from the wait state and remove either the I/O READ or I/O WRITE that started this wait state. When the computer removes this signal, Latch IC45 is opened and the next address on the address bus sets up. This in turn removes the SEVEN signal which forces IC7a into the CLEARed state. The Q outputof IC7a now

PRESETs IC2 while the $\overline{Q}$ output three states IC37a again. The wait Circuitry is now ready to start another cycle.

Note that when any one of the conditions to remove us from wait occurs, we must wait for the 2Mhz clock to occur. Then we must wait for the computer to acknowledge our request for wait state exit. If these first two events occur at their worst case times, (fastest) we could cycle so fast that we don't meet the access time of the controller IC29. There is a jumper removing the second period of wait if the CPU is running at 2.5Mhz. If the system were to be run at 4Mhz without the trace broken and the jumper installed to add this second 500ns delay (IC2-9) the access time of the controller IC29 would be exceeded. Therefore if the system is to be run at 2.5Mhz, no modifications need be done. However, if the system is to be run at 4Mhz, the user should cut the trace butween IC2-5 and IC37-14 and jumper IC2-9 to IC37-14. NOTE that The Digital Group does NOT support a 4Mhz system (4/79).

WAIT LOGIC

FIGURE 4



4.6 SEL PORT LOGIC

The SEL Port logic contains all drive select, side select, board interrupt enable, and drive change logic. The drive select bits are read/write. The side select bit is read/write only if that particular drive is jumpered as present. The board interrupt enable bit and the drive change bit are write only. All bits except the drive change bit are stored in D type Latch IC41.

There are three drive attribute bits associated with the SEL Port. These bits set up the drive's attributes according to the diode matrix. This matrix allows each drive to be of a different size or density or number of sides.

DRIVE SELECT CIRCUITRY

The lower two bits of the SEL port are the Drive Select bits. These bits are presented to the drive select decoder, IC28, where a Two Line to Four Line decode takes place twice. The first, in IC28a, is used to select the correct drive when the head is loaded. This decoder provides the drives with the Drive Select signal through inverter IC27 and Open Collector Driver IC39. The second set of decoding, IC28b, is active all the time and provides the diode matrix with one crosspoint per drive. These crosspoints are labeled 1 through 4 on the schematic and correspond to drives 1 through 4 that may be attached to the controller. The crosspoints provide a ground for the diodes that would be installed to select certain attributes.

SIDE SELECT CIRCUITRY

The Side Select bit is the third bit. This bit is sent to the drives through Open Collector Driver IC40d. The Side Select line, IC41-3, is logically ORed in IC31d with the "A" column of the diode matrix before being read back by the computer through Octal buffer IC42. Placing a diode in the "A" column for the selected drive causes resistor R18 to be pulled low by an output of IC28b. This low allows the output of IC31d to track the input IC31-13. If no diode was installed in the "A" column for the selected drive, resistor R18 presents a constant one to the output of IC31d regardless of the condition of the Side Select D Latch IC41.

The software selects the bottom side of a particular drive by writing a zero to the side select bit. If upon reading back this bit, the software finds that it has changed to a one, it can be assumed that no drive is present for this particular drive number.

DRIVE CHANGE CIRCUITRY

The Drive Change signal is generated by the combination of WE4 and the fifth bit of the SEL Port in IC16-10. This signal is a one microsecond positive strobe and is Write only. The drive change strobe triggers the

head load delay one shot IC4-4 if the head was already loaded. (See Figure 4.)

BOARD INTERRUPT CIRCUITRY

The top output bit is the Board Interrupt Enable bit. This bit is write only. When set to a one, this signal allows the interrupt generated by INTRQ or DRQ in IC36b,c to be gated through Open Collector driver IC40c. Specific causes for interrupts are discussed in the 1791 section.

ATTRIBUTE SELECT LOGIC

The Drive Attribute Logic performs all logic switching to convert the controller board from different densities and different size diskettes. There are four attributes that are selected by the diode matrix for each drive. These are:

A. Drive Present (explained in Side Circuitry).
B. Single or Double Density.
C. Mini or Standard Drive.
D. One or Two Sided.

Three of these attributes are presented to the computer on bits three through five of the SEL Port through IC42.

The first of these attributes is the Single/Double Density attribute. To generate the Double attribute, no diode is placed in the "B" column for the selected drive. This causes resistor R19 to pull up the "B" crosspoint for the selected drive. In turn, IC30b inverts this high to generate a low S/D signal. The S/D signal is gated with other portions of the circuit to select Double density. This signal is also presented to Octal buffer IC42. If a diode is installed in the "B" column in the matrix for the selected drive, the line from IC28b pulls down resistor R19, which is then inverted through IC30b to produce a high S/D signal. This high S/D signal is then gated to other portions of the circuit to select Single Density.

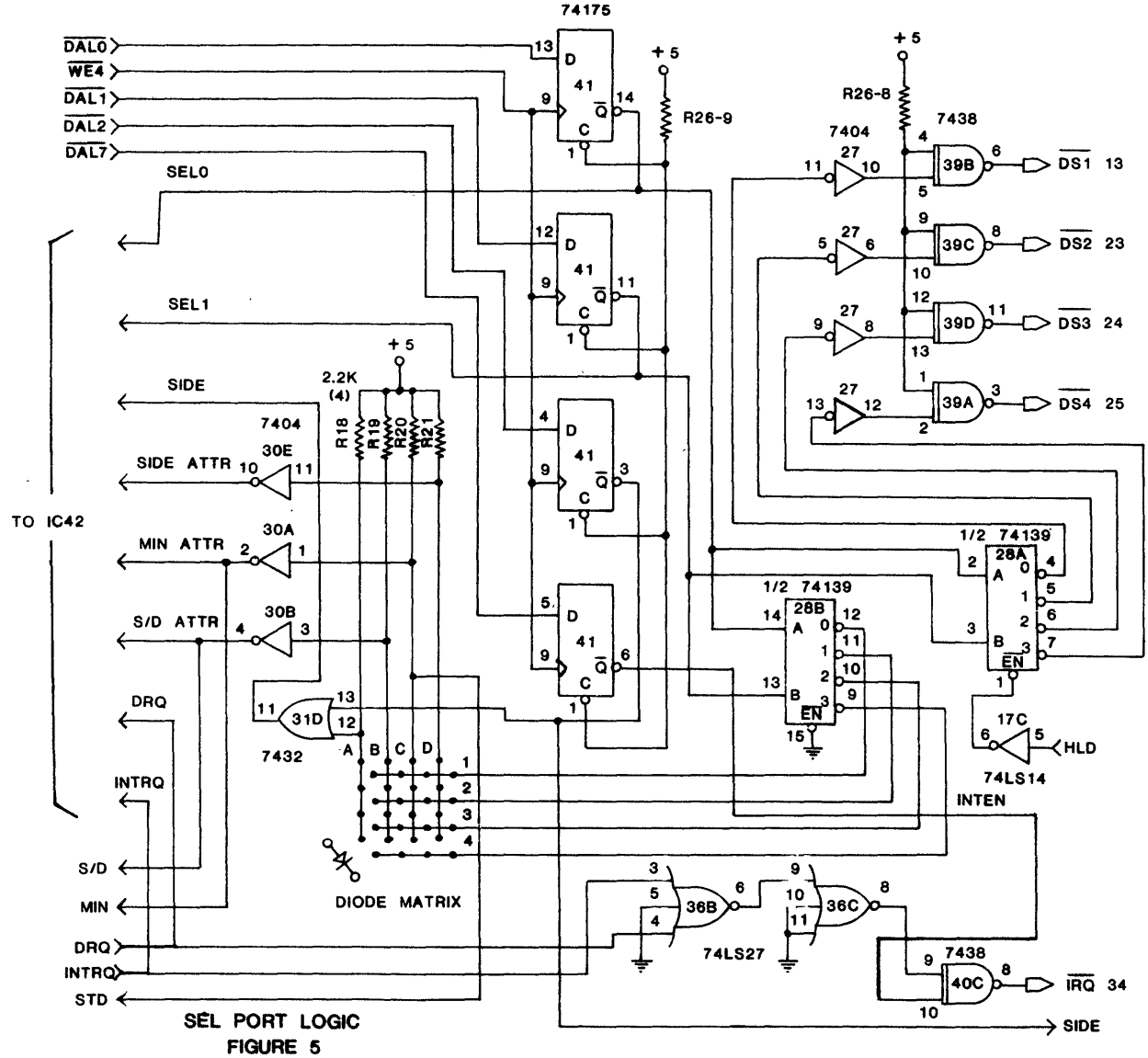
The second of these attributes is the Mini/Standard attribute. To generate the Standard attribute, no diode is placed in the "C" column for the selected drive. This causes resistor R20 to pull up the "C" crosspoint for the selected drive. This in turn generates a high STD signal attached to R20. IC30a invert this high level to generate a low MIN signal. Both of these signals are gated with other portions of the circuit to select a Standard drive. The output of IC30a is presented to Octal buffer IC42. If a diode is installed in the "C" column in the matrix for the selected drive, the line from IC28b pulls down resistor R20, which generates a low STD signal. This low is inverted in IC30a to generate the high MIN signal. Both these signals are gated to other portions of the circuit to select a Mini drive.

The third attribute is the Side attribute. To select a single sided

drive, no diode is installed in the "D" column for the selected drive. This causes resistor R21 to pull up the input of inverter IC30e. The low output of IC30e is passed to Octal buffer IC42 to be read by the computer as single sided. If a diode was placed in the "D" column of the selected drive, the output of IC28b will pull down resistor R21. This low is inverted by IC30e and passed to Octal buffer IC42 to be read by the computer as double sided.

OTHER SEL PORT SIGNALS

Two other read only signals are accessable by reading the SEL port. These are status outputs of the controller IC29. The INTRQ output IC29-39 is passed to the top bit of Octal buffer IC42 while the DRQ output IC29-38 is presented to the ~~sixth~~ bit of Octal buffer IC42. These two signals will be explained in the 1791 section.

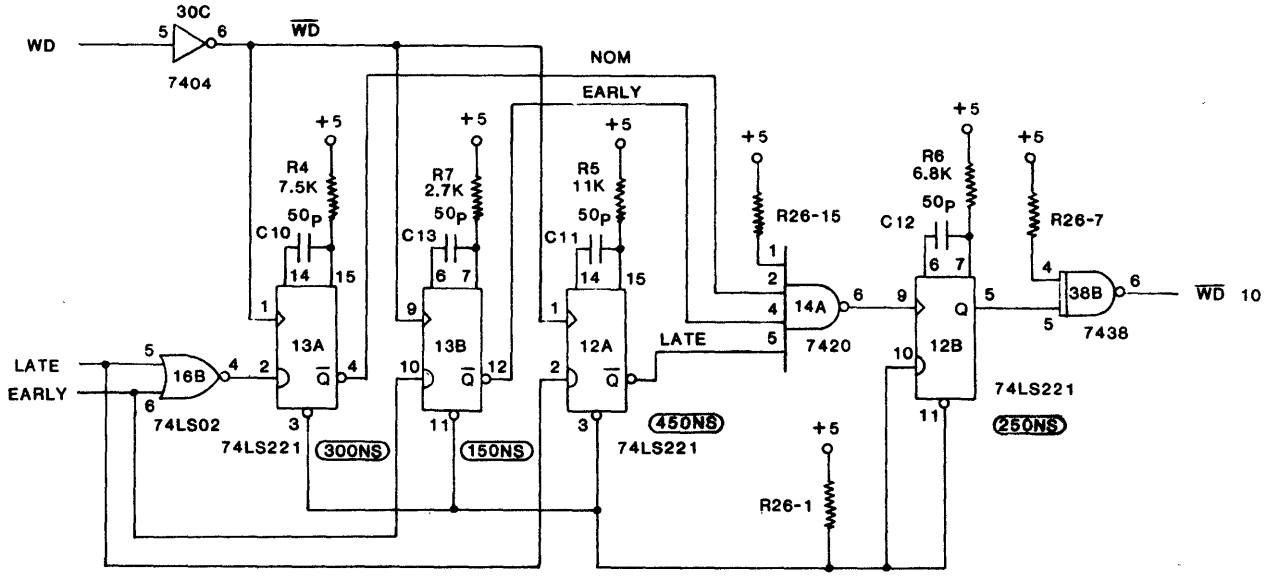


SEL PORT LOGIC
FIGURE 5

4.7 WRITE PRECOMPENSATION CIRCUIT

The Write Precompensation Circuit generates the proper amount of compensation to the Write Data pulse for reliable Double Density operation. This is done by selecting one out of the three one-shots to be fired for the correct length of time. The original Write Data pulse is delayed a fixed amount of time for Nominal Data timing. For an Early Write data pulse, the original Write Data pulse is generated 150 nanoseconds earlier than a Nominal Data pulse. For a Late Write data pulse, the original Write Data pulse is delayed 150 nanoseconds after the Nominal Data pulse.

Three signals from the controller IC29 are required to operate the Write Precompensation Circuit. These are Early, Late and Write Data. The Early and Late signals are valid prior to the leading edge of each Write Data pulse. The Early signal IC29-17 is passed directly to the negative edge enable input of the Early one shot IC13b. The Late signal IC29-18 is passed directly to the negative edge enable input of the Late one shot IC12a. Both the Early and Late signals are NORed in IC16b to produce the negative edge enable signal for the Nominal one shot IC13a. Note that under normal operating conditions, the combination of Early and Late being high at the same time is not possible. The Write Data pulses are inverted by IC30c to produce a negative pulse. This negative pulse is presented to the negative edge trigger input of Early, Nominal and Late one shots IC13b, IC13a, and IC12a. Whichever oneshot has its negative edge enable input high will fire at this time. This pulse in NANDed in IC14 to trigger the Write Data one shot IC12b on the falling edge. This one shot produces a positive going 250 nanosecond Write Data pulse that is presented to the drives through Open Collector Inverting Driver IC38b.



WRITE PRECOMPENSATION CIRCUIT

FIGURE 6

4.8 DELAY AND READY LOGIC

The delay logic performs three delay functions. The READY logic is also included in this section.

MINI MOTOR DELAY TIMER

The first delay is the motor timeout timer for Mini drives. This timer IC3 acts as a retriggerable one shot. The timer is enabled by the MIN signal on Pin 4. The timer is triggered by one of the four port enable strobes RE, WE, RE4, WE4 through IC14. Once triggered, capacitor C9 charges through resistor R3. When further accesses are made to the board, IC14 pulses high. These high pulses are used to partially discharge capacitor C9 through two Open collector Inverters IC21c,d. This discharge pulse is one micro second in duration and many of these pulses are required to maintain a low voltage on capacitor C9. It should be noted then, that the motor on timer requires HEAVY board usage to maintain the mini motors in the on state.

MINI MOTOR STARTUP DELAY TIMER

The second timer is the mini motor startup timer IC4b. This timer inhibits the controller IC29 from reading or writing until the mini motors are up to speed. The only time this timer fires is when a rising edge is generated by the mini motor timer starting. If the selected drive is a Mini drive, the STD signal is low. This signal is presented to the positive edge trigger enable input IC4-9. The rising edge of IC3-3 generates a negative going pulse out of IC4-12. This negative going pulse is ANDed with the Head load delay timer in IC15a to produce a low on IC29-23 whenever a delay in reading or writing to the disc is required.

HEAD LOAD DELAY TIMER

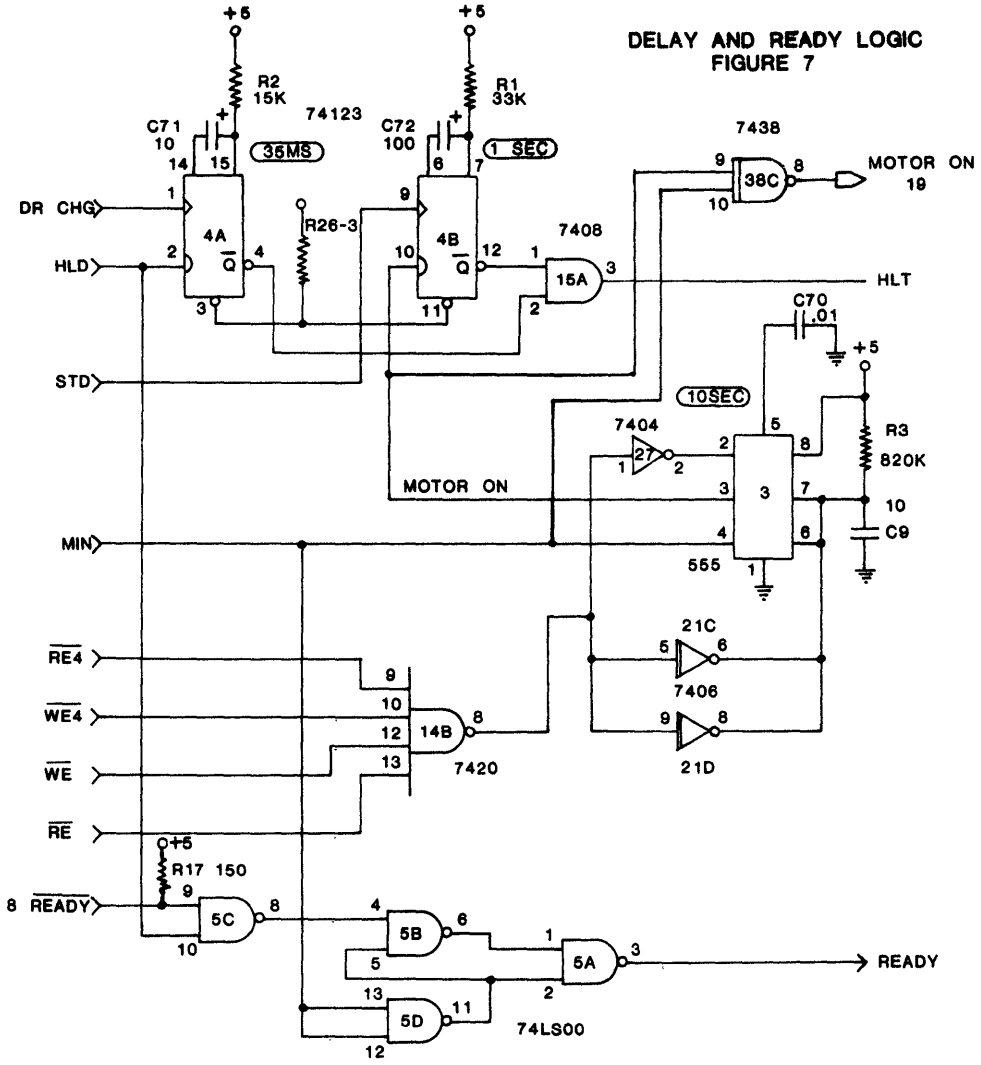
The third timer is the head load delay timer. This timer inhibits reading or writing to the disc whenever the head has been loaded and the head settling time has not expired. The head load delay timer can be triggered in one of two ways. The first way is when the controller IC29-28 (HLD) goes high signifing that the head is to be loaded. On this occasion, IC4-1 is low. The rising edge HLD into IC4-2 causes the one shot to trigger. This generates a low outpput pulse on IC4-4 which is ANDed with the mini motor startup timer in IC15a. The output of IC15a generates a low on IC29-23 causing reading or writing to the disc to be inhibited.

The second way the head load timer may be triggered is when the head is loaded and a drive change pulse is issued. When the head is loaded, HLD presents a high to IC4-2. This high level is also equivalent to the negative edge enable required by the negative edge trigger input to trigger. When a drive change pulse is generated in IC16c (DR CHG), the negative edge of this pulse triggers the Head load timer. The drive change pulse only will trigger the head load timer when the HLD signal is active high.

READY LOGIC

The Ready logic performs three tasks. It allows the Ready line from a Standard drive to be inverted and gated to the controller IC29-32 whenever the head is loaded. It prevents the Ready line to the controller IC29-32 from going Not Ready whenever the head is not loaded. It also presents a constant Ready to the controller whenever the controller is using Mini drives.

IC5 performs all the Ready logic functions. IC5a,b,d combine to form an AND OR circuit. One input to the AND OR is through IC5c. The two inputs to IC5c are the high true head load (HLD) signal and the low true Drive Ready signal from 36 Pin edge connector Pin 8. Resistor R17 terminates the Drive Ready signal. The only time a Not Ready signal is Presented to the IC5-4 input to the AND OR circuit is when the drive is Not Ready (IC5-9 high) and the HLD signal to IC5-10 is high. This causes the output of the AND OR gate to go low if IC5-5 was high. In order for IC5-5 to be high, IC5d must have a low on its input, which is the MIN signal. This case would be true if the STD signal has high (selecting Standard drives). If the MIN signal was high, its inversion through IC5d disables the Standard drive ready line and produces a constant high on the output of the AND OR gate by placing a low on IC5-2.



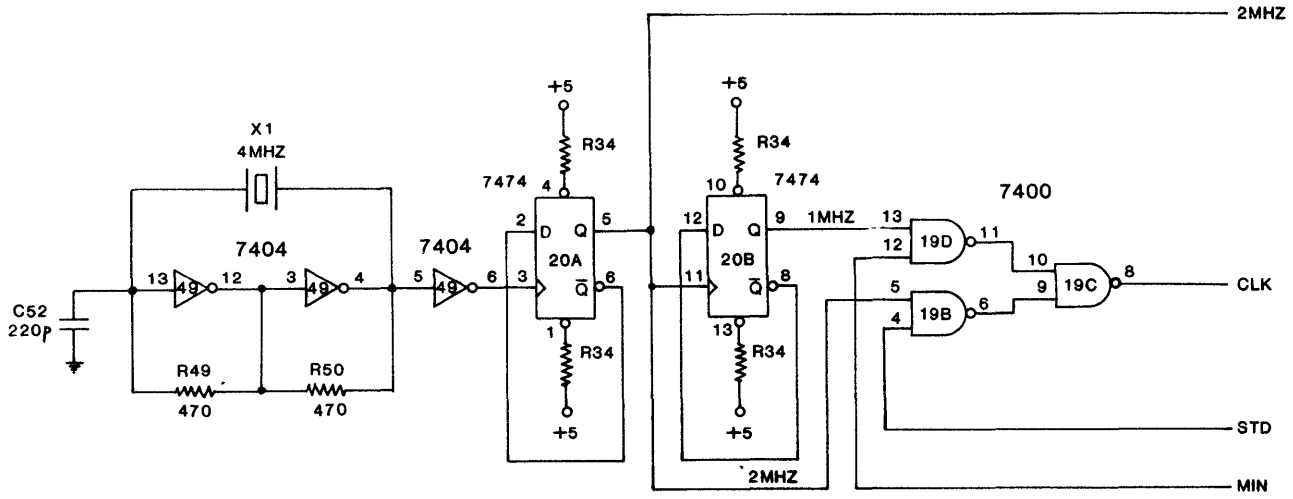
DELAY AND READY LOGIC
FIGURE 7

4.9 CONTROLLER CLOCK CIRCUIT

The controller clock circuit generates and switches the system clock between the two frequencies required for Mini and Standard drives. The clock frequency for Standard drives is 2 Mhz and the the clock frequency for Mini drives is 1 Mhz.

A 4 Mhz clock signal is generated by the TTL oscillator IC49. D type Flip Flop IC20a divides this 4Mhz clock by 2 before it is presented to D Flip Flop IC20b where it is divided by 2 again. The Q output of IC20a is presented to IC19b which is acting as a two to one line decoder. The Q output of IC20a is presented to IC19d. The 2 Mhz clock is passed to the controller IC29-24 through IC19b,c when the STD signal is high. The 1 Mhz clock is passed through IC19d,c when the MIN signal is high.

The 2 Mhz signal from IC20a is also presented to the Wait logic for the clocking of IC2.



CONTROLLER CLOCK CIRCUIT
FIGURE8

4.10 VCO PHASE LOCKED LOOP

The VCO Phase Locked Loop is comprised of six sections. These are:

1. Phase Comparator
2. Loop Filter (switchable)
3. Amplifier
4. Low Pass Filter
5. Voltage Controlled Oscillator
6. Divider Chain

PHASE COMPARATOR

The Phase Comparator determines the phase error of the input frequency (Data) against the present VCO frequency and generates a difference voltage used to change the frequency of the VCO towards the incoming Read Data frequency.

Read Data from the disc is buffered by IC37d. The Read Data line is terminated by resistor R15. The buffered Read Data is presented to IC25b where the input pulse is shortened to 200 nanoseconds. The Q output of IC25b is sent to the controller IC29-27 as the RD pulses. The Q output of IC25b is presented to the clock input of IC35b. IC35b, a D type Flip Flop performs a divide by two on the data. This converts the input data from a pulse to either a rising edge or a falling edge. This divided by two data is presented to D type Flip Flop IC35a. Here the Data is clocked with the 2X VCO frequency. A phase comparison is made between the 2X VCO and the input data in IC6b. This comparison is inverted in IC17e and then reinverted in IC21f to produce the Pump Up signal. The Pump Up signal is also ANDed with the 1X VCO signal in IC15d and then presented to the D input Of D type Flip Flop IC24b. This Flip Flop is clocked by the 2X VCO signal. The Q output of IC24b is inverted in IC21e to produce the Pump Down signal.

LOOP FILTER

The Loop Filter generates the lock, range and steady state Phase error constants of the system. It has two extra capacitors that are switched into operation to change the characteristics of the loop for different data rates.

The Pump Up and Pump Down signals are combined at the junction of resistors R40, R32, and R33. The steady state bias point of this junction is 2.5 Volts. The Pump Up and Pump Down signals vary this voltage in proportion to the frequency difference between the incoming data pulses and the 1X VCO frequency. Loop filtering is done in resistor R33 and Capacitors C48, C49 and C50. In Double Density Standard mode, both C48 and C50 are gated off by the two lows presented to the inputs of IC's 15b and 6c. The two lows are the MIN and S/D signals produced in the diode matrix. In the Single Density Standard and Double Density Mini mode, only capacitor C48 is gated off. In this case, one of the two signals MIN or S/D is low. One of these lows inhibits one input of AND gate IC15b. Capacitor C50 is gated on by one of these signals also through IC6c. The last case is the Single Density Mini. Here, capacitor C48 is gated on and capacitor C48 is gated off. In Single Density Mini, both MIN and S/D are active high. This enables AND gate IC15b and disables XOR gate IC6c. These capacitors modify the natural frequency of the loop to accomodate the different data rates of the above types of drives.

LOOP AMPLIFIER

The Amplifier is used to adjust overall loop gain. This Amplifier must have a high slew rate.

The Loop Amplifier is a noninverting high slew rate Operational Amplifier with a gain of +2.1. The input resistance is the parallel combination of R41 and R47. The feedback resistor is R46. The negative input is biased at 2.5 Volts to adjust for the steady state input bias from the Loop Filter. This steady state bias is passed to the next stage.

LOW PASS FILTER

The Low pass filter is used to remove high frequencies introduced by the digital phase comparitor. It is also used to reduce the response of the loop to instantanious variations in the input data stream.

The Low Pass Filter is a 2 Pole Butterworth Active filter. The cutoff frequency of this filter is approximately 150 Khz. The Low Pass Filter consists of IC9 a LM741, capacitors C65 and C66, plus resistors R44 and R45. It is a noninverting type filter.

VCO

The VCO is the basic clock for the loop. It has a Range input to set the Mhz/Volt constant and a Frequency input to vary the output frequency to achieve lock.

The VCO is a Texas Instruments 74S124 Dual VCO IC. Its free running frequency is set by the Range input and capacitor C53. The output frequency is 8Mhz. Capacitor C54 filters the Frequency control input to remove any high frequency noise generated by the TTL circuits nearby. The 8Mhz output

on IC8-7 is sent to the Divider Chain to provide the 1X and 2X VCO signals required for the Phase Comparitor. The second VCO section of IC8 is disabled.

DIVIDER CHAIN

The Divider Chain provides different divide rates for the different data rates used in the controller. It also provides the controller IC29 with the 180 degree out of phase bit rate clock required for data separation.

The Divider Chain receives its input from IC8-7 the VCO. This 8Mhz signal is first divided by two in D type Flip Flop IC7b. The output of IC7b is a 4 Mhz signal presented to the Binary divider IC10. IC10 divides this 4 Mhz signal into the different 1X and 2X VCO signals required. IC11 is a Dual four line to one line multiplexer. The output of IC11b is the 1X VCO signal. The output of IC11b is the 2X VCO signal. The multiplexer is switched by the S/D and MIN diode matrix signals. The output periods of IC11 for different S/D and MIN signals are tabulated below.

S/D	MIN	DRIVE TYPE	IC11a	IC11b
0	0	D.D. STD	1 us	.5 us
0	1	D.D. MIN	2 us	1 us
1	0	S.D. STD	2 us	1 us
1	1	S.D. MIN	4 us	2 us

The output of IC11b is first limited to a period of 800 ns low and 800 ns high by IC1. This prevents exceeding the limits imposed by the controller IC29 on its RCLK input IC29-26 (see 1791 operating specs). This signal is then divided by two to generate the 180 degree out of phase RCLK signal in IC24a. The RCLK signal is presented to the controller IC29-26.

4.11 DISC I/O BUFFERING

The Disc I/O signals and the IRQ signal buffering will be discussed here.

There are three Status signals from the drive that are buffered by parts of IC37. These are:

The Write Protect Signal enters the controller board on 36 Pin edge connector Pin 9. This line is terminated by resistor R12. The Write Protect signal is buffered in IC37a and is presented to the WP controller input IC29-36.

The Index signal enters the controller board on 36 Pin edge conector Pin 5. This line is terminated by resistor R13. The Index signal is buffered in IC37b and then presented to the IP controller input IC29-33.

The Track 0 signal enters the controller board on 36 Pin edge connector Pin 12. This line is terminated by resistor R14. The Track 0 signal is buffered in IC37c and then presented to the TR00 controller input IC29-34.

There are four controller outputs that are inverted and buffered by Open Collector IC38. These are:

The Write Gate signal is conditioned by the Master Reset signal in IC38a before being sent to the drives on 36 Pin edge connector Pin 7.

The Write Data signal is sent to the drives through IC38b. This signal leaves the board on 36 Pin edge connector Pin 10.

The Motor On signal from IC3-3 is conditioned by the MIN signal in IC38c before being sent to the drives on 36 Pin edge connector Pin 19.

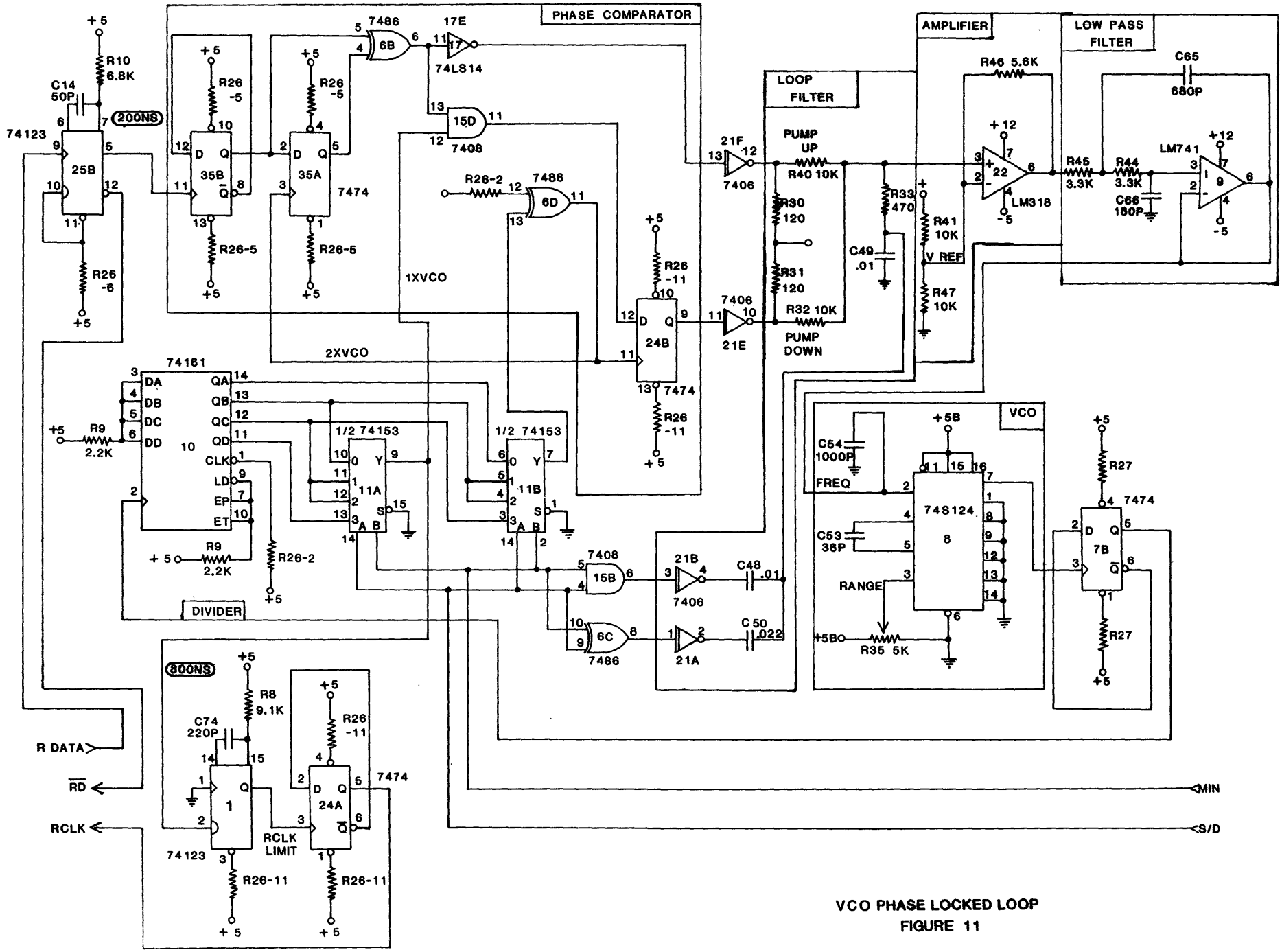
The Head Load signal is conditioned by the STD signal in IC38d before being sent to the drives on 36 Pin edge connector Pin 18.

The Drive Select signals DS1, DS2, DS3, and DS4 are inverted and buffered by IC39b,c,d,a before being sent to the drives in 36 Pin edge connector Pins 13, 23, 24, and 25 respectivly.

There are three drive lines and one CPU line buffered in IC40. These are:

The Direction line is buffered in IC40a before being sent to the drives on 36 Pin edge connector Pin 15.

The Step signal is buffered in IC40b before being sent to the drives on 36 Pin edge connector Pin 6.



VCO PHASE LOCKED LOOP
FIGURE 11

The Side signal is buffered in IC40d before being sent to the drives on 36 Pin edge connector Pin 21.

The IRQ signal is buffered in IC40c before being sent to the CPU Interrupt Socket Pin 8 through 36 Pin edge connector Pin 34.

4.12 POWER SUPPLIES

The +12 Volt supply for the board enters on 22 Pin edge connector Pin 22. It provides +12 Volts to the controller IC29, The Amplifier IC22, the Low Pass Filter IC9 and to the Comparator IC34. It is filtered by capacitors C38, C59, C63, C68 and C69.

The -5 Volt supply for the board enters on 22 Pin edge connector Pin B. It provides -5 Volts to the Amplifier IC22 and the Low Pass Filter IC9. It is filtered by capacitors C41, C42, C60 and C64.

The +5 Volt supply for the board enters on 22 Pin edge connector Pins 1 and A. This supply provides all +5 Volts to the TTL integrated circuits and to the pullup resistors. The +5 Volt supply is also filtered by inductor L1 and then provides the +5b Voltage for the VCO section. The +5 volts is filtered by numerous tantalum and disc ceramic capacitors.

4.13 INTERRUPTS

The Digital Group Double Density Controller board uses a scheme of Interrupts that you probably have never seen before. This type of interrupt uses Interrupt Mode Zero (8080) to jam an instruction into the Z80. This instruction is a LD A,A. This instruction is jammed onto the bus through the CPU Vector Interrupt Socket Pin 8 (bit 7). When CPU Interrupts are enabled, pulling down one of the Vector lines causes an Interrupt to occur. When the Z80 acknowledges the interrupt, a Vector of 177Q or 7FH is jammed onto the bus. In Interrupt Mode Zero, this Vector is taken as an instruction and is executed by the CPU as if this instruction was fetched from memory. After execution, the program counter is incremented as in any instruction, and normal processing continues.

In the Digital Group Double Density Controller Software for reading or writing a sector, this interrupt scheme is used. When the controller board needs to read or write a sector:

1. Controller Board interrupts are enabled.
2. Read or Write command is issued.
3. CPU Mode Zero Interrupts are enabled.
4. Halt instruction executed. (Refresh working)
5. Controller Board issues an Interrupt.
6. The LD A,A instruction executed instead of Halt.
7. Read or Write data is done using Wait logic.
8. Controller Board interrupts disabled.
9. Software returns to calling program.

CHAPTER 5

1791 PRODUCT SPECIFICATION

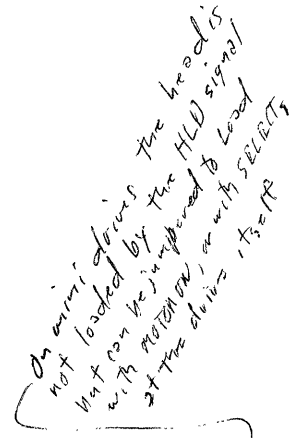
5.1 INTRODUCTION TO WD1791 PRODUCT SPECIFICATION

We should review some of the curcuitry of the controller board before reading the 1791 Product Specification.

The 1791 IC is equivalent in architecture to many of the microprocessors in use today. It has a fixed instruction set and executes instructions as they are given to it. These instructions take longer to execute than a normal microprocessor instruction, but these instructions are more powerfull than most microprocessor instructions. When an Instruction is given, the 1791 resets the INTRQ flag (if set) and then sets its busy flag. Upon completion of the instruction, the 1791 resets its busy flag and then sets the INTRQ flag. This latter flag is available for testing as the top bit in the SEL Port. It is STRONGLY recommended that the software test the INTRQ bit while waiting for instruction completion.

Each instruction has a field in that instruction that performs specific functions. These are :

1. Load the head at the start of the operation.
2. Verify for the correct track when done.
3. Update the internal track register when done.
4. Step at a specific rate.
5. Read or Write multiple sectors.
6. Write with Deleted or Regular Address Mark.
7. 15 millisecond delay or not.



With the hardware configuration of the Digital Group Double Density Controller Board one of these optional bits is NO LONGER OPTIONAL. The Head load bit in all Step, Seek and Restore Instructions MUST be SET. One of the conditions for drive select in the hardware is that the head must be loaded.

Also some of the bits have to be used correctly. Here is a summary of these bits and how they should be used.

The Verify bit should be used at the users option. It verifys the position of the head after a Seek, Step or Restore by reading the first ID field it encounters on the Track. UNDER NO CIRCUMSTANCES should the user

have the verify bit ON during a DISK FORMAT operation. It should also be noted here that on a Seek, Step or Restore Instruction that had the Verify bit RESET, no step settle time is added to the Instruction. That is, the user must now wait the drive manufacturers specified Step Settle Time BEFORE issuing a Read Sector or Write Sector Instruction.

The Update bit is used to increment/decrement the Track register in the 1791. Presently no software provided by the Digital Group uses this bit. All Stepping operations are done with the Seek Instruction and this Instruction automaticlly updates the Track Register.

The Step Rate bits are used to set the step rate to one of four available rates. These bits should be set closest (equal or above) to the drive manufacturers specified step rates.

The Read or Write Multiple Sector bit allows the user to read or write entire tracks of data to/from memory with only one Instruction. This bit is not presently used in any of the Digital Group software. It is recommended that the user NOT try this option until he has MASTERED the theory behind the Interrupt/Halt data transfer scheme used in the software.

The Write with Deleted Data Mark bit should always be set to zero. This bit is fine for IBM but it serves no usefull purpose as far as we are concerned.

Another bit that should always be set to zero is the 15 millisecond delay bit. This bit is left over from the 1771 IC and since then the Read and Write Sector flowcharts have changed. If this bit is set, only one sector per revolution can be read if you are reading sectors sequentially. (See the 1791 flowcharts for a better explanation.)

Other bits that have not been implemented in the Digital Group software are Interrupt Instruction bits 0 through 3. The user might find a use for these bits after he becomes familiar with the system. We recommend that the Interrupt Instruction be executed with all these bits off.

A brief explanation of the 1791 internal registers is also in order.

The first register is the Command/Status Register. This is the register that all Instructions are written to and all Status is read from. Reading this register resets the INTRQ bit in the SEL Port. Since this bit is used to generate CPU Interrupts it is recommended that all software read the status register after command completion to clear the INTRQ bit whether or not the status is needed.

The second register is the Current Track Register. This register should only be written to when changing drives. It can be read at any time to see what Track the head is presently under.

The third register is the Requested Sector Register. This register should be loaded with the desired Sector prior to the issuance of a Read or Write Sector Instruction.

The fourth register is the Data Register. This register is used to hold the requested Track during a Seek Instruction. It could also be used for read or write data bytes during Read or Write Sector Instructions. The way the hardware of the Digital Group Double Density Controller is setup, this data transfer operation will be done through the Wait Port which is actually this register but with wait states added.

Keep this information in mind when you read the 1791 Product Specification Section.

5.2 1791 PRODUCT SPECIFICATION

CHAPTER 6

SAMPLE DRIVER PROGRAM

6.1 INTRODUCTION

The Digital Group Double Density Disc Controller Sample Driver has three entry points used by the calling program.

The INITialization routine (INIT) fills the Drive Attribute Table and restores all drives that are present to Track 0. This routine should be called upon powerup and whenever a Drive Attribute change is made.

In DISKMON V3.00, INIT is called every time the system is restarted through location 340 000.

In OASIS V5.3D, a variation of this routine reinitializes only the drive specified in a 'MOUNT' or 'ATTACH' Command.

You can assume that the INIT Routine destroys all registers.

The Read Block(s) Routine (DSKRD) reads a specified number of blocks starting at the START BLOCK into memory. On entry the registers should be:

```
 A= UNIT NUMBER
BC= BLOCK COUNT (256 Bytes/Block)
DE= START BLOCK (0 through Maximum-1)
HL= START BUFFER ADDRESS
```

On a good read the registers are:

```
 A= 0  (Zero Flag=1)
BC= UNKNOWN
DE= LAST TRACK AND SECTOR READ
HL= START BUFFER ADDRESS
```

On a bad read the registers are:

```
 A= ERROR CODE (Zero Flag=0)
BC= UNKNOWN
DE= TRACK AND SECTOR OF ERROR (For errors 3-6)
HL= START BUFFER ADDRESS
```

The Write Block(s) routine (DSKWRT) uses the same parameters as the Read Block(s) routine EXCEPT the direction of data is reversed.

The error codes returned to the calling program are as follows:

1. DRIVE NUMBER TOO LARGE
2. DRIVE NOT PRESENT
3. SEEK ERROR
4. BAD TRACK NUMBER
5. READ ERROR
6. WRITE ERROR

The user can get more information from the controller Status port on a Read or Write Error. If a Read or Write error occurs, the user should read the controller status register if he needs more information. The typical errors read from the Status register are:

2XX = DRIVE NOT READY
004 = DATA TRANSFER ERROR
006 = DATA TRANSFER ERROR
010 = DATA CRC ERROR
020 = RECORD NOT FOUND
030 = ID FIELD CRC ERROR

Any others signify controller hardware problems and should be expressed as such.

6.2 SAMPLE DRIVER CODE

```
                    1;          Sample Driver for the Digital Group Double Dens
                    2;          Controller using the LD  A,A Interrupt Scheme.
                    3;
                    4;          (C) 1979 by The Digital Group
                    5;
                    6;          Written by Larry Williams
                    7;          Last Revision 04/11/79
                    8;
                    9;
                    10;
                    11;         MAIN READ/WRITE LOOP
                    12;
                    13;         input:          output:       error output:
                    14;
                    15;         AF= Unit Number  AF=0  Z=1    AF= ERR CODE  Z=
                    16;         BC= Block Count  BC= Destroyed
                    17;         DE= Start Block  DE= Last Tr/Se
                    18;         HL= Buffer Start HL= Buffer Start
                    19;
                    20;
                    21;
0000 F5             22 DSKWRT:  PUSH AF         ; Save the Unit Number
0001 F680           23          OR   200Q       ; Set top bit for Write
0003 1802           24          JR   RDWRA      ; Go around read entry Point
0005 F5             25 DSKRD:   PUSH AF         ; Save the Unit Number
0006 97             26          SUB  A          ; get zero for read
0007 32F501         27 RDWRA:   LD   (RDWR),A   ; Save the Read/Write Flag
```

```
000A F3          28              DI                  ; disable further interrupts
000B ED46        29              IM0                 ; Set to 8080 type interrupt
000D F1          30              POP  AF             ; Get the Unit Number back
000E DDE5        31              PUSH IX             ; Save IX in case used.
0010 DD2AF301    32              LD   IX,(UNITPTR)   ; Get current unit pointer
0014 E5          33              PUSH HL             ; Save Buffer address on stack
0015 EB          34              EX   DE,HL          ; Get Start Record Number to H
0016 50          35              LD   D,B            ; Upper half of Bolcks to D
0017 59          36              LD   E,C            ; Lower half of blocks to E
0018 CDBA00      37              CALL SETUP          ; Select the unit convert Tr/S
001B 2028        38              JR   NZ,ERROR1      ; Nonzero is a error
001D CD0C01      39 RDWRB:       CALL SEEK           ; get to the right track
0020 2023        40              JR   NZ,ERROR1      ; nonzero is error
0022 E3          41              EX   (SP),HL        ; get addr to HL blocks to (sp
0023 D5          42              PUSH DE             ; Save Tracke and sectors
0024 3AF501      43              LD   A,(RDWR)       ; Get read/write flag
0027 07          44              RLCA                ; put bit 7 into carry
0028 F5          45              PUSH AF             ; save flags
0029 D46F01      46              CALL NC,READS       ; Read if no carry
002C 2015        47              JR   NZ,ERROR3      ; error exit if nonzero
002E F1          48              POP  AF             ; get flags back
002F DC9A01      49              CALL C,WRITES       ; it is write if carry
0032 2010        50              JR   NZ,ERROR2      ; error exit if nonzero
0034 D1          51              POP  DE             ; get Track and sector back
0035 E3          52              EX   (SP),HL        ; trade blocks in HL for mem a
0036 2B          53              DEC  HL             ; one less block
0037 7C          54              LD   A,H            ; top half blocks to A
0038 B5          55              OR   L              ; see if H=L=0
0039 280A        56              JR   Z,ERROR1       ; zero is OK no error exit
003B CD5A01      57              CALL INCSEC         ; get the next sector number
003E 28DD        58              JR   Z,RDWRB        ; no errors get another sector
0040 E3          59              EX   (SP),HL        ; get mem adr back to HL
0041 1802        60              JR   ERROR1         ; error exit with nonzero
                 61;
                 62;
0043 E1          63 ERROR3:      POP  HL             ; get RDWR flag off stack
0044 D1          64 ERROR2:      POP  DE             ; get Track and Sector back
0045 E1          65 ERROR1:      POP  HL             ; get back real HL
0046 DDE1        66              POP  IX             ; and IX
0048 F5          67              PUSH AF             ; save error code if any
0049 DB2C        68              IN   A,(SEL)        ; get unit number
004B E66F        69              AND  157Q           ; mask off interrupt en bit
004D D32C        70              OUT  (SEL),A        ; disable board interrupts
004F F1          71              POP  AF             ; get error code back if any
0050 C9          72              RET                 ; Go back to calling routine
                 73;
                 74;
                 75;
                 76;
                 77;
                 78;             INITIALIZE ROUTINE
                 79;
```

```
                80; This routine initializes all parameters in the Disc
                81; Parameter table. It should be called upon powerup and any
                82; time the user wishes to change Drive Attributes.
                83;
                84;
0051 0600       85 INIT:    LD   B,0          ; start with drive 0
0053 DD21DA01   86          LD   IX,DS0       ; first table entry
0057 DDE5       87          PUSH IX           ; save it for later also
0059 78         88 INITA:   LD   A,B          ; get drive number to A
005A D32C       89          OUT  (SEL),A      ; select that drive
005C DB2C       90          IN   A,(SEL)      ; get Attributes for that driv
005E CB57       91          BIT  2,A          ; see if Side came back zero
0060 DD3605FF   92          LD   (IX+5),0FFH  ; set no drive there to be sur
0064 203D       93          JR   NZ,INITX     ; of came back one...no drive
0066 CB6F       94          BIT  5,A          ; Single Density ? One=S.D.
0068 2E80       95          LD   L,128D       ; Single Density Sector length
006A 2002       96          JR   NZ,INITB     ; Brif Single Density
006C 2E00       97          LD   L,0          ; Double Density Length (256)
006E DD7504     98 INITB:   LD   (IX+4),L     ; save sector length in table
0071 1605       99          LD   D,STDSTEP    ; step rate for Standard Drive
0073 211A4D     100         LD   HL,STDTRSE   ; Standard Tracks and Sectors
0076 CB67       101         BIT  4,A          ; See if Standard or Mini
0078 280B       102         JR   Z,INITC      ; zero is Standard Drive
007A 1604       103         LD   D,MINSTEP    ; step rate Mini Drive
007C 211228     104         LD   HL,MINI1SID  ; One Sided MINI Track and Sec
007F CB5F       105         BIT  3,A          ; see if 2 sided Mini
0081 2802       106         JR   Z,INITC      ; Brif only 1 Sided
0083 2623       107         LD   H,MINI2SID   ; 2 sided Mini is Different
0085 DD7401     108 INITC:  LD   (IX+1),H     ; Save Number of Tracks
0088 CB5F       109         BIT  3,A          ; Check for 2 sided again
008A 2802       110         JR   Z,INITD      ; 1 sided branches
008C CB25       111         SLA  L            ; double sectors for 2 sided
008E DD7500     112 INITD:  LD   (IX+0),L     ; save maximum Sectors
0091 DD7702     113         LD   (IX+2),A     ; Save copy of Attribute Bits
0094 DD7203     114         LD   (IX+3),D     ; Save step rate
0097 78         115 INITR:  LD   A,B          ; get Unit number back in A
0098 F608       116         OR   DRICHG       ; or in the drive change bit
009A D32C       117         OUT  (SEL),A      ; select the drive again
009C CDC501     118         CALL RESTORE      ; Get this drive to Track Zero
009F DD360500   119         LD   (IX+5),0     ; set current track to zero
00A3 110600     120 INITX:  LD   DE,6          ; the table increment
00A6 DD19       121         ADD  IX,DE        ; add in the increment
00A8 04         122         INC  B            ; get to next drive
00A9 CB50       123         BIT  2,B          ; got to four yet ?
00AB 28AC       124         JR   Z,INITA      ; no go test another
00AD 97         125         SUB  A            ; get a zero in A
00AE 32F201     126         LD   (UNIT),A     ; set current unit as zero
00B1 D32C       127         OUT  (SEL),A      ; make sure controller matches
00B3 DDE1       128         POP  IX           ; get DS0 pointer back
00B5 DD22F301   129         LD  (UNITPTR),IX  ; save current unit pointer
00B9 C9         130         RET               ; done initializing all avail
                131;
```

```
                132;
                133;
                134;           SETUP ROUTINE
                135;
                136; This routine checks drive validity first, then changes
                137; drives if required. Lastly, it converts block number and
                138; start block to number of sectors and startng sector.
                139;
                140;
                141;
00BA FE04       142 SETUP:     CP    4              ; see if valid drive
00BC 3804       143            JR    C,SETUPA       ; carry is ok
00BE 3E01       144            LD    A,1            ; INVALID DRIVE NUMBER
00C0 B7         145            OR    A              ; set nonzero
00C1 C9         146            RET                  ; go back with error
00C2 E5         147 SETUPA:    PUSH  HL             ; save start record
00C3 21F201     148            LD    HL,UNIT        ; see if same drive
00C6 BE         149            CP    (HL)           ; zero is same drive
00C7 2816       150            JR    Z,SETUPC       ; don't mess with unitptr
00C9 D5         151            PUSH  DE             ; save blocks for a moment
00CA 77         152            LD    (HL),A         ; save new unit number
00CB F608       153            OR    DRICHG         ; or in the drive change bit
00CD D32C       154            OUT   (SEL),A        ; change the controller to new
00CF E603       155            AND   3              ; get back fresh unit number
00D1 DD21D401   156            LD    IX,DS0-6       ; table base address less 6
00D5 110600     157            LD    DE,6           ; table increment
00D8 3C         158            INC   A              ; for once thru the loop for s
00D9 DD19       159 SETUPB:    ADD   IX,DE          ; add in the table increment
00DB 3D         160            DEC   A              ; for each unit number
00DC 20FB       161            JR    NZ,SETUPB      ; not done until unit is zero
00DE D1         162            POP   DE             ; get blocks back
00DF DD22F301   163 SETUPC:    LD  (UNITPTR),IX     ; current unit ptr
00E3 DD7E05     164            LD    A,(IX+5)       ; get current track for this u
00E6 D329       165            OUT   (TRACK),A      ; update the controller
00E8 3C         166            INC   A              ; see if was 0FFH
00E9 2005       167            JR    NZ,SETUPD      ; unit is there branch
00EB 3E02       168            LD    A,2            ; NO DRIVE PRESENT
00ED B7         169            OR    A              ; set nonzero
00EE E1         170            POP   HL             ; get start record back
00EF C9         171            RET                  ; go back with error
00F0 E1         172 SETUPD:    POP   HL             ; get starting block back
00F1 DDCB026E   173            BIT   5,(IX+2)       ; see if double density
00F5 2804       174            JR    Z,SETUPE       ; if double no add needed
00F7 29         175            ADD   HL,HL          ; double start block for secto
00F8 EB         176            EX    DE,HL          ; swap around
00F9 29         177            ADD   HL,HL          ; double blocks for sectors
00FA EB         178            EX    DE,HL          ; get back in order
00FB 97         179 SETUPE:    SUB   A              ; get a zero
00FC 47         180            LD    B,A            ; into B also
00FD DD4E00     181            LD    C,(IX+0)       ; get number od sectors
0100 ED42       182 DIVIDE:    SBC   HL,BC          ; divide start block by secto
0102 3C         183            INC   A              ; new track
```

```
0103 30FB       184             JR    NC,DIVIDE    ; not done until overfolw
0105 09         185             ADD   HL,BC        ; get remainder back
0106 3D         186             DEC   A            ; for extra time thru loop
0107 2C         187             INC   L            ; sectors start at one
0108 67         188             LD    H,A          ; track to H
0109 EB         189             EX    DE,HL        ; put tr/se in DE blocks in HL
010A 1858       190             JR    SETUPX       ; setup exit code shared by ot
                191;
                192;
                193;
                194;            SEEK ROUTINE
                195;
                196;
                197; The seek routine gets the head of the selected drive to
                198; the correct track. It then performs the logical to
                199; physical sector mapping if 2 sided.
                200;
                201;
                202;
010C DB29       203 SEEK:       IN    A,(TRACK)    ; Get current track
010E BA         204             CP    D            ; same as requested ?
010F 2824       205             JR    Z,SEEKD      ; Brif same
0111 ED4BF501   206             LD    BC,(RTRY-1)  ; get retry count into B
0115 7A         207 SEEKA:      LD    A,D          ; get requested track to A
0116 D32B       208             OUT   (DATA),A     ; put to controller
0118 DD7E03     209             LD    A,(IX+3)     ; get the step rate
011B F618       210             OR    SEEKCOM      ; or in the seek command
011D D328       211             OUT   (CMND),A     ; issue seek command
011F DB2C       212 SEEKB:      IN    A,(SEL)      ; wait for completion (bit 7)
0121 87         213             ADD   A            ; into carry
0122 30FB       214             JR    NC,SEEKB     ; not done if no carry
0124 DB28       215             IN    A,(STAT)     ; get status of completed seek
0126 E618       216             AND   SEEKMASK     ; mask only wanted bits
0128 280B       217             JR    Z,SEEKD      ; zero is good seek
012A 3E03       218             LD    A,3          ; SEEK ERROR
012C 1002       219             DJNZ  SEEKC        ; go to seekc if retrys left
012E B7         220             OR    A            ; set nonzero
012F C9         221             RET                ; nonzero error exit
0130 CDC501     222 SEEKC:      CALL  RESTORE      ; get home for reference
0133 18E0       223             JR    SEEKA        ; try all over again
0135 DDCB025E   224 SEEKD:      BIT   3,(IX+2)     ; see if 2 sided
0139 4B         225             LD    C,E          ; put sector in C
013A 0680       226             LD    B,BOTMASK    ; interrupt and side mask in B
013C 280D       227             JR    Z,NOTTOP     ; Brif NOT 2 sided
013E DD7E00     228             LD    A,(IX+0)     ; get maximum sectors
0141 0F         229             RRCA               ; divide them by 2
0142 BB         230             CP    E            ; still on bottom ?
0143 3006       231             JR    NC,NOTTOP    ; if no carry still on bottom
0145 4F         232             LD    C,A          ; save dividing line for top/b
0146 7B         233             LD    A,E          ; get oversized sector in A
0147 91         234             SUB   C            ; subtract dividing line secto
0148 4F         235             LD    C,A          ; put new sector in C
```

```
0149 0684      236            LD   B,TOPMASK    ; interrupt and new side mask
014B DB2C      237 NOTTOP:    IN   A,(SEL)      ; get unit number in A
014D E603      238            AND  3            ; mask unwanted bits
014F B0        239            OR   B            ; or in interrupt and side inf
0150 D32C      240            OUT  (SEL),A      ; enable interrupts and put si
0152 79        241            LD   A,C          ; get the sector number
0153 D32A      242            OUT  (SECTOR),A   ; to controller
0155 DD7205    243            LD   (IX+5),D     ; save new current track numbe
0158 97        244 SEEKXA:    SUB  A            ; get a zero
0159 C9        245            RET               ; shared return code
               246;
               247;
               248;
               249;           INCREMENT SECTOR ROUTINE
               250;
               251;
               252; The increment sector routine bumps the sector by one and
               253; checks for overflow. If overflow exists, track is
               254; incremented and then checked for out of bounds.
               255;
               256;
               257;
015A DD7E00    258 INCSEC:    LD   A,(IX+0)     ; get maximum sectors to A
015D 1C        259            INC  E            ; for next sector
015E 93        260            SUB  E            ; (max sector-sector)
015F 30F7      261            JR   NC,SEEKXA    ; good number exit with a zero
0161 1E01      262            LD   E,1          ; bumped past start this 1 aga
0163 14        263 INCSED:    INC  D            ; next track
0164 DD7E01    264 SETUPX:    LD   A,(IX+1)     ; get max tracks
0167 3D        265            DEC  A            ; for 0 to max-1 not 1 to max
0168 92        266            SUB  D            ; see if overflow
0169 30ED      267            JR   NC,SEEKXA    ; good number exit with a zero
016B 3E04      268            LD   A,4          ; BAD TRACK NUMBER
016D B7        269            OR   A            ; set nonzero
016E C9        270            RET               ; return from INCSEC or SETUP
               271;
               272;
               273;
               274;           READ SINGLE SECTOR ROUTINE
               275;
               276; The read single sector routine reads a single sector and
               277; then returns. Based on the following:
               278;
               279;           input:             output: error output:
               280;           AF= don't Care     AF=0 Z=1        AF=err Z=0
               281;           BC= don't Care     BC= Destroyed
               282;           DE= Tr/Se          DE= Tr/Se
               283;           HL= buffer addr    HL= buffer+lengh HL= buffer ad
               284;
               285;
               286;
016F ED5BF601  287 READS:     LD   DE,(RTRY)    ; get retry count to E
```

```
0173 E5          288 READA:    PUSH HL           ; save buffer start address
0174 3E88        289           LD   A,READCOM    ; get the read sector command
0176 D328        290           OUT  (CMND),A     ; issue to controller
0178 0E2F        291           LD   C,WAIT       ; wait port number to C
017A DD4604      292           LD   B,(IX+4)     ; sector length to B
017D FB          293 READB:    EI                ; enable interrupts
017E 76          294           HALT              ; refresh until first byte rea
017F EDB2        295           INIR              ; get all the bytes to memory
0181 DB2C        296 READC:    IN   A,(SEL)      ; get completion flag (bit 7)
0183 87          297           ADD  A            ; into carry
0184 3802        298           JR   C,READD      ; when done carry is one
0186 10F9        299           DJNZ READC        ; wait only 256 times for flag
0188 DB28        300 READD:    IN   A,(STAT)     ; get read sector status
018A E69F        301           AND  READMASK     ; mask only wanted bits
018C 2808        302           JR   Z,RDWRX      ; if no errors use common exit
018E 1D          303           DEC  E            ; retry again ?
018F E1          304           POP  HL           ; get start buffer address
0190 20E1        305           JR   NZ,READA     ; if nonzero retry
0192 3E05        306           LD   A,5          ; READ ERROR
0194 B7          307           OR   A            ; get nonzero
0195 C9          308           RET               ; go back with error
                 309;
0196 E3          310 RDWRX:    EX   (SP),HL      ; swap buffer+length for buffe
0197 E1          311           POP  HL           ; get incremented in HL
0198 97          312           SUB  A            ; get a zero
0199 C9          313           RET               ; return from READS or WRITES
                 314;
                 315;
                 316;
                 317;          WRITE SINGLE SECTOR ROUTINE
                 318;
                 319; The Write single sector routine uses the same structure
                 320; as the read sector routine.
                 321;
                 322;
019A ED5BF601    323 WRITES:   LD   DE,(RTRY)    ; get retry count to E
019E E5          324 WRITEA:   PUSH HL           ; save start buffer address
019F 3EA8        325           LD   A,WRITECOM   ; get the write sector command
01A1 D328        326           OUT  (CMND),A     ; issue it to the controller
01A3 0E2F        327           LD   C,WAIT       ; get the wait port to C
01A5 DD4604      328           LD   B,(IX+4)     ; get the sector length
01A8 FB          329 WRITEB:   EI                ; enable interrupts
01A9 76          330           HALT              ; refresh until first byte nee
01AA EDA3        331           OUTI              ; put the first byte
01AC FB          332           EI                ; enable interrupts again
01AD 76          333           HALT              ; refresh until rest needed
01AE EDB3        334           OTIR              ; write the rest of the sector
01B0 DB2C        335 WRITEC:   IN   A,(SEL)      ; wait for crc write
01B2 87          336           ADD  A            ; completion flag into carry
01B3 3802        337           JR   C,WRITED     ; if complete Branch
01B5 10F9        338           DJNZ WRITEC       ; only wait 256 for completion
01B7 DB28        339 WRITED:   IN   A,(STAT)     ; get write sector status
```

```
01B9 E69F       340             AND   WRITMASK     ; mask only wanted bits
01BB 28D9       341             JR    Z,RDWRX      ; if zero no errors use com ex
01BD 1D         342             DEC   E            ; retry again ?
01BE E1         343             POP   HL           ; get start buffer address
01BF 20DD       344             JR    NZ,WRITEA    ; no try again
01C1 3E06       345             LD    A,6          ; WRITE ERROR
01C3 B7         346             OR    A            ; set nonzero
01C4 C9         347             RET                ; go back with error
                348;
                349;
                350;
                351;            RESTORE ROUTINE
                352;
                353; This routine gets the selected drive back to track zero.
                354; It also updates the current track pointer.
                355;
                356;
01C5 DD7E03     357 RESTORE:    LD    A,(IX+3)     ; Get the step rate
01C8 E603       358             AND   3            ; remove the verify bit if set
01CA F608       359             OR    RESTCOM      ; or in the restore command
01CC D328       360             OUT   (CMND),A     ; issue the restore to control
01CE DB2C       361 RESTA:      IN    A,(SEL)      ; get completion bit
01D0 87         362             ADD   A            ; into carry
01D1 30FB       363             JR    NC,RESTA     ; not done until carry
01D3 DD360500   364             LD    (IX+5),0     ; update the current track poi
01D7 DB28       365             IN    A,(STAT)     ; read to clear the completion
01D9 C9         366             RET                ; just return no error checkin
                367;
                368;
                369;
                370;            DRIVE PARAMETER TABLES
                371;
                372;
                373;
01DA 00         374 DS0:        DC    0            ; MAXIMUM SECTOR   DRIVE 0
01DB 00         375             DC    0            ; MAXIMUM TRACK    DRIVE 0
01DC 00         376             DC    0            ; ATTRIBUTE FLAGS  DRIVE 0
01DD 00         377             DC    0            ; STEP RATE        DRIVE 0
01DE 00         378             DC    0            ; SECTOR LENGTH    DRIVE 0
01DF FF         379             DC    0FFH         ; CURRENT TRACK    DRIVE 0
01E0 00000000   380 DS1:        DC    0,0,0,0,0,0FFH ; DRIVE 1
01E6 00000000   381 DS2:        DC    0,0,0,0,0,0FFH ; DRIVE 2
01EC 00000000   382 DS3:        DC    0,0,0,0,0,0FFH ; DRIVE 3
                383;
01F2 00         384 UNIT:       DC    0            ; CURRENT UNIT NUMBER
01F3 DA01       385 UNITPTR:    DC    (DS0)        ; CURRENT UNIT TABLE POINTER
                386;
01F5 00         387 RDWR:       DC    0            ; READ/WRITE COMMAND STORAGE
01F6 0200       388 RTRY:       DC    (2)          ; RETRY COUNT
                389;
                390;
                391;
```

```
                392;            SYSTEM EQUATES
                393;
                394;
                395;
0028            396 PORT:       EQU   050Q          ; BASE ADDRESS OF CONTROLLER
0028            397 STAT:       EQU   PORT          ; CONTROLLER STATUS PORT
0028            398 CMND:       EQU   PORT          ; CONTROLLER COMMAND PORT
0029            399 TRACK:      EQU   PORT+1        ; CONTROLER CURRENT TRACK PORT
002A            400 SECTOR:     EQU   PORT+2        ; CONTROLLER REQUESTED SECTOR
002B            401 DATA:       EQU   PORT+3        ; CONTROLLER DATA PORT
002C            402 SEL:        EQU   PORT+4        ; SELECT AND STATUS PORT
002F            403 WAIT:       EQU   PORT+7        ; CONTROLLER WAIT DATA PORT
4D1A            404 STDTRSE:    EQU   77*256+26     ; STANDARD TRACKS AND SECTORS
2812            405 MINI1SID:   EQU   40*256+18     ; MINI 1SIDED TRACK AND SECTOR
0023            406 MINI2SID:   EQU   35            ; MINI 2SIDED TRACKS
0018            407 SEEKCOM:    EQU   030Q          ; CONTROLLER SEEK COMMAND
0008            408 RESTCOM:    EQU   010Q          ; CONTROLLER RESTORE COMMAND
0088            409 READCOM:    EQU   210Q          ; CONTROLLER READ SECTOR COMMA
00A8            410 WRITECOM:   EQU   250Q          ; CONTROLLER WRITE SECTOR COMM
009F            411 READMASK:   EQU   237Q          ; CONTROLLER READ ERROR MASK
009F            412 WRITMASK:   EQU   237Q          ; CONTROLLER WRITE ERROR MASK
0018            413 SEEKMASK    EQU   030Q          ; CONTROLLER SEEK ERROR MASK
0005            414 STDSTEP:    EQU   5             ; STANDARD DRIVE STEP RATE
0004            415 MINSTEP:    EQU   4             ; MINI DRIVE STEP RATE (MPI)
0008            416 DRICHG:     EQU   10Q           ; DRIVE CHANGE BIT
0080            417 BOTMASK:    EQU   200Q          ; INTERRUPT ENABLE AND BOTTOM
0084            418 TOPMASK:    EQU   204Q          ; INTERRUPT ENABLE AND TOP MAS
0000            419             END                 ; thats all folks
```

CHAPTER 7

SAMPLE FORMAT PROGRAM

7.1 INTRODUCTION

The Format Program is a callable Subroutine that formats a diskette. On entry the accumulator contains the drive number (0-3). No prompt message is given to avoid clobbering drive 0. There is no error exit and the Format routine assumes that the calling program has verified that the drive actually exists.

A track is formatted by first arranging all the bytes for that track in memory first. This includes all Gap, ID, and Data Fields. The track is then written to the disc during a single revolution.

For Double Density Standard drives, this track buffer is 11K bytes long. Therefore, to run the Format Program, the user requires at least 11.25K bytes of continuous memory PLUS whatever memory the calling program requires.

The Format Program for DISKMON V3.00 is the same as the sample Format Program except that there is a front end for swap messages for drive zero.

The Format Program for OASIS V5.3D uses the same table driven formatter, but is more extensive (more Bells and Whistles) than the sample Format Program.

7.2 FORMAT CODE

```
                    1 ;
                    2 ;
                    3 ;Sample Format Program for the Digital Group
                    4 ;Double Density Controller Board
                    5 ;
                    6 ;(C) 1979 by The Digital Group
                    7 ;
                    8 ;Written by:
                    9 ;Larry Williams
                   10 ;
                   11 ;
                   12 ;
0000 FE04          13 FORMAT:   CP   4          ; be sure its a valid drive
0002 D0            14           RET  NC         ; go back if GE 4
0003 F610          15           OR   DRICHG     ; flip drive change bit
0005 D32C          16           OUT  (SEL),A    ; select the desired drive
0007 DB2C          17           IN   A,(SEL)    ; get back the attributes
                   18 ;
                   19 ; Mini INIT routine to find max tracks and sectors
                   20 ;
```

```
0009 211A4D    21 INIT:     LD   HL,STDTRSE ; get standard track and sector
000C CB67      22           BIT  4,A        ; see if standard
000E 2809      23           JR   Z,INITA    ; Brif standard
0010 211228    24           LD   HL,MINI1SI ; get Mini 1sided track and sect
0013 CB5F      25           BIT  3,A        ; see if 2 sided
0015 2802      26           JR   Z,INITA    ; Brif 1 sided
0017 2623      27           LD   H,MINI2SI  ; tracks different for 2 sided
0019 32DB01    28 INITA:    LD   (ATTR),A   ; save the attributes
001C 2C        29           INC  L          ; get one extra sector
001D 22D701    30           LD   (NSECTS),HL ; save the tracks and sectors
0020 21DC01    31           LD   HL,GAPTAB  ; get gaptable address's
0023 E630      32           AND  60Q        ; mask only S/D and M/S
0025 CB2F      33           SRA  A          ; divide by 2
0027 CB2F      34           SRA  A          ; divide by 2
0029 0600      35           LD   B,0        ; get upper half to zero
002B 4F        36           LD   C,A        ; get lower half from A
002C 09        37           ADD  HL,BC      ; add in offset
002D 5E        38           LD   E,(HL)     ; get lower half of gaptab
002E 23        39           INC  HL         ; for next
002F 56        40           LD   D,(HL)     ; get upper half of gaptab
0030 EB        41           EX   DE,HL      ; put gaptab in hl
0031 22D301    42           LD   (TEMP2),HL ; save gaptab addr in temp2
0034 EB        43           EX   DE,HL      ; get offset back in HL
0035 23        44           INC  HL         ; for next
0036 5E        45           LD   E,(HL)     ; get lower half of sectab
0037 23        46           INC  HL         ; for next
0038 56        47           LD   D,(HL)     ; get upper half of sectab
0039 EB        48           EX   DE,HL      ; sectab addr in HL
003A 22D501    49           LD   (TEMP1),HL ; save sectab addr in temp1
003D ED62      50           SBC  HL,HL      ; get pair of zeros
003F 22D901    51           LD   (SIDE),HL  ; zero side and track temps
0042 EB        52           EX   DE,HL      ; get a zero to D
0043 CDED00    53 FORMC:    CALL RESTORE    ; get this drive to track 0
0046 D5        54 FORMD:    PUSH DE         ; save current track
0047 CD8800    55           CALL FORMIN     ; format the buffer
004A CDCC00    56           CALL WRITETR    ; write the buffer
004D D1        57           POP  DE         ; get current track back
004E 14        58           INC  D          ; for next track
004F 3AD801    59           LD   A,(NTRKS)  ; get maximum tracks
0052 BA        60           CP   D          ; see if done
0053 2811      61           JR   Z,FORMX    ; done with one side
0055 7A        62 SEEK:     LD   A,D        ; get the new track
0056 D32B      63           OUT  (DATA),A   ; to controller
0058 32DA01    64           LD   (TRACKS),A ; save it for formatting
005B 3E1B      65           LD   A,SEEKCOM  ; slow seek with no verify
005D D328      66           OUT  (CMND),A   ; issue the command
005F DB2C      67 SEEKA:    IN   A,(SEL)    ; wait for completion (bit 7)
0061 87        68           ADD  A          ; into carry
0062 30FB      69           JR   NC,SEEKA   ; no carry is not done
0064 18E0      70           JR   FORMD      ; go for another track
               71 ;
               72 ;
```

```
0066 3AD901     73 FORMX:    LD   A,(SIDE)    ; see if just formatted top
0069 B7         74           OR   A           ; see if a one
006A 2018       75           JR   NZ,FORMXX   ; if one were all done
006C 3ADB01     76           LD   A,(ATTR)    ; get attributes again
006F CB5F       77           BIT  3,A         ; see if realy 2 sided
0071 2811       78           JR   Z,FORMXX    ; if 1 sided we have to be done
0073 DB2C       79           IN   A,(SEL)     ; get device number
0075 E603       80           AND  3           ; mask out all rest
0077 F604       81           OR   4           ; or in top side
0079 D32C       82           OUT  (SEL),A     ; select top side
007B 3E01       83           LD   A,1         ; new side
007D 32D901     84           LD   (SIDE),A    ; save it in the side temp
0080 1600       85           LD   D,0         ; start with track zero again
0082 18BF       86           JR   FORMC       ; go restore and then format
                87 ;
                88 ;
0084 CDED00     89 FORMXX:   CALL RESTORE     ; get the drive back to track 0
0087 C9         90           RET              ; go back to calling program
                91 ;
                92 ;
                93 ;
                94 ;Track data generation routine
                95 ;
0088 0E01       96 FORMIN:   LD   C,1         ; loop count
008A 2AD301     97           LD   HL,(TEMP2)  ; get gaptab address
008D 11EC01     98           LD   DE,BUFFER   ; the track format buffer
0090 FD2AD501   99           LD   IY,(TEMP1)  ; IY is the sectab pointer
0094 CDBF00     100          CALL PUTIT       ; put Gap4b into buffer
0097 E5         101 FORML:   PUSH HL          ; save the start of sectors
0098 CDBF00     102          CALL PUTIT       ; put Gap3 into buffer
                103 ;
                104 ; Fill The ID field
                105 ;
009B 3ADA01     106          LD   A,(TRACKS)  ; get the current track number
009E 12         107          LD   (DE),A      ; into buffer
009F 13         108          INC  DE          ; for next
00A0 3AD901     109          LD   A,(SIDE)    ; get the current side number
00A3 12         110          LD   (DE),A      ; into buffer
00A4 13         111          INC  DE          ; for next
00A5 FD7E00     112          LD   A,(IY+0)    ; get the mapped sector
00A8 12         113          LD   (DE),A      ; into buffer
00A9 FD23       114          INC  IY          ; for next sector
00AB 13         115          INC  DE          ; for next
00AC CDBF00     116          CALL PUTIT       ; put rest of ID and DATA field
                117 ;
                118 ;
00AF 0C         119          INC  C           ; next sector
00B0 3AD701     120          LD   A,(NSECTS)  ; get max sectors+1
00B3 B9         121          CP   C           ; same ?
00B4 2803       122          JR   Z,FORMIX    ; done with data field if zero
00B6 E1         123          POP  HL          ; get pointer back to Gap3
00B7 18DE       124          JR   FORML       ; go for another sector
```

```
00B9 E3          125 FORMIX:  EX   (SP),HL     ; throw away top entry on stack
00BA E1          126          POP  HL          ; like this
00BB CDBF00      127          CALL PUTIT       ; now format Gap4a to index hole
00BE C9          128          RET              ; done with a track
                 129 ;
                 130 ;
                 131 ;        Putit routine
                 132 ;
                 133 ;Gets byte pairs from Gaptab. First byte is count
                 134 ;and second byte is value. If both are zero, stop.
                 135 ;
00BF 46          136 PUTIT:   LD   B,(HL)      ; get repeat count
00C0 23          137          INC  HL          ; for second byte
00C1 7E          138          LD   A,(HL)      ; get value
00C2 23          139          INC  HL          ; for next
00C3 80          140          ADD  B           ; see if both zero
00C4 C8          141          RET  Z           ; go back if both zero
00C5 90          142          SUB  B           ; restore value
00C6 12          143 LOOPIT:  LD   (DE),A      ; start putting the value
00C7 13          144          INC  DE          ; for next
00C8 10FC        145          DJNZ LOOPIT      ; until B is zero
00CA 18F3        146          JR   PUTIT       ; go for another byte pair
                 147 ;
                 148 ;
                 149 ;        Write Track routine
                 150 ;
                 151 ;Writes 11,000 bytes to drive whether or not the
                 152 ;drive requires that many.
                 153 ;
                 154 ;
00CC 012F00      155 WRITETR: LD   BC,WAIT     ; wait port to C
00CF 21EC01      156          LD   HL,BUFFER   ; where the data is
00D2 112BC0      157          LD   DE,MASK     ; data ready mask and loop count
00D5 3EF4        158          LD   A,WTRKCOM   ; the write track command
00D7 D328        159          OUT  (CMND),A    ; issue to controller
00D9 DB2C        160 WRITEA:  IN   A,(SEL)     ; wait for first byte
00DB A2          161          AND  D           ; see if ready
00DC 28FB        162          JR   Z,WRITEA    ; wait until first is ready
00DE EDA3        163          OUTI             ; put first byte
00E0 DB2C        164 WRITEB:  IN   A,(SEL)     ; wait for the rest
00E2 A2          165          AND  D           ; fast check
00E3 CAE000      166          JP   Z,WRITEB    ; faster that JR
00E6 EDB3        167 WRITEC:  OTIR             ; put a bunch of bytes
00E8 1D          168          DEC  E           ; 256 times E
00E9 C2E600      169          JP   NZ,WRITEC   ; not done yet
00EC C9          170          RET              ; put all bytes and then some
                 171 ;
                 172 ;
                 173 ;        Restore routine
                 174 ;
                 175 ;
00ED 3E0B        176 RESTORE: LD   A,RESTCOM   ; restore command
```

```
00EF D328       177           OUT   (CMND),A    ; to controller
00F1 DB2C       178 RESTA:    IN    A,(SEL)     ; wait for completion
00F3 87         179           ADD   A           ; into carry
00F4 30FB       180           JR    NC,RESTA    ; not done yet
00F6 DB28       181           IN    A,(STAT)    ; clear completion flag
00F8 C9         182           RET               ; go back
                183 ;
                184 ;
                185 ;
                186 ;
                187 ;         The Gap and Sector Tables
                188 ;
                189 ;All data following MUST be in this order !!!
                190 ;
                191 ;
00F9 0EFF0600   192 MINI:     DC    014,255,006,000,001,252,014,255,000,000
0103 08FF0600   193           DC    008,255,006,000,001,254,000,000,001,000
010D 01F70BFF   194           DC    001,247,011,255,006,000,001,251,128,229
0117 01F70000   195           DC    001,247,000,000,000,255,128,255,000,000
                196 ;
                197 ;
0121 1C4E0C00   198 MINID:    DC    028,078,012,000,003,246,001,252,028,078
012B 0000104E   199           DC    000,000,016,078,008,000,003,245,001,254
0135 00000101   200           DC    000,000,001,001,001,247,022,078,012,000
013F 03F501FB   201           DC    003,245,001,251,000,064,001,247,000,000
0149 004E004E   202           DC    000,078,000,078,000,000
                203 ;
                204 ;
014F 28FF0600   205 STD:      DC    040,255,006,000,001,252,026,255,000,000
0159 060001FE   206           DC    006,000,001,254,000,000,001,000,001,247
0163 0BFF0600   207           DC    011,255,006,000,001,251,128,229,001,247
016D 1BFF0000   208           DC    027,255,000,000,128,255,000,255,000,000
                209 ;
                210 ;
0177 504E0C00   211 STDD:     DC    080,078,012,000,003,246,001,252,050,078
0181 00000C00   212           DC    000,000,012,000,003,245,001,254,000,000
018B 010101F7   213           DC    001,001,001,247,022,078,012,000,003,245
0195 01FB0040   214           DC    001,251,000,064,001,247,054,078,000,000
019F 004E004E   215           DC    000,078,000,078,128,078,000,000
                216 ;
                217 ;
01A7 01020304   218 SECA:     DC    01,02,03,04,05,06,07,08,09,10,11,12,13
01B4 0E0F1011   219           DC    14,15,16,17,18,19,20,21,22,23,24,25,26
                220 ;
                221 ;
                222 ;
01C1 010A020B   223 SECB:     DC    01,10,02,11,03,12,04,13,05
01CA 0E060F07   224           DC    14,06,15,07,16,08,17,09,18
                225 ;
                226 ;         MUST BE IN THIS ORDER
                227 ;
01D3 0000       228 TEMP2:    DC    (0)         ; Gaptable pointer
```

```
01D5 0000       229 TEMP1:   DC   (0)          ; Sec table pointer
01D7 00         230 NSECTS:  DC   0            ; max sectors+1
01D8 00         231 NTRKS:   DC   0            ; max tracks
01D9 00         232 SIDE     DC   0            ; side
01DA 00         233 TRACKS:  DC   0            ; current track
01DB 00         234 ATTR:    DC   0            ; attribute bits
                235 ;
                236 ;
01DC 7701A701   237 GAPTAB:  DC   (STDD),(SECA),(MINID),(SECB)
01E4 4F01A701   238          DC   (STD),(SECA),(MINI),(SECB)
                239 ;
01EC            240 BUFFER:  EQU  $            ; write buffer starts here
                241 ;
                242 ;
                243 ;        System equates
                244 ;
                245 ;
0028            246 PORT:    EQU  050Q         ; controller base address
0028            247 STAT:    EQU  PORT         ; controller status port
0028            248 CMND:    EQU  PORT         ; controller command port
002B            249 DATA:    EQU  PORT+3       ; controller data port
002C            250 SEL:     EQU  PORT+4       ; select and side port
002F            251 WAIT:    EQU  PORT+7       ; data wait port
0010            252 DRICHG:  EQU  20Q          ; drive change bit
4D1A            253 STDTRSE: EQU  77*256+26    ; standard track and sector
2812            254 MINI1SI: EQU  40*256+18    ; mini track and sector 1 sided
0023            255 MINI2SI: EQU  35           ; mini track 2 sided
001B            256 SEEKCOM: EQU  33Q          ; seek slow no verify
000B            257 RESTCOM: EQU  13Q          ; restore slow no verify
00F4            258 WTRKCOM: EQU  364Q         ; write track command
C02B            259 MASK:    EQU  192*256+43   ; wait mask and loop count
0000            260          END               ;
```

APPENDIX A

PARTS LIST BY VALUE

DIGITAL GROUP DOUBLE DENSITY DISK CONTROLLER PARTS LIST

LABEL	DESCRIPTION	QUANTITY	PART #
IC19	7400 quad 2-input NAND	1	075-000
IC5	74LS00 quad 2-input NAND	1	075-046
IC16	74LS02 quad 2-input NOR	1	075-048
IC27,30,46,49	7404 hex inverter	4	075-004
IC21	7406 hex inverter O.C.	1	075-005
IC15	74LS08 quad 2-input AND	1	075-081
IC23	7408 quad 2-input AND	2	075-007
IC17	74LS14 hex inverter S.T.	1	075-075
IC14	7420 dual 4-input NAND	1	075-011
IC36	74LS27 triple 3-input NOR	1	075-071
IC32,48	7430 eight input NAND	2	075-012
IC18,31	7432 quad 2-input OR	2	075-013
IC38,39,40	7438 quad 2-input NAND O.C.	3	075-014
IC33	7442 binary to decimal conv.	1	075-016
IC2,7,20,24,35	7474 dual D Flip Flop	5	075-019
IC45	7475 quad latch	1	075-020
IC6	7486 quad Exclusive OR	1	075-021
IC1,4,25	74123 Dual One Shot (TI)	3	075-029
IC8	74S124 Dual VCO (TI)	1	075-076
IC28	74139 dual 2 to 4 Demult.	1	075-077
IC11	74153 dual 4 to 1 Mult.	1	075-034
IC10	74161 Binary counter	1	075-072
IC41	74175 quad D Latch	1	075-040
IC12,13	74LS221 dual One Shot (TI)	2	075-078
IC44	81LS95/97 Octal Buffer	1	075-074
IC42,43	81LS96/98 Octal Buffer Inv.	2	075-073
IC37	74367 Hex buffer	1	075-044
IC34	LM3302 quad Comparitor	1	078-006
IC3	NE555 Timer	1	078-002
IC9	LM741 Op Amp	1	078-004
IC22	LM318 Op Amp	1	078-015
IC29	FD1791-1 Controller IC	1	073-031
R42	47 Ohm 1/4w Resistor	1	001-006
R30,31	120 Ohm 1/4w Resistor	2	001-074
R12,13,14 R15,17	150 Ohm 1/4w Resistor	5	001-011
R22	270 Ohm 1/4w Resistor	1	001-015
R25	330 Ohm 1/4w Resistor	1	001-016
R33,37,49,50	470 Ohm 1/4w Resistor	4	001-018
R28,36,38	1K Ohm 1/4w Resistor	3	001-025
R9,18,19,20 R21,27,34,39	2.2K Ohm Resistor	8	001-029

LABEL	DESCRIPTION	QUANTITY	PART #
IC26	2.2K Ohm RPACK	1	008-002
R7	2.7K Ohm 1/4w Resistor	1	001-030
R44,45	3.3K Ohm 1/4w Resistor	2	001-052
R29	3.9K Ohm 1/4w Resistor	1	001-078
R43	4.7K Ohm 1/4w Resistor	1	001-032
R46	5.6K Ohm 1/4w Resistor	1	001-034
R6,10	6.8K Ohm 1/4w Resistor	2	001-035
R4	7.5K Ohm 1/4w Resistor	1	001-053
R8	9.1K Ohm 1/4w Resistor	1	001-054
R23,24,32,40 R41,47,48	10K Ohm 1/4w Resistor	7	001-037
R5	11K Ohm 1/4w Resistor	1	001-079
R2	15K Ohm 1/4w Resistor	1	001-039
R11	27K Ohm 1/4w Resistor	1	001-008
R1	33K Ohm 1/4w Resistor	1	001-041
R3	820K Ohm 1/4w Resistor	1	001-080
R35	5K 10 Turn Trim-Pot	1	005-013
C10,11,12,13 C14,34	50pf Silver Mica Capacitor	6	018-002
C53	36pf Silver Mica Capacitor	1	018-006
C66	180pf Silver Mica Capacitor	1	018-012
C52,74	220pf Silver Mica Capacitor	2	018-004
C65	680pf Silver Mica Capacitor	1	018-015
C32,54	1000pf Silver Mica Capacitor	2	018-000
C70,73	.01uf Disc Capacitor	2	014-002
C49,50	.01uf 10% Mylar Capacitor	2	016-028
C48	.022uf 10% Mylar Capacitor	1	016-029
C15	.022uf 10% Disc Capacitor	1	014-021
C40,42,43,68	4.7uf Tantalum Capacitor	4	010-002
C9,61,62,71	10uf Tantalum Capacitor	4	010-003
C16,39	22uf Tantalum Capacitor	2	010-008
C72	100uf Tantalum Capacitor	1	010-009
C1-8,17-31,33 C35-38,41,44-47 C51,55-60,63,64 C67,69,75	.1uf Disc Ceramic Capacitor	45	014-003
D1,3,4,5-20	1N4148 Diode	10	040-006
D2	1N4731A 4.3V Zener Diode	1	040-025

LABEL	DESCRIPTION	QUANTITY	PART #
X1	4.000 Mhz Crystal	1	030-011
L1	22uh Choke	1	055-004
	8 Pin Socket	7	060-000
	14 Pin Socket	27	060-001
	16 Pin Socket	14	060-002
	20 Pin Socket	3	060-013
	40 Pin Socket	1	060-006
	PC Board	1	090-078
	#30 Wire	3'	110-010
	#24 Solid Wire	1'	110-050
	System Manual	1	298-139
	Installation Manual	1	298-140
	Hmon/2 Users Manual	1	296-088
	Hmon/2 Cassette	1	299-917

CPU MODIFICATION KIT

R7	22K Ohm 1/4w Resistor	1	001-040
D1,D2,D3	1N4148 Diode	3	040-006
	#30 wire	2'	560-003

APPENDIX A

PARTS LIST BY LABEL

INTEGRATED CIRCUITS

LABEL	DESC	LABEL	DESC	LABEL	DESC
IC1	74123	IC18	7432	IC35	7474
IC2	7474	IC19	7400	IC36	74LS27
IC3	NE555	IC20	7474	IC37	74367
IC4	74123	IC21	7406	IC38	7438
IC5	74LS00	IC22	LM318	IC39	7438
IC6	7486	IC23	7408	IC40	7438
IC7	7474	IC24	7474	IC41	74175
IC8	74S124	IC25	74123	IC42	81LS96/98
IC9	LM741	IC26	2.2RP	IC43	81LS96/98
IC10	74161	IC27	7404	IC44	81LS95/97
IC11	74153	IC28	74139	IC45	7475
IC12	74LS221	IC29	1791-1	IC46	7404
IC13	74LS221	IC30	7404	IC47	NOT USED
IC14	7420	IC31	7432	IC48	7430
IC15	74LS08	IC32	7430	IC49	7404
IC16	74LS02	IC33	7442		
IC17	74LS14	IC34	LM3302		

RESISTORS

LABEL	DESC	LABEL	DESC	LABEL	DESC
R1	33K	R18	2.2K	R35	5K POT
R2	15K	R19	2.2K	R36	1K
R3	820K	R20	2.2K	R37	470
R4	7.5K	R21	2.2K	R38	1K
R5	11K	R22	270	R39	2.2K
R6	6.8K	R23	10K	R40	10K
R7	2.7K	R24	10K	R41	10K
R8	9.1K	R25	330	R42	47
R9	2.2K	R26	2.2RP	R43	4.7K
R10	6.8K	R27	2.2K	R44	3.3K
R11	27K	R28	1K	R45	3.3K
R12	150	R29	3.9K	R46	5.6K
R13	150	R30	120	R47	10K
R14	150	R31	120	R48	10K
R15	150	R32	10K	R49	470
R16	NOT USED	R33	470	R50	470
R17	150	R34	2.2K		

CAPACITORS

LABEL	DESC	LABEL	DESC	LABEL	DESC
C1	.1 uf	C26	.1 uf	C51	.1 uf
C2	.1 uf	C27	.1 uf	C52	220 pf
C3	.1 uf	C28	.1 uf	C53	36 pf
C4	.1 uf	C29	.1 uf	C54	1000 pf
C5	.1 uf	C30	.1 uf	C55	.1 uf
C6	.1 uf	C31	.1 uf	C56	.1 uf
C7	.1 uf	C32	1000 pf	C57	.1 uf
C8	.1 uf	C33	.1 uf	C58	.1 uf
C9	10 uf	C34	50 pf	C59	.1 uf
C10	50 pf	C35	.1 uf	C60	.1 uf
C11	50 pf	C36	.1 uf	C61	10 uf
C12	50 pf	C37	.1 uf	C62	10 uf
C13	50 pf	C38	.1 uf	C63	.1 uf
C14	50 pf	C39	22 uf	C64	.1 uf
C15	.022 uf	C40	4.7 uf	C65	680 pf
C16	22 uf	C41	.1 uf	C66	180 pf
C17	.1 uf	C42	4.7 uf	C67	.1 uf
C18	.1 uf	C43	4.7 uf	C68	4.7 uf
C19	.1 uf	C44	.1 uf	C69	.1 uf
C20	.1 uf	C45	.1 uf	C70	.01 uf
C21	.1 uf	C46	.1 uf	C71	10 uf
C22	.1 uf	C47	.1 uf	C72	100 uf
C23	.1 uf	C48	.022 uf	C73	.01 uf
C24	.1 uf	C49	.01 uf	C74	220 pf
C25	.1 uf	C50	.01 uf	C75	.1 uf

DIODES

LABEL	DESC	LABEL	DESC	LABEL	DESC
D1	1N4148	D5	1N4148	D9	1N4148
D2	1N4731A	D6	1N4148	D10	1N4148
D3	1N4148	D7	1N4148		
D4	1N4148	D8	1N4148		

IC SOCKETS

LABEL	DESC	LABEL	DESC	LABEL	DESC
IC1	16 Pin	IC19	14 Pin	IC37	16 Pin
IC2	14 Pin	IC20	14 Pin	IC38	14 Pin
IC3	8 Pin	IC21	14 Pin	IC39	14 Pin
IC4	16 Pin	IC22	8 Pin	IC40	14 Pin
IC5	14 Pin	IC23	14 Pin	IC41	16 Pin
IC6	14 Pin	IC24	14 Pin	IC42	20 Pin
IC7	14 Pin	IC25	16 Pin	IC43	20 Pin
IC8	16 Pin	IC26	16 Pin	IC44	20 Pin
IC9	8 Pin	IC27	14 Pin	IC45	16 Pin
IC10	16 Pin	IC28	16 Pin	IC46	14 Pin
IC11	16 Pin	IC29	40 Pin	IC47	NOT USED
IC12	16 Pin	IC30	14 Pin	IC48	14 Pin
IC13	16 Pin	IC31	14 Pin	IC49	14 Pin
IC14	14 Pin	IC32	14 Pin	IC50	8 Pin
IC15	14 Pin	IC33	16 Pin	IC51	8 Pin
IC16	14 Pin	IC34	14 Pin	IC52	8 Pin
IC17	14 Pin	IC35	14 Pin	IC53	8 Pin
IC18	14 Pin	IC36	14 Pin		

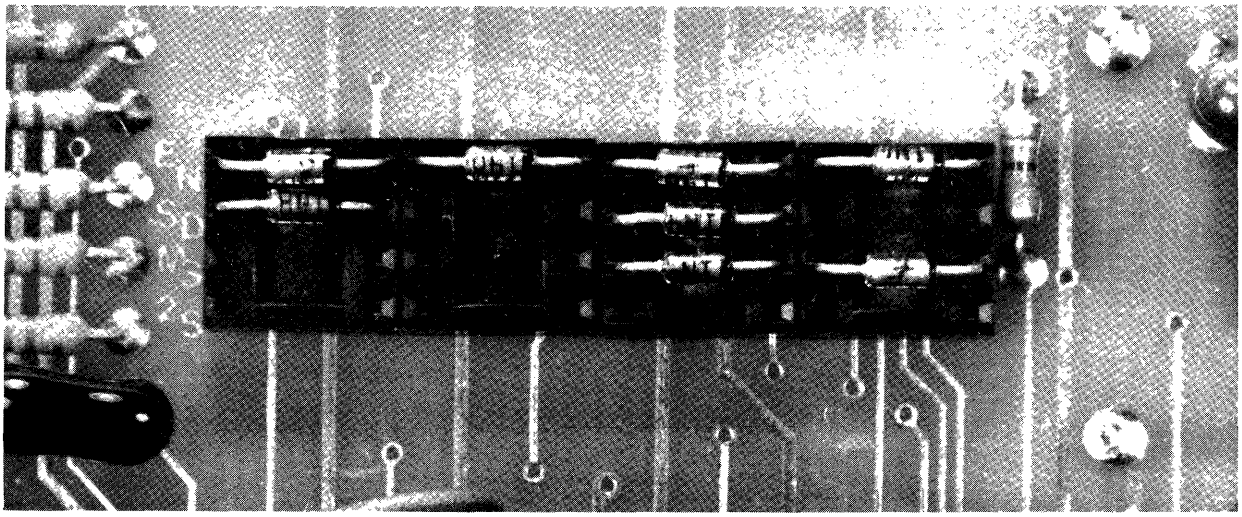
MISC

LABEL	DESC
X1	4.000 Mhz XTAL
L1	22 uh Choke

APPENDIX C

DRIVE ATTRIBUTE SOCKET DEFINITION

There are four 8 Pin Sockets for selecting drive attributes for the four possible drives. The Sockets are numbered IC50, 51, 52, 53 on the Component Placement Diagram. On the Printed Circuit board, they are labeled 1, 2, 3, and 4. The socket numbers correspond to drives DS1 through DS4.



The following table shows which diodes are to be installed for each particular attribute. Diodes should be bent on .3" centers and then installed with the band to the right. (As viewed from the component side.)

BOARD LABEL	SCHEMATIC LABEL	DIODE	NO DIODE
EN	A	DRIVE PRESENT	NO DRIVE
SD	B	SINGLE DENSITY	DOUBLE DENSITY
MS	C	MINI DRIVE	STANDARD DRIVE
2S	D	2 SIDED	1 SIDED

APPENDIX D

BOARD ADDRESSING

The board is addressed by jumpering the true or complement of each address line A3-A7 to IC48 through jumper pads at IC47.

To select the base address, first, write down the binary equivalent for each address bit A3-A7. Then place a jumper in the true position for each address line where the binary value is a one. Next, place a jumper in the complement position for each address line where the binary value was a zero. Example:

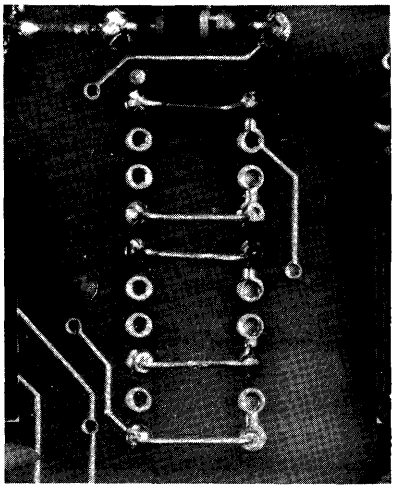
To Select the Base address of 050Q:

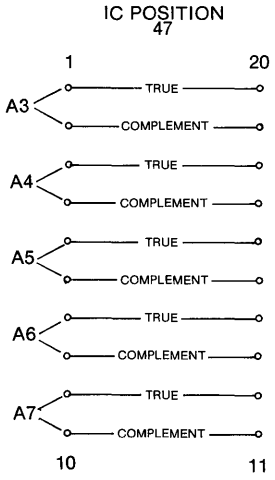
A7	A6	A5	A4	A3
0	0	1	0	1

Then jumper: A5 and A3 true

Then jumper A7 A6 and A4 complement

This should look like the following:





All Digital Group Software expects the Base Address of the Double Density Controller board to be 050Q or 28H.

APPENDIX E

ONE SHOT TIMINGS

The following is a table of the One Shot timings and their tolerance:

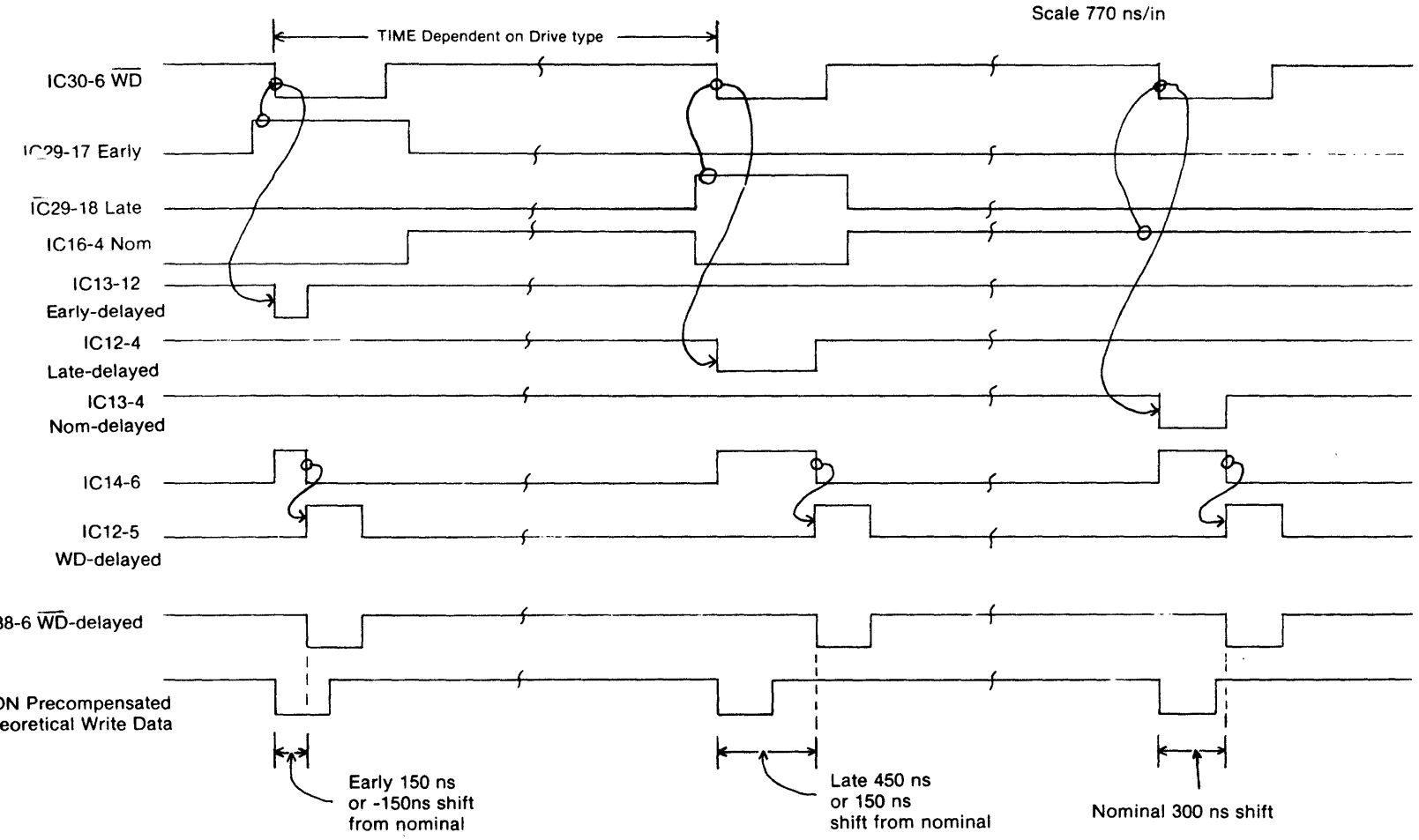
IC	R VALUE	C VALUE	OUTPUT PIN	TIME	TOL
IC1	R8 9.1K	C74 220 pf	13	800 ns	+-10%
IC3	R3 820K	C9 10uf	3	10sec	+-20%
IC4	R1 33K	C72 100uf	12	1 sec	+-20%
IC4	R2 15K	C71 10 uf	4	35 ms	+-10%
IC12	R5 11K	C11 50 pf	4	450 ns	+-10%
IC12	R6 6.8K	C12 50 pf	5	250 ns	+-10%
IC13	R4 7.5K	C10 50 pf	4	300 ns	+-10%
IC13	R7 2.7K	C13 50 pf	12	150 ns	+-10%
IC25	R10 6.8K	C14 50 pf	5,12	200 ns	+-10%
IC25	R11 27K	C15 50 pf	4	160 us	+-20%

APPENDIX F

WRITE PRECOMPENSATION TIMING DIAGRAM

The following timing diagram shows the relationship between the four one shots IC12 and IC13.

WRITE PRECOMPENSATION

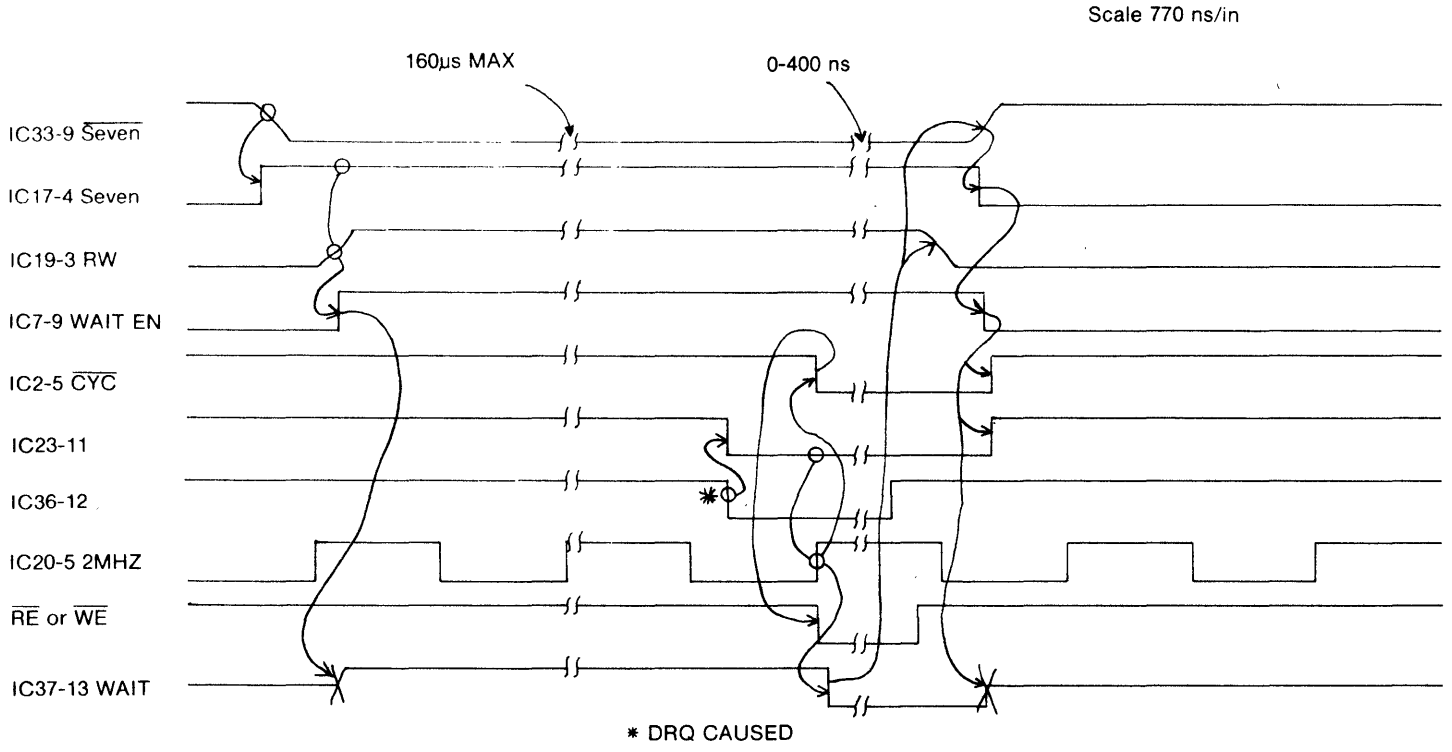


APPENDIX G

WAIT LOGIC TIMING DIAGRAM

The following timing diagram shows the relationship between the wait logic, controller select, and the wait line.

WAIT LOGIC



APPENDIX J

SOFTWARE COMPATIBILITY (OLD VS NEW)

APPENDIX K

APPLICATION NOTE #1

USING INTERRUPTS

Care should be exercised when using interrupts simultaniously with the Digital Group Double Density Controller Board.

If you are using interrupts, be sure that the circuits that can generate these interrupts are disabled before entering the Disc Driver. The High on IC40 Pin 10 can be used to disable other board interrupts.

Also remember that the Disc Driver returns with interrupts disabled and Interrupt Mode Zero selected.

If you call the Disc Driver from numerous locations, it might be wise to modify the Disc Driver to perform the other interrupt disables. This can be done by disabling the other interrupts just after the Disc Driver enables its board interrupt. Your reenable code should be placed after the Disc Driver disables its board interrupts.

APPENDIX L

APPLICATION NOTE #2

OPTIMIZING TIMING VALUES

The Digital Group Double Density Controller Board has some timings that are a tradeoff between Standard and Mini Drives. These are the wait timeout and the head load delay. The Write Precompensation circuit is not needed if the user is not going to be running Standard Double Density.

If you are going to run Mini Drives exclusivly, the Write Precompensation circuit should be disabled. To do this:

1. Lift IC12 Pin 5 from its socket.

2. Jumper IC29 Pin 31 to IC38 Pin 5.

Also, if you are to run Mini Drives only, set the head load delay timer to the manufacturers specs.

If you are going to run Standard drives only, you should reduce the Wait timeout timer. This can be done by using the procedures outlined in the Testing Section. Set the Wait Timeout Timer to 2.5 times the slowest Byte rate to be used.

APPENDIX M

APPLICATION NOTE #3

3 LOGICAL TO 2 PHYSICAL DRIVES

If you have a two drive system and want to run the second drive in both single and double density, this procedure might help.

Select the second drive as both DS2 and DS3. This is done by placing a black shorting plug on both DS2 and DS3 at the drive. Now, on the controller board, Select drive DS2 as present and single density. Select drive DS3 as present and double density.

For Diskmon, you can operate the system by just changing media and then changing the drive number you use. Example:

1. Have the Single density media in drive 1.
2. Perform a D#1 command.
3. Now place the double density media on drive 1.
4. Perform a D#2 command.

For OASIS, the above type logic also works but, after you have changed the media, 'MOUNT' the new media every time.

APPENDIX N

APPLICATION NOTE #4

MULTI HOLE DISKETTES

The Digital Group Double Density Controller Borad will operate on both single and multi-hole diskettes.

This can be accomplished by changing the 800/801 jumper on your drive accordingly.

Should you forget to change from 800 to 801 some unusual things happen. If the controller is requested to read or write a sector and this sector appears before 10 sector holes go by, it will read or write it without error. But if the requested read or write sector is farther around the diskette than 10 sector holes a RECORD NOT FOUND error is generated.

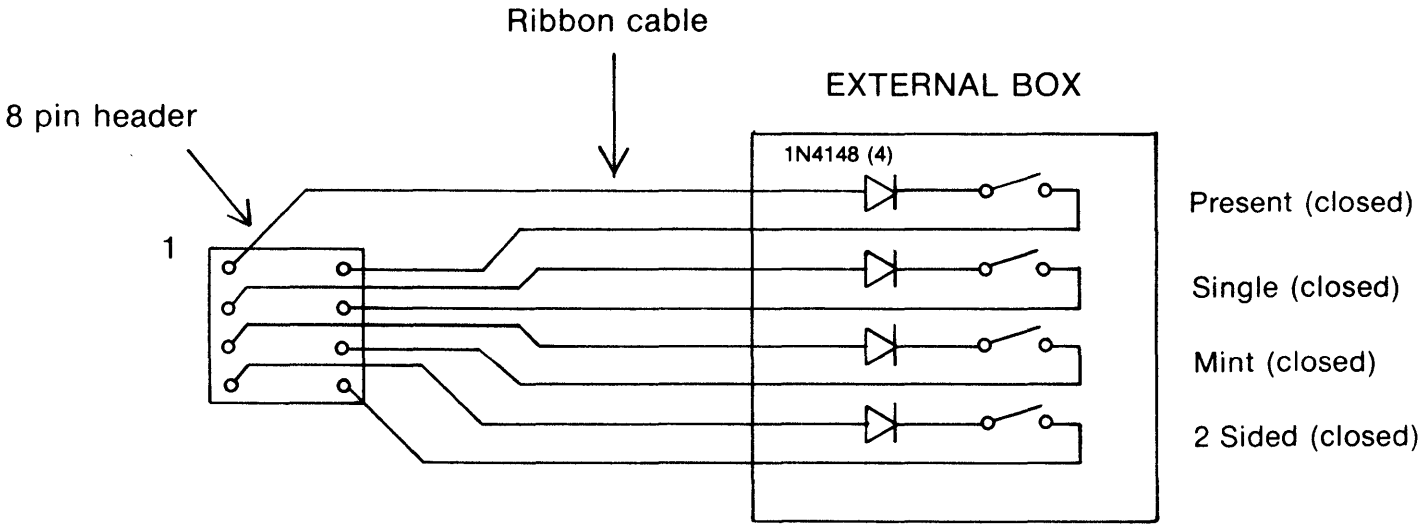
Therefore, if the reliability of your system just changed, and you are switching between single and multi-hole diskettes, CHECK THE 800/801 JUMPER.

APPENDIX O

APPLICATION NOTE #5

BRINGING OUT THE DRIVE ATTRIBUTE DIODES

The Drive Attribute diodes may be brought out to an external set of switches and diodes. This is done by cutting in half a 16 pin header socket. Ribbon cable should be used to bring out the desired attributes. Maximum length of this cable can vary but, try to keep the cable short. Study the following schematic for construction tips:



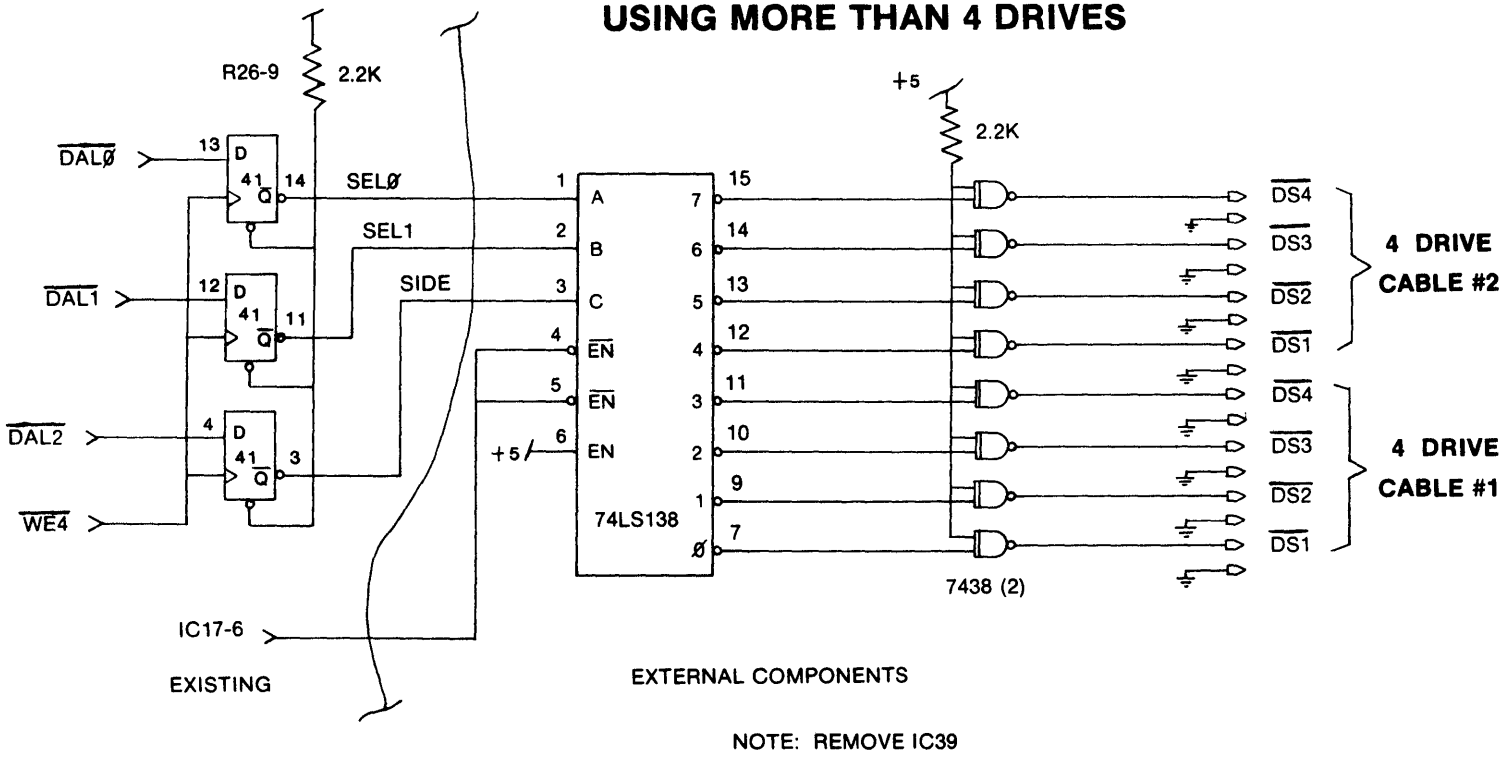
Bringing out the drive attribute diodes

APPENDIX P

APPLICATION NOTE #6

USING MORE THAN 4 DRIVES

The Digital Group Double Density Controller was designed for only 4 drives. This can be modified to 8 drives by external circuitry. Expanding to 8 drives isn't without sacrifice though, the user will loose the side bit to get to 8 Drives. The following schematic shows a typical method for getting to 8 drives:



APPENDIX Q

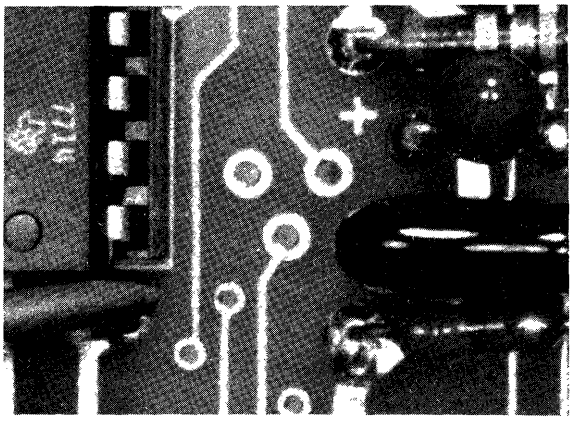
APPLICATION NOTE #7

2.5 MHZ VS 4 MHZ

At this writing (4/79) the Digital Group does NOT support a 4 Mhz Z80 System. The Digital Group Double Density Controller board has been thoroughly tested at 4 Mhz. It was found during this testing that the wait logic release was too fast for 4 Mhz operation. To fix this problem, 1/2 of IC2 was used to delay the release of wait to meet 4 Mhz operating conditions. To operate the controller board at 4 Mhz requires the following:

(1). Cut the default jumper trace to the right of IC2.

(2). Install a jumper wire to the other pad near IC2.



It might be noted here that the present Dynamic Memory board will NOT run at 4 Mhz due to insufficient T(ras) Precharge time during M1.

APPENDIX R

APPLICATION NOTE #8

DYNAMIC MEMORY AND REFRESH

The following is a table of the different refresh rates, for the different types of drives, during a sector data transfer. (using the INIR and OTIR instructions):

DRIVE TYPE	REFRESH PULSES	REFRESH RATE (128)
STANDARD DOUBLE DENSITY	2 per 16 us	0.5 ms
STANDARD SINGLE DENSITY	2 per 32 us	1.0 ms
MINI DOUBLE DENSITY	2 per 32 us	1.0 ms
MINI SINGLE DENSITY	2 per 64 us	2.0 ms

Note that the Mini single density requires a full 2.0 ms to refresh all 128 columns. Some of the Digital Group Dynamic boards shipped prior to 3/79 had Integrated Circuits that did not meet the 2.0 ms refresh rate at all temperatures.

If the user has a Dynamic Memory board with Fairchild 4027-7 IC's, AND intends to run Mini Standard Density, a memory test is in order.

Perform alternate memory writes, followed by heavy disc accesses, then followed by memory reads, to verify the data written in the memory is still valid. Try this test at high temperatures. That is, a temperature that is slightly above the temperature you expect your system to operate at normally.

Note: We don't expect you to have problems but, we want you to be aware of the situation.

APPENDIX S

APPLICATION NOTE #9

SHUGART DRIVE SYMMETRY ADJUST

If you experience an abnormal amount of read errors during double density operation and your free running VCO is set properly (tol: +5% and -0%), your drive might need a symmetry adjustment.

To perform the adjustment, you will need the following:

(1). HMON/2 Monitor

(2). 15 Mhz Triggered Sweep Oscilloscope

(3). Shugart Maintainance Manual

What we will be doing is alternately writing a pattern of all ones and then all zeros onto the media. We will then check for bit jitter between alternating bits. The purpose is not to remove the jitter completely (would be nice though) but to distribute the jitter equally between the one and the zero patterns.

If you have any problems during this adjustment, PLEASE consult the Digital Group Repair Department before continuing. (You could mess up the symmetry so bad that no reading is possible at all.)

Proceedure:

(1). Load HMON/2 and execute option 5.

(2). Place an "expendable" diskette in the drive to be adjusted.

(3). Select the desired drive with the following:

  (a). Execute: OUT-54,(drive number 0-3) (cr)

(4). Get the selected drive to Track 76 by the following:

  (a). Execute: TRK-114 (cr)

  (b). Wait for the stepping to finish.

  (c). Execute: Control C

(5). Trigger the scope on the rising edge of test point 16. Also, observe the pattern on test point 16 for all of the following. (Vert Amplitude 1V per cm)

(6). The ONE Pattern:

(a). Execute: ONE:TRK-114 (cr)

(b). Set sweep to 1us per cm.

(c). Observe the jitter on 2nd and 4th pulses.

(d). Adjust R57 to minimumize the jitter.

(e). Execute: Control C.

(7). The ZERO Pattern:

(a). Execute: ZER:TRK-114 (cr)

(b). Set sweep to 2us per cm.

(c). Observe the jitter on 2nd and 4th pulses.

(d). Adjust R57 to minimumize the jitter.

(e). Execute: Control C

(8). Repeat steps 6 and 7 alternately until the jitter is eliminated completely or is evenly distributed between the One and Zero Pattern.

(9). If you can't get the jitter below 300 ns, consult the Digital Group Repair Department.

(10). Reformat the diskette as Track 76 is blown.

APPENDIX T

APPLICATION NOTE #10

INNOVEX DRIVES

It is unknown at this time if the Innovex drive will handle double density.

For single density though, the Digital Group Double Density Controller will operate with one modification.

The Controller board lacks the Track Greater that 43 Signal. It should be noted that the Innovex drives lack the Side signal. To provide the TG43 signal to the Innovex drives, we must disable the Side logic to the drive and enable the TG43 signal. Somewhat by choice, the side signal is present on the very line that the Innovex requires the TG43 signal. To switch these, perform the following:

(1). Cut the trace leading to IC40 Pin 13.

(2). Jumper the TG43 signal from IC29-29 to IC40-13.

This Modification removes the Side signal from Controller 36 Pin edg connector Pin 21 and in its place substitutes the TG43 signal.

WESTERN DIGITAL
CORPORATION

FD1791A/B Floppy Disk Formatter/Controller

FEATURES

- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
- READ MODE
  - Single/Multiple Record Read with Automatic Search or Entire Track Read
  - Selectable 128 Byte or Variable Length Record
- WRITE MODE
  - Single/Multiple Record Write with Automatic Sector Search
  - Entire Track Write for Diskette Initialization
- PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Selectable Head Settling and Head Engage Times
- SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-chip Track and Sector Registers Comprehensive Status Information
- WRITE PRECOMPENSATION (MFM AND FM)
- WINDOW EXTENSION (IN MFM)
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY

APPLICATIONS

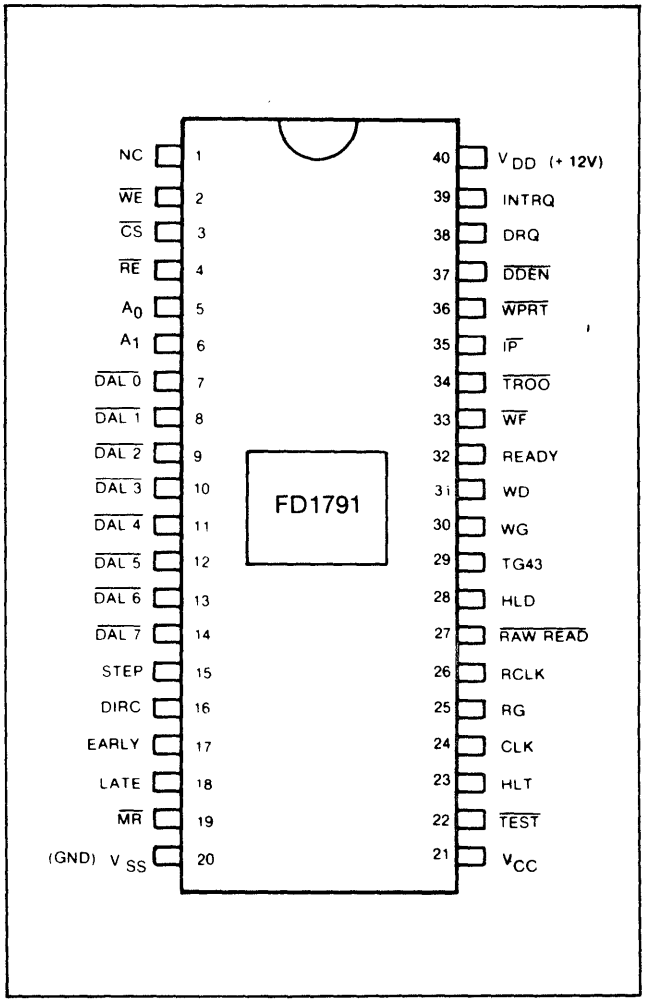
FLOPPY DISK DRIVE INTERFACE
SINGLE OR MULTIPLE DRIVE CONTROLLER/FORMATTER
NEW MINI-FLOPPY CONTROLLER

GENERAL DESCRIPTION

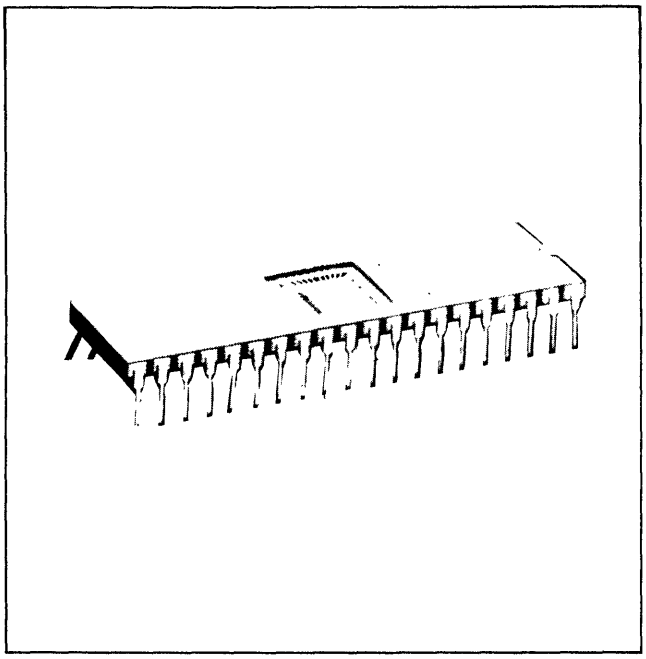
The FD1791 is a MOS LSI device which performs the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD1791, which can be considered the end result of both the FD1771 and FD1781 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD1791 contains all the features of its predecessor the FD1771, plus the added features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD1791 designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The FD1791 is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD1791 is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs.



PIN CONNECTIONS



ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 3. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register—This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register—This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register can be loaded from the DAL and gated onto the DAL under processor control.

Track Register—This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when this device is busy.

Sector Register (SR)—This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR)—This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the execution of the current command is to be overridden. This latter action results in an interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR)—This 8-bit register holds device Status information. The meaning of the Status bits is a function of the contents of the Command Register. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic—This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

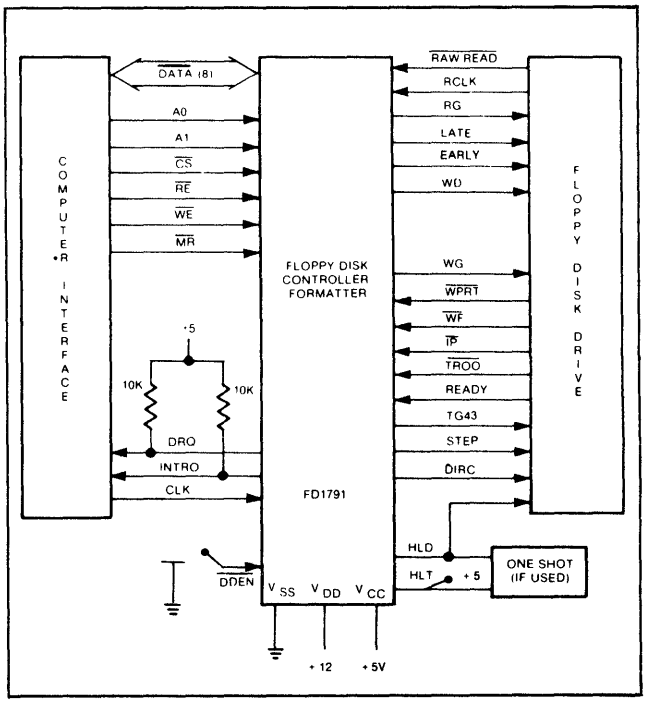
The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU)—The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

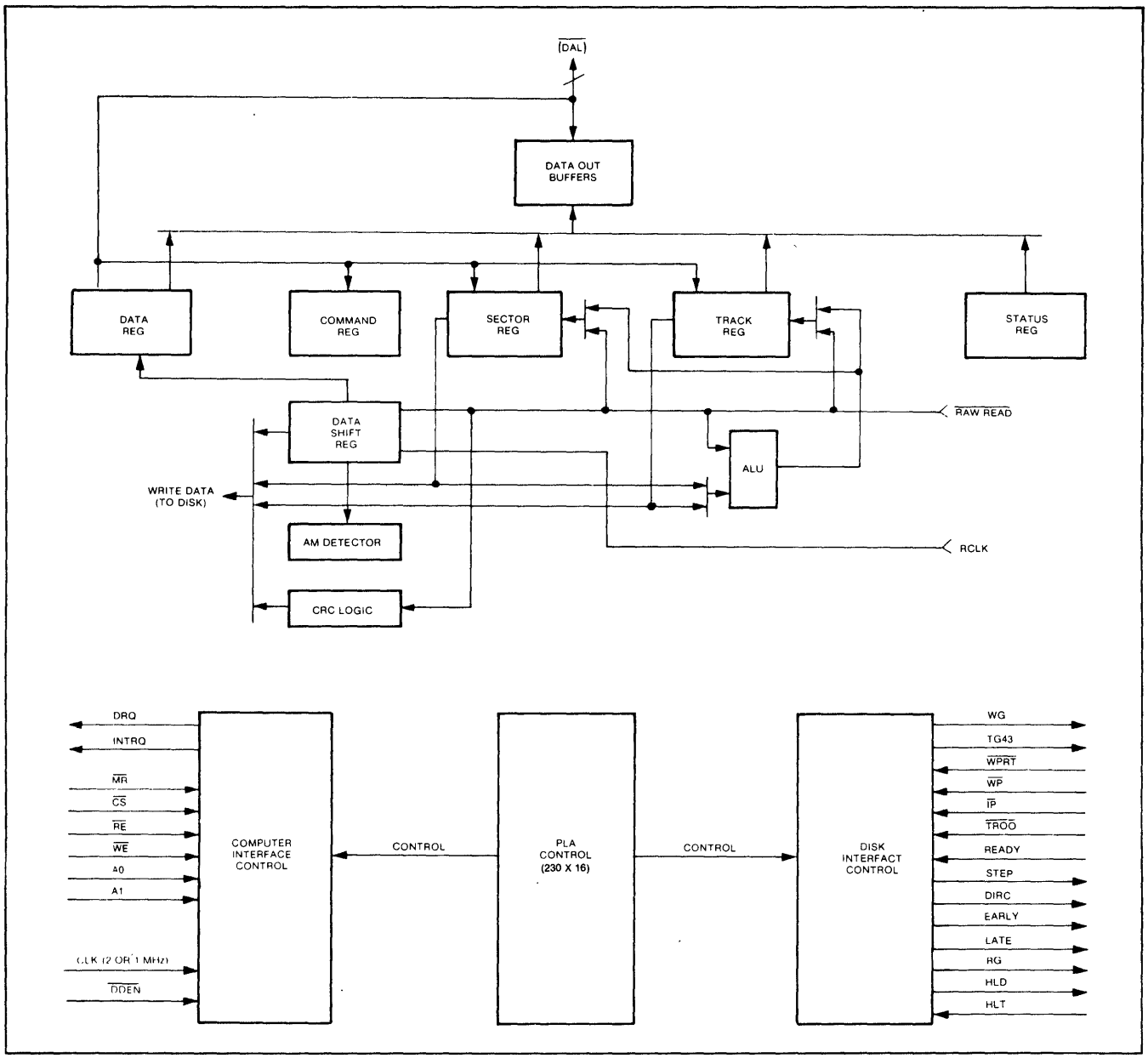
Timing and Control—All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD1791 has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = 0 double density (MFM) is assumed. When $\overline{DDEN}$ = 1, single density (FM) is assumed.

AM Detector—The address mark detector detects ID, data and index address marks during read and write operations.



1791 SYSTEM BLOCK DIAGRAM



FD1791 BLOCK DIAGRAM

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the FD1791. The DAL are three state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable (RE) are active (low logic state) or act as input receivers when CS and Write Enable (WE) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and CS is made low. The least-significant address bits A1 and A0, combined with the signals RE during a Read operation or WE during a Write operation are interpreted as selecting the following registers:

A1-A0	READ (RE)	WRITE (WE)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD1791 and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by

the processor. If the Data Register is read after one or more characters are lost, by having new data transferrd into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The 1791 has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density. When the clock is at 2 MHz, the stepping rates of 3, 6, 10, and 15 ms are obtainable. When CLK equals 1 MHz these times are doubled.

HEAD POSITIONING

Four commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If $\overline{TEST}$ = 0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type 2 or 3 command.

The rates (shown in Table 1) can be applied to a Step-Direction Motor through the device interface.

Step—A 2 μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

Direction (DIRC)—The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μs before the first stepping pulse is generated.

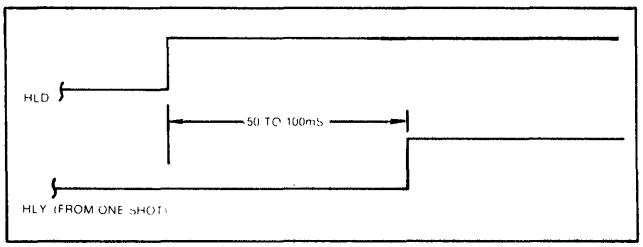
When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The FD1791 must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated.

Table 1. STEPPING RATES

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
$\overline{DDEN}$	0	1	0	1		
R1 R0	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=0	$\overline{TEST}$=0
0 0	3 ms	3 ms	6 ms	6 ms	Approx.	Approx.
0 1	6 ms	6 ms	12 ms	12 ms	200 μs	400 μs
1 0	10 ms	10 ms	20 ms	20 ms		
1 1	15 ms	15 ms	30 ms	30 ms		

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the FD1791 is in an idle state (non-busy) and 15 index pulses have occurred, it is reset.

Head Load Timing (HLT) is an input to the FD1791 which is used for the head engage time. When HLT = 1, the FD1791 assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FD1791.



HEAD LOAD TIMING

When both HLD and HLT are true, the FD1791 will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the FD1791 waits for HLT to be

true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the FD1791 then waits for HLT to occur.

For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true, with E flag on HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{\text{DDEN}}$ should be placed to logical "1." For MFM formats, $\overline{\text{DDEN}}$ should be placed to a logical "0." Sector lengths are determined at format time by a special byte in the "ID" field. If this Sector Length byte in the ID field is zero, then the sector length is 128 bytes. If 01 then 256 bytes. If 02, then 512 bytes. If 03, then the sector length is 1024 bytes. The number of sectors per track as far as the FD1791 is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD1791 is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track.

For read operations, the FD1791 requires $\overline{\text{RAW READ}}$ Data (Pin 27) signal which is a 250 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase lock loop, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) which informs some phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FD1791 must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD1791 is deriving any useful information from the data stream. Similarly for MFM, RG is made active true when 4 bytes of "00" or "FF" are detected. The FD1791 must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD1791 before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD1791 terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the $\overline{\text{Write Gate}}$ output becomes inactive.

For write operation, the FD1791 provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{\text{DDEN}}$ = 1) and 250 ns pulses in MFM ($\overline{\text{DDEN}}$ = 0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written early. EARLY is valid for the duration of the pulse. LATE is active true when the WD pulse is to be written late. If both are low when a WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD1791. The write precompensation signals EARLY and LATE are valid in both FM and MFM formats.

Whenever a Read or Write command (Type II or III) is received the FD1791 samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. The Seek or Step Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

COMMAND DESCRIPTION

The FD1791 will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 2.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field (r_0r_1), which determines the stepping motor rate as defined in Table 1.

Table 2. COMMAND SUMMARY

TYPE	COMMAND	BITS 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	X	E	0	0
II	Write Command	1	0	1	m	X	E	X	a_0
II	Read Address	1	1	0	0	0	1	0	0
III	Read Track	1	1	1	0	0	1	0	X
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrrupt	1	1	0	1	I_3	I_2	I_1	I_0

X = Don't care
Note: Bits shown in TRUE form.

Table 3. FLAG SUMMARY

TYPE I

h = Head Load Flag (Bit 3)

h = 1, Load head at beginning
h = 0, Unload head at beginning

V = Verify flag (Bit 2)

V = 1, Verify on last track
V = 0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)

Refer to Table 1 for rate summary

u = Update flag (Bit 4)

u = 1, Update Track register
u = 0, No update

Table 4. FLAG SUMMARY

TYPE II

m = Multiple Record flag (Bit 4)

m = 0, Single Record
m = 1, Multiple Records

a_0 = Data Address Mark (Bit 0)

a_0 = 0, FB (Data Mark)
a_0 = 1, F8 (Deleted Data Mark)

E = 15 ms Delay

E = 1, 15 ms delay

E = 0, no 15 ms delay

Table 5. FLAG SUMMARY

TYPE IV

Ii = Interrupt Condition flags (Bits 3-0)

I0 = 1, Not-Ready to Ready Transition
I1 = 1, Ready to Not-Ready Transition
I2 = 1, Index Pulse
I3 = 1, Immediate Interrupt

The Type 1 Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h = 1, the head is loaded at the beginning of the command (HLD output is made active). If h = 0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FD1791 receives a command that specifically disengages the head. If the FD1791 is idle (busy = 0) for 15 revolutions of the disk, the head will be automatically disengaged (HLD made inactive).

The Type I Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V = 1, a verification is performed, if V = 0, no verification is performed.

During verification, the head is loaded and after an internal 15 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID field is read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, and Seek Error Status bit (Status bit 4) is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the disk, the FD1791 terminates the operation and sends an interrupt, (INTRQ).

The Step, Step-In, and Step-Out commands contain an Update flag (U). When U = 1, the track register is updated by one for each step. When U = 0, the track register is not updated.

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{\text{TR00}}$) input is sampled. If $\overline{\text{TR00}}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{\text{TR00}}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r_1r_0 field are issued until the $\overline{\text{TR00}}$ input is activated. At this time the TR is loaded with zeroes and an interrupt is generated. If the $\overline{\text{TR00}}$ input does not go active low after 255 stepping pulses, the FD1791

terminates operation, interrupts, and sets the Seek error status bit. Note that the Restore command is executed when MR goes from an active to an inactive state. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command.

SEEK

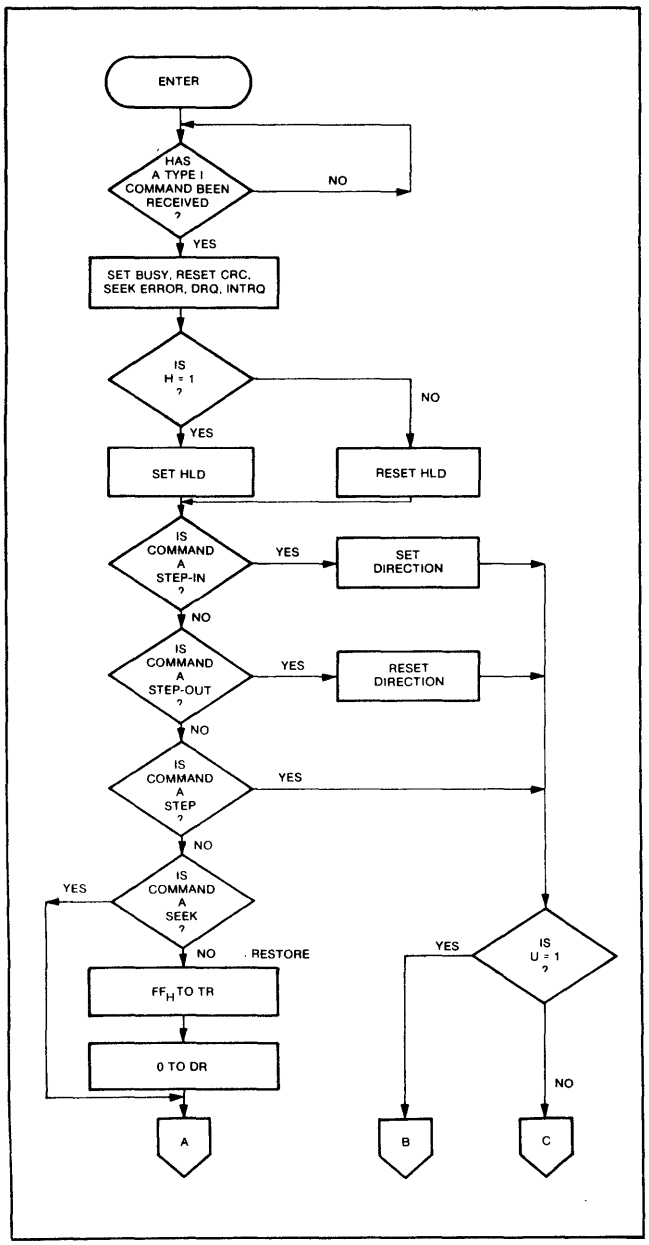
This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD1791 will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the data register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

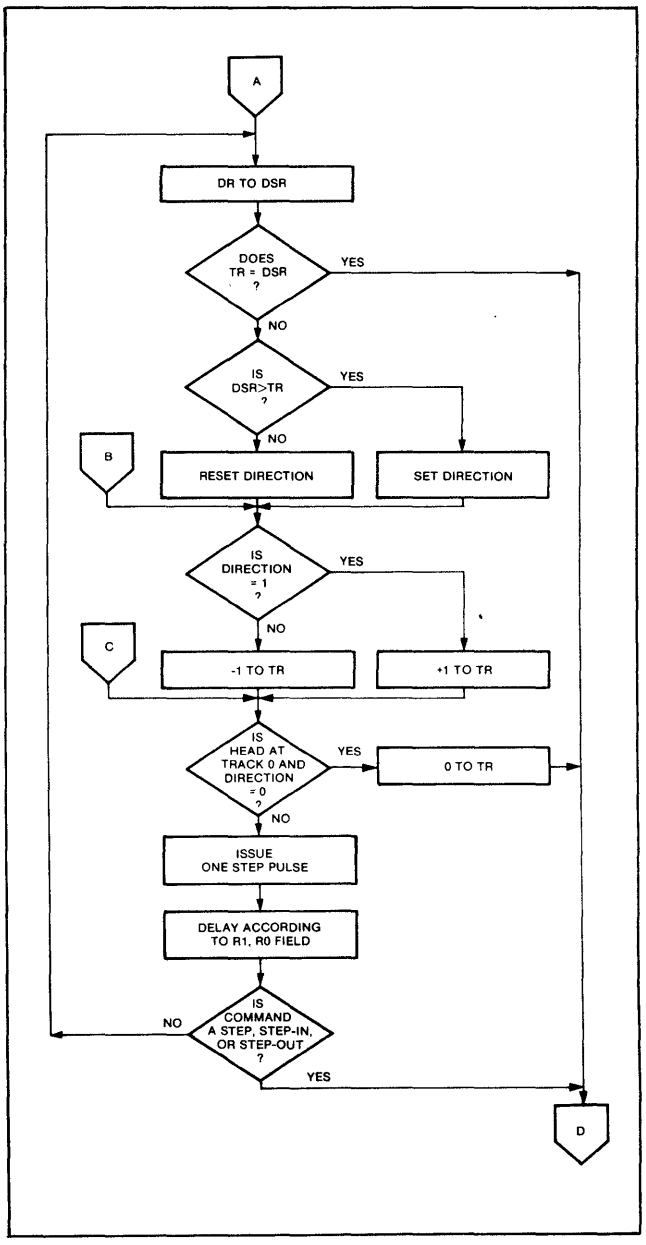
Upon receipt of this command, the FD1791 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the u flag is on, the TR is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the FD1791 issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.



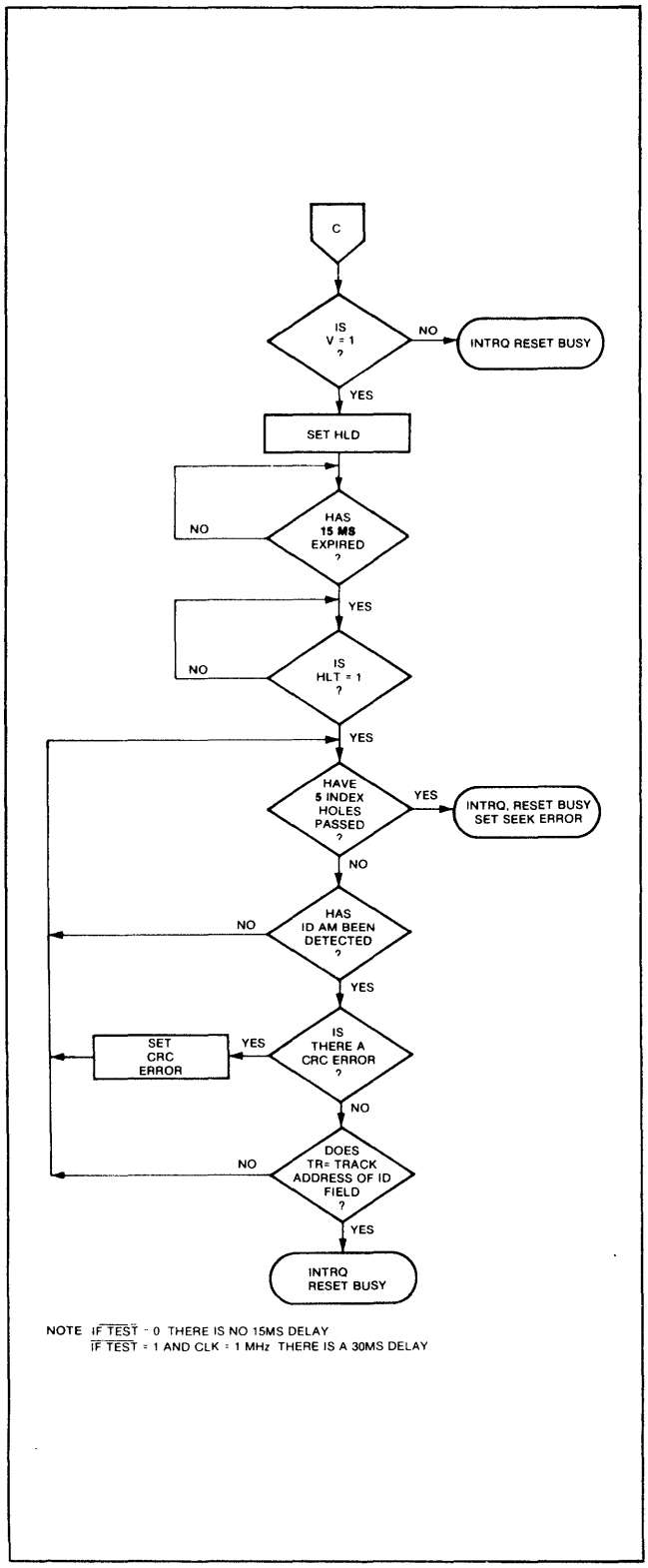
TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

STEP-OUT

Upon receipt of this command, the FD1791 issues one stepping pulse in the direction towards track 0. If the u flag is on, the TR is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows thee start of the command. An interrupt is generated at the completion of the command.



TYPE I COMMAND FLOW

TYPE II COMMANDS

The type II Commands include the Read Sector (s) and Write Sector (s) commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay. The ID field and Data Field format are shown below.

When an ID field is located on the disk, the FD1791 compares the Track number of the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD1791 must find an ID field with a Track number, Sector number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

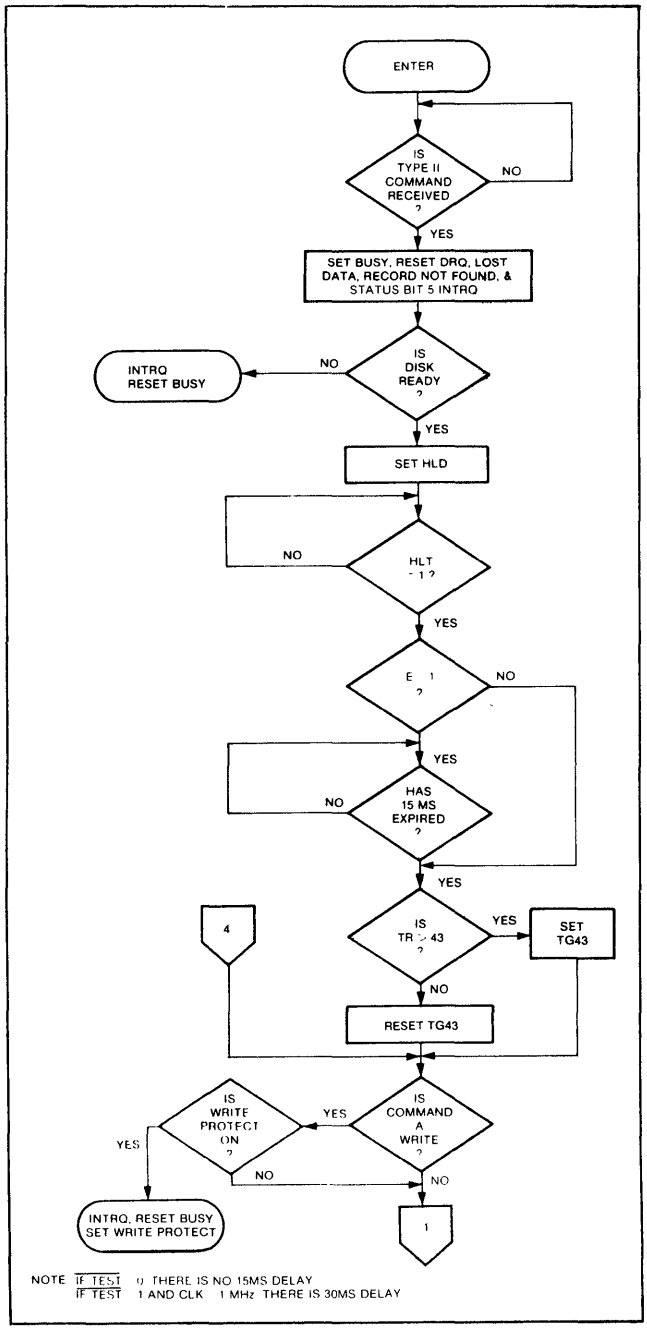
Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD1791 will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

READ COMMAND

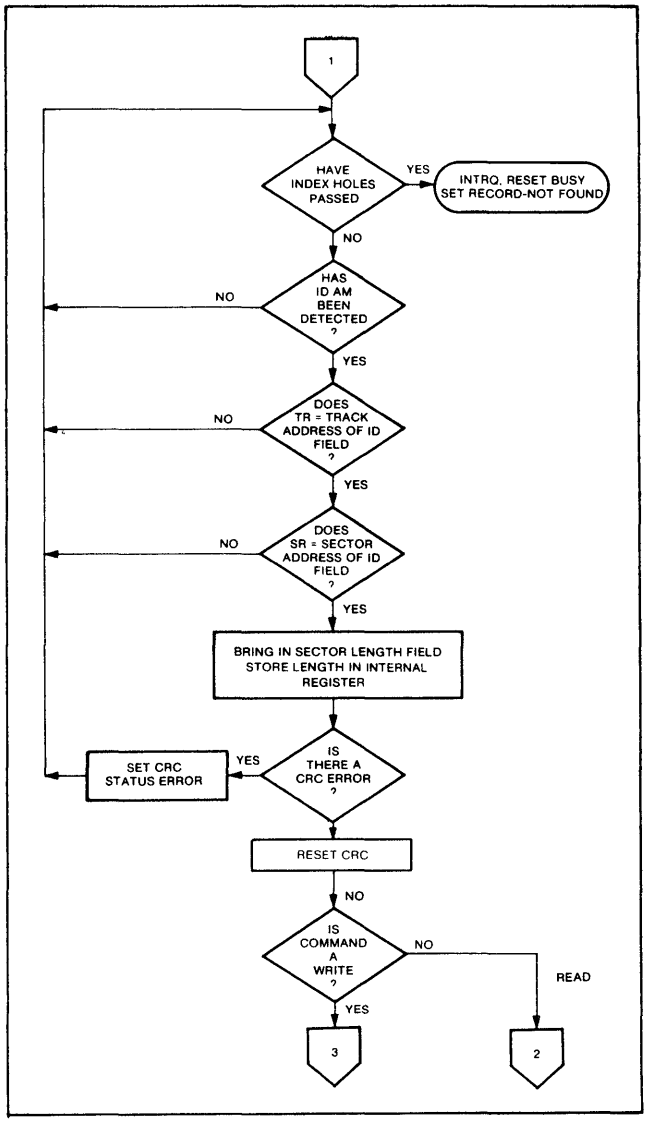
Upon receipt of the Read command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record Not Found status bit is set and the operation is terminated.

GAP III	ID AM	TRACK NUMBER	SIDE NUMBER	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP II	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD										DATA FIELD		

In MFM only, IDAM and DATA AM are preceded by three bytes of A1 with clock transition between bits 4 and 5 missing.



TYPE II COMMAND



TYPE II COMMAND

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

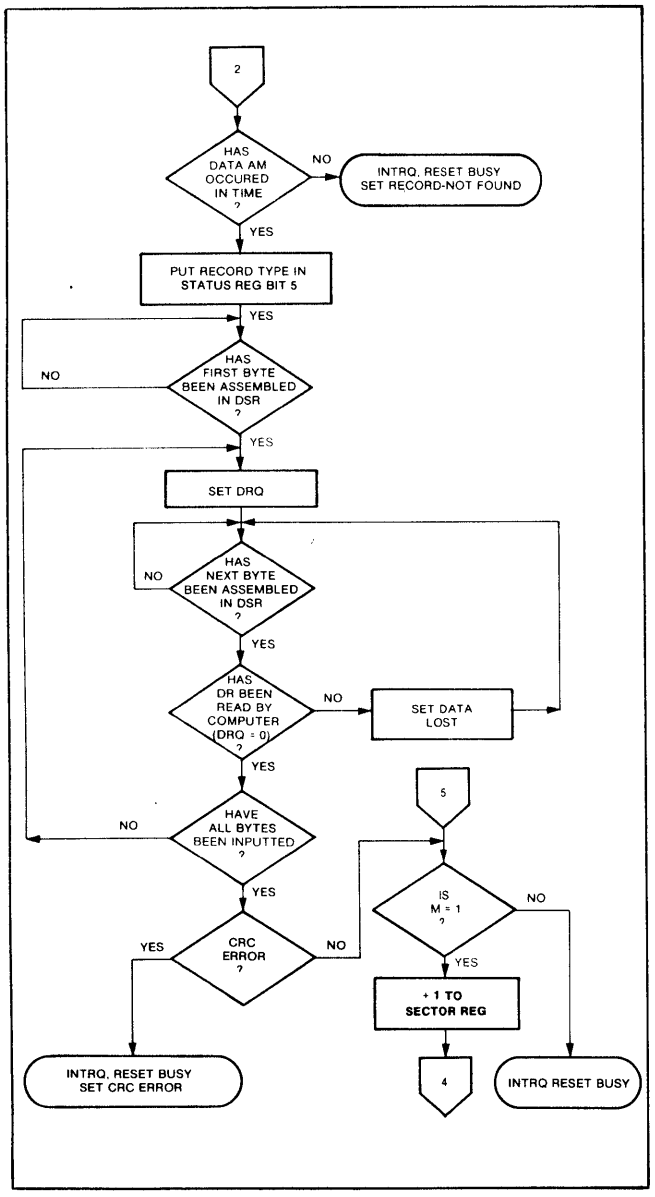
At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown below:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE COMMAND

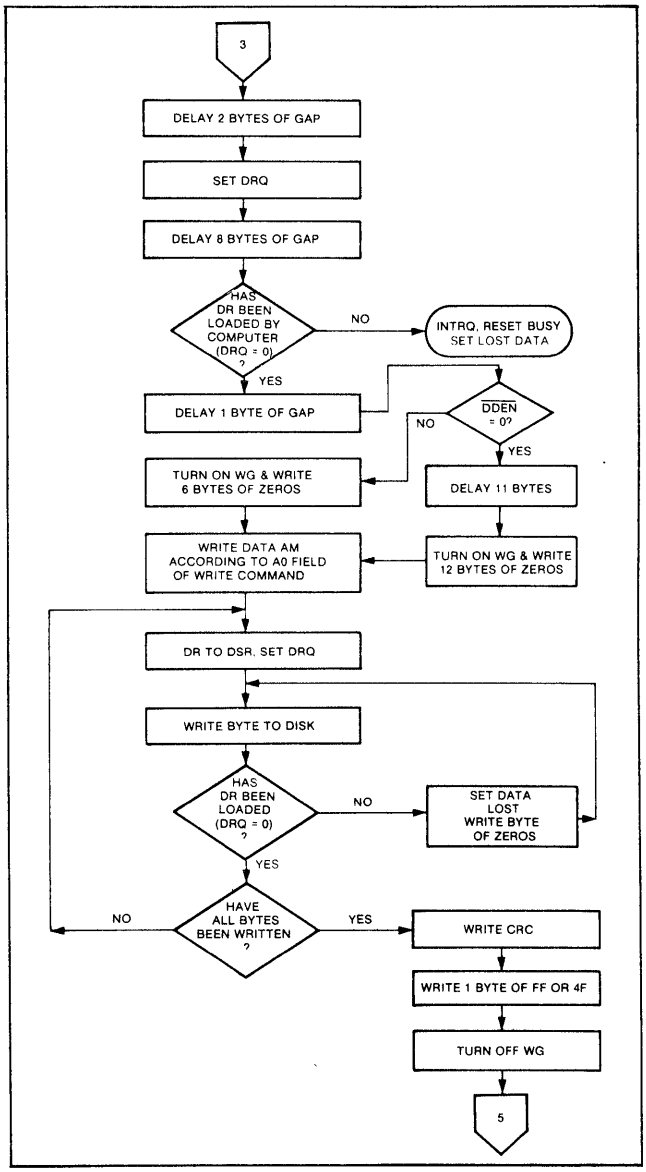
Upon receipt of the Write command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The FD1791 counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark



TYPE II COMMAND

The FD1791 then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or 4F in MFM. The WG output is then deactivated.



TYPE II COMMAND

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 2	CRC 2
1	2	3	4	5	6

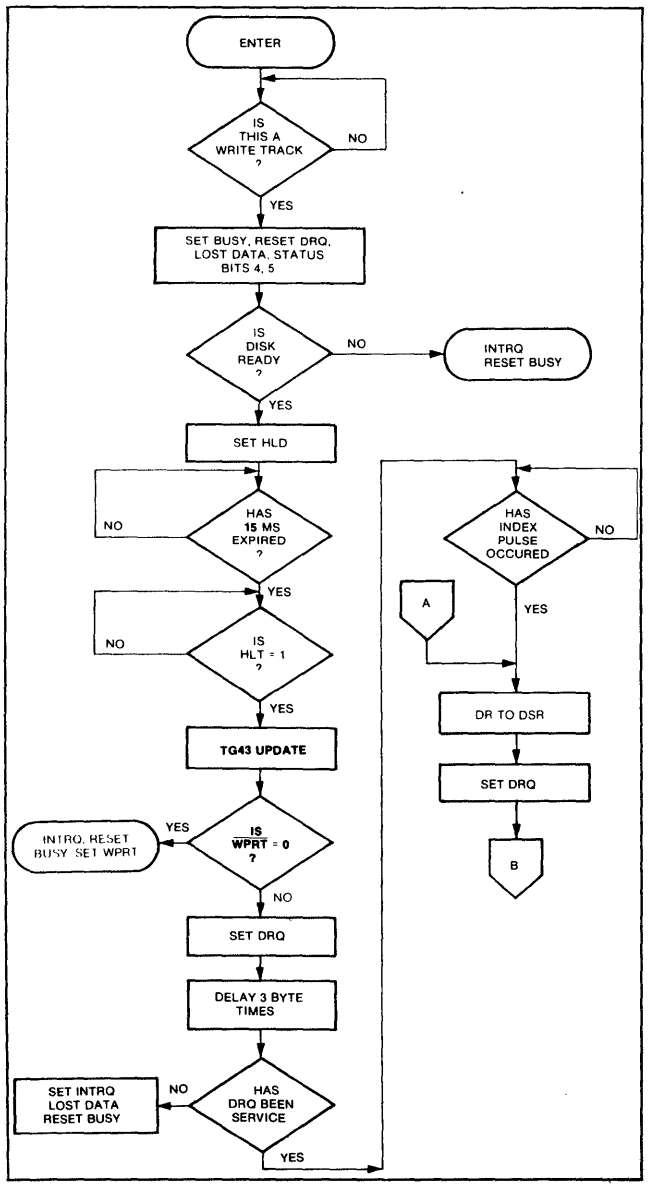
Although the CRC characters are transferred to the computer, the FD1791 checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

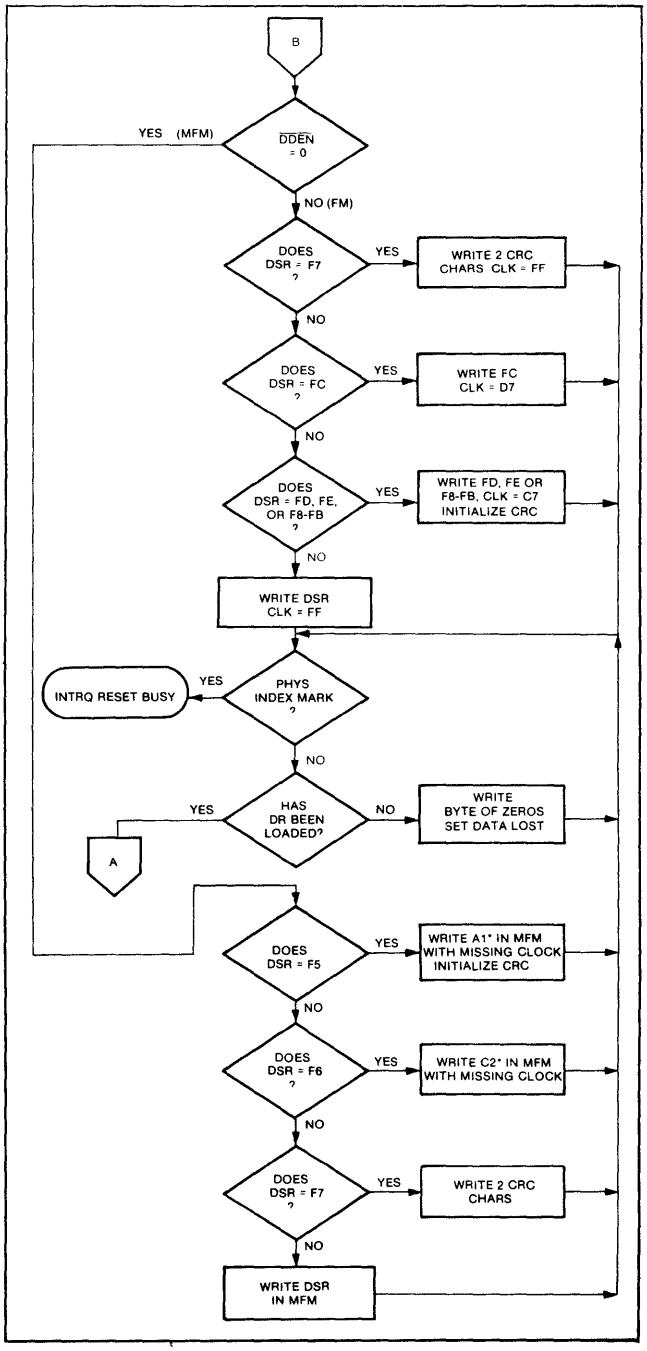
Upon receipt of the Read Track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. The accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated.

WRITE TRACK

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM.



TYPE III COMMAND WRITE TRACK



TYPE III COMMAND WRITE TRACK

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	FD1791 INTERPRETATION IN FM ($\overline{DDEN}$ = 1)	FD1791 INTERPRETATION IN MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 with Clk = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5
**Missing clock transition between bits 3 and 4

TYPE IV COMMAND

FORCE INTERRUPT

This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

I_0= Not-Ready-To-Ready Transition
I_1 = Ready-To-Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

NOTE: If $I_0 - I_3 = 0$, there is no interrupt generated but the current command is terminated and busy is reset. This is the only command that will clear the immediate interrupt.

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

Table 6. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ	READ TRACK	WRITE	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD	0	RECORD TYPE = DELETED DATA / RECORD NOT FOUND	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RECORD NOT FOUND		0	0	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" or HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S2 TRACK 00	When set, indicates Read Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TROO}}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS BITS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. On Read Track: Not Used. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND	When set, it indicates that the desired track and sector were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA control with a large amount of memory. When operating under DMA with limited amount of memory, formatting is a more difficult task. This is because gaps as well as data must be provided at the computer interface.

Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the FD1791 raises the data request signal. At this point in time, the user loads the data register with desired data to be written on the disk. For every byte of information to be written on the disk, a data request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the FD1791 detects a data pattern on F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation. For instance, in FM an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

IBM 3740 FORMAT—128 BYTES/SECTOR

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

	NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
	40	FF
	6	00
	1	FC (Index Mark)
	26	FF
*	6	00
	1	FE (ID Adress Mark)
	1	Track Number
	1	00
	1	Sector Number (1 thru 1A)
	1	00
	1	F7 (2 CRC's written)
	11	FF
	6	00
	1	FB (Data Address Mark)
	128	Data (IBM uses E5)
	1	F7 (2 CRC's written)
	27	FF
	247**	FF

*Write bracketed field 26 times

**Continue writing until FD1791 interrupts out. Approx. 247 bytes.

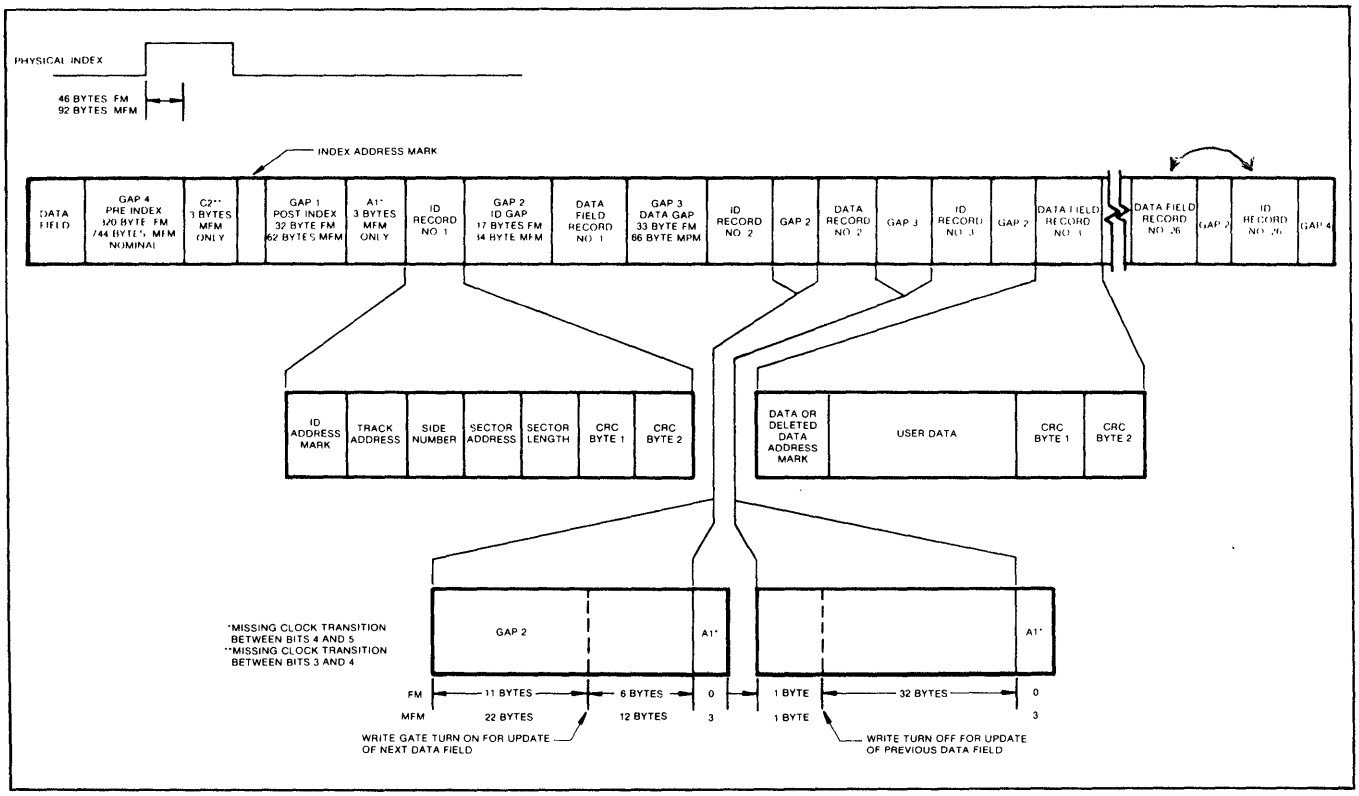
IBM SYSTEM 34 FORMAT-256 BYTES/SECTOR

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette, the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

	NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
	80	4E
	12	00
	3	F6
	1	FC
	50	4E
*	12	00
	3	F5
	1	FE
	1	Track Number (0 thru 4C)
	1	Side Number (0 or 1)
	1	Sector Number (0 thru 1A)
	1	01
	1	F7
	22	4E
	12	00
	3	F5
	1	FB
	256	40
	1	F7
	54	4E
	598**	

*Write bracketed field 26 times.

**Continue writing until FD1791 interrupts out. Approx. 598 bytes.



IBM TRACK FORMAT

NON-IBM FORMATS

Variations in the IBM format are possible to a limited extent if the following requirements are met: sector size must be a choice of 128, 256, 512 or 1024 bytes; gap size must be according to the following table. Note that the Index Mark is not required by the FD1791.

	FM	MFM
Gap I	16 bytes FF	16 bytes 4E
Gap II *	11 bytes FF 6 bytes 00	22 bytes 4E 12 bytes 00 3 bytes A1
Gap III **	10 bytes FF 4 bytes 00	16 bytes 4E 8 bytes 00 3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.

**Byte counts are minimum, except exactly 3 bytes of A1 must be written.

REFERENCES:

1. IBM Diskette OEM Information GA21-9190-1
2. SA900 IBM Compatibility Reference Manual—Shugart Associates.
3. IBM Two-Sided Diskette OEM Information GA21-9257-1

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V_{DD} With Respect to V_{SS} (Ground)	+15 to -0.3V
Max. Voltage to Any Input With Respect to V_{SS}	+15 to -0.3V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C

OPERATING CHARACTERISTICS (DC)

T_A = 0°C to 70°C, V_{DD} = +12.0V ±.6V, V_{SS} = 0V, V_{CC} = +5V ±.25V

V_{DD} = 10 ma Nominal, V_{CC} = 35 ma Nominal

SYMBOL	CHARACTERISTIC	MIN.	TYPE.	MAX.	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	μA	$V_{OUT} = V_{DD}$
V_{IH}	Input High Voltage	2.6			V	
V_{IL}	Input Low Voltage (all			0.8	V	
V_{OH}	Output High Voltage	2.8			V	I_O = 100 μA
V_{OL}	Output Low Voltage			0.4	V	I_O = 1.6 mA

NOTE: Pin 1 is normally connected to substrate with internal back bias generator. Be sure not to connect anything to Pin 1.

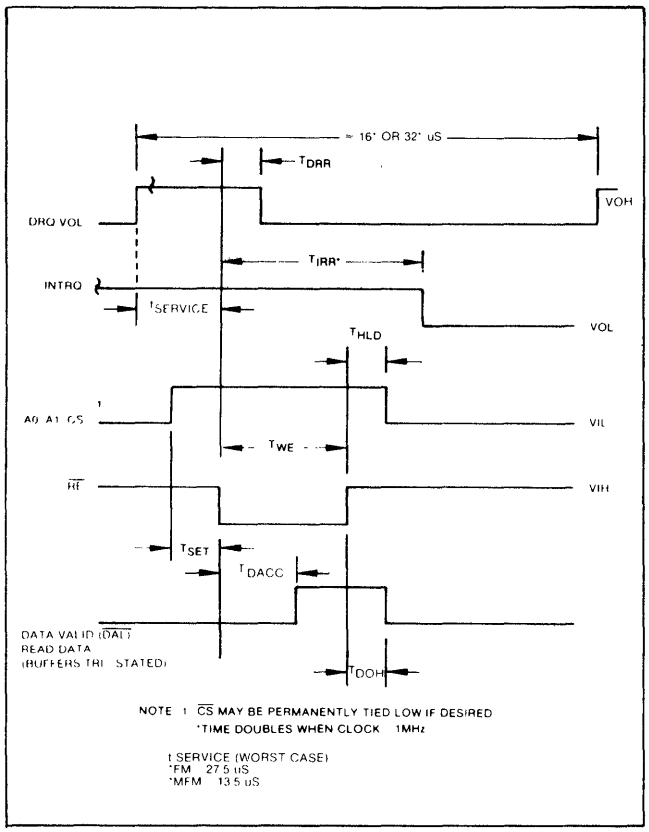
TIMING CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = + 12V ± .6V, V_{SS} = 0V, V_{CC} = +5V ± .25V

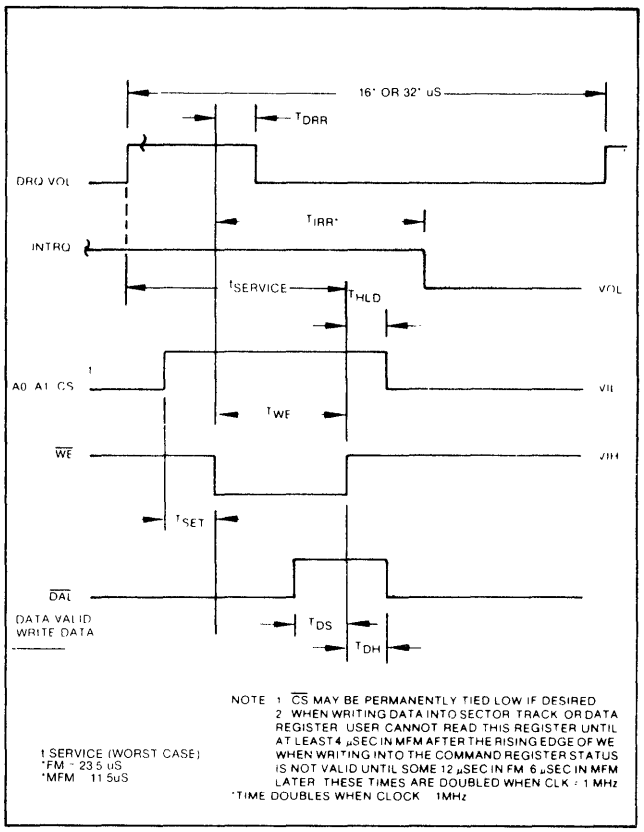
NOTE: Timings are given for 2 MHz Clock. For those timings noted, values will double when chip is operated at 1 MHz.

READ OPERATIONS

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{RE}$	100			nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	500			nsec	C_L = 25 pf
TDRR	DRQ Reset from $\overline{RE}$			500	nsec	
TIRR	INTRQ Reset from $\overline{RE}$		500	3000	nsec	See Note
TDACC	Data Access from $\overline{RE}$			350	nsec	C_L = 25 pf
TDOH	Data Hold From $\overline{RE}$	50		150	nsec	C_L = 25 pf



READ ENABLE TIMING



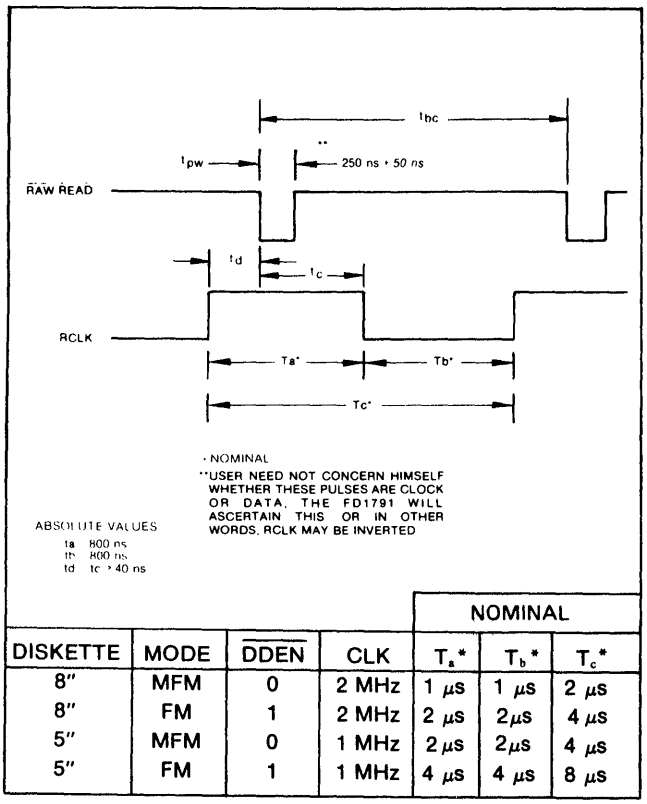
WRITE ENABLE TIMING

WRITE OPERATIONS

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	100			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$			500	nsec	
TIRR	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Note
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	20			nsec	

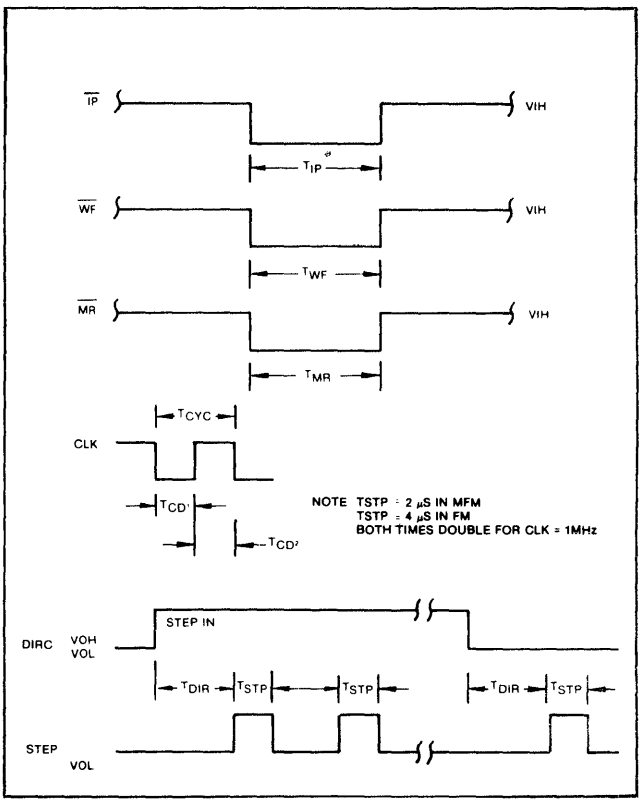
MISCELLANEOUS TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TCD_1	Clock Duty (low)	230			nsec	
TCD_2	Clock Duty (high)	200			nsec	
TSTP	Step Pulse Output	2 or 4			µsec	
TDIR	Dir Setup to Step	12			µsec	See Note
TMR	Master Reset Pulse Width	50			µsec	
TIP	Index Pulse Width	10			µsec	
TWF	Write Fault Pulse Width	10			µsec	



DISKETTE	MODE	$\overline{\text{DDEN}}$	CLK	NOMINAL T_a*	NOMINAL T_b*	NOMINAL T_c*
8"	MFM	0	2 MHz	1 μs	1 μs	2 μs
8"	FM	1	2 MHz	2 μs	2μs	4 μs
5"	MFM	0	1 MHz	2 μs	2μs	4 μs
5"	FM	1	1 MHz	4 μs	4 μs	8 μs

INPUT DATA TIMING



MISCELLANEOUS TIMING

NOTES:

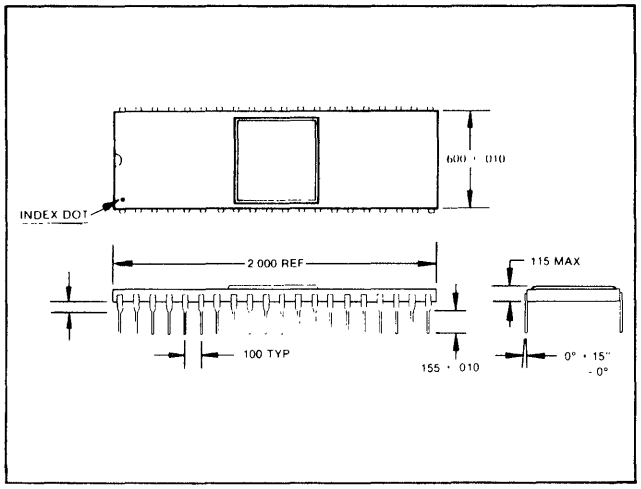
1. Pulse width on $\overline{\text{RAW READ}}$ (p.27) is normally 250 ± 50 ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK = 2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.
2. When flux reversals are totally nonexistent, the external separator should insure $\overline{\text{RAW READ}}$ = 1. Also, RCLK should be free running at all times.
3. t_{bc} (see input data timing) should be 2, 3, or 4 μs nominal in MFM and 2 or 4 μs nominal in FM. Times double when CLK = 1 MHz.
4. In MFM, the EARLY and LATE signals are valid at least 125 ns from either edge of WD.

PIN OUTS

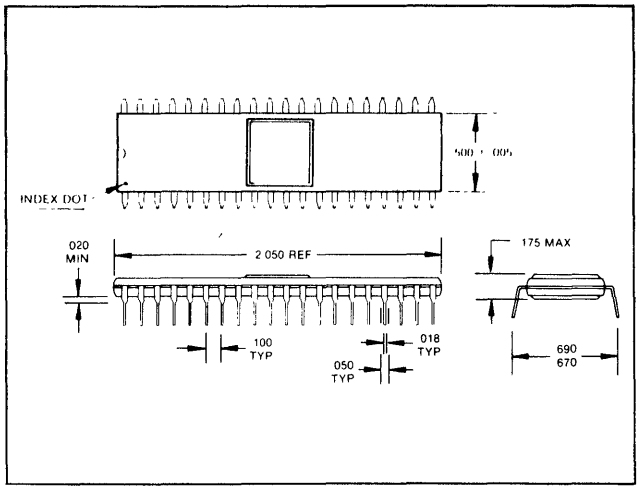
PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V
40		V_{DD}	+12V
19	$\overline{\text{MASTER RESET}}$	$\overline{\text{MR}}$	A logic low on this input resets the device and loads hex 03 into the command register. The Not Ready (Status Bit 7) is reset during MR ACTIVE. When MR is brought to a logic high a Restore Command is executed, regardless of the state of the Ready signal from the drive. Also, hex 01 is loaded into sector register.
COMPUTER INTERFACE:			
7-14	$\overline{\text{DATA ACCESS LINES}}$	$\overline{\text{DAL0}}$-$\overline{\text{DAL7}}$	Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by WE or a transmitter enabled by RE.
3	$\overline{\text{CHIP SELECT}}$	$\overline{\text{CS}}$	A logic low on this input selects the chip and enables computer communication with the device.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/ transfer data on the DAL lines under RE and WE control: A1 A0 RE WE 0 0 Status Reg Command Reg 0 1 Track Reg Track Reg 1 0 Sector Reg Sector Reg 1 1 Data Reg Data Reg
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operation, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register or the status register is read. Use 10K pull-up resistor to +5.
24	CLOCK	CLK	This input requires a free-running square wave clock for internal timing reference, 2 MHz for regular drives, 1 MHz for mini-drives.
FLOPPY DISK INTERFACE:			
25	READ GATE	RG	A high level on this output indicates to the data separator circuitry that a field of zeros (or ones) has been encountered, and is used for synchronization.
31	WRITE DATA	WD	A 250 ns (MFM) or 500 ns (FM) pulse per flex transition. WD contains the unique Address marks as well as data in both FM and MFM formats.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	RAW READ	$\overline{RAW\ READ}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media. When a logic high is found on the HLT input the head is assumed to be engaged.
23	HEAD LOAD TIMING	HLT	
15	STEP	STEP	Step and direction motor control. The step output contains a pulse for each step and the direction output is active high when stepping in, active low when stepping out.
16	DIRECTION	DIRC	

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
17	EARLY	EARLY	Indicates that the write data pulse occurring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read-Write head is positioned between the 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid when writing is to be performed on the diskette.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. A Seek operation is performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$	$\overline{\text{WF}}$	This input detects writing faults indications from the drive. When WG = 1 and $\overline{\text{WF}}$ goes low the current Write command is terminated and the Write Fault status bit is set. The $\overline{\text{WF}}$ input should be made inactive (high) when WG becomes inactive.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FD1791 that the Read-Write head is positioned over Track 00 when a logic low.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	Input, when low for a minimum of 10 μsec, informs the FD1791 when an index mark is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write Command is received. A logic low terminated the command and sets the Write Protect Status bit.
37	$\overline{\text{DOUBLE DENSITY}}$	$\overline{\text{DDEN}}$	This pin selects either single or double density operation. When $\overline{\text{DDEN}}$ = 0, double density is selected. When $\overline{\text{DDEN}}$ = 1, single density is selected.
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice actuated motors.



FD1791A CERAMIC PACKAGE



FD1791B PLASTIC PACKAGE

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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U?NT 54 SEL

INPUT SIGNAL		PIN		OUTPUT PIN	SIGNAL	
$\overline{\text{INTERrupt}}$	$\overline{D7}$	3		C	D7	BOARD INTERRUPT ENABLE
$\overline{\text{DRQ}}$ data request	$\overline{D6}$	4		D	D6	N/A
SCL DBASE ~~2 SIDED~~	$\overline{D5}$	5		E	D5	DRIVE CHANGE
$\overline{\text{MINI}}$	$\overline{D4}$	6		F	D4	N/A
$\overline{\text{2 SIDED}}$ ~~DRIVE~~	$\overline{D3}$	7		H	D3	N/A
~~CYLINDER~~ ~~HEAD~~ * $\overline{\text{SIDE}}$	$\overline{D2}$	8		J	D2	SIDE {1 = TOP, 0 = BOTTOM
$\overline{\text{DRIVE SELECT}}$	$\overline{D1}$	9		K	D1	DRIVE SELECT {11 = 4, 10 = 3, 01 = 2, 00 = 1
	$\overline{D0}$	10		L	D0	

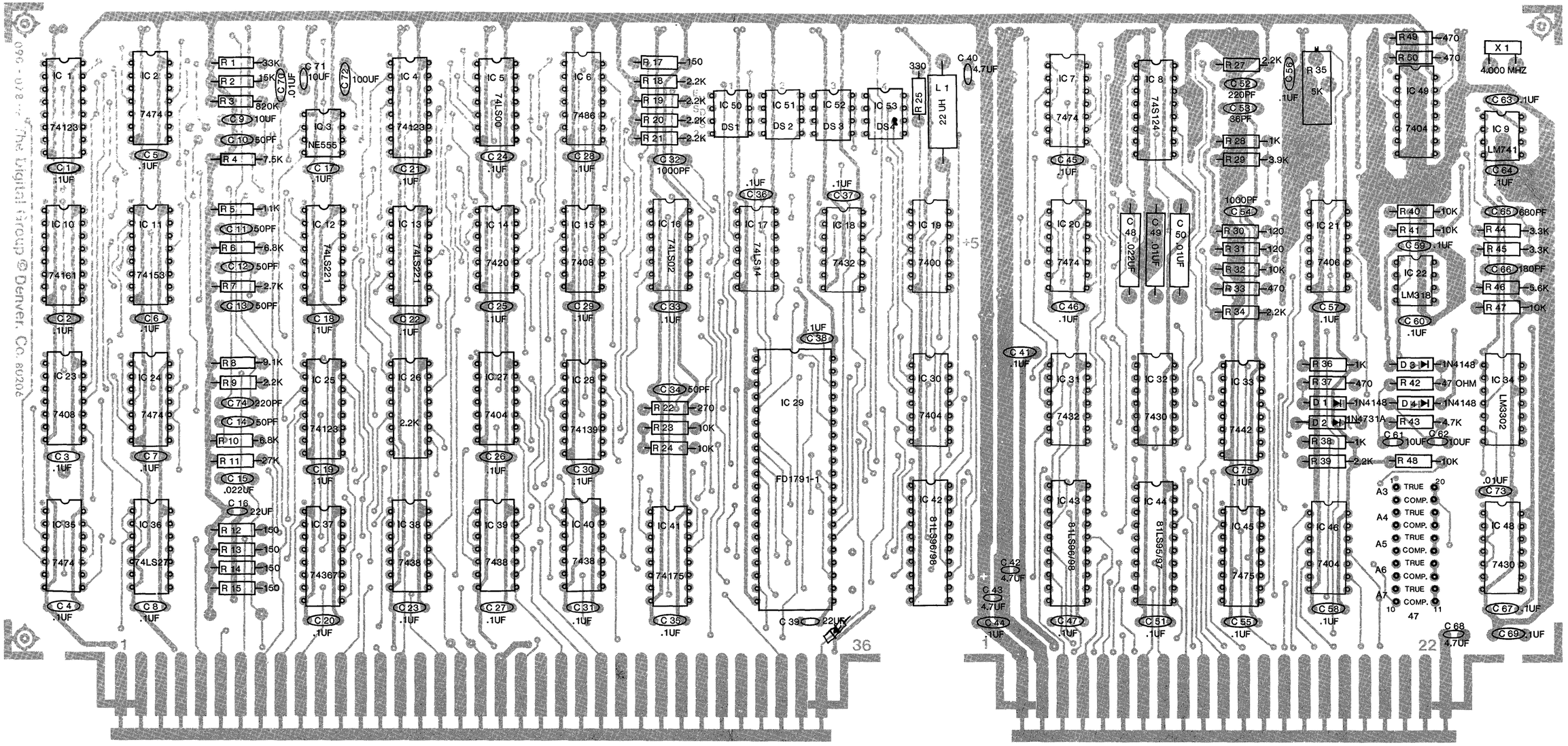
* IF DRIVE ~~SELECTED~~ ENABLE DIODE IS IN PLACE FOR SELECTED DRIVE
OTHERWISE A CONSTANT $\overline{1}$

TRACK FORMAT

(per DISKMON 3.00, "D.D. System Manual, p 60)

	SINGLE DENSITY (FM)			DOUBLE DENSITY (MFM)			
	FD 1791/ REQ	STD IBM 3740	MINI (3740)	MINI (OASIS)	FD 1791 REQ.	STD IBM System 34	MINI (System 34)	MINI (OASIS)
INDEX →								
GAP 4b		40 - FF 6 - 00	40 - FF 6 - 00	14 - FF 6 - 00		80 - 4E 12 - 00	80 - 4E 12 - 00	28 - 4E 12 - 00
INDEX MARK		1 - FC	1 - FC	1 - FC		3 - C2 (FC) 1 - FC	3 - C2 (FC) 1 - FC	3 - C2 (FC) 1 - FC
GAP 1	16 - FF	26 - FF	26 - FF	22 - FF	16 - 4E	50 - 4E	50 - 4E	44 - 4E
GAP 3b	MIN 4 - 00	6 - 00	6 - 00	6 - 00	MIN 8 - 00	12 - 00	12 - 00	8 - 00
SECTOR ID	1 - FE S A M E	1 - FE 1 - (TRACK) 0...) 1 - (SIDE: 0,1) 1 - (SECTOR: 1...) 1 - SEC. LENG. [0 = 128, 1 = 256, 2 = 512, 3 = 1024] 2 - CRC (F7)	1 - FE S A M E	1 - FE S A M E	3 - A1 (F5) 1 - FE S A M E	3 - A1 (F5) 1 - FE S A M E	3 - A1 (F5) 1 - FE S A M E	3 - A1 (F5) 1 - FE S A M E
GAP 2	11 - FF 6 - 00	11 - FF 6 - 00	11 - FF 6 - 00	11 - FF 6 - 00	22 - 4E 12 - 00	22 - 4E 12 - 00	22 - 4E 12 - 00	22 - 4E 12 - 00
SECTOR DATA	1 - FB [128, 256, 512, or 1024 DATA] 2 - CRC (F7)	1 - FB 128 - E5 (or 00's) 2 - CRC (F7)	1 - FB 128 - E5 (or 00's) 2 - CRC (F7)	1 - FB 128 - E5 (or 00's) 2 - CRC (F7)	3 - A1 (F5) 1 - FB [128, 256, 512, or 1024 data] 2 - CRC (F7)	3 - A1 (F5) 1 - FB 256 - 4E (or 00's) 2 - CRC (F7)	3 - A1 (F5) 1 - FB 256 - 4E (or 00's) 2 - CRC (F7)	3 - A1 (F5) 1 - FB 256 - 4E (or 00's) 2 - CRC (F7)
GAP 3	MIN 10 - FF	27 - FF	27 - FF	8 - FF	MIN 16 - 4E	54 - 4E	54 - 4E	16 - 4E
SECTOR LENGTH	169 x [STD 30 sec, MINI 18 sec] 297 x [17 sec, 10 sec] 533 x [9 sec, 5 sec] 1065 x [4 sec, 2 sec]	188 x 26 sec.	188 x 16 sec.	169 x 18 sec.	194 x [STD 53 s., MINI 32 s] 322 x [32 s, 19 s] 598 x [17 s, 10 s] 1090 x [9 s, 5 s]	372 x 26 sec	372 x 16 sec	330 x 18 sec
GAP 4a	128 [122 - FF, 69 - FF] 256 [143 - FF, 139 - FF] ~512 [395 - FF, 444 - FF] 1024 [932 - FF, 974 - FF]	~247 - FF	~44 - FF	~40 - FF	128 [118 - 4E, 26 - 4E] 256 [9C - 4E, 116 - 4E] ~512 [574 - 4E, 454 - 4E] 1024 [590 - 4E, 284 - 4E]	~598 - 4E	~152 - 4E	~222 - 4E
TOT:	5208 bytes: STD	3125 bytes: MINI			10,416 bytes: STD	6250 bytes: MINI		

DOUBLE DENSITY DISK CONTROLLER BOARD



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MOD. per GRAPHICS 25C p. 2

SPARE IC LIST

IC	TYPE-FUNCTION	SECTIONS NOT USED			
1	74123- one shot	9,10,11	30	7404-INV	12,13
6	7486-XOR	1,2,3	31	7432-OR	8,9,10
16	74LS02-NOR	1,2,3	34	3302-COMP	
17	74LS14-INV	12,13	46	7404-INV	12,13
23	7408-AND	1,2,3,4,5,6	49	7404-INV	1,2,8,9,10,11
26	2.2K Resistors	4,12,13			

LAST IC: 49
LAST RESISTOR: R50. R16 not used
LAST CAPACITOR: C75
LAST DIODE: D4

CONTRACT NO	THE DIGITAL GROUP
APPROVALS / DATE	DOUBLE DENSITY DISK CONTROLLER
DRAWN EJT 5/3/79	
CHECKED RW 5/23/79	
SIZE D	CODE IDENT NO.
DRAWING NO 090-078-B	
SCALE NONE	SHEET 1 OF 1