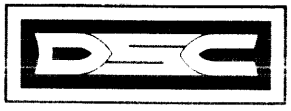
META 4™

series 16 computer system

Digital Scientific



THE DIGITAL SCIENTIFIC

META 4!™

SERIES 16

COMPUTER SYSTEM

Publication No. 7006MO

(Revision E)

PRELIMINARY
SYSTEM MANUAL

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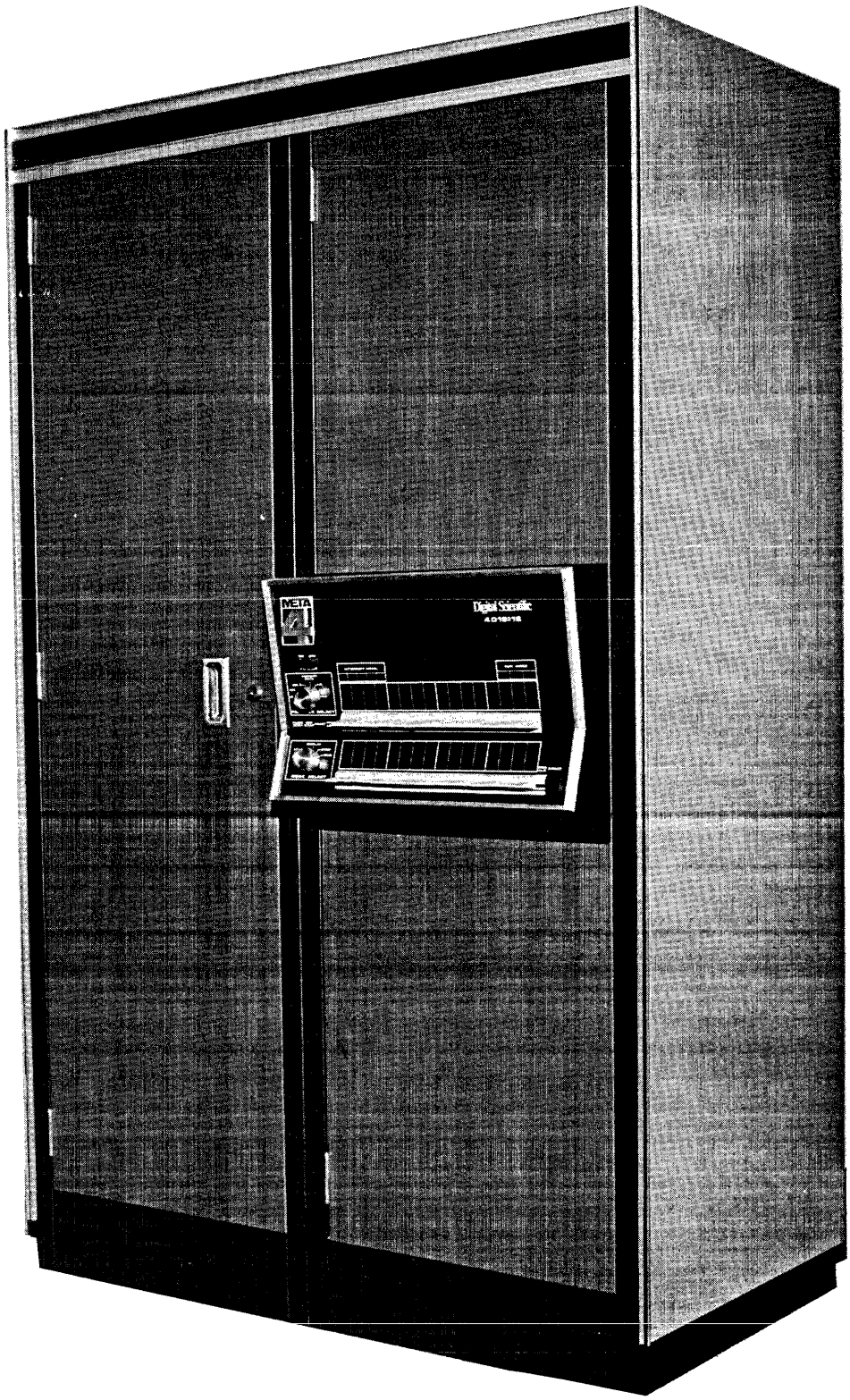

FRONTISPIECE. DIGITAL SCIENTIFIC META 4 COMPUTER SYSTEM

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DIGITAL SCIENTIFIC META 4 SERIES 16 COMPUTER SYSTEM

1.1 INTRODUCTION

1.1.1 META 4 SYSTEM CONCEPTS [1]

Organization of Digital Scientific's META 4 provides "general-purpose applicability" not only in a main memory instruction set, but also in its underlying, microprogram instruction set and in its flexible hardware organization. Contrary to the traditional computer organization, which bars the system designer from using registers and data paths other than as defined by a core memory instruction set, the system designer determines the number and functional assignment of general-purpose registers for data handling, external input/output, core memory input/output, accumulators or indexing, and the core memory instruction set to use.

The object of META 4 microprogramming capability is to allow the system designer to exercise the hardware as directly as possible without any intervening constraints. The system designer can act both as programmer and logic designer and can manipulate not only algorithms, but architecture.

The META 4 microprogrammed processor can be described as a "computer within a computer," where inner computer sequences emulate the machine language instructions for the outer computer and also execute special sequences not directly related to ordinary outer-machine instructions.

Conventional computer system organization limits the permissible interconnections among functional elements. Since machine language formats and logical organization of conventional computers are closely related, only one machine language instruction set can generally be executed efficiently and the full potential of possible interconnections among the functional elements cannot be realized.

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[1] Digital Scientific Corporation is indebted to Dr. Robert Rosin for permission to include some of his concepts on emulation in this introduction.

The META 4 microprogrammed computer organization offers the system designer an opportunity to match internal hardware facilities to a particular set of requirements.

Organization of the META 4 system is independent of the machine language instruction set in main memory and permits flexibility in specifying interconnections for functional elements such as arithmetic and Boolean operational units, registers, memory, and input/output devices.

For example, core memory instruction execution in every computer involves a sequence of steps such as:

- Place program location counter in memory address register.
- Fetch instruction from main memory and place in memory data register.
- Increment program location counter to prepare for next instruction.
- Move current instruction to instruction register.
- Decode current instruction and addressing mode.
- Calculate operand address.
- Place operand address in memory address register.
- Fetch operand from main memory and place in memory data register.
- Perform operation.

In a conventional computer, specially wired circuits control each sequence. The main memory instruction set is fixed and can be changed only by rewiring the computer.

In the META 4 Computer, a high-speed control memory replaces the specially wired circuitry. Control memory instructions (the microprogram) specify interconnections of functional elements. The control memory contents can be altered easily by the system designer, thus permitting great flexibility in specifying interconnections and allowing almost any desired main memory instruction set.

The META 4 microprogram emulator differs from a conventional computer program interpreter in several features, as described below.

- Microprograms are stored in a control memory which is distinct from the main memory of the emulated machine and is read-only memory (ROM) for the purpose of optimizing speed.

- Facilities to improve implementation and operation of emulators can be implemented at speeds comparable to those available from hardware. Examples are floating point arithmetic, character code conversion, and control panel operation.

The high-speed computing capability and flexibility are controlled by Digital Scientific Corporation's unique Read-Only Memory (ROM). ROM-controlled instruction cycle times are less than 90 nanoseconds, enabling 10 or more microintructions to be executed during each core memory cycle.

META 4 ROM microprograms (firmware) allow both core memory instructions and special algorithms to be executed much more rapidly than in other "general-purpose" devices. These factors — the computer organization and the high-speed ROM firmware — mean that applications which would normally require special hardware are standard capabilities for a META 4 Computer. For example:

- Instruction Set Emulator for Other Computers (with improved performance): An IBM 1130/1800 can be emulated completely and can be improved upon by adding floating-point instructions and register-to-register instructions.

- Channel Interface or Peripheral Equipment Controller for Other Computers: A disc controller with code and format conversion capabilities can be microprogrammed to operate at high speeds to provide economical standard interfacing to a variety of other computers.

- Communications Line Controller, Buffer, Editor, and Preprocessor: Serial-to-parallel conversion and data editing for multiple nonsynchronous or synchronous lines can be done at high speed to relieve a data processing system of a substantial overhead load.

- Digital Algorithm Processor: Convolution, fast Fourier transformation, correlation, high-level language compilation, or queue optimization algorithms can be executed at high speed, among multiple registers, using core memory for data only, not for program execution.

1.2 PROCESSOR ORGANIZATION

The processing unit (see Figure 1-1) consists of data registers, data processing logic paths, sequence control, input/output facilities, core memory, and integrated scratch-pad memory.

- Data Registers are 16-bit, integrated-circuit registers. Up to 31 directly addressable registers may be installed. During certain operations, data from the Read-Only Memory (ROM) may be used in place of register data.

  In Figure 1-1, registers for addresses 4 through 31 are optional. The requirement for and the choice of a particular type of register depend upon the user's system requirements for accumulator and scratch-pad registers, core memory registers, and input/output registers.

- Data Processing Logic Paths consist primarily of an arithmetic/Boolean unit, which processes data received via the A-bus and the B-bus, followed by a shifter unit, which transmits data to a destination register via the D-bus. The arithmetic unit is a 16-bit, high-speed parallel adder. Carry-in controls, together with overflow and carry-out condition register bits, allow multiple precision operation. The Boolean functions comprise the logical connectives AND, OR, or Exclusive OR. The shifter unit manipulates the result of either an arithmetic or a Boolean operation.

- Sequence Control for the processor is a program stored in high-speed, Read-Only Memory (ROM) and coded in a manner similar to Assembly language instructions for a conventional (hardware-sequenced) computer. Addresses in ROM instructions or in Register 2 (refer to page 1-8) are

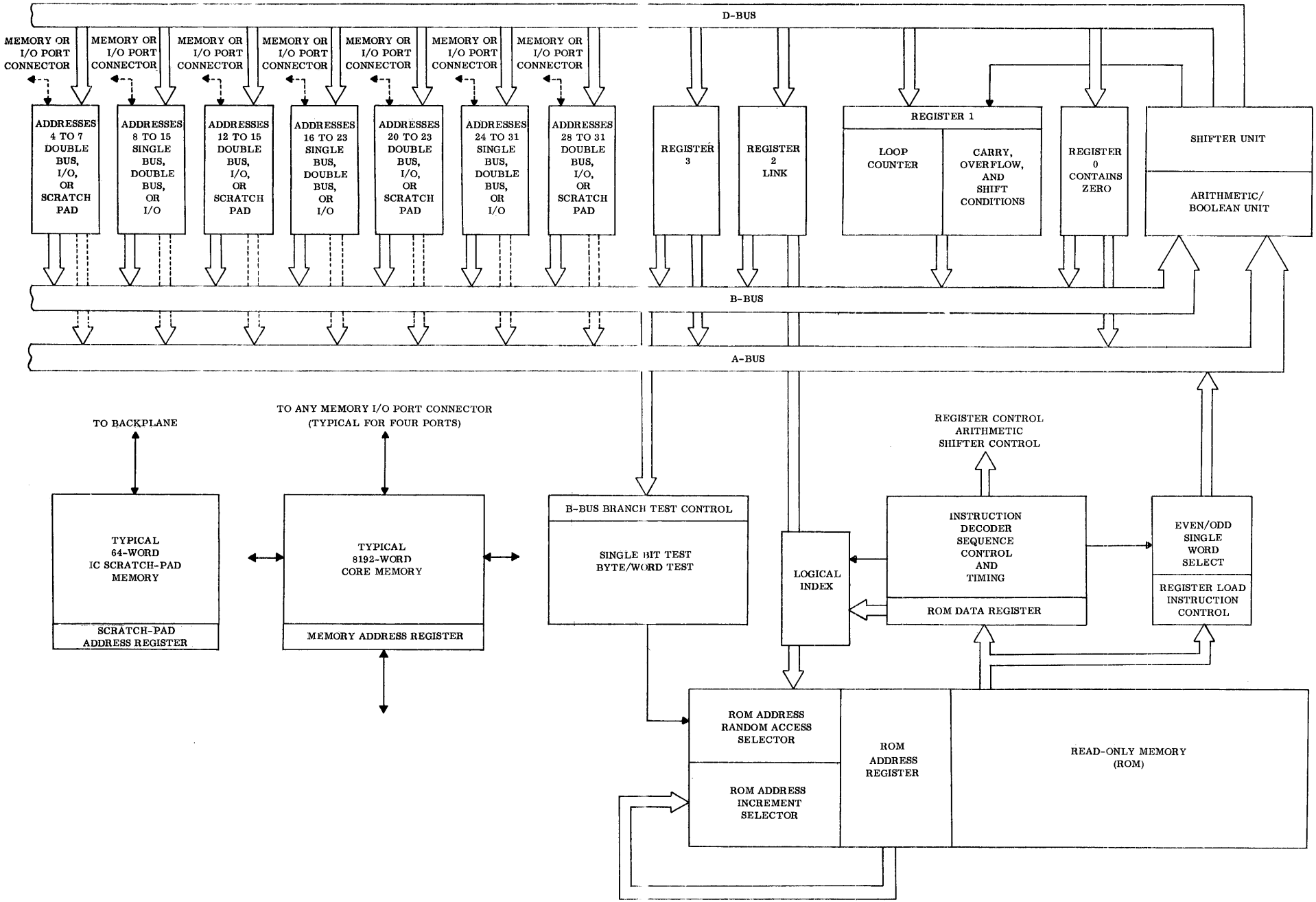


FIGURE 1-1. META 4 COMPUTER SYSTEM, BLOCK DIAGRAM

used by the branch-control unit to shift control between various sequences as the result of testing operations.

Any single bit of any addressable register may be tested for zero or nonzero, 8-bit or 16-bit fields may be tested for zero or nonzero, and a self-decrementing register may be tested for zero concurrently with operations of functional units.

- Input/Output Facilities are implemented at three levels:
  1. Direct cable connections to special types of directly addressable registers. The sequence control program may communicate with the system peripheral equipment through these registers.
  2. Chassis accepting standard controller for various peripheral equipment on a plug-in basis. No field wiring changes are required to add or delete peripheral equipment. Peripheral equipment controllers operate on a party-line I/O bus or directly to memory, as applicable.
  3. Direct access to core independently of the adapter chassis.

- Core Memory is operated by the control program through special registers and controls. Four standard memory ports allow multiple processors or special equipment to share memory. Each 8192-word bank of core memory is an independent unit. The processor can use additional memory registers to overlap accesses to several banks.

- Integrated Circuit Scratch-Pad Memory is operated by the control program through special registers.

1.3 PROCESSOR HARDWARE DESCRIPTIONS

The complete processor, including control memory, mounts in a 19-inch-wide rack housing and requires a 14-inch height for the logic and control memory chassis, a 14-inch height for up to two 8192-word memory banks, and a 14-inch height for the input/output adaptor chassis. Power supplies are normally mounted on the rear rails of a cabinet behind the processor chassis. (See Figure 1-2.)

Processor logic uses high-speed, emitter-coupled, integrated circuits for reliable operation at high speed. Major operation cycle time is 90 nanoseconds including

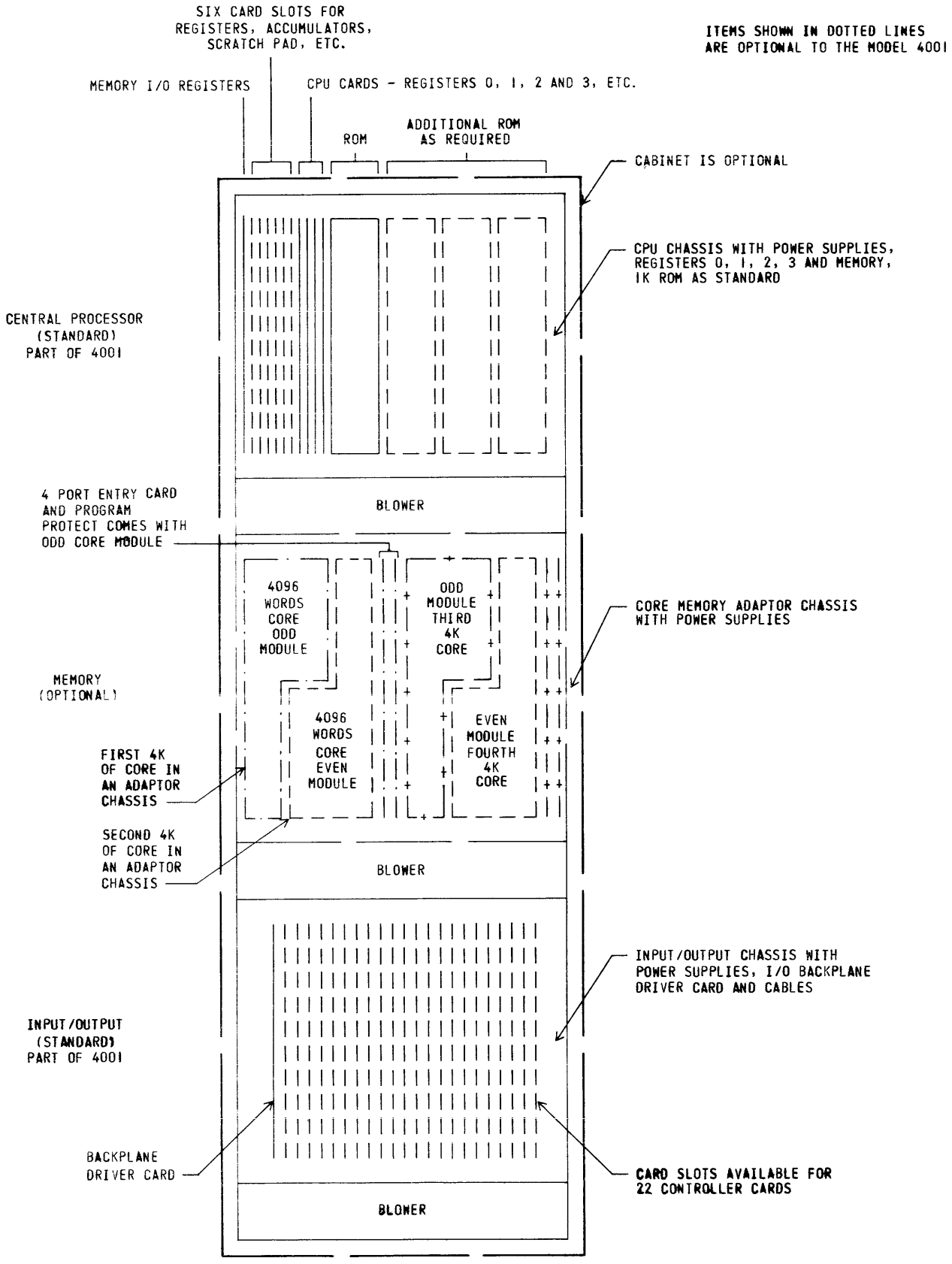


FIGURE 1-2. DIGITAL SCIENTIFIC META 4 SERIES 16 PROCESSOR, HARDWARE ORGANIZATION

Read-Only Memory (ROM) and data source register accesses, arithmetic and/or logical shift processing, and storage in a destination register.

Input/output logic uses a mixture of DTL and TTL integrated circuits.

1.3.1 REGISTERS AND SCRATCH-PAD MEMORY

Optional assemblies for directly addressed registers are available in several versions. Optional assemblies for integrated circuit scratch-pad memory are also available. Register types differ in internal bus connections, external I/O connections, and associated control functions. Register assemblies differ in the number and types of registers.

Type of Assembly	Number and Type of Registers per Assembly	Bus Connections
Double-Bus Accumulators/Index	4 read/write	B, D, A
Single-Bus Accumulators/Index	8 read/write	B, D
Input/Output	4 read, 4 write	B, D
Memory/Input/Output	2 read, 2 write for memory	B, D
	2 read, 2 write for I/O	B, D
Integrated Circuit Memory	64 read/write	B, D (both indirectly)

Registers may be data sources on the A-bus and B-bus and data destinations on the D-bus. Registers without physical connection to the A-bus will function as if the contents were zero for the A-bus only.

Register addresses 0, 1, 2, and 3 are assigned to the basic machine structure (see Figure 1-1). Addresses 4, 5, 6, and 7 are normally assigned to core memory and general I/O functions. All other addresses (8 through 31) are available for general use and are assigned in groups of four registers to seven connectors. Register assemblies containing eight assigned addresses can be installed only in the positions indicated and preclude use of the connector with redundant addresses.

The dedicated register address functions and connections are indicated below:

- Register 0 — Zero register: contains zero for operand use and serves as a dummy destination.

- Register 1 — Condition/Counter register: bits 8 through 15 contain a self-decrementing counter which may be initialized from the D-bus and decremented and tested by instruction control bits. Bits 0, 1, and 2 represent carry-out, overflow, and shift-out conditions and are not controllable from the D-bus. Bits 3 through 7 are fixed at zero. All register bits can be gated to the B-bus for operand use or program testing with the limitation that if Register 1 is specified as both the B-bus source and the D-bus destination of a single instruction the counter contents are indeterminate.

- Register 2 — Link register: serves as an address source for the ROM address selector during specific instructions. The Link register may be set from the D-bus and gated to the B-bus as required and may serve as a single bus accumulator if not required for ROM addressing.

- Register 3 — General-purpose, double-bus accumulator: has no special properties.

1.3.2 DATA PROCESSING LOGIC

1.3.2.1 Arithmetic Unit

The high-speed, 16-bit parallel adder operates in two's complement mode with carry input under program control. Carry-out and overflow automatically force the appropriate condition register bits. The carry-out and the overflow conditions may be tested in the Condition/Counter register. Carry input during an

instruction may be either inhibited, selected to be the previous carry output, or forced unconditionally. The ability to select a previous carry-out as a carry input simplifies multiple precision operation. The ability to force a carry input facilitates two's complement subtraction operations using logical complementing of operands rather than arithmetic complementing. If one's complement arithmetic operation is required, the processor program may use two-step additions in which the second step provides the end-around-carry characteristics of one's complement operations.

Two special addition operations expedite multiply and divide operations:

- Multiply step is addition which is completed only if the shift condition was previously true.
- Divide step is a trial addition where a negative sum inhibits changing the destination register.

1.3.2.2 Boolean Unit

The Boolean unit provides the logical connectives of AND, OR, or Exclusive OR of the A-bus and B-bus sources. Since Register 0 (containing zero) may be used as one of the operands, the Boolean unit may be used to zero registers using the AND function and to copy data using the OR function. An Exclusive OR using a data field from the ROM with all 16 bits true is used to complement data.

1.3.2.3 Shift Unit

The Shift unit provides bit manipulations on the output of the Arithmetic/Boolean unit. Both shift carry-out and shift carry-in for shift operations may be inhibited or selected independently. The shift carry-out status may be tested in the Condition/Counter register (Register 1) and represents the data spill from the most recent shift operation having carry-out enabled.

Shift operations comprise:

- One-place left or right shift
- Eight-place left or right shift/rotate
- Sign extend (copy bit 8 into bits 0 through 7)
- Average (one-place end-off right shift with arithmetic carry entering at left)
- No shift.

1.3.3 SEQUENCE CONTROLS AND READ-ONLY MEMORY (ROM)

The ROM is organized into 16-bit words. Addresses of instruction words must be even. Logically indexed references to data words may use either even or odd addresses. Up to 4096 single words may be installed in multiples of 1024 words. Each reference to the ROM calls up a double word so that access time is identical for single words and double words. Contents of the ROM can be readily modified or replaced in the field by either Digital Scientific Corporation or user personnel.

ROM instructions are executed in sequence unless a Branch causes transfer to another sequence. Branches occur in one of three ways: if specified during an RR format instruction, the next instruction is unconditionally taken from the address in the Link register (Register 2); if the counter section of the Condition/Counter register (Register 1) does not decrement to zero during an RR format instruction when tested, the next instruction is taken from the address in the Link register; if a Branch instruction to test various data or machine conditions is successful, the next instruction is taken from the data field of the instruction and logical indexing by the Link register is selectable.

A 4-bit field in the branch instruction "points" at any single bit of any addressable register. Branching may be selected for the true or false state of the specified bit, allowing tests for data sign, arithmetic carry/overflow, shift carry,

or any other single bit condition. Branching on zero or nonzero half words or single words is selected by a modified branch instruction.

The system is initialized by an externally applied signal which clears the I/O register controls and the ROM address register. Execution of the instruction at ROM address 000_{16} (normally a branch) can lead to a firmware routine that initializes other parts of the system such as internal working registers.

1.3.4 INPUT/OUTPUT TRANSMISSION AND CONTROL

Input/output transmission uses register reference instructions to gate 16 bits of input data directly to the B-bus and to store 16 bits of output data in the latch registers. Voltage-level shifter circuits between emitter-coupled logic and 0 to +5-volt levels are provided and an external signal may be used to enable output from the latch registers.

For input and output operations with the special I/O registers only:

- A program sequence pause occurs if the Pause control instruction bit is used. The input/output operation is delayed until a signal from the external equipment is received.

- A control signal is transmitted to the external equipment upon completion of the instruction if the input/output control instruction bit is used.

The Pause and I/O control bits are ignored if the referenced register is not an I/O-type register. Interlocked transmissions of data are readily made using control signals. Noninterlocked transmissions of data are made by not using one or both control bits.

Input/output pairs share a register address, but are not internally interconnected. Data in an output register cannot be gated back to the B-bus unless the input/output pair are strapped externally. Each pair shares a single ex-

terminal connector and any pair of one processor may be connected to any pair of the same or another processor by using a standard cable.

1.3.5 CORE MEMORY READ/WRITE TRANSMISSION AND CONTROL

Core memory read/write transmission uses register reference instructions in a manner similar to ordinary input/output register reference instructions. The two control instruction bits are interpreted as Read and Write rather than Pause and I/O control. The program sequence Pause function is implied as active when addressing any memory register.

The core memory is a coincident current system with a 900-nanosecond full cycle (read/write). Each completely independent bank of 4096 or 8192 words has four independent access ports. Port priority may be assigned at the discretion of the user and may differ between banks. Memory is protected against power failure.

One 16-bit output register is assigned as the core memory address register 4 and a second 16-bit output register is assigned as the core memory data output register 5. One of the corresponding 16-bit input register addresses is assigned to the core memory data input gate and the second corresponding 16-bit input register address is assigned to the input path for memory parity, protect status condition, and memory control signals. Input/output pairs are not externally connected except for memory data. Only one standard cable is required to connect the core memory with the four register paths. The memory data lines are bidirectional and are shared for input and output.

Standard memory feature:

- One 16-bit odd parity and one protect bit for each 18-bit storage word with automatic abort of Write instructions when the memory cell is protected and the Write control does not indicate a protected write status. Error conditions are transmitted to the processor.

1.4 PERIPHERAL EQUIPMENT

Peripheral equipment is operated either by dedicated registers or by a multiplexed signal bus using one pair of standard I/O registers. One output register is used for addressing and a second output register is used for control and data output. One of the corresponding input register addresses is used for data input and the second corresponding input register address is used for miscellaneous status and data bit inputs. Two standard cables are required to connect the two register paths with the chassis of the peripheral devices.

Standard peripheral devices are listed below:

- Keyboard/Printer
- IBM 1130 Computer Package, including SAC channel, control panel, and ROM containing instruction set firmware
- IBM 1800 Computer Data Channel
- 300-character-per-second Paper Tape Reader
- 50-character-per-second Paper Tape Punch
- 300-card-per-minute Hollerith Card Reader
- 200-card-per-minute Hollerith Card Punch and Reader combination
- Moveable Head Disc with Removeable Single Disc Pack
- 300-line-per-minute Line Printer
- Magnetic Tape Transports (1 x 2 controller, 7- or 9-track)
- Digital Input/Output Interface
- Analog-to-Digital (A/D) and Digital-to-Analog (D/A) Converters
- 300-step-per-second Incremental Plotter

- Teletype Line Adapters
- High-Speed Communications Line Adapters
- Computer-to-Computer Channel Interface for other manufacturers' computers
- Computer Channel Simulator for other manufacturers' computers
- Real-Time Clock/Time-of-Day Clock
- Stall Alarm/Timer

SECTION 2

READ-ONLY MEMORY (ROM) INSTRUCTIONS AND INSTRUCTION MODIFIERS

2.1 GENERAL DESCRIPTION

ROM instructions select specific operations of the arithmetic/Boolean, branch, and register load functions of the computer. Instructions are grouped into four categories, as shown in Figure 2-1.

- BR is the Branch format.
- RR is the Register-Register format.
- RI is the Register-Immediate format.
- RL is the Register Load format.

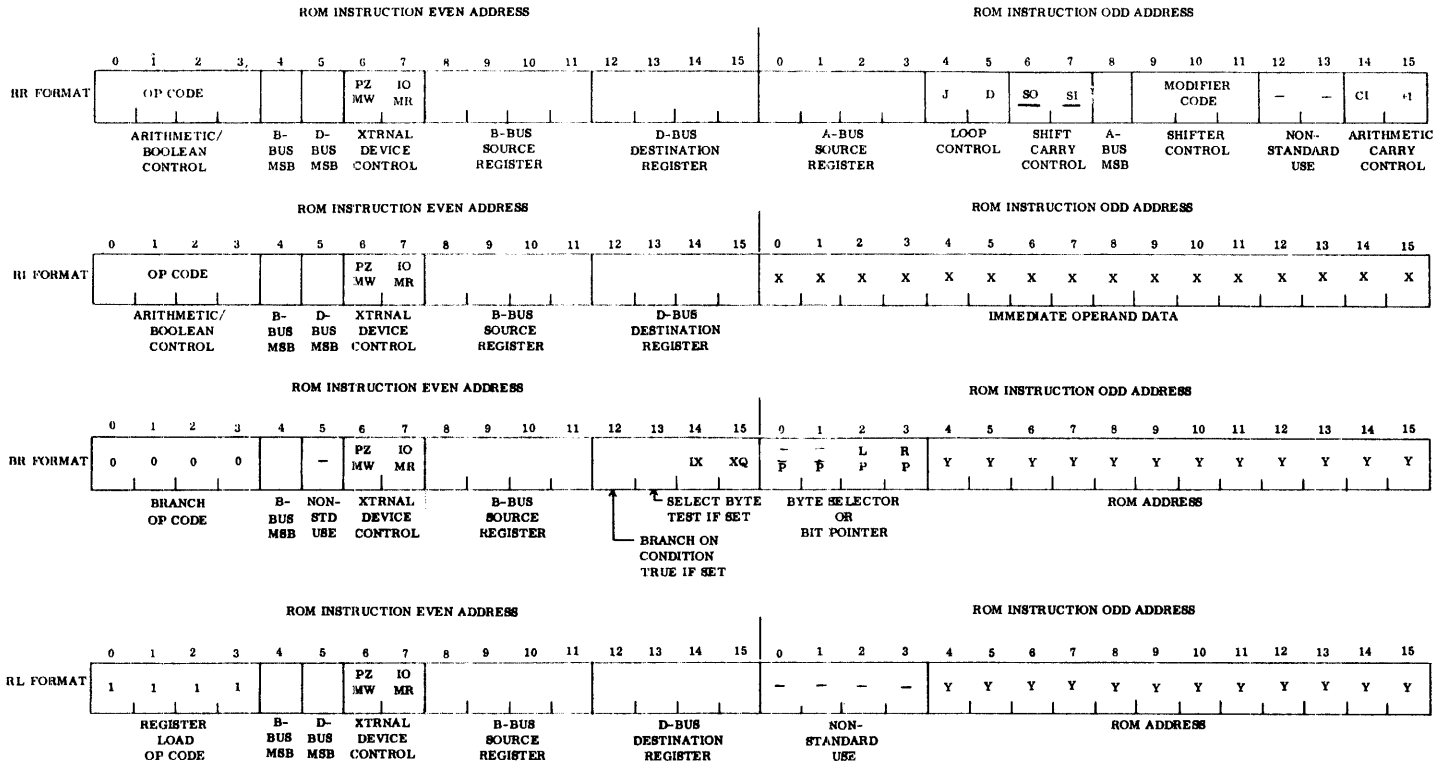
Instruction execution times are each one machine cycle (90 nanoseconds) except for the RL format instruction, which requires two machine cycles (180 nanoseconds).

ROM instruction modifiers select operations of the computer in addition to those selected by the basic instructions. Multiple modifiers may be specified and will operate within the basic instruction cycle times.

2.2

Modifiers are grouped into five categories, as follows:

- Shifter Control
- Arithmetic Control
- Branch Control
- Input/Output and Memory Control
- Instruction Loop Repeat Control



ARITHMETIC/BOOLEAN CONTROL OP CODES

MNEMONIC	HEXADECIMAL	FORMAT
BRZ BNZ	0	BR
AND	1	RR
OR	2	RR
XOR	3	RR
ADD	4	RR
MULT	5	RR
DIV	6	RR
ANDI	9	RI
ORI	A	RI
XORI	B	RI
ADDI	C	RI
LOAD	F	RL

SHIFTER CONTROL MODIFIER CODES

MNEMONIC	HEXADECIMAL
(NONE)	0
RI	1
LI	2
SK	3
SE	4
R8	5
L8	6
EX	7

MISCELLANEOUS MODIFIERS

SYMBOL	SYMBOL
CI	L
D	PZ
IO	R
IX	SI
J	SO
MR	XQ
MW	+1
W	

ARITHMETIC/BOOLEAN CONTROL ASSEMBLER PSEUDO OP CODES

MNEMONIC	HEXADECIMAL	FORMAT
COPY	2	RR
LDI	A	RR
NOP	B	RR
JMP	0	BR
SUBI	C	RI

ASSEMBLER CONTROL PSEUDO OP CODES

MNEMONIC
ORG
HEX
EQU
EQUR
END

MISCELLANEOUS SYMBLOS

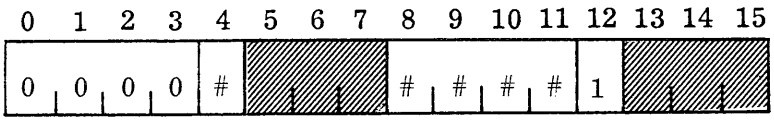
SYMBOLS
P
X
Y

ASSEMBLER SYMBOLS

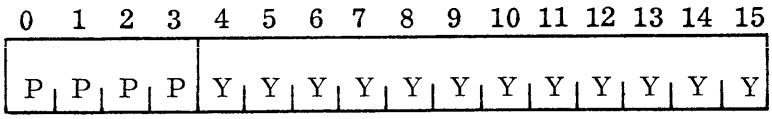
SYMBOL
* (asterisk)
. (period)
$ (dollar)
, (comma)
; (semi-colon)

FIGURE 2-1. META 4 SERIES 16 COMPUTER CONTROL INSTRUCTIONS

BNZ BRANCH IF NONZERO CONDITION **TIMING: 1 CYCLE(S)**



ROM INSTRUCTION, EVEN ADDRESS



ROM INSTRUCTION, ODD ADDRESS

The condition specified by modifiers or a register bit position is tested. If the test result is nonzero, the next instruction is taken from ROM location Y. If the test result is zero, the next sequential instruction is executed. The least significant bit of Y is ignored and interpreted as zero so that Y will be even. Registers and machine conditions are not changed by a Branch instruction.

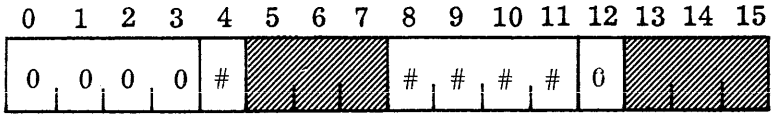
The 5-bit, B-bus source register address occupies bit positions 4, 8, 9, 10, 11 of the even ROM address.

VALID MODIFIERS:

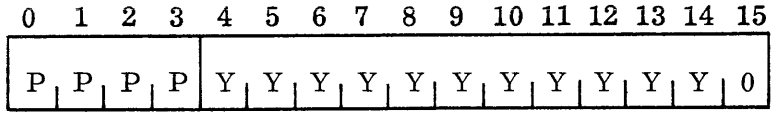
L R W IX XQ PZ IO (Refer also to page 2-4a.)

NOTE: See page 2-16, paragraph 2.3, for a discussion of instruction modifiers. Also, see page 3-4, paragraph 3.2.5, for a discussion of modifiers and their mnemonics as used in writing code for the firmware assembler.

BRZ BRANCH IF ZERO CONDITION **TIMING: 1 CYCLE(S)**



ROM INSTRUCTION, EVEN ADDRESS



ROM INSTRUCTION, ODD ADDRESS

The condition specified by modifiers or a register bit position is tested. If the test result is zero, the next instruction is taken from ROM location Y. If the test result is nonzero, the next sequential instruction is executed. The least significant bit of Y is ignored and interpreted as zero so that Y will be even. Registers and machine conditions are not changed by a Branch instruction.

The B-bus source register address occupies bit positions 4, 8, 9, 10, 11 of the even ROM address.

VALID MODIFIERS:

L R W IX XQ PZ IO (Refer also to page 2-4a.)

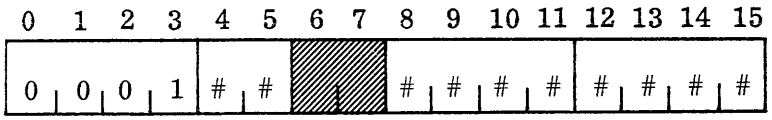
The use of mnemonics BNZ and BRZ is shown in the following table:

	Bits 0 - 7 zero Bits 8 - 15 zero	Bits 0 - 7 zero Bits 8 - 15 nonzero	Bits 0 - 7 nonzero Bits 8 - 15 zero	Bits 0 - 7 nonzero Bits 8 - 15 nonzero
BRZ W	•			
BRZ R	•		•	
BRZ L	•	•		
BRZ R, L	•	•	•	
BNZ R, L				•
BNZ R		•		•
BNZ L			•	•
BNZ W		•	•	•

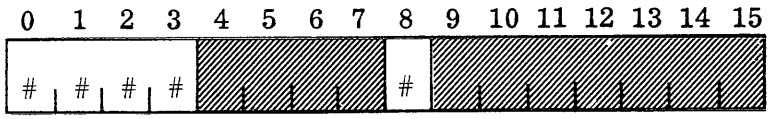
• indicates conditions for successful branch

NOTE: Branch testing of an I/O register input must not be attempted unless the I/O system is stabilized at the time. Stabilization is assured by input/output system data via timing interlocks. Stabilization is not assured for nonsynchronized inputs such as those used for interrupts. The effect of testing a nonstabilized input may be a ROM program branch to an address which is neither the next sequential address nor the expected branch address.

AND — AND B-SOURCE REGISTER WITH A-SOURCE REGISTER — TIMING: 1 CYCLE(S)



ROM INSTRUCTION, EVEN ADDRESS



ROM INSTRUCTION, ODD ADDRESS

The contents of the specified registers are placed on the B-bus and the A-bus, respectively. The AND'ed result is transmitted to the shifter unit for further processing and ultimate storage in the D-bus destination register. Only the D-bus destination register is changed by the AND instruction.

\# The B-bus source register address occupies bit positions 4, 8, 9, 10, 11 of the even ROM address

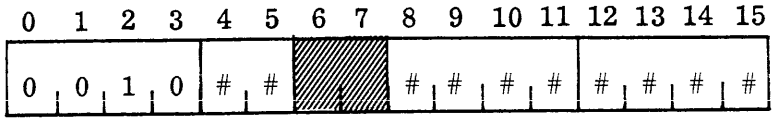
The D-bus destination register address occupies bit positions 5, 12, 13, 14, 15 of the even ROM address.

The A-bus source register address occupies bit positions 8, 0, 1, 2, 3 of the odd ROM address.

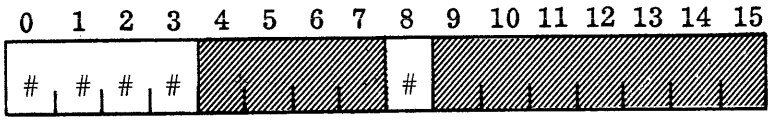
VALID MODIFIERS:

R1 L1 SK SE R8 L8 EX SI SO J D PZ IO MR MW

OR INCLUSIVE OR B-SOURCE REGISTER WITH A-SOURCE REGISTER TIMING: 1 CYCLE(S)



ROM INSTRUCTION, EVEN ADDRESS



ROM INSTRUCTION, ODD ADDRESS

The contents of the specified registers are placed on the B-bus and the A-bus, respectively. The Inclusive OR'ed result is transmitted to the shifter unit for further processing and ultimate storage in the D-bus destination register.

\# The B-bus source register address occupies bit positions 4, 8, 9, 10, 11 of the even ROM address.

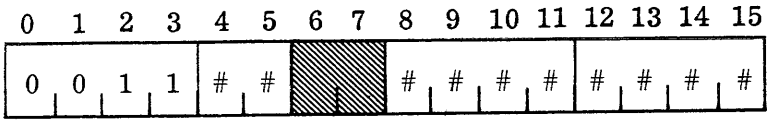
The D-bus destination register address occupies bit positions 5, 12, 13, 14, 15 of the even ROM address.

The A-bus source register address occupies bit positions 8, 0, 1, 2, 3 of the odd ROM address.

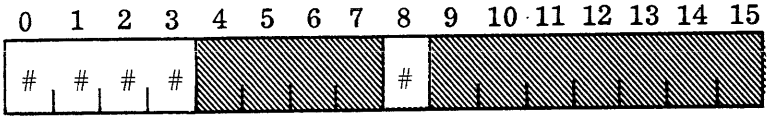
VALID MODIFIERS:

R1 L1 SK SE R8 L8 EX SI SO J D PZ IO MR MW

XOR — EXCLUSIVE OR B-SOURCE REGISTER WITH A-SOURCE REGISTER — **TIMING: 1 CYCLE(S)**



ROM INSTRUCTION, EVEN ADDRESS



ROM INSTRUCTION, ODD ADDRESS

The contents of the specified registers are placed on the B-bus and the A-bus, respectively. The Exclusive OR'ed result is transmitted to the shifter unit for further processing and ultimate storage in the D-bus destination register.

\# The B-bus source register address occupies bit positions 4, 8, 9, 10, 11 of the even ROM address.

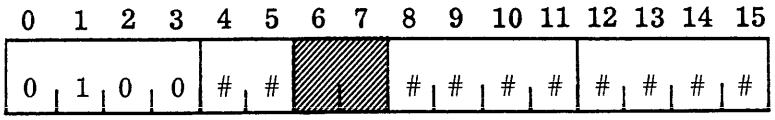
The D-bus destination register address occupies bit positions 5, 12, 13, 14, 15 of the even ROM address.

The A-bus source register address occupies bit positions 8, 0, 1, 2, 3 of the odd ROM ADDRESS.

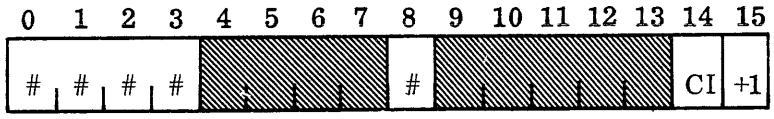
VALID MODIFIERS:

R1 L1 SK SE R8 L8 EX SI SO J D PZ IO MR MW

ADD — ADD B-SOURCE REGISTER TO A-SOURCE REGISTER — TIMING: 1 CYCLE(S)



ROM INSTRUCTION, EVEN ADDRESS



ROM INSTRUCTION, ODD ADDRESS

The contents of the specified registers are placed on the B-bus and A-bus, respectively. The sum is transmitted to the shifter unit for further processing and storage in the D-bus destination register. Addition is carried out in two's complement format. Carry input to the least significant bit is controlled by CI, which enables the previous carry condition as input, and +1, which forces carry input. The carry condition is set to correspond to the carry from bit 0 and the overflow condition is set to correspond to the Exclusive OR of the carries from bits 1 and 0. The D-bus destination register and the carry and overflow conditions are changed by the ADD instruction.

\# The B-bus source register address occupies bit positions 4, 8, 9, 10, 11 of the even ROM address.

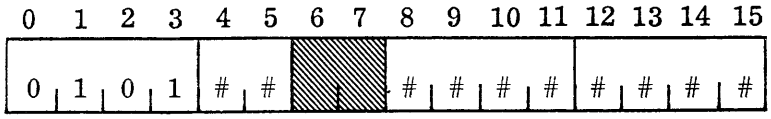
The D-bus destination register address occupies bit positions 5, 12, 13, 14, 15 of the even ROM address.

The A-bus source register address occupies bit positions 8, 0, 1, 2, 3 of the odd ROM address.

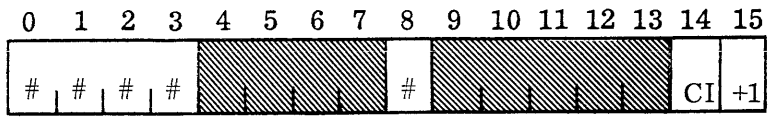
VALID MODIFIERS:

R1 L1 SK SE R8 L8 EX SI SO J D PZ IO MR MW CI +1

MULT — MULTIPLY STEP; CONDITIONAL ADD B-SOURCE REGISTER TO A-SOURCE REGISTER — TIMING: 1 CYCLE(S)



ROM INSTRUCTION, EVEN ADDRESS



ROM INSTRUCTION, ODD ADDRESS

The contents of the specified registers are placed on the B-bus and A-bus, respectively. The sum is transmitted to the shifter unit for further processing and storage in the D-bus destination register. If the shift condition is zero, prior to the MULT instruction execution, the B-bus data source is inhibited so that the A-bus data source passes through the adder unchanged.

Addition is carried out in two's complement format. Carry input to the least significant bit is controlled by CI, which enables the previous carry condition as input, and +1, which forces carry input. The carry condition is set to correspond to the carry from bit 0 and the overflow condition is set to correspond to the Exclusive OR of the carries from bits 1 and 0. The D-bus destination register and the carry and overflow conditions are changed by the MULT instruction.

\# The B-bus source register address occupies bit positions 4, 8, 9, 10, 11 of the even ROM address.

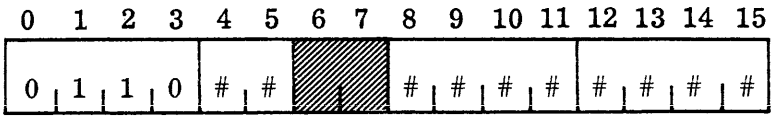
The D-bus destination register address occupies bit positions 5, 12, 13, 14, 15 of the even ROM address.

The A-bus source register address occupies bit positions 8, 0, 1, 2, 3 of the odd ROM address.

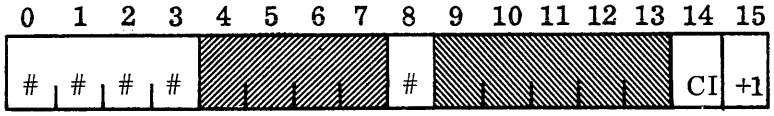
VALID MODIFIERS:

R1 L1 SK SE R8 L8 EX SI SO J D PZ IO MR MW CI +1

DIV DIVIDE STEP; TRIAL ADD B-SOURCE REGISTER TO A-SOURCE REGISTER TIMING: 1 CYCLE(S)



ROM INSTRUCTION, EVEN ADDRESS



ROM INSTRUCTION, ODD ADDRESS

The contents of the specified registers are placed on the B-bus and A-bus, respectively. The sum is transmitted to the shifter unit for further processing and storage in the D-bus destination register.

If the sign of the sum is negative, the destination register is not changed. Addition is carried out in two's complement format. Carry input to the least significant bit is controlled by CI, which enables the previous carry condition as input, and +1, which forces carry input. The carry condition is set to correspond to the carry from bit 0 and the overflow condition is set to correspond to the Exclusive OR of the carries from bits 1 and 0. The D-bus destination register and the carry and overflow conditions are changed by the DIV instruction.

Normal use of the DIV instruction requires that the SO modifier be specified concurrently in order to form the complement of the quotient, bit by bit.

\# The B-bus source register address occupies bit positions 4, 8, 9, 10, 11 of the even ROM address.

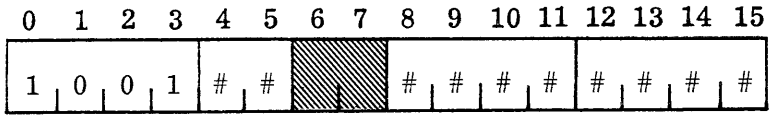
The D-bus destination register address occupies bit positions 5, 12, 13, 14, 15 of the even ROM address.

The A-bus source register address occupies bit positions 8, 0, 1, 2, 3 of the odd ROM address.

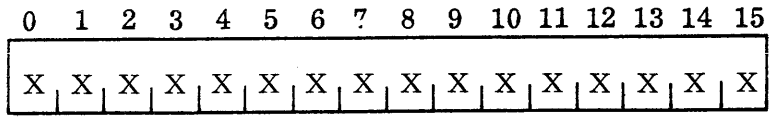
VALID MODIFIERS:

R1 L1 SK SE R8 L8 EX SI SO J D PZ IO MR MW CI +1

ANDI AND B-SOURCE REGISTER WITH IMMEDIATE OPERAND **TIMING: 1 CYCLE(S)**



ROM INSTRUCTION, EVEN ADDRESS



ROM INSTRUCTION, ODD ADDRESS

The contents of the specified register and the X field of the instruction are placed on the B-bus and A-bus, respectively. The AND'ed result is stored in the D-bus destination register.

\# The B-bus source register address occupies bit positions 4, 8, 9, 10, 11 of the even ROM address.

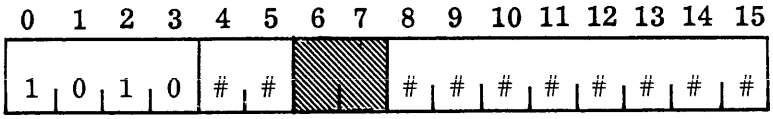
The D-bus destination register address occupies bit positions 5, 12, 13, 14, 15 of the even ROM address.

VALID MODIFIERS:

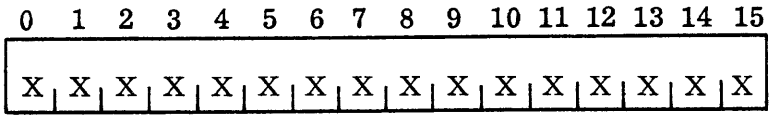
PZ IO MR MW

ORI INCLUSIVE OR B-SOURCE REGISTER WITH IMMEDIATE OPERAND

TIMING: 1 CYCLE(S)



ROM INSTRUCTION, EVEN ADDRESS



ROM INSTRUCTION, ODD ADDRESS

The contents of the specified register and the X field of the instruction are placed on the B-bus and the A-bus, respectively. The OR'ed result is stored in the D-bus destination register.

\# The B-bus source register address occupies bit positions 4, 8, 9, 10, 11 of the even ROM address.

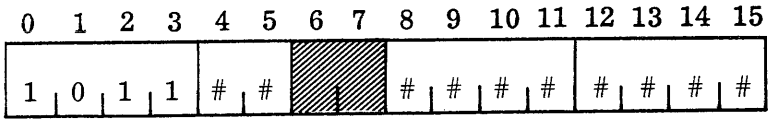
The D-bus destination register address occupies bit positions 5, 12, 13, 14, 15 of the even ROM address.

VALID MODIFIERS:

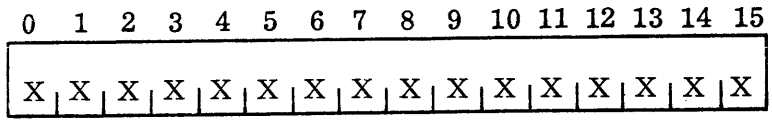
PZ IO MR MW

XORI EXCLUSIVE OR B-SOURCE REGISTER WITH IMMEDIATE OPERAND

TIMING: 1 CYCLE(S)



ROM INSTRUCTION, EVEN ADDRESS



ROM INSTRUCTION, ODD ADDRESS

The contents of the specified register and the X field of the instruction are placed on the B-bus and the A-bus, respectively. The XOR'ed result is stored in the D-bus destination register.

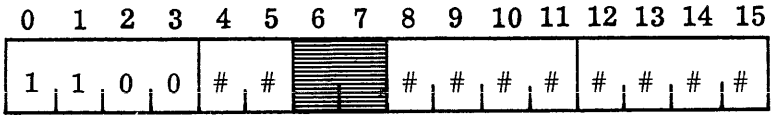
\# The B-bus source register address occupies bit positions 4, 8, 9, 10, 11 of the even ROM address.

The D-bus destination register address occupies bit positions 5, 12, 13, 14, 15 of the even ROM address.

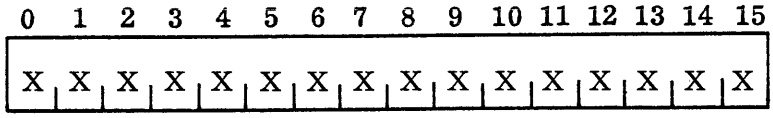
VALID MODIFIERS:

PZ IO MR MW

ADDI — ADD B-SOURCE REGISTER TO IMMEDIATE OPERAND — TIMING: 1 CYCLE(S)



ROM INSTRUCTION, EVEN ADDRESS



ROM INSTRUCTION, ODD ADDRESS

The contents of the specified register and the X field of the instruction are placed on the B-bus and the A-bus, respectively, and the sum is stored in the D-bus destination. Addition is carried out in two's complement format. The carry condition is set to correspond to the carry from bit 0 and the overflow is set to correspond to the Exclusive OR of the carries from bits 1 and 0. The D-bus register only may be changed by the ADDI instruction.

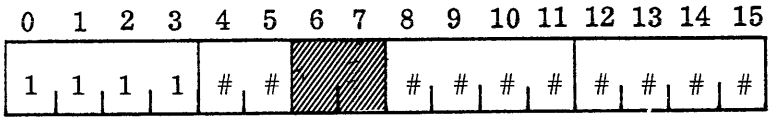
\# The B-bus source register address occupies bit positions 4, 8, 9, 10, 11 of the even ROM address.

The D-bus destination register address occupies bit positions 5, 12, 13, 14, 15 of the even ROM address.

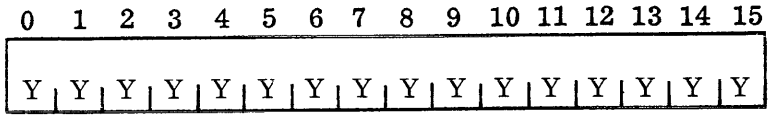
VALID MODIFIERS:

PZ IO MR MW

LOAD LOAD D-DESTINATION REGISTER WITH ROM FIELD **TIMING: 2 CYCLE(S)**



ROM INSTRUCTION, EVEN ADDRESS



ROM INSTRUCTION, ODD ADDRESS

The contents of the specified register and the contents of the ROM cell are placed on the B-bus and the A-bus, respectively. The Exclusive OR'ed result is stored in the D-bus destination register.

The ROM cell is specified by the contents of Register 2 logically indexed (Inclusive OR) with the Y field of the instruction.

\# The B-bus source register address occupies bit positions 4, 8, 9, 10, 11 of the even ROM address.

The D-bus destination register address occupies bit positions 5, 12, 13, 14, 15 of the even ROM address.

VALID MODIFIERS:

PZ IO MR MW

2.3 ROM INSTRUCTION MODIFIERS

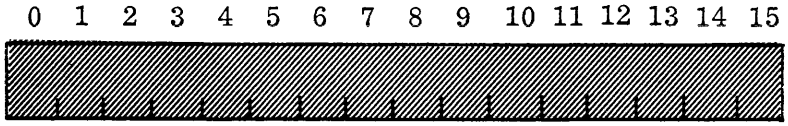
The ROM instruction modifiers are described in detail on the following pages. They are grouped as outlined below.

- Shifter Control Modifiers
- Arithmetic Control Modifiers
- Instruction Loop Repeat Control Modifiers
- Branch Control Modifiers
- Input/Output and Memory Control Modifiers

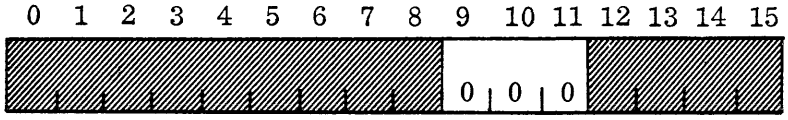
(No Shift Control Modifier)

APPLICABLE INSTRUCTION FORMAT(S): RR

TRANSMIT DATA WITHOUT MODIFICATION



ROM INSTRUCTION, EVEN ADDRESS



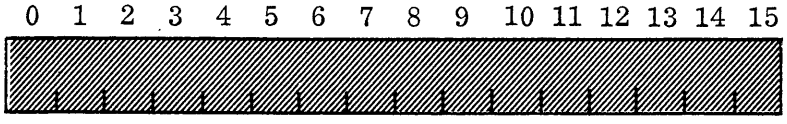
ROM INSTRUCTION, ODD ADDRESS

Output from the Arithmetic/Boolean unit is transmitted without modification.

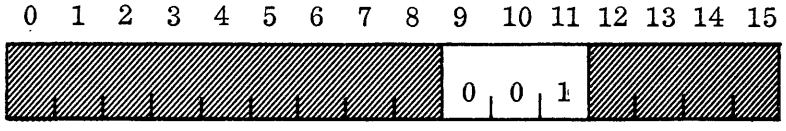
R1

APPLICABLE INSTRUCTION FORMAT(S): RR

SHIFT RIGHT ONE PLACE



ROM INSTRUCTION, EVEN ADDRESS



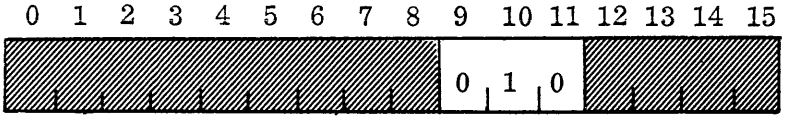
ROM INSTRUCTION, ODD ADDRESS

Output from the Arithmetic/Boolean unit is displaced right one place. Spill from bit 15 may be saved in the Shift Condition register bit by the SO modifier. Entry to bit 0 from the previous shift condition is controlled by the SI modifier.

L1 APPLICABLE INSTRUCTION FORMAT(S): RR

SHIFT LEFT ONE PLACE

ROM INSTRUCTION, EVEN ADDRESS

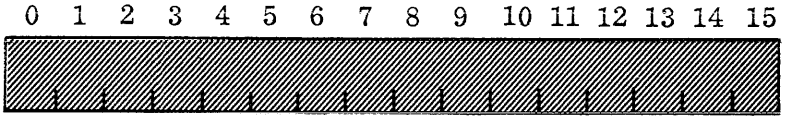


ROM INSTRUCTION, ODD ADDRESS

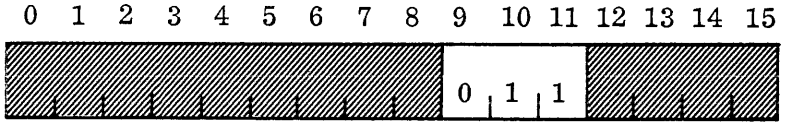
Output from the Arithmetic/Boolean unit is displaced left one place. Spill from bit 0 may be saved in the Shift Condition register bit by the SO modifier. Entry into bit 15 from the previous shift condition is controlled by the SI modifier.

SK APPLICABLE INSTRUCTION FORMAT(S): RR

SCALE



ROM INSTRUCTION, EVEN ADDRESS



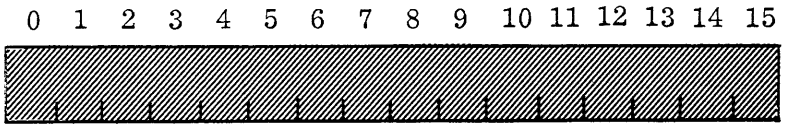
ROM INSTRUCTION, ODD ADDRESS

Output from the Arithmetic/Boolean unit is displaced one place to the right. Spill from bit 15 may be saved by the SO modifier. Entry to bit 0 is made from the current arithmetic carry during an ADD operation or from the Carry Condition register bit during operations other than ADD. If the SI modifier is specified concurrently with SK, entry to bit 15 is the OR between the Shift Condition register bit and the proper carry condition.

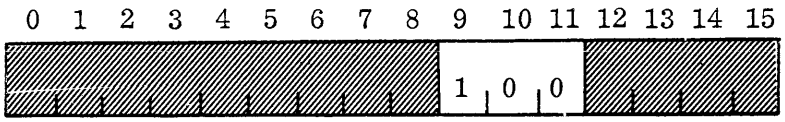
SE

APPLICABLE INSTRUCTION FORMAT(S): RR

SIGN EXTEND



ROM INSTRUCTION, EVEN ADDRESS



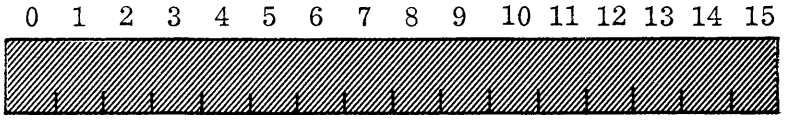
ROM INSTRUCTION, ODD ADDRESS

Output from the Arithmetic/Boolean unit is transmitted with bits 0 through 7 replaced by copies of bit position 8.

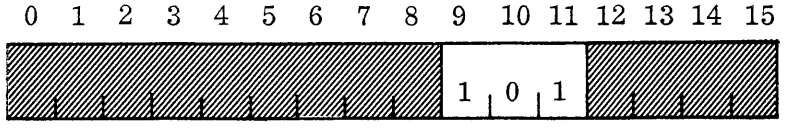
R8

APPLICABLE INSTRUCTION FORMAT(S): RR

SHIFT RIGHT EIGHT PLACES



ROM INSTRUCTION, EVEN ADDRESS

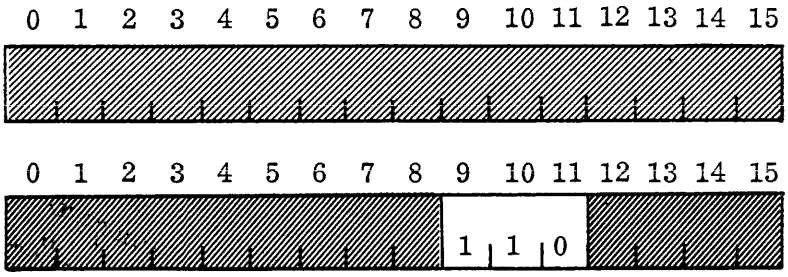


ROM INSTRUCTION, ODD ADDRESS

Output from the Arithmetic/Boolean unit is displaced right eight places. Spill from the right is lost; zeros enter at the left.

L8 APPLICABLE INSTRUCTION FORMAT(S): RR

SHIFT LEFT EIGHT PLACES



Output from the Arithmetic/Boolean unit is displaced left eight places. Spill from the left is lost; zeros enter at the right.

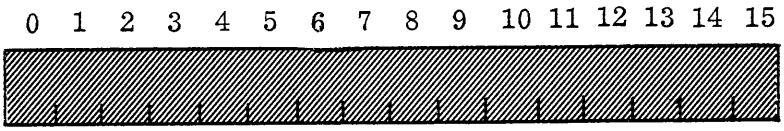
EX APPLICABLE INSTRUCTION FORMAT(S): RR

EXCHANGE BYTES

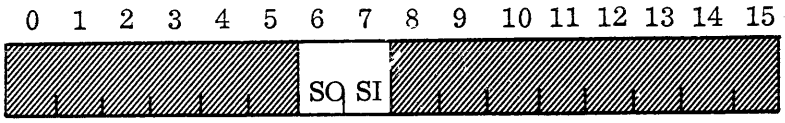
Output from the Arithmetic/Boolean unit is rotated eight places so that bits 0 through 7 and bits 8 through 15 are interchanged.

SO
SPILL SHIFTER TO SHIFT CARRY BIT APPLICABLE INSTRUCTION FORMAT(S): RR

SI
ENTER SHIFT CARRY BIT TO SHIFTER



ROM INSTRUCTION, EVEN ADDRESS



ROM INSTRUCTION, ODD ADDRESS

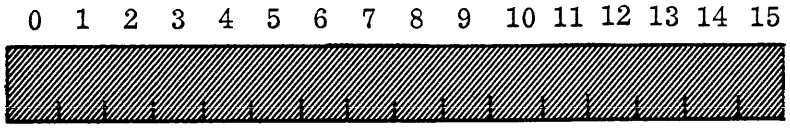
Shifter spill is always from either bit 0 or bit 15 of the operand. SO is effective for any shifter control modifier code. Spill is from bit 0 for no shift, L1, SE, and L8; and from bit 15 for R1, SK. R8, and EX. Refer to DIV instruction description for use of the SO modifier with operations other than a shift.

Shifter input is taken from the Shift Condition register bit when the SI modifier is specified. The SI modifier is enabled only for R1 and L1 modifiers and controls either bit 0 or bit 15 entry, as appropriate. If SK and SI modifiers are specified concurrently, the entry tc bit 0 is the OR between the shift condition and the arithmetic carry.

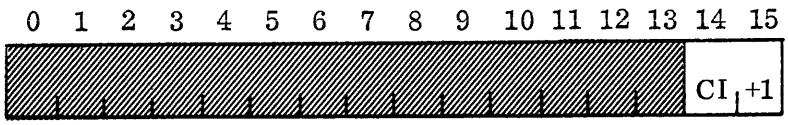
Circular shifts (end around) may be implemented by first executing a single shift operation (right or left, as appropriate) with register zero as the destination and SO specified. The shift carry bit will then be properly set so that subsequent shift operations with both SO and SI specified will be a circular shift.

CI
ENABLE ARITHMETIC CARRY INPUT APPLICABLE INSTRUCTION FORMAT(S): RR

+1
FORCE ARITHMETIC CARRY INPUT



ROM INSTRUCTION, EVEN ADDRESS



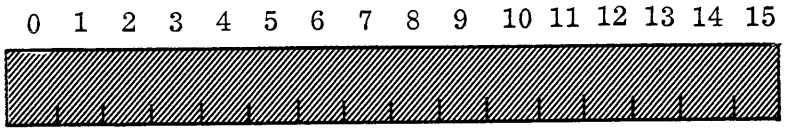
ROM INSTRUCTION, ODD ADDRESS

Carry input to the adder is controlled by CI and +1 modifiers. If neither is specified, the add is without carry input. If CI is specified, the previous carry condition is used as carry input to the least significant stage of the adder. If +1 is specified, a carry input is forced unconditionally.

D
DECREMENT COUNTER

APPLICABLE INSTRUCTION FORMAT(S): RR

J
JUMP ON COUNTER TEST



ROM INSTRUCTION, EVEN ADDRESS

ROM INSTRUCTION, ODD ADDRESS

The low-order 8 bits of Register 1 (the Counter) are decremented and tested using the J and D modifiers. If J is specified without D, a branch to the address specified by the contents of Register 2 (the Link) occurs.

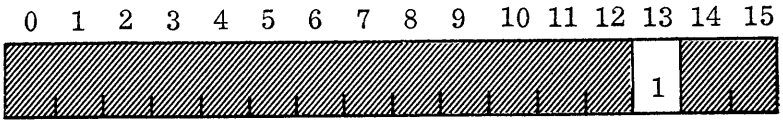
If D is specified without J, the counter is decremented at the conclusion of the instruction.

If J is specified concurrently with D, a branch to the address specified by the contents of Register 2 occurs unless the counter decrements to zero.

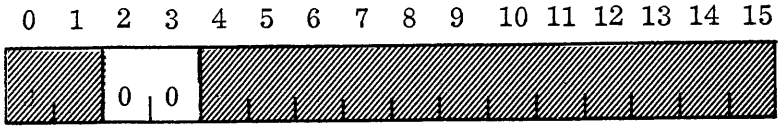
W

APPLICABLE INSTRUCTION FORMAT(S): BR

TEST WORD (RIGHT AND LEFT BYTES)



ROM INSTRUCTION, EVEN ADDRESS

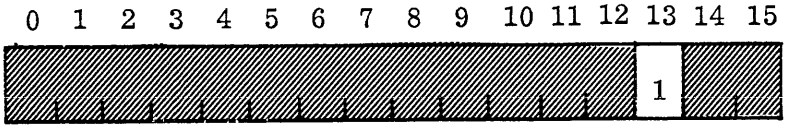


ROM INSTRUCTION, ODD ADDRESS

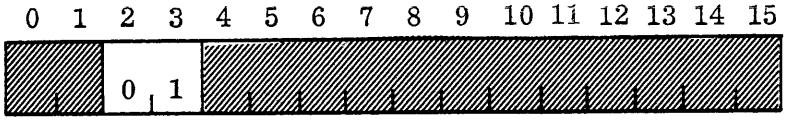
The contents of the register referenced by the B-bus address is tested for zero or nonzero condition.

R APPLICABLE INSTRUCTION FORMAT(S): BR

TEST RIGHT BYTE



ROM INSTRUCTION, EVEN ADDRESS

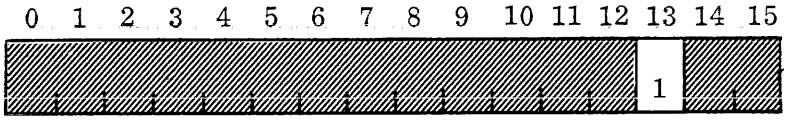


ROM INSTRUCTION, ODD ADDRESS

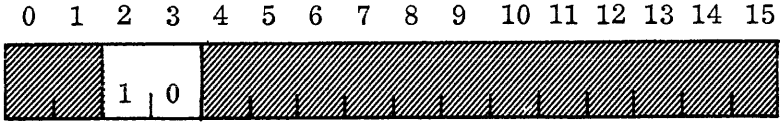
The right byte (8 bits) of the control of the register referenced by the B-bus address is tested for zero or nonzero condition.

L APPLICABLE INSTRUCTION FORMAT(S): BR

TEST LEFT BYTE



ROM INSTRUCTION, EVEN ADDRESS



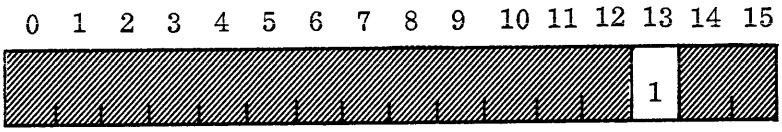
ROM INSTRUCTION, ODD ADDRESS

The left byte (8 bits) of the contents of the register referenced by the B-bus address is tested for zero or nonzero condition.

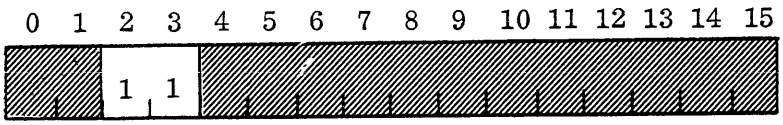
R, L

APPLICABLE INSTRUCTION FORMAT(S): BR

TEST RIGHT OR LEFT BYTE



ROM INSTRUCTION, EVEN ADDRESS



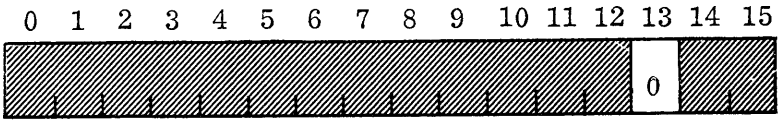
ROM INSTRUCTION, ODD ADDRESS

The right byte (8 bits) and left byte (8 bits) of the contents of the register referenced by the B-bus address are checked independently for zero or nonzero, with the Inclusive OR of the results tested for the zero or nonzero condition.

(No Byte Test Modifiers)

APPLICABLE INSTRUCTION FORMAT(S): BR

TEST SPECIFIED BIT



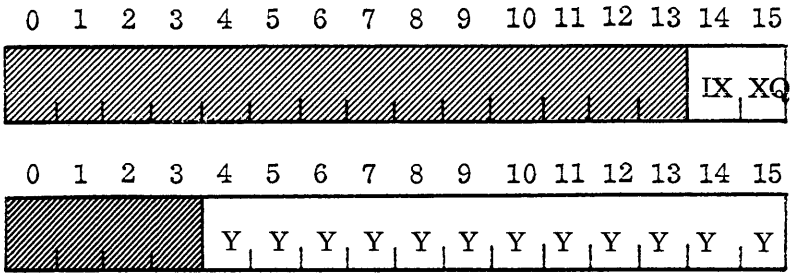
ROM INSTRUCTION, EVEN ADDRESS

ROM INSTRUCTION, ODD ADDRESS

One bit of the contents of the register referenced by the B-bus address and the P field is tested for zero or nonzero. This modifier enables a test and branch capability on any bit of any register and encompasses tests for even/odd, positive/negative, arithmetic carry, arithmetic overflow, and shift carry. The 4-bit P field (pointer) is decoded to define one of 16 bit positions with the tested word.

IX
LOGICAL INDEX APPLICABLE INSTRUCTION FORMAT(S): BR

XQ
EXECUTE ONE INSTRUCTION AFTER BRANCH



Logical indexing, if selected, OR's the contents of the Link register (Register 2) with the Y field to form the effective address.

Execute mode inhibits changing the ROM address register if the Branch instruction test is successful. The effective address is used directly for the execution of one instruction and the control sequence then reverts back to that instruction which would have been executed had the Branch not been successful, unless that one instruction is itself a Branch instruction. Multilevel Branch and Execute instructions may be used with ultimate reversion of control back to that instruction which would have been done with only one level of Branch and Execute. If a Branch without Execute is in the multilevel Branch sequence, then reversion of control will not occur if the Branch without Execute is successful.

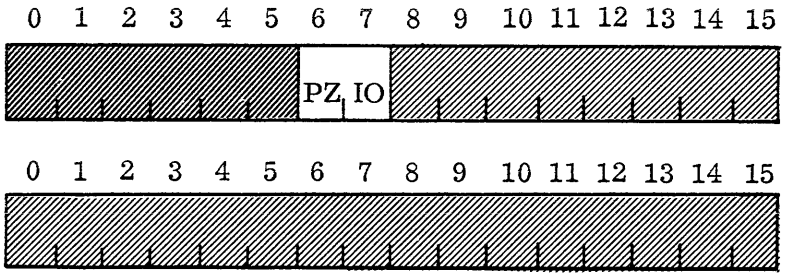
IO

OUTPUT I/O REGISTER CONTROL SIGNALS

APPLICABLE INSTRUCTION FORMAT(S): RR, RI, BR, RL

PZ

PROGRAM PAUSE FOR CONTROL SIGNAL INPUT



Pause occurs prior to any instruction execution; I/O control signals are output at the conclusion of the instruction execution.

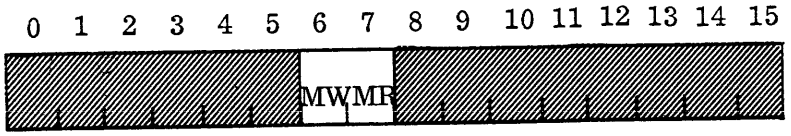
PZ and IO functions are enabled when any I/O register is specified by the B-bus or D-bus addresses. When PZ is specified, the program will pause until a control flip-flop is cleared by an external signal and the clearing pulse has terminated. If more than one I/O register is specified by the bus addresses, the pause condition occurs while any one of the associated control flip-flops is set and the control signal is output on all of the control lines. When IO is specified, the I/O register control line signals are output and control flip-flops are set. The control flip-flops are cleared by the external equipment or by the computer Master Clear.

Note the possible conflicts: MW and MR modifiers use the same control word bit positions as PZ and IO modifiers. Conflicts may occur if memory and I/O registers are specified concurrently.

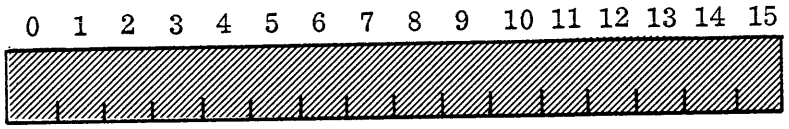
MW
INITIATE MEMORY WRITE

APPLICABLE INSTRUCTION FORMAT(S): RR, RI
BR, RL

MR
INITIATE MEMORY READ



ROM INSTRUCTION, EVEN ADDRESS



ROM INSTRUCTION, ODD ADDRESS

MW and MR modifiers are recognized only when a core memory register is specified by the D-bus address. When either MW or MR is specified, control flip-flops are set. The control flip-flops are cleared by signals from the memory. While the control flip-flops set, the program will pause if the register is specified on either the B-bus or the D-bus and will resume when the memory has completed the appropriate portions of a cycle.

Note the possible conflicts: When MR and MW are specified simultaneously, the core memory will change protect bits to the state specified by bit 15 of the memory data register. Data will be restored without change. PZ and IO modifiers use the same control word bit positions as MW and MR modifiers. Conflicts may occur if memory and I/O registers are addressed concurrently.

A timing restriction must be observed when reading data from the Memory Data register subsequent to initiation of a Read operation while loading the Memory Address register. Memory Read data is valid only if read during the approximately 8 ROM instruction cycles following initiation of the Memory Read cycle. Refer to the Memory Interface description (page 1-12) for Memory Read timing details. Memory Read data is destroyed by a Memory Write command.

SECTION 3

META 4 SERIES 16 COMPUTER FIRMWARE ASSEMBLER CODING

3.1 FUNCTION

The Firmware Assembler converts mnemonics, labels, constants, and modifiers into the various bit patterns of the instructions of the Digital Scientific META 4 Series 16 Computer

3.2 CODING

Instructions, modifiers, and comments are coded on the Firmware Assembler Coding Form (see Figure 3-1).

3.2.1 LOCATION FIELD

Columns 1 - 4 contain an absolute location, a label, or spaces. Absolute locations are represented in (even) hexadecimal notation, left-justified within the field and followed by a $. Labels are left-justified within the field and are terminated by a space. Labels may contain any combination of four alphanumeric characters. An * in column 1 indicates a full line of comments.

3.2.2 OPERATION FIELD

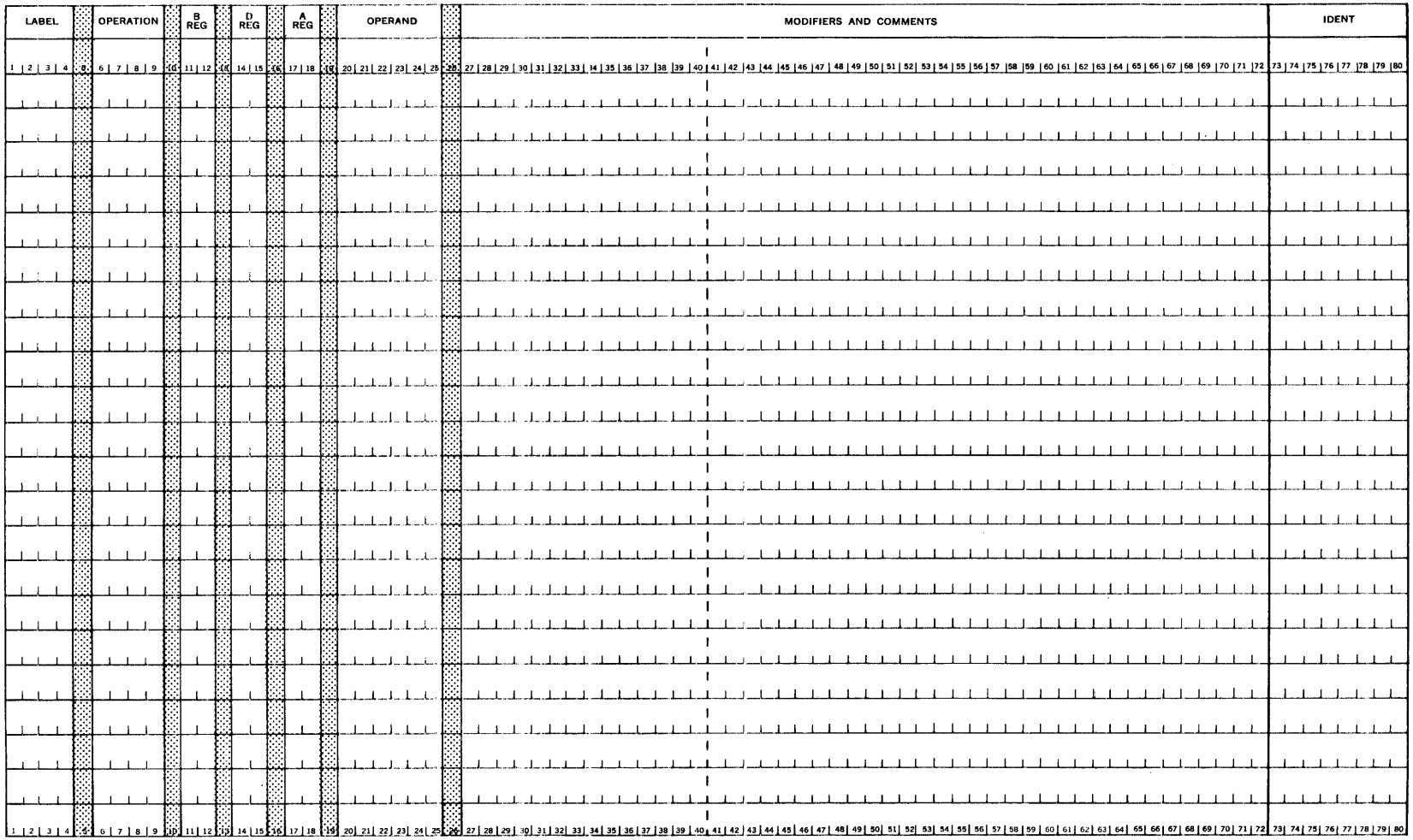
Columns 6 - 9 contain an operation mnemonic or pseudo-op, left-justified within the field. (Operation mnemonics are described in Section 2.) Assembler pseudo-ops are described below.

MNEMONIC	OP_{16}	DESCRIPTION	FORMAT
COPY	2	Copy the B Source to the Destination	RR
LDI	A	Load the Data Field into the Destination	RR
NOP	B	Copy the Data Field to Destination Zero	RR
JMP	0	Unconditional Jump (Test Source Zero = 0)	BR

Digital Scientific META 4 T.M. COMPUTER
FIRMWARE ASSEMBLER CODING FORM

PROGRAM _____ DATE _____

PROGRAMMED BY _____ SHEET _____ OF _____



DSC8A 12/69

FIGURE 3-1. FIRMWARE ASSEMBLER CODING FORM

(Assembler Pseudo-Ops Continued)

MNEMONIC	OP_{16}	DESCRIPTION	FORMAT
SUBI	C	Subtract Immediate: use the Two's Complement of the Data Field in an ADDI Instruction	RI
ORG		Set Origin Address of Routine	
HEX		Permit HEX Data (tables, etc.) to be Assembled with a Routine	
EQU		Equate a Tag with an Absolute Address, Value, or Another Tag	
EQUR		Equate a 2 Character Tag with a Register	
LIST		Allows Control of Output Listing if OFF is Specified in the Operand Field. The Listing will be Terminated until a List Card with ON is Encountered. The On Mode is Assumed if No List Card is Present	
PNCH		Allows Control of Output Binary Cards. Same Rules as List Card	
EJCT		Causes Listing to Start at the Top of a New Page	
END		Terminate Assembly	

3.2.3 SOURCE AND DESTINATION FIELD (BDA)

Columns 11 - 18 contain the source and destination registers to be used in the instruction.

Columns 11 - 12 = B source

Columns 14 - 15 = D destination

Columns 17 - 18 = A source of branch pointer

3.2.4 OPERAND FIELD

Columns 20 - 25 are used as a data field for BR and IM format instructions and must contain a label or a hexadecimal constant. Labels and constants are left-justified within the field and are terminated by a space or a $. A constant must be followed by a $. After a HEX pseudo-op, two 16-bit fields may be specified using a comma (,) as separator. A slash (/) separating two labels indicates that the low order 8 bits of each label are linked to form a 16-bit field.

3.2.5 MODIFIERS

Modifiers are added to instructions in order to control operations in addition to the basic function defined by the operation mnemonic. Modifiers must start in column 27 and can be in any order, spaced by commas. The first space encountered by the Assembler after column 26 indicates that all remaining characters are comments. The instruction modifiers are listed below.

MNEMONIC		VALID FOR
ARITH		
CI	Enable Arithmetic Carry-In	Add, Multiply, Divide
+1	Force Carry-In to 1 and Enable	Add, Multiply, Divide
SHIFT		
SO	Enable Shift Out	All RR Instructions
SI	Enable Shift In	All RR Instructions
L1	Shift Left 1	All RR Instructions
R1	Shift Right 1	All RR Instructions
L8	Shift Left 8	All RR Instructions
R8	Shift Right 8	All RR Instructions
EX	Exchange Bytes	All RR Instructions
SK (SCALE)	Shift Right 1 with Arithmetic Carry Shifted In	All RR Instructions
SE	Sign Extend (copy bit 8 into bits 0 - 7)	All RR Instructions
LOOP		
J	Jump through Link (if D set, jump only if count = 0)	All RR Instructions

MNEMONIC		VALID FOR
BRANCH		
R	Test Right Byte 0	BRZ, BNZ
L	Test Left Byte 0	BRZ, BNZ
W	Test Word 0	BRZ, BNZ
0 through F followed by $	Test Specified Bit Position (0 - 15) 0	BRZ, BNZ
IX	Logical Index With Link	BNZ, BRZ
XQ	Execute One Instruction Out Of Sequence	BNZ, BRZ
I/O		
MR	Initiate Memory Read	All Instructions
MW	Initiate Memory Write	All Instructions
PZ	Pause	All Instructions
IO	Initiate I/O Operations	All Instructions

3.2.6 COMMENT FIELD

Columns 27 - 72 may contain any combination of alphanumeric or special characters.

3.2.7 ASSEMBLER ERROR FLAGS

The following error flags will be typed in the three columns at the left of the assembly listing if any of the conditions are true.

U	Undefined Symbol
R	Undefined Register
O	Invalid Operation
M	Illegal Modifier
D	Duplicate Symbol
F	Format Error
S	Symbol Table Overflow
H	HEX Conversion Error

SECTION 4

META 4 SERIES 16 COMPUTER SYSTEM

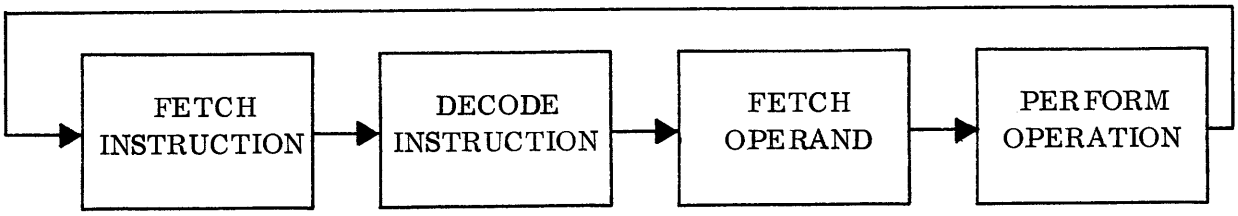
PROGRAMMING TECHNIQUES AND EXAMPLES

4.1 EMULATION

Instruction sets for other computers are readily implemented in the Digital Scientific META 4 Computer's Read-Only Memory (ROM). Firmware performs the operations which are carried out by hardware in computers that lack control memories for sequencing.

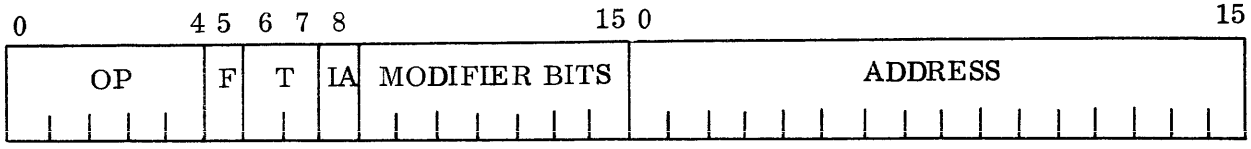
Emulating an IBM 1130 Computer typifies the programming techniques for 16-bit systems. The sequences shown here have been prepared directly from instruction descriptions in the programming manual and from other sources such as timing charts.

The basic functions of any emulation are diagrammed below:



Formats for the instruction to be emulated are as follows.

4.1.1 LONG INSTRUCTION FORMAT (IBM 1130)



OP (OPeration) Code. These five bits specify the operation to be performed.

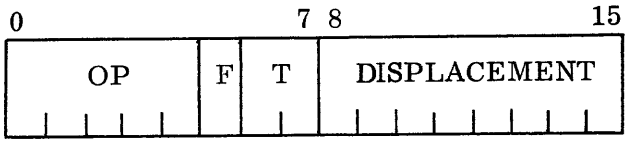
F (Format). The F bit controls the instruction format: 0 = short format; 1 = long format.

T (Tag). These two bits specify the register to be used in effective address generation: 00 indicates the I-register; 01 indicates XR1; 10 indicates XR2; and 11 indicates XR3.

IA (Indirect Address). A zero indicates a direct address (contained in the second word). A 1 bit designates an indirect address.

Modifier Bits. Bit positions 9 through 15 have various uses as modifiers.

4.1.2 SHORT INSTRUCTION FORMAT (IBM 1130)



The first eight bits of the short format are the same as those of the long format. The second eight bits contain the displacement, which is added to data in the register specified by the tag bits to form the effective address. Bit 8 is treated as a sign bit and is extended into bit positions 0 through 7 to obtain a 16-bit number. Negative numbers are expressed as two's complement.

4.1.3 INSTRUCTION DECODING

The instructions decode readily using a table look-up on eight bits of the instruction, which establishes not only the operation to be performed, but also the format and the method of operand-effective address generation.

Since most operations require an operand, a table can be devised to direct the reading of the operand and the subsequent operation to be performed. Using the Subtract instruction as an example, assume that Subtract is located at 044_{16} of the ROM and that the Operand Read routines are located as follows:

SUBROUTINE NAME	ROM ADDRESS
ORSI (Operand Read, Short Format, Relative to I-Register)	F00
ORS1 (Operand Read, Short Format, Index Register 1)	F08
ORS2 (Operand Read, Short Format, Index Register 2)	F10
ORS3 (Operand Read, Short Format, Index Register 3)	F18
OPRL (Operand Read, Long Format)	F40

The table is written in META 4 Computer Assembly language.

The Assembler generates the following table:

```
LOC.  INST.    LAB.  OP   BR DR AR OPRAND MODIFIERS AND COMMENTS

0E90 44004408  E90SHEX          S ORS1,S ORS1          SUBTRACT
0E92 44104418      HEX          S ORS2,S ORS3
0E94 44404440      HEX          S OPRL,S OPRL
0E96 44404440      HEX          S OPRL,S OPRL
0E98 6C206C28      HEX          SD OWS1,SD OWS1        DBL SUB
0E9A 6C306C38      HEX          SD OWS2,SD OWS3
0E9C 6C486C48      HEX          SD OPWL,SD OPWL
0E9E 6C486C48      HEX          SD OPWL,SD OPWL
```

A META 4 Computer address from the table may not exceed eight bits; therefore, the most significant portion of the address must be "understood" by the program using the logical index facility.

Referencing the numbers adjacent to the boxes of the sample flowcharts as a guide (see Figures 4-1 through 4-3, pages 4-9 through 4-14), the cracking and execution of an instruction proceed as follows. The area between F00 and FFF can be addressed by the least significant eight bits indexed logically by F00. This area is designated P1 and is used for preprocessing such as computing operand addresses, etc.

4.1.3.1 System Conditions

- A Subtract instruction (OP 10010) is located at core storage location 500.
- The accumulator contains 300_{16}.
- The operand in location 520 contains 150_{16}.
- Index Register 2 contains 510_{16}.

4.1.3.2 META 4 Computer Registers

The META 4 Computer registers are listed with their nomenclature on the following page.

META 4 COMPUTER REGISTERS

I	=	SIMULATED INSTRUCTION ADDRESS REGISTER	=	17_{16}
M	=	MEMORY ADDRESS REGISTER	=	4
T	=	INTERRUPT REGISTER	=	6
K	=	PRIORITY MASK REGISTER	=	$1D_{16}$
S	=	SCRATCH REGISTER	=	3
D	=	MEMORY DATA REGISTER	=	5
L	=	LINK REGISTER	=	2
U	=	TEMPORARY ACCUMULATOR	=	16_{16}
A	=	SIMULATED 1130 ACCUMULATOR	=	14_{16}
C	=	CONDITION /COUNTER REGISTER	=	1
X	=	SIMULATED 1130 STATUS REGISTER	=	18_{16}
Q	=	ACCUMULATOR EXTENSION	=	15_{16}
1	=	INDEX REGISTER 1	=	$1A_{16}$
2	=	INDEX REGISTER 2	=	$1B_{16}$
3	=	INDEX REGISTER 3	=	$1C_{16}$

NOTE

In the following listings, Register 1 is incorrectly assigned as the Link register and Register 2 is incorrectly assigned as the Contition/Counter register.

RNI

```
LOC.  INST.    LAB.  OP   BR DR AR OPRAND MODIFIERS AND COMMENTS

022E 29740000 RNI   COPY I  M            MR,             MOVE I TO MEM ADDRESS
              *                    AND READ NEXT INST
0230 28030000       COPY K  S                            MOVE MASK
0232 10633000       AND  Y  S  S                         AND MASK WITH RAW INT
0234 003C025A       BTC  S        INT    W,              VALID INTERRUPT
0236 CC770001       ADDI I  I     1$                     INCREMENT I
0238 20520050       COPY D  L            R8,             SHIFT OP CODE INTO L
023A F0020E00       LOAD 0  L     E00$                   LOAD THE LINK FROM
              *                    THE TABLE STARTING AT
              *                    E00 AND INDEXED BY
              *                    THE CONTENTS OF L
023C 00020F00       JMP           F00$   IX              JUMP TO P1 AREA
```

ORSI

```
LOC.  INST.    LAB.  OP   BR DR AR OPRAND MODIFIERS AND COMMENTS

              *ORSI COMPUTES THE OPERAND ADDRESS OF
              *SHORT FORMAT INSTRUCTIONS (REL TO I) AND
              *INITIATTEES THE READ OF THE OPERAND
0F00 20530040 ORSI COPY D  S            SE,             EXTEND SIGN OF DISP
0F02 41347080      ADD  S  M  I         MR,             COMP OP ADDR,READ OP
0F04 20220050      COPY L  L            R8              SHIFT P2 ADDRESS INTO
              *                    LOW 8 OF LINK
0F06 00020000      JMP           0$     IX              JUMP TO P2 AREA
              *                    INDEXED BY CONT OF L
              *
```

ORS1, ORS2, AND ORS3

```
LOC.  INST.    LAB.  OP   BR DR AR OPRAND MODIFIERS AND COMMENTS

                     *ORS1,ORS2 AND ORS3 ARE IDENTICAL TO ORSI
                     *EXCEPT FOR INDEX REGISTER USED TO
                     *COMPUTE THE EFFECTIVE ADDRESS (EA) OF
                     * HE OPERAND
0F08 20530040 ORS1   COPY D  S              SE,
0F0A 49A43000        ADD  1  M  S           MR,
0F0C 20220050        COPY L  L              R8,
0F0E 00020000        JMP                0$  IX
0F10 20530040 ORS2   COPY D  S              SE,
0F12 49B43000        ADD  2  M  S           MR,
0F14 20220050        COPY L  L              R8,
0F16 00020000        JMP                0$  IX,
0F18 20530040 ORS3   COPY D  S              SE;
0F1A 49C43000        ADD  3  M  S           MR,
0F1C 20220050        COPY L  L              R8,
0F1E 00020000        JMP                0$  IX,
```

ADD

```
LOC.  INST.    LAB.  OP   BR DR AR OPRAND MODIFIERS AND COMMENTS

0040 44544080 A      ADD  U  A  A                        ADD DATA TO (A)
0042 00000048        JMP             AOV
                     *
```

SUBTRACT

```
LOC.  INST.    LAB.  OP   BR DR AR OPRAND MODIFIERS AND COMMENTS

0044 B456FFFF S      XORI D  U     FFFF$                 1 S COMP DATA
0046 4C644081        ADD  U  A  A        +1              ADD WITH PLUS 1 = SUB
0048 0010104C AOV    BFC  C     1  *+2                   BR IF NO OVERFLOW
004A AC880001        ORI  X  X     1$                    SET OVFL INDICATOR
004C 00180052        BTC  C     0  *+3                   BR IF CARRY = 1
004E 9C880001        ANDI X  X     1$                    CLEAR CARRY INDICATOR
0050 0000022E        JMP           RNI
0052 AC880002        ORI  X  X     2$                    SET CARRY INDICATOR
0054 0000022E        JMP           RNI
```

MULTIPLY

```
LOC.  INST.    LAB.  OP   BR DR AR OPRAND MODIFIERS AND COMMENTS

007A A0010010 M     LDI      C      10$                      LOAD 16 INTO COUNTER
007C 08480126       BTC  A        0  MNEG                     BR IF MULTIPLIER NEG
007E 2C450210       COPY A   Q              SO,R1             COPY MULT. INTO Q, RIGHT
                    *                                        SHIFTED 1 PLACE TO COND.
                    *                                        A SUBSEQUENT MULT. STEP
0080 A0030000       LDI      S      0$                       SET SIGN PLUS
0082 0000012C       JMP              MNEG+3
                    *MNEG IS A CONTINUATION OF THE MULTIPLY
                    *ROUTINE IN P2 AREA
0126 BC45FFFF MNEG  XORI A   Q      FFFF$                    COMP MULTIPLIER TO(Q)
0128 4C550211       ADD  Q   Q  0           +1,R1,SO,        +1 FOR 2'S COMP
                    *ALSO SHIFT MULTIPLIER TO CONDITION A
                    *SUBSEQUENT MULTIPLY STEP
012A A0030001       LDI      S      1$                       SET SIGN NEG
012C A4040000       LDI      A      0$
012E 00580134       BTC  D        0  *+3                    BR IF DATA NEG
0130 24560000       COPY D   U                               POS MULTIPLICAND
0132 0000013A       JMP              *+4
0134 B456FFFF       XORI D   U      FFFF$                    COMP MULTIPLIER
0136 CC660001       ADDI U   U      1$
0138 B0330001       XORI S   S      1$                       FLIP SIGN
013A A002013C       LDI      L      MTOP
013C 5C644290 MTOP  MULT U   A  A           SO,R1,           SHIFT AND ADD
                    *CONDITIONED BY PREVIOUS CONTENTS OF THE
                    *SHIFT FLIP-FLOP
013E 2C550F10       COPY Q   Q              SO,R1,SI,D,J,    FORM LEAST
                    *SIGNIFICANT  PORTION OF RESULT,ALSO
                    *SHIFT NEXT BIT OF MULTIPLIER TO SHIFT FF
                    *THEN LOOP UNTIL COMPLETION
0140 0030022E       BFC  S        0  RNI                    EXIT IF POS
0142 BC55FFFF       XORI Q   Q      FFFF$                    COMP RESULT
0144 BC44FFFF       XORI A   A      FFFF$
0146 CC550001       ADDI Q   Q      1$

0148 4C440002       ADD  A   A  0           CI
014A 0000022E       JMP              RNI
```

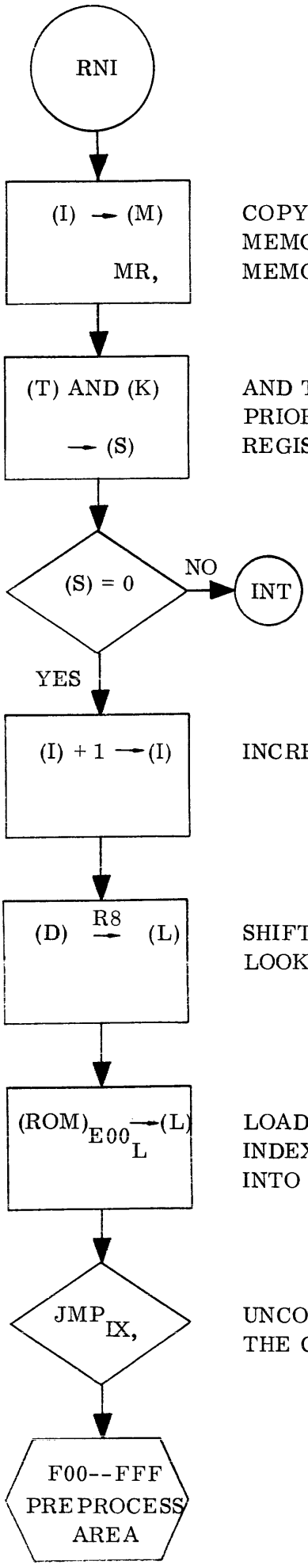
DIVIDE

```
LOC.  INST.   LAB.  OP   BR DR AR OPRAND MODIFIERS AND COMMENTS

0084 A0010010 D     LDI      C      10$                    LOAD 16 INTO COUNTER
0086 A0020164       LDI      L      DTOP                   TOP OF LOOP TO LINK
0088 0848014C       BTC  A        0  DNEG                   BR IF DIVIDEND NEG
008A A0030000       LDI      S      0$                     SET SIGN IF QUOT&DIV
008C 24560000       COPY D   U                             SAVE MEMORY DATA
008E 08680162       BNZ  U        0  DN                     BRANCH IF DIVISOR NEG
0090 086C015C       BNZ  U           DNZ     W            BR IF DIVISOR NOT ZERO
0092 AC880001 OVFL  ORI  X    X      1$                     SET OVFL BIT
0094 0000022E       JMP              RNI
                   *DNEG IS A CONTINUATION OF THE DIVIDE
                   *ROUTINE IN P2 AREA
014C 00540092 DNEG  BFC  D           OVFL    W            BR IF DIVISOR ZERO
014E BC44FFFF       XORI A    A      FFFF$                  COMP DIVIDEND
0150 BC55FFFF       XORI Q    Q      FFFF$
0152 CC550001       ADDI Q    Q      1$
0154 4C440002       ADD  A    A   0          CI
0156 24560000       COPY D    U                            SAVE MEMORY DATA
0158 A0030003       LDI      S      3$                     SET SIGN OF QUOT&DIV
015A 08680162       BNZ  U        0  DN                     BR IF DIVISOR NEG
015C BC66FFFF DNZ   XORI U    U      FFFF$                  COMPLEMENT DIVISOR TO
015E CC660001       ADDI U    U      1$                     PERFORM SUBTRACT
0160 00000164       JMP              DTOP
0162 B0330001 DN    XORI S    S      1$                     FLIP SIGN OF QUOTIENT
0164 6C644280 DTOP  DIV  U    A   A          SO,            TRIAL SUBTRACT OR
                   *                  SUBTRACT
0166 2C550320       COPY Q    Q              L1,SO,SI       SHIFT DIVIDEND
                   *BIT IN AND SHIFT DIVIDEND BIT OUT
0168 2C440D20       COPY A    A              L1,SI,D,J,     SHIFT DIVIDEND
                   *AND LOOP TO COMPLETION
016A 6C644280       DIV  U    A   A          SO,            LAST CYCLE REM NOW OK
016C 2C560320       COPY Q    U              L1,SO,SI       COMPLETE QUOT TO L
016E 00102092       BFC  C        2  OVFL                   SHIFT FF =0 = OVFL
0170 0030E182       BFC  S        F  RPOS                   BR IF REMAINDER PLUS
0172 BC45FFFF       XORI A    Q      FFFF$                  COMP REMAINDER
0174 CC550001       ADDI Q    Q      1$                     REMAINDER
0176 08600186 QUOT  BFC  U        0  UNEG                   QUOT IS NEG OK FOR OV
0178 0038F17E       BTC  S        F  QNEG                   BR,SIGN OF QUOT NEG
017A BC64FFFF       XORI U    A      FFFF$                  QUOTIENT TO A
017C 0000022E       JMP              RNI                    EXIT
017E CC640001 QNEG  ADDI U    A      1$                     CONVERT 1'S COMP QUOT
                   *                  TO 2'S COMP QUOTIENT
0180 0000022E       JMP              RNI                    EXIT
0182 2C450000 RPOS  COPY A    Q                             REMAINDER TO (Q)
0184 08680178       BTC  U        0  QUOT+1                 QUOT IS POS
0186 0030F092 UNEG  BFC  S        F  OVFL                   IF FORMED QUOTIENT IS
                   *NEGATIVE AND THE SIGN OF THE QUOTIENT IS
                   *POSITIVE,AN OVERFLOW IS INDICATED
0188 CC698001       SUBI U    O      7FFF$                  IF THE FORMED QUOT
                   *IS NEGATIVE AND THE SIGN OF THE QUOTIENT
                   *IS NEGATIVE AN OVERFLOW IS INDICATED
                   *EXCEPT FOR -2TO THE 15TH
018A 0894017E       BFC  O           QNEG    W,             TEST FOR -2TO 15TH
018C 00000092       JMP              OVFL
```

SAMPLE FLOWCHARTS

ARE INCLUDED ON THE FOLLOWING PAGES



1. COPY INSTRUCTION ADDRESS REGISTER INTO MEMORY ADDRESS REGISTER AND INITIATE MEMORY READ.
2. AND THE INTERRUPT REGISTER (T) WITH THE PRIORITY MASK REGISTER (K). USING TEMPORARY REGISTER, PLACE RESULT IN SCRATCH REGISTER.
3. TEST FOR VALID INTERRUPTS.
4. INCREMENT INSTRUCTION ADDRESS REGISTER.
5. SHIFT 8-BIT OP CODE INTO LINK FOR TABLE LOOK-UP.
6. LOAD THE CONTENTS OF THE TABLE AT $E00_{16}$, INDEXED BY THE CONTENTS OF THE LINK, INTO THE LINK.
7. UNCONDITIONALLY JUMP TO $F00_{16}$ INDEXED BY THE CONTENTS OF THE LINK.

FIGURE 4-1. SAMPLE FLOWCHART, READ NEXT INSTRUCTION (Sheet 1 of 2)

1. Copy the Instruction Address register, I (500), into the Memory Address register, M. Initiate a Read from location 500 in core storage.

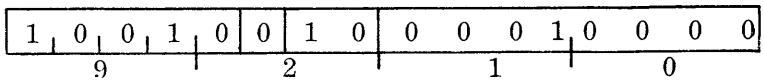
2. During the time required for memory to react, interrupts may be tested without time penalty. In this case, assume that the priority mask in the K-register when logically AND'ed with the raw interrupts in the T-register produce a zero, which is stored in the S-register for subsequent testing.

3. The S-register is tested for zero; if S is zero, any interrupts which may be in T are of a lower priority than the one being serviced and are, therefore, deferred.

4. The I-register is also incremented without time penalty:

   I (500) +1 → I (501).

5. When the Memory Data register, D, becomes available it contains the instruction. In this case, a short format is chosen and is as follows:

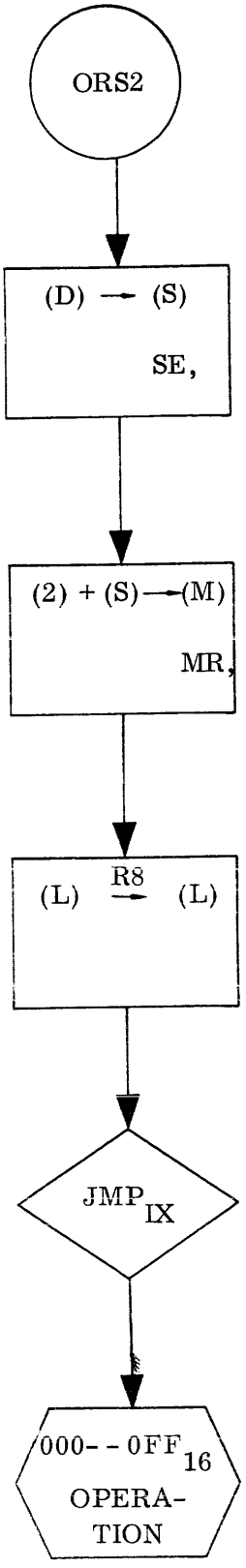


   $D = 9210_{16}$. D is shifted right eight places and stored in L. $L = 92_{16}$ at end of instruction.

6. A Load instruction with the address field set to $E00_{16}$ is used to read the contents of the table starting at E00. The Load instruction is indexed logically by the Link register giving an effective Read-Only Memory (ROM) address of $E92_{16}$. In this example, the contents of ROM location E92 are placed in the Link register. The Link register, L, now contains 4410_{16}. Load is a two-cycle instruction.

7. A Jump-to-F00 indexed by the Link causes program execution in the ROM to continue at location $F10_{16}$. (4410_{16} OR $F00_{16} = 4F10_{16}$. The ROM Address register is 12 bits; therefore, the effective address is $F10_{16}$.)

FIGURE 4-1. SAMPLE FLOWCHART,
READ NEXT INSTRUCTION (Sheet 2 of 2)



8. COPY INSTRUCTION (MEMORY DATA REGISTER) INTO SCRATCH WITH BIT 8 EXTENDED THROUGH BITS 7 - - 0.

9. ADD INDEX REGISTER 2 TO THE EXPANDED DISPLACEMENT TO FORM THE EFFECTIVE ADDRESS IN THE MEMORY ADDRESS REGISTER; INITIATE MEMORY READ.

10. SHIFT THE LINK RIGHT EIGHT PLACES TO FORM THE OPERATION ADDRESS.

11. UNCONDITIONALLY JUMP TO 000 INDEXED BY THE CONTENTS OF THE LINK.

FIGURE 4-2. SAMPLE FLOWCHART, OPERAND READ, SHORT FORMAT, RELATIVE TO INDEX REGISTER 2 (Sheet 1 of 2)

8. The instruction in the Memory Data register, D , is now copied into a Scratch register, S , with sign extension specified.

$D = 9210_{16}$ $S = 0010_{16}$. S now contains only the displacement.

9. Index Register 2 = 510_{16} is added to $S = 10_{16}$ giving 520_{16} as the effective address of the operand. This address is placed in the Memory Address register and a Read of the operand is initiated.

10. During the time required to fetch the operand, the exit to the operation subroutine may be prepared. The Link register, $L = 4410_{16}$, is shifted right eight places.

$L = 0044_{16}$, which is the address of the Subtract subroutine.

11. A Jump-to-LOC 000 indexed by the contents of the Link register results in an effective Jump-to-LOC 044 of ROM for execution of the Subtract when the operand becomes available in the Memory Data register, D.

FIGURE 4-2. SAMPLE FLOWCHART, OPERAND READ, SHORT FORMAT, RELATIVE TO INDEX REGISTER 2 (Sheet 2 of 2)

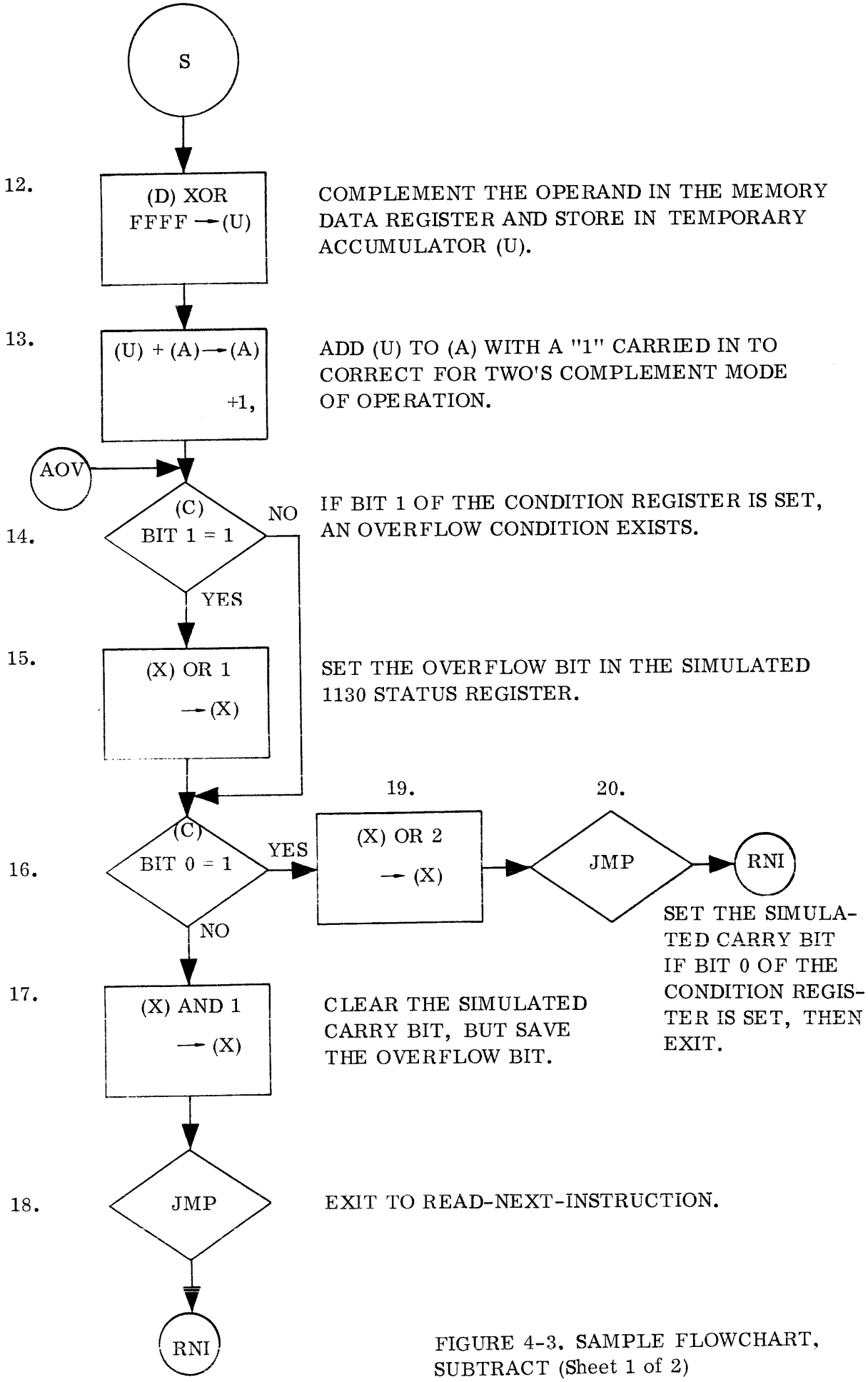


FIGURE 4-3. SAMPLE FLOWCHART, SUBTRACT (Sheet 1 of 2)

12. The operand in D (150_{16}) is complemented by an Exclusive OR with all 1 bits. The result is placed in the U-register:

$$150_{16} \text{ XOR } FFFF_{16} = FEAF_{16}.$$

13. The contents of the U-register ($FEAF_{16}$) are added to the contents of the accumulator (300_{16}) and a 1 bit is forced into the carry-in position for the two's complement mode of operation: $FEAF_{16} + 150_{16} + 1 = 1B0_{16}$ with a carry of 1.

	1111	1110	1010	1111	FEAF
	0000	0011	0000	0000	300
				1	1
1	0000	0001	1011	0000	

14. Bit 1 of the Condition/Counter register, C , contains the overflow status. This condition is tested. For this example, it is zero and the next instruction executed is 16.

15. If the overflow bit is set. a 1 bit is forced into the simulated 1130 status register.

16. Bit 0 of the C-register contains carry status. In this example, the carry is a 1 and control transfers to statement 19.

17. If the carry is zero, the carry bit (bit 14) and all the unused bits are cleared with an AND. The overflow bit (bit 15) is unchanged.

18. An Unconditional Jump to read the next instruction terminates the program.

19. The carry bit of the simulated Status register is forced to a 1 and the overflow bit (bit 15) is unchanged.

20. An Exit-to-RNI is performed.

FIGURE 4-3. SAMPLE FLOWCHART, SUBTRACT (Sheet 2 of 2)

APPENDIX A

POWERS OF TWO

APPENDIX A

POWERS OF TWO

2^n	n	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0.000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0.000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0.000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0.000 000 000 029 103 830 456 733 703 613 281 25
68 719 476 736	36	0.000 000 000 014 551 915 228 366 851 806 640 625
137 438 953 472	37	0.000 000 000 007 275 957 614 183 425 903 320 312 5
274 877 906 944	38	0.000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888	39	0.000 000 000 001 818 989 403 545 856 475 830 078 125
1 099 511 627 776	40	0.000 000 000 000 909 494 701 772 928 237 915 039 062 5
2 199 023 255 552	41	0.000 000 000 000 454 747 350 886 464 118 957 519 531 25
4 398 046 511 104	42	0.000 000 000 000 227 373 675 443 232 059 478 759 765 625
8 796 093 022 208	43	0.000 000 000 000 113 686 837 721 616 029 739 379 882 812 5
17 592 186 044 416	44	0.000 000 000 000 056 843 418 860 808 014 869 689 941 406 25
35 184 372 088 832	45	0.000 000 000 000 028 421 709 430 404 007 434 844 970 703 125
70 368 744 177 664	46	0.000 000 000 000 014 210 854 715 202 003 717 422 485 351 562 5
140 737 488 355 328	47	0.000 000 000 000 007 105 427 357 601 001 858 711 242 675 781 25
281 474 976 710 656	48	0.000 000 000 000 003 552 713 678 800 500 929 355 621 337 890 625
562 949 953 421 312	49	0.000 000 000 000 001 776 356 839 400 250 464 677 810 668 945 312 5
1 125 899 906 842 624	50	0.000 000 000 000 000 888 178 419 700 125 232 338 905 334 472 656 25
2 251 799 813 685 248	51	0.000 000 000 000 000 444 089 209 850 062 616 169 452 667 236 328 125
4 503 599 627 370 496	52	0.000 000 000 000 000 222 044 604 925 031 308 084 726 333 618 164 062 5
9 007 199 254 740 992	53	0.000 000 000 000 000 111 022 302 462 515 654 042 363 166 809 082 031 25
18 014 398 509 481 984	54	0.000 000 000 000 000 055 511 151 231 257 827 021 181 583 404 541 015 625
36 028 797 018 963 968	55	0.000 000 000 000 000 027 755 575 615 628 913 510 590 791 702 270 507 812 5
72 057 594 037 927 936	56	0.000 000 000 000 000 013 877 787 807 814 456 755 295 395 851 135 253 906 25
144 115 188 075 855 872	57	0.000 000 000 000 000 006 938 893 903 907 228 377 647 697 925 567 626 953 125
288 230 376 151 711 744	58	0.000 000 000 000 000 003 469 446 951 953 614 188 823 848 962 783 813 476 562 5
576 460 752 303 423 488	59	0.000 000 000 000 000 001 734 723 475 976 807 094 411 924 481 391 906 738 281 25
1 152 921 504 606 846 976	60	0.000 000 000 000 000 000 867 361 737 988 403 547 205 962 240 695 953 369 140 625
2 305 843 009 213 693 952	61	0.000 000 000 000 000 000 433 680 868 994 201 773 602 981 120 347 976 684 570 312 5
4 611 686 018 427 387 904	62	0.000 000 000 000 000 000 216 840 434 497 100 886 801 490 560 173 988 342 285 156 25

APPENDIX B

ASCII, TELETYPE, AND HOLLERITH CODES

APPENDIX B

ASCII, TELETYPE, AND HOLLERITH CODES

Hex. Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations	Hollerith Punch Code
80	Null/Idle	NULL	---	CTRL @	---
81	Start of Message	SOM	---	CTRL A	---
82	End of Address	EOA	---	CTRL B	---
83	End of Message	EOM	---	CTRL C	---
84	End of Transmission	EOT	---	CTRL D	---
85	Who Are You	WRU	---	CTRL E	---
86	Are You	RU	---	CTRL F	---
87	Audible Signal	BELL	---	CTRL G	---
88	Format Effector	FE	---	CTRL H	---
89	Horizontal Tabulation	H TAB	---	CTRL I	---
8A	Line Feed	LF	---	CTRL J	---
8B	Vertical Tabulation	V TAB	---	CTRL K	---
8C	Form Feed	FF	---	CTRL L	---
8D	Carriage Return	CR	---	CTRL M	---
8E	Shift Out	SO	---	CTRL N	---
8F	Shift In	SI	---	CTRL O	---
90	Device Control Reversed for Data Line Escape	DC0	---	CTRL P	---
91	Device Control ON	DC1	---	CTRL Q	---
92	Device Control (TAPE)	DC2	---	CTRL R	---
93	Device Control OFF	DC3	---	CTRL S	---
94	Device Control	DC4	---	CTRL T	---
95	Error	ERR	---	CTRL U	---
96	Synchronous Idle	SYNC	---	CTRL V	---
97	Logical End of Media	LEM	---	CTRL W	---
98	Separator, Information	S0	---	CTRL X	---
99	Separator, Data Delimiters	S1	---	CTRL Y	---
9A	Separator, Words	S2	---	CTRL Z	---
9B	Separator, Groups	S3	---	SHIFT CTRL K	---
9C	Separator, Records	S4	---	SHIFT CTRL L	---
9D	Separator, Files	S5	---	SHIFT CTRL M	---
9E	Separator, Misc.	S6	---	SHIFT CTRL N	---
9F	Separator, Misc.	S7	---	SHIFT CTRL O	---
A0	Space	SP	Space	Space Bar	**

** Space - No character is printed.

Hex. Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations	Hollerith Punch Code
A1	Exclamation Point	!	!	SHIFT !	***
A2	Quotation Marks	"	"	SHIFT "	12-8-7
A3	Number Sign	#	#	SHIFT #	11-8-6
A4	Dollar Sign	$	$	SHIFT $	11-8-3
A5	Percent Sign	%	%	SHIFT %	12-8-5
A6	Ampersand	&	&	SHIFT &	8-6
A7	Apostrophe	'	'	SHIFT '	8-7
A8	Parenthesis, Beginning	(	(	SHIFT (	0-8-4
A9	Parenthesis, Ending	)	)	SHIFT)	12-8-4
AA	Asterisk	*	*	SHIFT *	11-8-4
AB	Plus Sign	+	+	SHIFT +	12
AC	Comma	,	,	,	0-8-3
AD	Hyphen	-	-	-	11
AE	Period	.	.	.	12-8-3
AF	Virgule	/	/	/	0-1
B0	Numeral 0	0	0	0	0
B1	Numeral 1	1	1	1	1
B2	Numeral 2	2	2	2	2
B3	Numeral 3	3	3	3	3
B4	Numeral 4	4	4	4	4
B5	Numeral 5	5	5	5	5
B6	Numeral 6	6	6	6	6
B7	Numeral 7	7	7	7	7
B8	Numeral 8	8	8	8	8
B9	Numeral 9	9	9	9	9
BA	Colon	:	:	:	0-8-6
BB	Semicolon	;	;	;	8-4
BC	Less Than	<	<	SHIFT <	11-8-5
BD	Equals	=	=	SHIFT =	8-3
BE	Greater Than	>	>	SHIFT >	0-8-5
BF	Interrogation Point	?	?	SHIFT ?	12-8-6
C0	At	@	@	SHIFT @	—
C1	Letter A	A	A	A	12-1

***No Hollerith Punch or Card Code available for this character.

Hex. Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations	Hollerith Punch Code
C2	Letter B	B	B	B	12-2
C3	Letter C	C	C	C	12-3
C4	Letter D	D	D	D	12-4
C5	Letter E	E	E	E	12-5
C6	Letter F	F	F	F	12-6
C7	Letter G	G	G	G	12-7
C8	Letter H	H	H	H	12-8
C9	Letter I	I	I	I	12-9
CA	Letter J	J	J	J	11-1
CB	Letter K	K	K	K	11-2
CC	Letter L	L	L	L	11-3
CD	Letter M	M	M	M	11-4
CE	Letter N	N	N	N	11-5
CF	Letter O	O	O	O	11-6
D0	Letter P	P	P	P	11-7
D1	Letter Q	Q	Q	Q	11-8
D2	Letter R	R	R	R	11-9
D3	Letter S	S	S	S	0-2
D4	Letter T	T	T	T	0-3
D5	Letter U	U	U	U	0-4
D6	Letter V	V	V	V	0-5
D7	Letter W	W	W	W	0-6
D8	Letter X	X	X	X	0-7
D9	Letter Y	Y	Y	Y	0-8
DA	Letter Z	Z	Z	Z	0-9
DB	Bracket, Left	[	[	SHIFT K	***
DC	Reverse Virgule	\	\	SHIFT L	***
DD	Bracket, Right	]	]	SHIFT M	***
DE	Up Arrow (exponentation)	↑	↑	SHIFT	---
DF	Left Arrow	←	←	SHIFT	---
E1 through FC are not available					
FD	Unassigned Control	1	---	ALT MODE	---
FE	Not Available				
FF	Delete/Idle/Rub Out	DEL	---	RUB OUT	---

*** No Hollerith Punch or Card Code available for this character.

APPENDIX C

TABLE OF BINARY-TO-HEXADECIMAL CONVERSION

APPENDIX C

TABLE OF BINARY-TO-HEXADECIMAL CONVERSION

Binary	Hexdecimal
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

APPENDIX D

HEXADECIMAL-TO-DECIMAL CONVERSION TABLE

APPENDIX D

HEXADECIMAL-TO-DECIMAL CONVERSION TABLE

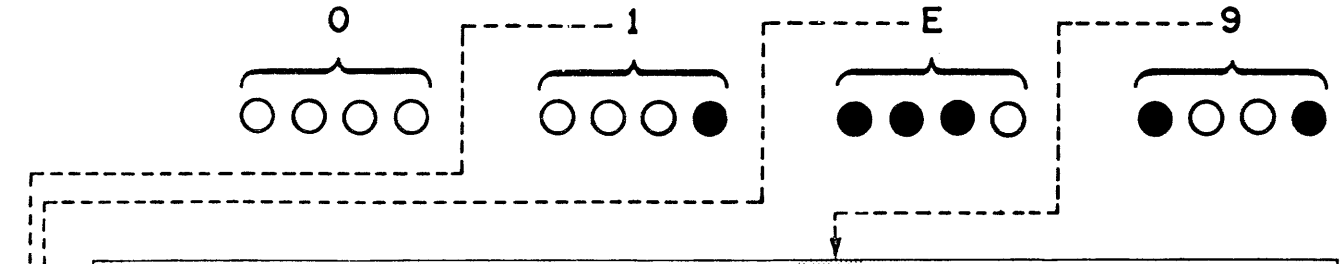
The table in this appendix provides for direct conversion of decimal and hexadecimal numbers in these ranges:

Hexadecimal	Decimal
000 to FFF	0000 to 4095

For numbers outside the range of the table, add the following values to the table figures:

Hexadecimal	Decimal
1000	4096
2000	8192
3000	12288

Hexadecimal	Decimal
4000	16384
5000	20484
6000	24576
7000	28672
8000	32768
9000	36864
A000	40960
B000	45056
C000	49152
D000	53248
E000	57344
F000	61440



	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000	0000	0001	0002	0003	0004	0005	0006	0007	0008	0009	0010	0011	0012	0013	0014	0015
010	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0030	0031
020	0032	0033	0034	0035	0036	0037	0038	0039	0040	0041	0042	0043	0044	0045	0046	0047
030	0048	0049	0050	0051	0052	0053	0054	0055	0056	0057	0058	0059	0060	0061	0062	0063
040	0064	0065	0066	0067	0068	0069	0070	0071	0072	0073	0074	0075	0076	0077	0078	0079
050	0080	0081	0082	0083	0084	0085	0086	0087	0088	0089	0090	0091	0092	0093	0094	0095
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7C0	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999
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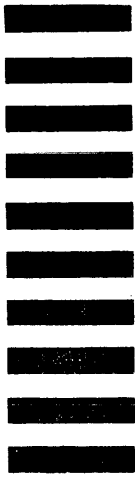

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