SECTION 3

INSTALLATION INSTRUCTIONS

3. INSTALLATION INSTRUCTIONS

3.1. Mounting Arrangements S214SB (See also Appendix J5.0)

The Supervisor 214 can be mounted in any standard 19-inch (483 mm) panel width cabinet/rack having 24 to 25 inches (610 to 635 mm) depth from front to rear mounting verticals. The front panel height is 10.5 inches (267 mm), i.e. 6 units of 1.75 inches.
This equipment has air filters which must be cleaned at suitably regular intervals (depending on the environment).
Note that the cooling air arrangements of the rack must allow for airflow from right to left viewed from the front.
Envelope dimensions and electrical connections for the unit are defined on installation drawing no. 07-03-14.

In order that the unit can be mounted in any standard rack irrespective of its vertical fixing positions in relation to other equipment, two sets of slide fix holes and two sets of lock plate fix holes are provided.

The selection of the appropriate sets of fix holes is defined on sheet 2 of the installation drawing.

3.2. Power Supply Connections

IMPORTANT

In common with other digital equipment, the power supplies in Supervisor 214 contain mains filters, which permit the chassis to rise to a potential equal to half the mains supply voltage if it is not earthed. IT IS THEREFORE ESSENTIAL, BOTH FOR THE SAFETY OF PERSONNEL AND THE EQUIPMENT THAT THE EARTH WIRE IS CONNECTED TO EARTH.

If the power supply module is mounted in the Supervisor 214 chassis proceed as follows:-

1. Attach a suitable plug to the end of the power cable and connect it to the mains supply.

2. Remove the bottom cover from the chassis and check that the four voltage selector switches are set for the correct mains voltage (i.e. 230V or 115V). The switches are fixed in position with a perspex retaining strip. The fan voltage selector switch is mounted on the Supervisor 214 adjacent to the low level dc busbars, the +5v and +12v selector switches are on the Gresham Lion power modules and the -5v selector switch is mounted between the Gresham Lion modules. Restore the bottom cover.

If the power supply module is externally mounted, proceed as follows:-

1. Remove the top cover from the power tray and check that the voltage selector switches are set for the correct mains voltage (i.e. 230V or 115V).

2. Remove the bottom cover of the Supervisor 214. Connect the mains plug from the power supply module to the fans socket, and the low voltage dc braided cables marked +5v, -5v, +12v to the corresponding busbars.

3. Connect the braided cable labelled 0V to the 0V stud adjacent to the busbars.

4. Attach a suitable plug to the end of the power cable and connect it to a mains supply outlet. Ensure a reliable earth connection with adequate current carrying capacity is made to the Supervisor 214 via the earth pin in the mains plug. Note that earth studs are provided on the power supply module and the power tray adjacent to the mains connection to allow alternative earth bonding if required.

3.3 Power Supply Checks

1. Remove the Supervisor 214 top cover. A maintenance switch is mounted on the inside of the front trim on the top right hand side, and controls the supply to the dc busbars. Move this switch to the OFF position.

2. Ensure the incoming power connections are made, and move the miniature circuit breaker at the rear of the power supply module to the ON position.

3. Check that the AC MAINS neon light on the Supervisor 214 front panel lights up.

4. Check that the fans are operating. When they sound as if they are at full speed, move the maintenance switch to the ON position.

5. Check that the +5V, -5V and +12V LEDs on the front panel are illuminated. It may also be noted that the RUN and ACTIVE LEDs flash momentarily.

Satisfactory completion of these checks indicates that the Supervisor 214 is correctly powered up and the low voltage dc supplies are present. Switch off the mains incoming supply, restore the maintenance switch to the ON position and proceed with the input and output connections.

3.4 Input Connections S214SB (See also Appendix J7.0)

Refer to the System configuration drawing in the overall System manual for details of cabling required to interface the Supervisor 214 with the host computer. One of three interface connections will be indicated:-

1. The Supervisor 214 does not include an internally mounted LSI11 micro-computer. In this case, a 40-way ribbon cable is required to connect from the Control PCB in the Supervisor 214 to the Interface PCB in the host computer or the externally mounted micro-computer. Ensure the polarity of the cable is correct by aligning the moulded arrow marks at both ends. Secure the ribbon cable in the clamps at the rear of the Supervisor 214 chassis.

2. The Supervisor 214 chassis includes an LSI11 microcomputer with serial interface. Check that the 40-way ribbon cable is correctly installed between the Interface PCB in the LSI11 backplane and the Control PCB in the system controller backplane. Connect the serial interface cable between the serial interface PCB in the LSI11 backplane and the Serial Interface in the host computer.

Secure the serial interface cable with a clamp at the rear of the Supervisor 214 chassis.

3. The Supervisor 214 chassis includes an LSI11 micro-computer with serial interface and DMA interface. In this case, carry out the procedures outlined in step 2. above, and install the cabling for the DMA interface in accordance with the instructions outlined in the manuals supplied with the DMA modules.

3.5 Output Connections S214SB (See Appendix J7.0)

Refer to the System configuration drawing in the overall system manual for details of the 75 ohm video signal connections between the Memory PCBs or Image Output PCBs and the display monitors.

Install the co-axial cables as indicated and secure them with the cable clamp at the rear of the Unit.

Ensure the maintenance switch is in the ON position and replace the Supervisor 214 top cover.

Reconnect the mains incoming supply and check that the fans are heard to be operating and the +5V, -5V and +12V LEDs on the front panel are illuminated.

The Supervisor 214 is now ready for testing in accordance with the diagnostic programs in the overall System manual.

SECTION 4

PROGRAMMING GUIDE (Group Ø Register)

N.B. This section is concerned with programming registers in Group Ø only. i.e. registers necessary in all Supervisor 214 systems.

For programming information regarding registers in Groups 1, 2 and 3 (optional facilities and image displays) see the appropriate appendix.

TABLES

4. PROGRAMMING GUIDE (Group Ø Registers)

4.1 Introduction

The program for running the Supervisor 214 is written for the computer which directly controls it, i.e. the host computer when there is no local intelligence or the LSI11 micro-computer.

Where an LSI11 micro-computer is provided complete with display software/firmware, reference should be made to the associated software manual supplied with the equipment.

Where a user is providing his own display program, this Section lays down guidelines for the programmer.

The Supervisor 214 display system is controlled by reference to a set of 16-bit registers. The manner in which these registers are accessed depends upon the particular computer, and reference should be made to the appropriate Appendix to this Manual. Apart from the method of accessing the registers, the programming is identical for all computers. It should be noted that the registers are generally write-only or read-only. This precludes the use of read/modify/restore instructions. Most of the registers do not contain data in byte format, and therefore byte operations should also be avoided.

4.2 System Registers

There are 64 possible register addresses which are divided into four groups of 16 as shown in Table 4.1.

Group 0 contains those registers and flags which are necessary for all display systems. Group 1 is for system options. Register addresses 16 - 19 are allocated to the registers on the Programmable Format PCB, when it is used, for computer control of the display parameters. The remaining register addresses in this group are available for use with cursor generators. Group 2 contains the register addresses for video output control required for image displays, and group 3 contains the register addresses for ASC11 display cards.

4.2.1 Data Register and Input/Output Cycle Counter

This is the register through which all data to or from the Memory PCBs passes.

Writing data to this register initiates a number of memory write cycles according to the setting of the input/output cycle counter. In each cycle, data is unpacked from the computer word and distributed to the Memory PCBs according to the data distribution mode selected.

Reading data from this register initiates the reverse process. A number of memory cycles are performed and the required data is assembled into the computer word.

The I/O cycle counter must be loaded with a number one less than the required number of cycles.

TABLE 4.1 SYSTEM REGISTERS

GROUP	ADDRESS	FUNCTION	PDP11/LSI11 ADDRESS
0	0	Data Register	170000
	1	Diagnostic Register	170002
	2	Command and Status Register	170004
	3	Input/output cycle counter	170006
	4	X access register/access row	170010
	5	Y access register/access column	170012
	6	Y offset register/scan row	170014
	7	Addressing control register/scan column & hardware vector fractional register	170016
	8	O/P Inh. flags, planes 0 - 15	170020
	9	Access flags, planes 0 - 15	170022
	10	Foreground flags, planes 0-15	170024
	11	Background flags, planes 0 - 15	170026
	12	Output flags, planes 16 - 31	170030
	13	Access flags, planes 16 - 31	170032
	14	Foreground flags, planes 16 - 31	170034
	15	Background flags, planes 16 - 31	170036
1	16 - 19	Programmable format registers	170040 - 170046
	20 - 31	3 cursors	170050 - 170076
2	32 - 33	Image output 0	170100 - 170102
	34 - 35	Image output 1	170104 - 170106
	36 - 37	Image output 2	170110 - 170112
	38 - 39	Image output 3	170114 - 170116
	40 - 41	Image Input 0	170120 - 170122
	42 - 43	Image input 1	170124 - 170126
	44 - 45	Image input 2	170130 - 170132
	46 - 47	Image input 3	170134 - 170136
3	48	H/W area fill, planes 0 - 15	170140
	49 - 50 - 51	Unused Mem flags, planes 0 - 15	170142 - 170146
	52	H/W area fill, planes 16 - 31	170150
	53 - 54 - 55	Unused Mem flags, planes 16 - 31	170152 - 170156
	56 - 57	ASCII Generator 3	170160 - 170162
	58 - 59	ASCII Generator 2	170164 - 170166
	60 - 61	ASCII Generator 1	170170 - 170172
	62 - 63	ASCII Generator 0	170174 - 170176

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Revised 11.6.82 - K.W.Travis

The number of input/output cycles is normally related to the data distribution mode in use as shown below:-

1 bit mode	1 to 16 cycles	Maximum = 16
6 bit mode	1 or 2 cycles	Maximum = 4
8 bit mode	1 or 2 cycles	See 5.2.4 "I/O Cycle Limitation"
12 bit mode	1 cycle	

The format of data in the register also depends upon the selected data distribution mode. In 1 bit mode, all 16 bits may be valid, and are transferred serially to all Memory PCBs. The number of bits to be transferred is set by the input/output cycle counter, and bit 0 (LSB) is transferred in the first cycle. In 6 bit and 8 bit modes, two bytes may be stored in the register, with bits 0 - 5 or 0 - 7 transferred in the first cycle and bits 8 - 13 or 8 - 15 in the second cycle. In 12 bit mode, bits 0 - 11 are transferred in every cycle.

If excess output cycles are performed in 6 bit or 8 bit modes, the two bytes in the computer word are used alternately until the input/output cycle count is exhausted. In 12 bit mode, the single intensity value is used repeatedly. This technique is useful when several adjacent pixels are required to be written with the same intensity, e.g. when performing an area erase.

Excess input cycles in 6 bit, 8 bit or 12 bit modes are of no value since only the data read in the last 1 or 2 cycles will be in the computer word. Excess cycles are not possible in 1 bit mode.

When the input/output cycle counter is set to 4 or less, the data transfer is acknowledged to the computer after the required input/output cycles have been completed. When the input/output cycle counter is set to 5 or more, the transfer is acknowledged before the first cycle is begun so that the computer is free to execute further instructions whilst the input/output cycles are proceeding. N.B. For a count of 4, load 3, etc.

A DATA READY flag is provided in the System command and status register which the computer may test to determine when the input/output cycles are complete. It need do this only if there is the possibility of the computer initiating a further transaction with the data register, or of modifying the X and Y access registers or the various control flags before the input/output cycles are complete.

The effect of this arrangement, when reading in 1 bit mode, is that the computer reads the data which resulted from the previous transaction. To read the current data a further transaction must be performed. In effect, therefore, the first read is a dummy and subsequent reads yield valid data.

Care must be taken when using DMA devices in 1 bit mode because they do not have the ability to wait for the DATA READY flag. The time required for the input/output cycles must be less than the DMA device word rate.

4.2.2 Command and Status Register

1. Bit 0. This is the erase enable signal and is a write only bit. It is set to binary 1 to initiate an automatic erase, and returns to binary 0 when the erasure is complete.

2. Bit 1. This is the 32 bit block write enable and is a write/read bit. When set to binary 1 it enables the 32 bit parallel write facility in the Memory PCBs.

3. Bit 2. This is the additive flag and is a write/read bit. When set to binary 1 it enables additive data writing to all the Memory PCBs.

4. Bits 3 and 4. These are write/read bits that specify the format of data transfer between the computer and the Memory PCBs as follows:-

Bit 4	Bit 3	Mode
0	0	1 bit
0	1	6 bit
1	0	8 bit
1	1	12 bit

5. Bit 5. This is the frame pulse and is a read only bit. It is set at binary 1 during odd field scanning in an interlaced system, and is of particular use when programming vertical scrolling.

6. Bit 6. This is the field interrupt enable and is a write/read bit. It enables an interrupt to occur at the end of every field, i.e. when bit 7 is set to a binary 1.

7. Bit 7. This is the field pulse and is a read only bit. It is set at binary 1 during the Scan cycle field blanking interval, and is at binary 0 at all other times. It is provided to enable the computer to control erasure, video switching and vertical scrolling and other operations which are preferred to be field synchronous.

8. Bit 8. This is the erase interrupt enable and is a read/write bit. It allows an interrupt to occur when bit 9, erase ready, returns to binary 1 on completion of an erasure.

9. Bit 9. This is the erase ready signal and is a read only bit. It is set to binary 0 when bit 0 (erase go) goes to binary 1, and returns to binary 1 on completion of the erasure.

10. Bit 10. This is the double buffer inhibit signal and is a read/write bit. It is set at binary 1 when double buffering is not required.

11. Bit 11. This is a read only bit which is set at binary 1 if the Programmable Format PCB is plugged in position in the system controller backplane. It indicates to the programmer whether the required picture may be programmed via the PCB. If the Programmable Format PCB is not present, the programmer must call up other test procedures to determine if the hard wired format PCB is compatible with the picture being called for.

12. Bit 15. This is the data ready flag and is a read only bit. When it is at binary 0 it indicates that a write or read sequence involving the data register is in progress.

Double Buffering and Inhibited Double Buffering

The auto-increment - auto-decrement feature of the X and Y registers may be operated in one of two ways. Double buffering is used with 1 bit mode for graphics generation and inhibited double buffering is used with 6, 8 and 12 bit modes for image reading and writing.

When double buffered, the X and Y addresses loaded by the programme, are stored in a buffer register. When a data register operation begins, the buffer contents are transferred automatically to counters. As the data I/O cycles are performed the counters increment or decrement according to how the control flags are set. During this time the programme may load new values to the buffer registers without disturbing the current operation. This allows computer operations to overlap hardware operations thus saving time.

In the case of writing graphics pixel arrays such as characters it is required after writing one row (or column) to return to the starting value of X (or Y) for the reset row (or column). With double buffering this happens automatically if the X or Y buffer is not reloaded.

With inhibited double buffering, when the X and Y registers are loaded by programme, the values are immediately transferred to the counters, and not at the start of a data register operation. Whilst a data register operation is in progress the X and Y counters increment or decrement in accordance with their control flag settings. Normally the I/O cycle count will be 1 or 2 and the counters will move accordingly. Further data register operations may now be programmed without reloading the X or Y registers and the counters will move on from where they had reached. Thus image rows or columns can be written or read as a series of data register operations without reference to the X and Y registers.

4.2.3 X and Y Access Registers

These registers provide the programmer with convenient Cartesian access to the picture elements. Hardware converts the X and Y values to a single physical address according to the equation:-

Y(HRES) + X

where (HRES) is the horizontal resolution with standard values of 256, 384, 512, 768 or 1024.

For Access cycles, both registers are write only. In the maintenance mode they may be read indirectly.

The X register has 12 bits which is more than the number required for the highest horizontal resolution. The excess bits allow several picture lines (up to 16 at 256 horizontal resolution) to be addressed via the X register. This permits DMA transfers which exceed 1 line to be programmed by setting X to auto increment. When this technique is used with an interlaced non-repeat field system, the lines accessed are consecutive in the same field. This is because the memory field partition is selected by the least significant Y bit which does not change as X increases through successive lines.

The maximum number of Y bits required for a given memory capacity is a function of the horizontal resolution. Two extremes are:-

4k RAMs	X = 10 bits (1024)	Y = 7 bits
16k RAMs	X = 8 bits (256)	Y = 11 bits

It is thus possible to program X and Y so that a physical address beyond the memory capacity is generated. In this case the excess bits at the most significant end are ignored and access thus 'wraps round' into the existing memory.

When multiple pictures are stored in memory, the programmer must calculate the correct Y address to access the desired picture.

For maintenance mode, the registers are used to verify the computation of the Access cycle row and column addresses. Maintenance mode is activated via the addressing control register and causes the normal selection circuits to be inhibited, allowing the computer to assume control. A diagnostic program loads the X and Y access registers with a range of values, and the resulting computation from the registers is checked for accuracy.

The size of the row and column fields depends upon the size of the memory RAM in use. Unused bits in the 16-bit registers are indeterminate and should be masked out by the program.

In this way the computer may verify that the X and Y access registers are generating the correct row, column and bit addresses according to the memory size and horizontal resolution in use. Dummy data transfer cycles can be performed with the various combinations of auto increment and decrement (via the addressing control register) to verify that the X and Y access registers are counting properly.

4.2.4 Y Offset Register/Scan Counter

The Y offset register is a 16-bit write only register which, during a Scan cycle, controls the physical address at which the scanning of the visible picture begins in each field. For maintenance mode, it is a write/read register for verifying the computation of the Scan row address.

The 16 bits are provided for future use with 64k RAMs. 14 bits are needed for 16k RAMs and 12 bits for 4k RAMs. With 16k and 4k RAMs, excess bits at the most significant end are ignored.

Five zeros are appended to the value in the register at the least significant end to form the actual physical address. Thus the start of picture read out can be specified on 32 pixel boundaries. This has a limited value in scrolling the picture horizontally because the picture 'wraps round'. The main purpose is to scroll a picture vertically or to select a particular picture from several that are stored simultaneously.

For repeat field systems, a single picture may be scrolled into unused memory areas. In this case the Y offset value is calculated according to the formula n(HRES/32) in which n represent the required number of lines of vertical scroll, and HRES is the horizontal resolution (256, 384, 512, 768 or 1024).

For an interlaced non-repeat field system, calculation of the Y offset value is more complicated. If the required vertical scroll is by an even number of lines, data for the even field is derived from the even field memory partition, but offset b y the required number of lines of vertical scroll. Data for the odd field is similarly derived from the odd field memory partition. The formula for the Y offset value is therefore (n/2) x (HRES/32).

If the required vertical scroll is by an odd number of lines, data for the even field is derived from the odd field memory partition, offset by the appropriate number of lines, and data for the odd field is similarly derived from the even field memory partition. For this requirement the computer sets an exhange memory partition flag in the addressing control register on the Address Computation PCB which alternates the automatic selection of memory partition during Scan cycles. The required Y offset value is different for the two fields. For an even field, the formula is (n - 1)/2 x (HRES/32); for an odd field it is (n + 1)/2 x (HRES/32). The field interrupt is used to allow the Y offset value to be changed regularly.

This register is also used during maintenance mode to verify the computation of the Scan cycle row and column addresses. The normal clocking of the Scan counter is inhibited, and the computer uses a diagnostic program to load the register and counter with a range of values. The computed addresses are then read from the Y offset register.

For non-repeat field systems, the most significant memory address bit is provided by the odd/even field waveform. The most significant bit of the scan counter is ignored. Interlaced repeat field systems have the same memory organisation as non-interlaced systems.

For maintenance mode, the Y offset value is transferred immediately to the Scan counter and does not wait for the next field pulse. Moreover, the ability of the Scan counter to increment may be tested by a 'maintenance mode only' feature which causes increment by 1 when the X access register is loaded .

4.2.5 Addressing Control Register

The addressing control register is a write only register which controls the auto incrementing or decrementing of the X and Y access registers and the memory partition exchange for non-repeat field scrolling. It also activates the maintenance mode for computer diagnosis of the Access and Scan address computation logic.

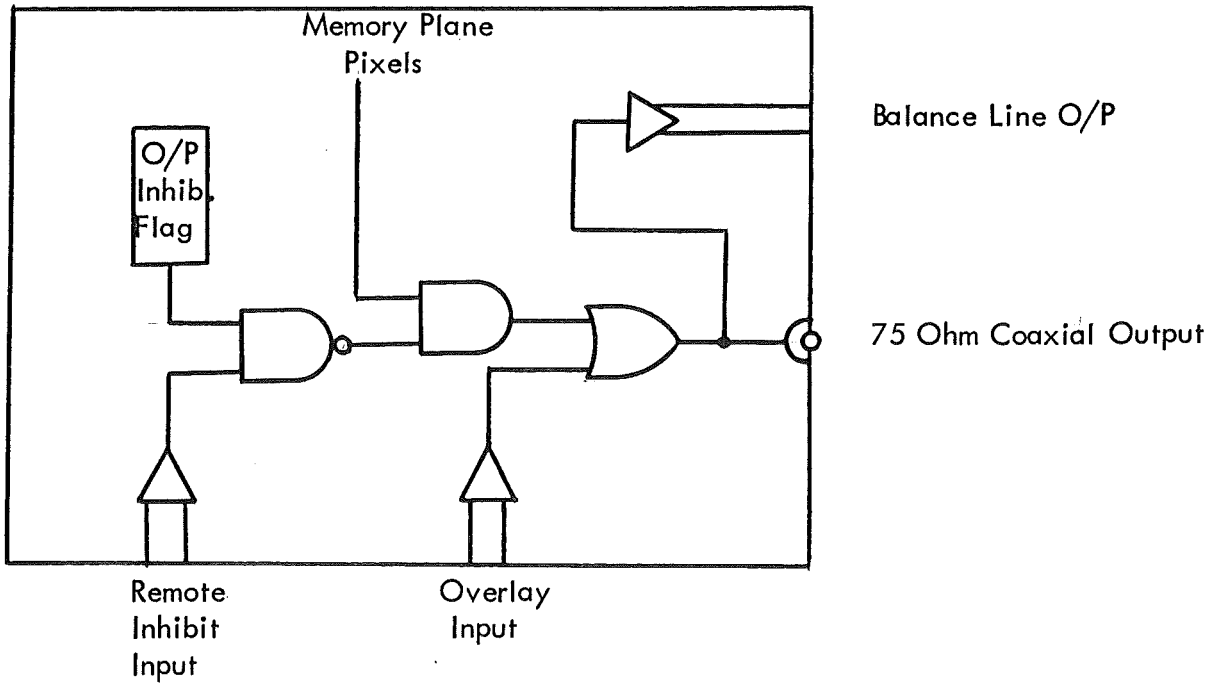
Automatic counting of the X and Y access registers on completion of input/output cycles is enabled when bits 2 and/or 0 are set to binary 1. The direction of counting is determined by bits 3 and 1. When they are set at binary 1 the count is incremented, and at binary 0 they are decremented.

Bit 4 is the exchange bit. When it is set at binary 1 it reverses the automatic alternation of the memory partitions when scrolling by an odd number of lines in an interlaced non-repeat field system. The purpose of this is described in sub-section 4.2.4.

The memory address generator logic is put into maintenance mode by setting bit 5 to binary 1.

4.2.6 Memory Plane Output Inhibit Flag

Memory Plane Output Logic Diagram



4.2.6 (cont.)

The output of the memory plane is dependant upon the combined effect of the Output Inhibit Flag and the Remote Inhibit input. Both the Output Inhibit Flag and the Remote Inhibit input must be asserted to cut off the memory plane pixels. The Overlay input is'OR'ed directly into the output circuit, and is not affected by the Output Inhibit Flag or the Remote Inhibit input. The table below sumarises the combinations of the Output Inhibit Flag and the Remote Inhibit Input.

Remote Inhibit Input		Output Inhibit Flag	Memory Plane Output
CP1 (RI-)	CP2 (RI+)		
-	+	0	Memory Plane Data
+	-	0	Memory Plane Data
-	+	1	Black
+	-	1	Memory Plane Data
Other memory plane balanced line output		1	Plane data is inhibited by other memory plane

4.2.7 Memory Plane Access Flags

When an Access cycle write sequence is performed, the data is written to all Memory PCBs that have their access flags set. For example, when writing a colour graphics picture in 1 bit mode, data will go to all planes, but only the red, green and blue planes of the desired monitor will have their access flags set and only these planes will be written.

When an Access cycle read sequence is performed, the data which makes up the computer word is the OR of the data from all memory planes which have their access flags set. In the example above, the programmer must decide whether to read the red component of the picture, the green, or the blue, or all ORed together, and set the access flags accordin gly. In other words, on output, data can usefully be 'exploded' into multiple pictures. An attempt to perform the reverse process on input may or may not give a useful result.

4.2.8 Memory Plane Background/Foreground Flags

These flags allow the programmer to specify the colour of the foreground and background of a graphics component, and to generate it in the red, green and blue Memory PCBs simultaneously. They may also be used for monochrome graphics and for image data.

The flags are used with the additive mode flag from the memory data register to control the bit loader logic on each memory PCB.

The additive flag is common to all Memory PCBs and determines whether the new data from the computer replaces or is added to the existing data in the memory. The foreground and background flags are individual to each memory plane and in combination with the additive flag determine the logic of loading. The results of all 8 flag combinations are shown below:

AD	BG	FG	Resulting Memory Data
0	0	0	Binary 0
0	0	1	True new data bit
0	1	0	Inverted new data bit
0	1	1	Binary 1
1	0	0	Existing store data bit
1	1	0	and inverted new data bit
1	0	1	Existing store data bit
1	1	1	or true new data bit

As shown, with the additive flag set at binary 0, data from the computer can be loaded in true or complement form by setting either the foreground or background flags. When neither flag is set, the data is ignored and binary 0 is loaded. Similarly, when both flags are set, binary 1 is loaded. The last two cases are useful for erasure and the generation of solid lines or areas.

With the additive flag set at binary 1, the resulting data is a function of both the existing stored data and the new data from the computer. The logical functions are chosen so that graphics components can be added correctly in monochrome or colour.

4.3 Loading Graphics Data

The programming and operation of monochrome graphics generation is self-evident and needs no illustration.

For loading colour graphics, the bit loader control flag combinations and the resulting data functions are arranged to make it easy for the programmer to specify the foreground and background colours of graphics components.

The necessary steps are:-

1. Set the access flags to binary 1 on all three Memory PCBs (red, green and blue).
2. Set the additive flag as required.
3. Set the foreground flag to binary 1 on those PCBs which contribute to the foreground colour.
4. Set the background flag to binary 1 on those PCBs which contribute to the background colour.
5. Load the graphics data.

In replacement mode (additive flag at binary 0) both the foreground and background colours will be generated correctly. In additive mode the foreground colour of the added components will always be correct. The background colour of the added component will also be correct except where modified by existing data in the memory.

For example, the flag settings for a green letter 'F' on a cyan background would be:

	BG	FG
Red Plane	0	0
Green Plane	1	1
Blue Plane	1	0

By reference to the table of flag combinations in sub-section 4.2.8, and assuming replacement mode for simplicity, it will be seen that the following plane data will result:

Red (0)	Green (1)	Blue (New data)
0000000	1111111	1111111
0000000	1111111	1000001
0000000	1111111	1011111
0000000	1111111	1011111
0000000	1111111	1000011
0000000	1111111	1011111
0000000	1111111	1011111
0000000	1111111	1011111
0000000	1111111	1111111

The red plane contributes to neither the background nor foreground and so is loaded with binary 0. The green plane contributes to both and so is loaded with binary 1 regardless of the data. The blue plane contributes only to the background and so is loaded with the complement of the data.

To illustrate the additive mode, assume the existing data is a white vertical strip:

Red	Green	Blue
0001000	0001000	0001000
etc.	etc.	etc.

The resulting data for the same example in additive mode will be the existing data or true new data in the red and green memory planes and the existing data and inverted new data in the blue memory plane:

Red	Green	Blue
0001000	0001000	0001000
0000000	0111110	0000000
0001000	0101000	0001000
0001000	0101000	0001000
0000000	0111100	0000000
0001000	0101000	0001000
0001000	0101000	0001000
0001000	0101000	0001000
0001000	0101000	0001000
0001000	0001000	0001000

Thus, the new component, F, will have the correct foreground colour which is green. The existing component (vertical strip) is also correct, white, except where crossed by the F. The background is black, i.e. the original background undisturbed.

4.4 Loading Image Data

The normal mode for loading image data is 001, i.e. to set AD to binary 0, BG to binary 0 and FG to binary 1. This causes the data to be loaded in true form. Mode 010 is useful when the image data is supplied in negative form and needs to be complemented.

Image margins where black or solid white is required can be generated by modes 000 011.

In certain specialised applications, the logical functions provided when the additive flag is set are of use.

4.5 32 Bit Parallel Writing

Normally on ly one pixel per plane is written for each write instruction, but a horizontal 32 bit pattern will be written for each write instruction, if BIT 1 of the command and status register (32 bit enable) is set. This facilitates the fast generation of large solid areas. Figure 5.9 shows the range of 32 bit pixel patterns that are available. When the 32 bit enable bit is set, the five least significant bits of the X address select the pixel pattern and the remainder of these bits selects the start address for the 32 bit word.

4.6 Hardware Area Fill Flag

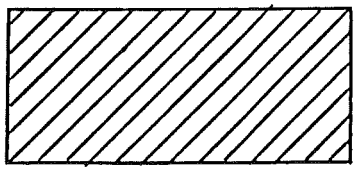
This facility fills the space on the monitor screen between pixels previously written into memory, as they are scanned out of the memory plane. The first pixel or contiguous group of pixels in any line on the monitor screen turns area fill on, and subsequent ones, alternately turn it off and on again. When the Area Fill Flag is set for a particular memory plane, it applies to the whole plane and cannot be used selectively within the plane. Where this facility is used there must always be an even number of pixels or groups of contiguous pixels in every line on the monitor screen, or the line will appear filled after the last pixel.

EXAMPLES

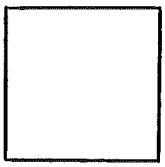
Shape in Memory

Shape on Screen

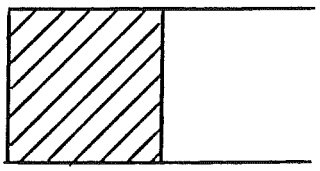
a. Filled Rectangle



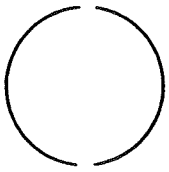
b. Error



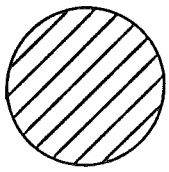
Single group of contiguous pixels in top and bottom lines cause 'break out' on the screen.



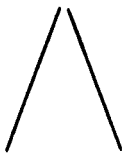
c. Filled Circle



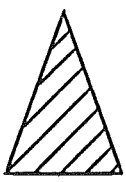
Note : Pixel space necessary top and bottom.



d. Filled Triangle



Note : Pixel space necessary in top line.



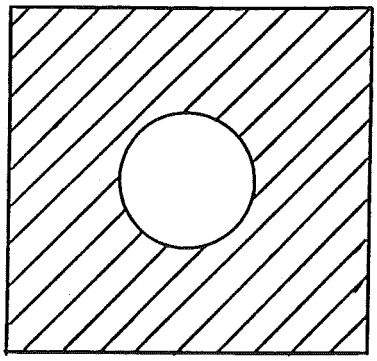
Although the hardware area fill facility may seem to have limitations and require attention to detail, it does provide a very fast means of writing large areas.

Example :- Artifical Horizon.

Display Required on Screen

Shape Written into Plane No. 1

Mask Written into Plane No. 2



The artificial horizon display is required to appear to rapidly rotate, forwards and backwards.

Without a hardware area fill facility, erasing and rewriting the filled semi-circle to simulate rotation, would be too slow. However, with a mask permanently written into plane No. 2, to define areas of plane no. 1 to be hidden from view, and the hardware area fill flag set for plane no. 1, only three vectors in plane no. 1 have to be erased and rewritten to simulate rotation of the filled semi-circle.

FIGURES

SECTION 5

CIRCUIT DESCRIPTIONS

TABLES

5. CIRCUIT DESCRIPTIONS

5.1 LSI11/S214 Interface

The LSI11 micro-computer and associated memories, interfaces, etc. are described in the standard publications issued by the Digital Equipment Corporation.

The LSI11/S214 Interface PCB is mounted in the LSI11 micro-computer and connects to the Supervisor 214 Control PCB via a ribbon cable. The circuit arrangements are shown on Drg. 02-504. The computer signals and connections are shown on Table 5.1

The LSI11 Q-bus signals are input via bus transceivers (L25, L27, L29, L30, L31, L32) with open collector drivers. The interrupt acknowledge (BIAK) and direct memory access grant (BDMG) signals are received from higher priority devices on the input pins (BIAKIL, BDMGI) and retransmitted via the output pins (BIAKOL, BDMGO) to lower priority devices along the Q-bus.

The address, data and control information is output to the Control PCB via transceivers L10, L11, L12, L13, L14, L15, L16. The signals are terminated in resistor networks L7, L8 to ensure a matched transmission line in the Supervisor 214.

5.1.1 Data Transfer Cycle

The initialise signal, BINITL, is generated at power up and is used to reset devices throughout Supervisor 214. It is applied to the Interface Adaptor PCB circuits via L27 pin 12, and output to the Supervisor 214 system via L10 pin 15 as the INIT- signal. A data transfer cycle cannot be initiated unless signal BSYNCL is negated indicating the previous bus transaction is completed.

The Supervisor 214 is controlled by reference to a set of 16 bit registers which appear in the input/outpu page of the LSI11 address space.

The page address for the 64 registers is set by the Links (RA7 - RA12) on L2 which provide the A inputs to comparators L4, L9. With the link open, the input is set high, closed it is set low. The B inputs are derived from address bits BDAL7L - BDAL12L. Thus the Supervisor 214 will not respond to an address unless signal BBS7L is set, indicating that the address is in the upper 4k bank (28 - 32k range), and one of the 64 register addresses is detected.

The data register, as well as appearing at a single address in the LSI11 input/output page, also appears as a block of addresses. The start of this block may be set anywhere in the LSI11 address space on 512 word boundaries, and may be adjusted in steps of 512 words up to 4096 words.

The required word block (page size) and start address are set up by links DA10 - DA15 and DR10 - DR12 on L1 as shown on Table 52. Switches DA10 - DA15 provide the B inputs to comparators L6, L3, and set the appropriate inputs high if they are open, low if they are closed. The A inputs are derived from data highway bits BDAL10L - BDAL15L, the most significant bits of which are linked in from the data lines (switches DR10 - DR12 closed) or tied to +5V (1).

5.1.2 Write Sequence

The write sequence is an output operation in which the LSI11 writes data in bit format into the registers or memory planes of the Supervisor 214.

Address information indicating the required operating mode, group or register address is placed on the data/address lines, and signals BBS7L is set. Comparators L4, L9 identify the register page address and set register page flip-flop L19 pin 2 high. When signal BSYNCL is set, it clocks the register page flip-flop and enables the transceivers L11, L12 . The BSYNCL signal clocks the group address bits (BDAL1L - BDAL12L) through L20 and into transceivers L11, L12 to generate signals A0 - A5 to the Control PCB.

The LSI11 then negates signal BBS7L, and replaces the address information with data. Upon recognition of the data register word block and starting address, data page flip-flop L19 pin 12 is set high so that when signal BSYNCL is set L19 pin 8 goes low. This is gated through to enable the transceivers L13, L14, L15 and L16.

The LSI11 sets data output signal BDOUTL to indicate data is available on the highway. This signal is gated through to L10 pin 2 to generate the Write- signal to the Control PCB.

The Supervisor 214 acknowledges receipt of the data with a REPLY- signal which is returned via L11 pin 3 and L25 pin 1 as the BRPLYL signal. Failure to receive a BRPLYL signal within 10us of setting the BDOUTL signal will be regarded by the LSI11 as an error condition. Upon receipt of the BRPLYL signal, the LSI11 cancels the BDOUTL signal and removes the data information. It then terminates the cycle by negating the BSYNCL signal.

During a byte transfer, BDAL0L selects high or low byte during the address sequence of the transfer cycles. If BDAL0L is asserted, the high byte (BDAL8 - BDAL15) is selected during the data sequence; otherwise the low byte (BDAL0 - BDAL7) is selected.

5.1.3 Read Sequence

The read sequence is an input operation in which the LSI11 reads data from the registers or memory planes of the Supervisor 214.

The read sequence is , in effect, the reverse of the write sequence. The address information is placed on lines BDAL0L - BDAL15L, and signals BBS7L and BSYNCL are set so that signals A0 - A5 are transmitted to the Supervisor 214. The address in formation is decoded by the Control PCB and the BBS7L signal is negated. The BDINL signal is now set to indicate the LSI11 is ready to accept data, and this is gated through to generate the READ- signal to the Control PCB.

Upon receipt of the READ- signal, the Supervisor 214 places the required data on the highway. Upon recognition of the data register word block and starting address, the data page flip-flop enables the BSYNCL and BDINL signals to enable the transceivers L29, L30, L31 and L32.

The Supervisor 214 also activates the REPLY- signal via L11 pin 5 which generates the BRPLYL signal to the LSI11.

THE LSI11 acknowledges receipt of the data by terminating the BDINL signal. The Supervisor 214 removes the data from the highway and negates the REPLY- signal. The cycle is terminated by the cancellation of the BSYNCL signal.

5.1.4 Interrupt Sequence

The Supervisor 214 requests an interrupt sequence by setting signal INT- from the Control PCB. This clocks L17 pin 3 to set L17 pin 5 high and causes the interrupt request signal, BIRQL, to be transmitted to the LSI11 via L27 pin 4.

Upon receipt of an interrupt request signal, the LSI11 sets acknowledge signal BIAKIL. This is gated through L21 to generate the reply signal, BRPLYLL, to the LSI11, and is also applied to L24, L23. This enables the interrupt vector address onto the relevant lines on the highway (BDAL8L - BDAL2L) for transmission to both the Control PCB and the LSI11.

The LSI11 responds to the reply signal with a BDINL signal, and the sequence proceeds as for a read sequence.

Note that the LSI11 responds to an interrupt request from any peripheral device by asserting the BIAKIL signal. If the request did not originate from the Supervisor 214, the signal is gated through L26 pin 11 and output as the BIAKOL signal.

TABLE 5.1 LSI11 Signal Connections

PIN	MNEMONIC	DESCRIPTION
AE2	BDOUTL	Data output signal
AF2	BRPLYL	Reply signal
AH2	BDINL	Data input request
AJ2	BSYNCL	Synchronise signal
AL2	BIRQL	Interrupt request
AM2	BIAKIL	Interrupt acknowledge input
AN2	BIAKOL	Interrupt acknowledge output
AP2	BBS7L	Bank 7 select signal
AR2	BDMGI	DMA grant input signal
AS2	BDMGO	DMA grant output signal
AT2	BINITL	Initialise signal
AU2	BDAL0L	
AV2	BDAL1L	
BE2	BDAL2L	
BF2	BDAL3L	
BH2	BDAL4L	
BJ2	BDAL5L	
BK2	BDAL6L	
BL2	BDAL7L	Data/address lines
BM2	BDAL8L	
BN2	BDAL9L	
BP2	BDAL10L	
BR2	BDAL11L	
BS2	BDAL12L	
BT2	BDAL13L	
BU2	BDAL14L	
BV2	BDAL15L	

TABLE 5.2 DATA REGISTER

DATA PAGE	DA12	DR12	DA11	DR11	DA10	DR10	SET START ADDRESS SW
4096 words	1	1	1	1	1	1	DA15 - DA1
2048 words		0	1	1	1	1	DA15 - DA1
1024 words		0		0	1	1	DA15 - DA1
512 words		0		0		0	DA15 - DA1
0 words	0	1	0	1	0	1	Data page disabled

1 = link out 0 = link in

5.2 Control Board

The circuit arrangements for the Control PCB are shown on Drg. 02-500.

The Control PCB is situated in position no. 1 of the control backplane. Connections from the Interface Adaptor PCB are made via a ribbon cable and 40-pin connector J1. Connections with other PCBs in the control backplane are made via edge connector sockets (EC).

The initialisation signal, INIT-, is input from the computer at power up or when a program is reloaded, and is used to clear and reset relevant circuit components. Circuitry on the control board generates an internal 'INIT'-signal when the S214 is powered up.

5.2.1 System Register Addresses

When the computer accesses a Supervisor 214 system register, it sets the register address on the highway, and then activates the WRITE- or READ- signal on connector J1 pin 7 or 9 to indicate whether it wishes to write information into, or read from, the addressed register. Highway bits H1 - H6 are clocked through to the Control PCB as signals A0-A5. They are gated through to decoders 13A to select the appropriate register.

1. Memory Flags : These signals are set to indicate whether the computer wishes to access Memory PCBs 0 - 15 or 16 - 31. Decoder 13A pin 6 or 7 is set low, gated with the WRITE- or READ- signal and output as signal M.FLAG1+ or M.FLAG2+ on EC pin BT2 or BU1. For a read sequence, the relevant signal is also gated through to reset the watchdog timer circuit.

2. Addressing control register : This signal is generated on 13A pin 5 when the computer wishes to access the a register on the Address Computation PCB. It is gated with the WRITE- or READ- signal to set the AC.READ+ or AC.WRITE+ signal on EC pin AA1 or AB1. A read sequence is initiated for maintenance mode only.

3. Input/output cycle counter : This signal is set on 13A pin 9 and allows the computer to set the number of input/output cycles required when accessing the memory data register. It is gated with the WRITE- signal to generate the I/O CTR WRITE+ signal. The operation of the input/output cycle counter is described in sub-section 5.2.3.

4. Command and status register : Decoder 13A pin 10 is set low when the computer wishes to access the command and status register to set up the required operating mode. It is gated with the WRITE- or READ- signal to generate either the CSR WRITE+ or CSR READ- signal.

5. Data register : Decoder 13A pin 12 is set low if the computer wishes to access the memory data register (which has address 0 in group 0). It is gated with the WRITE- or READ- signal to generate the WRITE DATA- or READ DATA- signal as required. It is also used to set up the reply circuit. Note that if the computer is not accessing this register but another in group 0, 15A pin 11 is set high. This is gated with either the READ+ or WRITE+ signal as appropriate and sets 14D pin 1 or 2 low to establish the REPLY- signal on connector J1 pin 36.

5.2.2 Command and Status Register

The command and status register sets up the required mode of operation for a write or read sequence. The register is connected to the address/data highway lines by transceivers 1B, 2B, 3B. The highway bits associated with the command and status register are:-

15	Data ready
11	Programmable Format PCB present
10	Double Buffer Inhibit
9	Erase ready
8	Erase interrupt enable
7	Field status
6	Field interrupt enable
5	Frame status
4, 3	Data mode
2	Additive enable
1	32 bit enable
0	Erase enable.

For a write sequence, the information is clocked from relevant circuits by the CSR WRITE+ signal from 16D pin 10. For a read sequence, the CSR READ- signal from 15D pin 8 inhibits the disable pins on the transceivers to allow information to be placed on the highway lines.

1. The DATA READY bit indicates that a write or read sequence involving the data register is in progress, and is generated from R-S latch 12B pin 9. It is held low during read or write sequences, and is set high when 6E pin 6 goes high at the completion of the input/output cycle count, and the last END CYCLE is detected.

2. Bit 11 is set high when the Programmable Format PCB is plugged into the system controller backplane. If a standard hard-wired Format PCB is used, bit 11 is set low. This feature indicates whether the picture may be changed by program.

3. When the computer wishes to write into the addressing control register or the X and Y access registers on the Address Computation PCB, the data is input from the highway into buffers. Signal XYTFR- on EC pin AD1 determines when the data is clocked through to the appropriate register.

   To inhibit this double buffering, bit 10 is set low. At the next CSR WRITE+ pulse, 10B pins 8 and 9 are clocked low and high respectively. This holds 14A pin 12 high and puts signal XYTFR- under the control of the addressing control AC WRITE+ signal on EC pin AB1.

   When bit 10 is set high, the XYTFR- signal goes low when 11E pin 6 pulses high. This pulse is also inverted and input to 12B pin 10 to hold the DATA READY signal low until the end of the cycle.

4. The erase and interrupt sequences are described in sub-sections 5.2.8 and 5.2.9 respectively.

5. The field status bit (7) is controlled from the field unblank signal, FUNBNK+, input on EC pin BS1 from the Sync and Timing PCB. This input is high during the field blanking interval and is enabled through 2B by the CSR READ+ signal.

6. The frame status bit (5) is set by the ODDEVE- signal input on EC pin BS2 from the sync and Timing PCB. This signal is high during odd field scanning in an interlaced system and is enabled through 2B by the CSR READ+ signal.

7. When the computer wishes to access the memory data register for a write or read sequence, it sets bits 3, 4. These are write/read bits which specify the format of data transfer between the computer and the Memory PCBs. They are clocked through 7B by the CSR WRITE+ signal (from 16D pin 10), and are output to the Memory PCBs on EC pins BM1, BM2 as signals MODE0- and MODE1-. On the Control PCB, they are input to the mode decoder 9C to set up the required data mode as follows:

Bit 4	Bit 3	MODE
0	0	1 bit
0	1	6 bit
1	0	8 bit
1	1	12 bit

8. When the computer wishes to write additional information to all the Memory PCBs, it sets bit 2 in the command and status register. This is a write/read bit and is clocked from 1B pin 13 through to 7B pin 3 by the CSR WRITE+ signal. It is output to all Memory PCBs as the additive mode enable signal, ADD-, on EC pin BP1.

9. When it is required to write a solid block of picture data 32 pixels wide into the Memory PCBs, bit 1 in the command and status register is set. This is a write/read bit and is clocked from 1B pin 3 through to 7B pin 2 by the CSR WRITE+ signal. It is output to the Sync and Timing PCB on EC pin CA1 as the 32 bit enable signal, 32ENB+.

5.2.3 Input/Output Cycle Counter

When the computer wishes to access the memory data register for a read or write operation, it is necessary to first set the number of input/ output cycles required for the selected data mode as follows:-

MODE	CYCLES
1 bit	1 to 16
6 bit	1 or 2
8 bit	1 or 2
12 bit	1

The number of cycles is indicated by highway bits 0 - 3 which are input to 7E via transceiver C1. This number is one less than the number of cycles executed.

To address the input/output counter for graphics systems, signals A0 - A5 set decoder 13A pin 9 low. This is gated with the WRITE- signal to generate the I/O CTR WRITE+ signal at 16D pin 13. This signal clocks the count code through 7E to the A inputs of comparator 6E. The B inputs are derived from the input/output cycle counter 4E. This counter is cleared at power up by the INIT- signal, and at the start of each write or read sequence when 11E pin 6 pulses high. The Sync and Timing PCB acknowledges each read or write cycle by causing the END CYCLE- signal on EC pin BD1 to pulse low. When the counter has clocked the required number of cycles so that input A equals input B in comparator 6E, the output on 6E pin 6 is set high.

5.2.4 Data Register Read-Write Reply Logic

All read and write pulses must be acknowledged by sending a reply to the computer. Reading or writing the Data Register (address 0) is complicated by the fact that S214 is required to respond in different ways depending upon the radix of the I/O cycle counter. Also some PDP11 computers do a read-write for the last cycle of a MOV instuction, and the read would generate unwanted I/O cycles in S214 if it were not inhibited. The reply for group 0 registers (addresses 2 to 15) is generated on the Control Board but the reply for all registers with an address greater than 15 is generated on other boards.

The data register read-write reply logic comprises a complex arrangement of gates, monostables and flip-flops, to the left of centre on the diagram. The main input signals are read data, write data, CO- and high or low I/O cycle count. The main outputs are data write+, data ready, cycle request and reply.

Reading the Data Register

The data read pulse goes low at 15Db. This enables the data register transceivers 1c, 2c, 3c, 4c at pins 7 and 9 and enables the direction flip flop at 12Bc at 11E11.

Low I/O Cycle Count Read (See Fig. 5.1) (No. loaded < 4, actual count < 5)

If the I/O cycle count is low (14C9 high), the W/R monostable is triggered (16C13 pulses high) which sets the direction flip flop 12Bc and resets the Data Ready flip flop. 12Bc13 goes high, and drives DATA WRITE+ low which enables the data transceivers on the memory planes. 12Bc is reset after the last I/O cycle. The trailing edge of the pulse from 16Ca13 triggers the Cycle Request monostable 16Cb. The cycle request is processed on the Sync and Timing Board, which responds with XY Count and End Cycle pulses at EC pins BR1 and BD1 respectively. The End Cycle pulse generates another cycle request provided that 16A6 remains low, and XY CNT+ increments the I/O cycle counter 4E. Cycle requests are thus regenerated until the output of the I/O cycle comparator 6E6 goes high, which inhibits further cycle requests at 16A5 and enables gate 14C at pin 2. The next End Cycle pulse is the last and it sets the Reply flip-flop which outputs a Reply to the Computer via 11E12 and 14D8. The Reply flip-flop is reset by the following Read or Write pulse. The last end cycle pulse also sets the Data Ready flip-flop.

High I/O Cycle Count Read (> 4) (See Fig. 5.2) (No. loaded >3)

If the I/O cycle count is high the S214 will require several memory cycles to load the data register, which takes several micro-seconds. In this case reply is sent to the computer before the data register is loaded in order that computer time is not wasted. The W/R monostable is not triggered by the read data pulse because 9d9 is low but by the End Read flip-flop 10Ba which is triggered by the trailing edge of the Read Data pulse. 9d6 is high which gates the Read pulse to 9C5 to generate Reply. The cycle request - end cycle sequence etc., is the same as for low count read.

Writing to the Data Register

The Data Write pulse 7E11 triggers the W/R monostable 10cb via 8B6 and 9F6, and the W/R monostable clocks the Data Register via C122, F74, E126, and E103/E106. The W/R monostable also resets the Data Ready flip-flop and triggers the Cycle Request sequences as described above.

Low I/O Cycle Count Write (Fig. 5.3)

If the I/O cycle count is low , (< 5) the Reply to the computer is generated by the Reply flip-flop 10d as for Low Count Read.

The write cycle is similar to the read described above. The W/R monostable is triggered by data read via 14C8 but the direction flip flop is not set because 11E is inhibited at pin 11. Thus 12Bc13 remains low and DATA WRITE+ is high indicating a write sequence to the memory planes. The I/O cycle sequence proceeds as above.

High I/O Cycle Count Write (See Fig. 5.4)

If the I/O Cycle Count is high then several S214 memory cycles are required to unload the Data Register and so Reply to the computer is generated before the I/O sequence commences to avoid wasting computer time. Write Data is gated with High Count at 9D6 and fed to the Reply Gate 9C5.

CO- Control Signal

The PDP11 04/05/10/15/20 computers do a read/write for the last cycle of a MOV instruction, whereas others do only a write cycle. Those that do, also assert the CO- signal during the read time to indicate that it is part of a read-write cycle. When the computer is writing to the data register, a preceding read would generate unwanted I/O cycles, so CO- is used to inhibit the read in this case and only the write pulse is effective. However, a Reply must be sent to the computer in response to the Read and to provide this, Read Data is gated with CO- at 7b1 and fed to the Reply gate via 12F2.

I/O Cycle Limitation

When reply is made before the I/O cycle sequence begins, the S214 bus must be free for computer access to registers other than the Data Register during the I/O cycle sequence. When operating in 6, 8 or 12 bit mode, the Data Register uses the bus, consequently, it is not permissible to use these modes with the immediate reply. i.e. with a high I/O cycle count. The signal at 9F3 is high if the I/O cycle is greater than 4 and any mode other than 1 Bit mode is selected. This condition is invalid, the W/R monostable is inhibited, and no I/O cycles are made.

5.2.5 One Bit Data Distribution Mode

This mode is provided for graphics generation. As all sixteen bits are valid with bit 0 transferred in the first input/output cycle, this mode can require up to 16 cycles.

For a data write sequence, the data register is input to the data serialisers, 1E, 2E. At the end of the Q- pulse on 16C pin 13, 16C pin 5 pulses high to set the CYCLE REQ- pulse to the Sync and Timing PCB via EC pin B1E. The first bit from the data serialiser is gated through to the one bit highway (EC pin BN2) by the DAT WRITE- signal from 12B pin 13. The bit is taken to the Memory PCBs and written into those which have their access flags set by the M.FLAG1 or M.FLAG2 signal. The Sync and Timing PCB returns an XY CNT+ signal via EC pin BR1 which clocks counter 4E to the next data bit position. The END CYCLE- signal generates the CYCLE REQ- pulse to allow the next bit to be loaded into the Memory PCBs.

This sequence of setting CYCLE REQ-, putting the next data bit on to the highway and receiving XY CNT+ in acknowledgment continues, with counter 4E being clocked on each transaction. When the number of cycles counted by 4E corresponds with the count code established by bits D0, D3, comparator E6 pin 6 is set high. This inhibits the CYCLE REQ- pulse at the next END CYCLE- input and generates the DATA READY signal on 12B pin 9.

For a read sequence, the one bit mode is established by address bits H4, H3 when the required register address information is written in the Supervisor 214. This sets the output on decoder 9c pin 4 low. It is gated with the DIRECTION signal from 12B pin 13 to enable pin 5 on demultiplexers 6C, 5C.

When the input/output counter is cleared to zero, the output on pin 11 enables demultiplexer 5C pin 4 for a count of 0 - 7, 6C pin 4 for a count of 8 - 15. The serial data from the one bit highway (EC pin BN2) is input to 5C or 6C pin 6.

The Sync and Timing PCB returns on END CYCLE- signal via EC pin BD1 which pulses 11D pin 12 high to enable pin 5 on the demultiplexers and so preset the appropriate bit of the data register. It also generates another CYCLE REQ- pulse to allow the next bit from the one bit highway to be input to the demultiplexer, and XY CNT+ clocks counter 4E to the next data bit position.

The sequence of setting CYCLE REQ-, receiving END CYCLE- in acknowledgement and demultiplexing the next data bit onto the highway continues, with 4E being clocked on each transaction. Each data bit is held in the data register (1D - 8D) until read by the computer. When the number of cycles counted by 4E corresponds with the count code established by bit D0 - D3, comparator 6E pin 6 is set high to inhibit the CYCLE REQ- pulse at the next END CYCLE- pulse. It also sets the DATA READY+ signal on 12B pin 9 which is input to the command and status register to indicate data is available on the highway.

5.2.6 12 Bit Data Distribution Mode

For the 12 bit mode, decoder 9C pin 7 is set low and the input/output cycle is normally set to a count of 1. The output on 8E pin 10 is set high for a low count and is gated with the data register signal from decoder 13A pin 12 to set 16A pin 1 high. However, the REPLY- signal is inhibited by 12B pin 7.

For a write sequence, the data is set on highway lines 0 - 11 and input to the data register via transceivers 1C, 2C, 3C. They are applied to the D inputs of the data register flip-flops at the transceiver output. The data write pulse from 8E pin 4 causes 9D pins 3 and 6 to clock the data into the register.

The read sequence for 12 bit mode is set up as for the write sequence except that when the CYCLE REQ- signal is activated, the required data from the Memory PCBs is placed on the Supervisor 214 bus and input to the data register via the transceivers. The READ DATA- signal causes 8E pin 1 to pulse high to clear the register, and also enables the transceivers. The END CYCLE- signal is gated through 11D pin 8 and sets 9D pins 3 and 6 to clock the data through the register and onto the highway lines via the transceivers.

5.2.7 6 Bit and 8 Bit Data Distribution Modes

For the 6 or 8 bit data modes, decoder 9C pin 5 or 6 is set low; the I/O cycle is normally set at a count of 2, and 8E pin 10 is set high for a low count. For a write sequence, the data bits from the highway lines (1 - 5 for 6 bit, 1 - 7 for 8 bit mode) are clocked through the associated transceivers and flip-flops during the first input/output cycle as for the 12 bit mode. The XY CNT+ signal clocks the I/O counter and END CYCLE- reactivates the CYCLE REQ- signal. The next data bits (6 - 13 or 8 - 15) are placed on the highway and clocked through as before. Upon receipt of the next END CYCLE- signal, 6E pin 6 goes high to inhibit the CYCLE REQ- signal and generate the REPLY- and DATA READY+ signals.

For a read sequence, the procedure is as described above except that when 4E is cleared by 11E pin 6 pulsing high, the output from 4E pin 14 sets 10D pin 6 low so that the lower byte of the 6 or 8 bit data is clocked through to the highway first. This also sets the BYTE- output on EC pin BN1. At the next cycle count, 4E pin 14 goes high and sets 10D pin 8 low so that the upper byte is clocked through to the highway, and the BYTE- output is removed.

5.2.8 Erase Facility

The erase mode is enabled when bit 0 is set in the command and status register. It is input from H0 via 1B pin 3 and is set low to initiate an erasure signal, ERSGO+. This is clocked through 9E pin 2 by the CSR WRITE+ signal and the ERASE READY+ signal goes low. The next frame pulse clocks 9E pin 11 to drive ERS WRI (EC pin CB1) high, resets 9E pin 1, and maintains ERASE READY low via 8E pin 11. The erase is complete during the current frame and the next frame pulse clocks 9E pin 11 to invert the ERASE READY and ERS WRI signals.

5.2.9 Interrupt Facility

1. Field Interrupt : This is set by bit 6 in the command and status register. The computer uses the interrupt facility to control erasure, video switching and vertical scrolling.

   Bit 6 is a read/write bit and enables an interrupt to occur at the end of every field, i.e. when field status bit 7 goes high. It is written into the command and status register via 2B pin 15 and clocked through to 7B pin 12 by the CSR WRITE+ signal from 16D pin 10. The signal is gated through 9B pin 3 to set the interface interrupt signal on connector J1 pin 38 low.

2. Erase Interrupt : An erase interrupt is set by bit 8 in the command and status register. This read/write bit is input from H8 via 3B pin 3 and is clocked through to 7B pin 15 by the CSR WRITE+ signal from 16D pin 10. It is inverted and applied to 9B pin 1. If an erase write procedure is not in progress (i.e. the ERASE READY+ signal at 8E pin 13 is not set low), and the CSR WRITE signal has been negated, the erase interrupt signal is gated through to 9B pin 6 by the F.SYNC+ signal on EC pin BU2 to set the interface interrupt signal on connector J1 pin 38.

5.2.10 Watchdog/Flash Timers

Links are provided to set the required count on flash timers 13C, 12C and watchdog timer 11C.

The flash timers are clocked by the F.SYNC signal from EC pin BU2, and the output via balanced line driver 12A establishes the screen flash signals FLASH+ and FLASH- on EC pins CK2, CK1.

The watchdog timer is looking for computer action and is cleared when the output on 15D pin 3 goes low (i.e. read and a memory flag is selected). If the preset count is achieved before the timer is cleared, 12B pin 4 sets the watchdog signals (W.DOG+, W.DOG-) on EC pins CL1, CL2.

5.3 Address Computation

There is an option for Address Computation. For other option see Appendix M.

The Address Computation PCB is situated in position no. 4 of the control backplane and the circuit arrangements are shown on Drg. 02 - 485. Connections with other PCBs are made via edge connector sockets (EC).

The board contains the X and Y access registers for the X and Y co-ordinates for Access cycles, the Y offset register for the starting address for Scan cycles, and the addressing control register which sets up these registers for the required mode of operation.

The computer accesses the registers by register address lines A0- and A1- on EC pins BF1, BF2. These are enabled into decoder a3 by the AC WRITE signal, input from the Control PCB on EC pin AB1, in order to set up the selected register. They are also applied to selector a8 to ensure the computed addresses are multiplexed onto the memory address highway. The computed address is divided into row and column components to drive the 4k or 16k RAMs on the Memory PCBs. Links are provided to allow compatability with the memory capacity.

5.3.1 Addressing Control Register

During the addressing sequence, the computer sets the required parameters for the selected mode on highway bits D0 - D5:

Bit D0	Y access register, automatic count.
Bit D1	Sets count direction for Y access register. High = count up; low = count down.
Bit D2	X access register, automatic count.
Bit D3	Sets count direction for X access register. High = count up; low = count down.
Bit D4	Scan cycle, exchange mode.
Bit D5	Maintenance mode.

Signals A0, A1 are set low to clock data into the register buffer, b12. The data is clocked into the register, b15, when the Control PCB sets transfer control signal, XYTFR, low (EC pin AD1).

5.3.2 Access Cycle Addressing

An Access cycle allows the computer to randomly address the Memory PCBs.

The relevant bits in the addressing control register (D0 - D3) which set the required access mode are clocked through d5 by signal XYTFR- from the Control PCB and set up the X and Y access registers.

The computer sets the X or Y co-ordinates on the data highway and they are converted by the address computation logic into the bit, row and column addresses. The co-ordinates are clocked into the buffer registers (d14, c14 for the Y co-ordinates, c12, b12 for the X co-ordinates) by decoder a3 pin 5 or 4 as selected by programmable flags A0, A1:

A0	A1	
H	H	X access register
L	H	Y access register

The physical memory address is calculated from the X and Y co-ordinates according to the formula:

Y(HRES) + X

The Y co-ordinates from the Y access buffer register (d14, c14) are loaded into Y access counter d13 c13 b13 by the trailing edge of the XYTFR- pulse which also provides a clock pulse via monostable d1 to clock the co-ordinates through the counter. If automatic counting is required, the XYTFR- pulse clocks highway bits D0 and D1 through b15 to set counter pins 7 and 10 low for automatic count, and counter pin 1 high or low to increment or decrement the count. The counter is consequently clocked by a XYCNT+ signal from the Sync and Timing PCB (EC pin AC1) at the end of each cycle.

The counter outputs are applied to multiplexers d11 c11 b11 The select pins on these units are controlled by the repeat field signal R.FIELD on EC pin BR2 such that the A inputs are selected for a repeat field system and the B inputs for a non-repeat field system. The A and B inputs are arranged so that for a non-repeat field system., the LSB from the counter becomes the MSB for the memory, and the remaining Y value bits are shifted down one place. This causes even lines to be stored in the lower half, and odd lines in the upper half of memory (see Fig. 4.1).

The 11 bit output from d11 c11 b11 is applied to multiplexers d9 , c9 , b9 and d10 c10 b10 The multiplication factor signals MF0, MF1, MF2 on EC pins CJ1, CJ2, CK1 determine the horizontal resolution value (HRES) which may be as follows:

256	(128 x 2)
384	(128 x 3)
512	(128 x 4)
768	(128 x 6)
1024	(128 x 8)

With MF2 set low, multiplexers d9 , c9 , b9 select 1Y or 4Y as determined by signal MF0, and d10 c10 b10 select 2Y or 4Y as determined by MF1. With MF0 set high, d9 , c9 , b9 are inhibited. The selected outputs are then input to adders d6 , d7 , c7 , to provide the required Y(HRES) value.

The X co-ordinates from the X access register (b12, c12) are loaded into X access counter b8, c8, d8 as described for the Y access counter above, and the counter is set up for automatic counting if required by address control register bits D2, D3.

The outputs from counter b8 pins 14, 13, 12, 11 and c8 pin 14 provide the memory address bits M0 - M4. The outputs on c8 pins 13 and 12 provide the access row signals AR1, AR0. The remaining outputs from the X access counter are input to adders d5, d4, c6 for summing with the Y(HRES) value from d6, d7, c7 to give the single physical address.

The output from d5 pin 15 (for 16k memory) or pin 6 (for 4k memory) is input to d11 pin 14 to provide the MSB for a repeat field system. The remaining outputs from d5 d4, c6 provide the access column (AC0 - AC5) and access row (AR2 - AR6) addresses which are applied to multiplexers b7, b6, b5, b4 for selection onto the memory address highway by multiplexer a8.

The computed access column and row addresses are input to multiplexers b4, b5, b6 & b7. The actual address to be multiplexed onto the internal and memory address highways is selected via multiplexer a8. The select input on a8 pin 1 is set low for Access cycles so that the outputs follow the A inputs, and signal RCS1 on EC pin BB1 is set high. Row or column is selected by signal RCS0- on EC pin BA1 which is set low for row, high for column.

The selected address is multiplexed onto the memory address highway via buffers a13, a14, and a15.

5.3.3 Scan Cycle Addressing

For Scan cycles, register address line A0 is set high and A1 low so that signal AC WRITE, via a3 pin 6, clocks the Y offset value (data bits D0-D13) into the Y offset register, d3, d2, d1. This register sets the actual address at which scanning of the visible picture begins, and the address provides the input to the scan counter.

The scan counter comprises c3, c2, c1, b1 and is controlled by multiplexer a10. The strobe, pin 15, is tied low and the select input, pin 1 is set low by the maintenance bit (D5) from the addressing control register.

For Scan cycles, the outputs on a10 follow the A inputs when the field is unblanked. Flip-flop A12 is clocked b on EC by FUNBNK+ at the start of the unblanked period which enables the next LINE SYNC pulse to load the start address into the scan counter. During the remainder of the field, the scan counter is clocked by SCAN UP.

The six least significant bits of the scan counter are not affected by the mode of operation and are connected directly to the multiplexers b4, b5 and b6. Higher order bits are dependant upon whether 4k or 16k RAMs are in use and upon scrolling techniques. Patch panel C1 links the counter outputs to the multiplexers to suit the size of RAM, and selector b3 routes the counter outputs according to the mode of scrolling (see Fig. 42).

For a repeat field system, b3 pin 2 is set low so that SC6 and/or SC5 follow the scan counter outputs. Vertical scroll is controlled by the Y offset value from the computer (see sub-section 2.3.1).

For interlaced systems where vertical scrolling is not required or is required by an even number of lines, the exchange input on b3 pin 14 is set low. The outputs SC6 and/or SC5 follow the ODDEVE field input on b3 pins 4 and 12. If vertical scrolling is required by an odd number of lines, the computer sets the exchange bit in the addressing control register so that b3 pin 14 is high. The outputs now follow the inverted ODDEVE field input on b3 pins 3 and 13 to alternate the memory partition selection.

The scan column and row addresses from the scan counter, are input to multiplexers b4, b5, b6, b7. The actual address to be multiplexed onto the memory address highway is selected via multiplexer a8. The select input ona8 pin 1 is set low so that the outputs follow the A inputs, i.e. Scan cycles are selected by signal RCS1 on EC pin BB1 which is set low for scan. Row or column is selected by signal RCS0- on EC pin BA1 which is set low for row, high for column.

The selected address is multiplexed onto the memory address highway via buffers a13, a14, a15.

5.3.4 Maintenance Mode

The purpose of maintenance mode is to allow the computer to verify the physical memory addresses generated from the X and Y access registers, the Y offset register and the scan counter.

For maintenance mode, bit D5 in the addressing control logic is set high and is clocked throughb15by the XYTFR- signal. It is input to the scan counter multiplexer a10and the address selection multiplexer a8 to inhibit the normal clocking of the scan counter and selection of the memory address.

A diagnostic program loads the X and Y access registers and the Y offset register with a range of values, and the resultant access or scan addresses are read by the computer to check the accuracy of the address computation circuits.

The diagnostic values for the Y offset register are loaded in the scan counter by the XYTFR- signal. This signal also provides the clock pulse via monostable a9 which causesa11 pin 6 to pulse high.

For address selection, the maintenance bit fromb15pin 15 setsa8 pin 1 high so that the a8 outputs follow the B inputs which are derived from the register address lines A0, A1 as follows:

A0	A1	Decoder a3	Selector a8
H	H	X access register	Access row address
L	H	Y access register	Access column address
H	L	Y offset register	Scan row address
L	L	Address control register	Scan column address