SC750/B1 SC750/B3

(RM03/RM05/RM80 COMPATIBLE)

DISK CONTROLLER

TECHNICAL MANUAL

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Section 1
INTRODUCTION

1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the SC750/B Disk Controller. In addition, this manual provides diagnostic and application information.

1.2 OVERVIEW

1.2.1 General Description

The SC750/B Disk Controller is a one-board imbedded controller for the VAX-11/750 computer manufactured by Digital Equipment Corporation. The controller serves as an interface between the computer and up to four large disk drives with Storage Module Drive (SMD) interfaces. The SC750/B controller emulates a DEC RM03, RM05 and/or RM80 Massbus disk subsystem, including the Massbus Adapter (RH750) and the logic in each of the drives connected to the Massbus. The controller is capable of operating with disk drives having different characteristics from those used in the DEC disk subsystems. The SC750/B controllers provide the capability of operating with a mixture of disks having storage capacity of 80 to 600 megabytes.

1.2.2 Controller Models

The SC750/B Controller is available with either /B1 or /B3 firmware. The controller model can be identified by its top level assembly number, which is located on the IC at location U28. The SC750/B1 is top level assembly number SC7510201-B1X and the SC750/B3 is top level assembly number SC7510201-B3X (X is the revision level of the firmware). The difference between the two models lies in their support of the 2351A Fujitsu Disk Drive. The /B1 firmware supports a 44 sector configuration of the 2351A. The /B3 firmware supports a 48 sector configuration of the 2351A, allowing use of an additional 40 Mb of capacity. The 2351A Fujitsu must be hard sectored according to specifications in Appendix A. See paragraph 3.2.6 for more information.

1.3 FEATURES

1.3.1 Microprocessor Design

The SC750/B design incorporates a unique 16-bit bipolar microprocessor to perform all controller functions. The microprocessor approach provides for a reduced component count, high reliability, easy maintainability, and most importantly, the ability to adapt a single set of hardware to a wide range of emulation capabilities through the use of microprogramming. The

Emulex controllers achieve functional capability beyond that of the DEC controllers which they emulate, by providing enhancement features such as built-in self-test during power-up, built-in disk formatting and the ability to work with disk drives of various sizes.

1.3.2 Packaging

The SC750/B is constructed on a single extended hex-size multi-layer PC board which is designed to plug directly into one of the three Massbus controller slots of the VAX-11/750. No cabling is required between the computer and the disk controller. The controller obtains its power from the VAX-11/750.

1.3.3 Self-Test

The controller incorporates an internal self-test routine which is executed upon power-up. This test exercises all parts of the microprocessor, buffer and disk data logic. Although this test does not completely test all controller circuitry, successful execution indicates a very high probability that the controller is operational. If the controller fails the self-test, it leaves the fault LED on and the controller cannot be addressed from the CPU.

1.3.4 Buffering

The controller contains a 1K x 16 high-speed RAM buffer used to store the MBA and map registers of the controller, the drive registers for eight drives, and one sector of data buffering.

1.3.5 Error Correction

The controller incorporates a 32-bit error correcting code (ECC) capable of correcting single error bursts of up to 11 bits in length and detecting bursts of longer length. The controller determines the location of the error and the error pattern and then passes this information back to the VAX-11/750 which actually performs the correction of the erroneous data. A 16-bit CRC is employed with the header of every sector.

1.3.6 Option and Configuration Switches

Three eight-pole DIP switches are used to configure the controller for various disk sizes, certain firmware options, MBA number and arbitration level. It is possible to select one of 32 possible combinations of disk characteristics for the four drives which can be handled by the controller, including mixtures of disk sizes and drive type codes.

1.3.7 Get Characteristics Capability

Since the SC750/B series of controllers can handle a number of different drive sizes, a capability has been provided to readout the maximum cylinder, maximum track, and maximum sector address, as

well as the selected drive type code. This is useful for self-configuring software to handle different drive configurations and sizes on the same controller.

1.3.8 Dual Port Capability

The controller can operate with disk drives having dual port capability which allows a second controller to have access to the drive on a priority basis.

1.4 FUNCTIONAL COMPATIBILITY

1.4.1 Functionality

The SC750/B is functionally compatible with the DEC RH750 Massbus Adapter with one or more RM type disk drives attached, except that the controller does not execute the diagnostic mode of the RH750 or the maintenance mode of the RM drive. The absence of the diagnostic mode prevents running the complete RH750 diagnostic program.

1.4.2 Media Compatibility

The SC750/B is media compatible with the DEC RM02/RM03 packs when using a CDC 9762 drive or equivalent and with the DEC RM05 when using a CDC 9766 drive or equivalent. There is no need for media compatibility with the RM80 since it is a fixed-media drive, but the format is the same as used by the DEC RM80.

1.4.3 Diagnostics

The controller executes the following standard DEC RM03, RM05 and RM80 diagnostics:

EVRAA	VAX RP/RK/RM/RX/TU58 Reliability
EVRAC	Disk Formatter
EVRDA	RM03/5 RM80 Diskless Diagnostic
EVRDB	RM03/5 Functional Diagnostic
EVRGA	RM80 Formatter
EVRGB	RM80 Functional Diagnostic

1.4.4 Operating Systems

When emulating standard size RM03, RM05 or RM80 drives, the controller is compatible with the VAX/VMS operating system. Non-standard size drives can be used by appropriate patching to the disk driver and booting facility.

Table 1-1

GENERAL SPECIFICATIONS

Functional	
Emulation	DEC RM03, RM05 and RM80
Media Compatability	DEC RM03 and RM05 when using appropriate disk drives.
Drive Interface	SMD
Drive Ports	4
Error Control	32-bit ECC for data and 16-bit CRC for headers. Correction of single data error burst of up to 11 bits.
Sector Size	512 bytes
Sectors/Track	32
Tracks/Cylinder	Selectable for each drive.
Cylinders/Drive	Selectable for each drive.
Drive Type Code	Selectable for each drive.
Computer Interface	VAX-11/750 CMI
CMI Address (hex)	F28000, F2A000 and F2C000
Vector Address (hex)	150, 154, 158 and 15C
Priority Level	BR5
Data Buffering	1 full sector
Data Transfer	32-bit DMA via CMI
Self-Test	Extensive internal self-test on powering up.
Indicators	Activity and Fault LEDs

Table 1-1 (cont'd)

Design	High-speed bipolar microprocessor using 2901 bit-slice components.
Physical	
Packaging	One DEC extended hex-size board.
Mounting	Any VAX-11/750 Massbus controller slot.
Disk Connection	Paddle board on rear of backplane has connectors for A cable and four B cables.
Electrical	
CMI Interface	DEC approved line drivers and receivers.
Drive Interfaces	Differential line drivers and receivers. A cable accumulative length to 100 feet. B cable length to 50 feet.
Power	+5 v, 10 Amp. max. -15 v, 1 Amp. max.

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2.1 CONTROLLER ORGANIZATION

A block diagram showing the major functional elements of the SC750/B controller is shown in Figure 2-1. The controller is organized around a 16-bit high-speed bipolar microprocessor. The ALU and register file portion of the microprocessor are implemented with four 2901 bit slice components. The microinstruction is 48 bits in length and the control memory of 2K words is implemented with twelve 2K x 4 PROMs.

The controller incorporates a 1K x 16 high-speed RAM buffer which is used to store the controller's MBA and drive registers, map registers and one sector of data buffering.

The A Cable Register (ACR) provides the storage of all A cable signals going to the disk drives. The inputs from the selected drive are testable by the microprocessor.

Serial data from the drive is converted into 16-bit parallel data and transferred to the buffer via the microprocessor. Likewise, the data access from the buffer by the microprocessor is serialized and sent to the drive under the control of the servo clock received from the drive. A 32-bit ECC Shift Register is used to generate and check the ECC for the data field. The same register is also used in a 16-bit CRC mode for the headers. The actual ECC polynomial operation is done independent of the microprocessor, but the determination of the error position and error pattern is done under the control of the microprocessor.

A configuration PROM is a source to the data bus. This PROM configures the maximum cylinder address, maximum track address and drive type code for each of the logical drives.

The CMI interface is a 32-bit wide bus over which addresses and data are transferred. It is used for programmed I/O and DMA data transfers. The microprocessor responds to all programmed I/O and carries out the functions required for the addressed controller register. The microprocessor controls all DMA operations and transfers data between the CMI and the internal buffer.

2.2 PHYSICAL DESCRIPTION

The SC750/B controller consists of a single extended hex-size board which plugs directly into a Massbus Controller (RH750) slot (7, 8 or 9) of a VAX-11/750 chassis. Figure 2-2 shows the board. A connector paddle board plugs onto the pins at the rear of the connector used for the controller. This board provides connection for the disk A cable and up to four B cables.

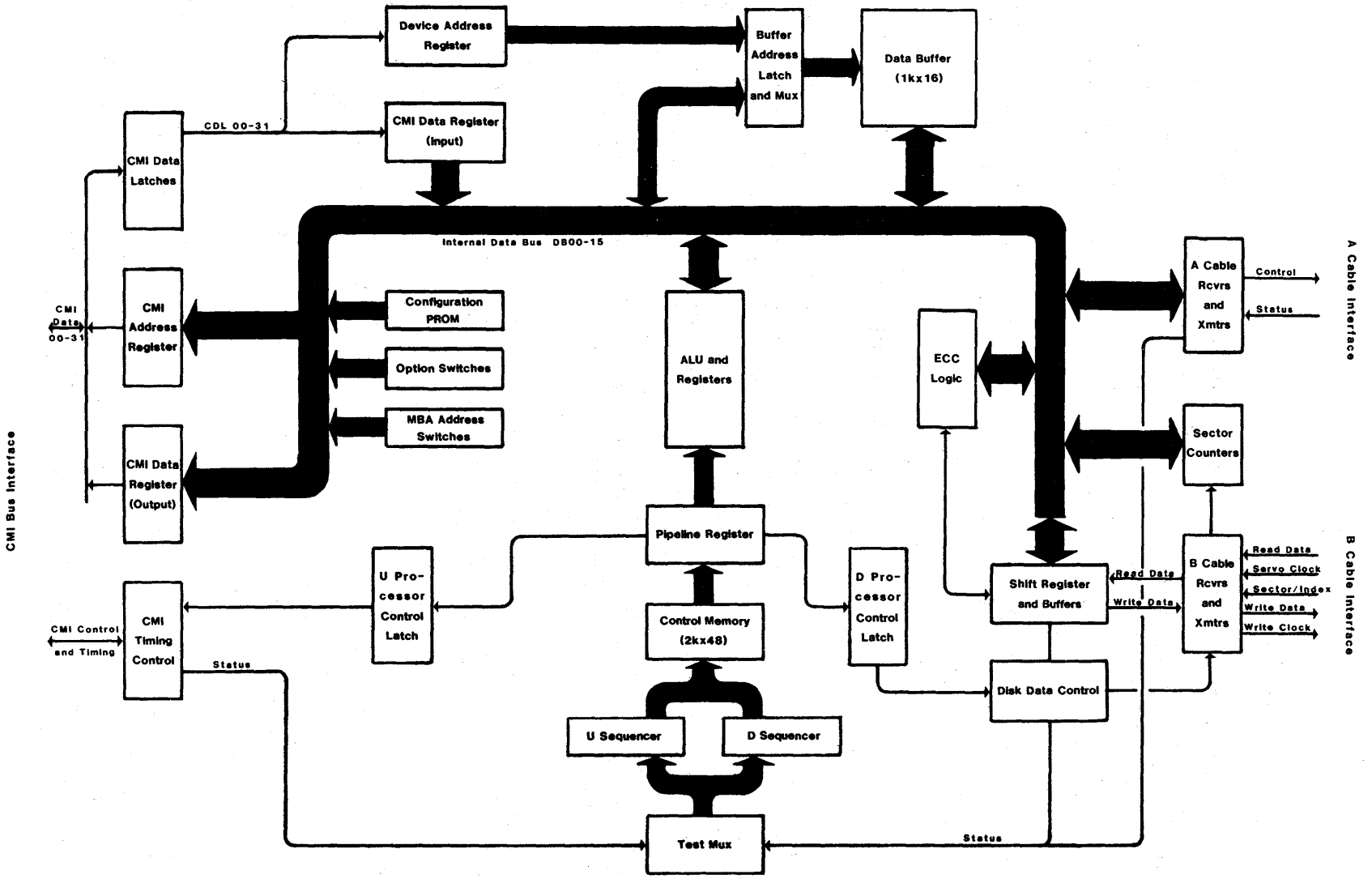


Figure 2-1 SC750 Block Diagram

2.2.1 Connectors

Connectors J1 and J2 are used with the Emulex test panel during manufacturing test and factory repair. They have no use in normal operation.

2.2.2 Switches

The three eight-pole DIP switches labeled SW1, SW2 and SW3 are used to configure the controller. SW1 provides firmware options, while SW2 provides selection drive configurations. SW3 is used to configure the MBA address and CMI arbitrate level.

2.2.3 Indicators

There are two LED indicators mounted between the connectors at the top of the board. They have the following use:

Fault - Indicates unsuccessful self-test execution. A flashing LED indicates successful self-test, but unable to find any drive connected and/or powered-up.

Activity - Indicates disk read or write activity.

2.2.4 PROMs

There are 24 PROM sockets used for the control memory located along the right edge of the board. Normally only 12 PROMs are used. The sockets are labeled PROM 0 through PROM 11. The numbers on the top of the PROM ICs are Emulex part numbers, which identify the unique pattern of the PROM. When inserting PROMs in the board, the ID numbers are placed in the same sequence as the PROM numbers on the board beside each socket.

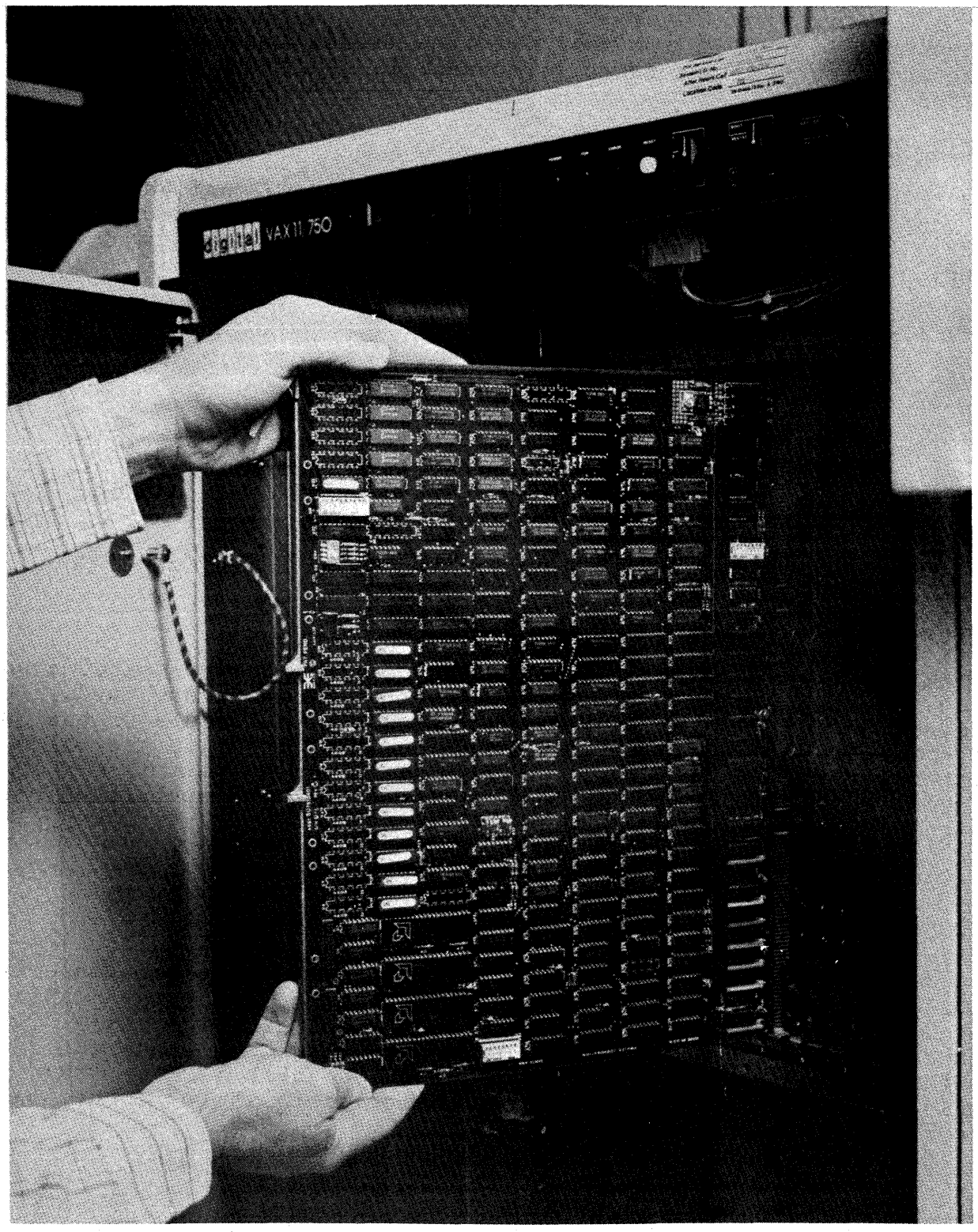
2.2.5 Paddle Board

2.2.5.1 A Cable Connectors

The 34-pin flat cable connector labeled J1 and the 26 pin connector labeled J2 at the top edge of the board are used for the A cable which daisy-chains to all the drives for control and status. Two connectors are used for the 60-conductor A cable to reduce the size of the paddle board. This does require a special A cable. Pin 1 is located on the left side of the connectors. The circuitry on the board are the A cable drivers.

2.2.5.2 B Cable Connectors

The four 26-pin flat cable connectors labeled J3, J4, J5 and J6 are for the radial B cables to each of four physical drives which may be attached to the controller. Pin 1 is located on the left side of the connector. The four B cable ports are all identical and any drive may be plugged into any connector.



SC7501-0057

Figure 2-2. SC750 Disk Controller

2.3 INTERFACES

2.3.1 Disk Interface

The A cable signals are taken off the controller board on the lower half of the backplane B connector (pins 53-92). The four sets of B cable signals are taken off the controller board on the backplane C connector (pins 3-42 and 53-92).

The controller implements the eleventh cylinder bit on the normally spare A cable pins 30 and 60.

The controller's disk interface conforms to the Flat Cable Interface Specification for the SMD, MMD, and CMD (CDC Document No. 64712400). The controller has been tested with most drives using the SMD interface and is compatible with these drives electrically and in timing.

The following defines the electrical interface and the recommended cables.

2.3.1.1 Drivers and Receivers

The drivers for the A and B cables are MC3453, which are equivalent to the 75110A. The receivers are MC3450 quad differential receivers, which are equivalent to 75108 receivers. The lines of the A cable are terminated with 82 ohms to ground. The lines of the B cable are terminated with 56 ohms to ground.

2.3.1.2 A Cable

The 60-conductor A cable is daisy-chained to all drives and is terminated at the last drive. The signals in this cable are listed in Table 2-1 along with their function when the control tag (Tag 3) is asserted. The A cable should be 30 twisted pair flat cable with an impedance of 100 ohms and an accumulative length of no greater than 100 feet.

2.3.1.3 B Cable

The 26-conductor B cable is a radial to each drive and contains the data and clock signals. In addition, it contains sector and index signal to drive the sector counter for the drive. The signals and grounds in this cable are listed in Table 2-1. The B cable should be 26 conductor flat cable with ground plane and drain wire. The impedance should be 130 ohms and the length must not be greater than 50 feet.

2.3.1.4 Pick and Hold Signals

The Pick and Hold signals which control the starting of the disk drive when it is remote, are activated when the controller is not being reset by DCLO.

Table 2-1
Disk Drive Connections

Pins Lo/Hi	Signal	(Tag 3 Function)	From/To
A Cable:			
22,52	Unit Select Tag		To
23,53	Unit Select bit 0		To
24,54	Unit Select bit 1		To
26,56	Unit Select bit 2		To
27,57	Unit Select bit 3		To
1,31	Tag 1		To
2,32	Tag 2		To
3,33	Tag 3		To
4,34	Bit 0	(Write Gate)	To
5,35	Bit 1	(Read Gate)	To
6,36	Bit 2	(Servo Offset Plus)	To
7,37	Bit 3	(Servo Offset Minus)	To
8,38	Bit 4	(Fault Clear)	To
9,39	Bit 5	(AM Enable)	To
10,40	Bit 6	(Return to Zero)	To
11,41	Bit 7	(Data Strobe Early)	To
12,42	Bit 8	(Data Strobe Late)	To
13,43	Bit 9	(Release)	To
30,60	Bit 10		To
14,44	Open Cable Detect		To
15,45	Fault		From
16,46	Seek Error		From
17,47	On Cylinder		From
18,48	Index		From
19,49	Unit Ready		From
20,50	Address Mark Found		From
21,51	Busy (dual port only)		From
25,55	Sector		From
28,58	Write Protected		From
29	Power Sequence Hold		To
59	Power Sequence Pick		To
B Cable:			
8,20	Write Data		To
6,19	Write Clock		To
2,14	Servo Clock		From
3,16	Read Data		From
5,17	Read Clock		From
10,23	Seek End		From
22,9	Unit Selected		From
12,24	Index		From
13,26	Sector		From

2.3.2 CMI Interface

The CPU Memory Interconnect (CMI) is a 32-bit wide tri-state bus which is used to interconnect the CPU, memory controller, Unibus Interface and up to three Massbus Adapters. It transfers both data and addresses in a multiplexed manner. The CPU accesses the controller by means of this interface for reads and writes of the controller's registers and the controller uses it for DMA data transfers with memory.

2.3.2.1 Arbitration Level

The arbitration level controls the priority of the controller obtaining the bus for DMA. Levels three, two or one may be selected for the controller. These three levels are below the Unibus Interface which is level four.

2.3.2.2 BR (Interrupt) Priority Level

The controller is hardwired for BR5. The other three Bus Grant signals are jumpered through.

2.3.2.3 Register Address

The three possible controller base addresses are: F28000, F2A000 and F2C000.

2.3.2.4 Interrupt Vector Address

The three interrupt vector addresses which correspond to the three base addresses are: 150, 154 and 158. Selection of the controller base address automatically selects the interrupt vector address.

2.3.2.5 DCLO

The controller is held in a reset condition as long as UBUS DCLO is asserted. Upon release of this signal the controller will execute its self-test. The UBUS INIT signal is not used by the controller.

2.4 DISK FORMAT

2.4.1 Disk Organization

The SC750/B emulates one or two logical RM drive units per physical drive. For a standard RM emulation, the typical number of sectors formatted per track is typically 32. The unit number of the physical drive must be in the range of 0-3.

When a physical drive has two logical RM units mapped onto it, the first logical unit will be mapped onto the first half of the heads and have a unit number the same as the physical unit number; the second logical unit will be mapped onto the second half of the heads and have a unit number which is four greater than the physical unit number.

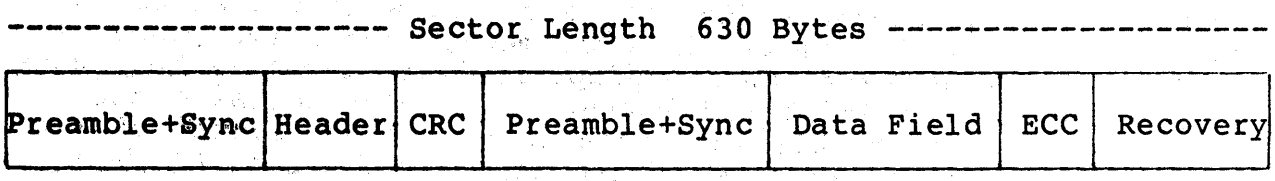
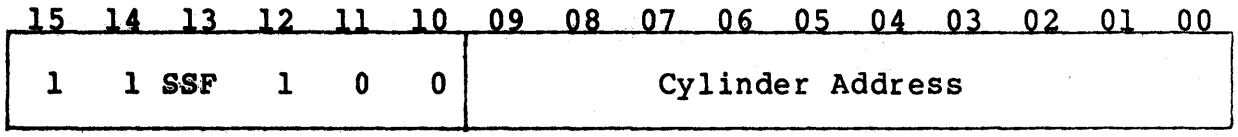
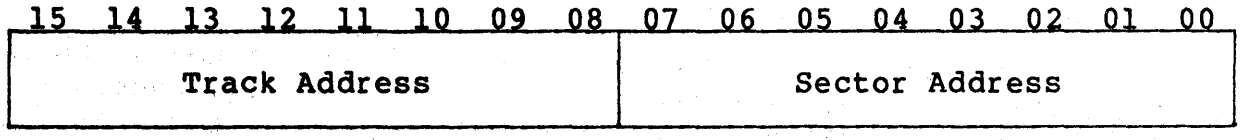


Figure 2-3 Sector Format

Header Word 1:



Header Word 2:



Header Word 3:

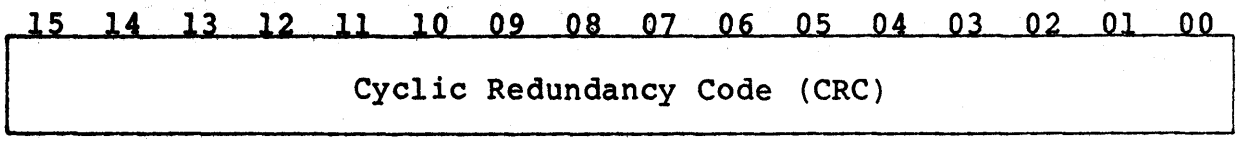


Figure 2-4 Header Format

2.4.2 Track and Cylinder Mapping

When the number of heads on the physical drive is equal to the number of tracks on the RM drive being emulated, there is a one to one correspondence between tracks and cylinders. This is essential for media compatible disk packs such as RM03 and RM05. When the physical drive has a number of heads which is different than the RM drive, the controller operates in a mapped track and cylinder mode. When operating in this mode with RM03/RM05 emulations, the drive should be configured for one extra sector so that there is additional time at the end of each track to do the mapping.

2.4.3 Sector Organization

Figure 2-3 shows the sector format used by the controller. A disk drive with 20,160 bytes per track is typically divided into 32 sectors of 630 bytes. The four byte header is preceded by a preamble of 30 bytes ending in the sync byte and is followed by a two byte CRC. The 256 word data field is preceded by a preamble of 20 bytes ending in the sync byte, and is followed by four bytes of ECC. This format is compatible with that of the DEC RM02/RM03 and RM05.

If the actual size of the useful data information is less than 512 bytes, the remainder of the data field will be filled with zeros until 512 bytes have been written. During disk formatting procedures, each data track is located and recorded with header information by means of the Write Header and Data command. A disk pack should be formatted and the format verified before any real data is written on it. Once formatted, individual or groups of sectors should not be reformatted unless absolutely necessary.

2.4.4 Header

2.4.4.1 Header Description

Figure 2-4 shows the header format, which consists of the following three words:

Word One -

This word contains the cylinder address. It contains a one-bit in bit 12 to identify 16-bit format to the software and one-bits in bit positions 14 and 15 to identify a good sector. For RM80 emulations, a one in bit 13 indicates that the data for this sector has been relocated to the next sector.

Word Two -

The low-order eight bits of this word contain the sector address. Each track on the drive typically contains 32 sectors. The upper byte of this word contains the track address.

Word Three -

This is the CRC word which is generated and checked by the controller logic. This word is not available to the software.

2.4.4.2 Header Field Handling

After the drive reports that it is on cylinder, the controller locates the desired sector by means of the sector counters for each drive. The sector counters are maintained in the controller. The controller compares the first two words of the header against the desired track, sector and cylinder and then checks the CRC word for errors. An error in the header field is indicated by turning on the appropriate error bit in the error register (format error, header compare error, bad sector error, skip sector error or CRC error). A header error is only valid when the sector count field of the RMLA register and the sector field of the RMDA have already matched. It is immaterial where a CRC error occurs in the header field since the controller cannot determine its location in the field. However, software may read the header to memory by means of a Read Header and Data command. The header compare may be inhibited by setting the HCI bit in the RMOF register.

2.5 GENERAL PROGRAMMING INFORMATION

2.5.1 Clearing the Controller

The controller can be cleared using the following methods.

a. Controller Clear - Controller Clear is performed by writing a one-bit into the INIT bit of the MBACR or by UBUS DCLO. This causes the following to be cleared:

   - MBACR, MBASR, MBADR is set to a "BF".
   - In all drives: RMCS1 bits <06:00>; RMER1; RMER2; RMDA; RMAS ATA bit; RMEC2; RMDS ATA, ERR and LST bits; RMMR1 bits <15:04>, <02:00>. Sets bit 03 of RMMR1 and DRY of RMDS.

b. Error Clear - The error bits in MBASR are cleared by writing a one-bit into the bit position and by the start of another data transfer operation.

c. Drive Clear - The Drive Clear is a command (Code 9). This causes the following registers in the addressed drive to be cleared:

   - RMER1; RMER2; RMAS ATA bit; RMEC2; RMDS ATA and ERR bits; RMMR1 bits <15:04>, <02:00>. Sets bit 03 of RMMR1.

2.5.2 Interrupt Conditions

The controller generates a CPU interrupt if the Interrupt Enable (IE) bit is set upon the following conditions:

a. Upon termination of a data transfer, either normally or abnormally.

b. Upon assertion of any of the drive attention bits.

c. Upon occurrence of a Programming Error (PGE), Non-existent Drive (NED) or Missed Transfer Error (MXE).

The interrupt condition will persist until the interrupting status bits are cleared.

2.5.3 Termination of Data Transfers

A data transfer which has been successfully started may terminate in the following ways:

a. Normal Termination - Byte count overflows to zero and the controller becomes ready at the end of the current sector.

b. Controller Error - One or more of the following MBASR bits are set:

    Data Transfer Abort (DTA)
    Data Late (DLT)
    Write Check Upper Error (WCU)
    Write Check Lower Error (WCL)
    Exception (EXC)
    Invalid Map (IM)
    Error Status (ERR)
    No Response Status (NRS)

c. Drive Error - The ERR bit in the RMDS register and at least one bit in RMER1 or RMER2 register is set. The ATA for the drive doing the data transfer becomes asserted.

d. Program-Caused Abort - By setting the Abort or INIT bits in MBACR the program can terminate a data transfer operation.

2.5.4 Ready Bits

There is no ready bit for the controller. Data Transfer Busy (DTB) in MBASR is set when a data transfer operation is underway. It is cleared when the data transfer is terminated. On read operations this occurs when the last word has been transferred to memory. On write operations this occurs when the last sector has been written. Data Transfer Complete (DTC) is set when the operation terminates.

DRY (RMDS, bit 07) is the ready indicator for the selected drive and is the complement of the drive's GO bit. To successfully

initiate a data transfer command this bit must be asserted. However, a non-data transfer command (Search, Drive Clear) may be issued to a drive at any time DRY is asserted regardless of the state of the DTB bit.

When a data transfer command is initiated DRY becomes negated and DTB becomes asserted.

2.6 DUAL CONTROLLER OPERATION

SMD drives may be equipped with a dual port option which provides the capability for two controllers (generally on separate computers) to access the drive. The SC750/B controller supports this type of operation as a standard feature. This mode of controller operation is selected by setting SW1-6 ON. Most of the dual port functions of the DEC controller being emulated are supported, and those which are not should be transparent to a properly written dual port driver. Table 2-2 summarizes the controller register responses in dual port operation.

2.6.1 Dual Port Drives

The two drive ports are known as Channel I and Channel II. Because only one controller may access the drive at a time, access is granted on a first-come, first-served basis. Once a controller has gained access to the drive, the other controller is denied access until the first controller's operation is complete. However, each channel has a physical disable switch which can disable the port and prevent the associated controller from having access to it.

2.6.2 Unseized State

The drive is in the unseized state when it is not connected to either controller. The CPU must issue a request for the controller to seize the drive. This request is done in one of the following ways:

a. Writing into any drive register, including read-only registers.

b. Writing a one-bit into the drive's ATA bit in RMAS. The bit does not have to be set.

2.6.3 Seized State

The drive is seized when it is logically connected to one of the controllers. At that time DVA (RMCS1, bit 11) is set indicating that the drive is ready to communicate with the controller which has seized it. If the drive has already been seized by the other controller, then the DVA bit will not set, all the drive registers will read as zeros and any write to a register will be ignored. Attempts to seize a drive which is busy with the other port are remembered and then acted upon when the drive is released by the other controller.

2.6.4 Returning to the Unseized State

The drive is released and returned to the unseized state by issuing a release command. In addition, a one second timer in the controller will timeout and release the drive if one of the events listed in section 2.6.2 for seizing the drive is not performed periodically to keep resetting the timeout timer. Reading the RMCS1 register will also reset the timeout timer if the drive is currently seized. This allows the CPU to check a drive's seized state, and if seized, not have to worry about a time-out release occurring.

When the controller sees a previously busy drive becoming unseized, it checks its request flag. If the flag is set (the drive had been requested while busy on the other port), the controller will seize the drive and set ATA causing an interrupt to the CPU if the IE bit is set. If the CPU does not respond to the attention within one second the drive will be released, but ATA remains set.

2.6.5 DEC Compatibility

The SC750/B controller differs from the equivalent DEC controller in three important areas.

First, there is no neutral state. Since the SC750 does not have instantaneous access to all drives at the same time (a limitation of the daisy-chained A cable and the microprocessor organization of the controller), the controller assumes the drive is busy on the other port if the controller has not already seized it. Thus, a read of RMCS1 will always indicate that the drive is seized by the other controller (DVA, bit 11 equals zero) unless the drive has been previously requested. The CPU must request the drive by writing into any drive register and wait until the ATA bit is set which indicates that the controller has seized the drive. If the drive was in reality not seized by the other controller, this will happen almost immediately. The DEC controllers, however, can switch from neutral to seized state within the time required to do a single read or write of a drive register. Thus, if the drive is not already seized, no ATA is set and the drive is immediately available to the seizing controller.

Second, the release command is not instantaneous since the controller takes a few microseconds to execute the command. During this time the drive will appear to be unseized.

Third, during a data transfer the timeout timers will not operate and the drives can not be polled to see if they are not busy. Therefore no drives are seized or released during the execution of a data transfer.

The software driver should not issue a Release command and then attempt to save the current status of a drive, since the Release command will immediately show the drive in the unseized state, thus returning zero data for the drive registers. In order to allow the

other controller time to poll the drive, the CPU should not communicate with any of the released drive's registers until required to seize the drive again.

2.6.6 Dual Port Drives in Single Port Mode

When using an operating system which does not have dual port drive software support, it may still be advantageous to use dual port drives while operating in the controller in single port mode. This will allow for a non-dynamic type of operation between two CPUs. In this type of operation the controller does not unseize the drive and, in effect, it is seized by both controllers all the time.

The one second timeout timer (and the release command) operate exactly as stated in paragraph 2.6.4. Even when released, a drive will still appear to be seized to the releasing controller. No attention is generated when the other controller finds the drive not busy. Should a command be issued to a controller while a drive is busy on the other port, the controller will wait until the drive becomes unbusy before executing the command. No timer exists in this case.

This mode of operation eliminates the need for manually switching the drive from one controller to another.

2.6.7 Dual Access Mode

In order to provide compatability with VMS when it is configured for dual access, the dual access mode is provided (SW4-4 ON). When in this mode, the controller sets Dual Port Mode (Drive Type Register) and Programmable (Drive Status Register) to imitate the DEC neutral state.

When DPM and PGM are set, the operating system will attempt to seize a drive by simply writing a command to it. If the drive is unbusy the command is executed. If the drive is already busy on its other port, the controller simply waits until it is released and then seizes and commands it. VMS has a timer sufficiently long to prevent causing a timeout when it is forced to wait.

The first time the SC750 sees a drive, it is ignored for one second. This one-second stall occurs once for each drive on the controller. It prevents the controller from seeing erroneous status information when power is applied to the drive after the controller has been powered-up. For a drive in dual port mode the stall will prevent the other CPU from accessing the drive until the stall completes. The dual access option switch bypasses the stall in all cases. For proper system operation with the dual access option switch ON, all drives must have power applied before either controller is powered-up.

Setting the Dual Port Option switch overrides the Dual Access Option, except for the power-on timer override.

Table 2-2
Register Access on Dual Controller Operation

Controller Action Drive State:	Response With Respect To Action On Ch. I
Read RMCS1	
Drive Not Seized:	Reads all zeros. No request flag is set.
Drive Seized by Ch. I:	DVA = 1; reads the register. Resets timer.
Drive Seized by Ch. II:	Reads all zeros. No request flag is set.
Read any other drive register	
Drive Not Seized:	Reads all zeros.
Drive Seized by Ch. I:	Reads the register.
Drive Seized by Ch. II:	Reads all zeros.
Write RMCS1	
Drive Not Seized:	The function code is attempted if GO = 1. A port request flag is set.
Drive Seized by Ch. I:	Loads the function code. (Switches to unseized if the function is a Release).
Drive Seized by Ch. II:	The function code is attempted if GO = 1. A port request flag is set.
Write any drive register	
Drive Not Seized:	The write is ignored, and a port request flag is set.
Drive Seized by Ch. I:	Loads the register.
Drive Seized by Ch. II:	The write is ignored, and a port request flag is set.

BLANK

Section 3
INSTALLATION

This section describes the step-by-step procedure for installation of the SC750/B Disk Controller in a VAX-11/750 system. The following list is an outline of the procedure. Each step corresponds to a second level heading in this section (i.e., item one, Inspect the SC750, is covered in paragraph 3.1).

All of the steps in the procedure outlined below apply to all installations except steps four and five (paragraphs 3.4 and 3.5). If there is already a DEC RH750 Massbus Adaptor on the system, perform step four and skip step five. If there is not an RH750 installed in the system, skip step four and perform step five.

Emulex recommends that Section 3 be read in its entirety before installation is begun.

1. Inspect the SC750.
2. Prepare the disk drives.
3. Prepare the VAX-11/750.
4. Remove and reinstall the RH750.
5. Install the Massbus Boot ROM.
6. Configure the SC750.
7. Install the SC750.
8. Route the drive I/O cables.
9. Install the cable paddle board.
10. Test the controller.

3.1 INSPECTION

Before unpacking the SC750, examine the packaging for any signs of damage. Notify the carrier if any damage is noted.

Make a visual inspection of the board after unpacking. Check specifically for bent or broken connector pins, damaged components or any other evidence of physical damage. Examine the PROMs to insure that they are firmly and completely seated in their sockets.

3.2 DISK DRIVE PREPARATION

3.2.1 Drive Placement

Uncrate and install the disk drives according to the manufacturer's instructions. Position and level the disk drives in their final places before beginning the installation of the SC750. This allows the I/O cable routing and length to be accurately judged. Place the drives side by side to make installation of the daisy-chained A Cable simpler.

3.2.2 Local/Remote

The LOCAL/REMOTE switch controls whether the drive can be powered up from the drive (local) or the controller (remote). Place the switch in the REMOTE position. With the VAX-11/750 powered down, press the START switch on the front panel of each of the drives (the START LED will light, but the drive will not spin up and become ready). When the VAX is powered up, the drives will spin up sequentially. This prevents the heavy current draw that would be caused if all of the drives were powered up at once. When in the remote mode the drives will power down when the VAX is powered down. While the VAX is powered on, the drives may be powered up and down individually (to change disk media, for example) using the drive START switch.

3.2.3 Sectoring

When using drives that allow the emulation to produce a one-to-one correspondence between the physical and logical (that is, emulated) recording heads, the drives are typically configured for 32 sectors per track.

When the physical drive has a different number of heads than the emulated RM drive, there is no one-to-one correspondence between the physical and logical heads. To accomplish this the controller operates in a mapped track and cylinder mode. When operating in this mode the drive is configured for one extra sector so that there is additional time at the end of each track to do the mapping.

The disk drives must be hard sectored as indicated in the SECTS column of Table A-1.

Because the procedure for entering the sector numbers differs from drive to drive, consult the drive manufacturer's installation manual for instructions.

NOTE: See paragraph A.2.3 for information regarding the sectoring of CDC and the Fujitsu 2351A models.

3.2.4 Address Selection

An address from 0 to 3 must be selected for each drive. Be careful that no two drives are assigned the same number. CDC drive addresses are selected by means of an ID plug. Drives by other manufacturers have their addresses selected by switches on one of the logic cards. Consult the particular drive manual for the exact procedure.

3.2.5 Sector and Index Modifications

The SC750 is designed to receive the sector and index signals from each drive on the B cable (see paragraph 3.6.4). Depending on the disk drive, the index and sector pulse signals may be carried on the A instead of the B cable. However, in most cases they are easily moved to the B cable by minor rewiring of the drive backplane, or this configuration may be ordered from the factory.

The procedure for moving the sector and index signals from the A to the B cables for several of the more common drives is described in Appendix B. If the procedure for the drive in question is not covered there, it is generally described in the drive manual.

NOTE: To prevent significant performance degradation when using more than one drive, Emulex strongly recommends modifying the drive to place the sector and index signals on the B cable if the drive is not delivered in that configuration.

3.2.6 Sectoring the 2351A Fujitsu for the SC750/B

The setting of the number of sectors for the 2351A Fujitsu (Eagle) will be dependent upon the type of Emulex SC750/B firmware the user has. Users with the /B1 firmware must configure the Eagle for 44 hard sectors. Those with /B3 firmware must configure the Eagle for 48 sectors. This 48 sector configuration supports an additional 40 Mb of capacity. See Table A-2 for the list of configurations supported by the SC750/B. Note that in Table A-2 configurations for the 2351A Fujitsu (key 470) are listed as being configured for 44/48 sectors. Those configurations are supported at 44 sectors per track by the /B1 firmware and 48 sectors per track by the /B3 firmware.

NOTE: See paragraph A.2.3 for more information concerning the sectoring of the 2351A Fujitsu.

3.3 SYSTEM PREPARATION

3.3.1 Powering Down the System

Power down the system and switch OFF the main AC breaker at the rear of the cabinet (the AC power light will remain lit). Open the front door of the CPU cabinet and remove the card rack cover. Open the rear door of the cabinet and remove the backplane cover.

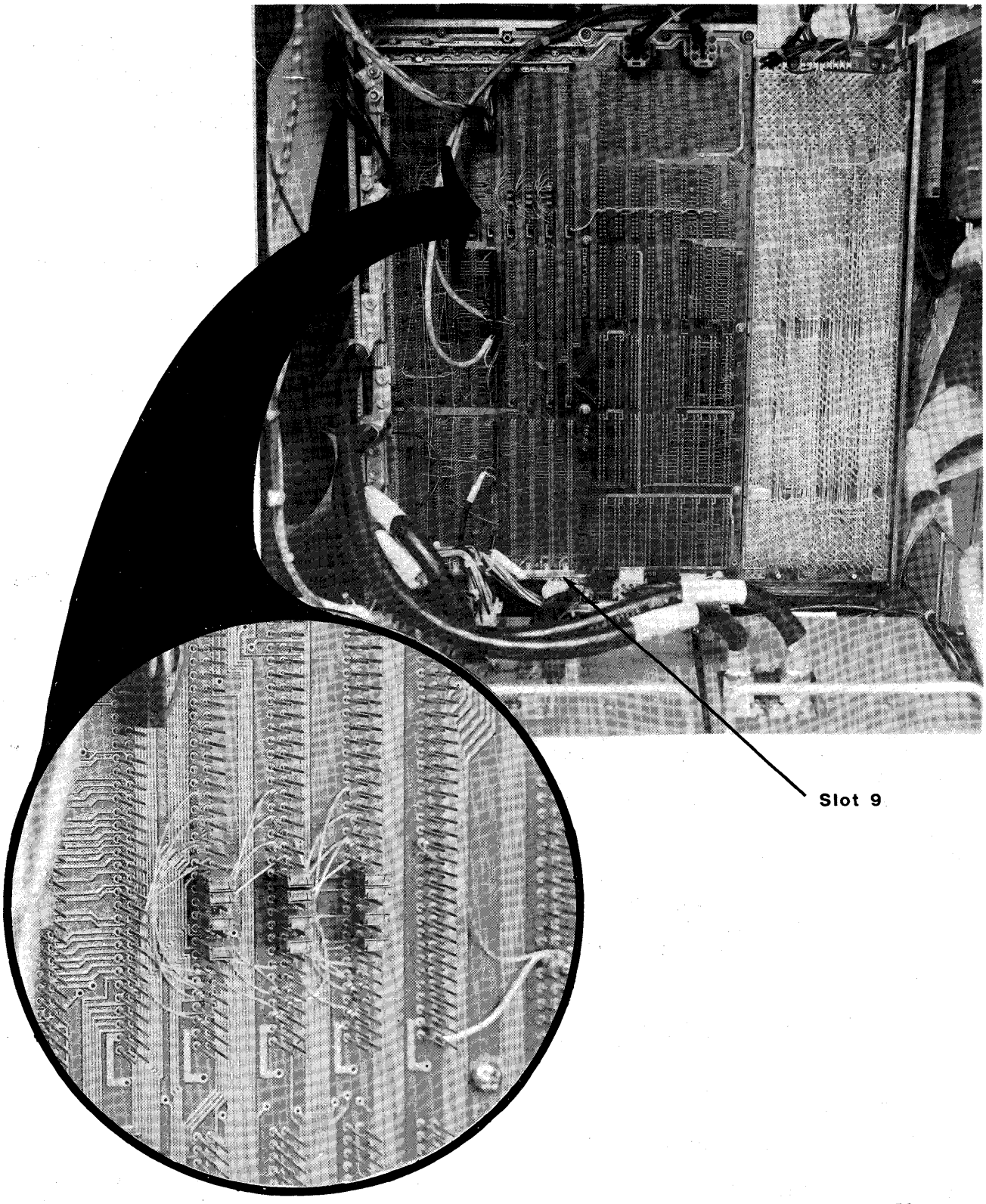


Figure 3-1. Backplane with Bus Grant Jumpers

3.3.2 Removing the Bus Grant Jumpers

Locate the bus grant jumpers for the option slots (7, 8 and 9) on the backplane. See Figure 3-1. Remove the jumpers for the slots in which SC750 controllers will be installed. If a controller is already present in one of the options slots, the jumpers for that slot will have already been removed. Save the jumpers.

3.4 RH750 RECONFIGURATION

If a DEC RH750 MASSBUS Adaptor is present on the system and located in slot nine, Emulex recommends moving the RH750 to slot eight or seven. CMI bus addressing is not related to the slot in which the controller is placed so the RH750 can remain the boot device.

If the RH750 is not located in slot nine, it will not be necessary to move it. However, it may be necessary to select a different bus arbitration level if the FCO described below has not been applied.

Before removing the RH750 from the card rack, determine whether or not FCO #RH750-R0001 has been installed. If the FCO has been installed, the RH750 module's new revision number, A1, will be indicated by brady markers on the module handle (outside edge of the PCBA). Also check the ECO/FCO section of the Site Management Guide for your VAX to see if the FCO has been entered. This FCO cures the RH750's tendency to seize and hold the CMI bus by asserting its arbitration signal for extended periods. If not cured, this problem causes other MASSBUS devices with lower arbitration levels to generate data late errors. EMULEX highly recommends that this FCO be applied before a second MASSBUS device (such as the SC750) is installed in the system.

If it is not possible for the FCO to be applied before the installation of the EMULEX SC750, then it will be necessary to reconfigure the RH750 to a CMI arbitration level lower than that of the SC750 to prevent data-lates. See paragraph 3.4.2, below.

Regardless of whether or not the FCO has been applied to the RH750, each MASSBUS device must be assigned a unique arbitration level. See paragraph 3.6.2 for instructions on setting the SC750's arbitration level.

3.4.1 RH750 Removal

Remove the RH750 from slot nine. If FCO #RH750-R0001 (see above) has not yet been applied to the RH750 module, do so now. Insert the RH750 in either slot eight or seven.

3.4.2 RH750 Backplane Reconfiguration

For all of the following, refer to Figure 3-2.

After noting down the arrangement of the jumpers, remove the SLOW CMI EN H, device address (MBA select) and CMI request level (CMI

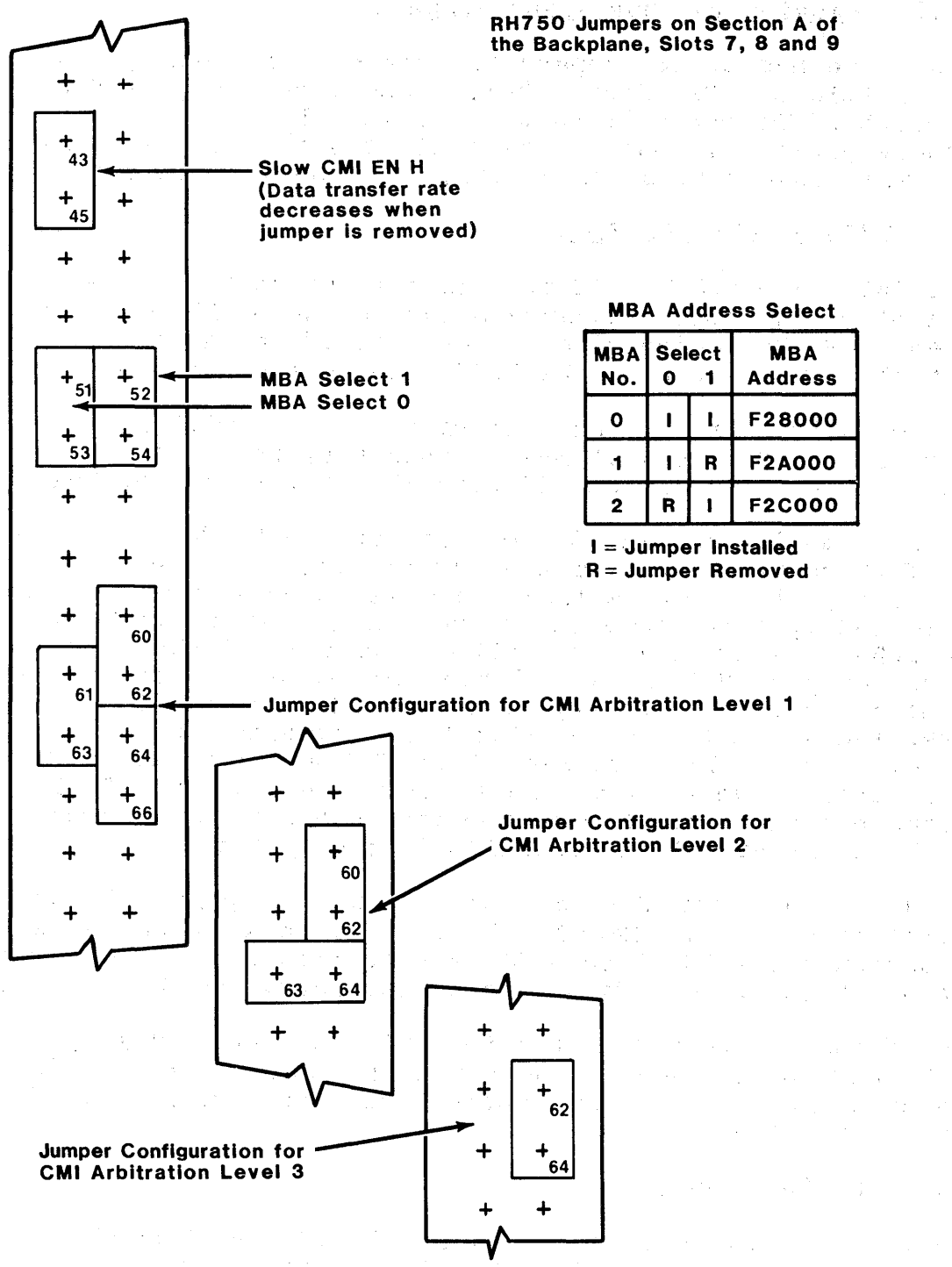


Figure 3-2 RH750 Backplane Jumpers

ARB) jumpers from the slot nine area of the backplane. Place the SLOW CMI EN H jumper in the same relative location on the backplane of the new RH750 slot.

If the RH750 is to remain the boot device (address F28000), place both MBA select jumpers in the same relative location on the new slot. If the EMULEX SC750 is to become the new boot device, select either F2A000 or F2C000 as addresses.

Using Figure 3-2, determine the arbitration level assigned to the original RH750 installation. If FCO #RH750-R0001 has been installed and the RH750 is to remain the boot device, place the CMI ARB jumper(s) in the same relative location on the new slot. If the FCO has not been applied and arbitration level 3 had been assigned, select a lower CMI ARB level (2 or 1). This must be done whether or not the RH750 is being moved. The Bus Grant jumpers removed in paragraph 3.3.2 may be used to select the lower CMI ARB level.

Remove the three MASSBUS plugs from sections B and C of the backplane and set them on top of the card rack. When the A and B cables for the SC750 have been installed on the paddle board, plug the three MASSBUS plugs into the same relative location of the new RH750 backplane slot.

3.5 BOOTSTRAP ROM INSTALLATION

The VAX-11/750 bootstrap ROMs are located on sockets on the memory controller module. Table 3-1 shows the DEC factory placement of the bootstrap ROMs.

Table 3-1
DEC Placement of the Bootstrap ROMs

Boot Switch Position	Device Type
A	TU58
B	RL02
C	RK07
D	EMPTY

When installing a SC750 disk system, you need to install a MASSBUS disk bootstrap ROM (EMULEX #497) on the memory controller module. The ROM is shipped in a spare socket on the SC750 PCBA (U169). Carefully remove the ROM from the SC750 and plug it into the memory module. You may plug this MASSBUS disk ROM in the location that corresponds to switch position D, or you can rearrange the bootstrap ROMs to correspond to any boot switch position configuration. The only requirement is that the TU58 bootstrap ROM remain on the memory controller module, preferably in either socket position A or D (Figure 3-3). Note that the physical location of the bootstrap ROM sockets on older L0011 memory boards may be different.

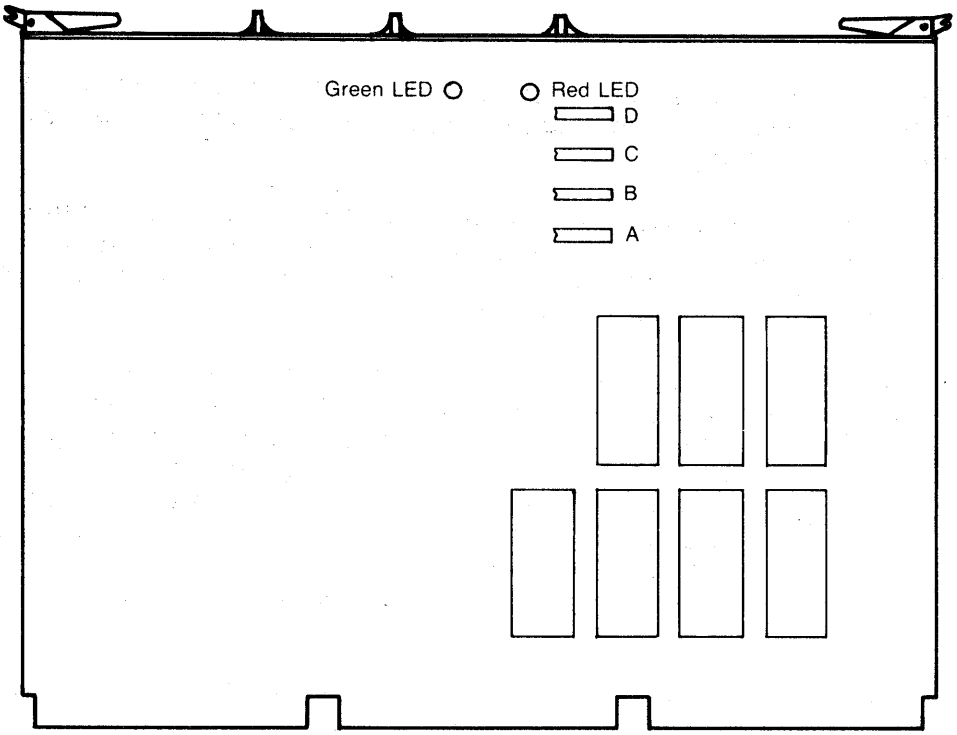
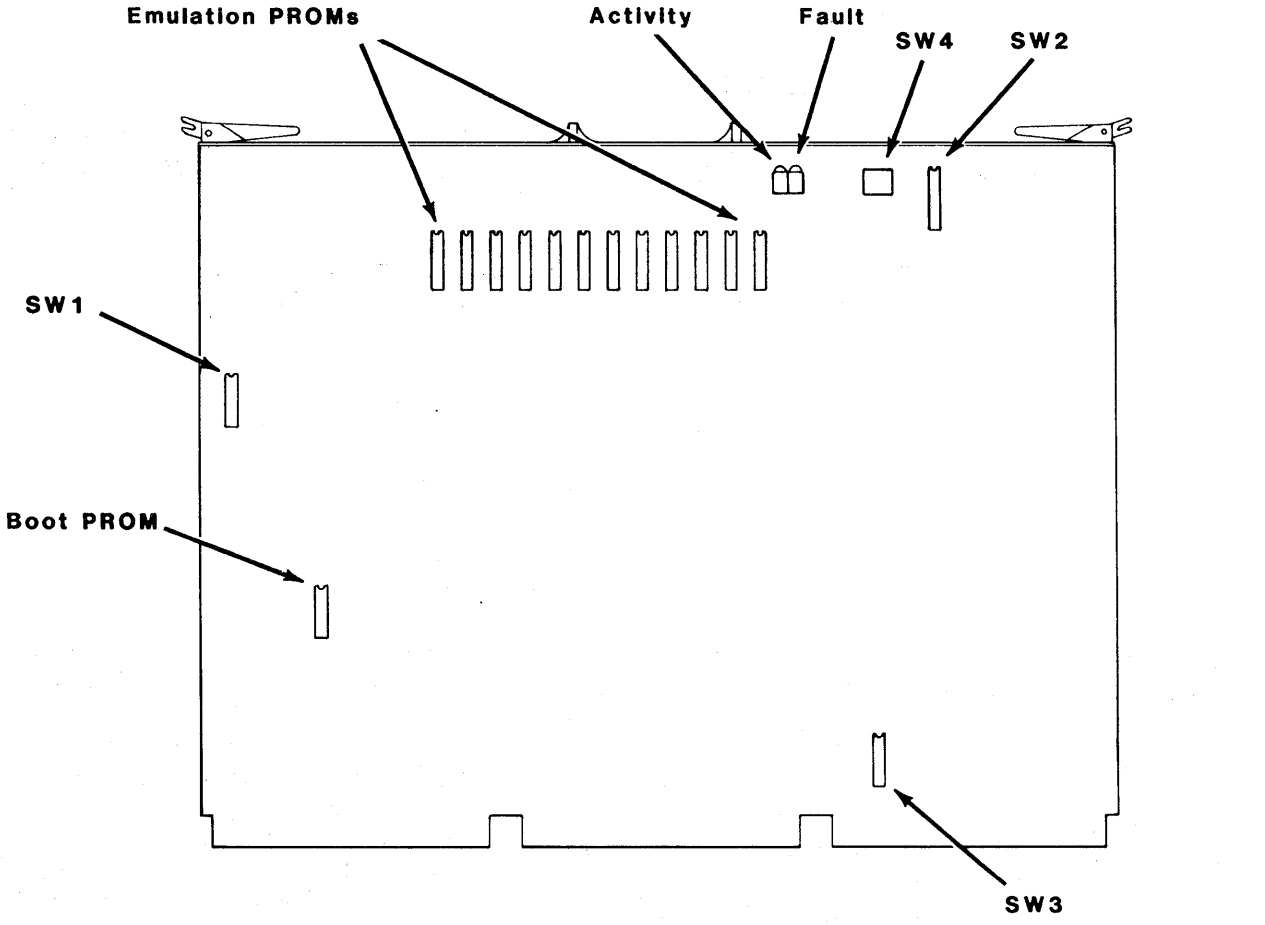


Figure 3-3 L0016 Memory Controller SC7501-0358



SC7501-0061

Figure 3-4 SC750 Controller Assembly

3.6 CONTROLLER SETUP

The selection of the controller's base address, arbitration level and drive configuration are made by SW1, SW2 and SW3 (see Figure 3-4). Neither the address or the arbitration level is selected using backplane jumpers. These setups must be made on the controller board before inserting it into the chassis.

3.6.1 MBA Number Selection

The MBA number selects the controller CMI address and the interrupt vector address. SW3-7 and SW3-8 are used for this purpose. If the drive to be used to boot the system on power-up is on the controller, then the controller must use the address F28000. This selection has no effect on the arbitration level which is set as described in paragraph 3.6.2. Selection is made as follows:

SW3-7	SW3-8	Address	Vector	Device No.
O	O	F28000	150	RH0
O	C	F2A000	154	RH1
C	O	F2C000	158	RH2

3.6.2 Arbitration Level Selection

The arbitration level (bus priority level) is selected by switch SW3 as shown below. Each MASSBUS device must be assigned a unique arbitration level. If there is an RH750 on the system and you have not already inspected its backplane jumpers to determine its arbitration level, do so now (see Figure 3-2). If the DEC FCO has been applied, select either of the levels that is not being used. If the FCO has not been applied, select a higher level (see 3.4).

	SW3-					
Level	2	3	4	5	6	Rank
3	C	O	O	O	O	Highest MBA level
2	O	C	O	C	O	
1	O	O	C	C	C	Lowest MBA level

3.6.3 Drive Configuration Selection

The phrase "drive configuration selection" describes the process that is used to select the logical disk drives that will be emulated by the SC750 using a given set of physical disk drives. That is, you have a particular set of physical disk drives. Using those disk drives and the SC750, you wish to emulate a specific type and arrangement of DEC subsystems. (The emulated subsystem is referred to as a logical disk drive.) Setting SW2-1 through SW2-6 on the controller allows you to select the logical disk drive configuration (limited by the physical disk drives available).

For ease of manual maintenance, the configuration table and instructions for using it are both contained in Appendix A.

3.6.4 Index and Sector Pulse Selection

The SC750 controller is designed to have the Index and Sector signals on the B cable from each physical drive. The signals are necessary for proper operation of the sector counters associated with each drive. The RM emulation requires an updated sector counter which can be read by the VAX-11/750. Failure to have a valid sector counter may cause incorrect operation of the rotational position sensing software.

It is possible to operate with the index and sector signals on the A cable by placing switch SW1-8 (located on the SC750) in the ON position. This feature is useful for initial evaluation of the controller with a disk drive that only provides the sector and index signals on the A cable. However, when operating in this manner there is a substantial loss of capabilities and performance including: the Search command operates as a Seek; the sector counter in RMLA will be incorrect; and each transfer must wait for an index pulse to sync-up the sector counter. Also, some of the lower level diagnostics will produce some errors. Emulex strongly recommends modifying the drive to place the sector and index signals on the B cable if the drive is not delivered in that configuration.

3.6.5 Option Switches

There are a number of SC750 options that can be selected by the user.

3.6.5.1 Dual Access Mode

In order to provide compatibility with VMS when it is configured for dual access, the dual access mode is provided (SW4-4 ON). This mode should only be selected when the disk drive has dual ports and is configured for dual port operation.

See paragraph 2.6.7 for programming information.

3.6.5.2 Dual Port Mode

Dual port mode is selected by setting SW1-6 ON. This option should only be selected when used in conjunction with a properly written dual port driver. See paragraph 2.6. In addition, this mode should only be selected when the disk drive has dual ports and is configured for dual port operation.

3.7 SC750 INSTALLATION

3.7.1 MBA Slot Selection

The SC750 controller may be used in slot seven, eight or nine of the VAX-11/750. Any of the slots not already in use may be used, but for ease of paddle board installation use slot nine.

3.7.2 Mounting the Controller

The controller board should be plugged into the VAX-11/750 backplane with components oriented in the same direction as the CPU and other modules. Always insert and remove the board with the computer power OFF to avoid possible damage to the circuitry. Be sure that the board is properly positioned in the throat of the connector before attempting to seat the board by means of the extractor handles.

3.8 CABLING

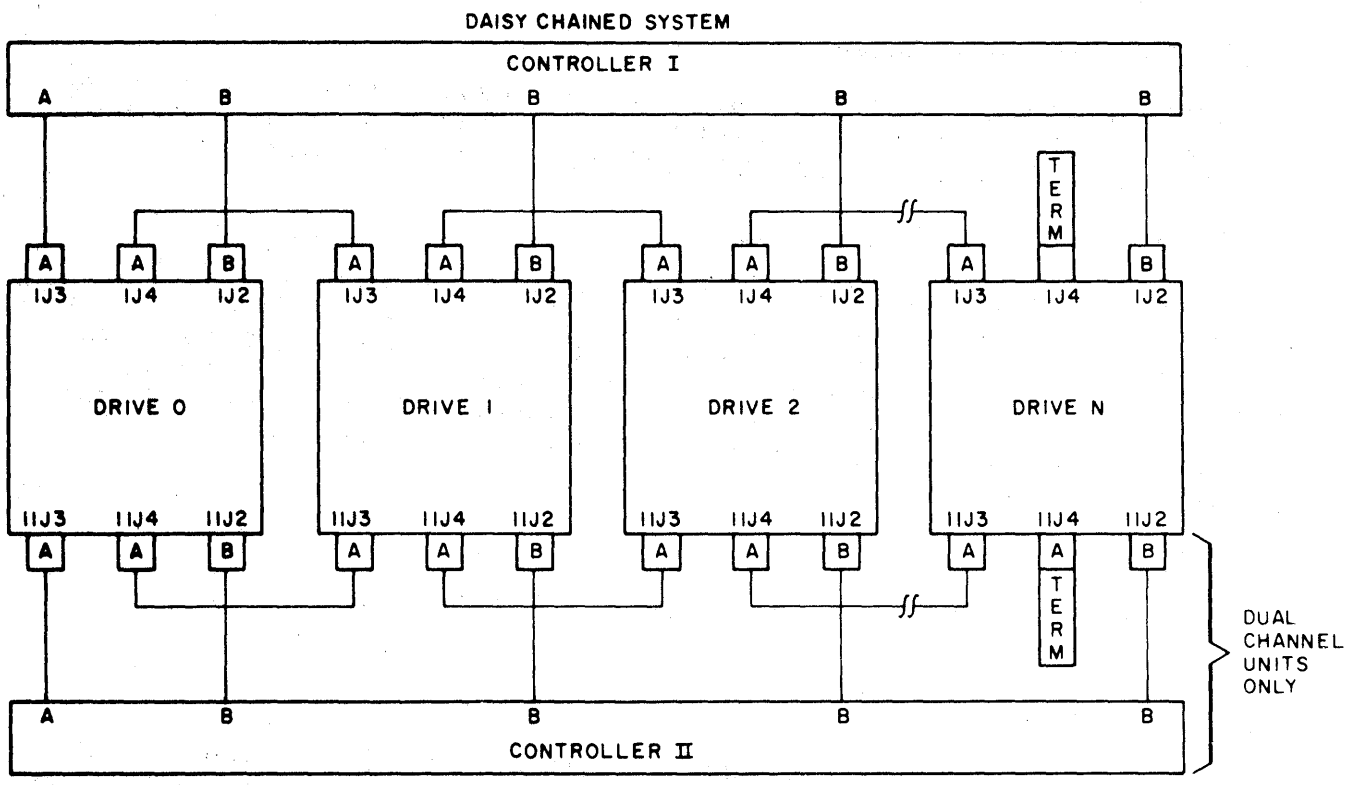
The subsystem cabling of the drives and controller is shown in Figure 3-5.

3.8.1 A Cable

Route the A cable from the drive nearest the CPU through the opening in the lower right-hand corner (below the I/O panel) of the cabinet back. From the opening in the cabinet run the cable up and over the cable rack into the space behind the backplane. The paddle board end of the 60-wire A cable is divided into two connectors. They should be plugged into their connectors on the paddle board before the paddle board is installed on the backplane. Align the plugs and jacks using the triangles molded into both connectors.

If more than one drive is used, the A cable is daisy-chained from the first drive to the other drives. The last drive on the A cable must have a terminator installed. This part is available from the drive manufacturer. The terminator is generally plugged into one of two A cable connectors on the drive. In some cases, a ground wire emerging from the terminator assembly will have to be connected to the drive to provide a ground return for the resistors in the terminator. Pin one of the drive connector is on the left. Pin one of the cable connector has a notch on the connector body to identify it.

NOTE: The connector is not keyed and can be physically reversed in the header. No damage should result, but the system will not operate.



NOTES:

1. MAXIMUM INDIVIDUAL A CABLE LENGTHS = 100 FEET
2. MAXIMUM INDIVIDUAL B CABLE LENGTHS = 50 FEET

SC7501-0000

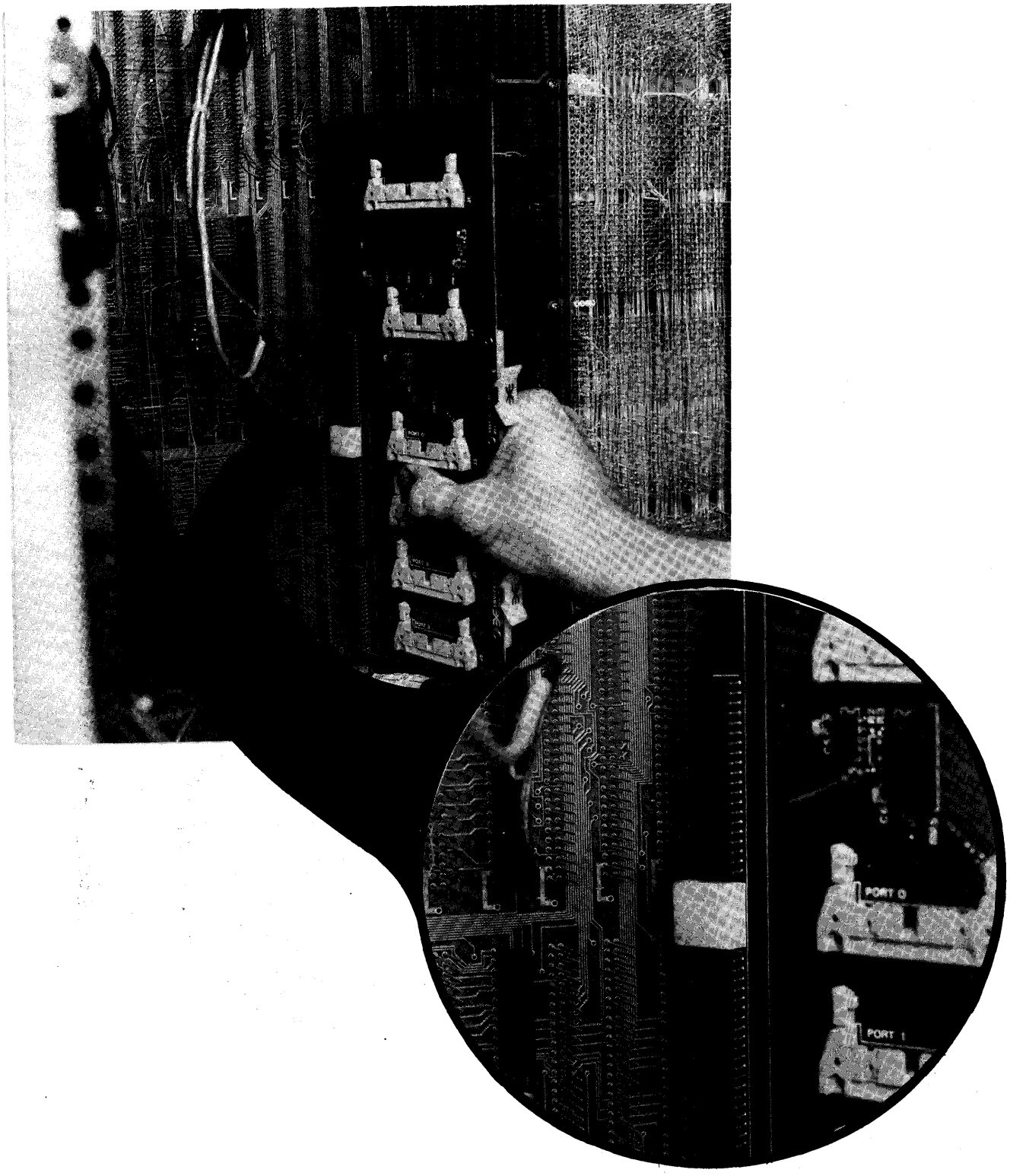
Figure 3-5 Cabling Diagram

3.8.2 B Cable

Route a B cable from each drive to the CPU through the opening in the lower right-hand corner (below the I/O panel) of the cabinet. From the opening in the cabinet run the cables up and over the cable rack into the space behind the backplane. The 26-wire B cables should be plugged into their connectors on the paddle board before the paddle board is installed on the backplane. It makes no difference which B port connection is used by a drive. Align the plugs and jacks using the triangles molded into both connectors.

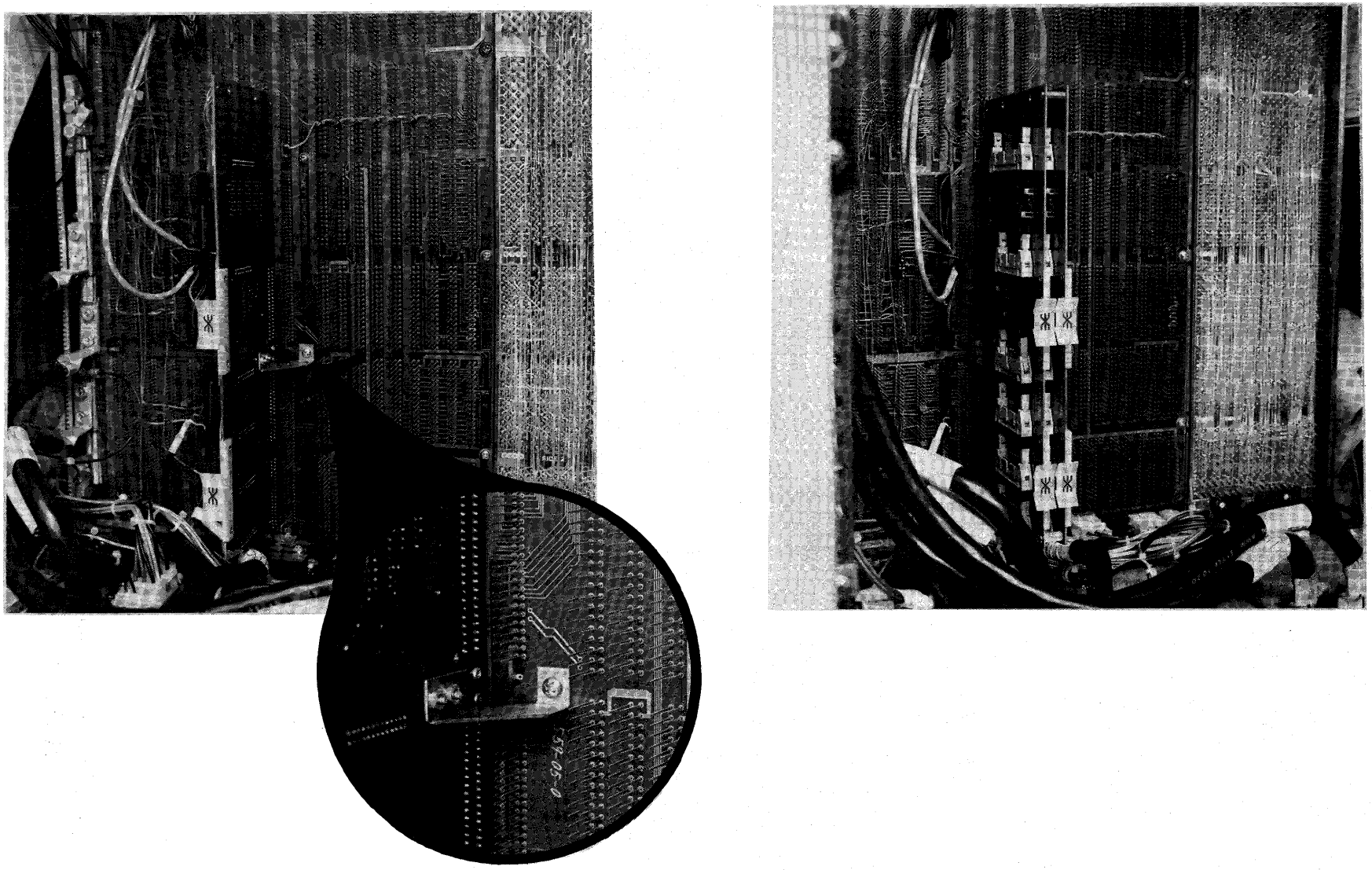
At the drive end of the B cable, pin one of the cable connector has a notch on the connector body to identify it. Pin one of the drive connector is on the left. No external terminators are used with the B cable.

NOTE: Observe the same caution on connector reversal given in paragraph 3.8.1.



SC7501-0062

Figure 3-6. Paddle Board Installation
(stiffener removed for clarity)



SC7501-0063

Figure 3-7. Paddle Board Mounting

3.8.3 Grounding

For proper operation of the disk subsystem, it is very important that the disk drives have a good ground connection to the logic ground of the computer. The ground connection should be a 1/4 inch braid (preferably insulated) or AWG No. 10 wire or larger. The grounding wire may daisy-chain between drives. If the drive has a switch or jumper which connects the logical signal ground to the cabinet ground (DC ground to AC ground), this connection should be removed once the drive is put on-line with the controller. It can be connected for performing local off-line maintenance on the drive.

NOTE: Failure to observe proper grounding methods will generally result in marginal operation with random error conditions. In particular, care must be taken when Fujitsu Eagles and CDC drives are mixed on the same daisy chain string.

The procedures below should be followed on any system which mixes Eagles and CDC drives on the same daisy chain:

1. Disable Tags 4 and 5 on the Eagle as described on pages 3-7 of the Fusjitsu manual.

2. Use one of the following three grounding procedures:

   A. Install CDC drives with chassis (AC) and signal (DC) grounds connected together at the drive. Refer to the system grounding section of the CDC drive manual for details.

      Install grounding strap SG (DC) to FG1 (AC) on the Eagle.

      Install separate ground straps from each drive to the common system ground on the CPU.

   B. Install FCC-approved drive cables and attach all cable shields to the CPU and drive chassis grounds.

   C. Separate the chassis (AC) and signal (DC) grounds on each drive.

      Install FCC-approved cables and attach the shield grounds to the chassis (AC) ground of each drive. Daisy chain the signal

      (DC) ground of each drive to the signal (DC) ground of the controller.

3. If the cable from the controller to the **first** drive is less than 25 feet, place the Eagles first in the daisy chain. If the cable from the controller to the **first** drive is more than 25 feet, place the Eagles last on the

daisy chain, closest to the terminator. If the **total** daisy chain length is more than 50 feet, use FCC approved cables whenever possible.

3.9 PADDLE BOARD INSTALLATION

Remove the phillips-head screw located to the right of backplane slot 10 between sections B and C.

Mount the support bracket (Emulex kit #SC7513101) on the paddle board and plug all of the A and B cables into the paddle board before plugging the board on to the backplane.

The paddle board's three connectors are inserted onto the backplane pins (sections B and C) of the slot containing the controller. The six A and B cable connectors will be on the left side. Carefully position the paddle board so that the white guide between the top and middle board connectors is between the bottom two pins of section B and the top two pins of section C. At the same time, rest the board against the righthand pins of the backplane connectors. When it looks and feels as if the pins are going to engage the connectors of the paddle boards, it should be pushed forward until it bottoms on the backplane. See Figure 3-6.

When the paddle board is in place, replace the screw removed from the backplane through the support bracket. See Figure 3-7.

Any subsequent paddle boards (for additional controllers) are attached to the first paddle boards with standoffs (Emulex kit #SC7513102). See Figure 3-7.

3.10 TESTING

3.10.1 Self-Test

When power is applied to the CPU, the controller will automatically execute a built-in self-test. If the self-test has been executed successfully, the FAULT LED on the top edge of the controller board will be OFF or flashing. The FAULT LED flashes when the controller cannot properly address at least one drive after successfully executing its self-test. This will occur if the A and B cables are not properly plugged in, a drive is powered-up without a code plug, or two drives have an identical code plug. If the FAULT LED is ON steadily the controller did not pass its self-test and the controller cannot be addressed from the CPU. The self-test will fail if the paddle board is not properly installed.

3.10.2 Register Examination

Before formatting the disk or running diagnostics, a quick check should be made to ensure that the controller registers can be read from the CPU console. Power up the CPU with the POWER ON ACTION switch in the HALT position. When the CPU has completed its self-test, a >>> prompt will be issued at the consol. This indicates that the consol is in the consol I/O mode. Check the FAULT indicator on the SC750. If it is not ON steadily, examine the controller's first MBA register. For RH0 this can be done by typing:

```
>>> E/L/P F28004<cr>
```

Use F2A004 for RH1 or F2C004 for RH2. If the controller can not be accessed at the base address the console will return "?", otherwise it will return 00000000 which is the contents of the first MBA register.

3.10.3 Hardware Formatting the Disk

The controller has the means to format the disk by writing headers and zero data in all sectors of the disk. This format does not verify the data or headers nor does it write a Bad Sector File on the last track of the last cylinder.

The consol should already be in the consol I/O mode as described in paragraph 3.10.2 (indicated by the >>> prompt). If it is not, type CNTL P to place the consol in that mode.

In determining the drive's register addresses remember that the base address for the first drive on RH0 is F28400, on RH1 it is F2A400 and on RH2 it is F2C400. Add 80 for each drive after the first.

If the drive is on-line and there are no drive errors, the formatting is carried out as follows (the addresses in the example are those of drive zero on RH0, <cr> indicates a carriage return, place spaces as indicated):

1. Deposit 0013 (Pack Acknowledge command) in RMCS1 (base address):

   ```
   >>> D/L/P F28400 0013<cr>
   ```

2. Deposit FFFF (enables optional Format command) in RMHR (base address + 2C):

   ```
   >>> D/L/P F2842C FFFF<cr>
   ```

3. Deposit 003F (Format command) in RMCS1 (base address):

```
>>> D/L/P F28400 003F<cr>
```

The ACTIVITY indicator will flash as long as the formatting is underway.

4. When the activity light stops flashing, examine RMDS (base + 4) to see if ERR (bit 14) is set indicating an error:

```
>>> E/L/P F28404<cr>
```

If there has been no error, the register will contain 15C0. If there is an error resulting from the format operation, RMER1 and RMER2 should be examined to determine the cause of the error, and RMDA and RMDC should be examined to see how far the formatting progressed.

The time to format the disk is as follows: RM03 - 1.8 min., RM05 - 5.5 min. and RM80 - 4.5 min.

3.10.4 DEC Diagnostics

The controller will execute the DEC diagnostics as indicated below if the drive is a standard RM03, RM05 or RM80 size. Consult Appendix C for more detailed information on operation of the DEC disk diagnostics listed below which are applicable to the SC750.

ECCAA - VAX-11/750 RH750 Diagnostic

This program tests only the RH750 portion of the SC750 controller. Most of the test is executed with the controller in diagnostic mode which allows for simulation of an attached Massbus. Since the SC750 has no Massbus, it does not simulate one and therefore only tests 1-3, 5-6 and 11 run without errors. Test 11 requires drive 0 to be on line.

EVRDA - RM03/5 RM80 Diskless Diagnostic

This program tests the drive portion of the controller's logic. No data transfers are performed. A portion of this program uses the diagnostic mode of the DEC drives. Since the diagnostic mode is not implemented in the SC750 controller only tests 1-23 will run without errors.

EVRAC - Disk Formatter

This program will format RM03 and RM05 type drives. A different format program is used for RM80's.

EVRDB - RM03/5 Functional

This program does simple operations, including data transfers, with an attached RM03 or RM05 type drive.

EVRGA - RM80 Formatter

This program does the formatting of the RM80 type drives.

EVRGB - RM80 Functional Diagnostic

This program does simple operations, including data transfers, with an attached RM80 type drive.

EVRAA - VAX RP/RK/RM/RX/TU58 Reliability

This program is a general purpose data reliability test program which will handle the RM drives.

BLANK

There are 32 device registers for each of the drives, plus seven Massbus Adaptor (MBA) registers in the SC750/B controller. The first MBA register is not used in the SC750 and reads back as zero. The registers are used to interface the controller to the drives and the CPU. The registers are loaded and/or read under program control in order to initiate drive commands, set-up for DMA data transfers, and monitor status and error conditions. The MBA registers and the 32 drive registers are read and written as long words. The drive registers return the upper half of MBASR in bits <31:16> when read.

In addition there are 256 map registers which control the virtual to physical mapping for DMA transfers.

This section shows the format of each of the registers and explains the use and the meaning of each of the bits. The addresses for the registers are for unit 0 and the first MBA, and are given in hexadecimal. Add 2000 for the second MBA and 4000 for the third MBA. Add 80 to the drive register address for unit 1, 100 for unit 2, etc.

4.1 MBA CONTROL REGISTER (MBACR) F28004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	IBC	MMM	IE	ABT	INIT

This register provides five control bits for the MBA functions of the controller. All bits are cleared by INIT.

IBC Mode (IBC) - Bit 04

When the Ignore Byte Count bit is set a data transfer is not terminated by the byte counter overflow. If IE is set then an interrupt is generated each time the byte counter overflows. This bit cannot be set while a data transfer is in progress.

MBA Maintenance Mode (MMM) - Bit 03

Setting this bit puts the controller in the maintenance mode, which will allow the diagnostic programmer to exercise and examine the controller registers. The controller can not be put in maintenance mode while a data transfer is in progress.

Interrupt Enable (IE) - Bit 02

When this bit is set the controller can interrupt the CPU when certain conditions occur. Cleared by writing a zero or by INIT.

Abort (ABT) - Bit 01

Setting this bit will initiate the data transfer abort sequence which will stop the data transfer and interrupt the CPU if the IE bit is set.

Initialize (INIT) - Bit 00

Setting this bit will clear the controller including any pending commands, abort any data transfer, and clear registers as well as this bit.

4.2 MBA STATUS REGISTER (MBASR) F28008

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DTB	0	CRD	0	0	0	0	0	0	0	0	0	PGE	NED	MCPE	ATTN

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	DTC	DTA	DLT	WCU	WCL	MXE	EXC	0	0	IM	ERS	0	NRS	0

Data Transfer Busy (DTB) - Bit 31

This bit is set when a data transfer command is received. It is cleared when the data transfer is terminated normally or when it is aborted.

Corrected Read Data (CRD) - Bit 29

This bit is set when the data received from memory has been corrected. It is cleared by writing a one or by INIT. It is also cleared by subsequent receipt of a valid data transfer command.

Programming Error (PGE) - Bit 19

This bit is set when one or more of the following conditions exists:

1. Program tries to initiate a data transfer when the controller is currently performing one,

2. Program tries to load MBAVAR, MBABCR or map registers when the controller is currently performing a data transfer operation and IBC = 0, or

3. Program tries to set Maintenace Mode or IBC mode during a data transfer.

This bit is cleared by writing a one to it, or by INIT. This bit is also cleared by subsequent receipt of a valid data transfer command. Setting this bit will cause an interrupt to the CPU if IE is set.

Nonexistent Drive (NED) - Bit 18

This bit is set when the program addresses the drive register of a drive which does not exist. The bit is cleared by writing a one or by INIT. Setting this bit will send zero drive data back to the CPU and interrupt the CPU if IE is set.

Massbus Control Bus Parity Error (MCPE) - Bit 17

This bit is set when NED is set.

Attention (ATTN) - Bit 16

This bit is asserted if any of the Attention bits in RMAS are asserted indicating that a drive requires attention. Asserting this bit will cause an interrupt to the CPU if IE is set.

Data Transfer Completed (DTC) - Bit 13

This bit is set when the data transfer is terminated either due to an error or normal completion. It is cleared by writing a one or by INIT. This bit is also cleared by subsequent receipt of a valid data transfer command. Setting this bit will cause an interrupt to the CPU if IE is set.

Data Transfer Aborted (DTA) - Bit 12

This bit is set when the data transfer is aborted for any reason. This bit is cleared by writing a one or by INIT. This bit is also cleared by subsequent receipt of a valid data transfer command. Setting this bit will cause an interrupt to the CPU if IE is set.

Data Late (DLT) - Bit 11

Set during a read if the buffer overflows. Set during a write or write check if the buffer underflows. This bit is cleared by writing a one or by INIT. It is also cleared by subsequent receipt of a valid data transfer command. Setting this bit will abort the data transfer operation.

Write Check Upper Error (WCU) - Bit 10

This bit is set when a compare error is detected in the upper byte while the controller is performing a write check operation. It is cleared by writing a one or by INIT. This bit is also cleared by subsequent receipt of a valid data transfer command. Setting this bit will abort the data transfer operation.

Write Check Lower Error (WCL) - Bit 09

This bit is set when a compare error is detected in the lower byte while the controller is performing a write check operation. It is cleared by writing a one or by INIT. This bit is also cleared by subsequent receipt of a valid data transfer command. Setting this bit will abort the data transfer operation.

Missed Transfer Error (MXE) - Bit 08

Set when an illegal command in the range 2D-3F is received. ILF in RMER1 will also be set. It is cleared by writing a one or by INIT. This bit is also cleared by subsequent receipt of receipt of a valid data transfer command. Setting this bit will abort the data transfer operation.

Exception (EXC) - Bit 07

The exception signal indicates an error condition during a data transfer between the controller and the drive. It is cleared by writing a one or by INIT. It is also cleared by subsequent receipt of a valid data transfer command. Setting this bit will abort the data transfer operation.

Invalid Map (IM) - Bit 04

Set when the valid bit of the next page frame number is zero and the byte counter is not zero. Cleared by writing a 1 to this bit or by INIT. The setting of this bit will cause the data transfer to be aborted.

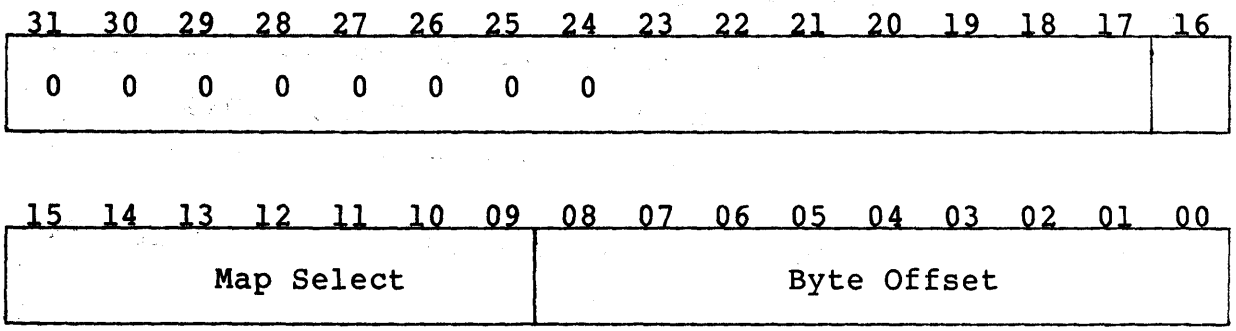
Error Confirmation (ERS) - Bit 03

Set when the MBA receives error confirmation for a read or write command. Cleared by writing a 1 to this bit or INIT. The setting of this bit will cause the data transfer to be aborted.

No Response Status (NRS) - Bit 01

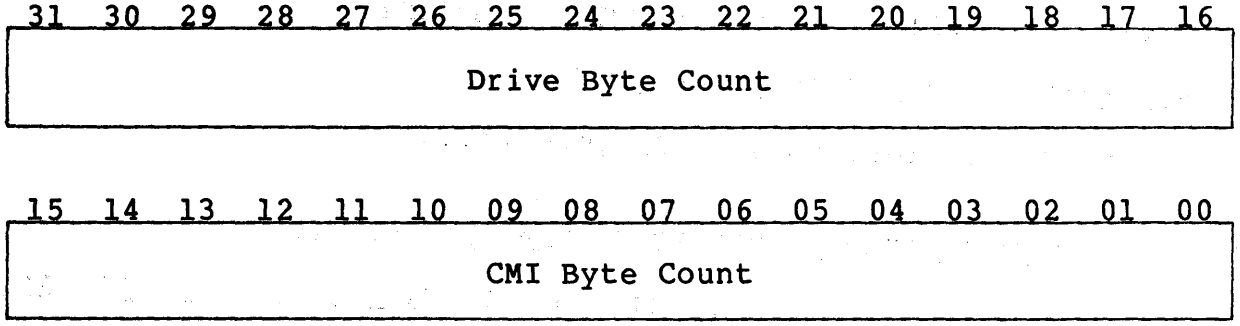
This bit is set when the controller receives no response from memory during a DMA operation. It indicates that the effective physical memory address was non-existent. This bit is cleared by writing a one or by INIT. This bit is also cleared by subsequent receipt of a valid data transfer command. Setting this bit will abort the data transfer operation.

4.3 MBA VIRTUAL ADDRESS REGISTER (MBAVAR) F2800C



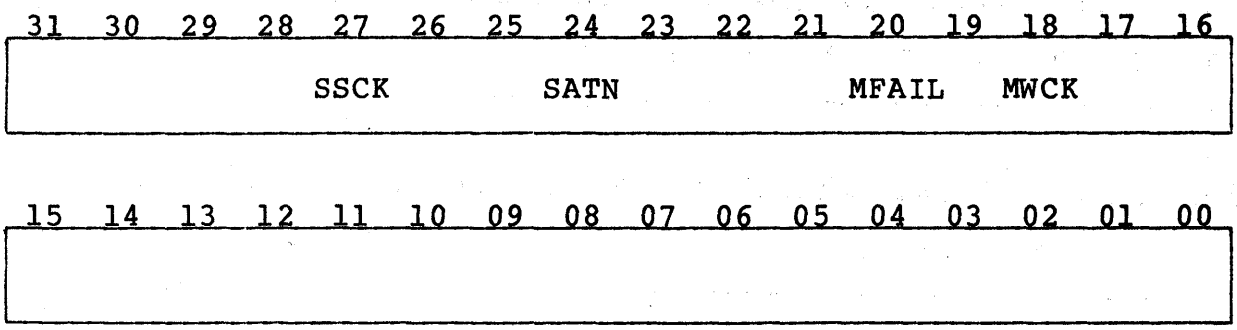
This 24-bit register contains the 17 bit virtual address for the data transfer. Bits <08:00> select the byte within the page and bits <16:09> select one of the 256 map registers. Bits <23:17> can be read or written but they have no function or effect. The 9-bit byte offset is concatinated with the 15-bit physical page address obtained from the addressed map register to form the 24-bit physical CMI address. The virtual address is incremented by four after every memory read or write and will not point to the next byte to be transferred if the transfer does not end on a longword boundary. Also, upon a write check error, the virtual address register will not point to the failing memory address due to the preloading of the data buffer. The virtual address of the bad data may be found by determining the number of bytes actually transferred by the drive and adding the difference to the initial virtual address.

4.4 MBA BYTE COUNT REGISTER (MBABCR) F28010



This register contains the byte count for the number of bytes transferred to or from the drive and the number of bytes transferred to or from memory. The two transfers stop when the byte counts reach zero. The program initially loads the two's complement of the number of bytes for the data transfer into bits <15:00> of this register. The controller then loads this value into bits <31:16>.

4.5 MBA DIAGNOSTIC REGISTER (MBADR) F28014



This register cannot be written into unless MMM in MBACR is set. Unless explicitly written into, this register will read 'BF' for data. Cleared to a 'BF' whenever Init is set. Only bits <31:21> are read/write. All others are read-only. Only the bits described are emulated.

Simulated SCLK (SSCK) - Bit 27

Setting this bit sets MWCK (Bit 18).

Simulated ATTN (SATN) - Bit 24

Setting this bit sets ATTN in MBASR.

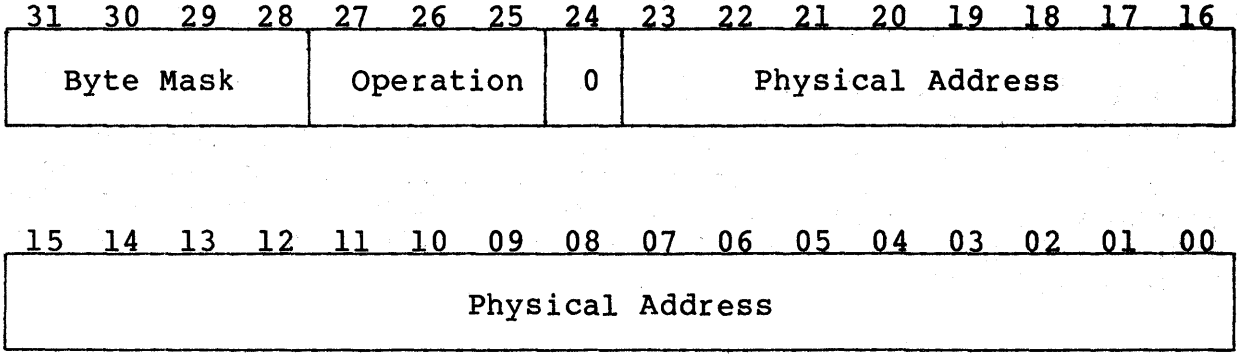
Massbus Fail (MFAIL) - Bit 20

This bit is a reflection of the MMM bit in MBACR.

Maint. Write Clock (MWCK) - Bit 18

This bit is a reflection of SSCK (Bit 27)

4.6 MBA COMMAND ADDRESS REGISTER (MBACAR) F2801C



This register is read-only and valid only when DT Busy (bit 31 of the MBA Status Register) is set. This register contains the byte mask, operation code and physical address of the last DMA operation.

4.7 CONTROL/STATUS REGISTER 1 (RMCS1) F28400

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	DVA	0	0	0	0	0	F4	F3	F2	F1	F0	GO

The RMCS1 register can be read or written by program control, and is used to store the current disk command function code. Setting the GO bit will cause the controller to recognize the function code in the register and initiate the operation for the corresponding drive. The actual start of execution of the command does not begin when the function code is loaded into the control register but commences when the controller has finished any previous operation and polls through the drive RMCS1's in search of a command needing initiation.

Drive Available (DVA) - Bit 11

This read-only bit is set when the drive is seized by the controller. When not in dual port mode, the drive is seized as long as it is powered-up.

Function Code (F4-F0) - Bits <05:01>

F4-F0 and the GO bit make up the function (command) code which determines the action to be performed by the controller and drive as shown below:

01	No Operation	29	Write Check Data
05	Seek Command	2B	Write Check Header and Data
07	Recalibrate	31	Write Data
09	Drive Clear	33	Write Header and Data
0B	Release	39	Read Data
0D	Offset Command	3B	Read Header and Data
0F	Return to Centerline	3F	Format (Optional)
11	Read-in Preset		
13	Pack Acknowledge		
19	Search Command		

GO (GO) - Bit 00

The GO bit must be set to cause the controller to respond to a command. The GO bit is reset after command termination.

4.8 DRIVE STATUS REGISTER (RMDS) F28404

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	PIP	MOL	WRL	LST	PGM	DPR	DRY	VV	0	0	0	0	0	OFM

This register contains various status indicators for the addressed drive. The register is a read-only register.

Attention Active (ATA) - Bit 15

An attention condition will set the ATA bit in this register and the Attention Summary register (RMAS). It is cleared by INIT, controller clear, loading a command with the GO bit set or loading a one bit in RMAS register corresponding to the drive's unit number. The last method of clearing the ATA bit will not clear the error indicators.

An attention condition is caused by: an error in the error registers, the completion of a positioning operation, the change of state of the MOL bit, dual port operation with the drive presently available if previously not available, or correct sector identification for the Search command.

Error (ERR) - Bit 14

Set when one or more of the errors in the error registers (RMER1 or RMER2) for a selected drive is set. While ERR is asserted, commands other than Drive Clear are not accepted.

Positioning in Progress (PIP) - Bit 13

Set when a positioning command is accepted. These commands are: Seek, Recalibrate, and Search. Cleared when the moving function is completed at the time the DRY and ATA bits are set. For RM03/5 Emulations; this bit is set when MOL is reset. Set during a mid-transfer seek during a data transfer command.

Medium On-Line (MOL) - Bit 12

Set when the unit ready line from the drive is asserted indicating that the drive is up to speed, the heads are positioned over the recording tracks and no fault condition exists within the drive. Cleared when the spindle is powered down or the drive is off-line. Whenever the MOL bit changes state, the ATA bit is set.

Write-Lock (WRL) - Bit 11

Set when the write protected line from the drive is asserted as enabled by a switch located on the drive. A write command on a write-locked drive will cause the write-lock error bit (WLE, bit 11 of RMER1) to be set. For RM80 emulations, this bit is set when MOL is reset.

Last Sector Transfer (LST) - Bit 10

Set when the last addressable sector on the disk pack has been read or written. Cleared when a new write to RMDA is received.

At the time LST is set, the RMDA register is reset to zero and the RMDC register increments by one to the first illegal cylinder address. If the RMWC register is not zero, a mid transfer seek is

aborted which will cause the AOE status bit (RMER1, bit 09) to be set indicating that the desired cylinder register overflowed during a read or write.

Programmable (PGM) - Bit 09

This bit is set when dual port or dual access operation is enabled.

Drive Present (DPR) - Bit 08

This bit is set if the controller has seized the drive and is reset when the other controller has seized the drive. This bit is a reflection of the DVA bit in RMCS1.

Drive Ready (DRY) - Bit 07

Set at the completion of every command and cleared at the initiation of a command. When set, this bit indicates the readiness of the drive to accept a command. If a mechanical movement command was initiated, the ATA bit will also be set when DRY is set. This bit is the complement of the drive's GO bit.

Volume Valid (VV) - Bit 06

Set by the Pack Acknowledge or Read-in Present commands. Cleared whenever the drive cycles up from the OFF state. When reset, this bit indicates that the drive has been off-line and a disk pack may have been changed.

Offset Mode (OFM) - Bit 00

Set by the offset command to indicate that a read will be done with the heads in the offset position as determined by RMOF Bit 07. Cleared by a Read-in Preset, Return-to-Centerline, Recalibrate or write command, or a mid-transfer seek. Also cleared whenever the drive cycles up.

4.9 ERROR REGISTER 1 (RMER1) F28408

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRC	HCE	ECH	WCF	FER	PAR	RMR	ILR	ILF

The RMER1 register is a read/write register that is used to store the error status for the addressed drive. The RMER1 register can only be written as a word. If the program attempts to write into this register while the drive is busy, an RMR (RMER1 register, bit 02) error is set, and the contents of the register are not otherwise modified. Writing zeros into this register should not be used as the normal way of clearing errors. The Drive Clear command should be used instead.

Data Check (DCK) - Bit 15

Set during a read operation when the ECC hardware detects an ECC error. The data transfer terminates with the current sector. If the Error Correction Inhibit (ECI) bit is off, the controller will go into the error correction process, and the DRY bit will not be set until the end of the process. If ECI bit is on, the error correction process is inhibited, and DRY is set immediately.

Unsafe (UNS) - Bit 14

This bit is a composite error bit of the unsafe and seek incomplete error conditions in the RMER2 register. With UNS set, correct results on any operation cannot be guaranteed. Some faults must be cleared by manual intervention at the drive.

Operation Incomplete (OPI) - Bit 13

Set when a read or write command involving header search cannot find the physical sector within three index pulses. Also set during a search operation where a sector count match is not made within three index pulses. In dual port mode, OPI is set when a seek, search or data transfer command is issued to a drive that is busy. When set, the GO bit is cleared and the DRY bit is set.

Drive Timing Error (DTE) - Bit 12

Set when either the header or data sync pattern is not found. When DTE is set, the GO bit will be cleared and the DRY bit set. Also set if a sector pulse occurs before the end of the data field.

Write Lock Error (WLE) - Bit 11

Set when a write command is issued to a write-locked drive.

Invalid Address Error (IAE) - Bit 10

Set when the address in RMDC or RMDA is invalid and a Seek, Search or data transfer command is initiated.

Address Overflow Error (AOE) - Bit 09

Set when the RMDC register overflows during a read or write operation indicating that the address has exceeded the cylinder address limit. With AOE set, the controller will terminate the operation when the last sector of the last cylinder has been read or written.

Header CRC Error (HCRC) - Bit 08

Set by a CRC error in the header. If a CRC error is detected during a read or write command, the controller will not make any data transfer. In the event of a CRC error during a read header and data command, the entire sector including header will be transferred with the HCRC bit set.

Header Compare Error (HCE) - Bit 07

Set when the first two words of the header read at the sector whose count is equal to the desired sector field of RMDA do not match the contents of RMDC and RMDA. If the HCE bit is set during a read or write command, the controller will not perform any data transfer. In the event of a read header and data command, the entire sector will be transferred with the HCE bit set.

ECC Hard Error (ECH) - Bit 06

Set when the error correction procedure indicates that the error was a non-correctable ECC error. DCK (bit 15) is also set.

Write Clock Fail (WCF) - Bit 05

This bit is normally a zero unless written into.

Format Error (FER) - Bit 04

Set if the FMT16 bit in RMOF does not match bit 12 in Word 1 of a sector's header. Although the controller implements both 16 bit and 18 bit sector formats, all sectors contain 256 16-bit words in either format. If FER is set, then HCE may not be set.

Massbus Parity Error (PAR) - Bit 03

This bit is normally a zero unless written into.

Register Modification Refused (RMR) - Bit 02

Set when a write is attempted to any drive register (except RMAS) with DRY equal to zero. The drive operation in progress continues.

Illegal Register (ILR) - Bit 01

This bit is set when addressing an illegal drive register. Only registers 0 to 15 are legal. The upper 16 registers are illegal.

Illegal Function (ILF) - Bit 00

Set when an illegal function code (with GO) is written into RMCS1.

4.10 MAINTENANCE REGISTER 1 (RMMR1) F2840C

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DMD

RMMR1 is a read/write register that allows a program to simulate various signals from the disk for diagnostic testing of the

controller. Writing to RMMR1 can occur at any time regardless of the status of the drive. A drive or controller clear resets this register except for bit 03, which is set.

Diagnostic Mode (DMD) - Bit 00

Set by the diagnostic program to reconfigure the drive into maintenance mode. Since Diagnostic Mode is not emulated on the SC750, none of the bits of this register have any affect on controller operation.

4.11 ATTENTION SUMMARY REGISTER (RMAS) F28410

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	ATA 7	ATA 6	ATA 5	ATA 4	ATA 3	ATA 2	ATA 1	ATA 0

The RMAS register allows the program to examine the attention status of all drives with only one register read operation. It also provides a means of resetting the attention logic in a selected group of drives. The eight low-order bits of this register correspond to the ATA bits in the RMDS of the drive having the same unit number as the bit position of this register.

A drive's ATA bit can be reset by loading a one into the bit position corresponding to the drive's unit number. Loading a zero has no effect. For a program to use the RMAS without losing status information, the program must use MOV instructions for all writes to this register. An instruction that does a read-restore (such as BIS) may cause bits that were asserted between the read and the restore to be lost. This register can be read or written at any time. This register is replicated for every drive, and can be accessed with any drive address without causing NED errors.

A persistent error, just like any error condition, will cause the ATA bit to be reasserted. Attempts by the controller to clear the error will not work in this case.

4.12 DISK ADDRESS REGISTER (RMDA) F28414

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Track Address								Sector Address							

This register is used to address the sector and track on the disk to or from which a transfer is desired. The RMDA is incremented each time a sector of data is transferred so that consecutive blocks are automatically addressed when the word count indicates that more than one block is to be transferred. At the end of a transfer, RMDA contains the address of the sector following the last one involved in data transfer.

The RMDA contains a sector counter that typically provides for 32 sectors per track. The register also contains a track counter which is incremented by one every time the sector counter overflows. When the sector address and the track address reach their maximum counts, they are reset to zero and the RMDC is incremented by one.
The invalid address error (IAE, RMER1, bit 10) is set if the address in the RMDA is invalid when a data transfer, Seek, or Search function is initiated. The maximum track and sector counts are obtained from the selected configuration.

4.13 DRIVE TYPE REGISTER (RMDT) F28418

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	MOH	0	DPM	0	0	0	Drive Type Code							

Moving-Head (MOH) - Bit 13

This bit is always a one indicating that the drive is a moving head device.

Dual Port Mode (DPM) - Bit 11

This bit signifies that the drive is operating in dual port mode as enabled by SW1-6, or dual access mode as enabled by SW4-4.

Drive Type Code - Bits <07:00>

This code specifies the type of drive as follows:

14 - RM03, 15 - RM02, 16 - RM80, 17 - RM05.

4.14 LOOK-AHEAD REGISTER (RMLA) F2841C

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	Sector Counter					0	0	0	0	0	0

The RMLA register contains the drive sector counter and is used to present the angular position of the disk relative to the read/write heads for the addressed drive. The purpose of this register is to provide the programmer with a means of optimizing disk accesses by minimizing rotational delays. The counter typically counts from 0 to 31 or from 0 to 29, depending on the status of the FMT16 bit in RMOF.

4.15 SERIAL NUMBER REGISTER (RMSN) F28420

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SW1 -8	SW1 -7	SW1 -6	SW1 -5	SW1 -4	SW1 -3	SW1 -2	SW1 -1	Firmware Rev.				Port No.			

The purpose of the RMSN register in a DEC RM drive is to distinguish a drive from similar drives attached to the controller by means of a four decade serial number. Here it contains the controller port number to which the drive is attached, the firmware revision level, and the eight SW1 switch settings.

4.16 OFFSET REGISTER (RMOF) F28424

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	FMT 16	ECI	HCI	SEI	0	OFD	0	0	0	0	0	0	0

The RMOF register contains three inhibit bits and the drive offset direction bit. The offset direction bit determines if a read will be done with the heads advanced or retarded from normal centerline position. The actual offset determination is done by the status of RMDS bit 00. All bits of this register are cleared by Read-in Preset command.

Format Bit (FMT 16) - Bit 12

Set for 31/32 sector (16 bit) mode and reset for 30 sector (18 bit) mode. Since the controller only handles 16 bits per word format, this bit should always be a one. When this bit is set, an RM80 emulation operates with one less sector per track than the track contains. The extra sector is a skip sector that is used when a bad sector is found. When set this bit typically allows for 32 sectors per track on RM03/RM05 emulations. Some configurations allow 48 sectors per track.

Error Correction Code Inhibit (ECI) - Bit 11

Set to inhibit error correction when an ECC error is detected.

Header Compare Inhibit (HCI) - Bit 10

Set to inhibit header compare and CRC check. With HCI set, the controller depends only on the sector count for sector identification. It is recommended that the HCI bit be reset during a write operation.

Skip Sector Error Inhibit (SEI) - Bit 09

For RM80 emulations only. Set to inhibit skip sector errors during a header check. When this bit is set the drive operates on all sectors per track, including the skip sector. This bit is reset whenever a data transfer command increments RMDA to a new track

address. This bit cannot be set unless the FMTI6 bit is already set.

Offset Direction (OFD) - Bit 07

Set under software control to select the direction of positioner offset. A one retards the heads, and a zero advances the heads.

4.17 DESIRED CYLINDER REGISTER (RMDC) F28428

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	Desired Cylinder Address									

The RMDC register contains the address of the cylinder to which the positioner is to move. The RMDC register will be cleared by the Read-in Preset command. Following an initial load, the value in the RMDC register will be incremented by one whenever the RMDA register is reset to zero during a data transfer. When the RMDC register is incremented and the RMWC register is not equal to zero, a mid-transfer seek is initiated by the controller.

The Invalid Address Error (IAE) bit will be set when, upon asserting the GO bit, the RMDC register contains an address greater than the largest addressable cylinder.

4.18 HOLDING REGISTER (RMHR) F2842C

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RMHR is a read-only register that returns a zero when read except as follows: If the register is written into with one of the values listed below, the configured size of the addressed drive is read-out as indicated:

8017 - Maximum cylinder address
8018 - Maximum track address
8019 - Maximum sector address (per status of RMOF)

Writing a FFFF into the register enables the optional Format command to be executed when loaded into RMCS1. The enable is cleared when any data transfer command terminates. Whenever data is written into RMDA, the complement of that data is placed in RMHR.

4.19 MAINTENANCE REGISTER 2 (RMMR2) F28430

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
$13FF_{16}$															

RMMR2 is a read-only register that always returns $13FF_{16}$ when read.

4.20 ERROR REGISTER 2 (RMER2) F28434

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BSE	SKI	OPE	IVC	LSC	LBC	MDS	DCU	DVC	ACU	SSE	0	DPE	0	0	0

Error Register 2 is a read/write register that contains status information relating to the electromechanical performance of the addressed drive. If any bit is set in this register, then the ERR bit in RMDS is also set. In some cases, the UNS bit in RMER1 will also be set. Writing zeros into this register should not be used as the normal way of clearing errors. A drive clear or a controller clear should be used instead. If the program attempts to write into this register while the drive is busy, the RMR bit in RMER1 will be set and the write will be ignored.

Bad Sector Error (BSE) - Bit 15

Set whenever the controller detects a zero in bit 14 or 15 of the first header word and the HCI bit in RMOF equals 0.

Seek Incomplete (SKI) - Bit 14

Set whenever a Seek Error is received from the drive. This error also sets the UNS bit in RMER1. The controller automatically issues a Fault Clear and a Return-to-Zero to the drive if a Seek Error is detected.

Operator Plug Error (OPE) - Bit 13

Set whenever the drive's address plug is removed and then reinstalled. Can be cleared by issuing a drive clear.

Invalid Command (IVC) - Bit 12

Set whenever any command is issued to a drive with ERR equal one or MOL equal zero. Set whenever any command except a Read-in Preset, a Pack Acknowledge or NOP is issued to a drive with VV equal zero.

Loss of Sector Clock (LSC) - Bit 11

Set when the controller detects more than 63 Sector pulses without an Index pulse (Sector and Index on B cable).

Loss of Bit Clock (LBC) - Bit 10

Set if the controller does not detect at least 16 servo clocks within 3.0 microseconds.

Multiple Drive Select (MDS) - Bit 09

Set when more than one drive responds to a logical address on the A cable. This bit cannot be set by a programmed I/O write.

D.C. Power Unsafe (DCU) - Bit 08

Set if the -5 VDC power supply to the cable drivers and receivers is not proper. This bit cannot be set by a programmed I/O write.

Device Check (DVC) - Bit 07

Set if a Fault indication is received from the drive. This error also sets the UNS bit in RMER1. The controller automatically issues a Fault Clear and a Return-to-Zero to the drive if a Fault is detected.

AC Power Unsafe (ACU) - Bit 06

Set if an ACLO indication is received from the Unibus. This bit cannot be set by a programmed I/O write.

Skip Sector Error (SSE) - Bit 05

For RM80 emulations only. Set whenever bit 13 of the header Word 1 is set and bit 09 of RMOF is reset. This error indicates that the sector has been skipped and the data resides in the next sector. This bit cannot be written into unless the drive is an RM80.

Data Parity Error (DPE) - Bit 03

This bit is normally a zero unless written into.

4.21 ECC POSITION REGISTER (RMEC1) F28438

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	ECC Position												

The Error Correction Code (ECC) Position register is a read-only register that contains the position of the error pattern as determined by the ECC correction procedure. The error position is the number of bit positions from the beginning of the sector's data field to (and including) the right most bit position of the error pattern stored in RMEC2. If the detected error is not correctable using ECC, the ECH error bit in RMER1 will be set.

4.22 ECC PATTERN REGISTER (RMEC2) F2843C

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	Error Pattern										

The Error Correction Code (ECC) Pattern register is a read-only register that contains the 11-bit error correction pattern obtained from the ECC correction procedure. A one in the error pattern

indicates that a bit of the data in memory from the last read sector is in error. The error pattern may straddle two 16-bit words in memory. The bit displacement to the right most bit of the pattern is determined by the bit count in RMEC1. The actual correction is done by an exclusive-OR of the error pattern and the data in memory.

4.23 ILLEGAL DRIVE REGISTERS

The top 16 drive registers (addresses F28440 to F2847C) are illegal addresses. Access to these locations will set ILR (bit 01, RMER1).

4.24 MBA MAP REGISTERS F28800 - F28BFC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
V	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	Physical Page Frame Number														

The controller contains 256 map registers which are used to form the CMI physical memory address from the 17-bit virtual address contained in MBAVAR. Map registers can only be written when there is no data transfer operation in progress or the IBC (MBACR, bit 04) is set. A write to a map register during a data transfer with the IBC clear will be ignored and cause PGE to set in MBA SR.

Valid Bit (V) - Bit 31

This bit indicates that the entry is a valid PFN.

Physical Page Frame Number (PFN) - Bits <14:00>

High-order 15 bits of the physical memory address.

Operations are initiated on the addressed drive by loading the function code and GO bit into RMCS1. The function code specifies a specific command. The commands can be divided into three categories: data transfer commands, positioning commands, and housekeeping commands. Commands and their corresponding function codes (always odd since the GO bit must be asserted to execute the command) are described below.

5.1 DATA TRANSFER COMMANDS

These commands involve data transfers to or from the disk and are designated by function codes 29 through 3F.

All data transfer commands have seek and sector search functions implied. When the desired cylinder does not equal the current cylinder during the execution of the data transfer, a seek will be issued to the desired cylinder. The controller will then search the desired track for the desired sector and, when found, will start the data transfer. On all commands except the Write Header and Data command (which is the format operation) and Read/Write Check Header and Data commands, a match of the sector header must be made before the data transfer is started. If the header compare inhibit (HCI, bit 10 in RMOF) is set, the header will not be compared or checked and, like the Write Header and Data command, the transfer will be started based on the pre-recorded sector pulses. With the HCI bit set, header errors will not be reported. With the HCI bit cleared, the transfer will be aborted if a header error is detected. The Read/Write Check Header and Data commands abort only the transfers following the sector that caused the error.

The desired sector, track and cylinder addresses are updated after the transfer of a sector. Therefore, at the end of a transfer, the disk is set up to transfer the next sequential sector. This allows multiple sector transfers and spiral transfers across tracks and cylinders. When the desired cylinder address changes during a transfer, the implied seek is performed and is termed a mid-transfer seek.

The data transfer commands are described below.

5.1.1 Write Check Data (29)

This command reads data from the selected drive and compares it on a byte by byte basis with that obtained from memory. If the data fails to compare, the WCU or WCL status bit is set and the command is terminated immediately. For additional information on write check errors see Sections 4.2 and 4.3.

5.1.2 Write Check Header and Data (2B)

This command reads the header field and data field from the selected drive and compares it on a byte by byte basis with data obtained from memory. If the header and data fail to compare, the WCU or WCL status bit is set and the command is terminated immediately.

5.1.3 Write Data (31)

This command writes the 256-word data field of the selected sector with data obtained from memory. A two-word ECC is appended to each sector. If the byte count goes to zero during the sector, the rest of the sector is zero filled. After a sector transfer the byte count is checked, and if not zero, the data transfer operation is continued to the next sector; otherwise the command is terminated.

5.1.4 Write Header and Data (format) (33)

This command writes the two-word header field and the 256-word data field of the selected sector with data obtained from memory. A one word CRC is appended to each header field, and a two word ECC is appended to each data field. After a sector transfer the byte count is checked, and if not zero, the transfer is continued to the next sector; otherwise the command is terminated. If byte count goes to zero during the sector, the rest of the sector is zero filled.

5.1.5 Read Data (39)

This command reads the 256-word data field from the selected sector and transfers the data to memory. When the sector data transfer is complete, the ECC is checked to ensure that the data read from the disk was error free. If a data error occurred, the ECC correction procedure is initiated (if the ECI bit in RMOF is reset) to determine whether the error is correctable. When finished, the read command is terminated to allow software to apply the correction information. If no data errors are detected, the byte count is checked; if the byte count is not zero, the data transfer operation is repeated with the next sector. If the byte count goes to zero during the sector, the rest of the sector is not transferred.

5.1.6 Read Header and Data (3B)

This command transfers the two-word sector header field and the 256-word data field from the selected sector to memory. When the sector data transfer is complete, the ECC is checked to ensure that the data read from the disk was error free. If a data error occurred, the ECC correction procedure is initiated (if the ECI bit in RMOF is reset) to determine whether the error is correctable. When finished, the command is terminated to allow software to apply the correction information. If no data errors are detected, the byte count is checked; if the byte count is not zero, the data transfer operation is repeated with the next sector.

5.2 POSITIONING COMMANDS

Positioning commands are mechanical movement commands used to position the heads over the disk pack and take milliseconds to complete. Upon initiating the positioning commands, the controller will set the PIP bit and reset the DRY bit. Upon completion of the positioning operation, the controller resets the PIP and GO bits, and sets the DRY and ATA bits. The positioning commands are described below.

5.2.1 Seek Command (5)

This command causes the heads to be moved to the cylinder address specified by the contents of RMDC. When the controller sees the Seek command with the GO bit set, it sends the cylinder address to the corresponding drive. Any attempt to write into RMDC while the seek is in progress will cause the RMR bit to be set and RMDC will not be modified. Upon completion of the seek operation, the ATA and DRY bits in RMDS are set, and the GO bit is reset. If the drive is unable to complete a move within 500 milliseconds or if it has moved the carriage to a position outside the recording field, the drive asserts the seek error signal and the controller sets the SKI error bit in RMER2 and the ERR, ATA and DRY bits in RMDS. The controller will automatically issue a Fault Clear and a Return-to-Zero to the drive so that Drive Clear command can clear the error.

5.2.2 Recalibrate (7)

This command will cause the drive positioner to position the heads over cylinder zero. A Return-to-Zero is automatically performed with each head load sequence and whenever a Fault or Seek Error is detected. This command clears the OFM bit in RMDS.

5.2.3 Offset Command (D)

This command causes the OFM bit in RMDS to be set. Subsequent reads will be done with the heads offset from track centerline in the direction specified by RMOF bit seven. This operation allows additional data recovery attempts over that provided by the ECC capability when an ECC error is detected. If an ECC hard error occurs, two offset positions should be used. At the completion of the offset command, the ATA bit is set indicating that a read command should be issued to the cylinder and track in order to recover data.

The OFM bit in RMDS will be cleared by any one of the following:

1. Seek to another cylinder by means of implied or mid-transfer seek,
2. Write command,
3. Return-to-centerline command,
4. Recalibrate command,

5. Read-in preset command, or
6. Whenever the drive cycles up from the OFF state.

5.2.4 Return-to-Centerline Command (F)

This command is used to clear the OFM bit and set the ATA bit in RMDS. It also resets the OFD bit in RMOF.

5.2.5. Search Command (19)

The search command causes the controller to first perform a seek to the desired cylinder and then compare the sector counter with the desired sector in the RMDA register. When they match, it sets the ATA bit causing an interrupt to the computer if IE in RMCS1 is set. An unsuccessful completion of a search command occurs when a sector count and desired sector address match is not made during the interval of three index pulses, in which case the OPI bit is set.

5.3 HOUSEKEEPING COMMANDS

Housekeeping commands are used to place drive logic into a known or initialized state and usually takes only a few microseconds to execute. The housekeeping commands are listed below.

5.3.1 NO OP (1)

This command does not perform any operation, except to clear the ATA bit.

5.3.2 Drive Clear (9)

This command causes the following registers and conditions associated with the drive selected to be cleared: ATA and ERR in RMDS, RMER1, RMER2, RMEC2, RMMR1 (except bit three which is set) and ATA bit in RMAS.

5.3.3 Release Command (B)

This command performs a drive clear function, and then releases the drive for use by the other port.

5.3.4 Read-In Preset (11)

This command sets the VV (volume valid) bit, clears the RMDC and RMDA registers, clears the RMOF register, and clears the OFM bit in the RMDS register.

5.3.5 Pack Acknowledge (13)

This command sets the VV bit for the command controller. This command or a Read-in Preset command must be issued before any data transfer or positioning command can be given if the pack has gone off-line and then on-line (i.e., MOL change of state). It is primarily intended to avoid unknown pack changes.

5.4 OPTIONAL COMMANDS

The Format command can be executed only after writing an FFFF into RMHR.

5.4.1 Format (3F)

This command executes a Return-to-Zero, clears RMDC and RMDA, and formats the entire pack in standard format. Each sector has bits 14, 15 and the FMT16 bit set in Header Word 1 and an all zeros data field. RMDC will be set to the last cylinder number plus one at completion, the LST bit in RMDS will be set, and the FMT16 bit in RMOF will be set. This command will format full tracks for all emulations. No Bad Sector File or Skip Sector File is written.

5.5 OVERLAPPED SEEKS AND SEARCHES

Normally, overlapped Seeks and Searches terminate and raise the drive's ATA bit as soon as the drive is properly positioned. On systems with two logical units per physical unit there is a slight change. In those cases where overlapped Seeks or Searches are issued to two logical units on the same physical drive, the following rules apply:

1) The first logical unit to be issued a seek or search command will do the physical seek. The other logical unit will simulate the seek.

2) For seek commands, the logical unit that did the physical seek will raise its ATA bit first. The other logical unit will raise its ATA bit at least 45 sec later.

3) For search commands, if option switch SW1-4 is OFF then the first logical unit that finds a rotational match after the physical seek has ended will raise its ATA first. If option switch SW1-4 is ON then the logical unit that did the physical seek will raise its ATA bit when a rotational match occurs after the physical seek has ended. The other logical unit will raise its ATA bit after the first logical unit raises its ATA bit and a rotational match subsequently occurs. This allows the user to service the logical unit actually on cylinder first, thus minimizing physical seeks.

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APPENDIX A

SC750/B CONFIGURATION AND OPTION SELECTION

A.1 INTRODUCTION

To allow the user of the SC750/B the greatest amount of flexibility in selecting disk drives for his system, the SC750/B supports a wide variety of disk types and offers a number of other user selectable options. This appendix is designed as a quick reference to the various switches which make this flexibility possible.

A.2 CONTROLLER CONFIGURATION

The SC750/B unit is capable of controlling a wide variety of disk drives of various sizes and types. The various drives that are supported are defined by one of the two configuration PROMs which are shipped with the SC750/B. Configuration PROM #496 is shipped already installed in the socket at U23. An alternate PROM, #C01, is shipped in a spare socket located at U24. Section A.2.4, below, describes configuration selection and exlains which PROM you will need to use. Table A-1 is a list of the drive types and sizes that are supported.

A.2.1 SC750/B1 vs /B3 Firmware

The setting of the number of sectors for the 2351A Fujitsu (Eagle) will be dependent upon the type of Emulex SC750/B firmware the user has. Users with the /B1 firmware must configure the Eagle for 44 hard sectors. Those with /B3 firmware must configure the Eagle for 48 sectors. This 48 sector configuration supports an additional 40 Mb of capacity. See Tables A-2 and A-3 for a list of configurations supported by the SC750/B. Note that in these tables configurations for the 2351A Fujitsu (key 470) are listed as being configured for 44/48 sectors. Those configurations are supported at 44 sectors per track by the /B1 firmware and 48 sectors per track by the /B3 firmware. See paragraph A.2.3 for important information on sectoring the Fujitsu Eagle.

A.2.2 Physical vs Logical Disk Numbering

One of the primary features of the SC750/B is that it can emulate up to eight DEC disk subsystems using only four physical disk drives. This is accomplished by mapping two logical disk subsystems on to one disk drive that has double the capacity of the standard DEC subsystem. In such cases the logical units are mapped on to the physical units as follows:

Physical Unit Number	Logical Unit Numbers
0	0 and 4
1	1 and 5
2	2 and 6
3	3 and 7

The physical/logical assignments for specific disk configurations can be found by comparing the Physical drive column to the Logical drive column in Tables A-2 and A-3.

A.2.3 Sectoring CDC Drives and the 2351A Fujitsu

To allow CDC drives and the 2351A Fujitsu to function properly with the SC750/B, some alterations must be made to the sector select switch settings found in their manuals.

To configure CDC drives for 33 sectors, switch 0 must be CLOSED, with all other switches set as per the CDC manual. To configure the 2351A Fujitsu for 48 sectors the jumpers at location BC7 must be set such that bit one is jumpered 2-3 (rather than 3-4), bit 2 is jumpered as 6-7 (rather than 5-6), and all other jumpers are as per the Fujitsu manual.

A.2.4 Drive Configuration Selection

The SC750/B emulates three different DEC disk subsystems, the RM03, the RM05 and the RM80. The RM03 subsystem has an unformatted capacity of 80 Mb. The RM05 has an unformatted capacity of 300 Mb. The RM80 has a capacity of 160 Mb.

There are essentially three different types of drive configurations. In the first case, each emulated DEC drive exists on one physical drive. In the second case, two emulated drives are mapped on to one physical drive (see paragraph A.2.1). The third case is a combination of the first two.

With the exception of configurations noted, none require patches to the operating system or diagnostics. The others require patches to the disk driver to include the expanded block counts and sector counts where applicable. Note that DEC drivers cannot be patched for more than 32 sectors per track. Emulex has a VMS driver that automatically self-sizes to each drive. The Emulex driver can accommodate up to 64 sectors per track. Neither the diskless nor the functional diagnostics will run on non-standard size drives.

To find the configuration switch setting that is suitable for your disk installation, use the following process. Note that some configurations require drives set with 32 hard sectors and some require drives set with 33 or 44 or 48 hard sectors (Physical SEC column of Tables A-2 and A-3). See the drive manufacturer's installation manual for instructions. Note also that use of a Trident type drive requires that SW1-5 be closed.

1. Locate your drive type and size in Table A-1. Note down the KEY assigned to your drive. If you intend to use more than one type of drive, note down their assigned KEYs as well. Make sure your drive is hard sectored as indicated in the SEC column of Tables A-2 and A-3.

2. Scan down the KEY column of Tables A-2 and A-3 until you find your drive's number. Check the type of emulation in the Logical drive column. If the emulation is not the one you require, continue to scan down the KEY column, etc., until you find the required emulation.

3. When you find a suitable match for Drive 0, check the drive key and type for Drives 1, 2 and 3 for that configuration row. You do not need to use all four drive ports.

4. When you find a suitable configuration, set the Configuration Switches (SW2) as indicated.

5. If the configuration you want to use is listed in Table A-3, you must use the alternate configuration PROM (Emulex PROM #C01) which is shipped in a spare socket located at U48. To use this PROM, carefully remove the configuration PROM located at U23 (Emulex PROM #496) and replace it with the alternate PROM. The unused PROM may be stored in the spare socket at U24.

TABLE A-1
DRIVES SUPPORTED

Model Numbers	KEY	Sects
Ampex/330	330	32/33
Ampex/9300	301	32
Century/T82RM	80	32
Century/T302RM	300	32
CDC/9715-340	340	32
CDC/9730-80	80	32
CDC/9730-160	160	32/33[1]
CDC/9762	80	32
CDC/9766	300	32
CDC/9775	675	32/33[1]
Fujitsu/2312	84	32/33
Fujitsu/2280	80	32
Fujitsu/2294	330	32/33
Fujitsu/M2284	160	32/33
Fujitsu/2351A	470	44/48[2]
NEC/D1510	331	32/33
STC/8775	673	32
Tecstor/S160	162	32/33

[1]See paragraph A.2.3.

[2]See paragraphs A.2.1 and A.2.3.

TABLE A-2
DRIVE CONFIGURATIONS, PROM No. 496

CONF NO.	SW2- 6	5	4	3	2	1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) = Dr Type	Rev
00	O	O	O	O	O	O	80	0	32	0 = RM03	A
							80	1	32	1 = RM03	A
							80	2	32	2 = RM03	A
							80	3	32	3 = RM03	A
01	O	O	O	O	O	C	160	0	33	0 = RM80	A
							160	1	33	1 = RM80	A
							160	2	33	2 = RM80	A
							160	3	33	3 = RM80	A
02	O	O	O	O	C	O	300	0	32	0 = RM05	A
							300	1	32	1 = RM05	A
							300	2	32	2 = RM05	A
							300	3	32	3 = RM05	A
03	O	O	O	O	C	C	160	0	33	0,4 = RM03	A
							160	1	33	1,5 = RM03	A
							160	2	33	2,6 = RM03	A
							160	3	33	3,7 = RM03	A
04	O	O	O	C	O	O	675	0	33	0,4 = RM05	A
							675	1	33	1,5 = RM05	A
							675	2	33	2,6 = RM05	A
							675	3	33	3,7 = RM05	A
05	O	O	O	C	O	C	673	0	32	0,4 = RM05	A
							673	1	32	1,5 = RM05	A
							673	2	32	2,6 = RM05	A
							673	3	32	3,7 = RM05	A
06	O	O	O	C	C	O	330	0	33	0,4 = RM80	A
							330	1	33	1,5 = RM80	A
							330	2	33	2,6 = RM80	A
							330	3	33	3,7 = RM80	A
07	O	O	O	C	C	C	80	0	32	0 = RM03	A
							80	1	32	1 = RM03	A
							300	2	32	2 = RM05	A
							300	3	32	3 = RM05	A
08	O	O	C	O	O	O	80	0	32	0 = RM03	A
							300	1	32	1 = RM05	A
							300	2	32	2 = RM05	A
							300	3	32	3 = RM05	A
09	O	O	C	O	O	C	300	0	32	0 = RM05	A
							300	1	32	1 = RM05	A
							80	2	32	2 = RM03	A
							80	3	32	3 = RM03	A
0A	O	O	C	O	C	O	300	0	32	0 = RM05	A
							300	1	32	1 = RM05	A
							300	2	32	2 = RM05	A
							80	3	32	3 = RM03	A
0B	O	O	C	O	C	C	160	0	33	0,4 = RM03	A
							160	1	33	1,5 = RM03	A
							80	2	32	2 = RM03	A
							80	3	32	3 = RM03	A

TABLE A-2, cont.

CONF NO.	SW2- 6 5 4 3 2 1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) = Dr Type	Rev
0C	O O C C O O	160	0	33	0,4 = RM03	A
		160	1	33	1,5 = RM03	A
		160	2	33	2,6 = RM03	A
		80	3	32	3 = RM03	A
0D	O O C C O C	160	0	33	0 = RM80	A
		160	1	33	1 = RM80	A
		80	2	32	2 = RM03	A
		80	3	32	3 = RM03	A
0E	O O C C C O	160	0	33	0 = RM80	A
		160	1	33	1 = RM80	A
		160	2	33	2 = RM80	A
		80	3	32	3 = RM03	A
0F	O O C C C C	675	0	33	0,4 = RM05	A
		675	1	33	1,5 = RM05	A
		300	2	32	2 = RM05	A
		300	3	32	3 = RM05	A
10	O C O O O O	675	0	33	0,4 = RM05	A
		675	1	33	1,5 = RM05	A
		675	2	33	2,6 = RM05	A
		300	3	32	3 = RM05	A
11	O C O O O C	300	0	32	0 = RM05	A
		300	1	32	1 = RM05	A
		675	2	33	2,6 = RM05	A
		675	3	33	3,7 = RM05	A
12	O C O O C O	300	0	32	0 = RM05	A
		675	1	33	1,5 = RM05	A
		675	2	33	2,6 = RM05	A
		675	3	33	3,7 = RM05	A
13	O C O O C C	160	0	33	0 = RM80	A
		160	1	33	1 = RM80	A
		300	2	32	2 = RM05	A
		300	3	32	3 = RM05	A
14	O C O C O O	160	0	33	0 = RM80	A
		160	1	33	1 = RM80	A
		160	2	33	2 = RM80	A
		300	3	32	3 = RM05	A
15	O C O C O C	330	0	33	0 = RM05[1]	A
		330	1	33	1 = RM05[1]	A
		330	2	33	2 = RM05[1]	A
		330	3	33	3 = RM05[1]	A
16	O C O C C O	160	0	32	0 = RM02[2]	B
		160	1	32	1 = RM02[2]	B
		160	2	32	2 = RM02[2]	B
		160	3	32	3 = RM02[2]	B
17	O C O C C C	330	0	32	0 = RM02[3]	B
		330	1	32	1 = RM02[3]	B
		330	2	32	2 = RM02[3]	B
		330	3	32	3 = RM02[3]	B

TABLE A-2, cont.

CONF NO.	SW2- 6	5	4	3	2	1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s)	= Dr Type	Rev
18	O	C	C	O	O	O	330	0	33	0	= RM05	C
							300	1	32	1	= RM05	C
							300	2	32	2	= RM05	C
							300	3	32	3	= RM05	C
19	O	C	C	O	O	C	330	0	33	0	= RM05	C
							330	1	33	1	= RM05	C
							300	2	32	2	= RM05	C
							300	3	32	3	= RM05	C
1A	O	C	C	O	C	O	330	0	33	0	= RM05	C
							330	1	33	1	= RM05	C
							330	2	33	2	= RM05	C
							300	3	32	3	= RM05	C
1B	O	C	C	O	C	C	162	0	33	0,4	= RM03	C
							162	1	33	1,5	= RM03	C
							162	2	33	2,6	= RM03	C
							80	3	32	3	= RM03	C
1C	O	C	C	C	O	O	162	0	33	0	= RM80	C
							162	1	33	1	= RM80	C
							162	2	33	2	= RM80	C
							162	3	33	3	= RM80	C
1D	O	C	C	C	O	C	160	0	33	0	= RM80	C
							330	1	33	1	= RM05	C
							330	2	33	2	= RM05	C
							330	3	33	3	= RM05	C
1E	O	C	C	C	C	O	160	0	33	0	= RM80	C
							330	1	33	1,5	= RM80	C
							330	2	33	2,6	= RM80	C
							330	3	33	3,7	= RM80	C
1F	O	C	C	C	C	C	160	0	33	0,4	= RM03	C
							160	1	33	1,5	= RM03	C
							330	2	33	2	= RM05	C
							330	3	33	3	= RM05	C
20	C	O	O	O	O	O	470	0	44/48	0	= RM80[4]	D
							470	1	44/48	1	= RM80[4]	D
							470	2	44/48	2	= RM80[4]	D
							470	3	44/48	3	= RM80[4]	D
21	C	O	O	O	O	C	470	0	44/48	0	= RM80[4]	D
							470	1	44/48	1	= RM80[4]	D
							470	2	44/48	2	= RM80[4]	D
							300	3	32	3	= RM05	D
22	C	O	O	O	C	O	470	0	44/48	0	= RM80[4]	D
							470	1	44/48	1	= RM80[4]	D
							470	2	44/48	2	= RM80[4]	D
							80	3	32	3	= RM03	D
23	C	O	O	O	C	C	84	0	33	0	= RM03	D
							84	1	33	1	= RM03	D
							84	2	33	2	= RM03	D
							84	3	33	3	= RM03	D

CL 1 2 3 4 5 6

OP — — —

TABLE A-2, con't.

CONF NO.	SW2- 6 5 4 3 2 1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s)	= Dr Type	Rev
24	C O O O C O O	84	0	33	0	= RM03	D
		84	1	33	1	= RM03	D
		84	2	33	2	= RM03	D
		80	3	33	3	= RM03	D
25	C O O O C O C	301	0	32	0	= RM02[5]	E
		301	1	32	1	= RM02[5]	E
		301	2	32	2	= RM02[5]	E
		301	3	32	3	= RM02[5]	E
26	C O O O C C O	160	0	32	0	= RM02[2]	E
		160	1	32	1	= RM02[2]	E
		301	2	32	2	= RM02[5]	E
		301	3	32	3	= RM02[5]	E
27	C O O O C C C	80	0	32	0	= RM03	F
		80	1	32	1	= RM03	F
		330	2	33	2	= RM05	F
		330	3	33	3	= RM05	F
28	C O C O O O	160	0	33	0	= RM80	G
		160	1	33	1	= RM80	G
		470	2	44/48	2	= RM80[4]	G
		470	3	44/48	3	= RM80[4]	G
29	C O C O O C	160	0	33	0	= RM80	G
		470	1	44/48	1	= RM80[4]	G
		470	2	44/48	2	= RM80[4]	G
		470	3	44/48	3	= RM80[4]	G
2A	C O C O C O	470	0	44/48	0	= RM80[4]	G
		470	1	44/48	1	= RM80[4]	G
		80	2	32	2	= RM03	G
		80	3	32	3	= RM03	G
2B	C O C O C C	470	0	44/48	0	= RM80[4]	G
		470	1	44/48	1	= RM80[4]	G
		300	2	32	2	= RM05	G
		300	3	32	3	= RM05	G
2C	C O C C O O	331	0	33	0	= RM05	G
		331	1	33	1	= RM05	G
		331	2	33	2	= RM05	G
		331	3	33	3	= RM05	G
2D	C O C C O C	470	0	44/48	0	= RM02[6]	H
		470	1	44/48	1	= RM02[6]	H
		470	2	44/48	2	= RM02[6]	H
		470	3	44/48	3	= RM02[6]	H
2E	C O C C C O	470	0	44/48	0	= RM02[6]	H
		470	1	44/48	1	= RM02[6]	H
		470	2	44/48	2	= RM02[6]	H
		300	3	32	3	= RM05	H
2F	C O C C C C	160	0	33	0,4	= RM03	H
		160	1	33	1,5	= RM03	H
		300	2	32	2	= RM05	H
		300	3	32	3	= RM05	H

1 2 3 4 5 6

TABLE A-2, cont.

CONF NO.	SW2- 6 5 4 3 2 1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s)	= Dr Type	Rev
30	C C O O O O	160	0	33	0	= RM80	J
		160	1	33	1	= RM80	J
		300	2	32	2	= RM05	J
		80	3	32	3	= RM03	J
31	C C O O O C	160	0	33	0,4	= RM03	J
		160	1	33	1,5	= RM03	J
		300	2	32	2	= RM05	J
		80	3	32	3	= RM03	J
32	C C O O C O	300	0	32	0	= RM05	J
		300	1	32	1	= RM05	J
		160	2	33	2,6	= RM03	J
		160	3	33	3,7	= RM03	J
33	C C O O C C	80	0	32	0	= RM03	K
		160	1	33	1	= RM80	K
		160	2	33	2	= RM80	K
		160	3	33	3	= RM80	K
34	C C O C O O	470	0	44/48	0	= RM02[6]	L
		300	1	32	1	= RM05[7]	L
		300	2	32	2	= RM05[7]	L
		300	3	32	3	= RM05[7]	L
35	C C O C O C	470	0	44/48	0	= RM80[4]	L
		300	1	32	1	= RM05	L
		300	2	32	2	= RM05	L
		300	3	32	3	= RM05	L
36	C C O C C O	470	0	44/48	0	= RM80[4]	M
		470	1	44/48	1	= RM80[4]	M
		160	2	33	2,9	= RM03	M
		160	3	33	3,7	= RM03	M
37	C C O C C C	160	0	33	0	= RM80[7]	N
		470	1	44/48	1	= RM02[6]	N
		470	2	44/48	2	= RM02[6]	N
		470	3	44/48	3	= RM02[6]	N
38	C C C O O O	470	0	44/48	0	= RM02[6]	P
		300	1	32	1	= RM05[7]	P
		80	2	32	2	= RM03[7]	P
		80	3	32	3	= RM03[7]	P
39	C C C O O C	470	0	44/48	0	= RM02[6]	P
		470	1	44/48	1	= RM02[6]	P
		300	2	32	2	= RM05[7]	P
		80	3	32	3	= RM03[7]	P
3A	C C C O C O	470	0	44/48	0	= RM02[6]	R
		470	1	44/48	1	= RM02[6]	R
		470	2	44/48	2	= RM02[6]	R
		80	3	32	3	= RM03[7]	R
3B	C C C O C C	675	0	32	0	= RM05[8]	S
		675	1	32	1	= RM05[8]	S
		675	2	32	2	= RM05[8]	S
		675	3	32	3	= RM05[8]	S

TABLE A-2, cont.

CONF NO.	SW2- 6 5 4 3 2 1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) = Dr Type	Rev
3C	C C C C O O	80	0	32	0 = RM03	S
		80	1	32	1 = RM03	S
		80	2	32	2 = RM03	S
		470	3	44/48	3 = RM80[9]	S
3D	C C C C O C	470	0	44/48	0,4 = RM03[10]	S
		470	1	44/48	1,5 = RM03[10]	S
		300	2	33	2 = RM05	S
		300	3	33	3 = RM05	S
3E	C C C C C O	340	0	32	0 = RM05	T
		340	1	32	1 = RM05	T
		340	2	32	2 = RM05	T
		340	3	32	3 = RM05	T
3F	C C C C C C	340	0	32	0 = RM05	T
		340	1	32	1 = RM05	T
		340	2	32	2 = RM05	T
		300	3	32	3 = RM05	T

[1]This emulation has 862 logical cylinders.

[2]This RM emulation has 823 cylinders, 10 heads and a DTC of 15_{16}. This emulation is not supported by VMS, but was specifically included for use with Berkeley UNIX.

[3]This RM emulation has 1024 cylinders, 16 heads, and a DTC of 15_{16}. This emulation is not supported by VMS, but was specifically included for use with Berkeley UNIX.

[4]This RM80 emulation has 842 cylinders, 20 heads, 44 (/B1) or 48 (/B3) sectors and a DTC of 16_{16}. It has the skip characteristics of the RM80.

[5]This RM02 emulation has 815 cylinders, 19 heads and a DTC of 15_{16}.

[6]This RM02 emulation has 842 cylinders, 20 heads and a DTC of 15_{16}. This emulation is not supported by VMS, but was specifically included for use with Berkely UNIX.

[7]For UNIX systems. Not compatible with VMS.

[8]This RM05 has 842 cylinders, 40 heads and a DTC of 17_{16} (unmapped).

[9]This RM80 has 842 cylinders, 20 heads, 43 sectors and a DTC of 16_{16}. It is an expanded RM80 with the skip sector feature.

[10]This RM03 has 842 cylinders, 10 heads and a DTC of 14_{16}.

C = Closed (ON) O = Open (OFF).

TABLE A-3
DRIVE CONFIGURATIONS, PROM No. C01

CONF NO.	SW2- 6 5 4 3 2 1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s)	= Dr Type	Rev
00	O O O O O O	300	0	32	0	= RM05[1]	A
		300	1	32	1	= RM05[1]	A
		470	2	44/48	2	= RM02[2]	A
		470	3	44/48	3	= RM02[2]	A
01	O O O O O C	300	0	32	0	= RM05[1]	A
		300	1	32	1	= RM05[1]	A
		470	2	44/48	2	= RM03[2]	A
		470	3	44/48	3	= RM03[2]	A
02	O O O O C O	80	0	32	0	= RM03	A
		80	1	32	1	= RM03	A
		330	2	32/33	2,6	= RM80	A
		330	3	32/33	3,7	= RM80	A
03	O O O O C C	330	0	32/33	0	= RM05	A
		330	1	32/33	1	= RM05	A
		80	2	32	2	= RM03	A
		80	3	32	3	= RM03	A
04	O O O C O O	330	0	32/33	0	= RM05	A
		330	1	32/33	1	= RM05	A
		160	2	32	2,6	= RM03	A
		80	3	32	3	= RM03	A
05	O O O C O C	330	0	32/33	0,4	= RM80	B
		330	1	32/33	1,5	= RM80	B
		330	2	32/33	2,6	= RM03	B
		80	3	32	3	= RM03	B

[1] For UNIX use only. Not compatible with VMS.

[2] This RM emulation has 842 cylinders, 20 heads, and a DTC of 15_{16}. This emulation is not supported by VMS, but was specifically included for use with UNIX.

A.3 USER SELECTABLE OPTIONS

Several other options including the register starting address for the SC750/B can be user selected. The functions of the switches that select those options are defined in Tables A-4, A-5, A-6 and A-7, below.

TABLE A-4
OPTION SWITCH SW1 SETTINGS

Option Sw	Open	Closed	Function
SW1-1			Not used[2]
SW1-2			Not used[2]
SW1-3			Not used[2]
SW1-4	Disable	Enable	Delay on overlapped searches to the same physical drive.
SW1-5	Disable	Enable	CDS Trident drive compatibility.
SW1-6	Disabled	Enabled	Dual port mode
SW1-7	750	780	CPU selection[3]
SW1-8	B Cable	A Cable	Sector and Index signals[1]

[1]See paragraphs 3.2.3 and 3.6.4.

[2]All unused switches MUST BE OFF.

[3]Must be OPEN.

TABLE A-5
OPTION SWITCH SW2 SETTINGS

Option Sw	Open	Closed	Function
SW2-1			Drive configuration[2]
SW2-2			Drive configuration[2]
SW2-3			Drive configuration[2]
SW2-4			Drive configuration[2]
SW2-5			Drive configuration[2]
SW2-6			Drive configuration[2]
SW2-7			Not used[1]
SW2-8			Not used[1]

[1]All unused switches MUST BE OFF.

[2]See Table A-2.

TABLE A-6
OPTION SWITCH SW3 SETTINGS

Option Sw	Open	Closed	Function
SW3-1	Disable	Enable	VAX CPU reset (via AC LOW) when SW4-1 is switched ON
SW3-2			MBA arbitration level[2]
SW3-3			MBA arbitration level[2]
SW3-4			MBA arbitration level[2]
SW3-5			MBA arbitration level[2]
SW3-6			MBA arbitration level[2]
SW3-7			CMI vector/address[3]
SW3-8			CMI vector/address[3]

[1]All unused switches MUST BE OFF.

[2]See paragraph 3.6.2.

[3]See paragraph 3.6.1.

TABLE A-7
OPTION SWITCH SW4 SETTINGS

Option Sw	Open	Closed	Function
SW4-1	Run	Halt-Reset	Controller Run/Halt-Reset[2]
SW4-2			Not used[1]
SW4-3			Not used[1]
SW4-4	Disable	Enable	Dual Access mode[3]

[1]All unused switches MUST BE OFF.

[2]Causes VAX CPU reset as well when SW1-1 is ON.

[3]See paragraph 2.6.7.

APPENDIX B

DRIVE MODIFICATIONS

This appendix provides modifications to commonly used drives for moving the Sector and Index signals from the A cable to the B cable.

B.1 CDC 9762

Remove (Ch. I)	Add (Ch. I)
B01-06B to JA82-18B	B01-06B to JA82-43B
B01-06A to JA82-18A	B01-06A to JA82-44A
B01-05B to JA82-25B	B01-05B to JA82-45B
B01-05A to JA82-25A	B01-05A to JA82-45A

Remove (Ch. II)	Add (Ch. II)
B03-06B to JA83-18B	B03-06B to JA83-43B
B03-06A to JA83-18A	B03-06A to JA83-44A
B03-05B to JA83-25B	B03-05B to JA83-45B
B03-05A to JA83-25A	B03-05A to JA83-45A

Rework transmitter card FTVV in location B01 (Ch. I) and B03 (Ch. II). Locate jumper at center bottom of board (as viewed with connector on the right). Remove jumper and reinsert one set of holes lower (i.e., from center hole to hole below original jumper). Remove the letter "F" from the card type designation FTVV and mark a "G" in its place so that the card type becomes GTVV.

NOTE - On later models of the 9762, CDC will ship units with an enhancement feature which will allow easy switchover to the B cable as follows: Remove the jumper plug on (B07) of the logic chassis backpanel.

B.2 CDC 9730

Rework transmitter-receiver card CFAX in location A04 (Ch. I) and B04 (Ch. II). When viewing card with connector on the right, locate four jumpers to the left of the I/O connectors and above the terminator ground lug. The bottom end of the jumpers must be removed from the holes to which they are soldered and moved to the holes immediately above. Next, find the small jumper to the right of the third IC from the connector edge of the board on the bottom row of ICs. This jumper must be removed and reinserted so that it connects the top and middle holes rather than the original connection of the bottom and middle. This connection ungates the sector and index driver.

Remove the letter "C" from the card type designation CFAX and mark a "D" in its place so that the card type becomes DFAX.

B.3 CDC 9766

Remove (Ch. I)		Remove (Ch. II)	
Sector +	J4-55	Sector +	J4-55
Sector -	J4-25	Sector -	J4-25
Index +	J4-48	Index +	J4-48
Index -	J4-18	Index -	J4-18

Move Wire (Ch. I)	Orgin	From	To
Sector +	PA01-5B	J3-55	J2-26
Sector -	PA01-5A	J3-25	J2-13
Index +	PA01-6B	J3-48	J2-24
Index -	PA01-6A	J3-18	J2-12

Move Wire (Ch. II)	Orgin	From	To
Sector +	PA03-5B	J3-55	J2-26
Sector -	PA03-5A	J3-25	J2-13
Index +	PA03-6B	J3-48	J2-24
Index -	PA03-6A	J3-18	J2-12

Rework transmitter card FTVV in location A01 (Ch. I) and A03 (Ch. II). Locate the jumper at center bottom of board (as viewed with connector on the right). Remove jumper and reinsert one set of holes lower (i.e., from center hole to hole below original jumper). Remove the letter "F" from the card type designation FTVV and mark "G" in its place so that the card type becomes GTVV.

NOTE - On later models of the 9766, CDC will ship units with an enhancement feature which will allow easy switchover to the B cable as follows: Cut the cable tie securing PD90 to the I/O cable and plug PD90 into JD90 pins 13 and 14 (Ch. I) and pins 11 and 12 (Ch. II) as indicated on the top of the connector.

B.4 CDC 9448

Sector and Index are on both the A and B cables.

B.5 TRIDENT DRIVES

Sector and Index are on both the A and B cables.

B.6 FUJITSU DRIVES

Sector and Index are on both the A and B cables.

B.7 AMPEX CAPRICORN

To place the sector and index signals on both the A and B cables make the following jumper connections on the I/O board: E1 to E2, E3 to E4, E5 to E6 and E7 to E8.

APPENDIX C

OPERATION OF DIAGNOSTICS

C.1 INTRODUCTION

The following is a step-by-step procedure for running the DEC RH750 and RM03/RM05/RM80 diagnostics. Emulex recommends running the diagnostic programs in the order presented (skip the programs not intended for your drive). Additional information on the Diagnostic Supervisor and running of the diagnostic programs can be found in the "VAX Diagnostic System User's Guide" (DEC Publication No. EK-VX11D-UG-001) or by typing HELP when in the Diagnostic Supervisor.

NOTES

Only standard size drives can be run with DEC diagnostics. For non-standard sizes, Emulex's Formatter and Reliability tests must be used.

The DEC Formatter Diagnostic, EVRAC, must be revision 5.2 or above. Older versions of the diagnostic have a bug which will not allow the bad block file to be written as required when using non-DEC media. EVRAC's revision level may be checked by running the diagnostic as described below. After EVRAC has been loaded, the diagnostic will identify itself and its revision.

C.2 LOADING AND STARTING

To allow the diagnostic supervisor to be booted on a command from the system consol, the consol must be in the consol I/O mode (indicated by a >>> prompt). If that prompt is not present, type CTRL P. That will place the consol in the I/O mode. To boot the diagnostic supervisor turn the BOOT DEVICE switch on the CPU panel to the proper position for the boot device to be used and then type B or B/10 in the case of the system disk. Once the diagnostic supervisor has been loaded it will prompt with DS>.

If the supervisor was booted from a cassette, remove the cassette from the drive and replace it with the cassette that contains the RH750 diagnostics.

The Massbus Adaptors (RH0, RH1 or RH2) and drives to be tested (DRBn) must be ATTACHed to inform the diagnostic supervisor of their presence and type.

1. ATTACH the RH750 (SC750): specify its device type (RH750), its link to the CPU (CMI), its generic device name and address (RH0, RH1 or RH2) and BR level (5):

```
DS>  ATTACH RH750 CMI RH1 5
```

2. ATTACH the disk drive: specify the type (RM03, RM05 or RM80), link to the CPU (RH0, RH1 or RH2) and generic device name (DBB0, DBB1, DBB2 or DBB3):

```
DS>  ATTACH RM03 RH1 DBB0
```

You must ATTACH a Massbus Adaptor in order to ATTACH a drive that is connected to it even if you do not intend to run diagnostics on the adaptor. One ATTACH statement is required for each device. Substitute the appropriate variable for each new statement.

After ATTACHing the group of devices to be tested, you must SELECT the specific devices that are to be tested.

3. SELECT the Massbus Adaptor to be tested: use its generic device name:

```
DS>  SELECT RH1
```

4. SELECT the disk drive to be tested: use its generic device name:

```
DS>  SELECT DBB0
```

All devices that are to be tested must be SELECTed using individual SELECT statements. When more than one device of the same type has been SELECTed, tests run against that type of device are run sequentially, lowest numbered device first.

To allow the operator to monitor the progress of the testing, the trace option can be SET. For diskless and functional diagnostics this greatly increases test time.

5. SET the trace option:

```
DS>  SET TRACE
```

The next step is to LOAD the diagnostics. The default load device is the device from which the supervisor was booted.

6. LOAD a diagnostic program (in this case ECCAA) is as follows:

```
DS>  LOAD ECCAA
```

Only one program may be LOADed at a time.

Once LOADed, the program may be STARTed (or restarted) in any section or test any number of times (without redoing any of the the above operations).

7. START the test that is currently in memory by typing:

```
DS>  START
```

   All tests and/or sections will be run one time.

8. START the diagnostic: specify the TEST number(s) to be run by typing:

```
DS>  START/TEST:first:last
```

   Substitute the decimal number of the first test to be run for the word first and the number for the last test to run for the word last. All of the tests between those two numbers will be run. To run only one test, the first and last numbers are the same.

9. START the diagnostic: specify the TEST numbers and to specify the number of PASSes of all the tests selected by typing:

```
DS>  START/TEST:first:last/PASS:n
```

   Substitute a decimal number for the letter n.

10. START the diagnostic: specify a SECTION name by typing:

```
DS>  START/SECTION:name
```

   Substitute the name of a SECTION of the diagnostic for the word name.

The program can be returned to the Diagnostic Supervisor by typing CTRL C. The program may then be aborted by typing ABORT or the program can be resumed (after possible flag changing) by typing CONT.

C.3 ECCAA - RH750 DIAGNOSTIC

To run this diagnostic SELECT the appropriate RH750 (RH0, RH1 or RH3). It is not necessary to ATTACH or SELECT a drive.

This diagnostic provides for functional verification and testing of the RH750 Massbus Adapter (MBA) portion of the controller. Much of the diagnostic makes use of the Diagnostic Register which simulates signals from the Massbus. Since the SC750 does not have an actual Massbus, it is not possible to run those test which make use of the Massbus simulation function. Tests 1-3, 5-6 and 11 will run without error and test the MBA controller registers and the map registers. Test 11 requires drive 0 to be on line.

C.4 EVRDA - RM03/5 RM80 DISKLESS DIAGNOSTIC

This diagnostic is a stand alone program which uses functional and diagnostic means to verify the operability of the controller independently of the drive.

Part of this diagnostic operates the drive in diagnostic mode which is not implemented in the SC750. Therefore, only tests 1-23 will run without error if the controller is operational. Tests 1-23 can be run with the drive cycled down. The functions performed by this diagnostic are very limited and do not involve any data transfers.

C.5 EVRAC VAX (RM03/5) DISK FORMATTER

The formatter consists of six sections made up of one or more common parts or tests. When the formatter is started, the initialization code requests a channel be assigned for the selected disk, builds a device dependent table and then reads the homeblock. If the pack is labeled SCRATCH the program will proceed. If the program is unable to read the homeblock or the pack is not labeled SCRATCH the user will be asked whether to proceed or not.

Initialization adjusts QIO buffer sizes dependent on which mode the program is running in. If the program is running in user mode under VMS the buffer size will be set to 35 pages. This will allow one track transfers for the largest disk. If the program is running in stand-alone the buffer size will be set to 110 pages. This will allow multi-track transfers.

The following is a description of each of the sections:

PACKINIT

This section formats and writes a bad sector file with zero entries on all sectors of the last track. The section then reads the bad sector file and verifies that the file conforms to the proper format and that all physical disk addresses are within the limits of the drive. (If the file cannot be read or is corrupt the program will be aborted).

After successfully reading the bad sector file, the disk pack is formatted a track at a time. At the completion of the format process a write/read sequence is performed on every sector of the disk pack. During this surface analysis any bad sector discovered is flagged and added to the bad sector file. The homeblock is written with the name SCRATCH in a form that allows disk diagnostics to see a valid label name, but makes the homeblock appear invalid to VMS.

This section should never be run unless the user has verified that the disk subsystem is functioning correctly and that the bad sector file is indeed missing or corrupt. This section will have to be used on all foreign packs and on those packs that have not had bad

sector files previously written on the pack. The user should be aware that the updated bad sector file is not written on the pack until the end of the verify operation.

FORMAT

This section reads and validates the bad sector file. If the file cannot be read or is corrupt the program will abort. After successfully reading the bad sector file the disk pack is formatted a track at a time. At the completion of the format process a surface analysis is performed and any bad sector discovered is flagged and added to the bad sector file. The homeblock is written with the name SCRATCH.

VERIFY

This section reads and validates the bad sector file. (If the file cannot be read or is corrupt the program will be aborted.) After successfully reading the bad sector file the disk pack is surface analyzed, and any bad sector discovered is flagged and added to the bad sector file. The homeblock is written with the name SCRATCH.

The user should be aware that the updated bad sector file is not written on the pack until the end of the verify section.

READALL

This section reads every sector on a pack and prints any data errors found in a head map error report. On a known good disk drive, this section can be used to search for data errors on a pack. Conversely, using a known good pack or one with known errors, this section can be used to check the read capability of the drive.

FLAGBAD

This section allows the user to manually update the bad sector file. The section prompts the user for the address of the bad block. After the user has selected all the bad blocks he wishes to flag, the program re-writes the bad block file and clears the bad sector flag in the header word of the bad block. The program then re-writes the homeblock to destroy the file directory. This is done to ensure that no files will contain holes. The program then reads the bad block file and displays its contents.

This section should not be used unless the user is familiar with the structure of the bad sector file and understands the significance of updating the file. Any data on the disk will not be preserved. The homeblock is re-written with the name SCRATCH.

HELP

This is the default section. Section names are identified along with their function.

Program and Event Flags

Quick - The quick flag reduces the number of data patterns used in verify from three to one.

Event Flag 23 - Causes the starting disk address to be printed for each step in a section.

Event Flag 22 - Causes the starting disk address to be printed once every 100 cylinders.

Event Flag 21 - Causes error messages to be printed in brief format.

Event Flag 20 - Causes single track transfers in the surface analysis test (stand-alone mode only).

Format and Verify Time

Drive	Normal	Quick
RM03	14 min.	7 min.
RM05	60 min.	37 min.

C.6 EVRDB - VAX RM03/5 FUNCTIONAL

The program contains a set of 40 tests which will verify the integrity of the controller and drives under test. The set of tests included are: data transfer tests, seek tests, timing tests, and manual intervention tests. Tests 34-37 are manual intervention tests and are invoked by running the section called MANUAL.

The program requires that there be a scratch pack mounted and online.

C.7 EVRGA - RM80 FORMATTER

The function of this program is to format the RM80 HDA. EVRGA is a section selectable formatter rather than test selectable to prevent accidental destruction of data. When the formatter is started, the initialization code requests that a channel be assigned for the selected disk, builds a device dependent table and then reads the homeblock. If the pack is labeled SCRATCH the program will proceed. If the program is unable to read the homeblock or if the pack is not labeled SCRATCH, the program will ask if you wish to override the protection check. If the program is running under VMS, the buffer will be set to 35 pages. This will allow one track transfers of the largest disk. If the program is running stand-alone the buffer size will be set to 110 pages. This will allow multi-track transfers (up to 3 tracks on an RM80).

The following is a description of each of the seven sections:

HDAINIT

This section will first ask the user which files are to be initialized, the skip sector file or the bad sector file. Once this has been determined the track that the file resides on is formatted and a zero entry bad or skip sector file is written and verified.

This section should never be run unless the user has verified that the disk subsystem is functioning correctly and that the bad or skip sector file is indeed missing or corrupt. This section will have to be used on all foreign HDA's and on those HDA's that have not had a bad sector file previously written on the HDA. The bad sector file and the skip sector file must have the same serial number.

FORMAT

This section reads and validates both sector files. (If the files cannot be read or are corrupt the program will abort). After successfully reading both the sector files, the disk HDA is formatted a track at a time. A surface analysis is performed at the completion of the format process, and any bad sector discovered is flagged and added to the bad sector file or the skip sector file. This is dependent on the error type and position. The homeblock is written with the name SCRATCH.

VERIFY

This section reads and validates both sector files. (If the files cannot be read or are corrupt the program will be aborted.) After successfully reading the bad sector and skip sector files, the disk pack is surface analyzed and any bad sector discovered is flagged and added to the bad sector file or skip sector file. This is dependent on the error type and position of the error. The homeblock is written with the name SCRATCH.

The user should be aware that the updated bad sector file is not written on the pack until the end of the verify section.

READALL

This section reads every sector on the HDA and prints any data errors found in a head map error report. On a known good drive, this section can be used to search for data errors on a HDA. Conversely, using a known good HDA or one with known errors, this section can be used to check the read capability of the drive and controller.

UPDATE

This section allows the user to manually update the bad sector file or skip sector file. The section prompts the user for the address of the bad block. After the user has selected all the bad blocks he wishes to flag, the program re-writes the bad block file or skip sector file. This section should not be used unless the user is familiar with the skip sectoring algorithm incorporated by the RM80. The user must also understand the structure of the bad sector file and the significance of updating the file. Any data on the disk will not be preserved.

REBUILD

This section allows the user to rebuild a bad or skip sector file should one become destroyed. First the track where the selected file is located is formatted, then a zero entry file is written on that track. From this point on the procedure is in accordance with the Update section.

HELP

This is the default section. Section names are identified along with their function.

Program and Event Flags

Quick - The quick flag reduces the number of track reads from five to one.

Event Flag 23 - Causes the starting disk address to be printed for each step in a section.

Event Flag 22 - Causes the starting disk address to be printed once every 100 cylinders.

Event Flag 21 - Causes error messages to be printed in brief format.

Event Flag 20 - Causes single track transfers in the surface analysis test (stand-alone mode only).

Event Flag 19 - Causes only the FE cylinders to be formatted.

Event Flag 18 - Causes FORMAT section to bypass verification.

Format and Verify Time

Drive	Normal	Quick
RM80	33 min.	16 min.

C.8 EVRGB - RM80 FUNCTIONAL DIAGNOSTIC

The program contains a set of 40 tests which verify the integrity of the controller and drives under test. The set of tests includes: data transfer tests, seek tests, timing tests and manual intervention tests. The tests require that the drive be online. Test 40 is a manual intervention test which is invoked by running the section called MANUAL.

C.9 EVRAA - RM DISK RELIABILITY TEST

The program requires that a formatted pack (or HDA) be on each drive under test. The packs should not be "mounted". Each pack must have a volume name of SCRATCH or DIAGNOSTIC. If either name is not recorded on the pack's home block, the program will abort any further activities on all drives. If the pack is not formatted or it is desired to run the test using a pack with some other volume name, then the appropriate formatter program must be run first. The formatter program will give the volume a name of SCRATCH after the format operation is complete.

The following paragraphs describe the various sections to this diagnostic. Only one section is run for each START.

QUALIFICATION

This section will issue each of the drive functions to ensure that the drive(s) under test will support all of the drive commands. After all non-data transfer functions have been tested the test will issue a write, write-check and read sequence to a group of disk addresses. The goal of the read/write portion of this test is to access a sector on every cylinder of every track without destroying the homeblock or the bad block file located on the last track of the last cylinder. The test must complete in less than a minute.

SEEK TIMING

This section will perform seeks between cylinder 0 and following cylinders: 1, 2, 4, 8, 16, 32, 64, 128, 256 and 512. Each seek range is timed and an average time is calculated. The results are presented.

MEDIA TEST

This section will write and write check every sector on the disk using an entire track for each operation. Any block in error will not be reported if it is in the bad block file located on the last track of the last cylinder. Five patterns are written onto each sector over the entire disk pack. Each pattern consists of a quadword which is replicated 64 times in each sector. The patterns used are:

1. F00FF00FF00FF00F ;worst case for RH750
2. EC6DEC6DEC6DEC6D ;worst case for media
3. A5A5A5A5A5A5A5A5 ;alternating ones and zeros
4. 123456789ABCDEF0
5. FEDCBA9876543210

After all sectors have been written using the above patterns, the test enters a random mode where random patterns are written to random disk addresses.

MULTI-DRIVE TEST

This section will test up to eight drives by transferring random data to random disk addresses for all selected drives at the same time. That is, all transfers are issued in parallel for those drives attached to the controller. The function sequence is:

1. Drive clear
2. Write random data
3. Write check data
4. Read data
5. Data compare

NOCUSTOMER TEST

This test is the same as the multi-drive test except that on an RM80 fixed media drive the entire physical area of the media is used and not just the FE cylinders.

CONVERSATION MODE

The conversation mode section is a set of routines designed to allow the user to design and run simple tests with a minimum of difficulty. The program prompts the user on the information needed to customize the test. Data pattern code 3 selects random data. Functions may be a sequence of READ, WRITE, etc. and must end with END.

Running default disk addresses will eventually destroy the homeblock and the bad sector file. Errors occurring in sectors which are flagged in the bad sector file are not inhibited as is the case with the multi-drive test.

Appendix D

VAX NUMBERS QUICK REFERENCE

780 Base Address	750 Base Address
20008000 - TR4	F28000 MBA 0
2000A000 - TR5	F2A000 MBA 1
2000C000 - TR6	F2C000 MBA 2
2000E000 - TR7	
20010000 - TR8	
20012000 - TR9	
20014000 - TR10	
20016000 - TR11	

Internal Register Byte Offsets (Hex)

00 - MBA Configuration/Status Register (MBA CSR) [780 only]
04 - MBA Control Register (MBACR)
08 - MBA Status Register (MBASR)
0C - MBA Virtual Address Register (MBAVAR)
10 - MBA Byte Count Register (MBABCR)
14 - MBA Diagnostic Register (MBADR)
18 - MBA Selected Map Register (MBASMR) [780 only]
1C - MBA Command Address Register (MBACAR)

800 to BFC - MBA Map Registers

External (Drive) Register Byte Offsets (Hex)

Register	0	1	2	3	4	5	6	7
Control/Status1 - RMCS1	400	480	500	580	600	680	700	780
Drive Status - RMDS	404	484	504	584	604	684	704	784
Error 1 - RMER1	408	488	508	588	608	688	708	788
Maintenance1 - RMMR1	40C	48C	50C	58C	60C	68C	70C	78C
Attention Summary - RMAS	410	490	510	590	610	690	710	790
Disk Address - RMDA	414	494	514	594	614	694	714	794
Drive Type - RMDT	418	498	518	598	618	698	718	798
Look Ahead - RMLA	41C	49C	51C	59C	61C	69C	71C	79C
Serial Number - RMSN	420	4A0	520	5A0	620	6A0	720	7A0
Offset - RMOF	424	4A4	524	5A4	624	6A4	724	7A4
Desired Cylinder - RMDC	428	4A8	528	5A8	628	6A8	728	7A8
Holding - RMHR	42C	4AC	52C	5AC	62C	6AC	72C	7AC
Maintenance 2 - RMMR2	430	4B0	530	5B0	630	6B0	730	7B0
Error 2 - RMER2	434	4B4	534	5B4	634	6B4	734	7B4
ECC Position - RMEC1	438	4B8	538	5B8	638	6B8	738	7B8
ECC Pattern - RMEC2	43C	4BC	53C	5BC	63C	6BC	73C	7BC

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