TC05

(TS11 COMPATIBLE)

TAPE COUPLER

TECHNICAL MANUAL

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TC0551001 Rev C
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WARNING

This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with instructions in this technical manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of Federal Communications Commission (FCC) Rules, which are designed to provide reasonable protection against such interference when operating in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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Emulex Corporation assumes no responsibility for any errors which may appear in the manual.

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EMULEX PRODUCT WARRANTY

TAPE COUPLER/CONTROLLER WARRANTY: Emulex warrants for a period of twelve (12) months from the date of shipment that each Emulex tape controller product supplies shall be free from defects in material and workmanship.

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Section 1
INTRODUCTION

1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the TC05 Tape Coupler for Magnetic Tape Cartridge Subsystems manufactured by Emulex Corporation. In addition, this manual provides diagnostic and applications information.

For reference convenience, this section is divided into five subsections as listed in the following table:

Subsection	Title
1.1	Scope
1.2	Overview
1.3	Features
1.4	Functional Compatibility
1.5	Specifications

1.2 OVERVIEW

The TC05 tape coupler is a single printed circuit board assembly (PCBA) designed to be embedded in a Digital Equipment Corporation (DEC) LSI-11 central processing unit (CPU). The TC05 tape coupler emulates the DEC TS11 Tape Coupler and is intended for use with the Control Data Corporation (CDC) 9219X family of Magnetic Tape Cartridge Subsystems. These peripheral subsystem devices operate in a serpentine sequential streaming recording mode.

1.3 FEATURES

The TC05 tape coupler includes five features that enhance performance and versatility.

1.3.1 MICROPROCESSOR DESIGN

The TC05 tape coupler design incorporates a unique high-speed, bipolar, eight-bit microprocessor that performs most of the coupler functions. Using the microprocessor reduces the component count, provides high reliability and easy maintainability, and enables a single set of hardware to be adapted to a wide range of emulation capabilities through the flexibility of microprogramming.

1.3.2 PACKAGING

The TC05 tape coupler is constructed on a single quad-size board. It is a four-layer PCBA that plugs directly into connectors A, B, C, and D of any Q-Bus slot in the LSI-11 CPU backplane or expansion box. No cabling is required between the CPU and the TC05 tape coupler. The TC05 tape coupler receives its power from the LSI-11 CPU backplane. One 34-conductor flat cable provides the interface between the TC05 tape coupler and the tape cartridge subsystem.

1.3.3 SELF-TEST

The TC05 tape coupler firmware includes an internal self-test routine which is automatically executed when power is first applied (Power-Up mode). This self test exercises all parts of the microprocessor, buffer, and storage-device data logic. It does not test all TC05 tape coupler circuitry, but successful execution indicates high probability that the TC05 tape coupler is operational. If the TC05 tape coupler fails the self test, the red FAULT light emitting diode (LED) on the upper edge of the PCBA is lit and the TC05 tape coupler cannot be addressed from the CPU.

1.3.4 DATA BUFFER

The TC05 tape coupler contains 3.5 kilobytes of data buffering and 500 bytes of buffering for the contents of the device registers on the TC05 tape coupler.

1.3.5 CONFIGURATION SWITCHES

Dual in-line package (DIP) switches are provided to configure the TC05 tape coupler for Q-Bus addresses, interrupt vector addresses, and operating characteristics.

1.4 FUNCTIONAL COMPATIBILITY

The TC05 tape coupler is compatible with media, address mapping, diagnostics, and operating systems to the extent described in this subsection.

1.4.1 MEDIA COMPATIBILITY

Tapes written by systems with DEC TS11 tape coupler are not interchangeable with tapes written by systems with the TC05 tape coupler.

1.4.2 ADDRESS MAPPING

One Standard or seven Alternate Tape Cartridge Subsystem Device Address(es) and interrupt vector address(es) may be mapped by the TC05 tape coupler. Addressing details are listed in Section 3, Tables 3-1 through 3-3.

1.4.3 DIAGNOSTICS

On LSI CPU systems, the TC05 tape coupler executes standard TS11 diagnostics ZTSHC0 and ZTSIB0.

1.5 SPECIFICATIONS

Specifications for the TC05 tape coupler are listed and described in Table 1-1.

Table 1-1. TC05 Tape Coupler Specifications

Parameter	Characteristics
FUNCTIONAL	
Recording Method	Streaming
Data Density	8000 bits per inch (bpi)
Number of Tape Cartridge Subsystems Supported	1
Tape Speed	55 inches per second (ips)
Data Buffering	3.5 kilobytes
Q-BUS INTERFACE	
Register Addresses	Switch selectable
Interrupt Vector Address	Switch selectable
Interrupt Priority Level	BR5
Data Transfer	DMA with word (16-bit) transfer, except for odd byte at beginning or end of data record
DESIGN	High-speed, bipolar microprocessor that uses 2901 bit-slice components
PHYSICAL	
Mounting	Any Q-Bus slot in standard DEC LSI-11 CPU backplane or expansion box
Cables	One 40-conductor flat cable and one 40-conductor, shielded round cable
ELECTRICAL	
Power Required	+5 Volts (V) ±5%, 6 Amperes (A)
Q-Bus Interface	DEC approved line drivers and receivers
Tape Cartridge Subsystem Interface	TTL compatible line drivers and receivers. Cable accumulative length to 10 feet maximum.

Table 1-1. TC05 Tape Coupler Specifications (continued)

Parameter	Characteristics
ENVIRONMENTAL	
Operating	10 to 40° Celsius (C) 50 to 104° Fahrenheit (F) 10 to 90 % relative humidity 28° C (82° F) wet bulb maximum 2° C (36° F) dew point minimum
Nonoperating	-40 to 66° C -40 to 151° F 0 to 95 % relative humidity
Altitude	2.4 kilometer (km), 8000 feet (ft) maximum, operating 9.1 km, 30,000 ft maximum, nonoperating

2.1 OVERVIEW

This section describes the physical characteristics, organization, and interfaces for the TC05 tape coupler, and is divided into four subsections as listed in the following table:

Subsection	Title
2.1	Overview
2.2	Physical Description
2.3	TC05 Tape Coupler Organization
2.4	Interfaces

2.2 PHYSICAL DESCRIPTION

The TC05 tape coupler is constructed as a single quad-size PCBA that contains all circuitry required to control one CDC 9219X Tape Cartridge Subsystem. The Emulex part number (P/N) for the TC05 Tape coupler is TU0510401. The PCBA contains interface circuitry for the Q-Bus of a DEC LSI-11 CPU and all other circuitry required for tape control, housekeeping, and Data Transfer operations.

The TC05 tape coupler PCBA is shown in Figure 2-1. The PCBA is made in four layers, with power and ground planes on the inner layers and etched interconnections on the outer layers.

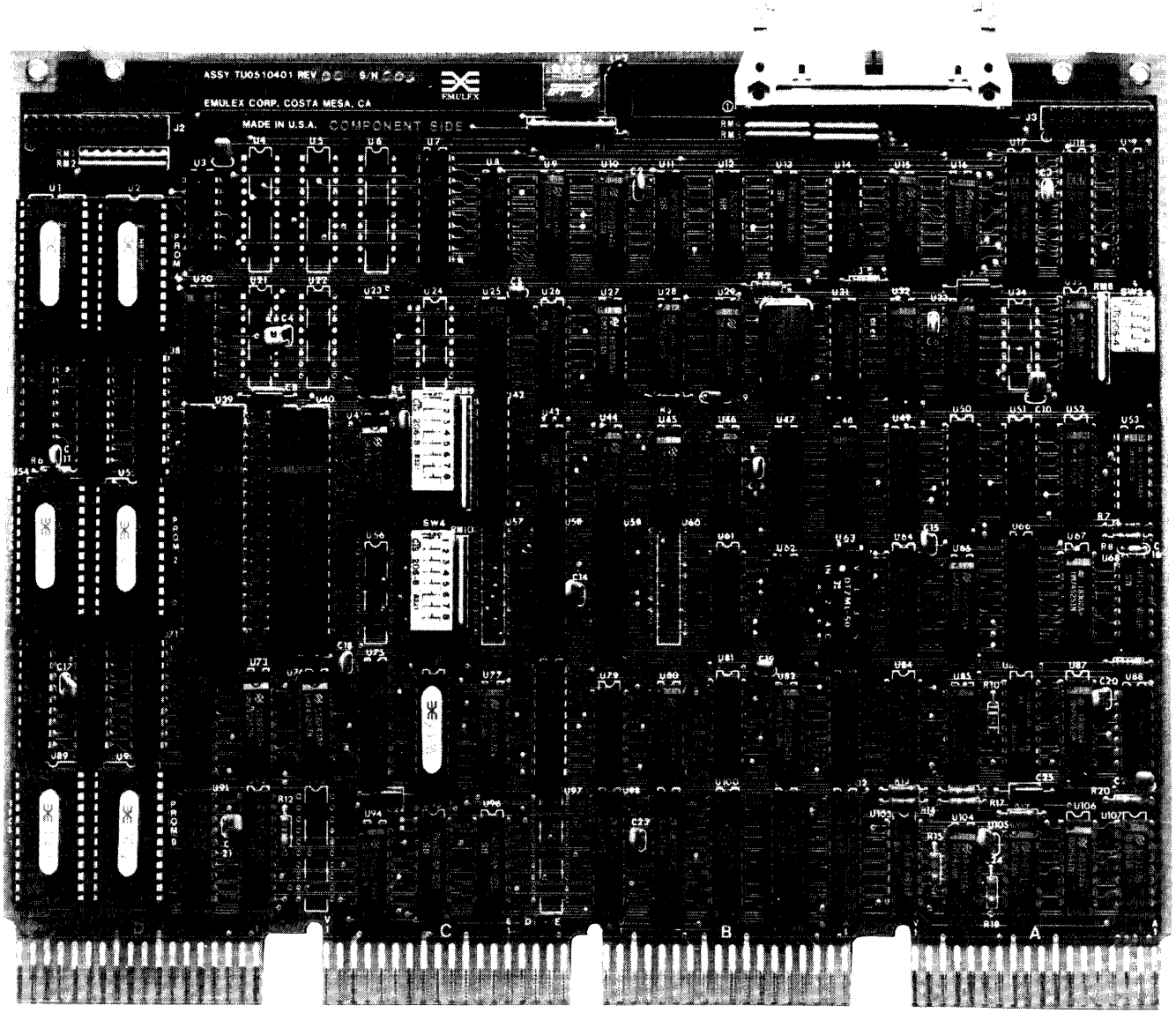
As a quad-size PCBA, the TC05 tape coupler interfaces only to connector rows A, B, C, and D on the LSI-11 CPU backplane. The 18 pins in each connector row are reference designated A through V, except letters G, I, O, and Q (from right to left) are not used. The component side of the PCBA is side 1 and the solder side is side 2.

NOTE

In this manual, directions for locating components on the PCBA assume the TC05 tape coupler is being viewed from the component side with edge connectors A, B, C, and D at the bottom.

2.2.1 TAPE SUBSYSTEM CONNECTOR

The TC05 tape coupler interfaces with the CDC 9219X Tape Cartridge Subsystem via one 40-pin flat-cable connector, reference designated J1, and located toward the right center at the top edge of the PCBA. The TC05 tape coupler can write to and read from 1/4-inch wide magnetic tape that meets American National Standards Institute



TC0501-0211

Figure 2-1. TC05 Tape Coupler for Magnetic Tape Cartridge Subsystem

(ANSI) Standard X3.55-1977. This tape is used in tape cartridges for serpentine serial recording of data on 11 tracks, as shown in Figure 2-2.

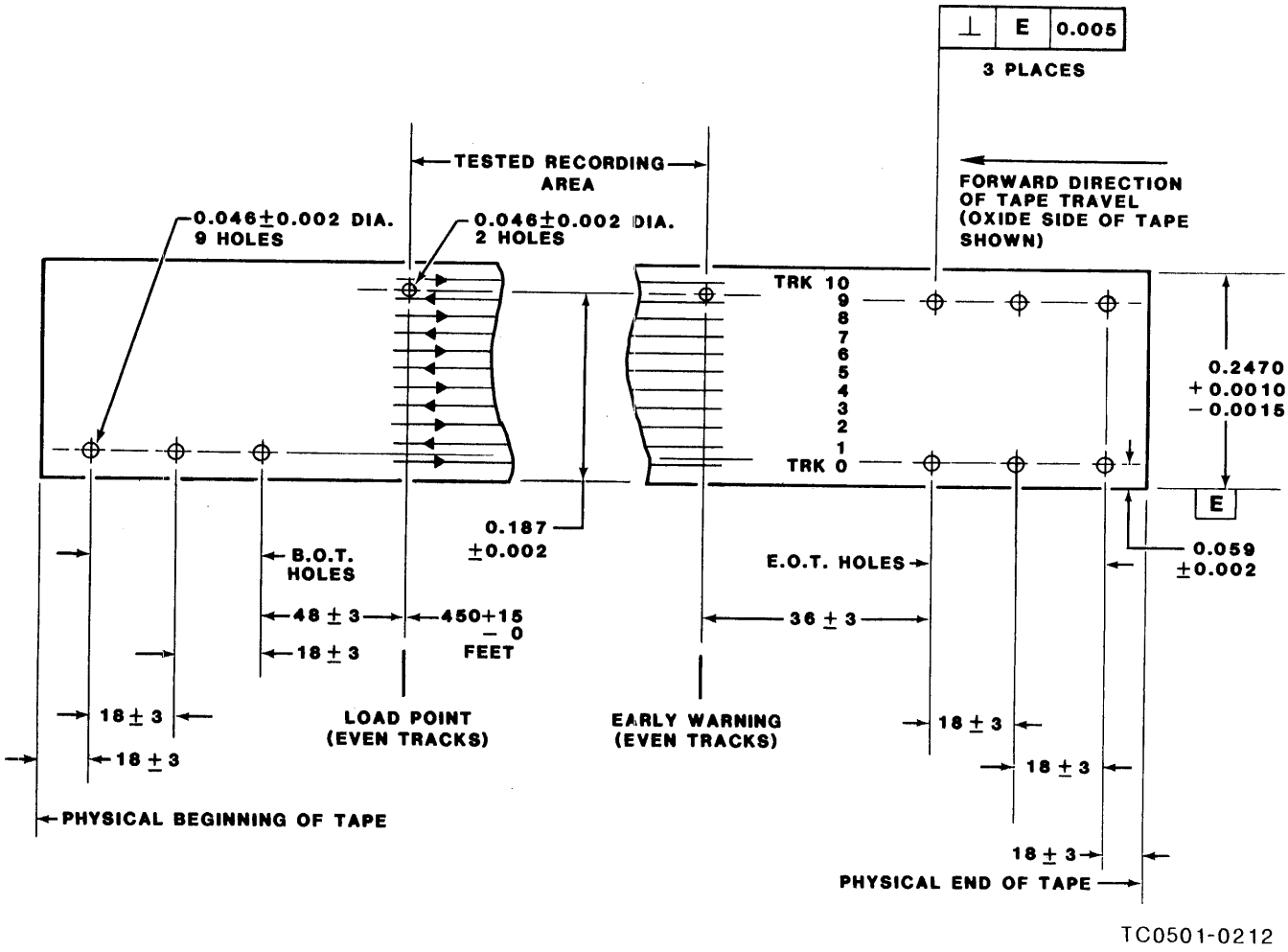


Figure 2-2. Track Pattern on Magnetic Tape Media per ANSI Standard X3.55-1977

2.2.2 TEST CONNECTORS

Two additional male flat-cable connectors, reference designated J2 and J3, are located near the top corners of the PCBA, and are used only for connecting special test panels during factory test and repair operations. Connectors J2 and J3 are not intended for use in normal operations.

2.2.3 SWITCHES

Three DIP switches are used for tape cartridge subsystem addressing, interrupt vector addressing, and selection of special options.

2.2.4 INDICATOR

An LED indicator for FAULT and ACTIVITY conditions is mounted near the center at the top edge of the PCBA (for indications, see subsection 2.4.1.5).

2.2.5 FIRMWARE PROMS

The TC05 tape coupler uses six Programmable Read-Only Memory (PROM) integrated circuits (ICs) that store the instructions which are used by the on-board microprocessor to perform the TS11 emulation (see Appendix A).

2.3 TC05 TAPE COUPLER ORGANIZATION

The TC05 tape coupler is organized around an 8-bit, high-speed, bipolar microprocessor. A simplified block diagram of the functional elements in the TC05 tape coupler is shown in Figure 2-3. The arithmetic logic unit (ALU) and the register file portion of the microprocessor are implemented with two 2901 bit-slice IC components. The microinstruction code is 48 bits long, and the 2048-word control memory is implemented by six 2K x 8-bit PROMs.

2.3.1 RAM BUFFER

The TC05 tape coupler incorporates a 4K X 8-bit high-speed RAM buffer which temporarily stores (buffers) the contents of the TC05 tape coupler's device registers plus 3.5 kilobytes of data.

2.3.2 DATA AND CONTROL REGISTERS

The Write Data Register (WDR) holds the eight bits of data to be transferred to the tape media, and the Read Data Register (RDR) receives the nine data bits from the tape media. The Control Register latches internal microprocessor control signals plus the external signals that are used to control the Tape Cartridge Subsystem. The status signals from the Tape Cartridge Subsystem are testable signals to the microprocessor.

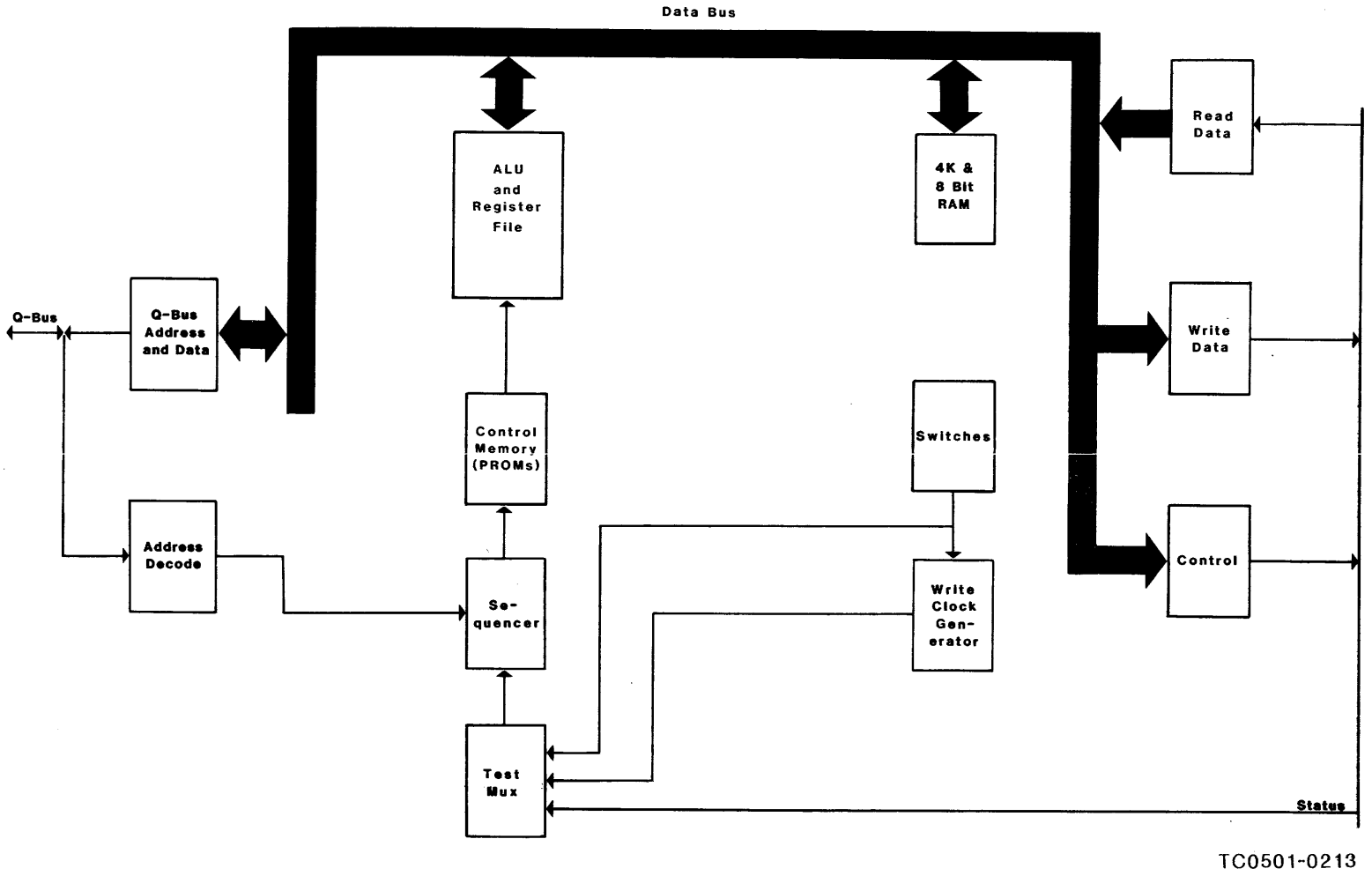


Figure 2-3. TC05 Tape Coupler, Simplified Block Diagram

2.3.3 MICROPROCESSOR RELATIONSHIPS

The microprocessor responds to all programmed input/output (I/O) and carries out the I/O functions required for the addressed register in the TC05 tape coupler. The microprocessor also controls all NPR operations and transfers data between the Q-Bus data lines and the tape cartridge subsystem via its own internal buffer.

2.4 INTERFACES

The TC05 tape coupler interfaces with one Tape Cartridge Subsystem via a 40-conductor flat cable connected to connector J1 on the TC05 tape coupler PCBA. It interfaces with the LSI-11 CPU via the Q-Bus.

2.4.1 Q-BUS INTERFACE

The Q-Bus between the LSI-11 CPU and the TC05 tape coupler contains 42 bidirectional signal lines and two unidirectional signal lines on connectors A and B, and two unidirectional signal lines on connector C. Q-Bus interface pin assignments are listed and described in Table 2-1. These signal lines provide the means by which the LSI-11 CPU and the TC05 tape coupler communicate with each other. The Q-Bus interface is used for programmed I/O, CPU interrupts, and NPR Data Transfer operations. Addresses, data, and control information are sent along these signal lines, some of which contain time-multiplexed information. The Q-Bus interface lines are grouped in the following categories:

a. Twenty-two Data/Address lines - <BDAL00:BDAL21>. The four Data/Address lines which carry the most significant bits (MSB) are lines BDAL21:BDAL18. They are used for addressing only and do not carry data. Lines BDAL17 and BDAL16 reflect the parity status of the 16-bit data word during a Write or Read Data Transfer operation via the Q-Bus cycle.

b. Six Data Transfer Control lines - BBS7, BDIN, BDOUT, BRPLY, BSYNC, and BWTBT.

c. Six Direct Memory Access (DMA) Control lines - BDMR, BSACK, BDMGI, and BDMGO (connectors A and C).

d. Seven Interrupt Control lines - BEVNT, BIAKI, BIAKO, BIRQ4, BIRQ5, BIRQ6, AND BIRQ7.

e. Five System Control lines - BDCOK, BHALT, BINIT, BPOK, and BREF.

Table 2-1. Q-Bus Interface Pin Assignments

Connector A Signal			Connector B Signal		
Component Side	Pin	Solder Side	Component Side	Pin	Solder Side
BIRQ5	A	+5V	BDCOK	A	+5V
BIRQ6	B		BPOK	B	
BDAL16	C	0V (GND)	BDAL18	C	0V (GND)
BDAL17	D		BDAL19	D	
	E	BDOUT	BDAL20	E	BDAL02
	F	BRPLY	BDAL21	F	BDAL03
	H	BDIN		H	BDAL04
0V (GND)	J	BSYNC	0V (GND)	J	BDAL05
	K	BWTBT		K	BDAL06
	L	BIRQ4		L	BDAL07
0V (GND)	M	BIAKI	0V (GND)	M	BDAL08
BDMR	N	BIAKO	BSACK	N	BDAL09
BHALT	P	BBS7	BIRQ7	P	BDAL10
BREF	R	BDMGI	BEVNT	R	BDAL11
	S	BDMGO		S	BDAL12
0V (GND)	T	BINIT	0V (GND)	T	BDAL13
	U	BDAL00		U	BDAL14
	V	BDAL01		V	BDAL15

Connector C Signal			Connector D Signal		
Component Side	Pin	Solder Side	Component Side	Pin	Solder Side
	A	+5V		A	+5V
	B			B	
	C	0V (GND)		C	0V (GND)
	D			D	
	E			E	
	F			F	
	H			H	
0V (GND)	J		0V (GND)	J	
	K			K	
	L			L	
0V (GND)	M	BIAKI	0V (GND)	M	
	N	BIAKO		N	
	P			P	
	R	BDMGI		R	
	S	BDMGO		S	
0V (GND)	T		0V (GND)	T	
	U			U	
	V			V	

All signals, except BDCOK and BPOK, are low active.

2.4.1.1 Interrupt Priority Level

The TC05 tape coupler is hardwired to issue both level 4 and level 5 interrupt requests. The level 4 request is necessary to allow compatibility with either an LSI-11 or LSI-11/2 CPU.

2.4.1.2 Register Address

The register address (1777XXXX) and the eight registers assigned to the TC05 tape coupler are decoded by a PROM (reference designated U104). The selections available are determined by configuration DIP switch pack SW1 (see Section 3).

2.4.1.3 DCOK and INIT Signals

The DCOK and INIT signals can each perform a Controller Clear operation. The Self-Test function is performed only when DC power is initially applied (Power-Up mode).

2.4.1.4 FAULT and ACTIVITY Indications

The LED indicator indicates FAULT and ACTIVITY conditions that may have the following causes:

a. When the TC05 tape coupler is reset (SW1-1 ON), or if a Power-Up sequence occurs on the system in which the TC05 tape coupler is installed, the TC05 tape coupler executes a self test of its internal logic. The self test takes only a fraction of a second, but during the self testing the LED is lit. After the self test is completed successfully, the LED is extinguished.

b. If self test fails, the LED remains continuously lit and the CPU cannot communicate with the TC05 tape coupler because the registers in the TC05 tape coupler remain inaccessible. The defective TC05 tape coupler must then be removed and replaced or must be repaired before the system can be functional.

NOTE

The TC05 tape coupler continuously polls the tape cartridge subsystem connected to it to determine subsystem status at all times.

c. The LED illuminates during Data Transfer operations to and from the tape cartridge subsystem. This LED illumination provides a visual indication of system activity.

2.4.1.5 NPR Operations

All DMA Data Transfer operations are performed under microprocessor control. When doing a Read from memory operation, a check is made for memory parity errors and if an error is detected, the Q-Bus Parity Error (UPE) error status bit is set.

2.4.2 TAPE CARTRIDGE SUBSYSTEM INTERFACE

Interface between the TC05 tape coupler and the Tape Cartridge Subsystem is provided by a flat cable with 20 twisted pairs of conductors. The cable has a 40-pin flat-cable connector at each end. One end of the cable connects to connector J1 on the TC05 tape coupler PCBA and the other end of the cable connects to a mating connector on the Tape Cartridge Subsystem. Pin assignments for this interface are listed and described in Table 2-2.

The signals at the TC05 tape coupler and Tape Cartridge Subsystem interface are grouped into three categories:

a. Device Control Signals

b. Device Status Signals

c. Data Transfer Signals.

NOTE

The signals described in the following subsections are asserted when set to logic 1 state by +5 Vdc unless otherwise specified.

2.4.2.1 Device Control Signals

Device control signals are transferred on six lines:

a. RESET - halts any in-progress command execution and places the tape cartridge subsystem in a known state. The RESET signal is asserted for a minimum of four microseconds and a maximum of 25 microseconds. No commands can be transferred within two milliseconds after RESET is negated.

b. CB0 through CB3 - provide a code to indicate which command is to be executed upon completion of the Command Transfer operation. Codes and commands are listed in Table 2-3.

c. CGATE - initiates the Command Transfer operation. Asserting the CGATE signal line indicates the contents of the Command Bus are valid. The Command Transfer operation is acknowledged when the Tape Cartridge Subsystem asserts the CACK line.

Table 2-2. TC05 Tape Coupler and Tape Cartridge Subsystem Interface

Signal	Name	J1 Pin Number	To/From
FMD	File Mark Detect	1	To
DER	Data Error Flag	3	To
BSY	Device Busy	5	To
RDATA	Read Data	7	To
RDY	Ready	9	To
INT	Interrupt	11	To
RGATE	Read Gate	13	To
DCLCK	Data Clock	15	To
CACK	Command Acknowledge	17	To
TR10	Track Number 10	10	To
RESET	Reset	19	From
WDATA	Write Data	21	From
WGATE	Write Gate	23	From
CB0	Command Bus 0	25	From
CGATE	Command Gate	27	From
CB1	Command Bus 1	29	From
CB3	Command Bus 3	31	From
CB2	Command Bus 2	33	From
LDSW	Load Switch	35	To
WP LED	Write Protect LED	37	From
RDY LED	Ready LED	38	From
FLT LED	Fault LED	39	From

All even-numbered pins, except pins 10 and 38, are ground (GND).
To = From Tape Cartridge Subsystem to TC05 tape coupler.
From = From TC05 tape coupler to Tape Cartridge Subsystem.

2.4.2.2 Device Status Signals

Device status signals are transferred on six lines:

a. BSY - indicates a function is in progress on the Tape Cartridge Subsystem. No Command Transfer operation can occur while BSY is asserted. Functions include command execution, positioning, cartridge initialization and health checks.

b. RDY - indicates the tape cartridge is loaded and initialized. The only commands that can be acknowledged without the RDY line active are Read Sense and Device Health Check commands. All other commands are rejected if RDY is not asserted.

Table 2-3. Command Bus Signal Decoding

CB3	CB2	CB1	CB0	Command
0	0	0	0	Not used
0	0	0	1	Device Health Checks
0	0	1	0	Reserved for future use
0	0	1	1	Read Sense
0	1	0	0	Read
0	1	0	1	Search File Mark
0	1	1	0	Read File
0	1	1	1	Backspace
1	0	0	0	Write
1	0	0	1	Write File Mark
1	0	1	0	Cartridge Check
1	0	1	1	Erase
1	1	0	0	Reserved for future use
1	1	0	1	Rewind
1	1	1	0	Restore
1	1	1	1	Reserved for future use

c. INT - indicates an abnormal condition has occurred. The cause for INT assertion is transferred via a Read Sense command. The Read Sense command serves as an INT Acknowledge; therefore, when a Read Sense command is issued, the INT line is cleared.

d. FMD - indicates a File Mark has been detected during a Read operation. The FMD signal is dynamic and is asserted while Read operation is in progress, if applicable. FMD is negated before the command in progress is terminated; i.e., before BSY is cleared.

e. DER - is asserted when a Write or Read operation is terminated, if a data error has been detected during the readback. If DER is asserted at command termination, Error Recovery procedures must be initiated.

f. CACK - acknowledges validity and acceptance of a command and indicates a Command Transfer operation has begun.

2.4.2.3 Data Transfer Signals

Data Transfer signals are conducted on five signal lines:

a. DCLK - is a device-sourced signal that strobes the current data over the interface. During a Write or Read operation, DCLK runs at the nominal data-transfer rate. During a Read Sense operation, DCLK runs at the nominal sense data-transfer rate.

b. WGATE - is an input signal generated by the host LSI-11 CPU. It is used as a Data Envelope signal to establish data record boundaries.

c. RGATE - is an output signal that is similar to WGATE. It is also used as a Data Envelope signal to establish data record boundaries.

d. WDATA - is an input signal generated by the host LSI-11 CPU. It is asserted at the active edge of the subsequent DCLK pulse and it represents the next data bit to be transferred to the tape.

e. RDATA - is an output signal that is similar to the WDATA signal, except it is asserted at the active edge of the subsequent DCLK pulse and it represents the next data bit to be transferred from the tape to the TC05 tape coupler.

2.4.2.4 Control/Indicators on Emulex Bezel

Three LED indicators and one control switch on the optional Emulex Bezel (operator control panel) installed on the Sentinel tape transport perform the following functions:

a. RDY LED (**READY**) - When +5 Vdc is applied on this signal line, this LED is lit to indicate a tape cartridge is loaded, and the Sentinel is in On-Line mode and not busy.

b. WP LED (**WRITE PROTECT**) - When +5 Vdc is applied on this signal line, this LED is lit to indicate the tape cartridge is write protected.

c. FLT LED (**FAULT**) - When +5 Vdc is applied on this signal line, this LED is lit to indicate an error condition exists in the Sentinel tape cartridge transport.

d. **LOAD** Switch - After an Unload command is executed by the subsystem, the RDY LED signal level drops from +5 Vdc to 0 Vdc, the READY LED is extinguished, and remains extinguished while the subsystem is in the Off-Line mode. Pressing the LOAD switch allows the system to return to the On-Line mode, provides +5 Vdc to the RDY LED signal line, and the READY LED is lit again. Removing and reinserting the cartridge causes the same effects as pressing the LOAD switch, except the cartridge goes through a retensioning cycle.

3.1 OVERVIEW

This section describes the step-by-step procedure for installation of the TC05 Tape Coupler for Magnetic Tape Cartridge Subsystems in an LSI-11 CPU System. To serve as an outline of this installation procedure, this section is divided into seven subsections, as listed in the following table:

Subsection	Title
3.1	Overview
3.2	Inspection
3.3	Tape Cartridge Subsystem Preparation
3.4	LSI-11 CPU Preparation
3.5	TC05 Tape Coupler Configuration
3.6	TC05 Tape Coupler Installation
3.7	Diagnostics

Emulex recommends this section be read in its entirety before installation procedures are begun.

3.1.1 MAINTAINING FCC CLASS A COMPLIANCE

Emulex has tested the TC05 tape coupler PCBA with DEC computers that comply with FCC Class A limits for radiated and conducted radio-frequency interference (RFI).

Each TC05 tape coupler PCBA complies with FCC regulations and is designed to be embedded in an LSI-11 CPU cabinet. When properly installed, the TC05 tape coupler system does not cause compliant computers to exceed RFI limits for Class A equipment.

There are two possible configurations in which the tape transports for the TC05 tape coupler system can be installed:

a. In the same cabinet as the DEC CPU and TC05 tape coupler.

b. In an expansion cabinet that is separate from the cabinet in which the CPU and TC05 tape coupler are installed.

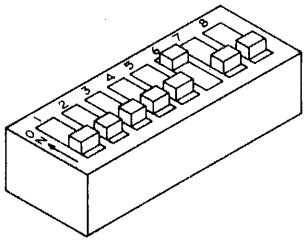
To limit radiated RFI, DEC completely encloses the computer system components, that could radiate or conduct RFI, with a grounded metal shield. When installing the system components, do nothing that could reduce the effectiveness of the shield. That is, when installation of the TC05 tape coupler system is complete, no gap in the shielding that would allow RFI radiation or conduction can be allowed.

Conducted RFI is generally prevented by installing a filter in the ac line between the computer system and the ac source. Most power distribution panels of current manufacture contain suitable filters.

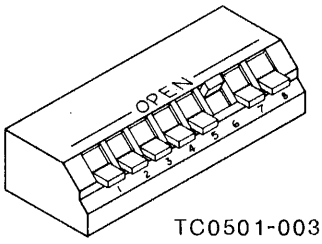
The procedures required to maintain shield integrity and to limit radiated and conducted RFI are explained fully in subsection 3.6.

3.1.2 DIP SWITCH TYPES

DIP switches used in this product may be either of two types shown in Figure 3-1.



Slide Switch:
To place a slide switch in the ON position, simply slide the switch in the direction marked ON or CLOSED. To place a slide switch in the OFF position, simply slide the switch in the direvtion marked OFF or OPEN.



TC0501-0034

Piano Switch:
To place a piano switch in the ON position, press the switch. To place a piano switch in the OFF position, raise the switch.

Figure 3-1. DIP Switch Types

Switch-setting tables in this manual use the numeral one (1) or the letter (C) to indicate the ON (CLOSED) position and the numeral zero (0) or the letter (O) to indicate the OFF (OPEN) position.

3.2 INSPECTION

Emulex products are shipped in special containers designed to provide full protection under normal transit conditions. Immediately upon receipt, the shipping container should be inspected for evidence of possible damage incurred in transit. Any obvious damage to the container, or indications of actual or probable equipment damage, should be reported to the carrier company in accordance with instructions on the form included in the container.

After unpacking the TC05 tape coupler, visually inspect the entire assembly for bent or broken connector pins, damaged components, or other visual evidence of physical damage. The PROMs should be carefully examined to ensure each is firmly and completely seated in its socket. Verify that the TC05 tape coupler model or part number designation, revision level, and serial number agree with those on the shipping invoice. This verification is important to confirm warranty. If evidence of physical damage or identity mismatch is found, notify an Emulex representative immediately.

3.3 TAPE CARTRIDGE SUBSYSTEM PREPARATION

Unpack and install the Tape Cartridge Subsystem as instructed in the manufacturer's manual. Position and level it in its final place before beginning installation of the TC05 tape coupler. This positioning allows I/O cable routing and length requirements to be accurately determined.

Configure the Tape Cartridge Subsystem for desired operating mode by using appropriate switches on operator control panel (OCP) of the Tape Cartridge Subsystem, or by issuing appropriate commands via software. (See manufacturer's technical manual.)

3.4 LSI-11 CPU PREPARATION

Power down the system and switch OFF the main AC breaker. Remove the side covers from the CPU and otherwise make the LSI-11 accessible.

3.5 TC05 TAPE COUPLER CONFIGURATION

Configuration setup is made by setting switches in DIP switch packs SW1, SW3, and SW4. The configuration of the TC05 tape coupler must be established before it is installed on the Q-Bus in the LSI-11 CPU chassis because the configuration switches are not accessible when the TC05 tape coupler is installed in the LSI-11 CPU. TC05 tape coupler component locations are shown in Figure 3-2.

The switches are factory preset for operation at standard Device Address 17772520 and Interrupt Vector Address 224. Emulex recommends these settings be used for initial checkout.

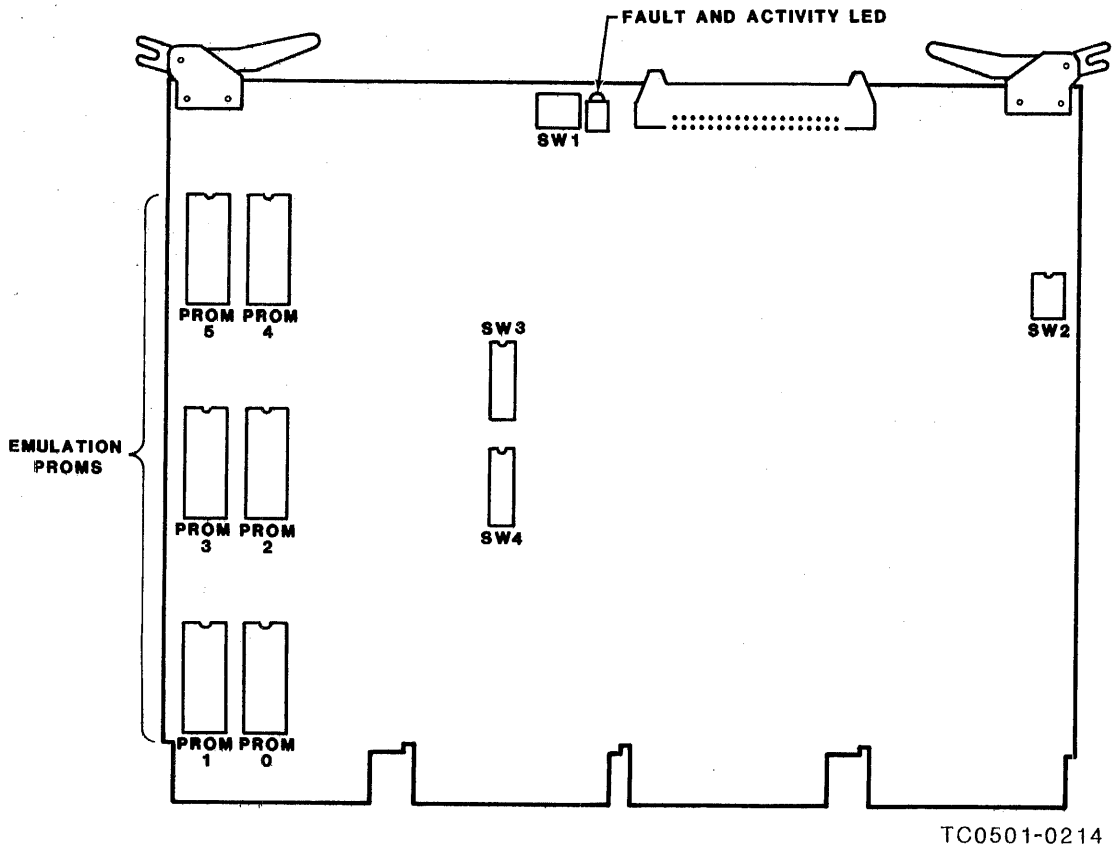


Figure 3-2. TC05 Tape Coupler, Component Locations

NOTE

If any switch position is changed on the TC05 tape coupler, the TC05 tape coupler must be reset by using switch SW1-1 or by removing and then restoring power to the TC05 tape coupler. This Reset operation is required because the switches are read by an Initialization routine in the firmware of the TC05 tape coupler.

Table 3-1 lists and describes the function and factory configuration of all switches in the DIP switch packs on the TC05 tape coupler. Tables 3-2 and 3-3 list and define address decoding switch settings. In all DIP switches, ON is the closed position of the switch and OFF is the open position of the switch. Unless otherwise stated, the ON position enables the applicable function and the OFF position disables that function.

Table 3-1. TC05 Tape Coupler DIP Switch Settings

Switch	OFF (0)	ON (1)	Factory Setting	Function	Sub-Section
SW1-1	Normal Run	Halt/ Reset	OFF (0)	Tape Coupler Run or Halt	3.5.3.1
SW1-2	Disable	Enable	OFF (0)	Extended Gap	3.5.3.2
SW1-3	Disable	Enable	OFF (0)	Checksum	3.5.3.3
SW1-4	Disable	Enable	OFF (0)	22-Bit Addressing	3.5.3.4
SW3-1	---	---	OFF (0)	Not used[1]	
SW3-2	Disable	Enable	ON (1)	Interrupt Vector Address decode bits 02 through 08 ON or OFF, as applicable (see Table 3-2).	3.5.1 and 3.5.2
SW3-3	Disable	Enable	OFF (0)		
SW3-4	Disable	Enable	ON (1)		
SW3-5	Disable	Enable	OFF (0)		
SW3-6	Disable	Enable	OFF (0)		
SW3-7	Disable	Enable	ON (1)		
SW3-8	Disable	Enable	OFF (0)		
SW3-9	---	---	OFF (0)	Not used[1]	
SW3-10	---	---	OFF (0)	Not used1[1]	
SW4-1	Disable	Enable	ON (1)	Device Address Select[2]	3.5.1
SW4-2	Disable	Enable	OFF (0)	Dev. Add. Sel.[2]	3.5.1
SW4-3	Disable	Enable	OFF (0)	Dev. Add. Sel.[2]	3.5.1
SW4-4	Disable	Enable	OFF (0)	Dev. Add. Sel.[2]	3.5.1
SW4-5	Disable	Enable	OFF (0)	Device Address Bank Select[2]	3.5.2
SW4-6	Disable	Enable	ON (1)	Device Address Bank Select[2]	3.5.2
SW4-7	Disable	Enable	ON (1)	PROM Select ON = 1K, OFF = 2K	3.5.3.5
SW4-8	Disable	Enable	OFF (0)	Tape Transport Operation Select. OFF enables operation with CDC Sentinel standard version 92192. ON enables operation with CDC Sentinel version 92192-02.	3.5.3.6

[1] Not used switches MUST BE OFF.
[2] See Table 3-3.

Table 3-2. Interrupt Vector Address Decode Example

Switch SW3-	8	7	6	5	4	3	2
Switch Setting	O	C	O	O	C	O	C
Address Bit	08	07	06	05	04	03	02
Binary	0	1	0	0	1	0	1
Interrupt Vector Address in Octal		2			2		4

Table 3-3. Device Address Decode Switch Settings

	SW4						
Address	1	2	3	4	5	6	7
17772520*	C	O	O	O	O	C	O
17772524	C	O	O	O	C	O	O
17772440	O	C	O	O	O	C	O
17772444	O	C	O	O	C	O	O
17776300	O	O	C	O	O	C	O
17776304	O	O	C	O	C	O	O
17777460	O	O	O	C	O	C	O
17777404	O	O	O	C	C	O	O

*Standard

3.5.1 TC05 TAPE COUPLER ADDRESS SELECTION

All Q-Bus coupler devices have a block of several command and status registers through which the LSI-11 CPU system can command and monitor the TC05 tape coupler. These registers are sequentially addressed, beginning with a starting Device Address assigned to the particular coupler device.

DIP switch pack SW4 is used to select the starting address to which the TC05 tape coupler is to respond. The standard starting Device Address is 17772520. The TC05 tape coupler can be addressed at any of three addresses, but only one address can be made available at any time. At least one switch of the select switches in the DIP switch pack must be closed to obtain response from the TC05 tape coupler. Table 3-3 lists the starting Device Addresses that can be selected by the switches in DIP switch pack SW4.

3.5.2 INTERRUPT VECTOR ADDRESS SELECTION

DIP switches SW3-2 through SW3-8 are used to select the Interrupt Vector Address for the TC05 tape coupler. The Interrupt Vector Address switching is explained in Table 3-2. The standard Interrupt Vector Address is 224.

3.5.3 OPTION SELECTION

There are a number of other TC05 tape coupler options that can be selected by the user. They are placed in effect by physically installing the option on the PCBA, or by setting the appropriate DIP switches.

CAUTION

Some manufacturers of Q-Bus backplanes omit 22-bit addressing capability and use the four lines that would be assigned for such addressing as power lines. In such systems, the 2908 IC should not be installed in IC socket U101 because that IC and possibly other circuitry would be destroyed by heat.

3.5.3.1 Halt/Reset Option

DIP switch SW1-1 allows selection of the Halt/Reset option. When enabled, normal running of the tape transport is halted, the TC05 tape coupler is reset and initialized, and the tape on the tape transport is rewound to the BOT position.

3.5.3.2 Extended Gap Option

DIP switch SW1-2 allows selection of the Extended Gap option. When enabled, a fixed-length gap of 3.5 inches is written to each record when another Write command is not issued before approximately six milliseconds has elapsed. If a Write command is written before the six milliseconds has elapsed, a normal 0.6-inch gap is made. The Extended Gap feature allows better streaming operation in applications where operating software is not always able to keep the Sentinel tape cartridge transport streaming.

NOTE

This feature may dramatically reduce storage capacity of the tape cartridge if an Extended Gap is generated for each record written.

3.5.3.3 Checksum Option

DIP switch SW1-3 allows selection of the Checksum option. When enabled, a Checksum of the written data is written as the last byte of each record. When the record is read back, a Checksum is generated and compared with the Checksum written on the tape.

NOTE

If a tape is read with Checksum switch ON but the Write operation was performed without writing the Checksum, errors are generated when the record is read. Also if a tape is read with Checksum switch OFF but the Write operation included a Checksum, errors are generated when the record is read.

3.5.3.4 Twentytwo-Bit Memory Addressing Option

The TC05 tape coupler can include the 22-Bit Memory Addressing option. Programming instructions for this option are included in Section 4. The option kit is Emulex P/N SC0213102, which consists of a single AMD2908 IC installed in IC socket U101 (see Appendix A).

To remove a replaceable IC from an IC socket and to install an IC in an IC socket, use the following procedure:

a. Remove installed IC from its socket by using an IC puller or equivalent tool.

b. Check separation distance of two parallel rows of pins on IC to be installed. If pin rows are too far apart to allow IC to fit in IC socket, perform step c, otherwise go to step d.

c. Grasp IC at its ends between thumb and forefinger, press one row of pins on one side against a table top or other firm flat surface, and gently bend that row of pins inward enough to allow IC to fit intended socket.

d. Orient IC so that pin 1 is at upper left when inserting IC. Identity method for pin 1 depends on IC manufacturer. Pin 1 end of IC is usually indicated by a cut or molded pattern in top of IC casing.

e. Carefully insert IC in socket. Verify IC is seated firmly and that no pins are bent or misaligned.

3.5.3.5 PROM Size Select Option

DIP switch SW4-7 allows the user to select a 1K or 2K PROM. When the 1K PROM is selected, switch SW4-7 must be enabled (ON). When the 2K PROM is selected, switch SW4-7 must be disabled (OFF). Switch SW4-7 should be left ON (closed).

3.5.3.6 Tape Transport Select Option

DIP switch SW4-8 allows compatibility the CDC Sentinel tape transport. When the CDC Sentinel standard version 92192 tape transport is used, switch SW4-8 must be OFF. When the CDC Sentinel version 92192-02 tape transport is used, switch SW4-8 must be ON. If SW4-8 is ON, SW1-2 must be OFF.

3.6 TC05 TAPE COUPLER INSTALLATION

The TC05 tape coupler can fit into any Q-Bus quad slot on the LSI-11 CPU backplane. Before selecting the Q-Bus quad slot for the TC05 tape coupler, system hierarchy and architecture **must** be examined to ensure proper priority sequence and backplane continuity. The TC05 tape coupler can buffer up to 3.5 kilobytes of data; therefore, it requires less direct memory access (DMA) priority than controller devices that contain less buffering and need higher priority for faster access to prevent early buffer overrun. Controllers with RK, RL, or TM11 emulations require higher priority than the TC05 tape coupler. The TC05 tape coupler must be installed in a Q-Bus quad slot that accommodates devices with less DMA priority than such controllers.

DMA continuity can be ensured by leaving no empty Q-Bus quad slots between PCBAs in the backplane. Several methods of preserving DMA continuity are available. For specific information applicable to the DMA continuity requirements, refer to the Backplane or CPU User's Guide.

C A U T I O N

To avoid potential circuit damage, always turn computer power OFF before installing or removing any PCBA.

3.6.1 RFI SUPPRESSION

Limits for electrical RFI are governed by requirements of the Federal Communications Commission (FCC). Paragraphs in subsection 3.6 describe the features, use, and installation of the RFI-suppression devices, manufactured by Emulex Corporation, to meet FCC requirements.

The TC05 tape coupler is designed to be installed in a system where all system components (CPU, tape coupler, and tape transports) are mounted in the same equipment cabinet. In such a system, no special RFI-suppression devices are required because the equipment cabinet furnishes all needed RFI suppression.

3.6.2 EQUIPMENT CABINET

The equipment cabinet in which the computer equipment is installed should be a standard LSI-11 CPU equipment cabinet, completely enclosed by metal. To ensure proper shielding of all equipment in the cabinet, all outer walls of the cabinet must be free from holes, except small perforations for air exhaust are permitted.

If shield integrity is maintained, no other steps are necessary to ensure RFI shield compliance for the cabinet. Conducted RFI should be prevented by the line filters that are installed by DEC in the power distribution panel for the CPU cabinet.

If the tape transport that is to be interfaced with the TC05 tape coupler PCBA is installed in a separate cabinet from that of the CPU, that expansion cabinet must prevent RFI radiation by being shielded in the same way the DEC CPU cabinet is shielded. Also, the cable that connects to the interface in the CPU cabinet must be shielded, since it is external to the shielded cabinet environment. In an expansion cabinet, conducted RFI on the ac line to the internal power supply must be prevented, so a power distribution panel with a line filter must be installed. A typical adequate filter is the Model 1020 EMI Filter, manufactured by Filter Concepts Corporation and included in the Model MDP110 Power Supply manufactured by Marway Products, Incorporated. **Compliance with RFI-suppression requirements in such nonstandard installations must be the responsibility of the user.**

3.6.3 INSTALLATION PROCEDURE

To install the TC05 tape coupler PCBA and related cabling, see Figure 3-3 and use the following procedure:

a. Open rear door or panel of CPU equipment cabinet.

b. Select CPU Q-Bus quad slot of appropriate DMA priority (see subsection 3.6).

c. Unplug other modules in CPU backplane, if necessary, to make room for TC05 tape coupler PCBA in selected Q-Bus quad slot. Reinstall removed modules in other Q-Bus quad slots on CPU backplane, but preserve DMA continuity so no empty slots between modules occur. Use DMA Continuity PCBA to fill empty slots (if needed).

d. Insert TC05 tape coupler PCBA edge connectors A through D into selected Q-Bus quad slots A through D on CPU backplane with component side of PCBA facing in same direction as other modules in backplane. Verify PCBA is properly positioned in throat of connector slots before attempting to seat PCBA.

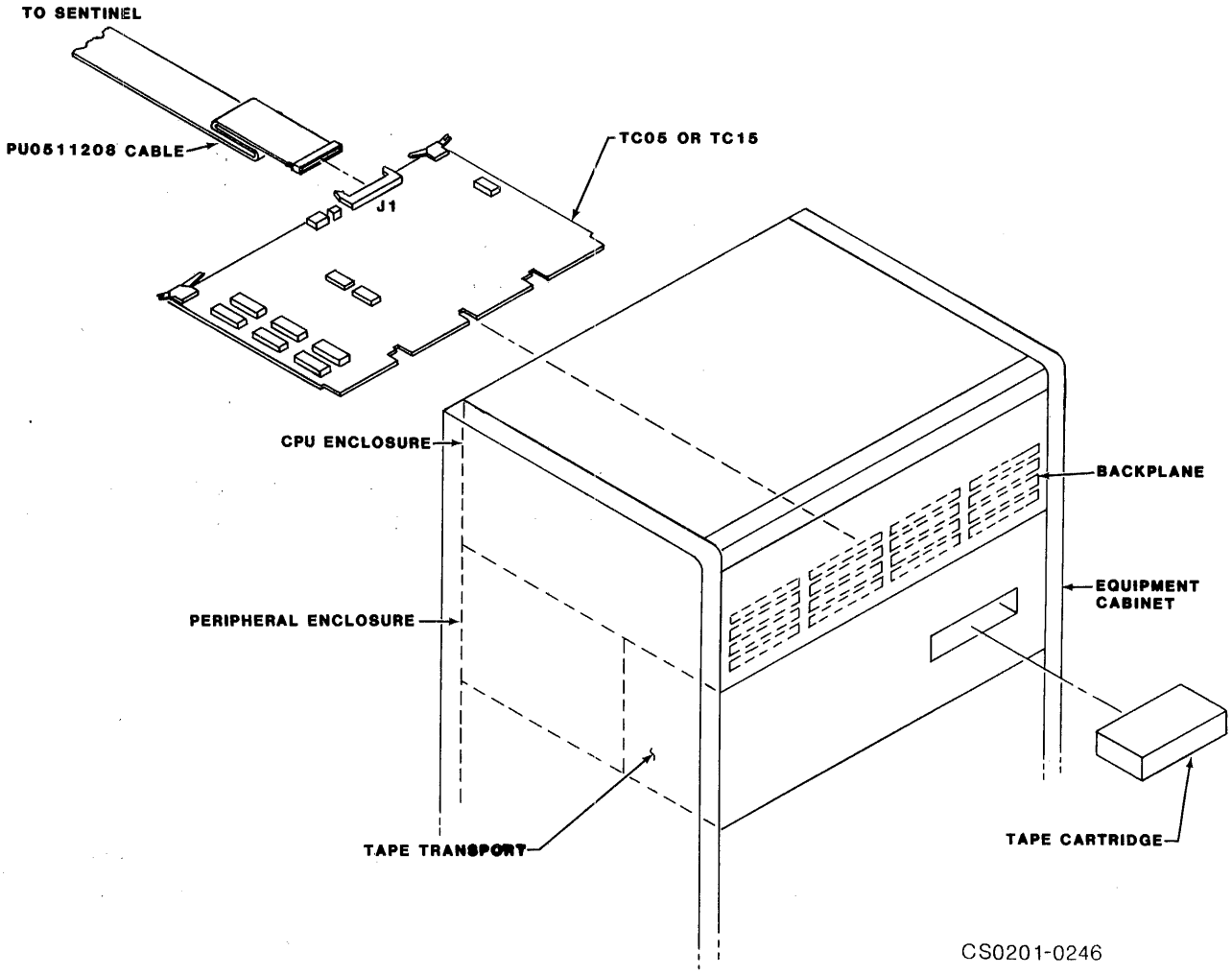


Figure 3-3. TC05 Tape Coupler Installation and Cabling

C A U T I O N

Pins in cables **must** be aligned correctly before loading a cartridge or tape may unwind past BOT or EOT when system is operated.

e. Align arrow on header of connector for 40-conductor flat cable with arrow on header of connector J1 on TC05 tape coupler PCBA. Arrow identifies pin 1 on each connector. Push cable connectors together to make firm connection.

f. Align arrow on header of six-conductor flat cable for Emulex Bezel with arrow on header of connector J1 on Emulex Bezel. Arrow identifies pin 1 on each connector. Push cable connectors together to make firm connection. Ignore this step if system lacks Emulex Bezel.

g. Align arrow on header of tape transport end of 40-conductor interface cable with arrow on header of mating connector on tape transport. Arrow identifies pin 1 on each connector. Push cable connectors together to make firm connection.

h. Verify tape transport is terminated as instructed in manufacturer's technical manual for tape transport.

i. Close CPU equipment cabinet and turn CPU system power ON.

j. Run diagnostics (see subsection 3.7).

Emulex furnished interface cables, Bezel and related hardware can be ordered from your Emulex sales representative or directly from the factory. The factory address is:

Emulex Corporation
In-House Sales
3545 Harbor Boulevard
Costa Mesa, CA 92626
(714) 662-5600 TWX 910-595-2521

3.6.4 GROUND STRAPS

For proper operation of the tape transport subsystem, the tape transport must have a sure ground connection to the chassis ground of the computer. This ground connection should be made with metal braid at least 1/4-inch wide (preferably insulated) or with AWG No. 10 wire or larger.

NOTE

Failure to observe proper grounding methods can result in marginal operation with random-error conditions.

3.7 DIAGNOSTICS

To verify proper system operation, run the following LSI-11 diagnostics:

ZTSIB0 Subsystem Repair Tests 1 through 3

ZTSHC0 Reliability Diagnostic

These diagnostics can be run without patching.

3.7.1 DIAGNOSTIC INSTRUCTIONS

Instructions for running the diagnostics is provided in the following example that applies to starting the ZTSIB0 diagnostic. In this example, the prompt is shown in regular type and the user response is shown in **bold** type.

At dot (.) prompt, type:

.R ZTSIB0 <cr>

At DR> prompt, type:

DR>**STA/TEST:1-3/FLA:PNT <cr>**

Do you wish to change hardware? **Y <cr>**

UNITS **1 <cr>**

UNIT 0 CSR=17772522 **<cr>**
VEC=224 **<cr>**

Do you wish to change software? **N <cr>**

Test runs. After two passes, type:

^Y (CTRL C)

At DR> prompt, type:

DR>**EXIT <cr>**

At . prompt, type:

.R ZTSHC0 <cr>

At DR> prompt, type:

DR>**STA/TEST:1-2/FLA:PNT <cr>**

Do you wish to change hardware? **Y <cr>**

UNITS **1 <cr>**
UNIT 0 CSR=17772522 **<cr>**
VEC=224 **<cr>**

Do you wish to change software? **Y <cr>**

The diagnostic program then asks a series of questions. Type **<cr>** in response to all questions except the third question which asks:

Do you want to print recoverable errors? **Y <cr>**

The test then begins running. The test numbers are printed as each test is run. The test may be stopped at any time by typing:

^Y (CTRL C)

At DR> prompt, type:

DR>**EXIT<cr>**

3.7.2 BOOTSTRAP INSTRUCTIONS

The hand bootstrap instructions for the TS11 emulation should be entered via the optical display terminal (ODT) on the console. Each entry follows an @ prompt symbol:

@17772522/100001<cr>
@/100001<cr>
@R0/0<cr>
@R1/17772522<cr>
@R4/2020<cr>
@2000/46523<cr>
@R7/0<cr>
@P<cr>

4.1 OVERVIEW

This section describes and defines the bit functions in the various registers, describes Command Packet formats and processing, and explains programming concepts used with the TC05 tape coupler. This section is divided into four subsections, as listed in the following table:

Subsection	Title
4.1	Introduction
4.2	Coupler Registers
4.3	Command Packet Processing
4.4	Programming Operations

4.2 COUPLER REGISTERS

Eight tape transport device registers are included in the TC05 tape coupler and their use is compatible with DEC TS11 definitions. The eight tape transport device registers are listed in the following table:

Register	Name
TSBA	Q-Bus Base Address Register
TSDB	Q-Bus Data Buffer
TSSR	Status Register
RBPCR	Residual Frame Count Register
XST0	Extended Status Register Zero
XST1	Extended Status Register One
XST2	Extended Status Register Two
XST3	Extended Status Register Three

For quick reference, Figure 4-1 shows the entire register set.

4.2.1 Q-BUS BASE ADDRESS REGISTER (TSBA)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Memory Address															

4.2.2 Q-BUS DATA BUFFER (TSDB)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
15	14	13	12	11	10	09	08	07	06	05	04	03	02	17	16

4.2.3 STATUS REGISTER (TSSR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SC	UPE	0	RMR	NXM	NBA	A17	A16	SSR	OFL	0	0	TC2	TC1	TC0	X

4.2.4.1 RESIDUAL FRAME COUNT REGISTER (RBPCR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Residual Frame Count															

4.2.4.2 EXTENDED STATUS REGISTER ZERO (XST0)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TMK	RLS	LET	RLL	WLE	NEF	ILC	ILA	MOT	ONL	IE	VCK	PED	WLK	BOT	EOT

4.2.4.3 EXTENDED STATUS REGISTER ONE (XST1)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	0	0	0	0	0	0	0	0	0	0	0	0	0	UNC	0

4.2.4.4 EXTENDED STATUS REGISTER TWO (XST2)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OPM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-1. TC05 Tape Coupler Registers (SH1 of 2)

4.2.4.5 EXTENDED STATUS REGISTER THREE (XST3)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	OPI	REV	0	DCK	0	0	RIB

Figure 4-1. TC05 Tape Coupler Registers (SH 2 of 2)

The tape transport has two Q-Bus word locations which are used to access device registers. The base address, when written to, is the Q-Bus Data Buffer (TSDB). The base address, when read, is the Q-Bus Address Register (TSBA). The second device register (base address plus two) is the Status Register (TSSR). Writing to the TSSR causes a subsystem Initialize command to be executed and reading from the TSSR contents provides the CPU with device status information.

The TSDB is the only register that is written to during normal operations. DATO or word access must be used to properly write Command Pointers into the TSDB. DATOB or byte access to the TSDB causes maintenance functions to be performed.

Commands are not written to the tape transport's Q-Bus registers. Instead, command pointers, which point to a Command Packet somewhere in CPU memory space, are written to the TSDB. The Command Pointer is used by the tape transport to retrieve the words in the Command Packet. The words in the Command Packet instruct the tape transport to perform a certain function. The words in the Command Packet also contain any function parameters such as bus address, byte count, record count, and modifier flags.

4.2.1 Q-BUS BASE ADDRESS REGISTER (TSBA)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Memory Address															

The TSBA is a Read-only 16-bit register that is read at the base address of the tape transport (1777XXXX). Its contents reflect the least significant 16 bits of the 18-bit TSDB (TSDB bits 17 and 16 are contained in TSSR bit positions 09 and 08, respectively). The contents of TSBA are valid only after the termination of a command. (A command is initiated by loading a Command Packet address into the TSDB.) The command termination may be with or without errors. The TSBA is not cleared by power-up, subsystem INIT, or bus INIT conditions. It can also be read at any time with or without the tape transport connected in the system.

When a command execution is completed, the TC05 tape coupler deposits a Message Packet in a Message Buffer located in CPU memory. The contents of the TSBA may be read to determine the highest Message Buffer address plus two.

4.2.2 Q-BUS DATA BUFFER (TSDB)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
15	14	13	12	11	10	09	08	07	06	05	04	03	02	17	16

The TSDB is a Write-only 18-bit register that is parallel loaded from the Q-Bus at the base address. The TSDB can be loaded when the tape transport is bus slave by different types of transfers from a bus master:

a. Two transfer types are for maintenance purposes (DATOB) to high byte and DATOB to low byte).

b. The third transfer type is for Normal (word) operation (DATO).

The TSDB is not cleared on power up, subsystem INIT, or bus INIT conditions. Anytime the TSDB is written to, the tape transport responds by asserting the SSYN signal.

4.2.2.1 Normal Operation

Using a DATO, a command is issued to the tape transport by loading an 18-bit address into the TSDB. The address is that of a Command Packet located somewhere in the Q-Bus address space. The address is loaded into the TSDB by using the following format event sequence:

a. Bits <15:02> of the register are loaded with bits <15:02>, respectively from the Q-Bus.

b. Bits 17 and 16 of the address are loaded from bits 01 and 00, respectively, from the Q-Bus.

c. Bits 01 and 00 of the address are automatically loaded with zeros by the logic in the tape transport.

Loading the TSDB causes the tape transport to fetch the Command Packet from the specified address. The command defined in the Command Packet is then executed.

4.2.2.2 Data Wraparound by Using DATOB (odd)

Using DATOB to load the high byte (odd address) in the TSDB causes the following event sequence:

a. Bits <07:00> of the TSDB are loaded with bits <15:08>, respectively, from the Q-Bus.

b. Bits <15:08> of the TSDB are loaded with bits <15:08>, respectively, from the Q-Bus.

c. Bits 17 and 16 of the TSDB are loaded with bits 09 and 08, respectively, from the Q-Bus.

d. The contents of the TSDB are then loaded into the TSBA. If SSR is clear (TSSR bit 07 in zero state), an RMR error occurs (TSSR bit 12 set), but transfer is still executed and completed.

In this event sequence, the TSSR is not affected, except SSR bit 07 is cleared. To use the tape transport again, the CPU must Initialize the tape transport by writing into the TSSR.

4.2.2.3 Data Wraparound by Using DATOB (even)

Using DATOB to load the low byte (even address) in the TSDB causes the following event sequence:

a. Bits <15:00> of the TSDB are loaded with bits <15:00>, respectively, from the Unibus. (Most LSI-11 CPUs assert all zeros for bits <15:08>, except for a MOVB which extends the sign bit (bit 07) into the high byte. See the respective processor handbook for a MOVB instruction.)

b. Bits 17 and 16 cannot be determined.

c. Contents of the TSDB are then loaded into the TSBA.

To use the tape transport again, the CPU must Initialize the tape transport by writing into the TSSR.

4.2.3 STATUS REGISTER (TSSR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SC	UPE	0	RMR	NXM	NBA	A17	A16	SSR	OFL	0	0	TC2	TC1	TC0	X

The TSSR is a Read/Write 16-bit register at base address 1777XXXX+2. Its contents can be read at any time with or without the tape transport connected in the system. The TSSR can only be updated by the logic in the tape transport; it cannot be modified from the Unibus, except indirectly. (SPE, UPE, RMR, NXM, and SSR bit positions are cleared when the TSDB is written into by the host CPU.)

Any Write function written to the TSSR is decoded as a subsystem Initialize function. Initializing resets the tape transport and the TC05 tape coupler, no matter what state they are in; if the tape transport is in the On-Line mode, Initializing causes an automatic Load sequence to occur which returns the tape to the BOT position.

Bit positions <14:11> and 07 are cleared only on system power up, tape transport power up, subsystem Initialize, or at the beginning of any Write command to the TSDB. Bit positions 15 and 07 are under control of the tape transport. These bits may be set or cleared independently of any tape transport operation. Bit positions 10 and <06:00> are controlled by the tape transport and the status of these bits reflect the subsystem status.

Bits <03:01> increase status reporting capability by providing the seven Termination Class codes listed and described in Table 4-1.

Table 4-1. Termination Class Codes

TSSR Bits <03:01>	TC Code	Description
000	0	Normal termination
001	1	Attention condition
010	2	Tape status alert
011	3	Function reject
100	4	Recoverable error (tape position = one record down from start of function)
101	5	Recoverable error (tape not moved)
110	6	Unrecoverable error (tape position lost)
111	7	Fatal error (tape transport data parity error)

On fatal errors (Termination Class 7), if the Need Buffer Address bit is not set (NBA = 0), the message may be valid. If the bit is set (NBA = 1), then there was no message.

The Register Modification Refused (RMR bit 12) status does not affect the Termination Class error codes because RMR may be set on a bug-free system. The set RMR bit does set the Special Condition (SC) bit 15. This condition indicates the user may have tried to have the tape transport perform the next command while the tape transport was outputting an Attention Message (ATTN MSG) If RMR is set in the TSSR, the CPU must have written to the TSDB while a command was being executed.

The contents of the TSSR may not reflect the current state of the hardware if the ATTN bits are not enabled and the Message Buffer is not released; i.e., the tape transport may be in the Off-Line mode while the TSSR reflects the On-Line mode. To keep the TSSR up-to-date would violate Message Packet protocol.

The TSSR is not cleared immediately after Initialization. The microprocessor continues running to complete an automatic Load sequence. When the tape is at BOT, the TSSR automatically updates.

Special Condition (SC) - Bit 15

When set, SC indicates the last command was not completed without incident; either an error condition was detected or an exception condition occurred. An exception condition could be a Tape Mark on Read commands, a reverse motion attempt while tape is at BOT, EOT encountered when writing, etc.

Q-Bus Parity Error (UPE) - Bit 14

When UPE is set and TC4 or TC5 are in effect, UPE indicates the tape transport has detected a parity error in the data being transferred from the CPU memory.

Register Modification Refused (RMR) - Bit 12

RMR is set by the tape transport when a Command Pointer is loaded into the TSDB while the Subsystem Ready (SSR) bit is not set. RMR bit may be set on a bug-free system if ATTN interrupt bits are enabled.

Nonexistent Memory (NXM) - Bit 11

When NXM is set and TC4 and TC5 are in effect, it indicates an attempt has been made to transfer data to or from a memory location which does not exist. Set NXM may occur when fetching the Command Packet, fetching or storing data, or storing the Message Packet.

Need Buffer Address (NBA) - Bit 10

Set NBA bit indicates the tape transport needs a Message Buffer address. Set NBA is cleared during the Set Characteristics command if the tape transport gets valid data; it is always set after subsystem initialization.

Bus Address Bits 17:16 (A17, A16) - Bits <09:08>

The status of A17 and A16 (bits 09 and 08, respectively) display the values of bits 17 and 16 in the TSBA.

Subsystem Ready (SSR) - Bit 07

Set SSR indicates the tape transport is not busy and is ready to accept a new Command Pointer.

Off-Line (OFL) - Bit 06

Set OFL indicates the tape transport is off line and not available for any tape motion commands from the TC05 tape coupler.

Termination Class (TC02, TC01, TC00) - Bits <03:01>

These bits provide an offset value when an error or exception condition occurs during performance of a command. Each of the eight possible values in this field represents a particular class of errors or exceptions. The Termination Class (TC) codes are listed and defined in Table 4-1. TC codes are used as an offset into a dispatch table for handling the error or exception condition. These bits are valid only when SC (TSSR bit 15) is set. For details about special conditions and errors, see subsection 4.4.3.

4.2.3.1 Bootstrap Command

The TC05 tape coupler can read the bootstrapped records from bootstrapable tapes by using a special command. This special command does not require a Command Packet to be constructed.

After power-up or bus INIT, writing the value 100001 into the TSSR twice causes the TC05 tape coupler to space over the first record on the tape and read the second record into the CPU, starting at location 000000. Motion of the magnetic tape then stops. By starting the program execution at location 000000, the bootstrapped record loads the CPU with the desired program from the tape. Table 4-2 lists and describes parameters for a sample bootstrap routine. Users may write their own program if preferred.

4.2.4 EXTENDED STATUS REGISTERS

The TC05 tape coupler includes five additional registers to provide additional status information: Residual Frame Count Register (RBPCR) and Extended Status Registers Zero through Three (XST0, XST1, XST2, and XST3).

The contents of these five registers are not read directly from the registers which are accessible at the Q-Bus interface. The Message Packet, located in the system memory, contains the extended status words, and is updated at the end of a command or by using a Get Status command. A Message Buffer must be defined to the susbystem before the extended status registers are available to the software.

Table 4-2. TS11 Bootstrap Routine

Address	Data					Code
			TSBA	=	172520	TS11 ADDRESS REGISTER ADDRESS
			TSSR	=	172522	TS11 STATUS REGISTER ADDRESS
001000	1012700	172520	START:	MOV	#TSBA,R0	GET ADDRESS OF TSBA INTO R0
001004	012701	172522		MOV	#TSSR,R1	GET ADDRESS OF TSSR INTO R1
001010	005011			CLR	(R1)	INIT AND REWIND TAPE
001012	105711			TSTB	(R1)	TEST IF 'SSR' IS SET
001014	100376			BPL	.-2	AND WAIT UNTIL IT IS
001016	012710	001064'		MOV	#PKT1,(R0)	ISSUE SET-CHARACTERISTICS COMMAND
001022	105711			TSTB	(R1)	TEST IF 'SSR' IS SET
001024	100376			BPL	.-2	AND WAIT UNTIL IT IS
001026	012710	001104'		MOV	#PKT2,(R0)	ISSUE READ OF FIRST RECORD ('MM:' BOOT)
001032	105711			TSTB	(R1)	TEST IF 'SSR' IS SET
001034	100376			BPL	.-2	AND WAIT UNTIL IT IS
001036	012710	001104'		MOV	#PKT2,(R0)	ISSUE READ OF SECOND RECORD (MS:' BOOT)
001042	105711			TSTB	(R1)	TEST IF 'SSR' IS SET
001044	100376			BPL	.-2	AND WAIT UNTIL IT IS
001046	005711			TST	(R1)	ANY ERRORS ????
001050	100421			BMI	HLT	HALT IN FRONT OF MESSAGE IF ERRORS
001052	012704	001100'		MOV	#NUM+20,R4	ADDRESS OF 'NUM'-->R4
001056	005007			CLR	PC	RESUME EXECUTION AT ZERO IF NO ERRORS
			046523(OCTAL) = MS (ASCII)			
001060	046523		NUM:	046523		
001062	000000		ZIP:	0		

Table 4-2. TS11 Bootstrap Routine (continued)

Address	Data			Code
		SET CHARACTERISTICS PACKET		
001064	140004	PKT1:	140004	
001066	001074'		PK	
001070	000000		0	
001072	000010		8.	
001074	001116'	PK:	MES	
001076	000000		0	
001100	000016		14.	
001102	000000		0	
		READ-DATA PACKET		
001104	140001	PKT2:	140001	
001106	000000		0	
001110	000000		0	
001112	001000		512.	
001114	000000	HLT:	HALT	
001116		MES:		

4.2.4.1 Residual Frame Count Register (RBPCR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Residual Frame Count															

Residual Frame Count - Bits <15:00>

This register contains the octal count of residual bytes, records, Tape Marks for Read operations, space records and Skip Tape Marks commands. The contents are meaningless for all other commands.

NOTE

In this manual, Tape Mark and File Mark have the same meaning.

4.2.4.2 Extended Status Register Zero (XST0)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TMK	RLS	LET	RLL	WLE	NEF	ILC	ILA	MOT	ONL	IE	VCK	PED	WLK	BOT	EOT

The contents of Read-only register XST0 appear as the fourth word stored in the Message Buffer by the TC05 tape coupler when a command is completed or when an Attention (ATTN) condition has been detected. For Termination Class (TC) codes, see Table 4-1.

Tape Mark Detected (TMK) - Bit 15

When set, TMK causes TC2 and indicates a Tape Mark has been detected during execution of a Read, Space, or Skip command. Also set whenever a Write Tape Mark or Write Tape Mark Retry command is issued.

Record Length Short (RLS) - Bit 14

When set, RLS causes TC2 and indicates one of the following conditions:

a. During a Read operation, the record length was shorter than the byte count.

b. During a Space Record operation, a Tape Mark or BOT was encountered before the position count was exhausted.

c. During a Skip Tape Marks command execution, a BOT or double Tape Mark (if Skip Tape Marks command was issued - see Logical End of Tape bit description) was encountered before the position count was exhausted.

Logical End of Tape (LET) - Bit 13

This bit can be set only if this mode of termination has been enabled through the use of the Set Characteristics command while the Skip Tape Marks command is simultaneously in effect. When set, LET causes TC2 and indicates one of two conditions:

a. Two contiguous Tape Marks have been detected.

b. The first record encountered when moving off BOT was a Tape Mark.

Record Length Long (RLL) - Bit 12

When set, RLL causes TC2 and indicates the record read during a Read operation was longer than the specified byte count.

Write Lock Error (WLE) - Bit 11

When set with a TC3, WLE indicates a Write operation was attempted while the tape transport was Write Locked. When set with a TC6, WLE indicates the WRT LOCK switch was activated during execution of a Write operation.

Non-Executable Function (NEF) - Bit 10

When set, NEF causes TC3 and indicates a command could not be executed because of one of four conditions:

a. The command specified Reverse tape direction, but tape was already at BOT.

b. A motion command was issued while the Volume Check (VCK) bit was set (see XST0 register bit 04 description).

c. Any command, except Get Status or Drive Initialize, is issued while the tape transport is in the Off-Line mode.

d. Write-type command attempted while the tape transport was Write Locked (WLE bit set).

Illegal Command (ILC) - Bit 09

When set, ILC causes TC2 and indicates the command field or the command mode field of a command that has been issued contains codes which are not supported by the TC05 tape coupler.

Illegal Address (ILA) - Bit 08

When set, ILA causes TC3 and indicates one of three conditions:

a. The command specifies an address with more than 18 bits.

b. Register TSDB has overflowed.

c. The command specifies an odd-numbered address when an even-numbered address is required.

Motion (MOT) - Bit 07

When set while tape is moving, MOT causes TC3 and indicates tape was moved during previous operation.

On-Line (ONL) - Bit 06

When set, ONL indicates the tape transport is in the On-Line mode and operable. A change in the state of this bit causes a TC1 and an ATTN message, if the ATTN bits are enabled.

If ONL is reset, it causes a TC3 if a motion command is issued to the tape transport.

Interrupt Enable (IE) - Bit 05

The IE bit reflects the state of the Interrupt Enable condition that was supplied when the last command was issued.

Volume Check (VCK) - Bit 04

When set, VCK causes TC3 and indicates the tape transport has changed state (On-Line mode to Off-Line mode and vice versa). VCK is always set after execution of the Initialization sequence. VCK is cleared by the set state of the Clear Volume Check (CVC) bit 14 in the Command Packet Header word.

Phase Encoded Drive (PED) - Bit 03

When set, PED indicates the TC05 tape coupler and tape transport are capable of writing and reading 1600 bits per inch (bpi) Phase Encoded (PE) data. This bit should always be set.

Write Locked (WLK) - Bit 02

When set, WLK indicates the tape cartridge is write protected.

Beginning of Tape (BOT) - Bit 01

When set, BOT indicates the tape is positioned at the Load Point. An attempt to reverse tape motion or to rewind from BOT causes TC3.

End of Tape (EOT) - Bit 00

When set, EOT indicates the tape cartridge is at the end of Track 11 (last track). The system Initialization sequence always resets the EOT bit (status termination during a Read operation, or TC2 during Write operation).

4.2.4.3 Extended Status Register One (XST1)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	0	0	0	0	0	0	0	0	0	0	0	0	0	UNC	0

The contents of Read-only register XST1 appear as the fifth word stored in the Message Buffer by the TC05 tape coupler when a command is completed or when an ATTN condition has been detected. For Termination Class (TC) codes, see Table 4-1.

Data Late (DLT) - Bit 15

When set, DLT causes TC4 and indicates one of two conditions:

a. During a Read operation, the tape transport attempts to enter another byte after the RAM buffer (silo) in the TC05 tape coupler is full.

b. During a Write operation, an attempt is made to Write another byte on the tape when the RAM buffer in the TC05 tape coupler is empty.

These conditions occur whenever the latency of the Q-Bus on the CPU exceeds the required Data Transfer rate of the TC05 tape coupler.

Not Used - Bits <14:02> and 00

Each of these bit positions should always contain logic zero.

Uncorrectable Data (UNC) - Bit 01

When set, UNC causes TC3, TC4, and indicates a data error has occurred during execution of a Read or Write command.

4.2.4.4 Extended Status Register Two (XST2)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OPM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The contents of Read-only register XST2 appear as the sixth word stored in the Message Buffer by the TC05 tape coupler when a command is completed or when an ATTN condition has been detected. For Termination Class (TC) codes, see Table 4-1.

Operation in Progress (OPM) - Bit 15

When set, OPM provides the tape-moving status indication.

Not Used - Bits <14:00>

Each of these bit positions should always contain logic zero.

4.2.4.5 Extended Status Register Three (XST3)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	OPI	REV	0	DCK	0	0	RIB

The contents of Read-only register XST3 appear as the seventh word stored in the Message Buffer by the TC05 tape coupler when a command is completed or when an ATTN condition has been detected. For Termination Class (TC) codes, see Table 4-1.

Not Used - Bits <15:07> and 04, 02 and 01

Each of these bit positions should always contain logic zero.

Operation Incomplete (OPI) - Bit 06

When set with a TC6, OPI indicates one of two conditions:

a. During a Read, Space, or Skip operation, about 25 feet of tape have moved past the read head without detecting any data transitions on the tape.

b. During a Write operation, about 4 feet of tape have moved past the read head without detecting any data transitions on the tape.

Reverse (REV) - Bit 05

When set, REV indicates the current operation caused reverse tape motion. Reverse tape motion results from Retry commands as well as Reverse Read, Reverse Space, etc. The REV bit is cleared when the operation being performed is a Rewind or an operation that involves forward tape motion.

Density Check (DCK) - Bit 03

When set, DCK indicates the Servo Track identification burst (IDB) was not detected when moving the tape forward from the BOT. Tapes with bad Servo Track cannot be written or read.

Reverse Into BOT (RIB) - Bit 00

When set with a TC2, RIB indicates a Read, Space, Skip, or Retry command already in progress has encountered the BOT marker when moving tape in the reverse direction. The set RIB bit halts tape motion at the BOT.

4.3 COMMAND PACKET PROCESSING

The Command Packet protocol scheme allows a TS11 emulation to provide a large amount of tape transport status and error information to the CPU while using only two words of Unibus address space. The Command Packet protocol also prevents the tape transport from updating error and status information asynchronously; that is, while the CPU is reading the error and status information.

NOTE

This subsection is not intended to detail all aspects of Command Packet protocol or Command Packet processing. It is intended to show how these concepts are implemented in the tape transport subsystem.

4.3.1 BUFFER OWNERSHIP AND CONTROL

To allow the tape transport to use only two words of address space, the operating system software defines a set of locations in memory.

These locations (Command Buffers) are used to tell the tape transport which operation is to be performed. The operating system software also defines a set of locations (Message Buffers) in memory where the tape transport is to place the error and status information. The CPU must give both the Command Buffer address and Message Buffer address to the tape transport. The CPU gives the Command Buffer address to the tape transport on every command by writing the address of the Command Packet into the TSDB. The CPU gives the Message Buffer address to the tape transport every time the CPU performs a Set Characteristics command. To prevent the tape transport from updating the Message buffer while the CPU is reading that buffer, the concept of ownership must be defined. Both the Command Buffer and Message Buffer may be owned by the tape transport or by the CPU, but not by both simultaneously. Ownership of a Command Buffer or Message Buffer can be transferred only by the current owner.

Four different combinations can be used to transfer ownership of the two buffers:

Command Buffer - CPU to tape transport by the CPU
Command Buffer - Tape transport to CPU by the tape transport
Message Buffer - CPU to tape transport by the CPU
Message Buffer - Tape transport to the CPU by the tape transport.

An Initialize condition aborts any current operation and gives ownership of both the Command Buffer and the Message Buffer to the CPU. During normal command processing, the ownership of both buffers passes simultaneously, first from the CPU to the TC05 tape coupler (at the start of command processing when the CPU writes a Command Pointer into register TSDB), and then from the TC05 tape coupler to the CPU (when command execution has been completed). Event sequences that occur in transfers of buffer ownership are listed and described in Table 4-3.

Table 4-3. Event Sequences in Buffer Ownership Transfer

Buffer	Direction	Transfer Method
Command Buffer	CPU to TC05 Tape Coupler	The CPU transfers ownership of the Command Buffer to the TC05 tape coupler by writing the address of the Command Buffer in register TSDB. This writing clears the SSR bit in register TSSR.

Table 4-3. Event Sequences in Buffer Ownership Transfer (continued)

Buffer	Direction	Transfer Method
Command Buffer	TC05 Tape Coupler to CPU	The TC05 tape coupler transfers ownership of the Command Buffer back to the CPU by depositing a Message Packet (in the Message Buffer) that has the Acknowledge (ACK) bit set in the message header word. After the TC05 tape coupler deposits the message, it sets the SSR bit in register TSSR to indicate the message is in the Message Buffer. If the ACK bit in the message has not been set, the CPU senses that the TC05 tape coupler did not decode the contents of the Command Buffer and that the CPU still owns control of the Command Buffer. The command may then be reissued by the CPU.
Message Buffer	CPU to TC05 Tape Coupler	The CPU transfers ownership of the Message Buffer to the TC05 tape coupler by setting the ACK bit in the Command Buffer and then initiating the command by writing it into register TSDB. If the ACK bit in the Command Buffer has not been set, the TC05 tape coupler senses that the CPU still owns control of the Message Buffer. Since the TC05 tape coupler does not own control of the Message Buffer, when the CPU writes into register TSDB, the TC05 tape coupler responds by setting the SSR bit and performing an Interrupt operation (if the IE bit is set) without sending a message.
Message Buffer	TC05 Tape Coupler to CPU	The TC05 tape coupler transfers ownership of the Message Buffer to the CPU by writing into the Message Buffer and setting the SSR bit. This activity can occur at either one of two times: a. At the end of a command execution.

Table 4-3. Event Sequences in Buffer Ownership Transfer (continued)

Buffer	Direction	Transfer Method
Message Buffer (cont'd)	TC05 Tape Coupler to CPU (cont'd)	b. When the TC05 tape coupler is inactive and the Attention (ATTN) message is output. In this situation, the SSR bit is already set to logic one state because ATTN only happens when the TC05 tape coupler is inactive. Therefore, the TC05 tape coupler clears the SSR bit, outputs the message, sets SSR again and interrupts the CPU if the IE bit in the Message Buffer Release command that gave control of the Message Buffer to the TC05 tape coupler was set. **NOTE** For an ATTN condition to occur, the EAI bit in the previous Set Characteristics command must have been set.

4.3.2 BUFFER CONTROL WITH ATTENTION ENABLED

An Attention (ATTN) condition is enabled when the CPU enters the appropriate characteristics mode word in the Set Characteristics command. ATTN allows the TC05 tape coupler to flag exceptional conditions when the TC05 tape coupler is in the idle state and not executing a command. (Change in On-Line/Off-Line status of the tape transport or microdiagnostic self-test errors in the TC05 tape coupler are examples of exceptional conditions.) If the ATTN condition occurs and the TC05 tape coupler does not own control of the Message Buffer, the TC05 tape coupler queues the ATTN internally. When the CPU releases control of the Message Buffer on the next command (with the ACK bit set), the TC05 tape coupler outputs the ATTN message with the ACK bit in the message header word reset to the logic zero state to indicate that the command was lost (except for the transfer of ownership of the Message Buffer to the TC05 tape coupler). This ATTN message indicates the TC05 tape coupler has refused to accept ownership of the Command Buffer, but has accepted ownership of the Message Buffer.

The CPU still owns control of the Command Buffer because the TC05 tape coupler did not accept control of that buffer, and it also owns control of the Message Buffer which is currently filled with an ATTN message. If the CPU still needs to have the ignored command performed, it must reissue the command (with the ACK bit set). Exceptions to this procedure are the Set Characteristics command and the Write Subsystem Memory command which are executed regardless of a pending ATTN condition. These exceptions are necessary to allow the software to specify a Message Buffer

address, to control enabling of the ATTN condition, and to perform diagnostics.

Normally, the TC05 tape coupler relinquishes ownership of Message Buffer control at the end of a command execution. If, however, the CPU is to be notified of a change in the status of the tape transport or of a microdiagnostic error while the TC05 tape coupler is idle for a long time, the TC05 tape coupler must own control of the Message buffer for that entire period of time. To enable reception of such necessary ATTN messages, ownership of Message Buffer control is transferred to the TC05 tpe coupler via the Message Buffer Release command. This special command tells the TC05 tape coupler not to give ownership of Message Buffer control to the CPU at the end of the command execution. The TC05 tape coupler does not output a message at the end of the Message Buffer Release command, but updates the contents of register TSSR (with the SSR bit set) and then interrupts the CPU if the IE bit was set in the command and if such an interrupt was enabled by the set EAI bit in the previous Set Characteristic command. The TC05 tape coupler then retains ownership of Message Buffer control until an ATTN condition is detected. In this condition, the CPU owns control of the Command Buffer and the TC05 tape coupler owns control of the Message Buffer. When an ATTN condition is detected, the TC05 tape coupler performs the following event sequence:

a. Clears the SSR bit

b. Outputs the ATTN message, but with the ACK bit cleared (not set) because the TC05 tape coupler is not responding to a command

c. Sets the SSR bit

d. Interrupts the CPU if the IE bit in the Message Buffer Release command has been set

e. When the TC05 tape coupler outputs the ATTN message, ownership of Message Buffer control passes to the CPU, which then owns control of both the Command Buffer and Message Buffer.

The TC05 tape coupler cannot send another ATTN message to the CPU until the CPU issues a Command Packet that contains a set ACK bit (word one, bit 15 of Command Packet) to release ownership of the Message Buffer that contains the ATTN message.

If the CPU has issued a Message Buffer Release command and needs to execute another command but has not received an ATTN message from the TC05 tape coupler (the TC05 tape coupler still owns control of the Message Buffer from the Message Buffer Release command), the CPU can issue a command without the ACK bit set in the Command Buffer. At the time the new command is issued, the CPU does not own control of the Message Buffer, so the CPU cannot release the Message Buffer. If the CPU does set the ACK bit, nothing happens

except the CPU might miss an ATTN message from the TC05 tape coupler if the TC05 tape coupler is sending an ATTN message at the same time the CPU is issuing the new command.

Since it is possible (but not necessarily likely) that the CPU mat attempt to issue a new command at or near the same time that the TC05 tape coupler attempts to output an ATTN message, the CPU should not set the ACK bit because it does not own control of the Message Buffer. If the CPU writes into register TSDB while the SSR bit is clear during an attempt by the TC05 tape coupler to deliver an ATTN message, the RMR error status bit is set and that command is ignored by the TC05 tape coupler. The ATTN message must not have the ACK bit set because the TC05 tape coupler does not own control of the Command Buffer.

NOTE

> The RMR bit may be set in this way on a bug-free system. All other means of setting the RMR bit indicate a software bug where the CPU has attempted to execute a command before the previous command execution was finished.

If the command from the CPU was lost because the TC05 tape coupler was outputting an ATTN message, the IE and VCK bits (XST0 <05:04>, respectively) are not updated. If the command from the CPU was rejected (Illegal Command, etc.) and not ignored, the IE and VCK bits are updated to the start of the rejected command.

Message Packet protocol may be violated if the TC05 tape coupler detects an error (NXM, memory parity error, serial bus parity error, or I/O silo parity error) during the reading in of the Message Packet. When one of these errors occurs, the TC05 tape coupler always sends a failure message (because the Message Packet is not reliable).

The system software should be written so that no crash occurs if the TC05 tape coupler interrupts while the CPU is servicing an interrupt message from another TC05 tape coupler. A system crash may happen, but only if the TC05 tape coupler receives a fatal hardware error.

4.3.3 COMMAND PACKET/HEADER WORD

15	14 12	11 08	07 05	04 00
CTL	Device Dependent	Command Mode	Packet Format 1	Command Code
ACK	C V C O P P S W B	0 0 M M	IE O O	0 C C C C

The Command Packet header word is shown above and the bit functions are described in the following paragraphs. Bits in the fields for the Command Mode and Command Code are listed and defined in Table 4-4.

Table 4-4. Command Code and Command Mode Field Definitions

Command Code Field	Command Name	Command Mode Field	Mode Name
00001	Read	0000	Read next (forward)
		0001	Read previous (reverse)
		0010	Reread previous (space reverse, read forward)
		0011	Reread next (space forward, read reverse)
00100	Set Characteristics	0000	Load Message Buffer address and set device characteristic
00101	Write	0000	Write data (text)
		0010	Write data retry (space reverse, erase, write data)
00110	Write Subsystem Memory	0000	Not supported
01000	Position	0000	Space records forward
		0001	Space records reverse
		0010	Skip Tape Marks forward
		0011	Skip Tape Marks reverse
		0100	Rewind
01001	Format	0000	Write Tape Mark
		0001	Erase
		0010	Write Tape Mark entry (space reverse, erase, write Tape Mark)
01011	Initialize	0000	Tape transport initialize
01111	Get Status Immediate	0000	Get status (END message only)

Acknowledge (ACK) - Bit 15

Set when command is issued and CPU owns Message Buffer. Set ACK informs tape transport that Message Buffer is available for any pending or subsequent Message Packet(s). Set ACK passes ownership of Message Buffer to tape transport.

Device Dependent Field - Bits <14:12>

Set state of these bits causes functions defined in the following table:

Bit	Name	Function
14	CVC	Clear Volume Check
13	OPP	Opposite (reverse execution sequence of Reread commands)
12	SWB	Swap Bytes

Command Mode Field - Bits <11:08>

The bits in this field extend the Command Code and allow extended device commands (Seek, Rewind, Erase, Write Tape Mark, etc.) to be specified. Definitions for the bits in this field are listed in Table 4-4.

Packet Format #1 Field - Bits <07:05>

The bits in this field define the two values listed in the following table:

Bit 07	Values 06	05	Definition
0	0	0	One word header: interrupt disable
1	0	0	One word header: interrupt enable

Command Code Field - Bits <04:00>

Bits <04:03> of this field determine the format and length of the Command Packet. The state of these bits are listed and defined in the following table:

Code Bits 04	03	02	01	00	Definition
0	0	X	X	X	Four words (header, two word address, count)
0	1	X	X	X	Two words (header, parameter word) - or - one word (header)

Bits in the Command Code and Command Mode fields are listed and described in Table 4-4.

The Swap Byte (SWB) bit in the Command Packet header word (bit 12) instructs the tape transport to alter the sequence of storing and retrieving bytes from the memory in the CPU. When SWB is asserted (set to logic one state), an industry compatible sequence (beginning with an even byte) is used. When SWB is cleared (reset to logic zero state), the byte swap sequence begins with an odd byte.

NOTE

This SWB function only serves Data Transfer operations. The state of SWB is ignored for all other functions.

Figures 4-2 and 4-3 show the memory positions for the bytes as they are read from or written on the tape in a Byte Swap sequence. In these figures, the bytes of data in the record block on tape are numbered by starting at zero. Byte zero is always the data byte at the beginning of the data block; i.e., that part of the data block which is closest to the BOT.

NOTE

When reading in reverse, the first data byte read is the last data byte of the sequence written. The Read Reverse command stores this first data byte in the last buffer position; the next data byte is stored in the next to last buffer position, etc. This sequence results in placing data in memory in the right order when sequentially reading the contents of the buffer.

SWAP BYTES = 0
BUFFER ADDRESS = 1000
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000	1	0
1002	3	2
1004	5	4
1006	7	6

SWAP BYTES = 1
BUFFER ADDRESS = 1000
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000	0	1
1002	2	3
1004	4	5
1006	6	7

SWAP BYTES = 0
BUFFER ADDRESS = 1001
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000	0	
1002	2	1
1004	4	3
1006	6	5
1010		7

SWAP BYTES = 1
BUFFER ADDRESS = 1001
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000		0
1002	1	2
1004	3	4
1006	5	6
1010	7	

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Figure 4-2. Byte Swap Sequence, Forward

SWAP BYTES = 0
BUFFER ADDRESS = 1000
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000	1	0
1002	3	2
1004	5	4
1006	7	6

SWAP BYTES = 1
BUFFER ADDRESS = 1000
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000	0	1
1002	2	3
1004	4	5
1006	6	7

SWAP BYTES = 0
BUFFER ADDRESS = 1001
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000	0	
1002	2	1
1004	4	3
1006	6	5
1010		7

SWAP BYTES = 1
BUFFER ADDRESS = 1001
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000		0
1002	1	2
1004	3	4
1006	5	6
1010	7	

SWAP BYTES = 0
BUFFER ADDRESS = 1000
BYTE COUNT = 7
BLOCK SIZE = 7 BYTES

1000	1	0
1002	3	2
1004	5	4
1006		6

SWAP BYTES = 1
BUFFER ADDRESS = 1000
BYTE COUNT = 7
BLOCK SIZE = 7 BYTES

1000	0	1
1002	2	3
1004	4	5
1006	6	.

SWAP BYTES = 0
BUFFER ADDRESS = 1001
BYTE COUNT = 7
BLOCK SIZE = 7 BYTES

1000	0	
1002	2	1
1004	4	3
1006	6	5

SWAP BYTES = 1
BUFFER ADDRESS = 1001
BYTE COUNT = 7
BLOCK SIZE = 7 BYTES

1000		0
1002	1	2
1004	3	4
1006	5	6

TC0501-0217

Figure 4-3. Byte Swap Sequence, Reverse

4.3.4 COMMAND PACKET EXAMPLES

This subsection contains examples of the Command Packets and information about operating programs that are used in the TC05 tape coupler subsystem. Each Command Packet contains four words. All four words are read in, even if the command requires only one word (Rewind) or two words (Space). The Command Packet must have correct parity because the tape transport rejects a Command Packet on the basis of errors in the unused words. The Command Packet examples are presented in the order listed in the following table:

Command Packet	Figure	Subsection
Get Status	4-4	4.3.4.1
Read	4-5	4.3.4.2
Set Characteristics	4-6	4.3.4.3
Write	4-7	4.3.4.4
Position	4-8	4.3.4.5
Format	4-9	4.3.4.6
Control	4-10	4.3.4.7
Initialize	4-11	4.3.4.8

4.3.4.1 Get Status Command

This command causes a Message Packet to be deposited in the Message Buffer area to update the extended status registers. Since the TC05 tape coupler hardware automatically updates the extended status registers after execution of any command, except the Message Buffer Release command, the Get Status command should be issued only for one of the following conditions:

a. The TC05 tape coupler has been left idle for some time

b. An extended status register update is desired without performing a Tape-Motion command.

Words, fields, and bits in the Get Status Command Packet are shown in Figure 4-4.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE CODE				FORMAT #1			COMMAND CODE				
ACK	CVC	0	0	0	0	0	0	IE	0	0	0	1	1	1	1
NOT USED															

MODE CODE: 0000 = GET STATUS (END MESSAGE ONLY)

Figure 4-4. Get Status Command Packet

4.3.4.2 Read Command

The Read command has four Normal modes: Read Forward, Read Reverse, Reread Previous, and Reread Next. In all modes, the Read operation is assumed to be performed on a record of known length. Therefore, the correct record byte count must be known. If the byte count is correct, normal termination occurs. If the record is shorter than the byte count, the Record Length Short (RLS) bit is set and a Tape Status Alert (TSA) termination occurs (see TC2 in Table 4-1). If the record is longer than the byte count, the Record Length Long (RLL) bit is set and a TSA termination occurs. Any Read operation that encounters a Tape Mark does not transfer any data. When a Tape Mark is encountered during a Read operation, the Tape Mark (TMK) and RLS bits are set, and a TSA termination occurs.

Read Reverse operations which run into the BOT marker cause the Reverse Into BOT (RIB) bit to be set and a TSA termination occurs. In this situation, tape motion stops at the BOT. If a Read Reverse command is issued while the tape is already at the BOT, the Non-Executable Function (NEF) bit is set and no tape motion occurs.

Words, fields, and bits in the Read Command Packet are shown in Figure 4-5.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE CODE				FORMAT #1			COMMAND CODE				
ACK	CVC	OPP	SWB	X	X	X	X	IE	0	0	0	0	0	0	1
A15	LOW ORDER BUFFER ADDRESS														A00
0	HIGH ORDER BUFFER ADDRESS									A21	A20	A19	A18	A17	A16
BUFFER EXTENT (BYTE COUNT) (16-BIT POSITIVE INTEGER)															

Figure 4-5. Read Command Packet

NOTE

Bits <A21:A18> are used only when 22-bit addressing is enabled (see subsection 3.5.3.4).

If the OPP bit (header word bit 13) is set, the event sequence that occurs in execution of a Reread-type command is altered:

a. Reread Previous, which is normally a Space Reverse operation followed by a Read Forward operation, becomes Read Reverse, then Space Forward.

b. Reread Next, which is normally a Space Forward operation followed by a Read Reverse operation, becomes Read Forward, then Space Reverse.

Reading data in the reverse direction with a correct byte count correctly places the data in memory (as if the record were read in the forward direction), not in reverse order. This feature allows data to be correctly placed in memory on one retry (Read Reverse). During this operation, data are placed in the data buffer in the reverse order (highest address first); the starting address is calculated by adding the byte count to the address specified in the Read Command Packet and then subtracting one. If the byte count is greater than the actual record length, the beginning of the data buffer (lowest addresses) does not contain the data from the tape. Similarly, if the actual record is longer than the byte count, the first part of the record (that nearest to the BOT marker) is not placed in the data buffer.

For any Data Transfer operations, the Swap Bytes (SWB) bit in the header word of the Read Command Packet controls the storing of bytes in the memory of the CPU (see Figures 4-2 and 4-3).

4.3.4.3 Set Characteristics Command

The contents of the Set Characteristics Command Packet inform the TC05 tape coupler and tape transport where the Message Buffer is located in memory and the size of that Message Buffer. The Message Buffer must be at least seven contiguous words long (eight when the extended features provision is enabled), and it must be located on a Modulo-4 boundary. The Set Characteristics Command Packet and characteristics data format are shown in Figure 4-6.

If a correct Message Buffer address has not been loaded with the Set Characteristics command, the Need Buffer Address (NBA) bit in the TSSR is set.

The Set Characteristics command also transfers a Characteristics Mode byte to the tape transport. This byte is the low-order byte in the fourth word of the Characteristics Data Packet. This byte causes specific actions for certain operational modes. The meaningful bits in the Characteristics Mode byte are defined in the following paragraphs.

Enable Skip Tape Marks Stop (ESS) - Bit 07

When set, ESS instructs the tape transport to stop when a double Tape Mark (two contiguous Tape Marks) has been detected during execution of a Skip Tape Mark command. In the default reset state (logic zero), the Skip Tape Marks command terminates only when the Tape Mark count is exhausted or when the BOT marker is sensed by the tape transport.

Enable Tape Mark Stop Off BOT (ENB) - Bit 06

This bit has meaning only when the ESS bit is set. When both ESS and ENB are set (each returns a logic one when read), the tape position is at the BOT marker, a Skip Tape Marks Forward command is

COMMAND PACKET

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE CODE				FORMAT #1			COMMAND CODE				
ACK	CVC	0	0	0	0	0	0	IE	0	0	0	0	1	0	0
A15	LOW-ORDER CHARACTERISTICS DATA ADDRESS														A00
0	HIGH-ORDER CHARACTERISTICS DATA ADDRESS												0	A17	A16
BUFFER EXTENT (BYTE COUNT) (16-BIT POSITIVE INTEGER)															

MODE: 0000 = Load Message Buffer address and set device characteristics

CHARACTERISTICS DATA

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
A15	LOW-ORDER MESSAGE BUFFER ADDRESS														A00
0	HIGH-ORDER MESSAGE BUFFER ADDRESS												0	A17	A16
LENGTH OF MESSAGE BUFFER (AT LEAST 14 BYTES LONG) (16-BIT POSITIVE INTEGER)															
0	0	0	0	0	0	0	0	CHARACTERISTIC MODE BYTE ESS	ENB	EAI	ERI	0	0	0	0

Figure 4-6. Set Characteristics Command Packet and Characteristics Data Format

issued, and the first record encountered is a Tape Mark, then the TC05 tape coupler stops the operation and sets the LET status bit (XST0 bit 13). If the ENB bit is clear under these conditions, the TC05 tape coupler merely counts the Tape Mark and continues the operation.

Enable Attention Interrupts (EAI) - Bit 05

When this bit is cleared, Attention conditions such as transitions from On-Line mode to Off-Line mode, and microdiagnostic failures do not result in ATTN interrupt messages being sent to the CPU. Instead, the Attention condition is not noticed until the next command is issued; and that next command is rejected. When this bit state is set to logic one, Attention conditions cause an ATTN message to be generated (and an interrupt to be sent to the CPU if the IE bit was set on the last command) as soon as the TC05 tape coupler owns control of the Message Buffer.

Enable Message Buffer Release Interrupts (ERI) - Bit 04

If the state of this bit is logic zero, interrupts are not generated upon completion of a Message Buffer Release command. Upon recognition of the command, only the Subsystem Ready (SSR) status bit in the TSSR is reasserted. If this ERI bit is set to return a logic one when read, an interrupt is generated (without an accompanying Message Packet).

4.3.4.4 Write Command

Write operations can be performed in either of two Normal modes: Write Data and Write Data Retry. Each operation transfers data onto the tape in the forward direction only. Allowable mode codes for these functions are written in the header word of the Write Command Packet and are listed in the following table:

Mode	Function
0000	Write Data
0010	Write Data Retry (Space Reverse, Erase, then Write Data)

Words, fields, and bits in the Write Command Packet are shown in Figure 4-7.

The Write Command Packet contains four words: a header word, two words that specify the address of the data buffer in the CPU memory space where the data to be written onto tape are stored, and a Buffer Extent (byte count) word that specifies the number of bytes available in the data buffer and the number of bytes to be written onto tape. A byte count of zero specifies that 65,536 (64K) bytes are to be written.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE CODE				FORMAT #1			COMMAND CODE				
ACK	CVC	0	SWB	X	X	X	X	IE	0	0	0	0	1	0	1
A15	LOW ORDER BUFFER ADDRESS														A00
0	HIGH ORDER BUFFER ADDRESS									A21	A20	A19	A18	A17	A16
BUFFER EXTENT (BYTE COUNT) (16-BIT POSITIVE INTEGER)															

MODE: 0000 = Write Data
0010 = Write Data Retry (Space Reverse, Erase, Write Data)

Figure 4-7. Write Command Packet

NOTE

Bits <A21:A18> are used only when 22-bit addressing is enabled (see subsection 3.5.3.4).

If execution of a Write command is attempted at or beyond the EOT marker, a Tape Status Alert (TSA) termination occurs (see Table 4-1, TC2). The EOT status bit remains set until the EOT marker is passed while the tape is moving in the reverse direction or until the subsystem is initialized.

If execution of a Write command is attempted anywhere on the tape and the Identification Burst (IDB) was previously written incorrectly or was not found when the tape position left the BOT, the Density Check (DCK) bit (XST3, bit 03) is set and a Tape Position Lost (TC6) termination occurs.

For any of the Write modes, the Swap Bytes (SWB) bit, in the header word of the Write Command Packet, controls fetching of bytes from the memory in the CPU (see Figures 4-2 and 4-3).

4.3.4.5 Position Command

The Position command can cause tape to space records forward or reverse, skip tape marks forward or reverse, or to rewind to the BOT marker. For a Rewind command, the Tape Mark/Record Count in the second word of the Position Command Packet is ignored. The mode

code bits in the header word of the Position Command Packet define the positioning function to be performed. The mode codes are listed and defined in the following table:

Mode	Function
0000	Space Records Forward
0001	Space Records Reverse
0010	Skip Tape Marks Forward
0011	Skip Tape Marks Reverse
0100	Rewind (Tape Mark/Record Count ignored)

Words, fields, and bits in the Position Command Packet are shown in Figure 4-8.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE CODE				FORMAT #1			COMMAND CODE				
ACK	CVC	0	0	X	X	X	X	IE	0	0	0	1	0	0	0
TAPE MARK/RECORD COUNT (16-BIT POSITIVE INTEGER)															

Figure 4-8. Position Command Packet

The Space Records operation skips over the number of records that are specified in the Record Count word of the Position Command Packet, but the operation automatically terminates with a TSA code if a Tape Mark is encountered during execution of the operation. (The Tape Mark is included in the Record Count.) Also, if the record count is not decremented to zero, the RLS error bit (XST0 bit 14) is set.

The Skip Tape Marks operation skips over the number of Tape Marks that are specified in the Tape Mark Count word of the Position Command Packet, but the operation is automatically terminated if two contiguous Tape Marks without intervening data are encountered while the ESS bit in the Characteristics Mode Byte is set (result of the last Set Characteristics Command Packet).

Termination of a Skip Tape Marks command can also occur if a Tape Mark is the first record read after leaving the BOT marker when the ESS and ENB bits in the Characteristics Mode Byte are set (result of the last Set Characteristics Command Packet). Also if the record count is not decremented to zero, the RLS error bit (XST0 bit 14) is set.

Any Space Records Reverse or Skip Tape Marks Reverse operation which encounters the BOT marker, during command execution, sets the Reverse Into BOT (RIB) error status bit (XST3 bit 00) and causes a TSA termination. If one of these Reverse-Motion commands is issued while the tape is already positioned at the BOT marker, the Nonexecutable Function (NEF) error status bit (XST0 bit 10) is set

and a Function Reject termination occurs (see Table 4-1, TC3). When the NEF error status bit is set, the tape is prevented from moving. If the DCK error is present when a Position command is issued, the DCK error status bit (XST3 bit 03) is set but the operation is not stopped. The Positioning operation is terminated with a TSA termination. This function restriction allows tapes with a bad Identification Burst (IDB) area to be read.

When a Rewind command is issued, the interrupt (if enabled) does not occur until the tape reaches the BOT marker and has stopped.

NOTE

If the tape is positioned between BOT and the first record when a Space Reverse or Skip Reverse command is issued, the RIB error status bit is set and the contents of the Residual Frame Count Register (RBPCR) is the same as the specified Record Count in the Positioning command.

4.3.4.6 Format Command

The Format command can be used to write a Tape Mark, Rewrite a Tape Mark, or erase tape. The mode code bits in the header word of the Format Command Packet define the function to be performed. The mode codes are listed and defined in the following table:

Mode	Function
0000	Write Tape Mark
0001	Erase
0010	Write Tape Mark Retry (Space Reverse, Erase, Write Tape Mark)

Words, fields, and bits in the Format Command Packet are shown in Figure 4-9.

NOTE

Although the second word is present (fetched by the TC05 tape coupler), it is not used in the Format command and the state of each bit in this word should be logic zero.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE CODE				FORMAT #1			COMMAND CODE				
ACK	CVC	0	0	X	X	X	X	IE	0	0	0	1	0	0	1
NOT USED															

Figure 4-9. Format Command Packet

In all operations, attempting to execute a Format command at or beyond the EOT marker causes a TSA termination. Error status bit EOT (XST0 bit 00) is set and that bit remains set until the EOT marker is passed while the tape is moving in the reverse direction.

The Write Tape Mark command causes approximately 3.75 inches of tape to be erased and a Tape Mark to be written. The Erase command merely causes 3.75 inches of tape to be erased. Successive Erase commands can be used to erase more than 3.75 inches of tape, but only in 3.75-inch increments. The erase length is controlled automatically by tape transport hardware.

NOTE

Some system designers call a Tape Mark a File Mark; the two terms have the same meaning.

The Write Tape Mark Retry command causes a Space Reverse operation (over the previous record), followed by an erase of 3.75 inches of tape, followed by a Write Tape Mark operation (which erases another 3.75-inch segment of tape before writing the new Tape Mark. If the tape is at the BOT position when the Write Tape Mark Retry command is issued, the attempted operation is aborted with a Function Reject termination (TC3) and error status bit NEF (XST0 bit 10) is set.

Any attempt to execute a Format command while error status bit DCK (XST3 bit 03) is set causes a Tape Position Lost termination (TC6).

4.3.4.7 Control Command

The Control Command Packet can be used to point to three Normal command modes: Message Buffer Release, Unload, and Clean Tape. The mode code bits in the header word of the Control Command Packet define the function to be performed. The mode codes are listed and defined in the following table:

Mode	Function
0000	Message Buffer Release
0001	Unload
0010	Clean Tape

Words, fields, and bits in the Control Command Packet are shown in Figure 4-10.

NOTE

Although the second word is present (fetched by the TC05 tape coupler, it is not used in the Control command and the state of each bit in this word should be logic zero.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE CODE				FORMAT #1			COMMAND CODE				
ACK	CVC	0	0	X	X	X	X	IE	0	0	0	1	0	1	0
NOT USED															

Figure 4-10. Control Command Packet

When the Message Buffer Release command is executed with the ACK bit set, ownership of the Message Buffer is passed to the tape transport so it can update the status area in the Message Buffer in response to an ATTN condition. This function is beneficial when the operating system is processing data in other areas that are not related to the tape transport subsystem and the host CPU needs information about the current status of the tape transport.

The Unload command is used to rewind the tape completely onto the supply reel and place the tape transport in the Off-Line mode. When this command is executed, termination occurs immediately and an interrupt message is sent to the CPU if the IE bit has been set in the header word of the Control Command Packet.

The Clean Tape command moves ten inches of tape over the tape cleaners on the tape transport and then returns the tape to the original position. Successive Clean Tape commands are not recommended because the tape may creep outside the margins of the inter-record gap (IRG). Also, the Clean Tape command does not recognize BOT; therefore, tape can be cleaned while reversing past the BOT marker and then moving forward again without setting any status bits.

4.3.4.8 Initialize Command

If there are no microdiagnostic errors, this command is treated as a No-Op command and results in a Message Buffer update in the same way the update is performed in a Get Status command. If there are errors present, however, this command performs the same functions as a Write operation into the TSSR. The Initialize command is not very useful, but it is included for compatibility with Command Packet protocol.

In the header word of the Initialize Command Packet there is only one mode code available: 0000, so all bits in the mode code field are cleared and return a logic zero when read. Words, fields, and bits in the Initialize Command Packet are shown in Figure 4-11.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE CODE				FORMAT #1			COMMAND CODE				
ACK	CVC	0	0	0	0	0	0	IE	0	0	0	1	0	1	1
NOT USED															

Figure 4-11. Initialize Command Packet

NOTE

Although the second word is present (fetched by the TC05 tape coupler), it is not used in the Initialize command and the state of each bit in this word should be logic zero.

4.3.5 MESSAGE PACKET HEADER WORD

Words, fields, and bits in the Message Packet header word are shown in Figure 4-12, and the bit functions are explained in the following paragraphs.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	RESERVED			CLASS CODE				PACKET FORMAT #1			MESSAGE CODE				
ACK	0	0	0	0	0	C	C	0	0	0	1	M	M	M	M

Figure 4-12. Message Packet Header Word

Acknowledge (ACK) - Bit 15

This bit is used by the tape transport to inform the CPU the Command Buffer is available for any pending or subsequent Command Packets. This bit is not set for an ATTN message because the tape transport does not own the Command Buffer.

Reserved - Bits <14:12>

These bits are reserved for future expansion and should always return logic zero when read.

Class Code Field - Bits <11:08>

These bits define the class of message in the remainder of the Message Buffer. Class codes are defined as listed in the following table:

Message Type	Class Value	Definition
ATTN	0000	On-Line or Off-Line status
FAIL	0001	Other (ILC, ILA< NBA)
FAIL	0010	Write Lock Error (WLE) or Non-Executable Function (NEF)

Packet Format #1 Field - Bits <07:05>

Only a single value for this field is supported by the TC05 tape coupler. Value 000 means One Word Header.

Message Code - Bits <04:00>

The bits in this field indicate the definition codes listed in the following table:

Termination Class	Value	Definition
0, and 2	10000	End
3	10001	Fail
4, 5, 6, and 7	10010	Error
1	10011	Attention

4.3.5.1 Message Packet Example

All Message Packets are identical. Each contains the Message Packet header word, the data length word from the RBPCR, and the contents of four extended status registers (XST0, XST1, XST2, and XST3), as shown in Figure 4-13.

4.4 OPERATIONAL INFORMATION

This subsection explains four major requirements for operating and programming the tape transport subsystem:

a. Q-Bus registers

b. Command Packets and Message Packets

c. Special conditions and errors

d. Status error handling techniques

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE STATUS			STANDARD STATUS				PACKET FORMAT #1			MESSAGE CODE				
ACK	0	0	0	0	0	X	X	0	0	0	M	M	M	M	M
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
RBPCR															
XST0															
XST1															
XST2															
XST3															

MESSAGE CODE:
BITS <04:00>

10000 = END
10001 = FAIL
10010 = ERROR
10011 = ATTN

STANDARD STATUS:
BITS <11:08>

FAIL MESSAGE
0001 = OTHER
0010 = WRITE LOCK ERROR (WLE) OR NON-EXECUTABLE FUNCTION (NEF)

ATTN MESSAGE
0000 = ON-LINE MODE OR OFF-LINE MODE TRANSITION

Figure 4-13. Message Packet Example

4.4.1 Q-BUS REGISTERS

The tape transport has two Q-Bus word locations for device registers. The base address is written into the TSDB. The base address is read from the TSBA. The second device register (base address plus two) is the TSSR. Writing into the TSSR causes a subsystem Initialize command to be executed. Reading from the TSSR informs the CPU about the status of the selected tape transport.

During Normal operations, the TSDB is the only register written into. DATO or word access must be used to properly write Command Pointers into the TSDB. DATOB or byte access to the TSDB cause maintenance functions to be performed.

Commands are not written into the Q-Bus registers for the tape transport. Instead, Command Pointers are written into the TSDB. The Command Pointer points to a Command Packet somewhere in CPU memory space, and is used by the tape transport to retrieve the words from the Command Packet. The words of the Command Packet tell the tape transport which function is to be performed. They also contain any function parameters such as bus address, byte count, record count, and modifier flags.

4.4.2 COMMAND PACKETS AND MESSAGE PACKETS

Command Packets must reside on Modulo-4 address boundaries within CPU memory space. This requirement means the starting address of the Command Packet must be divisible by four; e.g., 00_8, 04_8, 10_8, 14_8, etc.

All four words of a Command Packet must exist and have proper memory parity, even if all four words are not used by a command. For instance, the Rewind command uses only one word.

Message Packets are issued by the subsystem and are deposited in the memory space in the CPU. Controlled operation of the tape transport requires it to be supplied with a Message Buffer address from a Set Characteristics command. The contents of the five extended status registers are stored in this Message Buffer area. The END Message Packet, which is sent when execution of any command is done, contains these extended status words.

4.4.3 SPECIAL CONDITIONS AND ERRORS

The Termination Class code field in the TSSR contains Termination Class codes in binary format. These binary values are listed and described in Table 4-5.

4.4.4 STATUS ERROR HANDLING TECHNIQUES

In the TSSR, the SC bit and error bits other than the fatal Termination Class (TC7) are cleared by loading a Command Pointer into the TSDB. The SC bit is reset if it was set by set UPE, SPE, RMR, or NXM error bits in the TSSR. Extended status error bits are cleared after the END Message Packet is sent.

All commands (even the Get Status command) clear all error bits in the extended status registers, except XST3 bits <15:08> and 01.

The TC05 tape coupler does not normally respond to a new command for the selected tape transport while another command execution is in progress on that tape transport. If an attempt is made to issue a new command while another command is being executed, the RMR error status bit (TSSR bit 12) is set, unless there exists one of the following exceptions:

Table 4-5. Termination Class Code Descriptions

TC Value	Message Type	Offset	Meaning
0	END	00	Normal termination. This TC code indicates the operation was completed without incident.
1	ATTN	02	Attention Condition. This TC code indicates the tape transport has changed status by going off line, or by coming on line, or the tape transport has failed a microdiagnostic.
2	END	04	Tape Status Alert. This TC code indicates a status condition occurred that can affect proper functioning of the program. Set bits which can produce TSA include TMK, EOT, RLS, and RLL.
3	FAIL	06	Function Reject. This TC code indicates the specified function was not initiated. Set bits which can produce this rejection include OFL, VCK, BOT, WLE, ILC, and ILA.
4	ERR	10	Recoverable Error. This TC code indicates tape position is one record beyond what its position was when the function was begun. Suggested recovery procedure is to log the error and issue the appropriate Retry command.
5	ERR	12	Recoverable Error. This TC code indicates tape position has not changed. Suggested recovery procedure is to log the error and reissue the original command.
6	ERR	14	Unrecoverable Error. This TC code indicates tape position has been lost. No valid recovery procedures exist unless the tape has labels or sequence numbers.
7	ATTN/ERR	16	Fatal Subsystem Error. This TC code indicates the subsystem is incapable of properly performing commands or the integrity of the subsystem is seriously questionable.

a. A DATO (word access) to the TSSR (subsystem Initialize operation) brings any operation in progress to an immediate halt. All subsystem parameters which had been in the memory of the subsystem (VCK reset, EOT, etc.) are erased.

b. The tape transport responds to any nontape motion command while performing a Rewind and Unload operation (while the tape transport is in the Off-Line mode) because the SSR status bit (TSSR bit 07) is still set.

The tape transport also responds to any commands which do not require tape motion (Get Status, Initialize, Set Characteristics, and Message Buffer Release) when off line, except when in the Maintenance mode. In the Maintenance mode, SSR is not asserted so that commands which do not require tape motion cause setting of the RMR bit.

If a Command Packet header word has the Interrupt Enable (IE) bit set (bit 07), a failure condition normally results in an Interrupt, but certain failures can occur with IE set without resulting in an Interrupt. Such failures are identified by the set condition of the following error status bits:

NXM
UPE

These error status bits may be set before the IE bit is fetched as part of the Command Packet.

Section 5
TROUBLESHOOTING

5.1 OVERVIEW

This section describes preventive maintenance and servicing procedures for maintaining optimum performance of the TC05 tape coupler system. This section is divided into foyr subsections, as listed in the following table:

Subsection	Title
5.1	Overview
5.2	Preventive Maintenance
5.3	Service
5.4	Fault Isolation

5.2 PREVENTIVE MAINTENANCE

The regularly scheduled maintenance checks, cleaning procedures, component replacement procedures, and adjustment procedures detailed in the separately supplied DEC and CDC system manuals should be accomplished at the prescribed intervals. There are no adjustments or calibrations required in servicing the TC05 tape coupler. Emulex recommends the diagnostic software programs be used in the DEC LSI-11 system checkout. The diagnostic programs should be run at regularly scheduled intervals to verify correct system operation.

NOTE

When any circuit component has been replaced, the diagnostics should be run and all pertinent circuit characteristics should be checked before the system is returned to normal operation.

Preventive maintenance of the TC05 tape coupler system also includes three periodic verifications:

a. Proper seating of TC05 tape coupler PCBA in CPU backplane.

b. Proper seating of cables in connectors.

c. Proper seating of replaceable ICs, including PROMs, in their respective IC sockets.

These verifications should be made about once a year or whenever physical location of components of the TC05 tape coupler is changed.

5.3 SERVICE

The components of the Emulex TC05 tape coupler have been designed to give years of trouble-free service, and they were thoroughly tested before leaving the factory. Corrective maintenance should not normally be required. Except for setting DIP switches and placing jumpers on proper connective points (see subsection 3.5), no adjustments or alignments are required. If a malfunction does occur, as indicated by Fault Isolation procedures, and a component is not working properly, the entire TC05 tape coupler should be returned to the factory or to an Emulex-authorized repair center for service. Emulex products are not designed to be repaired in the field.

If the TC05 tape coupler is to be returned, Emulex recommends that a description of the symptoms and operating environment be included with the returned unit to expedite troubleshooting. Figure 5-1 shows a configuration record sheet to be filled in. The depicted configuration shows component locations, PROMs, DIP switch settings and cable connections.

Before returning the TC05 tape coupler to Emulex, whether it is or is not under warranty, request the factory or the factory representative to provide return-shipment instructions and a Return Materials Authorization (RMA) number.

DO NOT RETURN A PRODUCT OR COMPONENT TO EMULEX
WITHOUT AUTHORIZATION

A product or component returned for service without an authorization will be returned to the owner at the owner's expense.

In the continental United States, Alaska, and Hawaii notify:

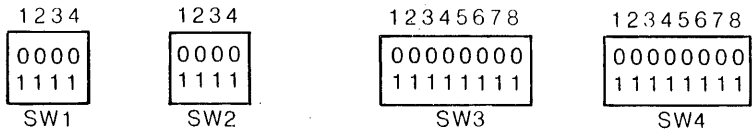
Emulex Technical Support
3545 Harbor Boulevard
Costa Mesa, CA 92626
(714) 662-5600 TWX 910-595-2521

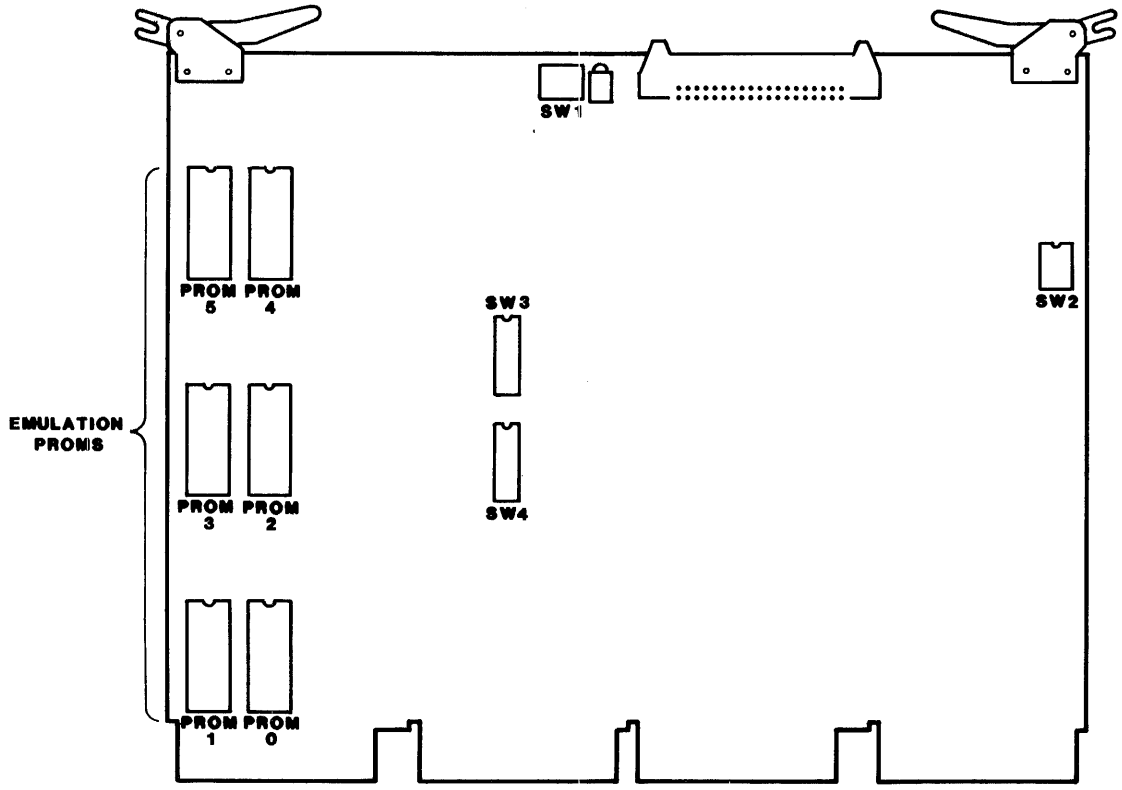
Outside of the United States, notify the distributor from whom the product or component was initially purchased.

After notifying Emulex and receiving an RMA, package the product (preferably by using the original packing material) and send the product **POSTAGE PAID** to the address provided by the Emulex representative. The sender must also insure the package.

TC05 TAPE COUPLER CONFIGURATION RECORD SHEET

Configuration PROM numbers range from _____ to _____.





Use Pencil

TC0501-0218

Figure 5-1. TC05 Tape Coupler Configuration Record Sheet

5.4 FAULT ISOLATION

The ensuing suggested fault isolation procedures are general in nature, based on established troubleshooting techniques, and should be used primarily as a guide. Following these procedures can aid in determining whether the equipment failure is a result of operator error or equipment malfunction, speed location of a failed circuit component, and minimize down time caused by equipment malfunctions.

5.4.1 ISOLATING THE PROBLEM

In troubleshooting electronic equipment, the problem can usually be attributed to any of three sources:

a. Operator error

b. Advise environmental factor(s)

c. Equipment malfunction.

Operator error is a more prevalent source of equipment problems than most operators care to admit. Operating procedures should always be investigated and eliminated before assuming any other source of malfunction exists. The symptoms should not be systematically investigated for environmental or electromechanical symptoms of malfunction until all possibility of human error has been eliminated.

5.4.2 OPERATING PROCEDURE CHECK

A system malfunction, appearing to be caused by circuit failure, is often found to be the result of improper operation or application of the equipment. When a problem is observed, the operating procedures being used with the malfunctioning unit and its associated units must therefore be thoroughly checked to ensure they are being correctly performed.

5.4.3 MANUAL OPERATIONS CHECK

A check must be made to determine if manual operations such as cleaning, servicing, or troubleshooting were performed on the equipment or related equipment before the first observed abnormal operation. Recently performed manual operations are suspect and should be double-checked to ensure that they were properly executed. Emulex recommends the following checks:

a. Verify recently changed procedures correctly performed

b. Verify adjustment settings properly made

c. Verify tightness of system connector installations

d. Verify that any parts temporarily removed or disconnected were properly and securely replaced

e. Verify that no accidentally loosened or damaged components are evident. Tighten any loose components and replace any obviously damaged components.

5.4.4 VISUAL INDICATOR CHECK

If the malfunction persists after double-checking all recent manual operations, visually check the status of all operating controls and indicators in the system. Visual indicators include the following items:

a. Switches and indicator lights on PCBAs and operator control panels (OCPs)

b. Busses

c. Switches and/or indicators mounted out of sight on internal chassis or PCBAs

d. Printed data outputs.

Correct any observed control-setting errors. Attempt to determine possible causes of erroneous indication.

5.4.5 POWER CIRCUIT CHECK

The effects of power supply malfunctions are normally widespread, which makes diagnosis of the problem difficult. Error indications tend to appear throughout the equipment and are difficult to localize. These symptoms, however, can sometimes be used as an indication that the cause of the problem is basic and pertains to the power circuits.

5.4.5.1 Fuses

Verify that all fuses in the power circuits are of the proper type and rating, and that none have blown. This check should include any fuses (or circuit breakers) internally mounted and not readily accessible from the front or rear of the major units of the system. Remove any blown fuse and replace with new fuse of the same type and rating.

CAUTION

Fuses with higher ratings or faster blow time limits than those removed must never be installed. Determine cause of fuse failure and correct problem before replacing failed fuse.

5.4.5.2 Voltage levels

Verify that power of the proper frequency and amplitude is being supplied to the equipment. If the primary input power is correct, check the output levels from all internal power supplies. All such outputs must be within required specifications (see applicable technical manuals for the equipment) and not subject to slow or intermittent drifting. If the problem is cyclic or intermittent; i.e., appears for a period of time and then disappears, check the power supplies for extreme sensitivity to variations in ambient temperature (heat or cold).

5.4.6 ELECTRONIC CIRCUIT CHECKS

When the possibility of operator error has been eliminated, and the existing symptoms have been thoroughly analyzed but the cause of the problem cannot be found, then attempt to determine if the problem is repeatable, continuous, or intermittent. The identical operation should be repeated several times to determine the types and number of failures.

If repeating the operation fails to sufficiently isolate the location of the malfunctioning circuit area, all the diagnostic programs should be run to determine if the symptoms appear under all conditions.

The power supply voltages, as well as the AC line voltage at the input, should be checked first to determine if they are within specification. The basic timing circuits should then be checked; problems in either of these areas are difficult to diagnose, since these circuits affect operation of all other circuits. These timing circuits, in turn, make error indications intermittent and problem isolation difficult. Varying the environment (power supply voltages, heat, mechanical shock, etc.) may sometimes cause an intermittent problem to occur more often so that it can be investigated more effectively.

CAUTION

The +5V should only be varied ±5% in margin tests. The IC chips used are rated from +4.75V to +5.25V.

5.4.6.1 Circuit Divisions

When attempting fault isolation in electronic systems, it is best to divide the system into troubleshooting areas, with each system unit being considered as a separate area. Then each functional section of each unit (power circuits, amplifier circuits, servo circuits, digital circuits, analog circuits, etc.) should be considered as a separate area. In this way, each area can be individually evaluated, and those not involved in the problem can

be eliminated from consideration. The source of the problem is thus isolated into ever smaller areas until only the actual problem area remains.

Most electronic equipment operates from an interwoven network of circuits. Malfunctions or improper operating procedures originating in one area of the equipment often cause failure symptoms within that area and other related areas. These symptoms are the foremost troubleshooting aids available and should be used to their fullest extent. In many instances, a malfunction can be isolated to a particular area by completely analyzing the symptoms.

5.4.7 NOISE PROBLEM CHECKS

Many times, equipment failures occur which are extremely intermittent and seem to appear at random intervals. The cause of these symptoms can often be traced to the power on/off switching of heavy machinery or high-powered electrical devices in the immediate area. Such events can cause extreme noise signals on the primary AC power input lines and a sudden variation in line voltage may be reflected in the DC operating voltages which can result in an equipment failure. Therefore, when extremely intermittent failures are encountered, an attempt must be made to reference these failures to a simultaneous outside occurrence which might have a bearing on the problem.

Individual power supplies within the equipment must be checked for excessive ripple in output levels. Checks must also be performed for noise bursts causes by the combination of loose electrical connections and mechanical shock or vibration. In some situations, individual components may also be found to be sensitive to mechanical shock or vibration even though all connections are secure.

5.4.8 FAULT ISOLATION GUIDE

Table 5-1 is a Fault Isolation Guide that should be used as a diagnostic aid for the isolation of faults in the TC105 tape coupler system. It lists possible symptoms, probable cause of the malfunction, and corrective actions.

Table 5-1. TC05 Tape Coupler Fault Isolation Guide

Symptom	Probable Cause	Remedy
CPU powered up, FAULT/ACTIVITY LED indicator lit	Self-Test failure	Verify TC05 tape coupler PCBA is properly seated in CPU backplane; reset if necessary
		Defective unit. Return TC05 tape coupler to factory.
Switch SW1-1 ON to reset and FAULT/ACTIVITY LED indicator lit steadily	Self-Test failure	Defective Unit. Return TC05 tape coupler to factory.
Data Transfer operation attempted but ACTIVITY LED not lit	Cable for control lines or data lines reversed	Check cable connections and reverse if pins of connectors not properly matched
	Interface cables to/from addressed tape transport not connected	Connect cables to/from addressed tape transport
	Addressed tape transport does not have Ready status	Perform operations on tape transport that are needed to produce Ready status condition
	Wrong CSR device address coded in configuration DIP switches	Encode correct Interrupt configuration DIP switch pack
Unable to interrupt CPU	Wrong Interrupt Vector Address coded in configuration DIP switch pack	Encode correct Interrupt Vector Address in configuration DIP switch pack

Appendix A
PROM REMOVAL AND REPLACEMENT

A.1 OVERVIEW

This appendix provides instructions for PROM removal and replacement. PROMs are usually exchanged only when an emulation is to be changed or when necessary for maintenance. Owners of existing TC05 tape couplers may wish to take advantage of the flexibility of Emulex hardware by replacing their existing TS11 emulation PROM set with a PROM set for another compatible emulation at some future date. The PROM set consists of an emulation firmware set and the associated Address PROM. This appendix is divided into three subsections, as listed in the following table:

Subsection	Title
A.1	Overview
A.2	Location
A.3	Removal and Replacement

A.2 LOCATION

The TC05 tape coupler has six IC sockets for insertion of PROMs which store instructions used by the on-board microprocessor to perform the TS11 emulation. These sockets are located along the left edge of the PCBA and are reference designated U90 (PROM0), U89 (PROM1), U55 (PROM2), U54 (PROM3), U2 (PROM4), and U1 (PROM5), as shown in Figure 3-2 and listed in Table A-1. The number on the top of each PROM IC is an Emulex part number (P/N) which identifies the unique program pattern of the PROM.

Two other IC sockets are provided for replaceable ICs. Socket U76 (eighth IC from left, second row from bottom) contains the Address Decode PROM. Socket U101 (seventh IC from right, bottom row) is used for the optional Extended (22-bit) Address option. This option requires a bit-slice AMD 2908 IC.

Table A-1. PROM Locations

Emulex PROM P/N	Socket	Reference Designator
924	PROM0	U90
925	PROM1	U89
926	PROM2	U55
927	PROM3	U54
928	PROM4	U2
929	PROM5	U1

A.3 REMOVAL AND REPLACEMENT

To remove any replaceable IC, pry each installed IC from its socket by using an IC puller or equivalent tool. When inserting PROMs in sockets, the ID numbers on top of the PROMs must be in the same sequence as the PROM reference designation numbers on the PCBA beside each respective PROM socket; e.g., PROM with ID3 must be inserted in IC socket reference designated PROM3.

Verify each PROM is seated firmly and that no pins are bent or misaligned. If the two rows of pins on any PROM are too far apart to fit in the IC socket, grasp the PROM at its ends between thumb and forefinger, press one row of pins on one side against a table top or other firm, flat surface, and gently bend the row of pins inward enough to allow the PROM to fit the intended IC socket.

EMULEX

PUBLICATION ADDENDUM

NO. AD0016C DATE: 08 Aug 1984

PAGE: 1 OF 1

PUBLICATION NUMBER	PUBLICATION TITLE	REV	EFFECTIVE DATE
TC0251002	TC02/FS Technical Manual	All	08 Aug 1984
TC0551001	TC05 Technical Manual	All	16 Jul 1984
TC1251002	TC12/FS Technical Manual	All	16 Jul 1984
TC1351001	TC13 Technical Manual	All	16 Jul 1984
TC1551001	TC15 Technical Manual	All	16 Jul 1984
PE0251001	Medley User's Manual	All	30 Jul 1984
PE0551001	Vault User's Manual	All	30 Jul 1984

RT11 USERS

CAUTION

The BUP (Backup/Restore) Utility provided by Digital Equipment Corporation's (DEC's) RT-11 Operating System (Versions 5.0 and 5.1) may, under certain conditions, **ALTER DATA** during the backup or restore process when used in conjuction with Emulex TS11-type products.

Other DEC users have reported this problem as well, and Emulex believes that the problem lies within the DEC software. Emulex has advised DEC of this problem by means of a Software Problem Report (SPR).

Pending resolution of this problem, Emulex does not recommend the use of the BUP Utility for backup or restoration of disk files when operating with the Emulex TS11-type tape couplers or subsystems listed above.

Emulex supplies and maintains a Backup and Restore Program (BRP) that supports image mode backup and restore operations to TS11-type tape subsystems from any of several DEC disk subsystems. Note that BRP does not support single file backup or restore; only complete disks may be backed up or restored. BRP (Emulex part number PD9960403) can be ordered from your Emulex sales representative or directly from the factory. Contact:

Emulex Corporation
In-House Sales
3545 Harbor Boulevard
Costa Mesa, CA 92626
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