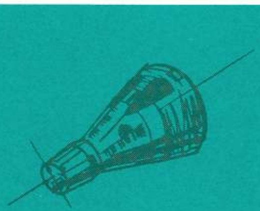
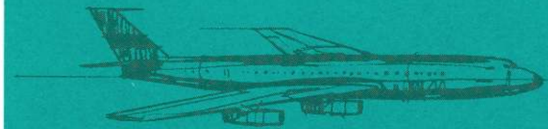
THE COMPATIBLES/600

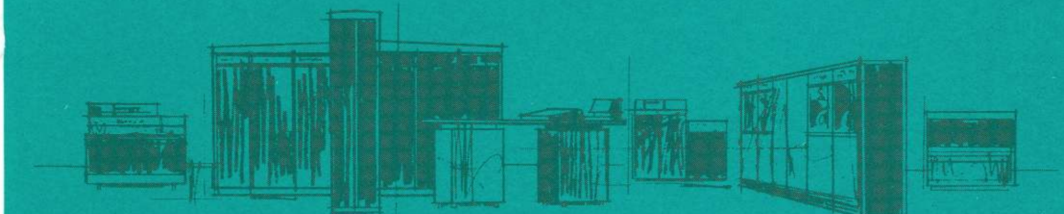
Real - Time Input / Output Controller

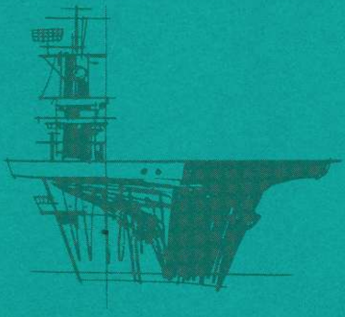


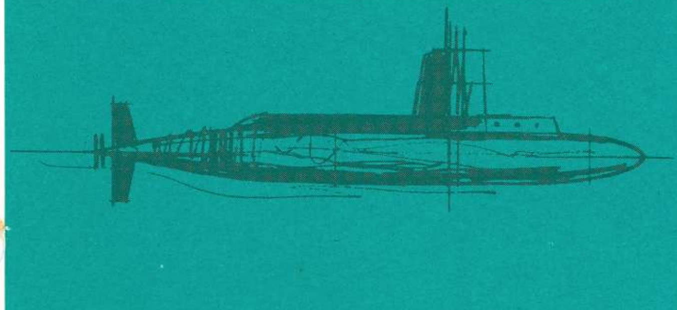
RT-IOC

providing a real-time external interface for...
The Compatibles/600









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REAL-TIME INPUT/OUTPUT CONTROLLER REFERENCE MANUAL

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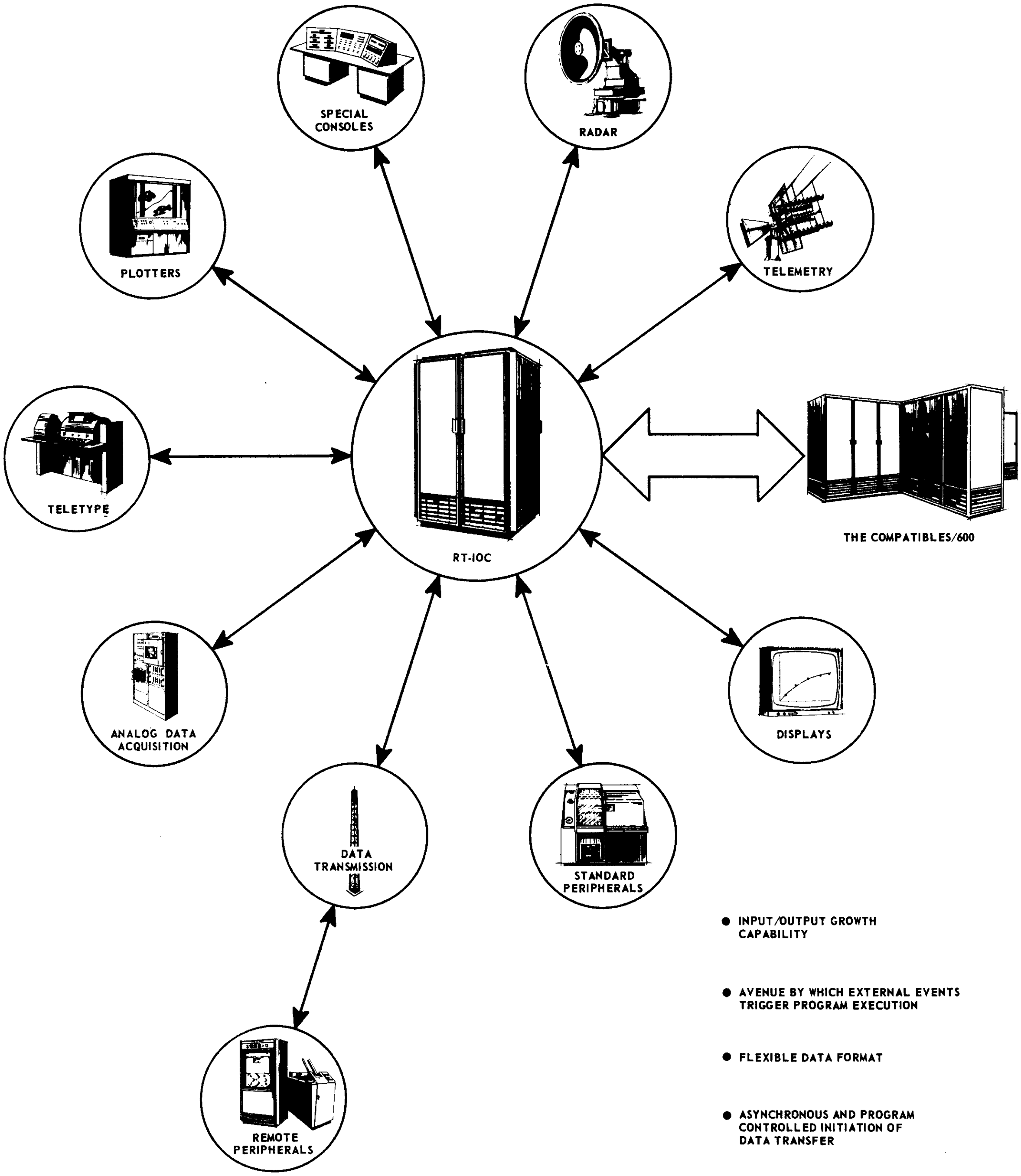

- INPUT/OUTPUT GROWTH CAPABILITY
- AVENUE BY WHICH EXTERNAL EVENTS TRIGGER PROGRAM EXECUTION
- FLEXIBLE DATA FORMAT
- ASYNCHRONOUS AND PROGRAM CONTROLLED INITIATION OF DATA TRANSFER

The RT-IOC Interfaces with Unique User Systems

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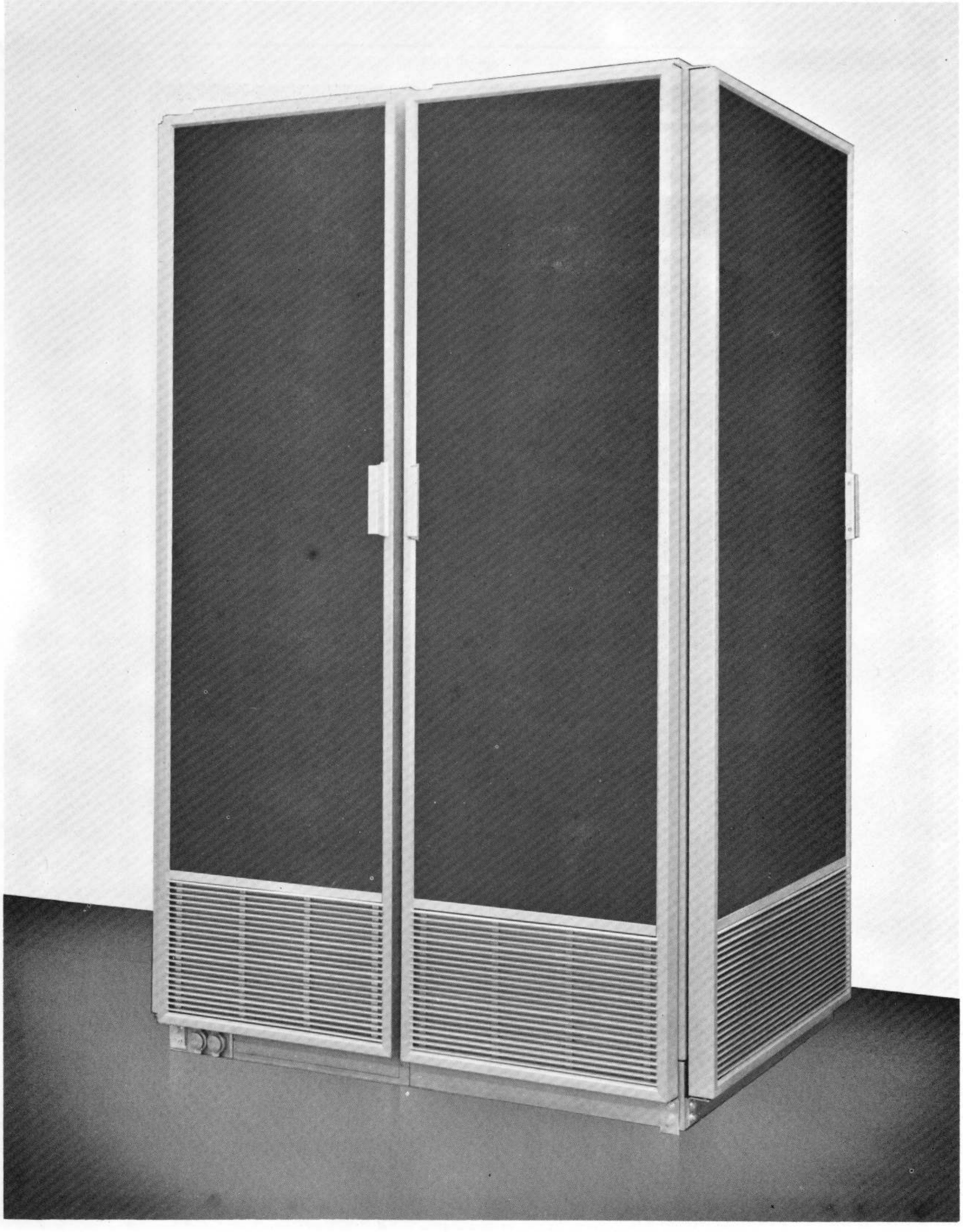
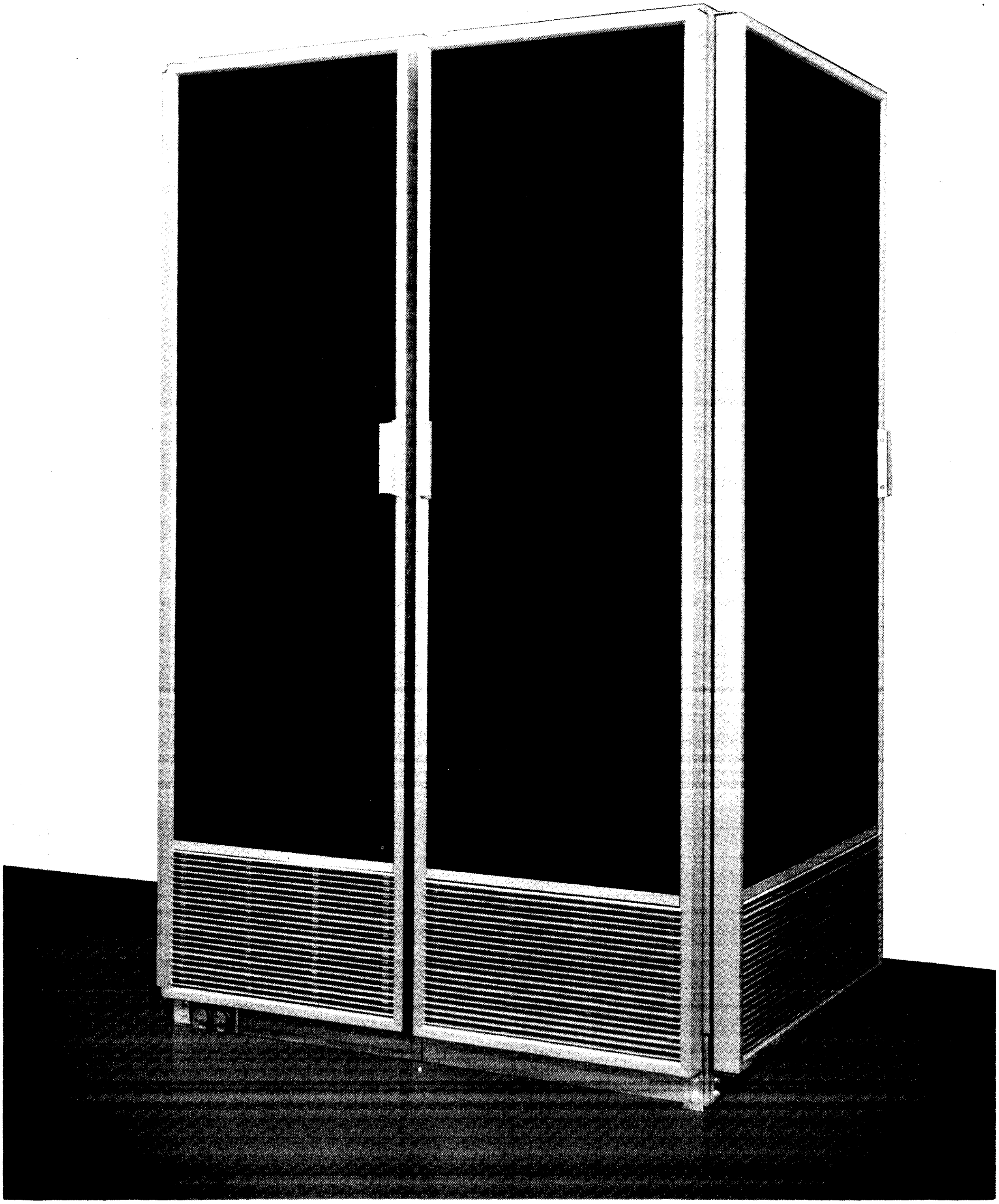
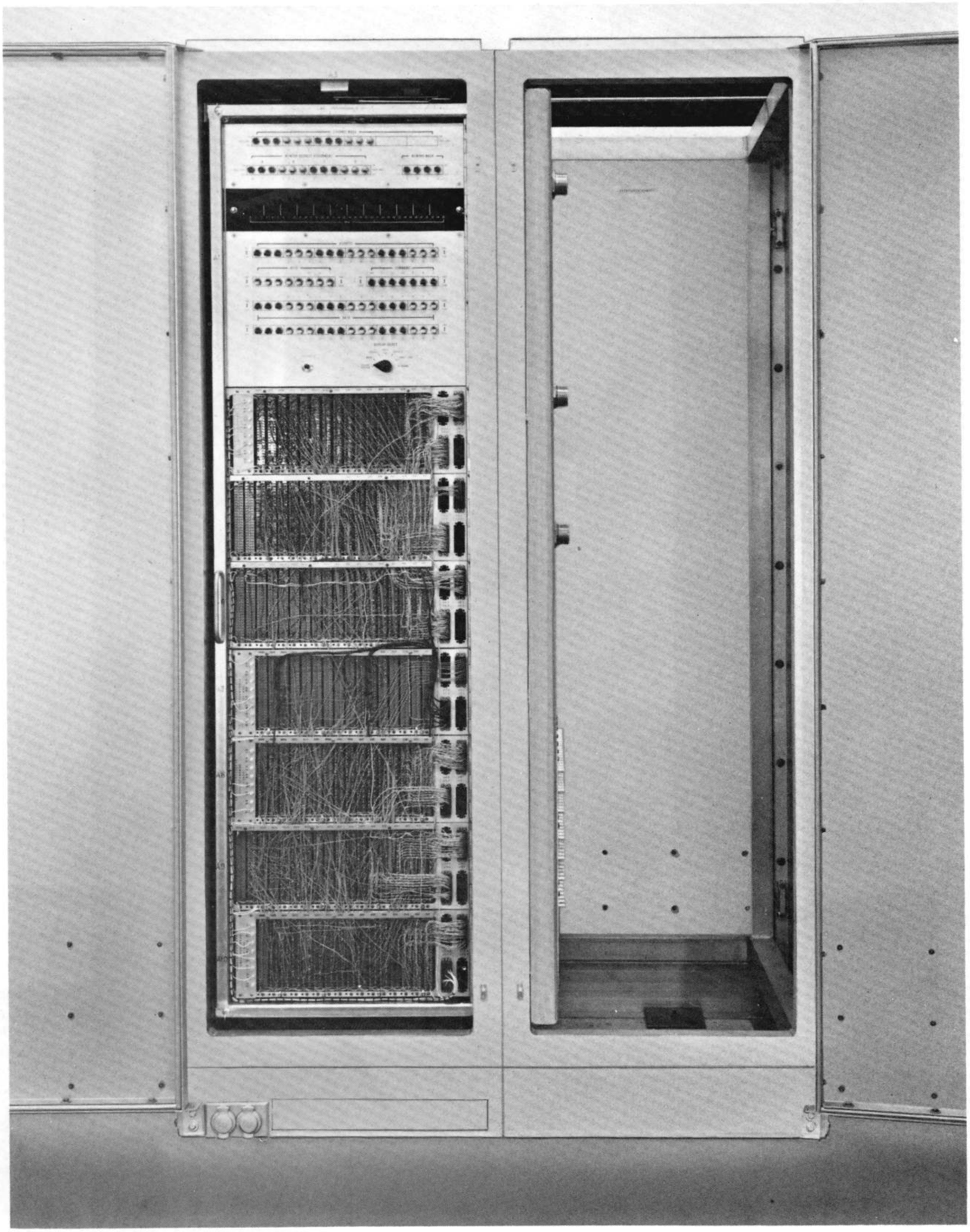


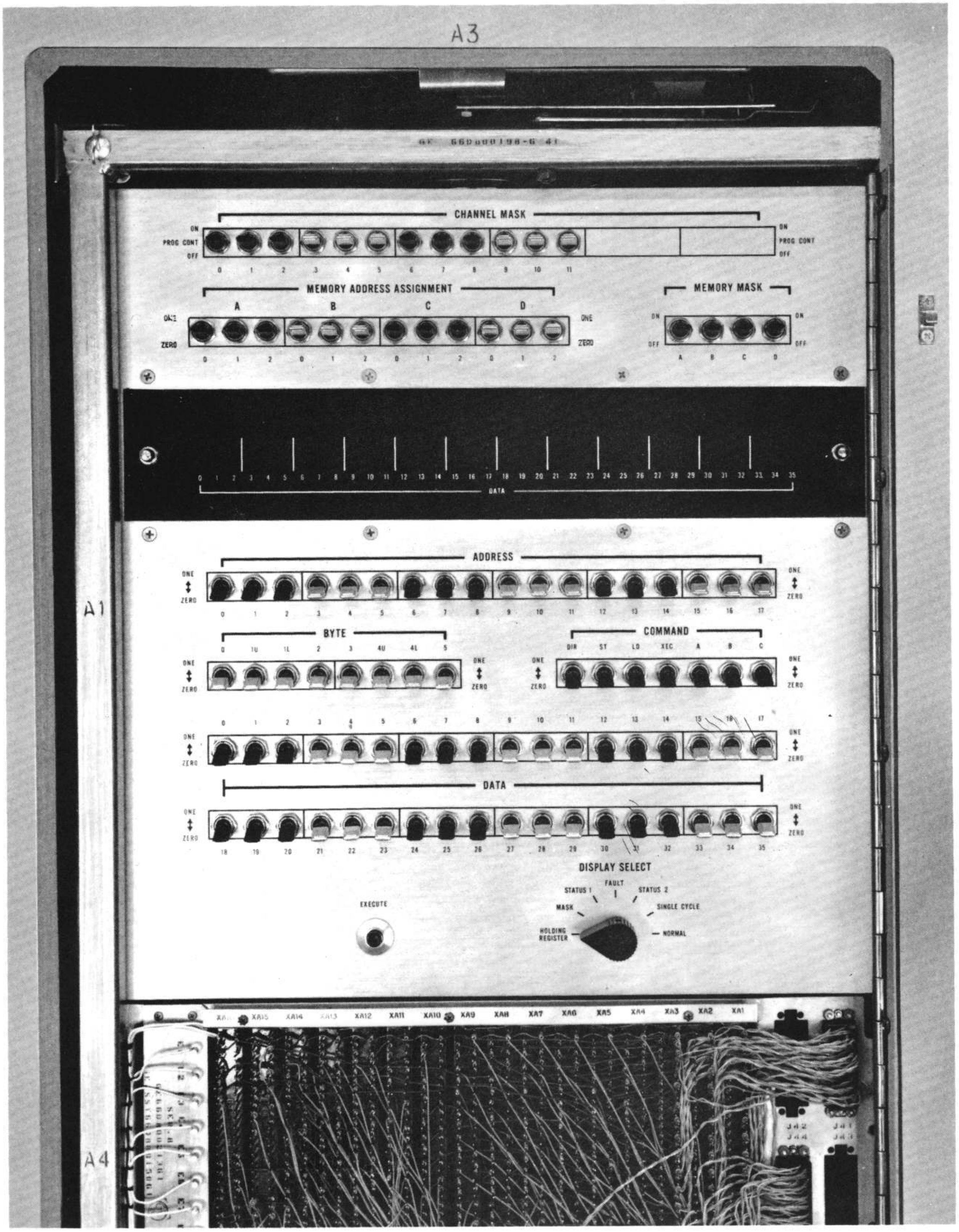
The RT-IOC



The RT-IOC



RT-IOC Interior



RT-IOC Maintenance Panel

I. PURPOSE AND APPLICATION OF THE RT-IOC

A. INTRODUCTION

The RT-IOC is an equipment module of the Compatibles/600. It provides the electrical interface between any member of this General Electric computer family and the external real-time environment. The RT-IOC design philosophy, of customizing its channel interface to each unique external device rather than requiring such devices to present a standard peripheral interface to the computer, provides programming simplicity, fast and efficient data transfer, and reduced hardware complexity. Thus, the RT-IOC enables the GE-600's to communicate with the "one of a kind" devices of real-time mission-oriented systems, as well as the more traditional computer peripheral devices.

The RT-IOC performs its basic functions of data transfer, issuing of commands, and forwarding of program interrupts with significant flexibility. For example, its peak data rate varies as a function of the following user choices: the memory speed of the computer used, and the direct versus indirect input/output addressing options. The number of I/O channels which are implemented in a given RT-IOC depend on the user's needs and the aggregate data rate of the devices being considered. A maximum of 27 half-duplex payload (external) channels can be accommodated per RT-IOC, for use by real-time devices, standard peripherals, and channel expanders.

As shown in the system diagram, the RT-IOC can be used in multi-processor and multi-computer systems and can interface with up to four memory modules. This capability means that as additional memory modules are introduced to an existing system, all the external devices served by an existing RT-IOC are placed in communication with the new memory region by implementing the RT-IOC interface to the additional memory module.

In further recognition of the variation in user needs, the RT-IOC module is available with other optional features which include input/output parity checking and generation, and an Automatic Program Loader Option. When the RT-IOC is to be used with the GE-635, a special high data rate version of the RT-IOC can be elected for use in applications where unusually fast external devices must be accommodated.

The RT-IOC is supported by the standard software of the Compatibles/600. An extended version of GECOS (General Comprehensive Operating Supervisor) can be supplied containing the unique interrupt handlers and initiate routines needed for specific system applications. This additional module of GECOS is RT-IOS (Real-time Input/Output Supervisor). RT-IOS performs necessary I/O initiate operations, and utilizes a "communications and control" block within the executive region of memory for cross-tell between unique external user devices and easily replaceable user programs.

To meet the needs of complex real-time applications, the RT-IOC provides the user interface with two forms of asynchronous interrupt techniques. One is the chain of maskable channel interrupt cells associated with access to memory by the I/O data channels of the RT-IOC and the second is

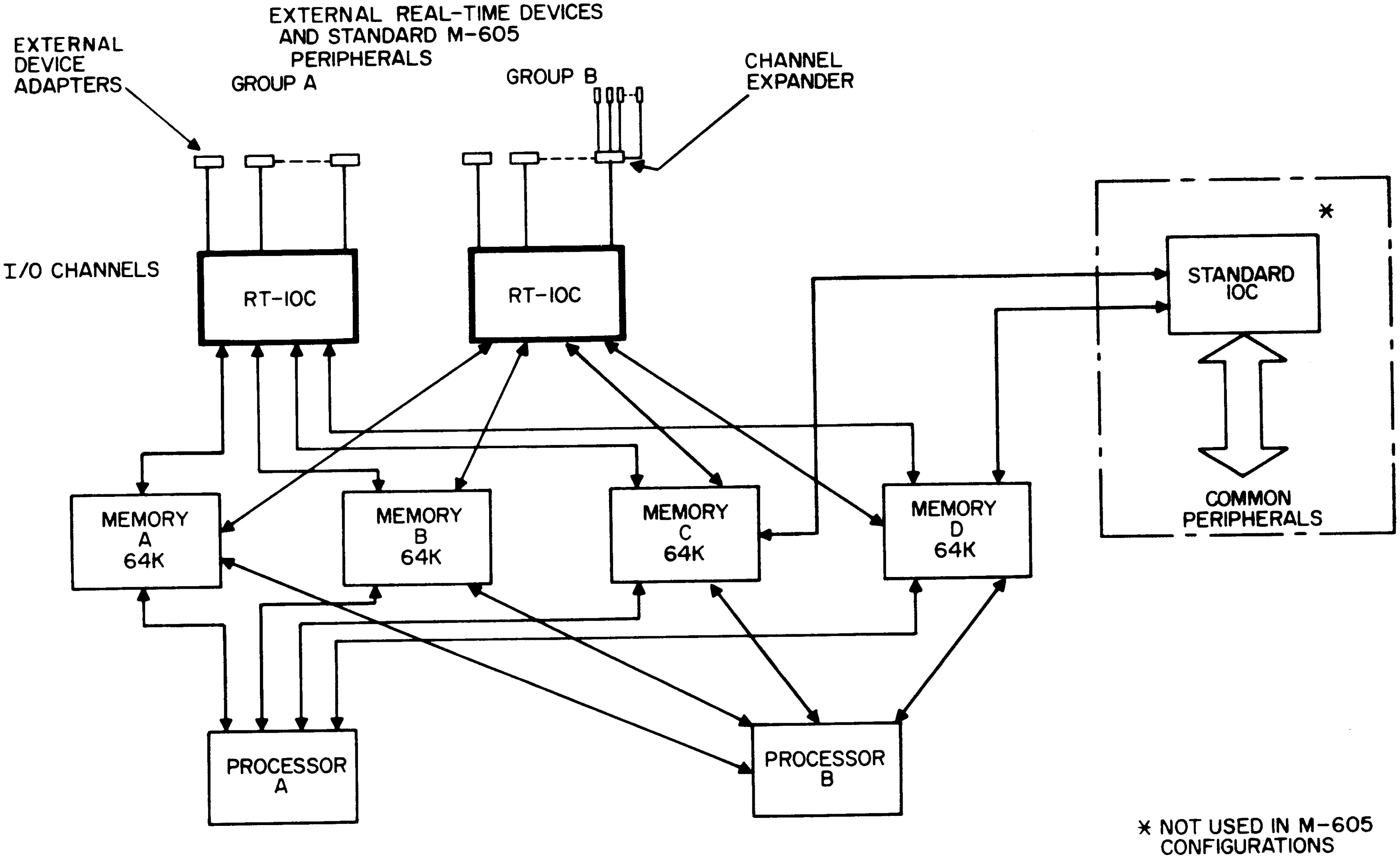


Figure I-1. RT-IOC Usage in Large Scale GE-600 Computer Configuration

an avenue for setting of the program execute interrupt cells in the memory controller module so that the execution of various interrupt handlers and mission program modules can be "triggered" by the external user system.

In summary, the RT-IOC uses a combination of fixed control logic common to each application, combined with user selected optional features, and customized channel-by-channel format and interface specifications, to integrate any member of the Compatibles/600 with user subsystems in order to fulfill the requirement of the real-time missions of modern data systems.

B. RT-IOC PERFORMANCE LEVELS

The memory module, with which the RT-IOC is communicating, sets the peak data transfer capability of the RT-IOC module. For example, if the RT-IOC is transferring data into a memory module of a multi-processor system in which that memory module is momentarily acting as an I/O memory (not being accessed by a processor or any other device) then the RT-IOC can achieve a transfer rate that begins to approach the reciprocal of the rated cycle time of that memory module. However, in typical applications, the memory module will be subject to access requests from other principal modules concurrently with access requests by the RT-IOC. After derating the RT-IOC to allow for other devices making concurrent access to the same memory module, there remain three available performance limits under which the RT-IOC may operate. These limits are related to the use of an RT-IOC with:

(a) the 2 μsec memory of the M-605, M-625, and GE-625

(b) the 1 μsec memory of the GE-635

(c) the 1 μsec memory of the GE-635, but using a special RT-IOC design which achieves increased speed at the cost of some flexibility.

These three performance regions of the RT-IOC may be depicted as shown in the diagram.

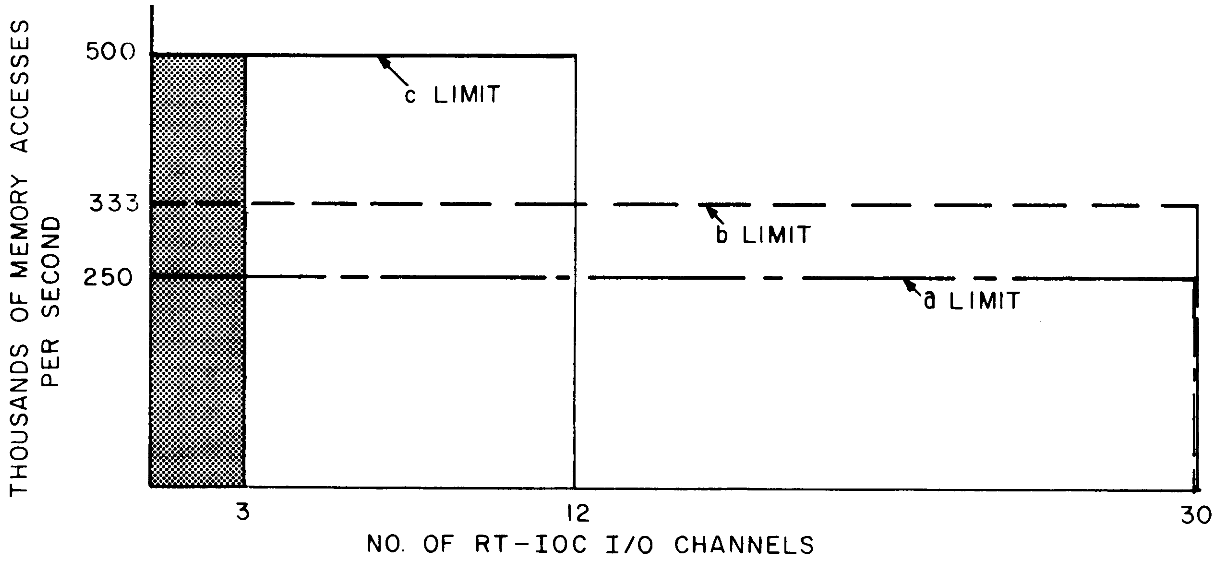


Figure I-2. RT-IOC Applications Chart

Line (a) is the upper limit of normal RT-IOC operation with the M-605, M-625, and GE-625. This limit may be approached while the memory is under concurrent access by other devices and permits the use of indirect addressing and the implementation of up to 27 payload I/O channels per RT-IOC.

Line (b) is the upper limit of normal RT-IOC operation with the GE-635. This limit may be approached while the memory is under concurrent access by other devices and permits the use of indirect addressing and the implementation of up to 27 payload I/O channels per RT-IOC.

Line (c) is the upper limit of modified RT-IOC operation with the GE-635. This limit may be approached while the memory is under concurrent access by other devices but does not permit the use of indirect addressing nor the implementation of more than 9 payload I/O channels per RT-IOC.

The crosshatch region represents the three RT-IOC internal channels which are not part of the user interface.

Having presented the three initial performance models, a technique for selecting the appropriate model for a given application may now be considered.

C. SELECTING THE APPROPRIATE RT-IOC PERFORMANCE MODEL

External user devices served by the I/O channels of the RT-IOC can be divided into two basic categories which are:

Category 1. Devices which will lose data or fault if not serviced at their specified data rate (telemetry sources for example).

Category 2. Devices which will merely slow down if not serviced at their specified rate but not lose data (such as the rate at which new plotting points appear on a cathode ray tube display).

The potential RT-IOC user may then sketch a plot of his category 1 and category 2 external devices on the RT-IOC applications chart to determine the model of RT-IOC required for his specific application. Category 1 devices should be plotted in additive fashion with respect to their data rates.

The high point of the category 1 plot will indicate the performance level of the RT-IOC model required. Category 2 devices should merely be entered with respect to the number of half-duplex RT-IOC I/O channels required to support each. The total horizontal excursion of both category 1 and 2 devices will indicate if more than one RT-IOC is required on the basis of quantity of channels. It should be noted that channel expanders can be supplied which permit up to 64 low data rate devices to be interfaced via each external I/O channel of the RT-IOC.

INITIAL RT/IOC PERFORMANCE MODELS	COMPUTERS USED WITH	MAXIMUM RT-IOC MEMORY ACCESSES/SEC	INDIRECT ADDRESSING AVAILABLE	MAX. NO. OF PAYLOAD I/O CHANNELS	CAPABILITY FOR DOUBLE-CYCLE (STORE-EXECUTE)	CAPABILITY FOR DIRECT BYTE MANIPULATION	NO. OF MEMORY MODULES ADDRESSABLE	NO. OF 36 BIT MEMORY LOCATIONS ADDRESSABLE	CAPABILITY FOR STD EXECUTE MULTIPLEXING	MAX BITS TRANSFERRED PER MEMORY ACCESS
a	M-605 M-625 GE-625	250,000	YES	27	YES	YES	4	262,144	YES	36
b	GE-635	333,000	YES	27	YES	YES	4	262,144	YES	36
c	GE-635	500,000	NO	9	NO	YES	4	262,144	NO	36

OTHER OPTIONAL FEATURES AVAILABLE

- AUTOMATIC PROGRAM LOADER OPTION
- INPUT/OUTPUT PARITY CHECKING AND GENERATION

Figure I-3. RT-IOC Specifications

D. SAMPLE APPLICATION EXERCISE

Assume that a given user has the following array of external devices which are to be interfaced with a GE-600 computer via the RT-IOC:

	Device	Character Rate	Category Assumed	Character Size
1.	Telemetry data source	100 KC	1	12 bits
2.	Tracking radar	20 cps	1	18 bits
3.	Mission Control Console With 10 display registers	static	2	36 bits
4.	Telephone data link (full duplex)	2 × 41 KC	1	serial

First, an external device adapter should be defined, when required, for each device to accomplish such functions as logic level shifting, pulse shaping, and any character collecting which might be desired. Secondly, a decision to employ either indirect addressing (the RT-IOC forms the memory address for each access) or direct addressing (the external adapter or the external device itself, forms the address) should be made for each device, as well as determining the number of half duplex RT-IOC I/O channels needed to support each adapter. For the given devices, their collective interfaces to the RT-IOC might be presented as follows:

	Device	Memory Addressing	Collection by Adapter	Resultant Access Rate
1.	Telemetry data source	Direct	None	100 KC
2.	Tracking radar data	Indirect	None	40 cps
3.	Mission Control Console with 10 Display Registers	Indirect	None	static
4.	Telephone data link	Indirect	6 bits/char.	27.4 KC
			Total	127,440 accesses/sec

The adapter for the telemetry source uses the direct technique which means that each access will be for the purpose of transferring data and the resultant rate is equal to the device rate.

The adapter for the tracking radar uses indirect addressing which means that for every data access, the RT-IOC will make an additional memory access to manipulate the indirect control word of the radar device, and the resulting rate is double the device data rate. The radar adapter is now greatly simplified relative to the telemetry adapter since it need not increment an address field or maintain a tally register.

The mission control console also will use indirect addressing, for simplicity, but its very low data rate remains essentially static.

The telephone adapter will collect 6 serial bits to form a character before interrupting the RT-IOC for access. Each access will be accompanied by a control word access and the resultant rate must also reflect the full duplex phone line's capability to carry on concurrent input and output requests. The equation for the resultant data rate of the phone line is then:

$$R_r = \frac{D\ I\ R_d}{C} = \frac{2\ (2)\ 41,000}{6} = 27.4\ \text{KC}$$

where D = full duplex factor = 2

I = factor due to indirect control word accessing = 2

R_d = basic rate of external device = 41 KC

C = character collection effect of the adapter = 6 bits/character

R_r = resultant access rate = 27,400 memory accesses per second.

The full duplex telephone adapter is assigned two half duplex RT-IOC I/O channels, unlike the other devices which are assigned one each.

The loading for the devices under consideration may then be plotted on the RT-IOC applications chart as follows:

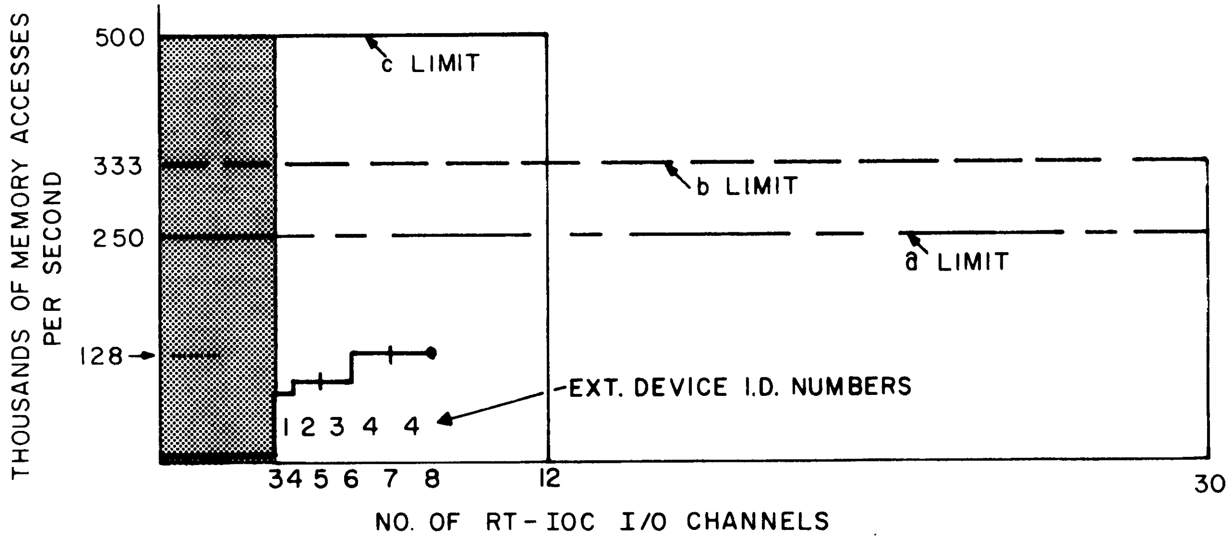


Figure I-4. Usage of the Applications Chart

The resultant plot indicates that the sample application could be accommodated by the "a" performance model of the RT-IOC, working with a 2 μsec. memory and using the indirect addressing feature. It should be noted that had the telemetry source also been assigned the indirect technique, its contribution would have been 200 KC and the "a" performance model RT-IOC would have contained correspondingly less I/O growth potential. The delivered RT-IOC would thus contain five implemented payload channels, three overhead channels, and as many spare channels as the user wishes to implement for estimated growth; up to a total of 30 channels for all functions of that RT-IOC module.

E. VARIATION IN PERFORMANCE LIMITS

The preceding example has illustrated a procedure for determining the memory access rate requirement, on the RT-IOC, as a function of the aggregate data transfer characteristics of the set of external devices being considered. This technique is suggested as a preliminary tool for sizing the RT/IOC to the needs of specific applications. While an access rate, so determined, is an accurate representation of how often an RT-IOC may be required to capture access cycles to the memory module, it does not take into consideration input/output conditions which can momentarily cause an excursion in the performance limit. An example of such an excursion occurs when the memory module does not receive concurrent access requests from other principal modules and thus, during such a period, the RT-IOC performance limit can be visualized as rising temporarily to a higher value.

Other circumstances can cause a temporary downward excursion of the performance limit such that the summation point for concurrent operation by category one devices must not exceed a reduced level without the protection of buffer techniques in the external device adapters. A condition under which this will occur is the period following a tally runout at the end of a block transfer using the indirect addressing technique such that more than two memory accesses are required to complete the servicing of the terminating external device. This effect would not occur with the "C" performance model since it does not use the indirecting feature. Another operational condition which may introduce buffer requirements is the initial "start-up" cycle of a high speed I/O channel after the current access cycle has already been committed to a different I/O channel.

Considerations of this nature are accounted for in each application during the system engineering phase of each real-time application of The Compatibles/600.

II. RT-IOC DESCRIPTION

The RT-IOC may be conveniently tailored to the specific needs of each installation. It can interface with from 1 to 4 memory modules and can provide up to 27 external half-duplex I/O channels per RT-IOC. Three additional channels are reserved for internal overhead functions. The major portion of the RT-IOC is fixed and invariant from one application to another while the I/O channel configurations and optional features implemented are set by the needs of the specific application.

As indicated in Section I, there are three performance models of the RT-IOC available, each defined mainly by the speed of the memory with which it is used. The choice of a model in turn affects the maximum number of I/O channels which may be implemented and whether or not such techniques as indirect addressing may be employed.

A. SUMMARY OF FEATURES

1. Memory Interface

The RT-IOC is designed to interface with any of the 600 line Memory modules using one of the memory ports for communication. One RT-IOC can communicate with up to 4 memory modules. The RT-IOC performs other transactions with the memory such as the setting of the program execute interrupt cells in addition to the transfer of data. Provision is made for the acknowledgment of faults signaled from the Memory module to the RT-IOC.

As with other 600 line principal modules, provision is made for the logical Memory address assignment of the four RT-IOC Memory channels. Furthermore, the fixed control locations utilized by the RT-IOC can be offset to lie within any 512 word block of storage. Thus, the control block locations can be placed in any memory module desired. When the user system is operating under the control of extended GECOS, the RT-IOC control block will be located in the master mode portion of the lower memory.

Each memory access by the RT-IOC is single precision and thus may transfer a maximum of 36 bits (the single precision word size of the GE-600 computers). Each RT-IOC is normally assigned 8 program execute interrupt cells in the memory controller of the memory module which contains its block of 512 control locations and hence is the control memory of that RT-IOC.

The control memory is defined as that memory module from which the RT-IOC accepts its initiation commands.

2. Data Transfer

The RT-IOC is designed to permit the external devices to specify the time and rate of data transfer and uses an interrupt priority chain for granting access in the same fashion as the Memory modules. Each I/O channel of the RT-IOC can be provided with different word size and transfer characteristics.

The RT-IOC can transmit and receive, from the user system, word sizes of up to 36 bits plus one parity bit. Although non-standard word sizes can be accommodated, the common word sizes accepted are (parity bit optional):

6 bits + parity

9 bits + parity

12 bits + parity

36 bits + parity

Characters are unpacked and stored in memory with six 6 bit characters, four 9 bit characters, three 12 bit characters or one 36 bit word per core memory location.

There are two basic methods of data transfer used: direct and indirect.

With the direct method of transfer, the external device adapter connected to the channel provides the core location address for each data transfer, and must contain sufficient logic to manipulate address and tally registers in the external device adapter. Each memory access, however, is devoted to data transfer.

Under the indirect transfer method, the RT-IOC relieves the external device of the task of addressing. Each time the external device makes an access request, the RT-IOC obtains from Memory an indirect control word which contains the address to either load or store the data and a tally specifying the number of words or characters to be transferred. The format of the indirect control words is substantially identical to the format of the indirect and tally address modifiers used by the 600 line Processors and is shown in a later paragraph. The external device using the indirect transfer method can specify the location of the indirect word using the address lines provided with each channel or a fixed address can be provided by the RT-IOC. Thus, an external device can have access to many indirect control words. For example, a 64 subchannel teletype demultiplexer/multiplexer can use a block of 64 indirect words with each indirect control word assigned to a subchannel. The address and character counting is then accomplished by the RT-IOC. For each data access to memory,however, a second access is required for the RT-IOC to increment the indirect control word.

In addition to the direct and indirect form of data transfer, there are two additional forms of static data transfer that can be used for either control or data transfer. Provision is made, using the CIOC instruction, to either send a control word to an external device or to request a reading of static lines presented to the RT-IOC by an external device (status lines for example).

3. Hardware Aspects of I/O Initiation

Each implemented channel of an RT-IOC will be assigned either an asynchronous interrupt technique or a synchronous program control technique for the initiation of data transfer, depending on the role a given external device is to play in the operation of the total system.

In the asynchronous case, the external device determines when a data transfer is desired and "raises" its interrupt line, address lines and one or more command lines. The transfer request would then be recognized and serviced on the basis of the given I/O channel's position in the RT-IOC data channel interrupt chain.

I/O channels initiated on a synchronous program control basis are served as the result of the execution of the instruction CIOC (Connect Input/Output Channel) which is found in the initiate portion of RT-IOS, which in turn had been initiated at the request of a user program. Once these channels have been initiated on a program control basis they require no further program attention. Each channel then interrupts at its own data transfer rate and continues until the specified block of data has been transferred. At the end of the transaction, the external device sends a program execute interrupt to the computer which indicates to the program that the specified block has been transferred and the external device is ready for another transaction.

4. Program Execute Interrupt Provisions

Eight program execute interrupt cells are normally reserved for each RT-IOC in the system. The 8 cells must be in the same Memory module as the block of 512 control locations. For some applications the RT-IOC may use the 8 interrupt cells in conjunction with 8 fixed wired core locations to establish an effective program execute interrupt chain of 240 cells. Using this technique each of the 30 channels may have 8 unique levels of program interrupt priority. Thus, upon program interruption, the program may examine the core location corresponding to the execute interrupt cell and determine which of the 30 channels caused the execute interrupt. In many applications, however, 8 cells are adequate such that each may have only one discrete meaning when it occurs, and thus not require demultiplexing. In some applications it is also possible to modify the RT-IOC so that more than 8 discrete execute cells may be set.

Three of the RT-IOC channels are reserved for internal RT-IOC functions (CIOC, status, fault). These three channels can share the 8 execute cells with the 27 external channels in the way described above. No distinction is made between internal or externally generated execute interrupts. The maintenance panel of the RT-IOC also uses an I/O channel. This channel may be provided by sharing a payload channel not needed in the test mode, or by assigning a channel for full time availability to the maintenance panel as a fourth overhead channel.

Each of the 8 program execute interrupt cells assigned to the RT-IOC can be set from the maintenance panel of the RT-IOC.

5. I/O Channel Mask

Associated with the 30 channels is an I/O channel mask register, each bit of which corresponds to one of the 30 channels. The channel mask can be read or its contents changed by the use of the CIOC instruction. The mask is used in the same fashion as the channel mask in the Memory to inhibit the acknowledgment of I/O data channel interrupts. Mask word bits in the "1" state turn on a channel and bits in the "0" state turn off a channel. When the channel mask is set so as to inhibit acknowledgment of memory access requests, a level is sent via the "Channel Masked" line to the external device and is normally used to halt or initialize the device.

6. I/O Parity (Optional)

Parity generation and checking logic is available in the RT-IOC as an optional feature. All parity checking and generation is between the RT-IOC and the external devices connected to the RT-IOC. Parity generation is accomplished for 6, 9, or 12 bit characters or for 36 bit words with a parity bit added in each case. Parity is checked for incoming 6, 9, or 12 bit characters and for incoming 36 bit words. In the event of parity error detection for received data, the RT-IOC raises the Parity Error line to the external device to indicate the occurrence of the parity error. The device may then generate a program execute interrupt, or as an option the RT-IOC can generate the execute interrupt internally without the intervention of the external device.

If a non-standard word size is used (i.e., other than 6, 9, 12, or 36 bits + parity), unused bits from storage must be zero in the case of output data.

7. Fault Provisions

In the event a fault is indicated by a Memory with which the RT-IOC is transferring information, the fault coded on the illegal action lines by the Memory is stored in a Fault Register in the RT-IOC and an execute interrupt is generated. The RT-IOC will automatically mask the I/O channel related to the fault. The contents of the Fault Register can be read by program control using the CIOC instruction as described in a later paragraph.

8. Automatic Program Loader Option

As an optional feature, an Automatic Program Loader Option is available in the RT-IOC. The loader, upon receiving a signal from a remote source, will store in Memory a loader program and will force the Processor to execute the loader. This short routine will bring in a start-up program from a selected peripheral device.

The loader option included within the RT-IOC can be used in conjunction with any peripheral in the system including peripherals that interface through a standard IOC. The peripheral to be used can be plug-board selected and changed at will in the RT-IOC. The loader uses one I/O channel interrupt cell of the RT-IOC and will share one program execute interrupt cell in the memory controller module.

The loader initiation signal (from a user console) will override the masking of the RT-IOC memory port in the memory module.

9. Memory Reassignment

All principal modules (those which interface directly with the memory module as does the RT-IOC) of the Compatibles/600, are capable of participating in reconfiguration of the system. This has been made possible by the fact that each principal module can place an address bias on the interface to a given memory. This is accomplished by manually setting the memory address assignment bits on the maintenance panels of the principal modules, thus controlling the address range by which the principal module "views" the memory module. The result is that a given physical memory module, which may have represented memory locations 0 through 65,536 for example, can be taken off-line for such purposes as preventative maintenance while a different physical memory module assumes the role of locations 0 through 65,536.

B. DETAILED DESCRIPTION

1. I/O Channel External Interface

The following is a list of the data, address, command, and strobe lines that may be associated with each of the 30 channels. All lines may be required by the external device in some cases; in other cases, only a portion of the lines may be needed and hence provided.

a. Data Lines-input - 37 maximum

One of the following options:

(1) 6 bit + parity

(2) 9 bit + parity

(3) 12 bit + parity

(4) 36 bit + parity

(parity bit is optional)

b. Data Lines-output - 37 maximum

(1) 6 bit + parity

(2) 9 bit + parity

(3) 12 bit + parity

(4) 36 bit + parity

(parity bit is optional)

c. Address Lines - 18 maximum

One of the following options:

(1) 6 lines

(2) 12 lines

(3) 18 lines

d. Byte Lines - 8

e. Command Lines - input

(1) Direct/Indirect

(2) Store

(3) Load

(4) Execute (program interrupt)

(5) Execute Function A

(6) Execute Function B

(7) Execute Function C

f. Status Line-input - 2 (Busy, Ready)

g. Flag Lines-output

(1) Tally runout - 1

(2) Parity Error - 1

(3) Channel Masked - 1

h. Strobe Line-input

(1) Memory Access Request (I/O data channel interrupt)

i. Strobe Line-output

(1) Memory Access Request answer strobe

(2) CIOC (connect) strobe

2. Operation

a. DATA TRANSFER

(1) Direct

A binary 1 on the Direct/Indirect command line specifies that a direct data transfer is to take place. A binary 0 specifies indirect. Under the direct transfer, the data on the input data lines is placed in the core location specified by the address lines if the Store command line is a binary 1. If the load command line is a binary 1, the contents of the core location specified by the address lines is placed on the output data lines accompanied by a pulse on the Answer Strobe line.

If each data transfer for a given channel is 36 bits, the Byte lines can be wired to the proper value in the RT-IOC. If the data transfer is 6, 9, or 12 bits, the external device adapter will use the byte lines to specify the byte position. For input data, the right justified byte (6, 9, or 12 bits in length) is placed in storage in the specified byte position. For data output, the contents of the core byte position specified by the byte lines is placed on the output data lines in the right justified position. The byte lines can be used only with the direct transfer and are ignored for indirect.

In order to permit a byte to be transferred into or out of a specific byte position of a memory location, the memory module defines eight zones within each memory location and accepts eight zone control lines from the RT-IOC. By manipulating combinations of these lines, the RT-IOC is able to place 6, 9, or 12 bit bytes in the character positions desired.

The zones of a memory location are defined as follows:

6	3	3	6	6	3	3	6
Z_0	Z_{1U}	Z_{1L}	Z_2	Z_3	Z_{4U}	Z_{4L}	Z_5
0							35

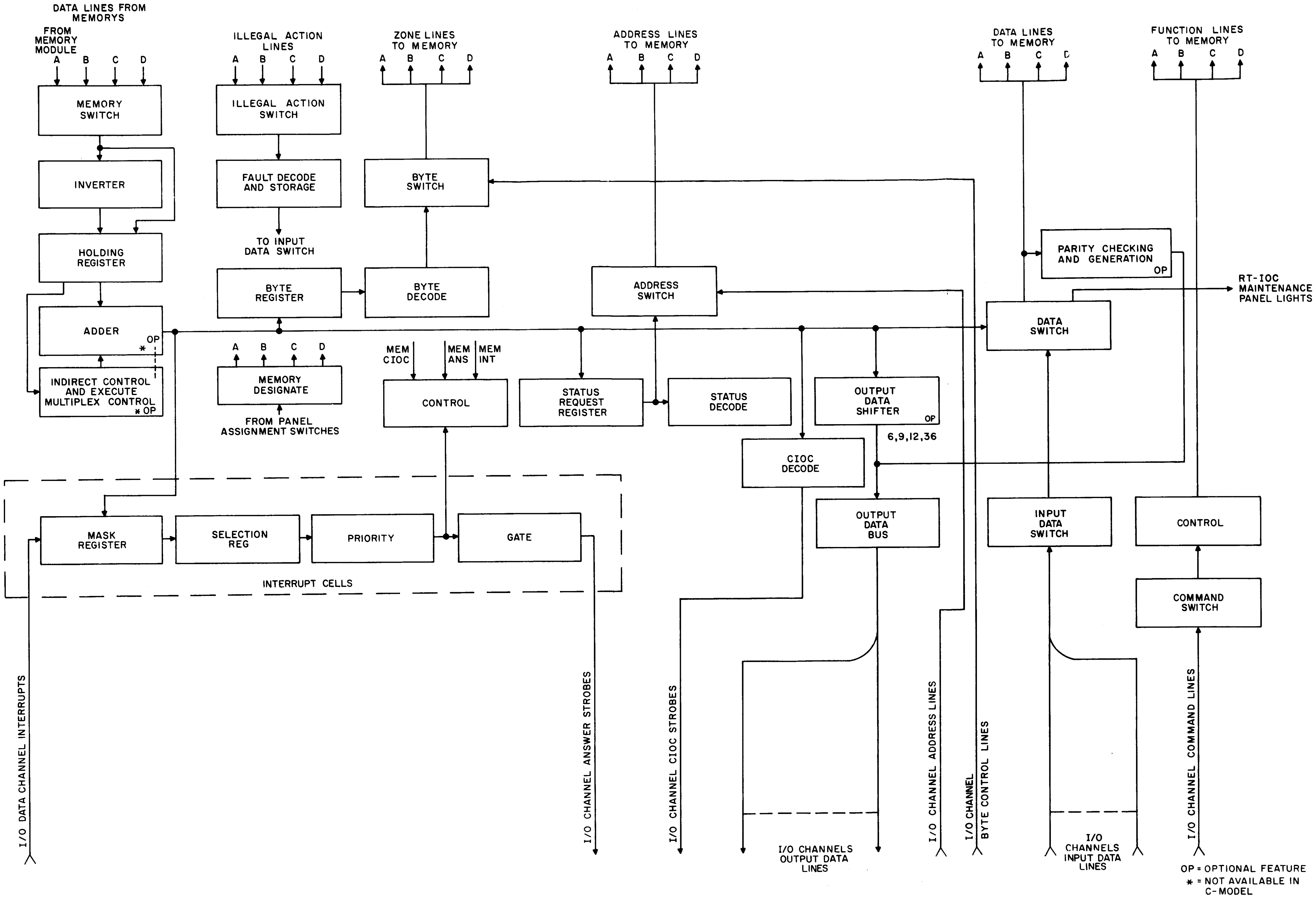


Figure II-1. Simplified Functional Diagram

Each I/O channel of the RT-IOC has 8 byte command lines corresponding to the 8 zones indicated. The following table shows the combined usage of the byte lines for 6, 9, and 12 bit bytes in order to load or store a byte in a specified byte position of the memory location.

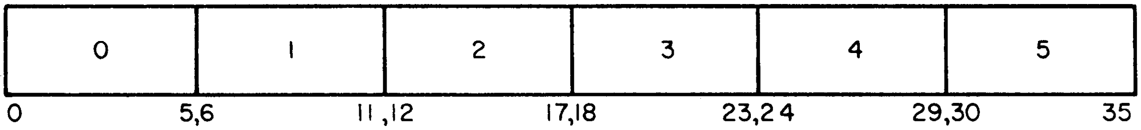
Byte Line Combinations Versus Byte Position Desired

Byte Position	Byte size: 6 bit	9 bit	12 bit	36 bit
0	Z_0	$Z_0 \cdot Z_{1U}$	$Z_0 \cdot Z_{1U} \cdot Z_{1L}$	All Lines
1	$Z_{1U} \cdot Z_{1L}$	$Z_{1L} \cdot Z_2$	$Z_{\dot{2}}Z_3$	--
2	Z_2	$Z_3 \cdot Z_{4U}$	$Z_{4U} \cdot Z_{4L} \cdot Z_5$	--
3	Z_3	$Z_{4L} \cdot Z_5$	--	--
4	$Z_{4U} \cdot Z_{4L}$	--	--	--
5	Z_5	--	--	--

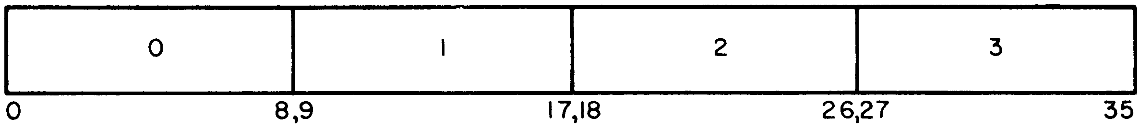
All other line combinations are invalid.

The byte positions within a word are defined as follows:

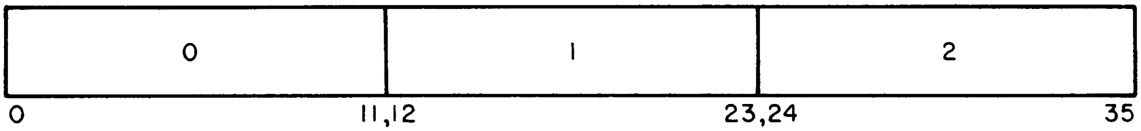
6 BIT BYTES



9 BIT BYTES



12 BIT BYTES



(2) Indirect

Using the indirect transfer, the RT-IOC will access the core location specified by the address lines and perform a Read-Alter-Rewrite cycle. The information obtained is an indirect control word which provides the address for the data transfer and maintains a running tally of the number of words to be transferred. The format of the indirect control word is as follows:

18	12	1	2	3
Y	T	E	C	B
0 17	18 29	30	31 32	33 35

The address field, y, initially specifies the memory starting location of the block to be transferred, and is incremented after each location is serviced.

The tally field, T, initially specifies the number of words or bytes to be transferred.

The execute bit, E, is examined by the RT-IOC to determine when the specified number of words has been transferred.

The control field, C, is used to specify the byte size involved in the indirect data transfer:

binary values of C	type, and byte size, of indirect transaction
00	Indirect 6
01	Indirect 9
10	Indirect 12
11	Indirect 36

The Byte position field, B, is used to specify the byte position for the current transfer to or from the memory location specified by the address field, y. When C = 11_2, B must contain 0.

For indirect 6, (C = 00), B may have the following values and interpretations:

B	Byte Position
0_8	$C(Y)_{0-5}$
1_8	$C(Y)_{6-11}$
2_8	$C(Y)_{12-17}$
3_8	$C(Y)_{18-23}$
4_8	$C(Y)_{24-29}$
5_8	$C(Y)_{30-35}$

For indirect 9 (C = 01), B may have the following values and interpretations:

B	Byte Position
0_8	$C(Y)_{0-8}$
1_8	$C(Y)_{9-17}$
2_8	$C(Y)_{18-26}$
3_8	$C(Y)_{27-35}$

For indirect 12 (C = 10), B may have the following values and interpretations:

B	Byte Position
0_8	$C(Y)_{0-11}$
1_8	$C(Y)_{12-23}$
2_8	$C(Y)_{24-35}$

Each time the external device makes an access request, the indirect word is brought from memory, altered and restored to core. For indirect 36, the address field is incremented and the Tally field is decremented for each reference to the indirect word. For indirect 6, 9, or 12, the Byte field is incremented and the tally field is decremented as each character is transferred. When B equals 5_8 in the case of indirect 6, 3_8 in the case of indirect 9, or 2_8 in the case of indirect 12, the address is incremented and the Byte field is reset to 0.

The unincremented information in the Address, Tally, and Byte field is used for the transfer of data, and then the alteration of the indirect control word is performed.

If during a reference to the indirect word the tally goes to zero, the execute bit is set to a binary 1 and the address field is incremented by one. The data transfer takes place and a Tally run-out flag is sent to the external device.

In response to the Tally run-out flag presented to the external device, the device will cause a program execute interrupt. As an option, the RT-IOC can automatically cause the proper program execute interrupt without the intervention of the external device.

b. PROGRAM EXECUTE INTERRUPTS

The execute command line is used by the external device to initiate a program execute interrupt.

When a device puts a pulse on the Memory Access Request line accompanied by a binary 1 on the Execute command line, the RT-IOC will set one of the eight execute interrupt cells assigned specifically to that RT-IOC in the control Memory module. The coded execute function command lines indicate which of the 8 cells to set.

For those applications in which it is elected to use the execute multiplexing technique, the RT-IOC will perform as follows:

Prior to setting the designated cell, the RT-IOC will OR a binary one into one of eight core locations, each of which corresponds to one of the eight execute interrupt cells. The first bit position of each of the eight words corresponds to channel 0; each succeeding bit position likewise corresponds to one of the 30 channels.

Thus, upon acknowledgment of an execute interrupt, the program scans the core location unique to that execute interrupt to determine the channel causing the interrupt. When this procedure is used, up to 240 different events can be conveyed to the program via the eight execute interrupt cells assigned to each RT-IOC.

It should be noted that it is possible to raise both the Execute command line and the Store or Load command line simultaneously. Following acknowledgment of the memory access request, the RT-IOC will store/load the data and then carry out the specified execute interrupt operation just described.

The three Execute Function Lines shall be manipulated by the external device adapter as follows:

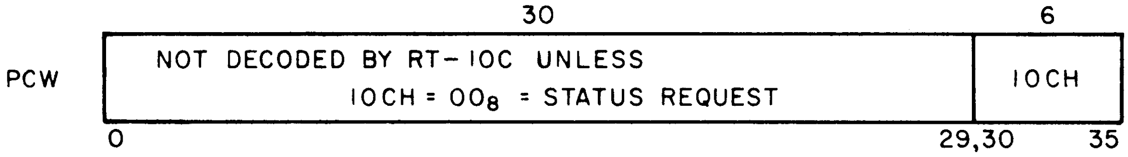
	(Execute function lines)		
	C	B	A
Execute 0	0	0	0
Execute 1	0	0	1
Execute 2	0	1	0
Execute 3	0	1	1
Execute 4	1	0	0
Execute 5	1	0	1
Execute 6	1	1	0
Execute 7	1	1	1

c. PROGRAM CONTROL AND STATUS REGISTER TRANSACTIONS

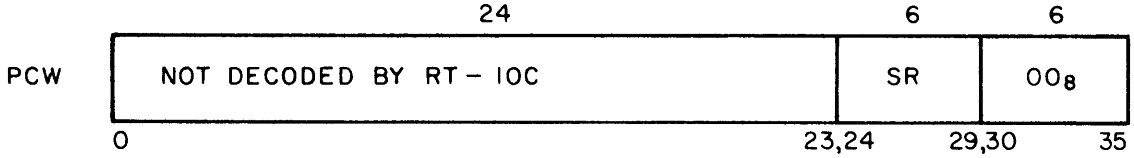
Program control of the external devices and of the RT-IOC itself is accomplished by the use of the basic CIOC instruction. Furthermore, the CIOC instruction can be used by the program to read static information either in the form of status within the RT-IOC, or static information from external devices.

Program controlled transactions, via the RT-IOC, are specified by various PCW's (Peripheral Control Words) which are placed in the RT-IOC mailbox. The program advises the RT-IOC to consult its mailbox (a fixed location) by executing a CIOC instruction, the address field of which specifies a core location containing a bit pattern which directs a strobe pulse to the memory port on which the RT-IOC resides. The RT-IOC interprets the occurrence of this strobe to mean that a new PCW has been placed in the RT-IOC mailbox. The RT-IOC then accesses the memory while addressing the mailbox location, and thus receives the new PCW.

After the RT-IOC obtains a PCW in the above manner, the RT-IOC decodes the lower six bits of the PCW to determine the IOCH (Input/Output Channel) over which the upper 30 bits of the PCW is to be transmitted, or to determine which internal RT-IOC overhead function is to be performed. The RT-IOC thus regards the PCW as follows:



If the IOCH field (bits 30 thru 35) is equal to 00_8, then the PCW is further decoded by the RT-IOC as follows:



The RT-IOC thus may also decode the Status Request (SR) field (bits 24-29) to determine what type of status this PCW is requesting.

Generally, however, the PCW will not be a status request and the RT-IOC will transmit the undecoded upper 30 bits of the PCW on out to the external device specified by the contents of the IOCH field, or perform another overhead function specified by the contents of IOCH which does not require further decoding such as "load RT-IOC channel mask register".

After the RT-IOC receives a PCW from the RT-IOC mailbox of the control memory, the RT-IOC will set its CIOC execute cell indicating to the program that the previous PCW has been taken and the mailbox is now "cleared" for a new PCW.

The IOCH field of the PCW is decoded into one of 32 (up to 64 by factory option) possible states. Normally, one CIOC strobe is associated with each of the 27 external channels and 5 additional serve for internal RT-IOC usage. The upper portion of the PCW, obtained from storage, is placed on the channel output data lines accompanied by the CIOC strobe. Thus, the upper 30 bits may be used by external devices for further control purposes in accordance with any format required by and defined for the external device.

A format commonly used for peripheral devices employs the high order 30 bits in the following fashion:

bits 0-17, Primary Address - specifies data address, control word address, status address, or mag tape delay number.

bits 18-23,	Operation	- command to controller such as read, write, or rewind.
bits 24-29,	Device Identification	- used to select particular subunit of the external device (such as tape transport number 3).

For 36 bit channels, the upper 30 bits of the PCW are placed on the output data lines. For 6, 9, and 12 bit channels, the following portions of the control word are put on the output data lines:

Channel Size	PCW Bit Positions transmitted
6 bit	18-23 (operation)
9 bit	15-23 (operation and partial address)
12 bit	12-23 (operation and partial address)

The five additional CIOC strobes (IOCH decodes) not associated with the external channels are used for the following internal RT-IOC functions:

Function	IOCH Value
(1) Status Request	00_8
(2) Load Channel Mask	01_8
(3) Spare	02_8
(4) (Reserved for future assignment)	03_8
(5) Spare	04_8

In the case of the Channel Mask, the upper 30 bits of the PCW are placed in the channel mask register, each bit of which corresponds to one of the 30 channels. A binary "0" inhibits the acknowledgment of memory access requests and cancels any interrupt that may be awaiting acknowledgment.

The IOCH decode (IOCH=00_8) is reserved for status requests. When this code is used, the SR (Status Request) field of the PCW is placed in a register in the RT-IOC and the status channel interrupt cell is set. When the interrupt is acknowledged, the 6 bits in the register are decoded to one of 64 possible states and used to select one of up to 64 possible static inputs which is then stored in Memory at one of 64 corresponding fixed address locations within the RT-IOC control block. The register output serves as the least significant 6 bits of the address for the store operation.

Internal RT-IOC functions which can be read via a status request are:

	Function	SR Value
(a)	Read Channel Busy Status	00_8
(b)	Read Channel Mask Register	01_8
(c)	Read Fault Register	02_8
(d)	(Reserved for future assignment)	03_8
(e)	Read General Status	04_8

External devices which offer status information will each be assigned an SR code, as a continuation of the above list, for each specific installation.

The channel busy status consists of one bit for each of the maximum of 27 external devices. One status line, included in the list of channel lines, is the busy line and is used to indicate device "busy."

Following the storage of any of the status returns, in one of the fixed address locations, the RT-IOC will set the status execute interrupt, indicating to the program that the requested status reading has been stored in memory.

d. DATA CONTROL WORDS (DCW'S)

Some external device transactions cannot be initiated on the basis of the amount of information which can be expressed in the upper 30 bits of a PCW. Some external devices are required to transfer many scattered blocks of data such that program participation may not be desired until the entire process has been completed. For such operations, when the indirect addressing technique is not used, another technique involving the use of DCW's (Data Control Words) is available.

The DCW is decoded by the external device adapter and its format will be unique to the needs of that device. The device adapter locates the DCW, or the beginning of a queue of DCW's (some external devices utilize a queue of pairs of DCW's) by virture of a pointer conveyed to it within the upper 30 bits of the PCW. Therefore, the initiating program employs the CIOC instruction in the usual way, but in this case the PCW is merely used to direct the external device adapter to a list of one or more DCW's. The queue of DCW's need not be of a specified length, since the adapter can be designed to take a new DCW from the list after each block transfer is finished, and continue to do so until a DCW is encountered which contains a "disconnect" bit in the "set" state. After finally exhausting the queue in this way, the adapter will request the RT-IOC to set a program execute interrupt cell, indicating to the program that all of the blocks of data associated with a given queue have been transferred.

The 36 bit DCW format is typically used to contain the following kind of control information.

- Data block memory starting address - up to 18 bits
- Block tally field for counting number of words transferred

- Disconnect bit, for indicating the last DCW in a queue of DCW's
- Device address field, for cases in which the external device exhibits the characteristics of an external memory
- Distribution field, for external devices possessing two or more subunits
- Command field, for external devices possessing a repertoire of peripheral operations.

e. FAULT PROCESSING

There are six faults defined for the RT-IOC. Five are called to the attention of the RT-IOC via the illegal action lines from the memory and one is detected by the RT-IOC. The faults are described as follows.

F_0 - Not Control
This fault is declared by the memory when a principal module (such as the RT-IOC) attempts to read or set the execute mask, the memory channel mask, or the file protect register and is not designated as the control module.

F_1 - Not Master
This fault is declared by the memory when a principal module attempts to set a program execute interrupt cell and the principal module is not in the master mode.

F_2 - Protected Area
Memory modules equipped with the file protect register will declare this fault if a principal module attempts to address a protected region of memory, and did not first place a "1" on the protect command line.

F_3 - Non-Existent Address
The memory module will declare this fault if a principal module attempts to present an address value not contained in the range of that memory. This would occur when attempting an address between 40,960 and 65,536 to a memory module only containing 40,960 locations.

F_4 - Memory Parity
The memory module will declare this fault if a memory parity error occurs during a read transaction to a given principal module.

F_5 - Interrupt Not Answered
The memory fails to respond to the RT-IOC access request within a fixed number of microseconds.

The action taken by the RT-IOC, after the occurrence of any of these faults is as follows.

The RT-IOC will mask (turn off) the interrupt cell of the I/O channel associated with the faulting transaction and send a flag to the external device to advise it that it has been involved in a fault and is masked off.

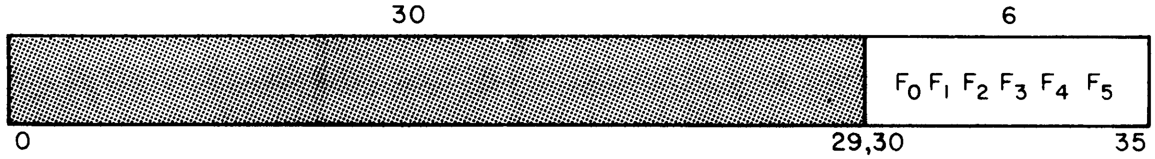
The RT-IOC also sets the appropriate fault description bit of the RT-IOC fault register and sets the channel interrupt cell assigned to the RT-IOC overhead fault channel.

When the requested memory cycle is granted, the RT-IOC uses it to set the RT-IOC fault execute cell in the memory controller.

The user program which responds to the RT-IOC faults may then initiate the CIOC's which request the RT-IOC to store the contents of the RT-IOC channel mask and fault registers.

The channel mask word may be interpreted by the program on the basis that bit position corresponds to I/O channel number, and masked channels will be in the zero state.

The fault word may be interpreted according to the following format, with declared faults set to the "one" state.



Contents of Fault Register Return Word

3. Supporting Software

GECOS (General Comprehensive Operating Supervisor) is the operating system for the Compatibles/600. Standard GECOS is designed to supervise the data processing activities of the GE-635 and GE-625 systems in "job shop" applications, while a derivative of GECOS (GECOS/M-605) is used with the M-605 in mission oriented applications, and an extended version of GECOS is used with the GE-635, GE-625 and M-625 in those applications which have both real-time and job shop requirements. In any system in which the RT-IOC is employed, the linkage between GECOS and the RT-IOC resides in the software module called RT-IOS (Real-Time Input/Output Supervisor). RT-IOS consists of a set of program execute interrupt handler routines peculiar to the needs of external devices served by a given RT-IOC, plus an I/O initiate portion, and provides the RT-IOC with services somewhat parallel to the services performed by GEIOS (General Input-Output Supervisor) for the standard IOC equipment module.

The essential features of RT-IOS may be described as follows.

a. REAL-TIME INPUT/OUTPUT SUPERVISOR

The RT-IOS is functionally an extension of the Input/Output Supervisor (GEIOS) and therefore encompasses all of the features of GEIOS such as symbolic to physical unit translation, supervision of interrupts, and queuing of I/O requests.

The function of the RT-IOS is to perform input/output operations for those devices attached to the RT-IOC and any special devices that may be attached to separate memory ports. The interface between the user programs and RT-IOS is consistent with the interface between user programs and GEIOS.

The execution of input/output commands consist of two parts: initiation and termination. When a user program wishes to initiate input/output it executes a master mode entry (MME instruction) which is followed by a select sequence specifying additional information pertaining to the input/output operation.

Whenever an input/output operation performed by RT-IOS terminates, control is given to the appropriate termination portion of RT-IOS and all registers and indicators for the interrupted program are safe stored.

RT-IOS returns any requested status of the device to the program which requested this terminating input/output operation and removes the terminated request from this queue for the device involved. If there should be another queued request which can now be serviced RT-IOS will immediately initiate this pertinent I/O action.

b. INPUT/OUTPUT INITIATION

In the form that is most frequently used, a request to perform input/output can be expressed in terms of the following select sequence:

Master Mode Entry	MME
Operation Word	I/O command to be executed
Identification Word	File Pointer, DCW Pointer
Return Word	Status return pointer, Courtesy Call Address

This is the form used in GEIOS. The file pointer in this case indicates that the device is controlled by the RT-IOC and RT-IOS will perform the I/O operation.

Although the above calling sequence will handle many devices, there exist some devices in which it becomes necessary to extend the sequence in order to perform the required I/O operation. For these special cases, the basic calling sequence may be extended to include whatever information is necessary.

c. RT-IOC CONTROL AND COMMUNICATIONS BLOCK

The RT-IOC module is normally supported by a 512 word block of core locations in the control memory module. The block is general in that it will support different models of the RT-IOC in diverse applications. While some segments of the block may not be in use for a given application, it is subject to a standard map within certain portions of the block related to invariant features of the RT-IOC. The block map may be shown as follows:

Octal	
A + 000	Channel busy status return location
001	Channel mask status return location
002	Fault register return location
003	(Reserved for future assignment)
004	General status return location
005 . . 077	Specific external device status return locations
100 . . 107	Reserved for eight execute multiplexing words
110	RT-IOC Mailbox - (PCW location)
111 . . . . A + 777	This region's usage is unique for each real-time installation. Typical usages are: 1. Alternate input buffer areas 2. Indirect control words for each indirect user channel 3. Flag tables 4. Mailboxes for unique devices 5. Queues of DCW's (Data Control Words)

The RT-IOC permits the manual relocation of the above block, address-wise, to any location of memory, moving in increments of 512 locations.

APPENDIX A
RT-IOC CHANNEL EXPANDERS

Real-time applications frequently include large numbers of static and low data rate external devices. If such devices were each given an RT-IOC I/O channel, the available channels could thus become assigned without making any appreciable load on the data transfer rate capability of that RT-IOC. Consequently, I/O channel multiplexing devices are available for use with the RT-IOC which have the effect of "fanning-out" each I/O channel into many subchannels. These devices are the

IDM-32 and IDM-64	32 and 64 subchannel Input Data Multiplexers

and the

ODD-32 and ODD-64	32 and 64 subchannel Output Data Demultiplexer

Each type consists of a control and a switching segment. The control function performs the necessary timing and control to carry out the scanning and acknowledgment of the external subchannel access requests. This function is common to both types and includes a maintenance test control panel and power supply.

The switching segment of the multiplexers is tailored to the quantity and byte-size requirements of the user devices and is implemented in the standard byte sizes according to the needs of each subchannel.

The IDM provides the means of compressing as many as 32 and 64 input data subchannels into one RT-IOC half-duplex channel. This is accomplished by sequentially scanning all subchannels at a 5 mc rate and halting to service any requesting subchannel. The scan will resume after the RT-IOC completes the given store transaction and therefore the time required will be a function of the RT-IOC model used and the position of the IDM in the chain of RT-IOC I/O channel interrupt cells. The IDM is also capable of a manual "step" mode of operation, for test purposes. An optional feature is the use of input data registers to collect characters from serial devices and to relieve user devices from having to "wait for the scan."

The ODD provides the means of expanding a half-duplex RT-IOC channel in order to provide output data for up to 32 and 64 external devices, and employs a scan technique similar to that of the IDM.

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