



# **1343 disk controller**

88A00116A-B



**GENERAL AUTOMATION, INC.**

PRICE \$7.50  
88A00116A-B

## ***TECHNICAL MANUAL***

# **1343 DISK CONTROLLER**

***GENERAL AUTOMATION, INC.***

1055 East Street, Anaheim, California 92805 (714) 778-4800

© 1971, 1972, General Automation, Inc.



REVISION

<u>Symbol</u>	<u>Description</u>	<u>Manager Publications</u>	<u>Approved</u>	<u>Date</u>
A	Production Release			Feb 71
B	Added SPC-16 Programming Information, section 3	<i>RCM</i>	<i>R&amp;B</i>	Aug 71



CONTENTS

<u>Section</u>	<u>Title</u>	<u>Page</u>
1	INTRODUCTION	1-1
	1.1 General	1-1
	1.2 Model 1343 Disk Storage Unit	1-3
	1.2.1 Recalibrate (Restore)	1-4
	1.2.2 Program Seek	1-4
	1.2.3 Read/Write	1-4
	1.2.4 Linear Positioner	1-6
	1.2.5 Read/Write Heads	1-6
	1.3 Disk Formats	1-7
	1.4 Model 1343 Disk Controller	1-10
	1.4.1 Installation and Cabling	1-11
	1.4.2 System Configuration	1-11
2	CONTROLLER PROGRAMMING FOR 18/30 SYSTEM	2-1
	2.1 General	2-1
	2.2 Command and Timing	2-1
	2.2.1 Control	2-1
	2.2.2 Sense Device	2-4
	2.2.3 Sense Interrupt Level	2-9
	2.2.4 Initiate Read	2-10
	2.2.5 Initiate Write	2-14
	2.2.6 Initial Program Load	2-16
	2.3 Device Addressing (Area Code and Interrupts)	2-16
	2.3.1 Addressing	2-16
	2.3.2 Interrupts (Standard Equipment)	2-16
	2.4 18/30 Device Status Words	2-16
3	CONTROLLER PROGRAMMING FOR SPC-16 SYSTEM	3-1
	3.1 General	3-1
	3.2 Input/Output Commands	3-3
	3.2.1 Control Command Execution	3-7
	3.2.2 Sense Device Command Execution	3-9
	3.2.3 Initiate Read Command	3-13
	3.2.4 Initiate Write Command Execution	3-17
	3.2.5 Sense Interrupt Level	3-20
	3.2.6 Multiplex Data Channel (MDC8)	3-21
	3.2.7 SPC-16 Device Status Words	3-21

**CONTENTS (continued)**

<u>Section</u>	<u>Title</u>	<u>Page</u>
4	MAINTENANCE	4-1
	4.1 General	4-1
	4.2 Mnemonic Definitions	4-1
	4.3 Function Descriptions	4-23
	4.3.1 Data Buffer and Word Counter	4-23
	4.3.2 Signal Board	4-24
	4.3.3 Control Board	4-27
	4.3.4 DC Board	4-27
	4.3.5 Data Board	4-27
	4.3.6 Phase Lock System	4-30
	4.4 Theory of Operation	4-37
	4.4.1 Control and Sequencing	4-37
	4.4.2 Status Gates	4-44
	4.4.3 Interrupt Logic	4-51
	4.4.4 Write Data and Read Data	4-51
Appendix A	INSTALLATION	A-1
<u>Figures</u>		
1-1	Disk Characteristics	1-8
1-2	Disk Track Representation	1-9
1-3	Disk Sector Configuration	1-9
1-4	Model 1343 Controller Boards	1-11
1-5	System Configuration	1-12
2-1	Control Command Timing (Applies to 1804 Processor)	2-3
2-2	Sense Device Command Timing (Applies to 1804 Processor)	2-4
2-3	Disk Controller Device Status Word	2-5
2-4	Sense Interrupt Timing (Applies to 1804 Processor)	2-10
2-5	Initiate Read Timing (Applies Only to 1804 Processor)	2-13
2-6	Initiate Write Timing (Applies to 1804 Processor)	2-15
2-7	18/30 Device Status Words	2-17/18
3-1	SPC-16 Interface System	3-2
3-2	XIO Command	3-3
3-3	DTOR/DTOM and DTIR/DTIM Examples	3-4
3-4	Object Word Example	3-6
3-5	CONT and SEND Timing	3-10
3-6	Model 1343 Disk Controller Device Status Word	3-11
3-7	INRE/INWT Timing	3-14



CONTENTS (continued)

<u>Figures</u>	<u>Title</u>	<u>Page</u>
3-8	INRE/INWT Timing with MDC8 (Non-Chaining)	3-15
3-9	SPC-16 Device Status Words	3-22
4-1	Raw Data Characteristics	4-31
4-2	One Shot Timing	4-31
4-3	Phase Lock System	4-33
4-4	Error Detection Operation	4-34
4-5	Decoder Timing	4-35
4-6	Implement the Phase Detector Into a System	4-36
4-7	Out of Phase Condition Resulting from Tracking Raw Data	4-36
4-8	Disk Controller Block Diagram	4-38
4-9	Initiate Read/Initiate Write	4-39
4-10	Read Operational Flowchart	4-40
4-11	Write Operation Flowchart	4-40
4-12	Initiate Read/Initiate Write Command Initiation Timing	4-41
4-13	Initiate Read/Read Check Command Timing	4-42
4-14	Initiate Write Operation Timing	4-43
4-15	Control Command Flowchart	4-45
4-16	Restore Operation Flowchart	4-46
4-17	Control Command Timing	4-47
4-18	IPL Operation Flowchart	4-48
4-19	IPL Operation Timing	4-49
4-20	Sense Device Command Flowchart	4-50
4-21	Write Data and Read Data	4-52
A-1	Disk Controller Installation	A-1

<u>Tables</u>	<u>Title</u>	<u>Page</u>
1-1	Model 1343 Disk Controller Specifications	1-2
1-2	MOD 4 Check Bit Pattern	1-10
2-1	Control Command Operations and Disk Number Decode	2-2
2-2	Head Number Decode	2-11
2-3	Sector Decode	2-12
3-1	Register Identifier Codes	3-5
3-2	Control Command Operations and Disk Number Decode	3-8
4-1	Data Buffer and Word Counter Mnemonics	4-2
4-2	Signal Board Mnemonics	4-5
4-3	Signal Board Mnemonics	4-8
4-4	Control Board Mnemonics	4-10
4-5	DC Board Mnemonics	4-13
4-6	DC Board Mnemonics	4-16
4-7	Data Board Mnemonics	4-19



CONTENTS (continued)

<u>Tables</u>	<u>Title</u>	<u>Page</u>
4-8	Pulse Shaper Board Mnemonics	4-22
4-9	Phase Demodulator Board Mnemonics	4-22
4-10	Data Decoder Board Mnemonics	4-23
4-11	Cylinder Address Bit Assignment	4-24
4-12	Difference Address Bit Assignments	4-24
4-13	Head and Direction Bit Assignments	4-25
4-14	Control Tag Bit Assignments	4-25
A-1	I/O Adapter Card Locations	A-2

## SECTION 1 INTRODUCTION

### 1.1 GENERAL

This manual describes the operation, programming and maintenance of the model 1343 disk controller. Section 1 provides introductory material intended to familiarize users with a disk storage system. Disk storage units, disk formats and the disk storage unit controller are discussed in this section.

Sections 2 and 3 of this manual present detailed programming requirements, techniques and examples for the controller used with a GA 18/30 or SPC-16 computer. The programming sections will enable the user to thoroughly understand and use the disk storage system. Section 4 is designed to aid the maintenance technician in understanding the functional operation of the controller.

The model 1343 disk controller consists of interface logic housed on five printed circuit cards. The controller is the electronic interface between the processor and the disk storage unit. This interface performs data and control functions between the GA 18/30 or SPC-16 computers and up to four 1343 disk storage units.

A disk storage unit is generally the largest random-access storage device in a computer system; usually a single disk is capable of holding more bits than all of core. It also provides the fastest storage outside of core. The disk is constantly in motion and has a predetermined format with data blocks of fixed length. Individual data blocks are addressable, and the average random-access time is half a revolution. The model 1343 disk runs at 2400 rpm, giving an average access time of 35 milliseconds. Each disk pack can store 10,240,000 16-bit word and transfers one 16-bit word every 8 microseconds.

A model 1343 disk system consists of a disk controller and up to four 1343 disk storage units. Each disk storage unit is a separate unit. The program communicates with the controller, which in turn controls all model 1343 disk storage units connected to it, but communicates with only one at a time. The control is connected to a data channel, so the program need only set up the disk system for reading or writing, and all transfers to and from memory are handled automatically.

The disk controller responds to a command with the proper address and function decoded in the I/O system. The controller generates requests for data via the data channel, accepts data from the processor, one word at a time, via a data bus and sends the word, in a bit serial fashion, to the selected disk storage unit. Data read from the disk storage unit is accepted by the controller, a bit at a time, and a 16-bit word is assembled in the controller and sent to the processor.

The status of the controller and the selected disk storage unit is transferred to the processor using the Sense Device command or the Sense Interrupt Level commands. Data to be written on the disk is contained in the processor memory. The program initiates a write function, i.e., a core to disk transfer, by executing an Initiate Write command which specifies the address of the data table to be written. Writing continues until the processor indicates the end of the data block. A read function, i.e., a disk to core transfer, is initiated by executing an Initiate Read command. The first word of the data table contains the number of words to be transferred. Table 1-1 presents the 1343 disk controller specifications.





Table 1-1. Model 1343 Disk Controller Specifications

Characteristic	Specification
General	The controller controls data transfer and control functions between the processor and disk drives.
Organization	The controller contains the input and output data registers and timing circuitry for initiation of command functions for control of data transmission between the controller and disk drive.
Commands	The command set is comprised of control, initiate read, initiate write, sense device and sense interrupt level.
Data Word	A word of data consists of 16 bits.
Word Rate	Rate is one 16-bit word every 8 microseconds.
Transfer Rate	2.5 million bits per second.
Area Code	4
Priority Interrupt Level	Level 2
Environment	Operating environment is 0 to 50°C (+32 to 122°F), 10 to 90% relative humidity without condensation (controller only).
Installation	The controller boards installed are located in slots 12, 13, 14, 15, 16, 17, 18 and 19 of the adapter chassis. Appendix A presents detailed installation information.
Maximum number of disk drives per controller	4



## 1.2 MODEL 1343 DISK STORAGE UNIT

The model 1343 disk drive is a movable head, random access rotating memory device which utilizes a standard eleven high, removable disk pack as the storage medium. The disk pack contains 20 surfaces of 203 tracks each that are used for data storage. The vertical alignment of tracks forms 203 cylinders of 20 tracks each. A single read/write head serves each storage surface and is attached to a linear positioner which can move to any of the 203 cylinder positions selected by the controller. The disk drive accepts control signals and activates the internal subsystems necessary to position the read/write heads, select the disk surface to be accessed, and read or write data.

Basic Operation: The disk drive performs three basic operations: first seek, program seek, and data transfer. The first seek operation is a function of the power on sequence and causes the heads to be positioned at the reference cylinder position 000.

Signals from the controller to the disk drive are carried on an eight line timeshared data bus which is interpreted by control tag signals. The data on the bus can represent a command, cylinder address, head address and direction head is to be moved, or the difference count between the present and next cylinder positions.

The program seek is begun by the controller which transfers the new cylinder address, and head address to the disk drive which stores them in the appropriate registers. The disk drive reads the contents of the cylinder address register and computes the number of positions the heads are to be moved (difference count) and the direction. The controller then sends a seek start signal to the drive which develops control functions for the positioning system. The difference counter provides an input to the positioning system that is proportional to the distance the heads must travel to the new position. As the head carriage moves, each cylinder position crossing is detected and the difference counter is decremented. When the heads reach the selected cylinder, the difference counter will be decremented to zero, which will cause drive voltage to be removed from the positioning system, the servo system locks the carriage in position, and the controller is then notified that the seek has been completed.

The controller synchronizes with sector/index pulses generated from the disk pack and activates the data read or write gates. Data to be stored is sent to the disk in double frequency format which has been produced in the controller. Data read from the disk is amplified, shaped and sent to the controller data discriminator which frames the bits and assembles them into bytes for storage. Sequential read or writes may be performed on all 20 heads by issuing a head advance signal. When the head 20 is reached, an end of cylinder signal will be presented to the status lines.

The disk drive sends status signals to the controller which indicates major events during the operation such as seek complete, seek error, drive unsafe for operation, drive on-line etc.

Power-On Sequence and First Seek: The power-on and first seek operations prepare the drive for on-line operation with the controller by energizing the disk drive motor, ensuring the disk rotation is up to speed, positioning the heads at cylinder 000, and initializing the control logic.

The main power switch for each drive is left in the on position which places the responsibility of on/off sequencing control upon the controller. One or more drives may be connected to the same controller with discrete addressing for unit selection.

### 1.2.1 RECALIBRATE (RESTORE)

The controller may issue a Recalibrate command any time after the power-on sequence has been completed. Recalibrate performs the same function as First Seek - it causes the disk drive to position the read/write heads at cylinder 000. The most common reason for doing a Recalibrate is that incorrect data records have been read from the disk indicating a possible positioning error. The controller can then issue a Recalibrate and enter a data recovery routine to position the heads to the correct cylinder.

### 1.2.2 PROGRAM SEEK

The controller initiates a seek operation whenever the computer program wants to move the read/write heads to another cylinder position. When the heads are positioned, any of the 20 tracks within that cylinder can be accessed by selecting the appropriate head. Major events during a seek operation are:

- a. Controller selects a disk drive for access.
- b. The selected drive returns a unit selected signal and the controller reads the present cylinder position from the cylinder address register.
- c. The controller computes the difference between present and new cylinder addresses.
- d. The controller transfers the new cylinder address into the disk drive cylinder address register.
- e. The controller transfers the head address (disk surface) into the disk drive head address register and sends the positioner direction bit.
- f. The controller transfers the computed difference count into the disk drive difference counter.
- g. The servo drive system is activated by the seek start signal and the head carriage is moved to the selected cylinder position under control to the difference counter.
- h. The counter is decremented as each cylinder position is crossed and when the counter content is zero the carriage is locked in position.
- i. When the seek is completed, the seek ready and gated attention status signals are sent to the controller.

### 1.2.3 READ/WRITE

A data transfer operation is initiated when the controller verifies that the read/write heads are located at the selected cylinder position. The disk surface to be accessed is determined by the contents of the head address register which was loaded during the seek operation. The controller synchronizes the data transfer timing logic with the index pulse (or sector pulse) generated from the disk pack. The controller then locates the data field to the accessed and sends the appropriate read or write/erase signals to the disk.

Recording Data: The controller clock generator is used to produce Clock Pulses every 400 nanoseconds (2.5 mHz) which defines data bit cell time. A series of Data Pulses are also generated which are 180° out-of-phase with the Clock Pulses. The Clock Pulses are combined with the Data Pulses to form the bit-serial, double-frequency data stream to the disk. When data is to be recorded, the controller reads it out of main system storage (core memory) and converts it to bit-serial pulses. When a data zero is to be recorded, no flux change occurs during the data cell time. A data one change the data cell flux direction 200 nanoseconds after the Clock Pulse and a double-frequency signal is recorded.



The Write Gate signal from the controller activates the write driver circuits and the input data is recorded by the selected head. An erase head is turned on by Erase Gate which erases the edge of the track to provide optimum playback and maximum separation of adjacent tracks.

Reading: Data read from the disk is amplified, shaped, peak detected, and sent to the controller in the double-frequency format. The RDATA pulse train is clocked into the controller data discriminator for conversion to data zeroes and ones. The data bits must be stored in a data buffer until a storage unit (byte or word) of data has been assembled. The controller then sends the data to the system memory and prepares to receive more data.

Disk Pack: The model 1343 disk drive uses a standard eleven-high disk pack as the storage medium. The pack has eleven 14 inch diameter disks mounted 0.350 inch apart on a single hub with an additional protective disk at each end. The bottom protective disk is made of aluminum and is the Sector/Index Disk.

It has 32 equally spaced Sector Marks machined into the outer edge and an additional slot next to one of the Sector Marks which defines the Index Mark. Data storage is limited to 20 surfaces of the pack: the bottom of the top disk, both surfaces of the inner nine disks, and the upper surface of the bottom disk. The storage surfaces and corresponding heads are numbered 0 through 19 starting with the upper disk. The pack is attached to the disk drive spindle by a threaded shaft located in the pack hub. When the pack is placed on the spindle, the shaft is screwed into the spindle by rotating the handle on the pack in a clockwise direction. The spindle is locked to prevent rotation while loading or unloading a disk pack.

Disk Pack Drive Spindle and Motor: The drive spindle is mounted on the upper deck plate surface and is driven by the spindle drive motor. The motor and spindle are coupled by a pulley and belt system designed to provide a disk pack rotational speed of 2400 rpm. The drive motor is powered by 208 vac supplied through the motor power relay on the power distribution panel. The motor has two speeds with automatic changeover; it provides high starting torque at low speed and as it accelerates, an internal centrifugal switch changes the motor windings to the high speed configuration. The high speed is reduced to 2400 rpm by different diameter pulleys on the motor and spindle. The disk pack normally reaches full speed in about ten seconds.

The loading and removal of disk packs is facilitated by the spindle lock which prevents spindle rotation when the pack access lid is open. A mechanical linkage activated by the open lid pushes the spindle locking arm into a detent in the spindle collar under the deck plate and holds the spindle in place. The pack mounting shaft can then be tightened or loosened.

When a disk pack is mounted, the spindle shaft is drawn up and the pack switch interlock is closed. The switch is located under the deck plate at the end of the spindle shaft. The interlock is used to disable the power-on sequence when no disk pack is mounted.

#### 1.2.4 LINEAR POSITIONER

The linear positioner is a servo driven voice coil motor which moves the read/write heads to a cylinder position selected by the controller. The motor consists of a permanent magnet stator and a voice coil armature (bobbin) which is attached to the head carriage. Positioning current produced by the servo amplifier is driven through the voice coil to generate a magnetic field which is dependent on the amplitude and polarity of drive current. The voice coil field reacts with the stator field to move the head carriage along the carriage way on rollers. When the selected cylinder position is reached, the motion is stopped and the carriage is locked electrically in position with an accuracy of 300 microinches or less.

Two motion transducers are included in the positioner to detect cylinder positions (cylinder transducer and index rack) and carriage velocity (tachometer). The cylinder transducer output is used to decrement the difference counter which determines the distance the carriage moves. A tachometer provides feedback to the servo amplifier to limit the maximum velocity of the carriage.

#### 1.2.5 READ/WRITE HEADS

The model 1343 disk drive utilizes 20 heads to record and read data on the disk pack storage surfaces. Each head is attached to the positioner head carriage by a spring-loaded mounting plate which is long enough to extend the head to the innermost cylinder position. The head actually consists of two heads, the read/write and a straddle erase head, mounted on a single large pad. The recorded track is straddle erased to provide optimum playback for a given write current and to provide adequate track separation. Write current and erase current are controlled by separate logic functions to provide the proper timing relationship.

The head pad rides (or flies) on a thin layer of air that adheres to the disk surface as it rotates. A very high pressure air layer is formed under the head pad which subsequently tries to lift away from the disk surface. The spring tension of the head mount counteracts the air pressure and holds the head in the airstream. The head is designed to fly above the disk surface at a constant altitude. One edge of each head mount contains a camming surface which controls the loading and unloading of the head. When the head carriage is retracted, the spring arm is lifted by a tower-mounted stationary cam, which causes the head to be raised from the disk (unloaded). As the head carriage is moved forward during a First Seek operation, the spring arm is allowed to move toward the disk surface and the head pad is lowered into the disk airstream. The spring arm is then completely free of the cam and the head starts flying (loaded).

Air System: Air for cooling and pack chamber pressurization is supplied by the blower assembly located in the bottom of the cabinet. Intake air passes through a fiberglass filter into a vertical duct. The air is then passed through an extremely fine filter which removes any remaining particles of dirt. The pack shroud forms a positive pressure chamber when sealed by the access lid. Input air flows through this filter into the disk area at the spindle opening. The positive pressure environment helps prevent small foreign particles from entering the pack area to cause head crashes or pack damage. An outlet directly over the logic chassis allows air to flow down through the modules, power supply, and out through the exhaust louvers in the bottom of the rear panel.



Air is also forced up into the disk pack hub through a filter on the bottom of the pack. Outlets in the hub provide a clean air source to maintain the air bearing on the storage surfaces. Should the filter system become clogged, a resultant air starvation condition will result which could cause the heads to fly incorrectly. This condition is monitored by an air flow detection device and results in a select lock or error condition disallowing activation of the system.

During the power-up sequence, the servo control circuits are initialized to perform the initial seek operation that positions the read/write heads at cylinder 000. During the power-down sequence, the sequencing circuits provide signals to the servo control circuits that result in the retraction of the head carriage mechanism.

Power-Up Sequence: During normal operation, AC on power switch S1, on the power distribution panel, is left in the ON position. When the controller provides ac operating power to the disk drive, the power-up sequence occurs automatically or semiautomatically, according to the following conditions:

- a. If the POWER ON pushbutton indicator switch is on, a disk pack is installed, and the disk access door is closed, the sequence proceeds automatically.
- b. If the operator first installs the disk pack, closes the disk access door, then presses the POWER ON pushbutton, the sequence proceeds in a semiautomatic manner because circuit operation depends upon the closing of switches involved with these operations.

In this discussion, it is assumed that the operator-type functions given above are performed only when necessary to progress in the power-up sequence; the discussion is based on this semiautomatic operation because various control functions are better explained in this manner. The sequence of events is as follows:

- a. The controller provides 3-phase, 208/230 vac, 50 or 60 Hz power in parallel to all devices in the device chain. Single-phase, 208/230 vac power is applied directly to the dc power supply through prime power switch S1. With the power supply energized, the control logic is initialized.
- b. The controller provides a control ground (CON GRD) signal in parallel to all devices, thereby grounding the K1 relay coil.

#### NOTE

The controlled ground signal is delayed 15 seconds by the controller to allow dc power to stabilize.

### 1.3 DISK FORMATS

A typical disk consists of a round, platter-like, metal disk coated with a thin layer of ferromagnetic material. Each disk has 203<sub>10</sub> twenty-track cylinders as shown in figure 1-1.

Every track is divided into 8 sectors, each of which contains 322 words of data. The disk track representations are shown in figure 1-2.

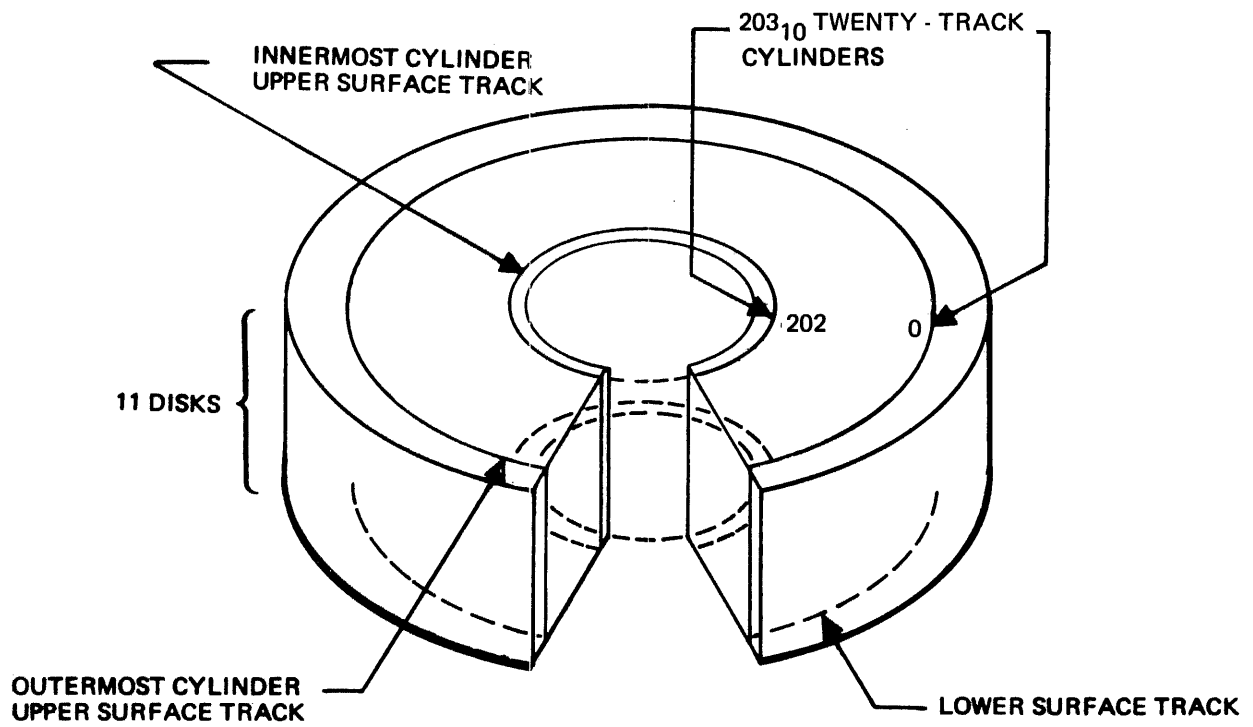
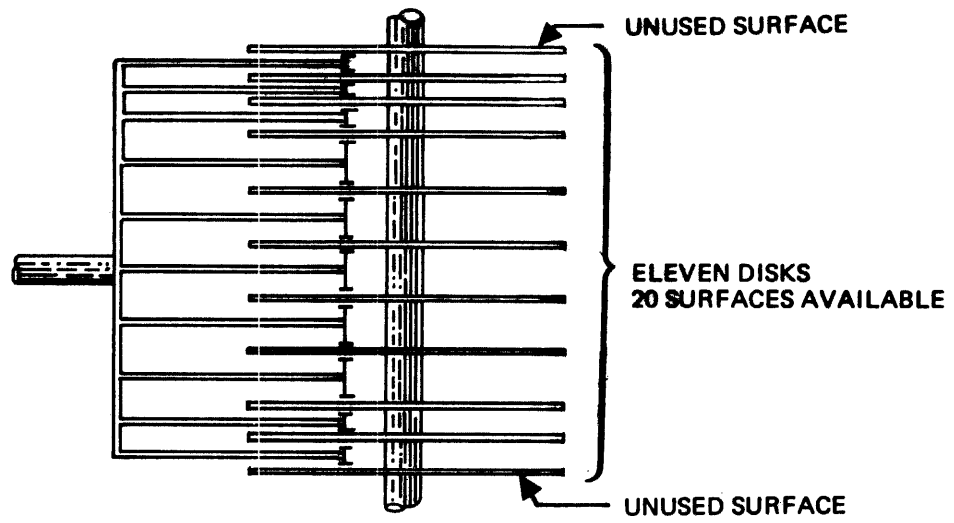


Figure 1-1. Disk Characteristics

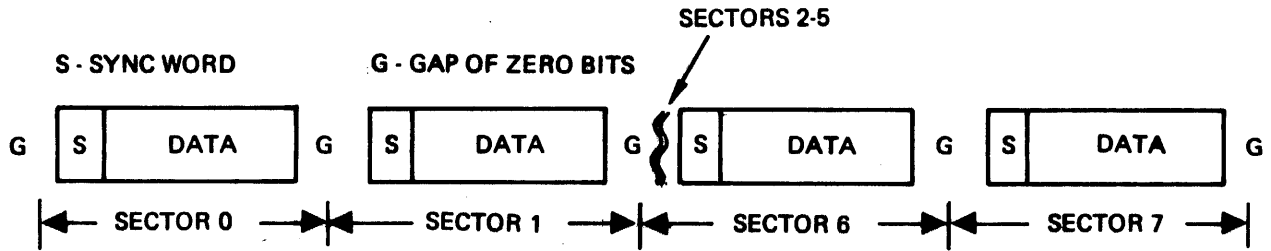


Figure 1-2. Disk Track Representation

The eight disk sectors are presented in figure 1-3. One sector is redrawn to better show the track-to-sector characteristic. During a write operation, normally 321 or less data words are written, but the controller continues to write all zero words until 322 total words are written. The write operation always terminates and interrupts after 322 words are written.

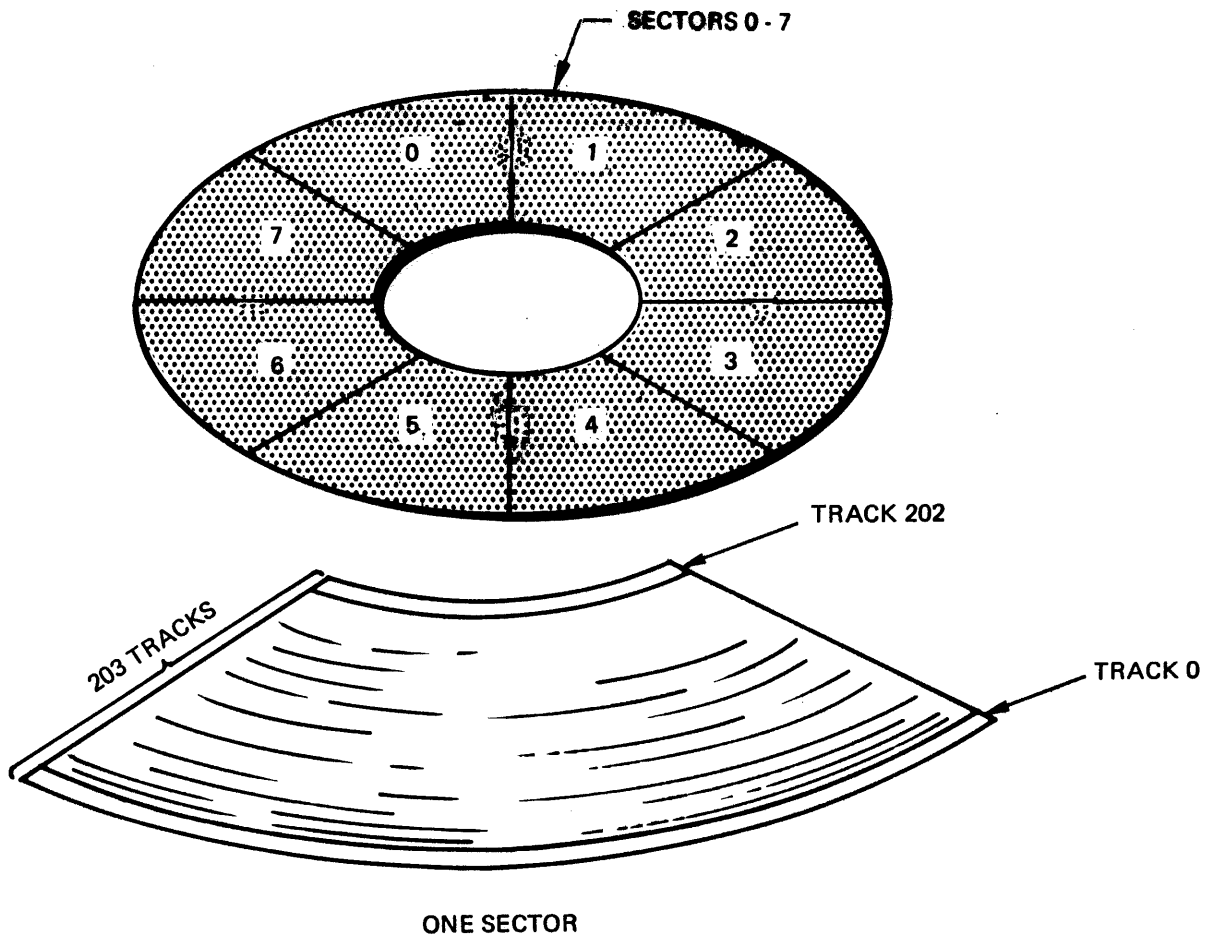
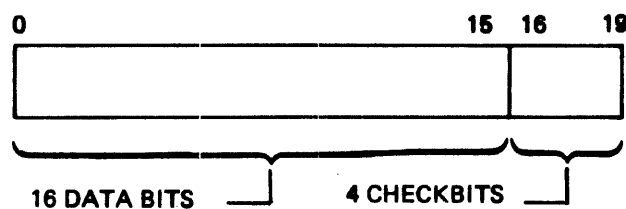


Figure 1-3. Disk Sector Configuration



The sync (15 zeroes, 4 ones, 1 zero) word and data (321 data words) are preceded and followed by gaps or series of zero data words to provide time for the processor to access (read or write) consecutive data sectors and to allow for write transients and mode and a head switching. The minimal time from the end of data in one sector to the beginning of the next sector (i.e., programming time between sectors) is 297 microseconds.

A single word of data and associated check bits is shown below.



The check bits are calculated to make the total number of one bits in the twenty-bit word an integral multiple of four (equal to zero modulo four). Table 1-1 shows the check bit pattern for all possible data patterns using MOD 4 checking.

#### 1.4 MODEL 1343 DISK CONTROLLER

The GA 1343 disk storage unit controller contains control and sequencing logic which accepts and decodes a device address from the central processor and produces all necessary signals to control disk storage unit operation and the transfer of data. The controller also responds to disk storage unit indicators completing the interface function.

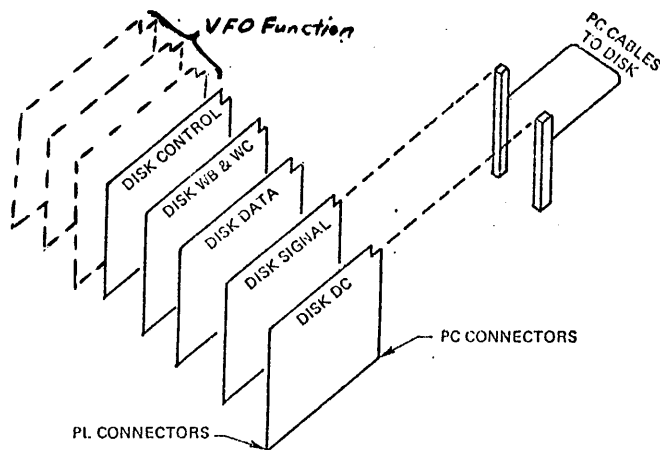
The electronic circuits required to perform controller functions are mounted on glass-epoxy, etched circuit boards. Five basic boards are required in each controller. They are the control board, data buffer and word control board, data board, signal board, and disk DC board.

Table 1-2 MOD 4 Check Bit Pattern

Number of one bits written in the data bits 0 - 15	0	1	2	3
	4	5	6	7
	8	9	10	11
	12	13	14	15
	16			
Check Bits Required				
16	0	1	1	1
17	0	1	1	0
18	0	1	0	0
19	0	0	0	0

### 1.4.1 INSTALLATION AND CABLING

Controllers are housed in the I/O enclosure. The backplane connectors of the I/O enclosure are connected to the PL connectors of the controller boards. The PC connectors of the boards are interconnected in various configurations with PC cabling. Controller/computer interface and controller/device interface is accomplished via the I/O cables. Figure 1-4 shows the basic board configuration for the model 1343 disk controller system. In addition there is a Variable Frequency Oscillator (VFO) function which must be included. Presently, this function is housed either on 3 piggy-back Century Data System boards or 1 GA designed VFO board.



VFO Function	
Century Data Piggy-Back Boards	GA Designed Board
Pulse Shaper Phase Demodulator Data Decoder	VFO Board

Figure 1-4. Model 1343 Disk Controller Boards

#### NOTE

This manual describes the 3 Century Data piggy-back boards and includes timing and adjustment procedures. The timing and adjustment procedure for the single GA designed VFO board is included on logic diagram 90C015667A.

### 1.4.2 SYSTEM CONFIGURATION

As shown in figure 1-5, the controller/device interface cable is connected to a disconnect panel which in turn interfaces with the device. The disconnect panel functions primarily as a distribution system which allows a device to be taken off or put on line without disturbing the system. The disconnect panel is connected by drive interconnect cables. A disconnect panel terminator is provided for the 1343 controller.

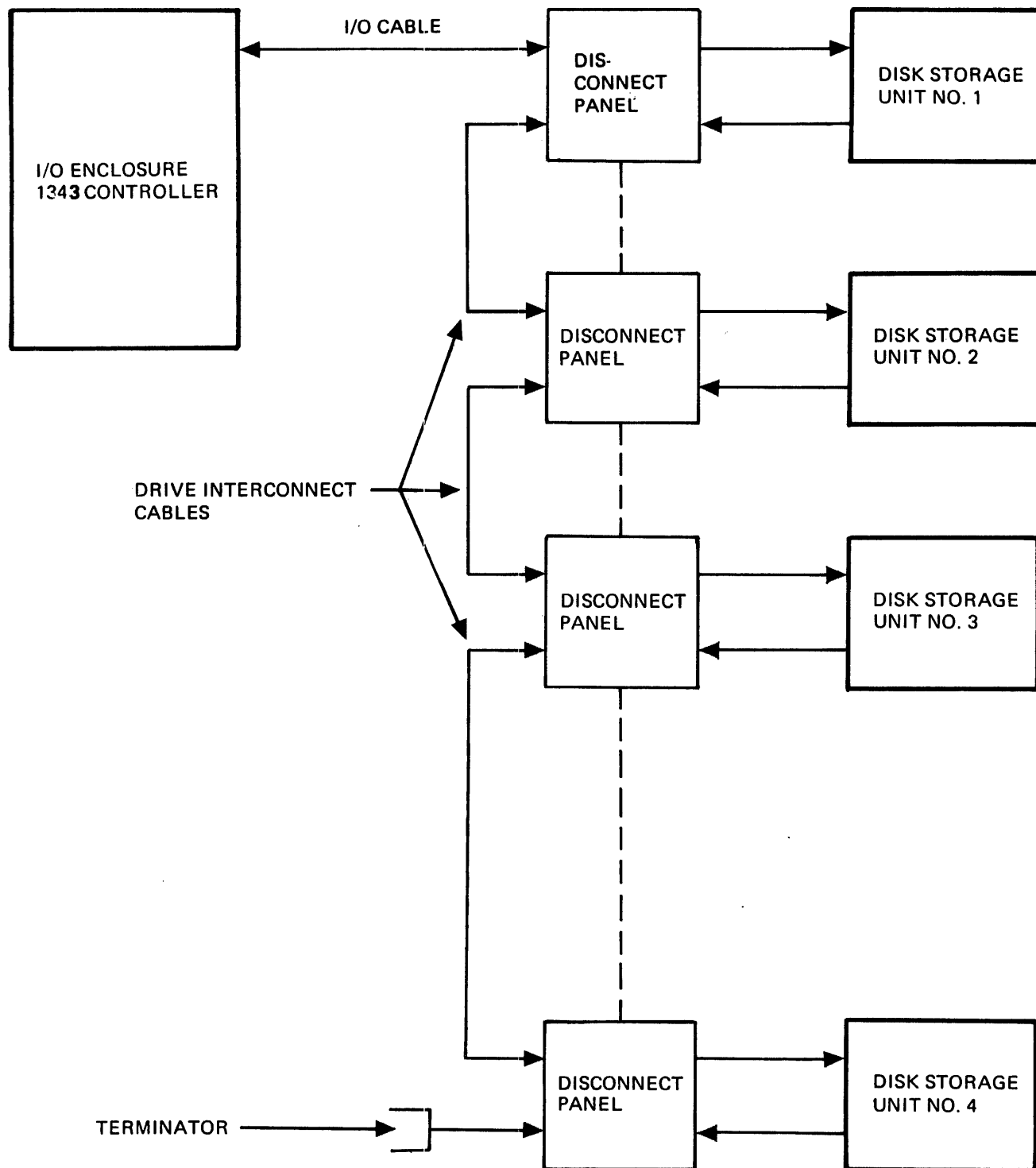


Figure 1-5. System Configuration



## SECTION 2 CONTROLLER PROGRAMMING FOR 18/30 SYSTEM

### 2.1 GENERAL

This section provides command timing, status bits, area code and interrupt information and a sample program and flowchart for the disk controller. Refer to section 3 of this manual for SPC-16 programming information. This information will aid the user in determining programming requirements. Refer to section 4 of this manual for information pertaining to functional operations of the controller.

### 2.2 COMMAND AND TIMING

An XIO instruction initiates all input and output operations by fetching a double word I/O control command (IOCC) from processor memory as specified by the effective address of the XIO instruction. The IOCC double word specifies the operation and all parameters defining the operation to be performed.

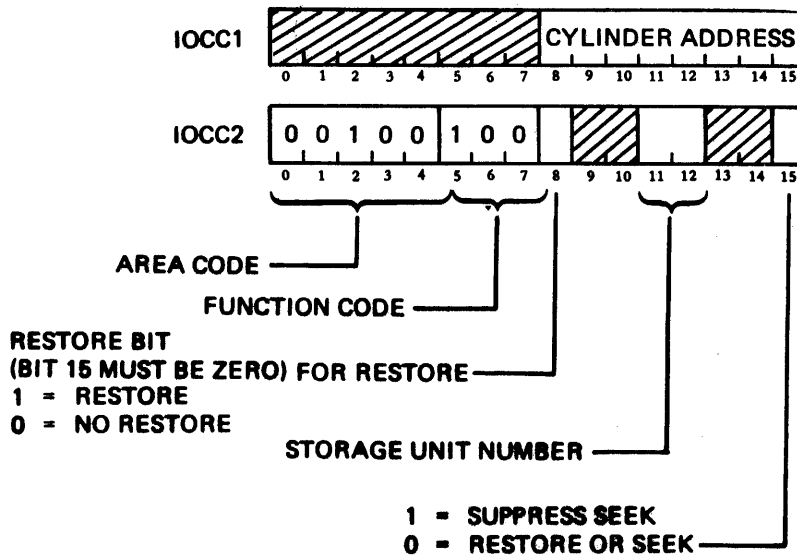
The XIO instruction generates a function address (FAP+) pulse that indicates the IOCC2 word is on the OUT bus. The area code, function code and modifier bits are contained in the IOCC2 word. The area code specifies the I/O device or I/O group affected by the operation and the function code specifies the operation to be performed. The modifier bits identify the head and sector within an area code or unit and seek option.

The relative timing of all the I/O signals that occur during an XIO instruction are shown in the 18/30 I/O design reference manual number 88A00122A. The disk controller accepts five commands from the processor:

- Control
- Sense Device
- Sense Interrupt Level
- Initiate Read
- Initiate Write

The function codes for these commands are specified in bits 5, 6 and 7 of the IOCC2 word.

#### 2.2.1 CONTROL



The control command is used to select a unit in order to test status or perform a read or write operation if multiple seeks are executed prior to these operations. Three operations may be performed with this command depending on the state of bits 8 and 15 as shown in the table 2-1. Bits 8 through 15 of the IOCC1 specify the cylinder address in binary. Valid addresses are 0 through 202.

Bits 0 through 4 of the IOCC2 specify the standard area code (00100) to which the controller will respond. Bits 5 through 7 of the IOCC2 specify the function (100 for this command). Bit 8 specifies a restore operation is to be performed if bit 15 is a zero. Bits 11 and 12 specify the disk storage unit.

Table 2-1. Control Command Operations and Disk Number Decode

	Bits			Storage Unit (up to four)		
	8	15			11	12
Seek to cylinder number specified in IOCC1.	0	0		0	0	0
				1	0	1
				2	1	0
				3	1	1
	0	1	No seek, select storage unit specified in bits 11,12.			
Perform a restore operation in storage unit specified in bits 11, 12.	1	0				
	1	1	Illegal, no operation is performed.			

This command has both an on-line and off-line execution period. A portion of the execution occurs while the cylinder address is transferred to the storage unit. During this period, the controller is in a busy status condition. Then the seek operation occurs while the storage unit is off line. The controller is now able to accept other commands.

Control Command Execution - On Line. When this command is received by the controller, assuming that the controller or storage unit is not busy executing a previous command a sequence of operations is performed. The difference address [(calculated by the controller (cylinder address in bits 8 - 15 of IOCC1) - (current arm position)] and direction of travel are transferred to the disk storage unit specified by bits 11 and 12 of IOCC2. During this period, the controller returns to a busy status condition. If the controller is busy when this command is received, the command is ignored. When the start seek signal is transferred to the storage unit, assuming that the storage unit is not busy with a previous seek operation and that no status conditions exist which otherwise prevent the operation, the storage unit commences a seek operation to the cylinder address specified. Assuming that no previous status conditions exist, the possible status conditions

when a sense device command is issued subsequent to a Control command are described in paragraph 2.2.3. A seek error occurs when the seek cylinder is larger than 202 or a seek is given to a busy unit (busy seeking).

After a Control command has been issued and a seek operation is initiated in a storage unit, the controller can accept other commands for the same storage unit or for other storage units. In either case, the storage unit selected must be capable of accepting the command or the command will be rejected. The command will not cause the desired operation to occur but will force a status condition to occur in the selected storage unit. For instance, if a control command is attempted with a storage unit which is currently performing a seek operation, the seek-error status condition occurs in the storage unit and the second seek is not performed.

Control Command Execution - Off Line. After the start seek signal is transferred to the storage unit the seek operation is started by the storage unit and occurs whether or not that unit remains selected by the controller. Upon completion of the off line seek operation, the storage unit reflects an access-ready status condition to the controller which then causes a priority level interrupt to the processing system. Execution of a seek operation in which the cylinder address specified is the same as the storage unit's current cylinder address will cause the priority level interrupt, even though no positioning movement occurs. The I/O signals associated with the Control command are shown in figure 2-1.

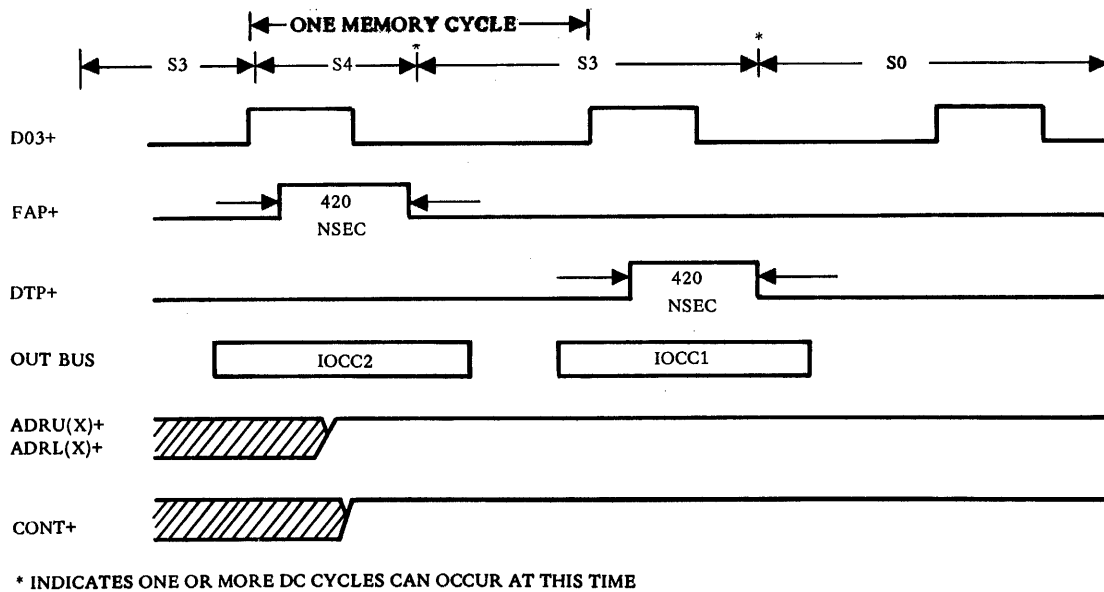
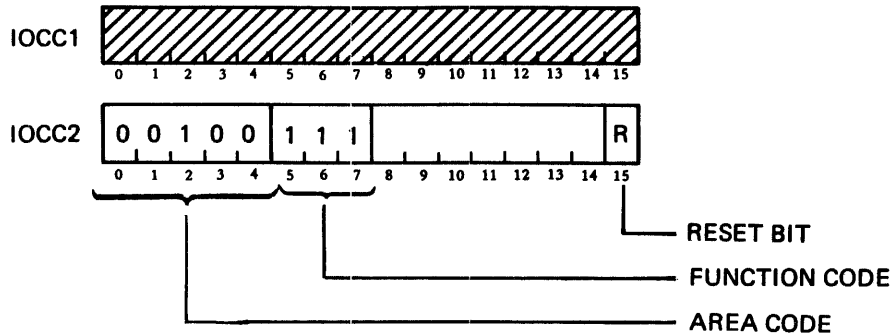


Figure 2-1. Control Command Timing (Applies to 1804 Processor)

2.2.2 SENSE DEVICE



Sense Device Command Execution. When this command is received by the controller, the status of the controller and the currently selected storage unit are transferred to the processing system. This command is always accepted by the controller whether or not it is busy with a previous command and the status conditions are indicated as they currently exist in the equipment. The returned status will be from the currently selected storage unit. Bit 15 is a reset bit and causes certain status conditions to be reset if it is a ONE. The Sense Device command timing is presented in figure 2-2.

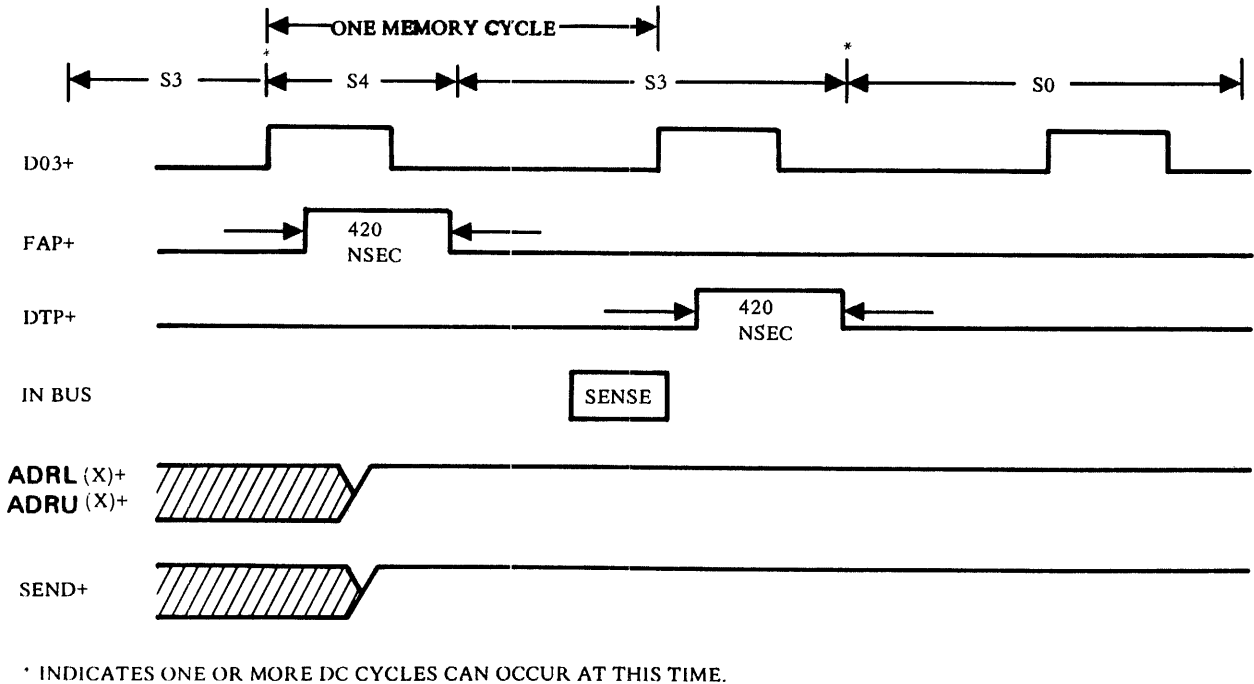


Figure 2-2. Sense Device Command Timing (Applies to 1804 Processor)

The single word transferred to the processor when this command is issued is called the device status word (DSW). The status word (DSW) of the controller and currently selected storage unit is read into the processor accumulator when the Sense Device command is decoded. The bits shown in figure 2-3 with annotation are used to indicate status. The remaining bits are set as indicated. The significance and meaning of the status bits are further described in the following paragraphs.

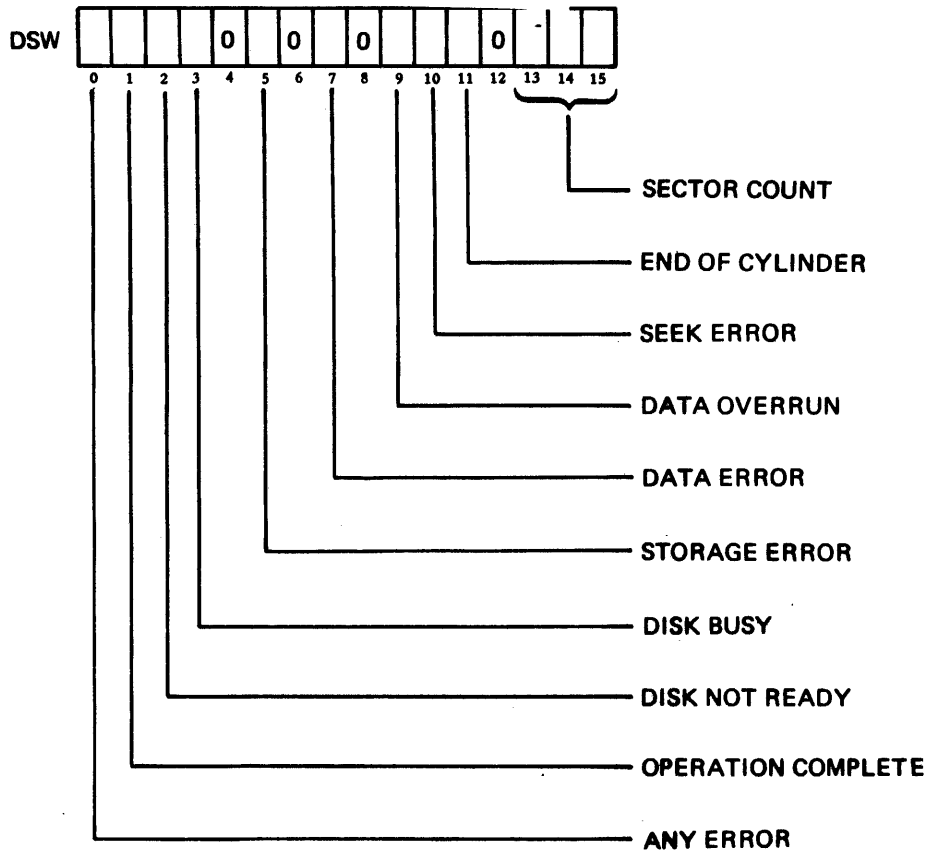


Figure 2-3. Disk Controller Device Status Word

Bit 0 - Read/Write Operation Complete. This bit is set to one at the completion of an operation specified by an Initiate Read (SCW bit 0 equals 0 or 1) or Initiate Write instruction. This happens whether the completion occurs because the specified number of words have been transferred or the end of sector is detected before the specified number of words are transferred. This bit is reset by the Sense Device instruction when IOCC2 bit 15 equals 1.

Bit 1 through 4 - Seek Complete Units 0 through 3. These bits, a unique one for each unit, are set at the completion of an operation specified by a Control (Seek) instruction, whether successful completion or seek error termination occurs. Each bit is reset by a Sense Device instruction when IOCC2 bit 15 equals 1.





Interrupts: All interrupts from this subsystem occur on interrupt level two. Two conditions within the subsystem cause interrupts. The read/write operation interrupt occurs at the completion of a read or write operation, either because the specified number of words have been transferred or the end of sector is detected before the specified number of words have been transferred. The seek complete interrupt occurs at the completion of a seek operation, either because of successful completion or seek error termination.

In a subsystem containing multiple storage unit, concurrent operation of all units is possible. The interrupts at the completions of these operations are not stacked, and only a single interrupt occurs if, for example, one or more seek operations and a read or write operation are completed at the same time or while the interrupt is active. However, the current status is indicated and will remain in the Interrupt Level Status Word (ILSW) until reset by a Sense Device instruction.

The basic disk storage unit status conditions and those associated with the Initiate Read and Initiate Write commands as well as the control for seeks are presented in the following paragraphs.

Bit 0 - Any Error: This bit is set to one if any of bits 5, 7, 9 or 10 are set to one, and is reset when all of the individual indicators are reset.

Bit 1 - Operation Complete: An Initiate Read operation completes when the specified number of words are transferred or an end of sector is detected. An Initiate Write operation completes when the specified number of words are written and the remainder of the sector (if any) plus one additional word is written as an all zeros field.

This bit is the inclusive OR of the operation complete status of up to four storage units and is set to a ONE upon completion of an Initiate Read (SCW bit zero is a ZERO or ONE) or an Initiate Write operation.

Bit 1 of the DSW is set if any of the conditions listed below are present after an Initiate Write or Initiate Read operation:

1. Specified number of words have been transferred.
2. End of sector has been detected before the specified number of words have been transferred.
3. Completion of a seek operation either because of successful completion or seek error termination.

Operation complete is the only condition which causes an interrupt. This bit is reset by the Sense Device instruction when IOCC2 bit 15 is a ONE.

Bit 2 - Disk Not Ready: This bit is set to ONE when the storage unit is not properly sequenced up, or an unsafe condition exists in the storage unit, or the storage unit is busy performing a seek, read or write operation.

Bit 3 - Disk Busy: This bit is set to ONE during the time the storage unit is performing a seek, read or write operation.

Bit 5 - Storage Error: This bit is the logical OR of the storage protect error and the parity check error conditions. Its meaning depends upon which command, Initiate Read (SCW bit zero is a ZERO) or Initiate Write is executed. The storage protect error (Initiate Read) bit is set to ONE if an attempt is made to write data from disk into a protected area of core memory. The parity check error (Initiate Write) bit is set to ONE if the processing system detects a core memory parity error during a disk subsystem access.

This bit is reset by the Sense Device instruction with IOCC2 bit 15 set to ONE.

Bit 7 - Data Error: This bit is set to ONE if a MOD 4 data check error is detected during the execution of an Initiate Read (SCW bit zero is a ZERO or ONE) operation, or if the end of sector is detected before the specified number of words have been transferred during an Initiate Read (SCW bit zero is a ONE). Also may occur if a word count larger than 321 is specified. Data error because of a end of sector or no block complete signal also sets the operation complete status and causes a read/write operation complete interrupt. This bit is reset by the Sense Device instruction with IOCC2 bit 15 set to ONE.

Bit 9 - Data Overrun (Access Error): This bit is set to ONE if a request to the processing system memory is not honored in time, resulting in an erroneous or incomplete record written in core or on the disk. This bit is reset by the Sense Device instruction with IOCC2 bit 15 set to ONE.

Bit 10 - Seek Error: This bit is set to ONE if a cylinder address greater than 202 is attempted, or if a seek is directed to a storage unit that is busy executing a previously specified seek, or if a seek operation has not progressed to completion within 180 milliseconds, or if the storage unit detects a condition in its access mechanism which prevents it from positioning properly. Seek error resulting from either of the first two condition causes an operation complete status and a seek complete interrupt. This bit is reset by a subsequent control command to the same storage unit.

Bit 11 - End of Cylinder: This bit is set to a ONE when the head address register in the disk storage unit is set to an address greater than 19. This bit is reset by a subsequent Initiate Read or Initiate Write command with a valid (0-19) head number specified.

Bits 13, 14, 15 - Sector Count: These bits indicate the next sector to become available for reading or writing. These bits are updated as the disk rotates, always indicating the address of the next sector to come under the heads.

#### THE INITIATE READ STATUS CONDITIONS ARE AS FOLLOWS:

Bit 9 - Data Overrun: A full word of data was read from the disk before a previously transferred word is acknowledged by the data channel.

Bit 7 - Data Error: A MOD 4 check error was detected during the reading operation or the leading edge of the following sector was detected while the controller was in the read mode. The latter condition also causes an operation complete status and a read write operation complete interrupt.

Bit 5 - Storage Error: An attempt was made to read data from disk into a protected area of core memory.

Bit 2 - Disk Not Ready: The storage unit is not properly sequenced up or some unsafe condition exists in the storage unit.

Bit 1 - Operation Complete: The read operation is complete, either because the specified number of words has been transferred or the end of sector was detected. This condition causes a read/write operation complete interrupt.

#### NOTE

Except for operation complete, the preceding status conditions could also be reflected whenever a Sense Device command is issued following the command initiation if the conditions occur. In addition, the following status condition will be reflected if the interrupt has not occurred:

Disk Busy: The Controller is busy performing the read operation.

THE INITIATE WRITE STATUS CONDITIONS ARE AS FOLLOWS:

Bit 9 - Data Overrun: A full word of data was written on the disk before another previously requested data word is received from the data channel.

Bit 7 - Data Error: The leading edge of the following sector was detected while the controller was in the write mode. This condition also causes an operation-complete status and a read/write operation-complete interrupt.

Bit 5 - Storage Error: A memory parity error was detected during a data channel operation.

Bit 2 - Disk Not Ready: The storage unit is not properly sequenced up or some unsafe condition exists in the storage unit.

Bit 1 - Operation Complete: The write operation is complete (322 words plus 16 bits are always written). This condition causes a read/write operation-complete interrupt.

#### NOTE

Except for operation complete and data error the above status conditions could also be reflected whenever a Sense Device command is issued following the command initiation if the conditions occur. In addition, the following status condition will be reflected if the interrupt has not occurred.

Disk Busy: The Controller is busy performing the Write operation.

THE CONTROL FOR SEEK STATUS CONDITIONS ARE AS FOLLOWS:

Bit 10 - Seek Error: The cylinder address transferred to the storage unit was greater than 202 or a seek operation was attempted while the storage unit was busy performing a previous seek.

This status condition will also occur if the seek operation is not completed within 180-200 milliseconds after it is initiated or if other checks within the storage unit indicate an impending failure in the actuator servo system.

Seek error resulting from either of the first two conditions causes an operation complete status and a seek complete interrupt.

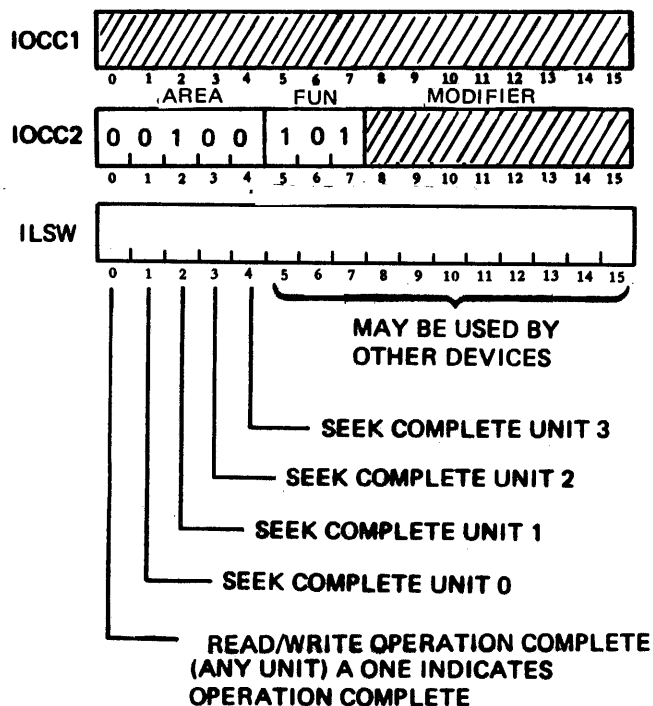
Bit 3 - Disk Busy: The storage unit is performing a seek, read or write operation.

Bit 2 - Disk Not Ready: The storage unit is not properly sequenced up or some unsafe condition exists in the storage unit, or the storage unit is busy performing the seek operation.

Bit 1 - Operation Complete: The seek operation has ceased, either because of successful completion or seek error termination. This condition causes a seek complete interrupt.

### 2.2.3. SENSE INTERRUPT LEVEL

In the interrupt identification routine as XIO Sense Interrupt Level instruction is executed to read the Interrupt Level Status Word (ILSW) into the accumulator. The IOCC for this instruction specifies only the sense interrupt level function; no other portions of the IOCC are used. Refer to figure 2-4 for the timing associated with this command. The following format is used for this IOCC:



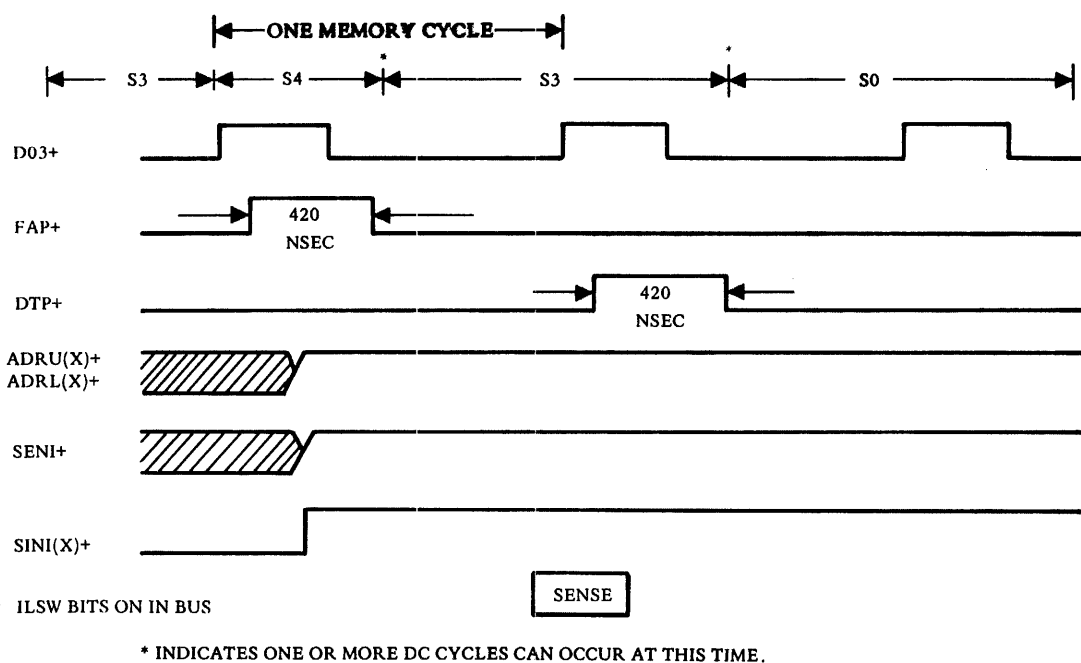


Figure 2-4. Sense Interrupt Timing (Applies to 1804 Processor)

Sense Interrupt Level Command Execution: When this command is received by the controller the interrupt status of the subsystem is transferred to the processor. The command will always be accepted by the controller whether or not it is busy with a previous command and the interrupt status is indicated as it currently exists, in the controller. The single word transferred to the processor when this command is issued is called the Interrupt Level Status Word (ILSW).

#### 2.2.4 INITIATE READ

IOCC1 is not used by the controller, however, it specifies the address of the I/O data table. Word one of the data table is called the scan control word (SCW) and contains the data table word count. A read operation terminates after the desired number of words have been transferred. A read-check operation does not use the SCW as long as it does not specify a zero word table, and always checks 322 words.

Bit zero of the SCW is the read-check bit. If bit zero is a ZERO, a normal read operation is performed and data is transferred to the processing system. If bit zero is a ONE, the operation is similar to a normal read except that data is not transferred to the processing system. The words are read from the disk and checked by the controller for correct MOD 4 check bits only.

Bits 8 - 12 of IOCC2 specify the head number and bits 13 - 15 specify the desired sector within a given cylinder. (Refer to table 2-2 and 2-3.)

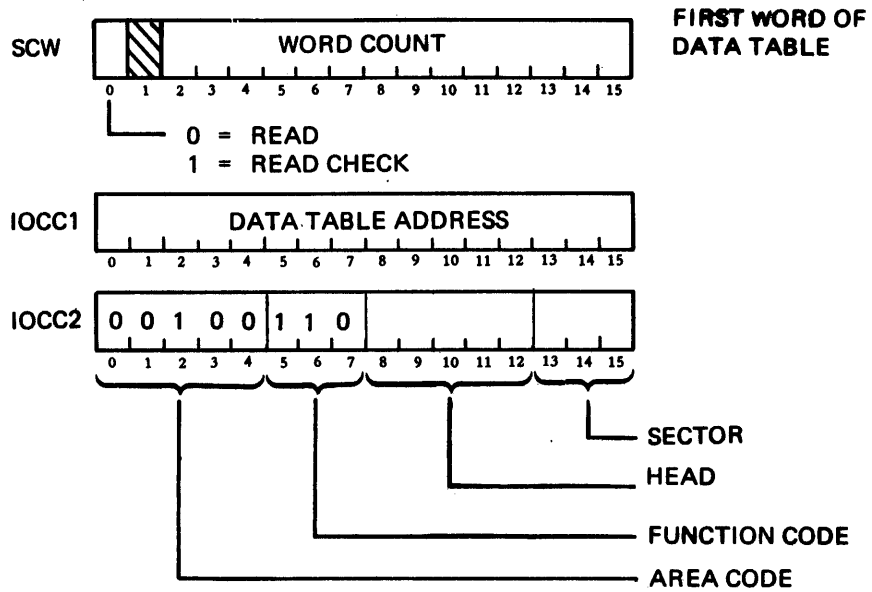


Table 2-2. Head Number Decode

Head Number	Bits				
	8	9	10	11	12
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	0	0	0	0
17	1	0	0	0	1
18	1	0	0	1	0
19	1	0	0	1	1



Table 2-3. Sector Decode

Sector Number	Bits		
	13	14	15
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

The Control command is used to select a unit if a seek to another unit could have occurred prior to the Initiate Read command.

Initiate Read Command Execution: Assume the storage unit or controller is not busy with a previous command. When this command is received by the controller it returns to a busy status condition and begins a search operation to locate the desired sector. When the sector is located the first data word is read from the disk and checked for proper MOD 4 check bits. If bit zero of the SCW is a ZERO, the controller transfers the word to the processing system via the data channel interface. Subsequent data words are checked and transferred until a block complete signal is received from the processing system, word count equal to 322 or end of sector (end of sector would be reached on an unwritten, i.e., not initialized, disk where no sync pattern could be located.)

After a block complete signal is received or 322 words are received, or the end of sector is detected, the operation complete status condition is set and a priority level interrupt is sent to the processing system. Specifying a word count of zero results in the operation complete status and interrupt, but no reading occurs.

If the command is accepted and the read operation is performed (bit zero of the SCW is a ZERO), the possible status conditions when a Sense Device command is issued after the interrupt are described in paragraph 2.2.3.

The read operation is performed by the controller at the currently positioned cylinder on the currently selected unit. Since the cylinder address is not verified by the controller, software checking of the cylinder address is required. The address can be checked by reading the first word of any sector or by reading the desired sector and verifying the address in the first word of the sector.

During a read check operation (bit zero of the SCW is a ONE), the operation proceeds as described except that no data is transferred to the processing system. The read check is always performed on all 321 words of the sector, then operation complete status is set and the processor is interrupted.

The possible status returns when a Sense Device command is issued after the interrupt are the same as when bit zero of the SCW is a ZERO except that the data-overflow and storage-error conditions can not occur.

The read operation (bit zero is a ZERO) normally terminates and interrupts after the last data word of the sector (or earlier). If the controller or storage unit is busy with a previous operation, the command is ignored (not recognized by the controller).

The timing associated with the Initiate Read command is shown in figure 2-5.

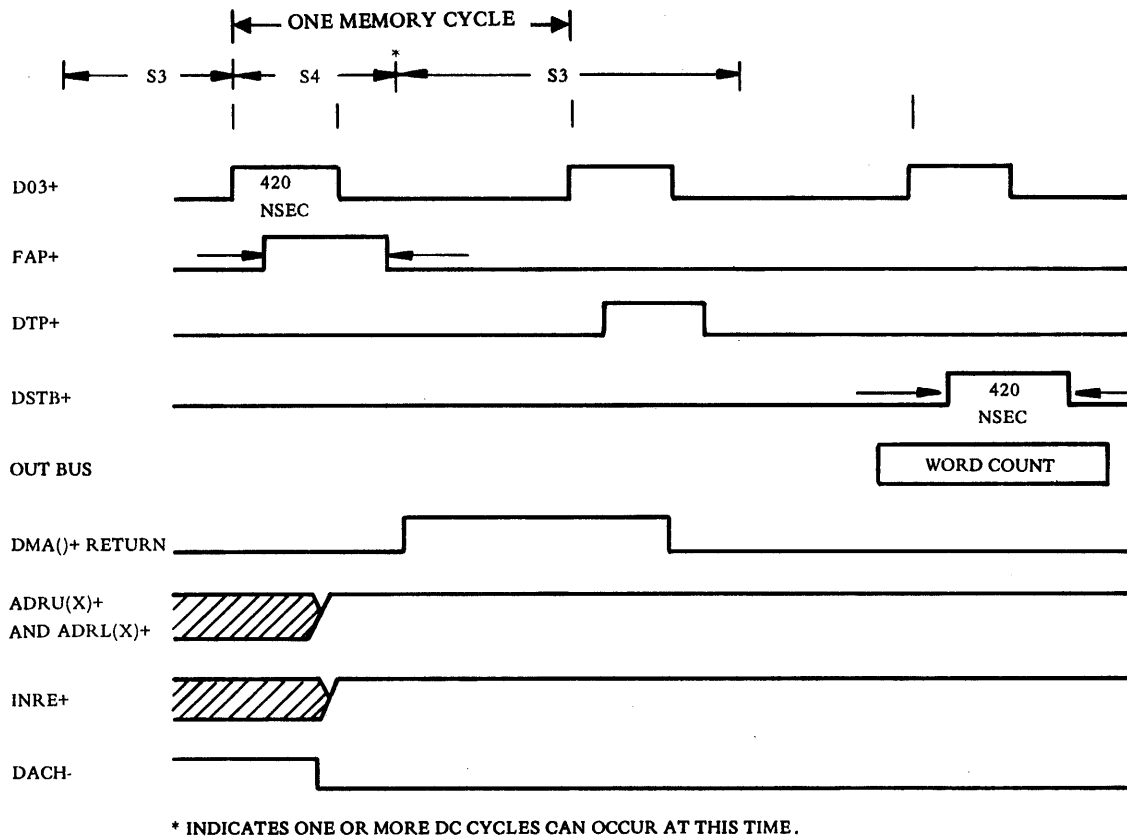
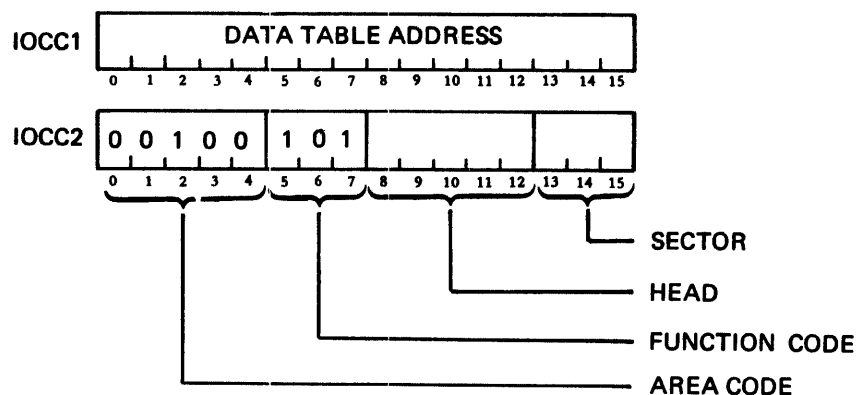


Figure 2-5. Initiate Read Timing (Applies Only to 1804 Processor)



## 2.2.5 INITIATE WRITE



The IOCC1 is not used by the controller; however, it specifies the address of the I/O table, the first word of which contains the word count.

In the IOCC2, bits 8 - 12 specify the head number and bits 13 - 15 are used to define the desired sector within a given cylinder as shown in table 2-2 and 2-3, respectively.

Initiate Write Command Execution. When this command is received by the controller, assuming that the storage unit or controller is not busy with a previous command, the controller reverts to a busy status condition and begins a search operation to locate the desired sector. When the sector is located, the controller requests the first data word from the processing system via the data channel interface, writes the proper gap and sync word, then continues to write the data words received from the data channel.

The controller calculates and writes the proper MOD 4 check bits for each data word. Writing continues until a block complete signal is received from the processing system. When the block complete signal is received, the controller continues to write all ZEROS words until 322 total words are written. Normally 321 or less data words are written, but the controller continues to request and write words until the block-complete signal is received or until 322 words are written. If the end of sector is reached and a block-complete signal has not been received the data-error status condition is set. After a block-complete signal is received and 322 words are written, the operation complete status condition is set and a priority level interrupt is sent to the processing system.

Specifying a word count of zero results in the operation complete status and interrupt, but no writing occurs.

If the command is accepted the write operation is performed. The possible status conditions which result from a write operation may be processed by a Sense Device command issued after the interrupt is processed as described in paragraph 2.2.3.

**NOTE**

The cylinder address is not verified by the controller. It must be verified by software prior to issuing a write command by reading the first word of any sector and comparing the cylinder address in that word with the desired cylinder address.

The write operation always terminates and interrupts after 322 words are written. The controller always writes all zero words after the last data word is written until 322 total words are written. If the controller or storage unit is busy with a previous operation, the Write command is ignored (not recognized by the controller).

The timing associated with the Initiate Write command is shown in figure 2-6.

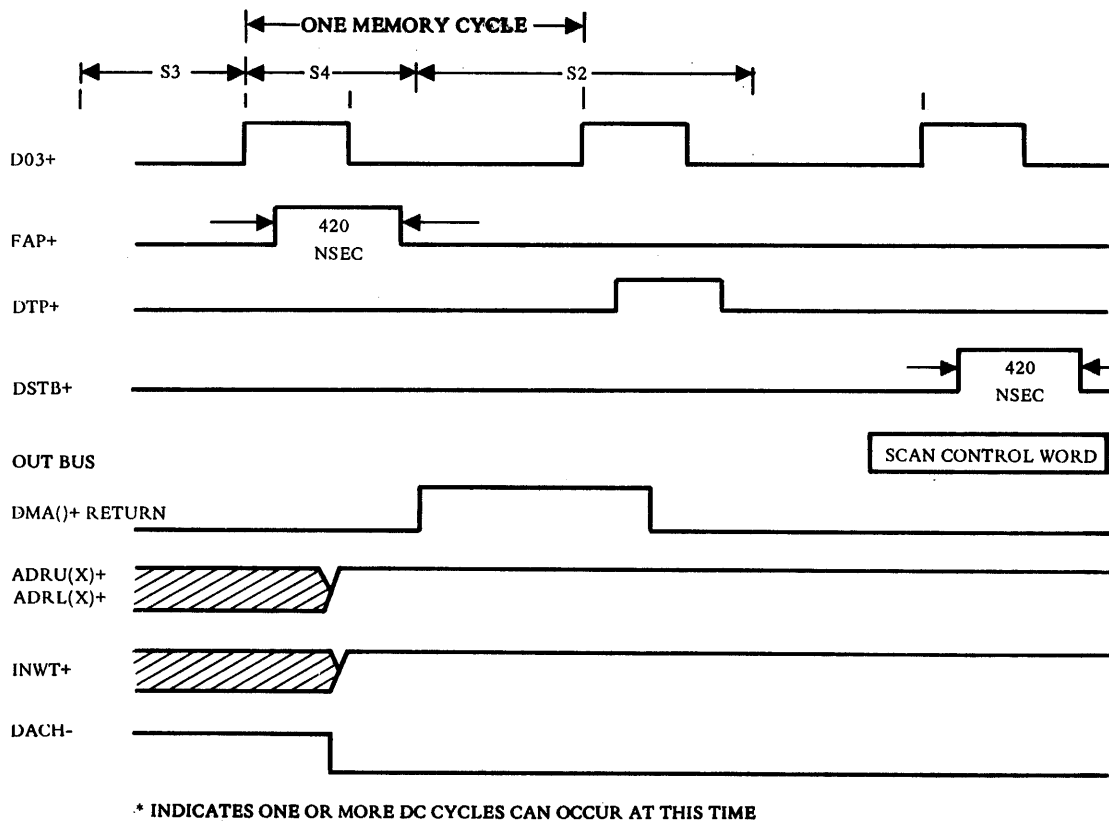


Figure 2-6. Initiate Write Timing (Applied to 1804 Processor)



### 2.2.6 INITIAL PROGRAM LOAD

The Initial Program Load (IPL) feature of the GA 18/30 system enables the operator to transfer a record from media into core memory using IPL hardware designed into selected controllers. Upon receipt of the IPL signal by the 1343 controller from the processing system, assuming that the storage unit is in a ready condition, the controller causes the storage unit to position its heads to cylinder 0, and then performs a 322 word read operation into core from head 0, sector 0. The IPL signal is ignored if the storage unit is not in a ready condition.

At the completion of the IPL operation, the controller generates an operation complete status and interrupt. This status should be reset prior to attempting any subsystem operations under program control. Reset is accomplished through execution of a Sense Device instruction with IOCC2 bit 15 equal to 1, or by the system reset signal from the processing system (press RESET switch on control panel).

## 2.3 DEVICE ADDRESSING (Area Code and Interrupts)

### 2.3.1 ADDRESSING

Up to four disk storage units may be connected to a GA 18/30. They are specified by bits 11 and 12 of the IOCC2 and the area code as shown in section 2.2.1 and table 2-1.

### 2.3.2 INTERRUPTS (Standard Equipment)

Six interrupt levels are provided for the GA 18/30 system. Each level has a unique hardware interrupt vector which is used to enter the subroutine that services the I/O device. The disk storage controller is assigned to level 2 and bits 0 - 4 are used for operation complete and seek complete for each of up to four drive, respectively.

## 2.4 18/30 DEVICE STATUS WORDS

Figure 2-7 presents the device status words associated with the 18/30 system including all standard peripherals.



18/30 DEVICE STATUS WORDS

Area	MODIFIER BITS							FEATURE	STATUS WORD BITS																
	8	9	10	11	12	13	14		15	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	1	1	0	0	0	0	0	0	Console Interrupt	Interrupt Request															
	0	0	0	1	0	0	0	0	Interval Timers	Timer A	Timer B	Timer C													
	0	1	0	0	0	0	0	0	Data Entry Switches	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	0	1	1	0	0	0	0	0	Teletype	Ready															
2								Card Punch Card Reader			Error		Operation Complete	Parity Error	Read Storage Protect Violation	Feed Check							Busy	Not Ready	
3								Paper Tape Reader/Punch										Reader Service Request	Punch Service Request	Reader Busy	Reader Not Ready	Punch Busy	Punch Not Ready		
6	0	0	0					Magnetic Tape Unit 0	Unit Select Bit	Unit Select Bit	Comm. Reject	End Of Table	Chain Stop	Data Chan. Error	Tape Data Error	Tape Mark	Data Over-run Error	Oper. Complete	Unit Select Bit	Wrong Length Recond	Tape Load Point	End Of Tape	Busy Or Rewinding	Tape Chan. Busy or Not Ready	
	0	0	1					Magnetic Tape Unit 1																	
	0	1	0					Magnetic Tape Unit 2																	
	0	1	1					Magnetic Tape Unit 3																	
	1	0	0					Magnetic Tape Unit 4																	
	1	0	1					Magnetic Tape Unit 5																	
	1	1	0					Magnetic Tape Unit 6																	
	1	1	1					Magnetic Tape Unit 7																	
							0	7-Track Odd Parity																	
							1	7-Track Even Parity																	
			0	0			7-Track 800 bpi																		
			0	1			7-Track 200 bpi																		
			1	0			7-Track 556 bpi																		
4								Disk Storage	Any Error	Operation Complete	Disk Not Ready	Disk Busy (RW) or Control				Data Error	Access Error	Seek Error	End of Cylinder					Sector Address	
8								Drum Storage (1342)	Any Error	Operation Complete	Drum Not Ready	Busy	End of Table		Lock-out	Data Error	Chain Error	Data Over-run	Illegal Track Addr.						
4								Disk Storage (1343)	Any Error	Operation Complete	Disk Not Ready	Disk Busy (RW) or Control				Data Error	Access Error	Seek Error	End of Cylinder					Sector Address	
8								Disk Storage (1344)	Any Error	Operation Complete	Disk Not Ready	Disk Busy (RW) or Control				Data Error	Data Over-run	Seek Error					C Model Access	Sector Address	
4								Disk Storage (1345)	Any Error	Operation Complete	Disk Not Ready	Disk Busy (RW) or Control				Data Error	Access Error	Seek Error	End of Cylinder				B Model Access	Sector Address	
5								Plotter	Service Response														Busy	Not Ready	
6								Line Printer	Transfer Complete		Printer Compl.	Channel 9	Channel 12	Channel 1	Parity								Carriage Busy	Printer Busy	Printer Not Ready
1	0	0	0	0	0	0	1	0	First Selectric	Printer Service Response	Keyboard Service Response		Printer Busy	Printer Not Ready	Keyboard Not Ready		Keyboard Parity Error	Printer Parity Error							
15	0	0	0	0	0	0	1	0	Second Selectric																
7	0	0	0	0	0	0	1	0	Third Selectric																

① Interrupt Condition      ② Indicator Reset by a Sense DSW  
Reset by Sense DSW

Figure 2-7. 18/30 Device Status Words





## SECTION 3 CONTROLLER PROGRAMMING FOR SPC-16 SYSTEM

### 3.1 GENERAL

This section contains information designed to show an unfamiliar programmer how to program the GA 1343 disk storage unit controller used in an SPC-16 disk system. Computer output commands, interface adapter and controller addressing, timing, status word, area code and interrupt information are all presented in a 'How To Use' format. A detailed description of program commands is also included in this section.

It is important to note that the information contained in this section applies to the SPC-16 disk system only. Programming information for the GA 18/30 disk system is provided in section 2 of this manual.

General Automation recommends that the user be familiar with the information contained in the SPC-16 Automation Computer reference manual (88A00238A) before programming the disk system.

Programming the disk system is made easy through the use of only four function commands. These commands are initiated at the computer in the form of SPC-16 XIO commands DTOR/DTOM and DTIR/DTIM. The XIO commands are passed to the controller via a programmed control interface adapter (PCIA) which interprets the commands and presents them to the controller as Sense Device (SEND), Control (CONT), Initiate Write (INWT) and Initiate Read (INRE).

The PCIA is part of the SPC-16 I/O interface system. More than one PCIA can be used in a system and each PCIA can accommodate up to 16 controllers depending on loading requirements or limitations. The PCIA operates in conjunction with other interface adapters as shown in figure 3-1.

Each PCIA requires the assignment of two device select functions (DSF's). The DSF's are part of the computer output commands and addresses the PCIA. DSF assignment is made at the system level of documentation.

If more than one controller is connected to a PCIA, and more than one PCIA is used in the system, the first output command (DTOR/DTOM) will address/select the specified PCIA, and the area code of the first object word (associated with the first output command) will address/select the specific controller. The second output command addressing the same PCIA and controller enables its associated object word which contains the function to be performed. The function to be performed is dependent on whether the second output command is DTOR/DTOM or DTIR/DTIM. Detailed use of these output commands is explained in paragraph 3.2.

The SPC-16 I/O interface system contains a Programmed I/O channel and a Direct Memory Access (DMA) channel. The disk storage system uses the DMA channel and may include the high speed data channel (HSDC) option. In addition, a multiplex data channel (MDC8) option is available as part of the DMA channel.

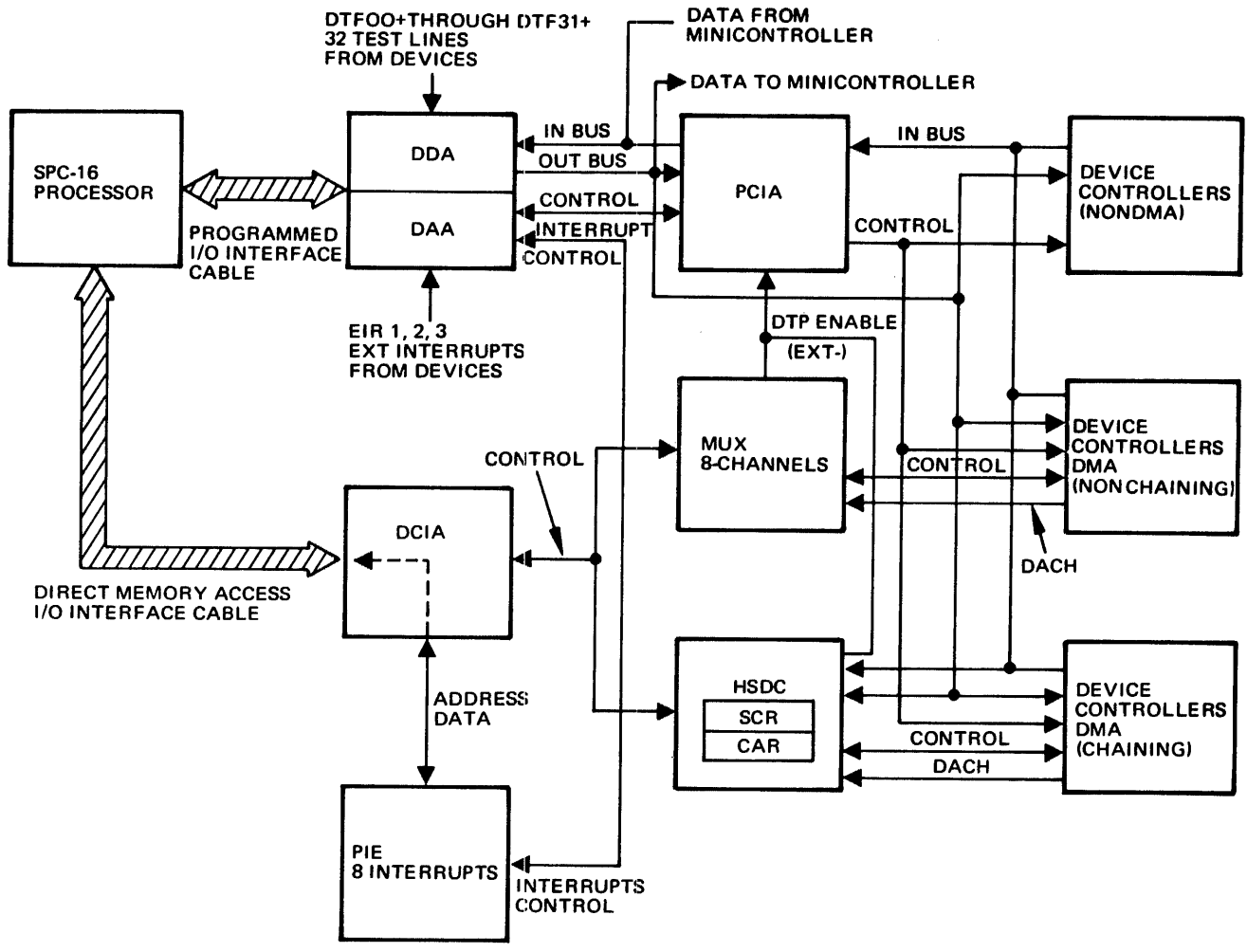


Figure 3-1. SPC-16 Interface System

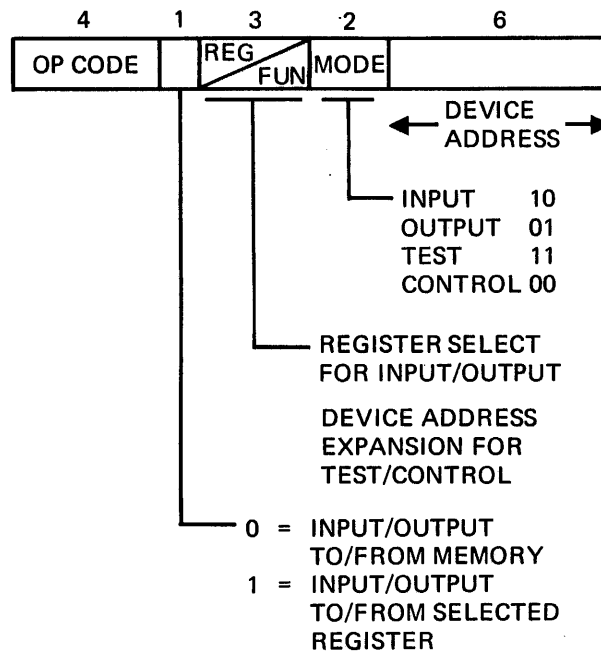
### 3.2 INPUT/OUTPUT COMMANDS

The SPC-16 XIO commands of DTOR/DTOM and DTIR/DTIM are interpreted by the PCIA and presented to the controller as Sense Device (SEND), Control (CONT), Initiate Read (INRE) and Initiate Write (INWT). These controller function commands cause the disk storage unit to perform the specified operation.

To initiate a SEND and CONT function command, the programmer must use two SPC-16 XIO output commands. The INRE and INWT function commands require only one XIO output command.

Each XIO output command has an associated object word which selects the controller and defines the function to be performed. The object words also have a modifier field for further definition.

The XIO output command whether DTOR/DTOM or DTIR/DTIM contains a six-bit device address field, a two-bit mode select field, a three-bit register select or device address expansion field, a one-bit input/output memory/register select field and a four-bit op-code field. Construction of the XIO command is shown in figure 3-2.



#### NOTE

1. When the source/destination is memory the memory address is contained in the selected register.
2. For test and control, bit 11 must be '0'.

Figure 3-2. XIO Command



The op-code (bits 15, 14, 13 and 12) portion of XIO command defines the class of instruction. Since instructions or commands used to communicate with external devices are always XIO commands, the op-code will always be '0001' as shown in figure 3-3.

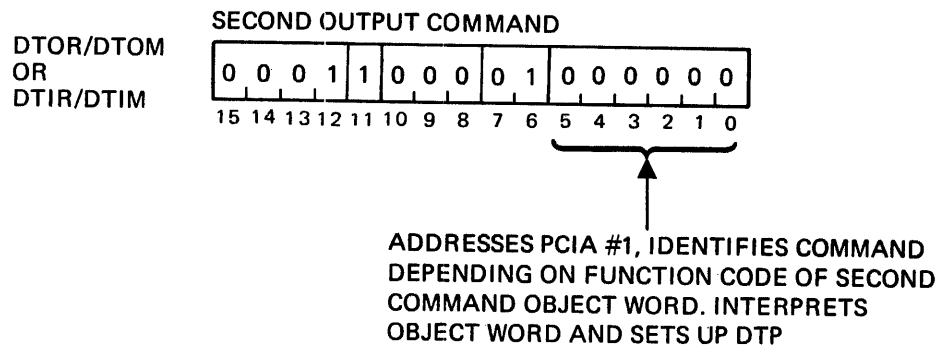
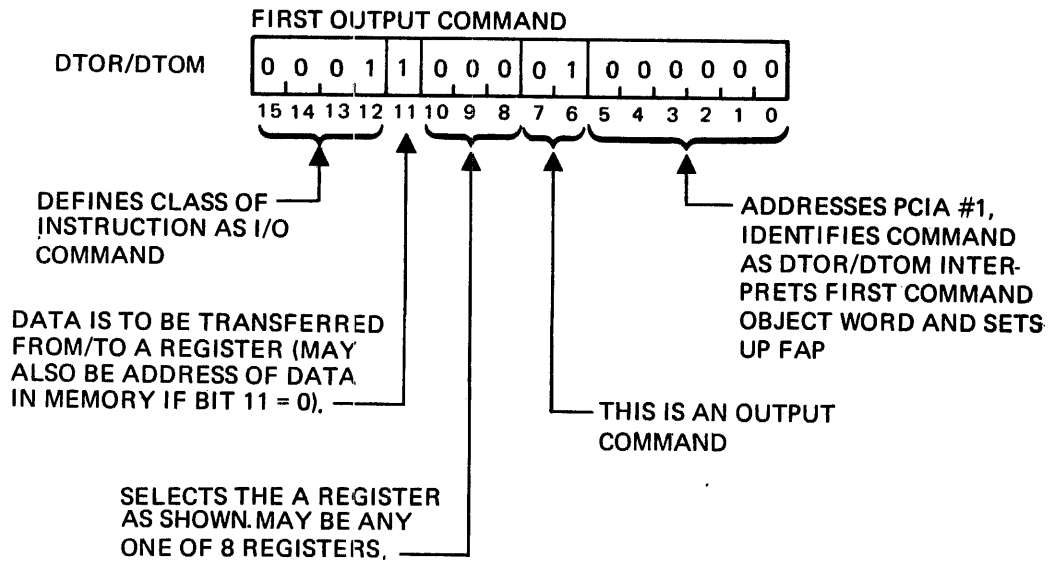


Figure 3-3. DTOR/DTOM and DTIR/DTIM Examples

Bit position 11 of the XIO command is used to define whether the transfer of data is from/to memory or from/to the selected register. If the transfer is from/to memory, bit position 11 should contain a '0'. If the transfer is from/to the selected register, bit position 11 should contain a '1'.

The register select field of the XIO command (bits 10, 9 and 8) is used to select the register or the register containing the memory address as source or destination for the following transfer of data. If the data is to be transferred from/to memory as specified by the contents of bit position 11, the starting address of the memory data is contained in the selected register. If the data is to be transferred from/to a specific register, the contents of bit positions 10, 9 and 8 will contain the identifier code for the register to be operated on. (Register mode useful only for status on disk) The register select identifier codes are shown in table 3-1.

Table 3-1. Register Identifier Codes

Bits				Bits			
10	9	8	Register	10	9	8	Register
0	0	0	A	1	0	0	B
0	0	1	X	1	0	1	C
0	1	0	Y	1	1	0	D
0	1	1	Z	1	1	1	E

In addition to register select, bit positions 10, 9 and 8 can be used for device address expansion when performing a test or control function as defined by the contents of bit positions 7 and 6.

The mode select field of the XIO command (bits 7 and 6) are used to indicate input, output, test or control as the designated mode of operation. Since all XIO commands are output commands to the device or input commands from the device, the mode select code should be '01' or '10'.

The device address field (bits 5, 4, 3, 2, 1 and 0) contains one of two device select functions DSF's. The DSF used in the first output command is '000000'. This code selects PCIA number one. If more than one PCIA is used a DSF code must be assigned for the second, third and/or fourth PCIA's. These codes are assigned when a system is configured that has more than one PCIA.

The DSF used in the second output command is '000001' for the first PCIA. Again if more than one PCIA is used, appropriate DSF codes must be assigned.

The DSF of the first output command is used by the addressed PCIA to set up a function address pulse (FAP) used in timing of the output commands to the controllers. The DSF of the second output command is used to set up a data transfer pulse (DTP) used as a strobe in transferring data.

If the controller function command requires only one XIO output command, as in the case of INRE and INWT, the second DSF function of DTP is derived from the data channel interface logic (high-speed data channel or multiplex data channel options).

For the purpose of this manual, the XIO output commands DTOR/DTOM and DTIR/DTIM will address the first PCIA as if only one PCIA is used.

Each DTOR/DTOM or DTIR/DTIM output command has an associated object word which must accompany the output command. The object word of the first output command defines the area code of the controller and the function to be performed: SEND, CONT, INRE or INWT. In addition, the object word contains a modifier field which is used to further define the operation. The object word of the second output command can contain specific data or status depending on the type of command. Figure 3-4 shows example object word.

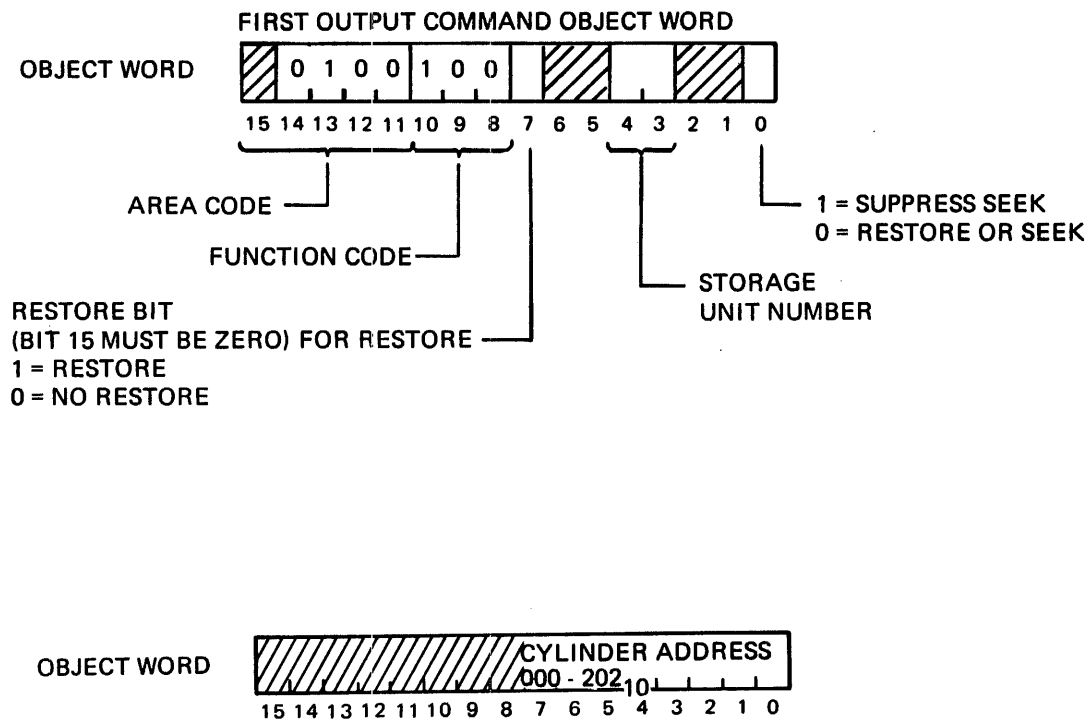


Figure 3-4. Object Word Example

Bit positions 14, 13, 12 and 11 of the first output command contain the area code for the controller. The disk storage unit controller uses area code 10100. Bit 15 of this object word is not used. The area code could be different if more than one controller was connected to a PCIA.

Function bits 10, 9 and 8 of the first output command object word are used to define the function to be performed. If a Sense Device (SEND) is to be performed, bits 10, 9 and 8 will be a '111'. The function code for a Control command (CONT) is '100'; the Initiate Read command (INRE) function code is '110'; and Initiate Write (INWT) is '101'.

The modifier field of the first output command object word (bits 7, 6, 5, 4, 3, 2, 1 and 0) is used differently for each command.

When the function code specifies a SEND, CONT, INRE or INWT operation, bits 4 and 3 of the modifier are used to select which unit, if more than one is connected to the controller is to be selected.

### 3.2.1 CONTROL COMMAND EXECUTION

The control function transfers one 16-bit word from the SPC-16 processor to the controller. Refer to table 3-1. Execution of the control function requires two SPC-16 DTOR/DTOM commands executed in the following sequence:

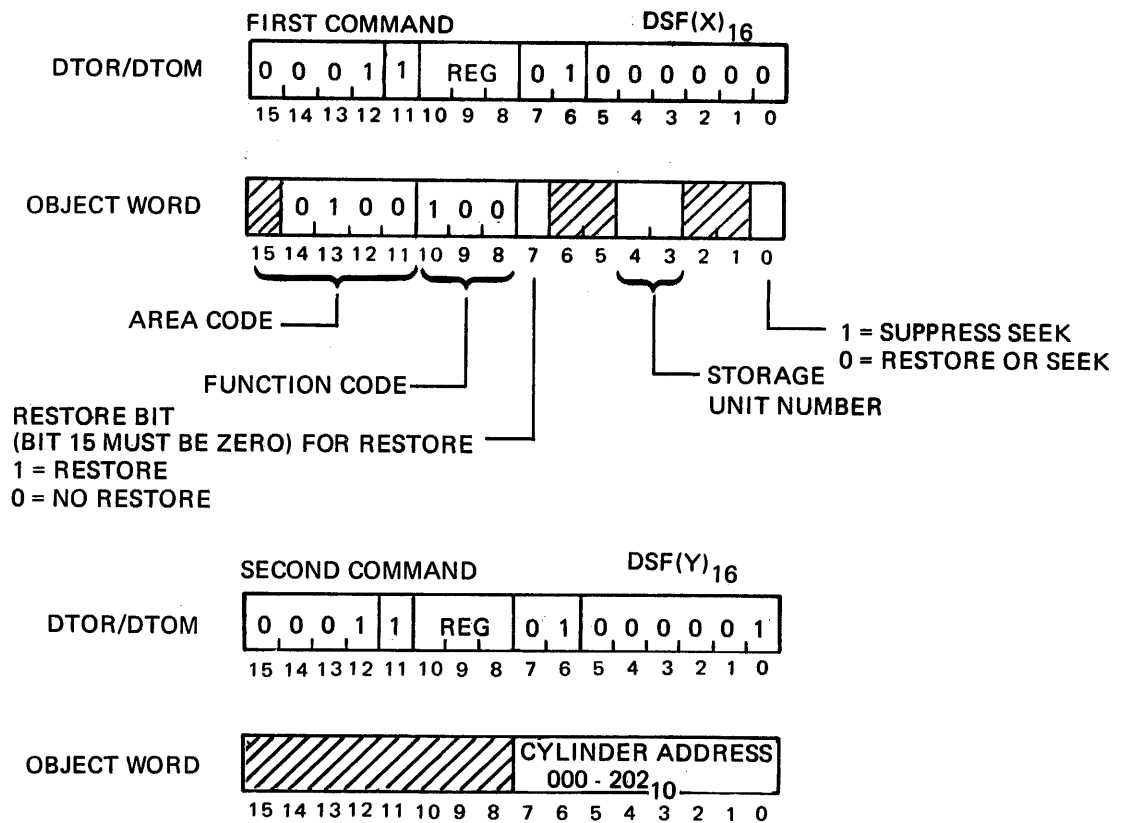




Table 3-2 Control Command Operations and Disk Number Decode

	Bits			Storage Unit (Up to Four)	Bits			
	7	0			4	3		
Seek to cylinder number specified in second object word.	0	0	No seek, select storage unit specified in bits 3,4.	0	0	0	0	
	0	1		1	0	1	0	1
	1	0		2	1	0	1	0
Perform a restore operation in storage unit specified in bits 3,4.	1	1	Illegal, no operation is performed.					

The control command is used to select a unit in order to test status or perform a read or write operation if multiple seeks are executed prior to these operations. Three operations may be performed with this command depending on the state of bits 0 and 7 as shown in the table 3-1. Bits 0 through 7 of the second object word specify the cylinder address in binary. Valid addresses are 0 - 202<sub>10</sub>.

Bits 11 through 15 of the first object word specify the standard area code (00100) to which the controller will respond. Bits 8 through 10 specify the function (100 for this command). Bit 7 specifies a restore operation is to be performed if bit 0 is a zero. Bits 3 and 4 specify the disk storage unit.

This command has both an on-line and off-line execution period. A portion of the execution occurs while the cylinder address is transferred to the storage unit. During this period, the controller is in a busy status condition. Then the seek operation occurs while the storage unit is off line. The controller is now able to accept other commands.

Control Command Execution - On-Line: When this command is received by the controller, assuming that the controller or storage unit is not busy executing a previous command a sequence of operations is performed. The difference address [calculated by the controller (cylinder address in bits 0 - 7 of the second object word - current arm position)] and direction of travel are transferred to the disk storage unit specified by bits 3 and 4 of the first object word. During this period, the controller returns to a busy status condition. If the controller is busy when this command is received, the command is ignored. When the start seek signal is transferred to the storage unit, assuming that the storage unit is not busy with a previous seek operation and that no status conditions exist which otherwise prevent the operation, the storage unit commences a seek operation to the cylinder address specified. Assuming that no previous status conditions exist, the possible status conditions when a Sense Device command is issued subsequent to a Control command are described later. A seek error occurs when the seek cylinder is larger than 202 or a seek is given to a busy unit (busy seeking).

After a Control command has been issued and a seek operation is initiated in a storage unit, the controller can accept other commands for the same storage unit or for other storage unit. In either case, the storage unit selected must be capable of accepting the command or the command will be rejected. The command will not cause the desired operation to occur but will force a status condition to occur in the selected storage unit. For instance, if a Control command is attempted with a storage unit which is currently performing a seek operation, the seek-error status condition occurs in the storage unit and the second seek is not performed.

Control Command Execution - Off-Line: After the start seek signal is transferred to the storage unit the seek operation is started by the storage unit and occurs whether or not that unit remains selected by the controller. Upon completion of the off-line seek operation, the storage unit reflects an access-ready status condition to the controller which then causes a priority level interrupt to the processing system

Execution of a seek operation in which the cylinder address specified is the same as the storage unit's current cylinder address will cause the priority level interrupt, even though no positioning movement occurs. The I/O signals associated with the Control command are shown in figure 3-5.

### 3.2.2 SENSE DEVICE COMMAND EXECUTION

Prior to initiating a Read or Write operation, the programmer will usually Sense Device to ascertain the current status of the disk storage unit. The Sense Device controller command (SEND) requires execution of the two XIO commands, one DTOR/DTOM and one DTIR/DTIM. Execution of this command causes one 16-bit device status word (DSW) to be transferred from the controller to the processor. The object word of the second XIO command is read to the processor as the DSW.

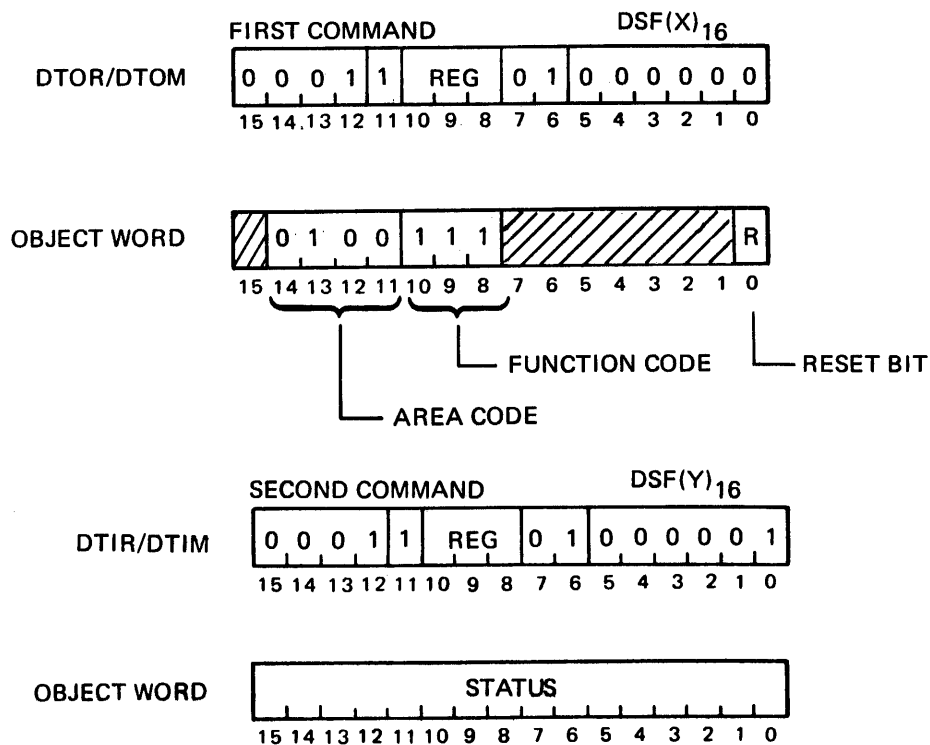
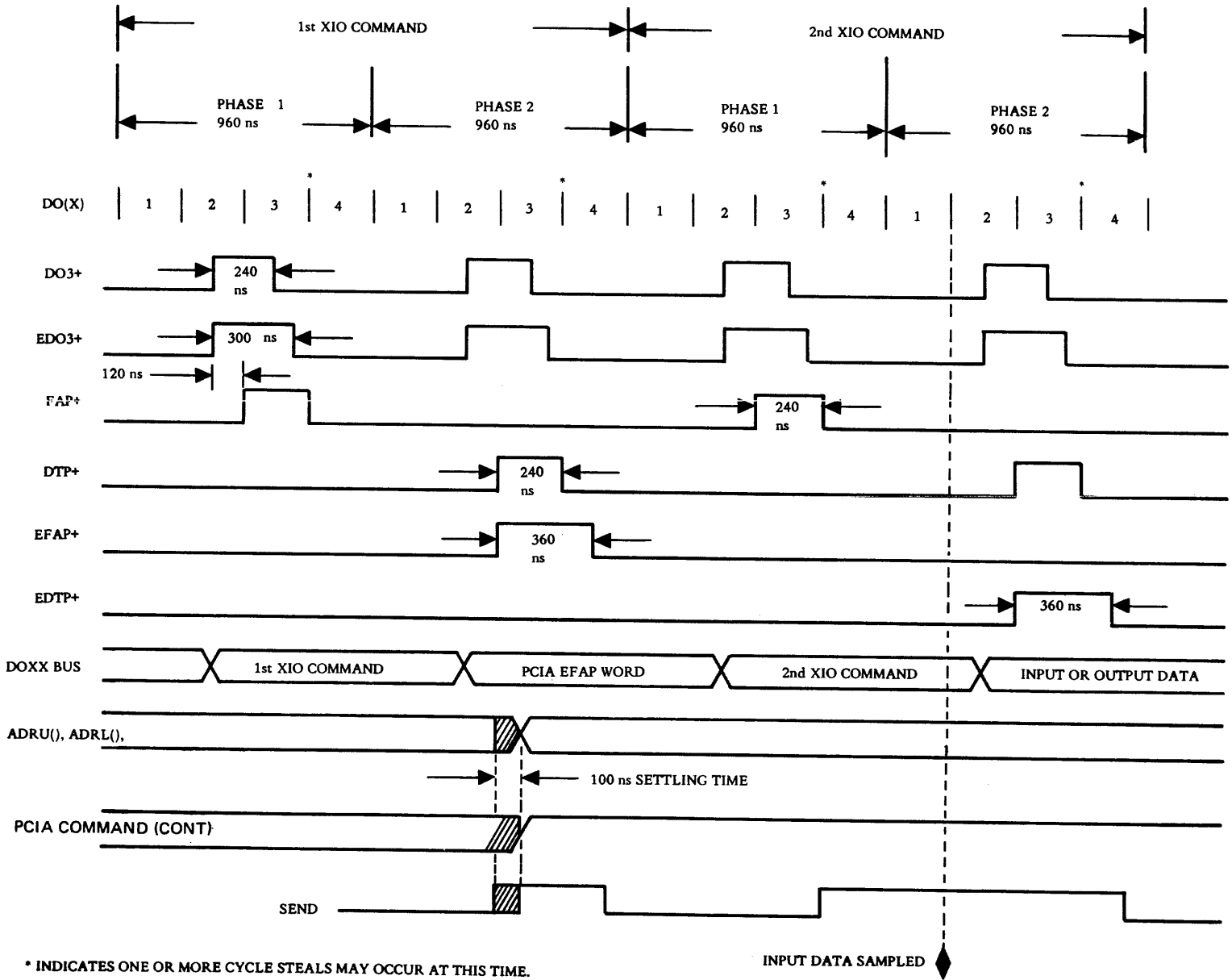


Figure 3-5. CONT and SEND Timing



\* INDICATES ONE OR MORE CYCLE STEALS MAY OCCUR AT THIS TIME.

INPUT DATA SAMPLED



GENERAL AUTOMATION, INC.

88A00116A

Sense Device Command Execution: When this command is received by the controller, the status of the controller and the currently selected storage unit are transferred to the processing system. This command is always accepted by the controller whether or not it is busy with a previous command and the status conditions are indicated as they currently exist in the equipment. The returned status will be from the currently selected storage unit. Bit 0 of the first object word is a reset bit and causes certain status conditions to be reset if it is a ONE. The single word transferred to the processor when this command is issued is called the device status word (DSW). The timing associated with the Sense Device command is shown in figure 3-5. Refer to figure 3-6 for disk DSW information. Refer to figure 3-9 at the end of this section for the other SPC-16 device status words.) The DSW status bits are defined as follows:

Bit 15 - Any Error: This bit is set to '1' if any of bits 5, 6 or 8 are set to '1', and is reset when all of the individual indicators are reset. These conditions cause an Operation Complete interrupt to occur.

Bit 14 - Operation Complete: An Initiate Read operation completes when the specified number of words are transferred or an end of sector is detected. An Initiate Write operation completes when the specified number of words are written and the remainder of the sector (if any) plus one additional word is written as an all zeros field.

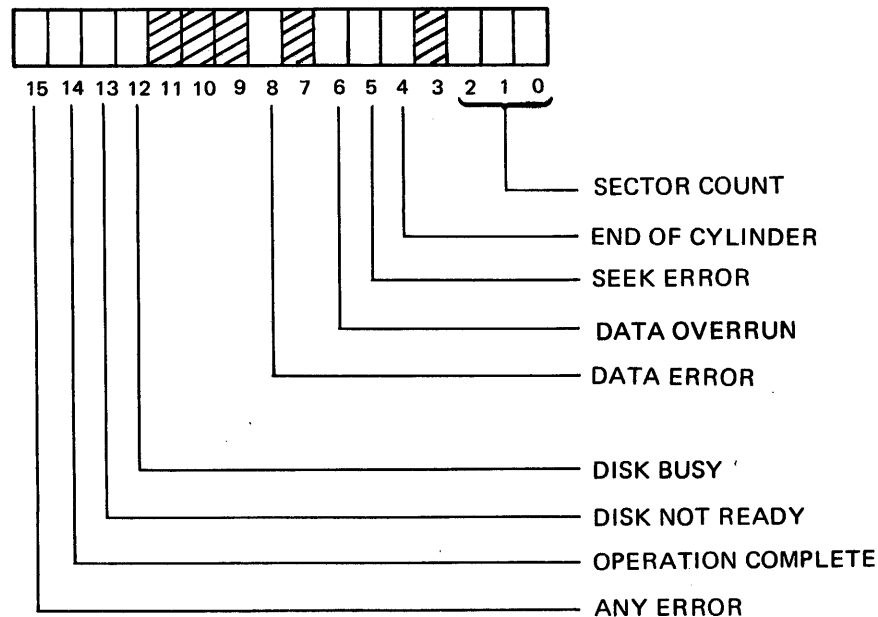


Figure 3-6. Model 1343 Disk Controller Device Status Word





This bit is the Inclusive OR of the operation complete status of up to four storage units and is set to a ONE upon completion of an Initiate Read (SCW bit 15 is a ZERO or ONE) or an Initiate Write operation.

Bit 1 of the DSW is set if any of the conditions listed below are present after an Initiate Write or Initiate Read operation:

1. Specified number of words have been transferred.
2. End of sector has been detected before the specified number of words have been transferred.
3. Completion of a seek operation either because of successful completion or seek error termination.

Operation complete is the only condition which causes an interrupt. This bit is reset by the Sense Device instruction when bit zero of the first object word is a ONE.

Bit 13 - Disk Not Ready: This bit is set to '1' when the disk drive not properly sequenced up, an unsafe condition exists in the storage unit, or the storage unit is busy performing a read or write operation.

Bit 12 - Disk Busy: This bit is set to '1' during the time the disk drive is performing a read or write operation.

Bit 11 - Not Used.

Bit 10 - Not Used.

Bit 9 - Not Used.

Bit 8 - Data Error: This bit is set to '1' if a cyclic check code error is detected during execution of an Initiate Read command.

Bit 7 - Not Used.

Bit 6 - Data Overrun (Access Error): This bit is set to '1' if a request to the processing system's memory is not honored in time, resulting in an erroneous or incomplete record written in core or on the disk.

Bit 5 - Seek Error: This bit is set to ONE if a cylinder address greater than 202 is attempted, or if a seek is directed to a storage unit that is busy executing a previously specified seek, or if a seek is directed to a storage unit that is busy executing a previously specified seek, or if a seek operation has not progressed to completion within 180 milliseconds, or if the storage unit detects a condition in its access mechanism which prevents it from positioning properly. Seek error resulting from either of the first two condition causes an operation complete status and a seek complete interrupt. This bit is reset by a subsequent control command to the same storage unit.

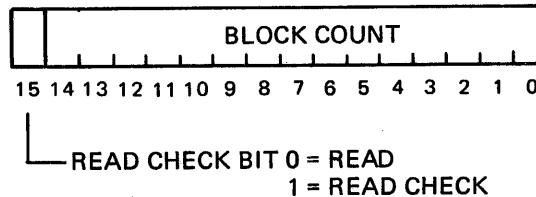
Bit 4 - End of Cylinder: This bit is set to a ONE when the head address register in the disk storage unit is set to an address greater than nine. This bit is reset by a subsequent Initiate Read or Initiate Write command with a valid (0-9) head number specified.

Bits 0, 1 and 2 - Sector Count: These bits depict the current status of the next sector to become available for reading or writing. These bits are updated as the disk rotates, always indicating the address of the next sector to come under the heads.

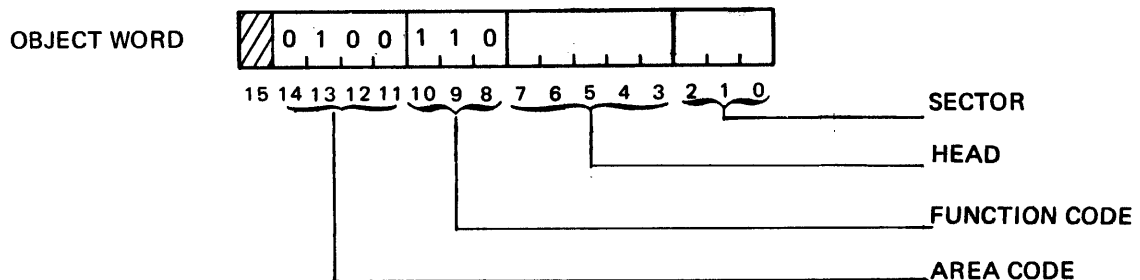
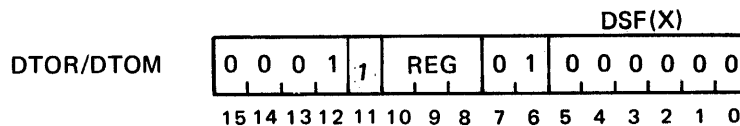
### 3.2.3 INITIATE READ COMMAND

The Initiate Read function is used in initiating data channel operations for controller to SPC-16 core transfers. Execution of the Initiate Read function requires one SPC-16 DTOR/DTOM command. This DTOR/DTOM command cannot be immediately followed by another DTOR/DTOM specifying DSF(X). One instruction cycle must be skipped. The Data Table Address and Block Count information must have been established prior to execution of the DTOR/DTOM. Refer to paragraph 3.2.6 for a description of the Data Table Address and a Block Count control. Timing for the Initiate Read command is shown in figure 3-7 and 3-8.

SCAN CONTROL WORD (SCW)  
(DEDICATED CORE LOCATION  
PER DATA CHANNEL,  $22_{16}$ )



CORE ADDRESS WORD (CAW)  
(DEDICATED CORE LOCATION  
PER DATA CHANNEL,  $23_{16}$ )



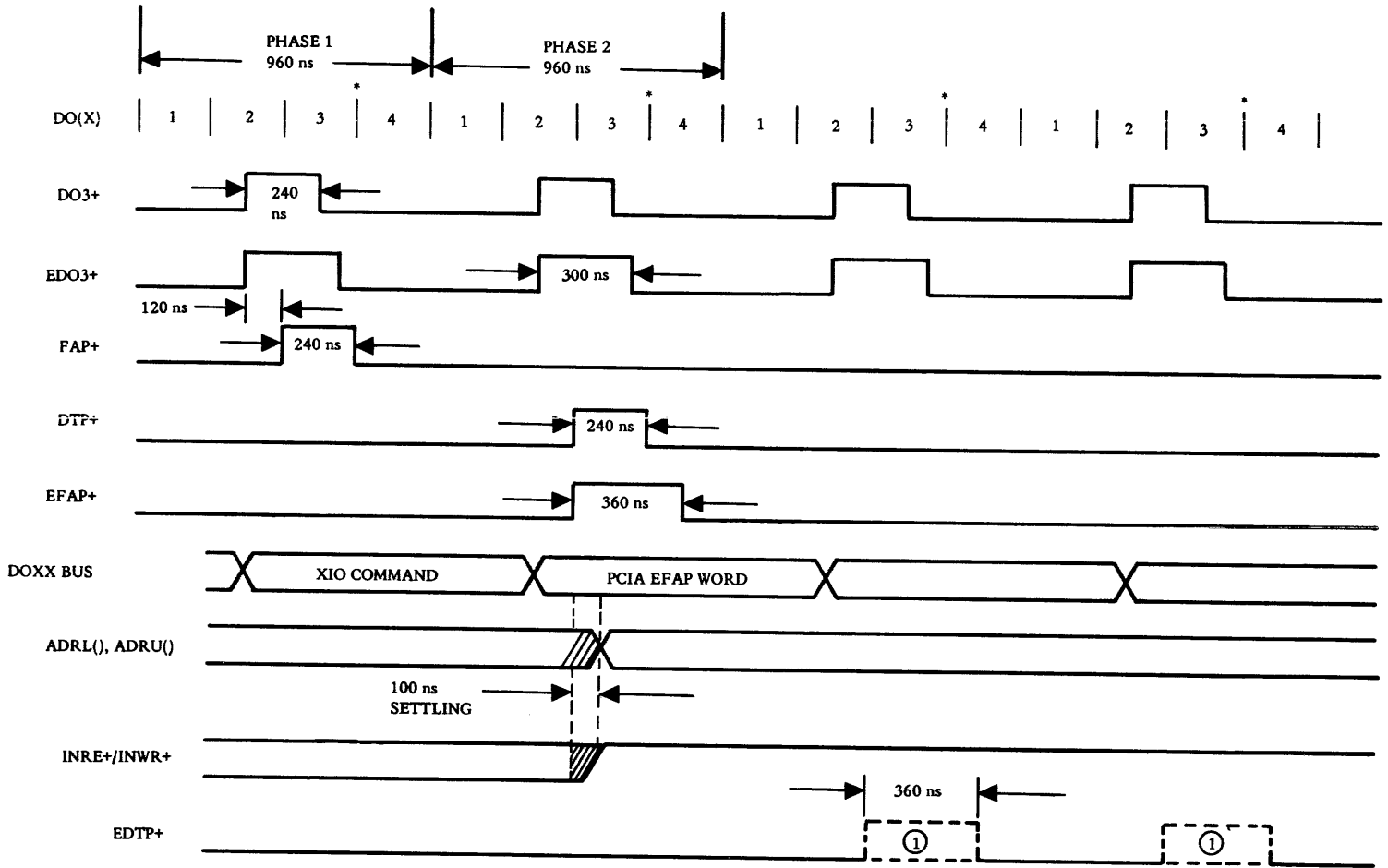
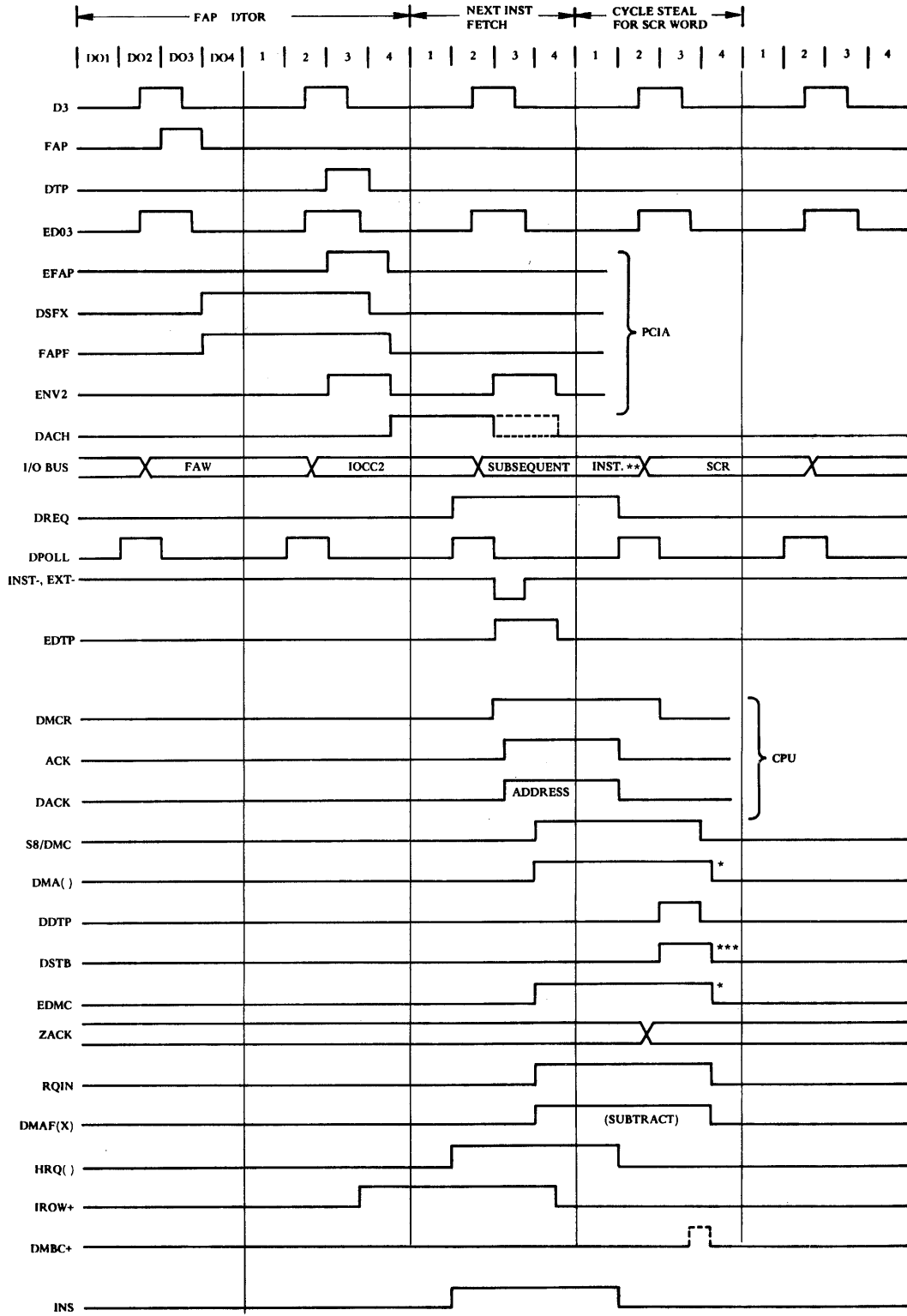


Figure 3-7. INRE/INWT Timing

① EDTP MAY OCCUR AT THE TIME SHOWN IN EITHER MEMORY CYCLE TIME DEPENDING ON WHETHER MDC8 OR HSDC IS ACTIVATED AND WHETHER OTHER CYCLE STEALS ARE IN PROGRESS.  
 \* INDICATES ONE OR MORE CYCLE STEALS MAY OCCUR AT THIS TIME.





\* THIS EDGE CAUSED BY TRAILING EDGE OF DSTB. \*\* CANNOT BE XIO INSTRUCTION WHICH ADDRESSES PCIA \*\*\* THIS EDGE ESTABLISHED BY PULSE EXPANDER IN DCIA

Figure 3-8. INRE/INWT Timing with MDC8 (Non-Chaining)

The Initiate Read command is used to transfer data from the controller to core via a data channel (DMA). Execution of this command requires one DTOR/DTOM output command. This command cannot be immediately followed by another DTOR/DTOM specifying DSF. This allows one computer cycle time to elapse before the next output command (DTOR/DTOM) is issued. A no-op instruction can be used to allow the necessary time for the data channel to become set (cycle-steal and SCR set-up). A DTOR/DTOM can be immediately followed by another DTOR/DTOM if the second DTOR/DTOM does not specify DSF (address the PCIA). In this case the second DTOR/DTOM would, for example, address the PIE. This is also true when executing an INRE command. The DSF of the first and only DTOR/DTOM will specify the PCIA and generate FAP as usual, however, since there are no second DTOR/DTOM output commands to generate DTP, this signal is produced by the data channel (MDC8 or HSDC).

Read Check: Bit 15 of the SCW is the read check bit. If bit 15 is a zero, a normal read operation is performed and data is transferred to the processing system. If bit 15 is a one, the operation is similar to a normal read except that data is not transferred to the processing system. The words are read from the disk and checked by the controller for MOD 4 check bits only.

Head Number Decode					
Head Number	Bits				
	7	6	5	4	3
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	0	0	0	0
17	1	0	0	0	1
18	1	0	0	1	0
19	1	0	0	1	1

Sector Decode			
Sector Number	Bits		
	2	1	0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1



Bits 3 - 7 of the second object word specify the head number decode and bits 0 - 2 specify the desired sector within a given cylinder. The control command is used to select a unit if a seek to another unit could have occurred prior to the Initiate Read command.

Initiate Read Command Execution: Assume the storage unit or controller is not busy with a previous command. When this command is received by the controller it returns to a busy status condition and begins a search operation to locate the desired sector. When the sector is located the first data word is read from the disk and checked for proper MOD 4 check bits. If bit 15 of the SCW is a ZERO, the controller transfers the word to the processing system via the data channel interface. Subsequent data words are checked and transferred until a block complete signal is received from the processing system, word count equal to 322 or end of sector (end of sector would be reached on an unwritten, i.e., not initialized, disk where no sync pattern could be located.)

After a block complete signal is received or 322 words are received, or the end of sector is detected, the operation complete status condition is set and a priority level interrupt is sent to the processing system. Specifying a word count of zero results in the operation complete status and interrupt, but no reading occurs. If the command is accepted and the read operation is performed (bit 15 of the SCW is a ZERO), the possible status conditions when a Sense Device command is issued after the interrupt are described later.

The read operation is performed by the controller at the currently positioned cylinder on the currently selected unit. Since the cylinder address is not verified by the controller, software checking of the cylinder address is required. The address can be checked by reading the first word of any sector or by reading the desired sector and verifying the address in the first word of the sector. During a read check operation (bit 15 of the SCW is a ONE), the operation proceeds as described except that no data is transferred to the processing system. The read check is always performed on all 321 words of the sector, then operation complete status is set and the processor is interrupted. The possible status returns when a Sense Device command is issued after the interrupt are the same as when bit 15 of the SCW is a ZERO except that the data-overflow and storage-error conditions can not occur.

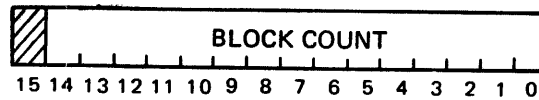
The read operation (bit 15 is a ZERO) normally terminates and interrupts after the last data word of the sector (or earlier). If the controller or storage unit is busy with a previous operation, the command is ignored (not recognized by the controller).

### 3.2.4 INITIATE WRITE COMMAND EXECUTION

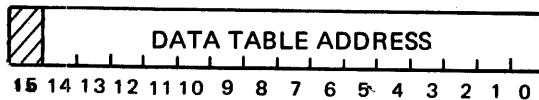
The Initiate Write function is used in initiating data channel operations for SPC-16 core to controller transfers. Execution of the Initiate Write function requires one SPC-16 DTOR/DTOM command. The DTOR/DTOM command cannot be immediately followed by another DTOR/DTOM specifying DSF(X). The Data Table Address and Block Count information must have been established prior to execution of the DTOR/DTOM. Relative timing for the Initiate Write command is presented in figures 3-7 and 3-8.



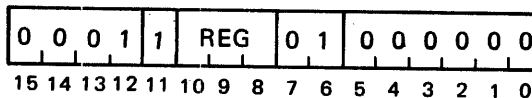
SCAN CONTROL WORD (SCW)  
(DEDICATED CORE  
LOCATION, 22<sub>16</sub>)



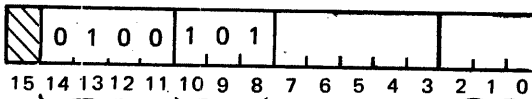
CORE ADDRESS WORD (CAW)  
(DEDICATED CORE  
LOCATION, 23<sub>16</sub>)



DTOR/DTOM



OBJECT WORD



SECTOR

HEAD

FUNCTION CODE

AREA CODE

The Initiate Write command is used to transfer data from core to the controller via a data channel (DMA). Execution of the INWT command requires one DTOR/DTOM output command. This command cannot be immediately followed by another DTOR/DTOM specifying DSF. This allows one computer cycle time to elapse before the next output command (DTOR/DTOM) is issued. A no-op instruction can be used to allow the necessary time for the data channel to become set (cycle-steal and SCR set-up). A DTOR/DTOM can be immediately followed by another DTOR/DTOM if the second DTOR/DTOM does not specify DSF (address the PCIA). In this case the second DTOR/DTOM would, for example, address the PIE. This is also true when executing an INRE command. The DSF of the first and only DTOR/DTOM will specify the PCIA and generate FAP as usual, however, since there are no second DTOR/DTOM output commands to generate DTP, this signal is produced by the data channel (MDC8 or HSDC).

In the object word, bits 3 - 7, specify the head number and bits 0 - 2 are used to define the desired sector within a given cylinder as shown in the tables.

Initiate Write Command Execution: When this command is received by the controller, assuming that the storage unit or controller is not busy with a previous command, the controller reverts to a busy status condition and begins a search operation to locate the desired sector. When the sector is located, the controller requests the first data word from the processing system via the data channel interface, writes the proper gap and sync word, then continues to write the data words received from the data channel.



Head Number Decode					
Head Number	Bits				
	7	6	5	4	3
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	0	0	0	0
17	1	0	0	0	1
18	1	0	0	1	0
19	1	0	0	1	1

Sector Decode			
Sector Number	Bits		
	2	1	0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

The controller calculates and writes the proper MOD 4 check bits for each data word. Writing continues until a block complete signal is received from the processing system. When the block complete signal is received, the controller continues to write all ZEROS words until 322 total words are written. Normally 321 or less data words are written, but the controller continues to request and write words until the block-complete signal is received or until 322 words are written. If the end of sector is reached and a block-complete signal has not been received the data-error status condition is set. After a block-complete signal is received and 322 words are written, the operation complete status condition is set and a priority level interrupt is sent to the processing system. Specifying a word count of zero results in the operation complete status and interrupt, but no writing occurs. If the command is accepted the write operation is performed. The possible status conditions which result from a write operation may be processed by a sense device command issued after the interrupt is processed as described later.



NOTE

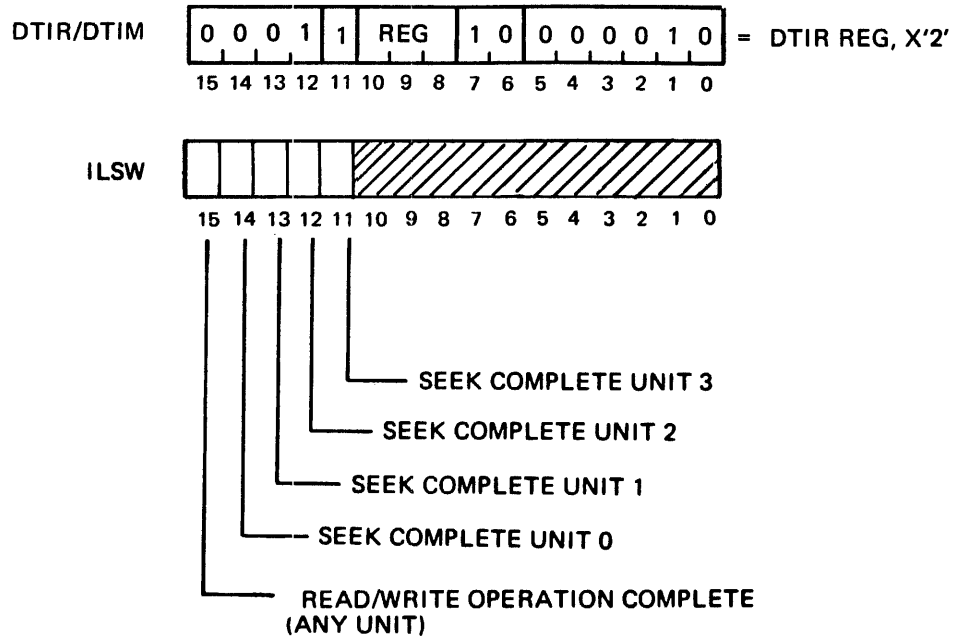
The cylinder address is not verified by the controller. It must be verified by software prior to issuing a write command by reading the first word of any sector and comparing the cylinder address in that word with the desired cylinder address.

The write operation always terminates and interrupts after 322 words are written. The controller always writes all zero words after the last data word is written until 322 total words are written. If the controller or storage unit is busy with a previous operation, the write command is ignored (not recognized by the controller).

3.2.5 SENSE INTERRUPT LEVEL

The Sense Interrupt function transfers one 16-bit status word from the controller to the SPC-16 processor. Execution of the Sense Interrupt Level function requires one SPC-16 XIO command, the DTIR/DTIM command. The DTIR must address a PIE. The PIE address for the 1343 disk controller is:

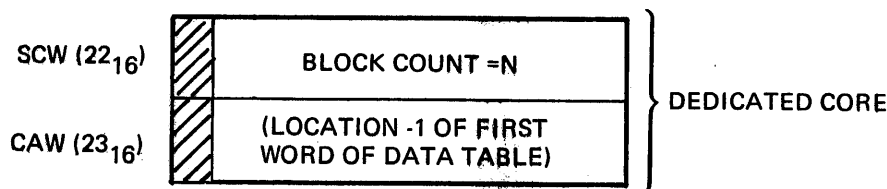
<u>PIE Number</u>	<u>PIE Address (Hex)</u>
1	$02_{16}$



### 3.2.6 MULTIPLEX DATA CHANNEL (MDC8)

Each multiplex data channel uses eight SCW/CAW pairs. These pairs are at locations 20 through 2F (Hex) or 30 through 3F (Hex). The SCW is used to specify a 16-bit Block Count. The 15-bit CAW specifies the location, minus one, of the first word of the data table. Following data channel initiation by the execution of an Initiate Write or Initiate Read DTOR/DTOM command, the preassigned SCW/CAW locations serve as the Block Count and Core Address registers and are updated by the MDC8 with each word transfer. The SPC-16 standard data channel assignment for the 1343 disk is:

Scan Control/Core Address Locations (Hex)	Controller
22/23	Disk



During an Initiate Read function, bit 15 is used for Read Check Mode.

### 3.2.7 SPC-16 DEVICE STATUS WORDS

The device status words associated with the SPC-16 system including all standard peripherals are presented in figure 3-9.



SPC-16 DEVICE STATUS WORDS

MODIFIER BITS																FEATURE	STATUS WORD BITS															
Area	8	9	10	11	12	13	14	15	15	14	13	12	11	10	9		8	7	6	5	4	3	2	1	0							
2																																
17																																
3																																
4																																
6	0	0	0																													
	0	0	1																													
	0	1	0																													
	0	1	1																													
	1	0	0																													
	1	0	1																													
	1	1	0																													
	1	1	1																													
									0																							
									1																							
					0	0																										
					0	1																										
					1	0																										
4																																
8																																
9																																
4																																
8																																
9																																
4																																
8																																
9																																
4																																
8																																
9																																
4																																
8																																
9																																
5																																
6																																
1	0	0	0	0	0	0	0	1	0																							
15	0	0	0	0	0	0	0	1	0																							
7	0	0	0	0	0	0	0	1	0																							

① Interrupt Condition    ② Indicator Reset by a Sense DSW  
Reset by Sense DSW

Figure 3-9. SPC-16 Device Status Words



## **SECTION 4 MAINTENANCE**

### **4.1 GENERAL**

This section provides function descriptions, mnemonic definitions, pin assignments and functional theory of operation information for the model 1343 disk controller.

The information in this section is intended to familiarize the user with disk controller operation, and enable senior level technicians to troubleshoot and maintain the equipment.

### **4.2 MNEMONIC DEFINITIONS**

Tables 4-1, 4-2, 4-3, 4-5, 4-6, 4-7, 4-8, 4-9 and 4-10, present the signal lists associated with the disk controller boards. The signal lists are presented in table form and contain pin numbers, signal mnemonic and a brief description of each signal. Table 4-1 contains the data buffer and word counter signal list. Table 4-2 contains the signal list associated with the PL connector of the signal board. Table 4-3 contains the signal list associated with the PC connector of the signal board. Table 4-4 contains the signal list associated with the PL connector of the control board. Table 4-5 presents the signal list associated with PL connector of the DC board. Table 4-6 contains the signal list associated with the PC connector of the DC board. Table 4-7 presents the signal list associated with the PL connector of the data board. Table 4-8 presents the signal list associated with the PL connector of the pulse shaper board. Table 4-9 presents the signal list associated with the PL connector of the phase modulator board. Table 4-10 presents the signal list associated with the PL connector of the data decoder board.



Table 4-1. Data Buffer and Word Counter Mnemonics

Pin	Term	Function Description
1		
3	BCRB-	Block complete remember
5	GND	
7		
9	DD15-	In bus bit 15
11	DD14-	In bus bit 14
13	DD13-	In bus bit 13
15	DD12-	In bus bit 12
17	DD11-	In bus bit 11
19	DD10-	In bus bit 10
21	DD09-	In bus bit 9
23	DD08-	In bus bit 8
25		
27		
29		
31	PSCT+	Set control flip-flops (not used)
33		
35		
37		
39		
41	RSTO-	Restore
43	OT00+	Out bus bit 0
45	SRCK-	Shift register clock
47	SRDA-	Shift register data
49	GND	
51	RSCT+	Reset word counter
53	OT15-	Out bus bit 15
55	OT14-	Out bus bit 14
57	OT13-	Out bus bit 13
59	OT12-	Out bus bit 12
61	OT11-	Out bus bit 11
63	OT10-	Out bus bit 10
65	OT09-	Out bus bit 9
67	OT08-	Out bus bit 8
69	SR15+	Shift register bit 15



Table 4-1. (continued)

Pin	Term	Function Description
71	DIPL-	Initial program load
73	SEQ3+	Sequence 3
75	LD-	Reset side of load flip-flop
77	ACK-	Acknowledge
79		
2		
4	CNTC-	Word counter count complete
6		
8	CNTC+	Count complete
10	DD07-	In bus bit 7
12	DD06-	In bus bit 6
14	DD05-	In bus bit 5
16	DD04-	In bus bit 4
18	DD03-	In bus bit 3
20	DD02-	In bus bit 2
22	DD01-	In bus bit 2
24	DD00-	In bus bit 1
26	BRCK+	B register clock
28		
30		
32	GND	
34		
36	+5V	
38	WRITE	Write
40	READ+	Read
42	SR03+	Shift register bit 3
44	SR02+	Shift register bit 2
46	SR01+	Shift register bit 1
48	SR00+	Shift register bit 0
50		
52	CSR0-	Clear shift register bit 0
54	OT07-	Out bus bit 7
56	OT06-	Out bus bit 6
58	OT05-	Out bus bit 5



Table 4-1. (continued)

Pin	Term	Function Description
60	OT04-	Out bus bit 4
62	OT03-	Out bus bit 3
64	OT02-	Out bus bit 2
66	OT01-	Out bus bit 1
68	OT00-	Out bus bit 0
70	BCR4+	MSB of mod 20 bit counter
72	SEQ0+	Sequence 0 (rest state)
74		
76	GND	
78		
80	+5V	



Table 4-2. Signal Board Mnemonics

Pin	Term	Function Description
PL CONNECTOR		
1		
3		
5	GND	
7		
9		
11	SA+	Sequence A
13	DD13+	In bus bit 13
15		
17	DOPR+	
19		
21		
23	SCTG-	Set cylinder tag line
25	BR0+	B register bit 0
27	CTTG-	Control tag line
29		
31		
33		
35	BRICK+	BR1 clock
37	SHRB+	
39	SHAB+	
41	SDTG-	Set difference tag line
43	SHTG-	Set head tag line
45	SENS+	Sense
47	SEKRDY+	Seek ready
49	GND	
51		
53	OT15-	Out bus bit 15
55	OT14-	Out bus bit 14
57	OT13-	Out bus bit 13
59	OT12-	Out bus bit 12
61	OT11-	Out bus bit 11
63	OT10-	Out bus bit 10
65	OT09-	Out bus bit 9
67	OT08-	Out bus bit 8





Table 4-2. (continued)

Pin	Term	Function Description
69	BRG+	
71	SFEC-	Attention
73	SECP+	Sector pulse
75		
77	INDEX	Index
79		
2	DO3+	
4		
6		
8	B102+	B register bit 1 or bit 2
10	BUS0-	Control bus bit 0
12	BUS1-	Control bus bit 1
14	BUS2-	Control bus bit 2
16	BUS3-	Control bus bit 3
18	BUS4-	Control bus bit 4
20	BUS5-	Control bus bit 5
22	BUS6-	Control bus bit 6
24	BUS7-	Control bus bit 7
26	BR5+	B register bit 5
28		
30		
32	GND	
34		
36	+5V	
38		
40		
42		
44		
46		
48		
50		
52		
54	CARY+	Carry condition
56	SEKER+	Seek error



Table 4-2. (continued)

Pin	Term	Function Description
58	NDCYL+	
60		
62	BR7+	B register bit 7
64		
66		
68		
70		
72	-3V	
74		
76	GND	
78		
80	+5V	



Table 4-3. Signal Board Mnemonics

Pin	Term	Function Description
PC CONNECTOR		
B1	CAR1-	Cylinder address register (1)
A1	GND	Cylinder address register (1)
B2	CAR2-	Cylinder address register (2)
A2	GND	
B3	CAR4-	Cylinder address register (4)
A3	GND	
B4	CAR8-	Cylinder address register (8)
A4	GND	
B5	CAR16-	Cylinder address register (16)
A5	GND	
B6	CAR32-	Cylinder address register (32)
A7	GND	
B8	CAR128-	Cylinder address register (128)
A8	GND	
B9	QSECT-	Sector pulse from disk unit
A9	GND	
B10	QINDY-	Index pulse from disk unit
A10	GND	
B11	QSEKRY-	Seek ready
A11	GND	
B12	QSEKR-	Seek error
A12	GND	
B13	QONLINE	Unit on line
A13	GND	
B14	QUNSF-	Unit safe
A14	GND	
B15	QBUS4-	B register bit 4
A15	GND	
B16	QBUS5-	B register bit 5
A16	GND	
B17	QBUS6-	B register bit 6
A17	GND	
B18	QBUS7-	B register bit 7
A18	GND	



Table 4-3. (continued)

Pin	Term	Function Description
B19	QCLOCKOUT	Safe line signal from I/O interface
A19	GND	
B20	QNDCYL-	
A20	GND	
B21	QSDIG-	Set difference address tag line
A21	GND	
B22	QSHTG-	Set head and direction tag line
A22	GND	
B23	QCTTG-	Set control tag line
A23	GND	
B24	QBUS0-	B register bit 0
A24	GND	
B25	QBUS1	B register bit 1
A25	GND	
B26	QBUS2-	B register bit 2
A26	GND	
B27	QBUS3-	B register bit 3
A27	GND	



Table 4-4. Control Board Mnemonics

Pin	Term	Function Description
PL CONNECTOR		
1	DSTB+	Data strobe
3	CTTG-	Set control tag line
5	GND	
7	DBC+	Block complete
9	DD15-	In bus bit 15
11	DD14-	In bus bit 14
13	SCTG-	Set cylinder tag line
15	ATFO+	Read/write complete
17		
19	B102+	B register bit 1 or 2
21	BR0+	B register bit 0
23	GO	Start sequencer
25	ADRU()+	Address upper code line
27	ADRL()+	Address lower code line
29	RSF1-	Reset controller sequencer
31	DD13-	In bus bit 13
33	DACH()-	Data channel
35	BRICK+	B register clock
37	SBRB+	
39	SHAB+	Set head address
41	REST+	Reset status
43	OT00-	Out bus bit 0
45	SENS+	Sense device status
47		
49	GND	
51	RSCT+	Reset word counter
53	RSTC+	Reset controller
55	D3+	General purpose clock from I/O interface
57	DAR1+	Device address bit one
59	OT12-	Out bus bit 12
61	OT11-	Out bus bit 11
63	OT10-	Out bus bit 10
65	BR5+	B register bit 5
67	OT08-	Out bus bit 8



Table 4-4. (continued)

Pin	Term	Function Description
69	BRG+	
71	CCLD-	Clear load flip-flop
73	SECP+	Sector pulse
75	LD-	Load flip-flop
77	INDEX-	Index pulse
79	SYRT+	
2	DO3+	General purpose clock from I/O interface
4	FAP+	Function address pulse
6	DTP+	Data transfer pulse
8	SHTG-	Set head and direction tag line
10	BUS0-	Control bus bit 0
12	SA+	Sequencer A
14	BUS2-	Control bus bit 2
16	BUS3-	Control bus bit 3
18	DD03-	In bus bit 3
20	DD02-	In bus bit 2
22	BUS6-	Control bus bit 6
24		
26	SOPC-	Set operation complete
28	SEKRDY+	Seek ready
30		
32	GND	
34		
36	+5V	
38	WRIT+	Write flip-flop set
40	READ+	Read flip-flop set
42	REST-	Reset status
44	CONT+	Control operation
46	INWT+	Initiate write
48	INRE+	Initiate read
50	SEND+	Sense device status
52	R15+	Bit 15 of IOCC2 (reset status)
54	CARY+	Cylinder address ready
56	DOPR+	Device operable
58	SEKER+	Seek error



Table 4-4. (continued)

Pin	Term	Function Description
60	SDTG-	Set direction tag line
62	BR7+	B register bit 7
64		
66	DAR2+	Device address bit 2
68	RCHK-	Read check bit
70	CMPR+	Compare signal
72	CMPR	Compare signal
74		
76	GND	
78		
80	+5V	



Table 4-5. DC Board Mnemonics

Pin	Term	Function Description
PL CONNECTOR		
1	SEQ3+	Sequence state 3
3	RDDB+	Raw read data
5	GND	
7		
9		
11		
13		
15	ATF0+	Read/write complete
17	DD11-	In bus bit 11
19	DD10-	In bus bit 10
21	DD09-	In bus bit 9
23	WRGT+	Write gate
25		
27	DACK	Data clock
29	WRD+	Write data
31		
33	OPCM+	Operation complete
35	OPCM-	Operation complete
37		
39		
41	REST+	Reset status
43	SCLK+	Separated clock
45	SENS	Sense
47	SRDA-	Serial read data into shift register
49	GND	
51	SIN()+	Sense interrupt
53	RSTC+	Reset count
55	D3+	DO3 time delayed
57	ACER+	Access error
59	DTERR+	Data error
61		
63		
65		
67		
69		





Table 4-5. (continued)

Pin	Term	Function Description
71	SFEC-	STAL line
73		
75		
77		
79		
2		
4	SDAT+	Separated data
6	SPHA-	Set phase
8	SEQ2-	Sequence 2
10	DD07-	In bus bit 7
12		
14	DD05-	In bus bit 5
16	DD04-	In bus bit 4
18	DD03-	In bus bit 3
20	DD02-	In bus bit 2
22	DD01-	In bus bit 1
24	DD00-	In bus bit 0
26	SDTU-	Separated data unshaped
28	INT-	Interrupt
30		
32	GND	
34		
36	+5V	
38		
40	READ+	Read flip-flop
42	DACK+	Data clock
44		
46		
48	BCR4-	Enabled during 4-bit sync time
50		
52	DAR1+	Disk address register bit 1
54	STOER+	Storage error
56	SEKER	Seek error
58	ENDCYL+	End of cylinder



Table 4-5. (continued)

Pin	Term	Function Description
60	RDTA+	Read data
62		
64		
66	DAR2+	Disk address register bit 2
68		
70		
72	-3V	
74		
76	GND	
78		
80	+5V	



Table 4-6. DC Board Mnemonics

Pin	Term	Function Description
PC CONNECTOR		
B3	ATTN3-	Interrupt from unit 3
A3	GND	
B4	MODSEL3-	Unit 3 selected
A4	GND	
B5	MODSEL2-	Unit 2 selected
A5	GND	
B6	ATTN2-	Interrupt from unit 2
A6	GND	
B7	WCX1-	Write clock
A7	GND	
B8	WCX2-	Write clock
A8	GND	
B9		
A9		
B10	WCX3-	Write clock
A10	GND	
B11	WCX0-	Write clock
A11		
B12		
A12		
B13	RCX2+	Read clock
A13		
B14	RCX3+	Read clock
A14		
B15		
A15		
B16		
A16		
B17		
A17		
B18		
A18		
B19		
A19		



Table 4-6. (continued)

Pin	Term	Function Description
B20		
A20		
B21		
A21		
B22		
A22		
B23		
A23		
B24		
A24		
B25		
A25		
B26		
A26		
B27		
A27	+3V	
B28		
A28	+3V	
B29	RCX1+	Read clock
A29	GND	
B30		
A30		
B31		
A31		
B32	ATTN1-	Interrupt from unit 1
A32	GND	
B33		
A33		
B34		
A34		
B35	RCX0+	Read clock
A35	GND	
B36		
A36		



Table 4-6. (continued)

Pin	Term	Function Description
B37	MODSEL1-	Unit 1 selected
A37	GND	
B38	MODSEL0-	Unit 0 selected
A38		
B39	-3V	
A39	GND	
B40	-3V	
A40	GND	



Table 4-7. Data Board Mnemonics

Pin	Term	Function Description
PL CONNECTOR		
1	DSTB+	Data strobe
3	BCRB-	Block complete remember
5	GND	
7	DMBC+	Block complete
9		
11	DBC+	MEM acknowledge and block complete
13		
15	CSRO-	Clear shift register bit 0
17	WRGT+	Write gate
19	GO-	Initiate read write or load
21	RDGT+	Read gate
23	RSTO+	Restore
25	SOPC-	Set operation complete
27	DACK-	Data clock
29	DMA()+	Memory acknowledge
31	DMR()-	Memory request
33	OPCM+	Operation complete
35	OPCM-	Operation complete
37	DMIN-	Direction read/write to DMA Interface
39	REST-	Reset status
41	DACK+	Data knowledge
43	REST+	Reset status
45	SRCK-	Shift register clock
47	BCR4-	MSB of mod 20 bit counter
49	GND	
51		
53	STOER+	Storage error
55	ACER+	Access error
57	RDTA+	Read data
59	DTERR+	Data error
61	DLY3-	Delay 3
63		
65		
67	CMPR-	Sector address compare



Table 4-7. (continued)

Pin	Term	Function Description
69	DCSE-	Core parity error or storage protect error
71	DIPL-	Initial program load
73	SEQ3+	Sequence 3
75	WRD+	Write data
77	ACK-	Memory acknowledge
79	SYRT+	System reset
2	DO3+	DO3 time
4	CNTC-	Word count complete
6	CTTG-	Control tag line (not used)
8	SEQ2-	Sequence 2
10	BUS0-	Control bus bit 0 (not used)
12	BUS1-	Control bus bit 1 (not used)
14	DMA()D+	Memory acknowledge
16	RSF1-	Reset control sequencer
18	BUS4-	Control bus bit 4 (erase gate)
20	BUS5-	Control bus bit 5 (not used)
22	SDLY3+	Set delay 3
24		
26	BRCK+	B register clock
28		
30		
32		
34		
36		
38	WRIT+	Write flip-flop
40	READ+	Read flip-flop
42	SR03+	Shift register bit 3
44	SR02+	Shift register bit 2
46	SR01+	Shift register bit 1
48	SR00+	Shift register bit 0
50		
52		
54		
56	SDLY4+	Set delay 4



Table 4-7. (continued)

Pin	Term	Function Description
58		
60		
62		
64	DLY4-	Delay 4
66	CMPR+	Sector address compare
68	SR15+	Shift register bit 15
70	BCR4+	MSB of mod 20 bit counter
72	SEQ0+	Sequence 0
74		
76	GND	
78		
80	+5V	





(Applies to 3 piggy-back Century Data boards only.)

Table 4-8. Pulse Shaper Board Mnemonics

Pin	Term	Function Description
PL CONNECTOR		
14	RDDB+	Raw read data
22	SRDDB+	Shaped ran read data
24	35NS	35 NS delay
26	25NS	25 NS delay
27	5NS	5 NS delay
28	15NS	15 NS delay
38	10NS	10 NS delay
40	20NS	20 NS delay
42	30NS	30 NS delay
44	40NS	40 NS delay
46	45NS	45 NS delay
48	50NS	50 NS delay
50	SELD	Selected delay
52	DSRDDDB+	Delayed and shaped raw read data

Table 4-9. Phase Demodulator Board Mnemonics

Pin	Term	Function Description
PL CONNECTOR		
10	OFST+	Offset
22	DSRDDDB+	Delayed and shaped raw read data
26	VFO+	Variable frequency oscillator
31	CLPH-	Clock phase
33		
35	VF02+	Half frequency VF0
38	DAPH-	Data phase
40	VF02-	Half frequency VF0
42	SPHA-	Set phase
44	RPHA-	Reset phase

(Applies to 3 piggy-back Century Data boards only.)



(Applies to 3 piggy-back Century Data boards only.)

Table 4-10. Data Decoder Board Mnemonics

Pin	Term	Function Description
PL CONNECTOR		
10	SDTU-	Separated data unshaped
26	VF0+	Variable frequency oscillator
27	WSTB+	Window strobe
35	VF02-	Half frequency VF0
38	VF02+	Half frequency VF0
40	DDAT+	Delayed data
50	DSRDDB+	Delayed and shaped raw read data
52	SDAT+	Separated data
54	SCLK+	Separated clock

### 4.3 FUNCTION DESCRIPTIONS

The model 1343 disk controller is housed on eight circuit boards. They are the data buffer and word counter board, the signal board, the control board, the data board, the DC board, the phase demodulator, shaper/delay line and the data decoder. The last three boards make up the phase lock system, described in paragraph 4.3.6. The circuit boards are described in the following paragraphs.

#### 4.3.1 DATA BUFFER AND WORD COUNTER

The data buffer and word counter handles the data transmitted to/from the disk storage unit.

The control function signals WRIT+ and READ+ determine the direction of data flow. When a Write command is decoded, the WRIT+ signal is high and the data word is transmitted from the out bus (OT00- through OT15-) to the B register at the time specified by the B register (BRCK+) clock. The data word is then sent to the shift register during the time that the check bits are being written (BCR4). It is shifted in a bit serial manner from the shift register to the disk storage drive with the shift register clock (SRCK-).

The decoding of a read command is indicated by READ going positive.

Read data from the disk storage unit enters shift register bit zero and is shifted right until a 16-bit word is assembled. It is transferred to the B register then to the processor via the in bus.

The word counter complete (CNTC+) signal is generated either during a Write command after 322 words have been written or during a read command when the block complete (DMBC-) signal is received from the processor. The DMBC signal during a write command disables memory requests and causes the remainder of a record to be written as zeros if it occurs before 321 words are written.

### 4.3.2 SIGNAL BOARD

The signal board contains two one shots, DLY3 and DLY4, two 8-bit buffer registers, output drivers for the control bus and tag lines, input receivers for the disk status, sector and index pulses and associated logic. The difference address (DIFO-7) is calculated on this board.

Set Cylinder Address Tag Line: When this line is true it indicates to the selected disk storage unit that the lines of the control bus now contain the address of the cylinder to be accessed. This tag pulse will set the address into the proper register in the disk storage unit. The bit assignments are shown in table 4-11.

Table 4-11. Cylinder Address Bit Assignment

Control Bus Bit Number	Cylinder Number
0	128
1	64
2	32
3	16
4	8
5	4
6	2
7	1

Set Difference Address Tag Line: When this line is true it indicates to the selected disk storage unit that the lines of the control bus now contain positioning information. This information consists of a binary number representing the one's complement of the difference between the disk storage unit current cylinder address and the cylinder address desired by the controller. This address is calculated by the controller. The bit assignments are shown in table 4-12.

Table 4-12. Difference Address Bit Assignments

Control Bus	Cylinder Difference
Bit 0	Not 128
Bit 1	Not 64
Bit 2	Not 32
Bit 3	Not 16
Bit 4	Not 8
Bit 5	Not 4
Bit 6	Not 2
Bit 7	Not 1



Set Head and Direction Tag Line: When this line is true, it indicates to the selected disk storage unit that the lines of the control bus now contain head select information and direction of travel required. The bit assignments are presented in table 4-13.

Table 4-13. Head and Direction Bit Assignments

Control Bus	Function
Bit 0	Forward
Bit 1	Not used
Bit 2	Not used
Bit 3	Head address 16
Bit 4	Head address 8
Bit 5	Head address 4
Bit 6	Head address 2
Bit 7	Head address 1

Control Tag Line: When this line is true, it indicates to the selected disk storage unit that the lines of the control bus now contain control information. Bit assignments are presented in table 4-14.

Table 4-14. Control Tag Bit Assignments

Control Bus Bit Number	Function
0	Write Gate. The write-gate function specifies that the data on the write-data line, from the controller is, to be written on the currently selected cylinder of the disk storage unit.
1	Read Gate. The read-gate function specifies that the data on the selected cylinder is to be transmitted over the read-data line to the controller.
2	Seek Start. The seek start function provides a pulse signal which starts a seek operation. The seek operation causes the head carriage mechanism to move from its present address to a new address. No motion takes place if the contents of the difference counter in the storage unit equal zero.



Table 4-14. (continued)

Control Bus Bit Number	Function
3	Reset Head Register. The reset head register function provides a pulse signal to clear the head address register (head 00 condition).
4	Erase Gate. The erase gate function enables the selected head to tunnel erase recorded data. To ensure a complete tunnel erase of the guard bands of a data record, the erase gate must remain active for a minimum of 20 microseconds after the write gate is inactive.
5	Select Head. The select head function, enables the selected head to read or write. The head selected is determined by the contents of the head-address register.
6	Restore. The restore function, initiate access motion to cylinder 000. The storage unit generates an attention signal upon completion of the restore operation.
7	Not used.

Cylinder Address Register: Eight lines from the disk storage unit cylinder address register indicate the present cylinder address to the controller. A set cylinder tag pulse changes the contents of the cylinder address register. These lines are active during the time that disk select is active.

Index Pulse (INDEX-): This line is used by the controller to receive a track reference mark, indicating the beginning of a track. The pulse width is approximately 80 microseconds.

Sector Pulse (SECP+): A pulse on this line indicates a track reference mark, to locate a sector within a track, from the selected disk storage unit. The pulse width is approximately 2 microseconds.

Selected Drive Unit Unsafe: This line indicates to the controller that there exists in the selected disk storage unit one or more of several fault conditions. They are:

- a. Multiple head select.
- b. Any head selected and not ready.
- c. DC write current and not write gate.
- d. Erase current and not erase gate.

- e. Write gate and no write current.
- f. Write gate and no write current.
- g. Read gate or not seek ready and either write gate or erase gate.
- h. Loss of dc power.
- i. Loss of primary power.

For any of the above conditions, the disk storage unit will deselect the heads and turn off the selected write and erase current, and hold them off until the unsafe condition is corrected.

Selected On Line: This line indicates that the selected disk storage unit is available. Conditions that make a unit not ready are:

- a. Head not loaded.
- b. No disk pack in unit.
- c. Disk pack cover not removed.
- d. Shroud cover open.

#### 4.3.3 CONTROL BOARD

The control board generates and accepts signals required to receive commands from the processor and performs all operations in the disk drive exclusive of the actual reading and writing. The more important signals generated on this board are: reset status (REST), sense status (SENS), compare (CMPR), control bus bits (BUS0, BUS2, BUS3, BUS6), set head and direction tag (SHTG), set difference tag (SDTG), set cylinder tag (SCTG), control tag (CTTG) and the start signal (GO+) that initiates sequencer operation on the data board.

#### 4.3.4 DC BOARD

The DC board contains a 5 mHz write oscillator, the device address decode, four write data drivers, four read data receivers, the serial read data (SRDA) and data clock logic (DACK), the seek complete (ATTN-) for four disk drives, interrupt logic and the DD- drivers for status bits 0, 5, 7, 9, 10 and 11. The double frequency write data is generated on this board by supplying the clock pulses at a 5 mHz rate and gating alternate pulses with the WRD (NRZ write data) signal from the data board. The serial read data signal (SRDA) is generated here by using the separated data signal from the phase lock system to set the data flip-flop which is then reset by the following data clock (DACK).

#### 4.3.5 DATA BOARD

The data board contains a sequencer to control the Initiate Read and Initiate Write operations. It also contains a 5-bit, 20 state counter, the 2-bit check bit counter and various read, write, error and control flip-flops. Logic on this board is normally activated by the GO+ signal from the control board. Reading or writing of a sector is controlled by this board including generation and checking of the MOD 4 parity bits. The compare signal (CMPR) and the two one shots (DLY3 and DLY4) are used to provide the zero gaps and sync areas of the sector format.

Data Board Sequencer: The sequencer on the data board consists of three flip-flops (FF0, FF1, FF2). These operate from the DO3- clock and are controlled by various timing and count signals. Flip-flop FF2 is the least significant bit. The sequence signals generated are SEQ0 and SEQ7.

These signals are used in conjunction with the timing and count signals to enable the logic of the sequencer flip-flops. The three flip-flops are counted in a grey code fashion.

Sequence states 0 and 1 are common to both the read and write operation. Sequence state 0 is the rest state. The conditions to enable the set logic of the FF2 flip-flop are GO- (generated on the control board sequencer) and no sector compare. Flip-flop FF2 is then set on the next DO3- clock and sequence state 1 is entered.

After state 1, sequencing is different for the read or write operation. Refer to paragraph 4.4 for a detailed description.

Some of the more important signals generated on the data board are described in the following paragraphs.

Clear Shift Register Bit 0 (CSR0): Sets shift register 0 and resets all other bits.

Operation Complete (OPCO): The OPCO flip-flop is normally set during a read operation by the block complete signal (DMBC) via the block complete remember flip-flop (BCRB). During a write operation, OPCO is set after the erase delay at the end of a sector. It can also be set by the SOPC signal during an Initiate Read or Initiate Write sequence if an illegal head address is specified or a zero word transfer is specified.

If OPCO sets, flip-flop OPCMis set on the next DO3 clock. OPCO is reset during SEQ0 but OPCM holds the operation complete condition for interrupt and status. OPCM is reset with a sense device command and bit 15.

Control Bus: Control bus bits 0, 1, 4 and 5 (BUS0-, BUS1-, BUS4-, BUS5-) can be activated from this board. Control bus bit 0 is the write gate, bit 1 is the read gate, bit 4 is the erase gate and bit 5 is the select head signal.

Write Gate: The write gate (WRGT) flip-flop is turned on in data board sequencer state 5. The normal reset is sequence state 4 (SEQ4-) after 321 data words and two additional all zero words have been written.

Read Gate: Read gate flip-flop (RDGT) is turned on in sequence state 3. The only reset is SEQ0+.

Control Tag Line (CTTG): When this line is true, it indicates to the selected unit that the lines of the control bus (BUS0, BUS1, BUS4, BUS5) now contain control information. CTTG is active when either the WRGT or RDGT flip-flop is set.

Error Flip-Flops: The error flip-flops are: ACR0, ACR1, DPED, DPER and STOER. The ACR0 and ACR1 flip-flops are access error flip-flops and are set to indicate a data overrun condition. DPED and DPER are the parity error flip-flops to detect a MOD 4 parity error condition.

The STOER flip-flop is set when the DCSE+ (logical OR of core parity error or storage protect violation) signal is received from the CIT interface.

Memory Request: The request (REQ) flip-flop is set in sequence state 5 during a write (preliminary request). Thereafter it sets at BCR4 time, the most significant bit of the bit counter. Everytime BCR4 is set, it defines the end of a word time.

Block Complete: The BCRB and BCR1 flip-flop are associated with block complete. When a block complete (DMBC) signal occurs during a read or write operation, BCRB is set and on the next DO3 clock BCR1 is set. This inhibits further memory requests (DMR) and in the case of a read command also sets the count complete (CNTC) flip-flop. During a read check operation, BCRB is set to inhibit all memory requests.

B Register Clock: BRCK during a read operation is equal to the signal BCR4, a flip-flop in the bit counter which is set during the four bit times which define the parity check bits. Data in the shift register (SR--) is transferred to the holding register (BR--) by BRCK. During a write operation, DMA()+ and DSTB+ form the signal BRCK which causes information to be clocked from the out bus (OT--) into the holding register.

Acknowledge: ACK- transfers information into or out of the shift register on the data buffer and word counter board. It is equal to the DMA() signal, which is the data channel acknowledge. During a read operation, data is transferred from the holding register to the shift register. During a write operation, data is transferred from the out bus into the holding register.

Check Bit Generation: The check bit generator consists of two flip-flops (CBR0, CBR1) connected as a binary counter. During a write operation the count is accumulated, MOD 4, for 16 bits. The four check bits are then written from the accumulated count as follows:

<u>CBR1</u>	<u>CBR0</u>	<u>Check Bits</u>
0	0	0 0 0 0
0	1	1 1 1 0
1	0	1 1 0 0
1	1	1 0 0 0

During a read operation, the 16 data bits and the 4 check bits are shifted into the counter. The last bit shifted in is checked for zero (the four valid check patterns all have the last bit equal to zero) and the counter is checked for zero after the last bit is shifted in. A data error is indicated if either check fails.

Bit Counter: The bit counter is a MOD 20 counter consisting of BCR0, BCR1, BCR2, BCR3 and BCR4 flip-flops. The counting sequence is shown below:





BCR									
4	3	2	1	0	4	3	2	1	0
0	0	0	0	0	0	1	0	1	0
0	0	0	0	1	0	1	0	1	1
0	0	0	1	0	0	1	1	0	0
0	0	0	1	1	0	1	1	0	1
0	0	1	0	0	0	1	1	1	0
0	0	1	0	1	0	1	1	1	1
0	0	1	1	0	1	0	0	0	0
0	0	1	1	1	1	0	0	0	1
0	1	0	0	0	1	0	0	1	0
0	1	0	0	1	1	0	0	1	1
					0	0	0	0	0

Sync Flip-Flop: During a write, in sequence state 6 the sync flip-flop is set and enables the counter logic. During a read operation, when a sync pattern is detected (SR00+, SR01+, SR02+ and SR03+), the sync flip-flop is set and identifies the beginning of data.

Shift Register Clock: The shift register clock (SRCK-) signal operates the shift register. It is identical to the data clock (DACK) except that the SRCK clocks are disabled during BCR4 time.

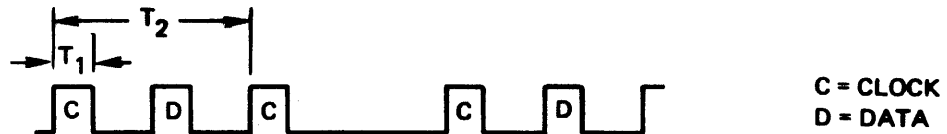
4.3.6 PHASE LOCK SYSTEM (Applies to 3 piggy-back Century Data boards only.)

This discussion presents one approach to the retrieval of high density information from a rotating magnetic medium. Data retrieval as used here will be concerned with the extraction of data after this data has been recovered and processed by the disk drive read electronics.

One commonly used technique for recording high density information is the double frequency or Manchester Method. This recording scheme writes a clock bit at the beginning of each data bit cell time and therefore doubles the recording frequency. Advantages of this method are numerous and include self clocking, a restricted set of output waveforms due to increased recording symmetry and low frequency noise immunity.

In the discussion which follows it is assumed that data recording is double frequency bit serial at a frequency of 5 mHz. Data characteristics at the output of the disk drive are shown in figure 4-1.

There are two phenomena which result in frequency variations in the read back or raw data. One is a slowly varying function of time and results from gradual changes in the RPM of the disk drive. Variations in rpm may be as large as +2% from nominal; however, the rate of change of rpm variations is small during the time required to transfer a data record. A worst case +4% variation from drive to drive may exist, however. The second phenomenon is an instantaneous frequency shift due to the uncertainty regarding the time occurrence of an incoming pulse. This uncertainty is caused primarily by magnetic pulse interference and is commonly known as pulse crowding.



$T_1$  = PULSE WIDTH = 80 + 10 NS

$T_2$  = DATA CELL TIME = 400 + 70 NS

RISE AND FALL TIMES ARE 30 NS

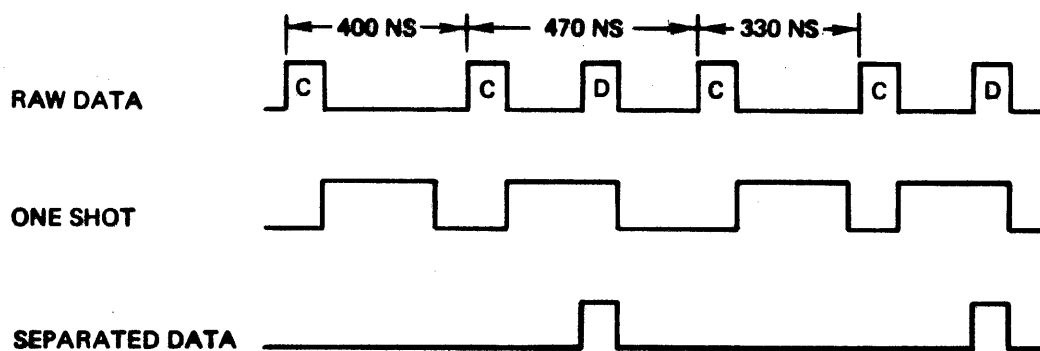
(Applies to 3 piggy-back Century Data boards only.)

Figure 4-1. Raw Data Characteristics

The purpose of the phase lock system (PLS) is to compensate for frequency variations due to rpm changes while remaining relatively insensitive to pulse crowding. In addition to this frequency tracking requirement, the phase lock system separates data and clock bits from the incoming raw data signal.

Before discussing in detail the operation of the phase lock system an alternate method of data retrieval employing one shots will be presented. An analysis of the two schemes will indicate the superiority of the phase lock system because of its ability to more accurately define the beginning and end of a data bit cell. The data bit cell time is predicted from a time average of previous cell times derived from frequency information in the incoming raw data. Instantaneous frequency shifts due to pulse crowding are thereby minimized.

A one shot system in general utilizes the falling edge of each clock pulse to trigger a fixed duration one shot. If a raw data pulse should occur during this time increment, this pulse is output as data. Figure 4-2 shows the timing of a one shot system used to recover data.



(Applies to 3 piggy-back Century Data boards only.)

Figure 4-2. One Shot Timing

It has been assumed that a method is available to distinguish between clock and data pulses. This scheme utilizes the self clocking properties of double frequency recording to define the beginning of a bit cell. The one shot duration is determined by the variations in the bit cell time due to rpm differences, pulse crowding and read data pulse width.

The phase lock system (PLS) is shown in figure 4-3. A description of its operation is given below. Initially the PLS has been packaged using the three Century Data boards mounted in piggyback fashion onto three General Automation universal boards. Both sets of board pin numbers, the Century Data and the General Automation universal boards, are shown in figure 4-3.

Pulse Shaper: The pulse shaper is used to remove pulse width variations in the incoming raw data so that the input to the error detector is a fixed width pulse nominally 100 ns in duration. Operation of the error detector is relatively independent of pulse width; however, as this signal defines a sampling period the requirement exists that the pulse width remain constant during a data record.

Delay Line: The delay line is used to compensate for inherent delays in the error detector, variable frequency oscillator (VFO) and phase control circuits.

Error Detector: The error detector generates an error signal that is proportional to the phase relationship of the incoming raw data and an internal variable frequency oscillator. When the phase lock system is locked onto the incoming raw data, the VFO lags the incoming data by  $90^\circ$  and the error signal is zero. The error signal is integrated to form a time average error signal so that instantaneous frequency changes do not appear as a frequency error. Response to pulse crowding is therefore minimized. The response time of the phase lock system is chosen so that the initial lock up time is acceptable but after lock up only slowly varying frequency shifts associated with disk rpm changes are tracked. Figure 4-4 shows the error detection timing relationships assuming double frequency raw data (clocks and data).

In figure 4-4 the lock-up time has been exaggerated to show the operation of the error detector and variable frequency oscillator.

Variable Frequency Oscillator (VFO): The VFO is a free running oscillator nominally operating at 5 mHz. Its actual tracking frequency is controlled by the output of the error detector. An error of one polarity will increase the VFO frequency while an error of the opposite polarity will decrease its frequency. The output of the VFO is used by the phase control and decoder circuits to define the bit cell time.

Phase Control: The phase control circuit consists of a D flip-flop which is toggled by the VFO. Its output is therefore nominally 2.5 mHz and serves to define when the incoming data is a clock or data bit. Once the VFO has locked onto and is tracking raw data the phase control must be orientated to be in the proper phase relationship to the incoming data and clock bits. The means of initializing the phase control are numerous and depend primarily on the record format. A common method is to write an all zero area (clocks only) before the actual data record and enable the phase lock system in this area. After enabling, the phase control can be orientated so that only separated clocks are being output from the decoder. One drawback to this method is that during lock-up the VFO is seeing single frequency data and therefore the error sampling rate is one half that obtained with double frequency data.

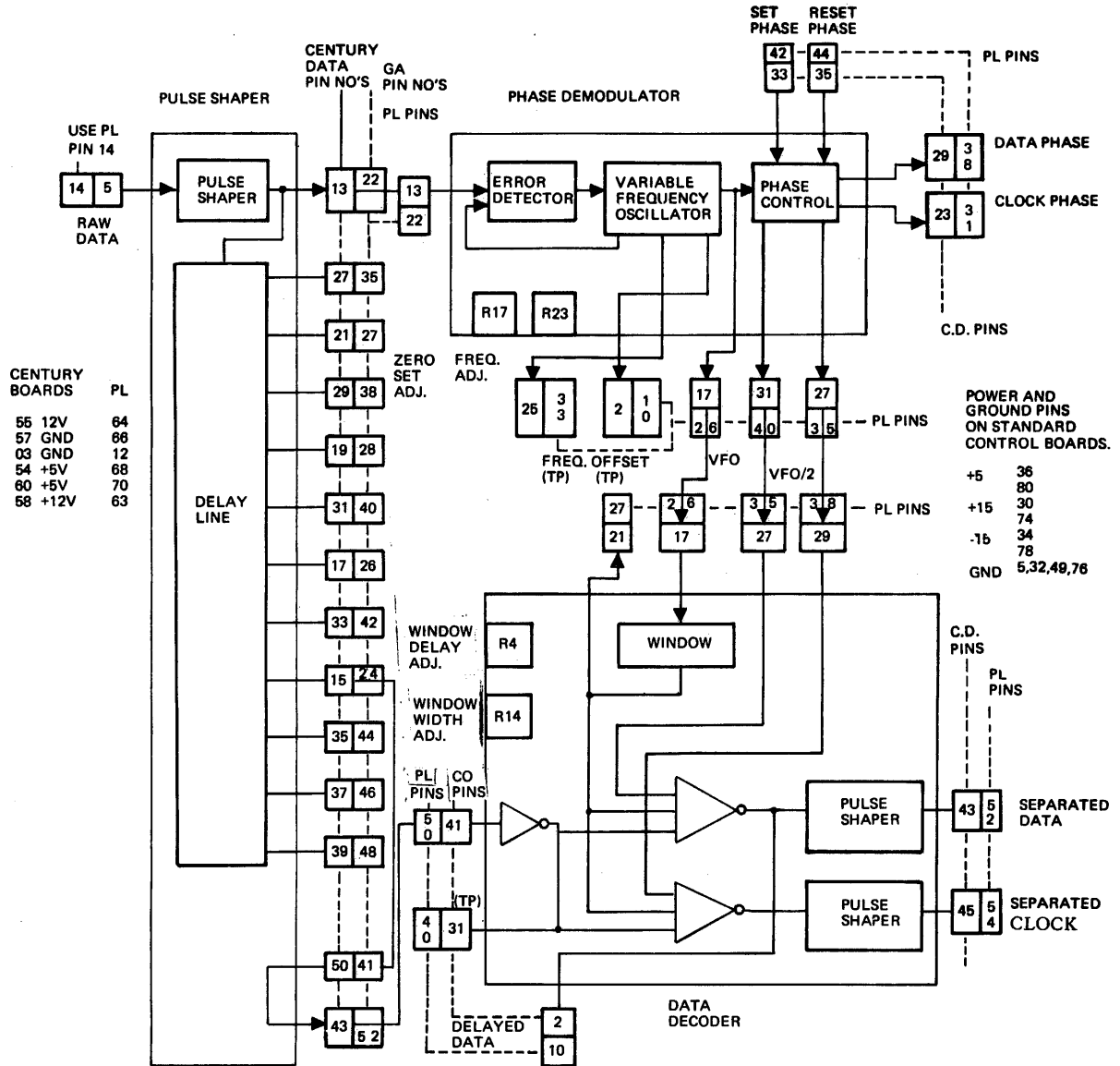
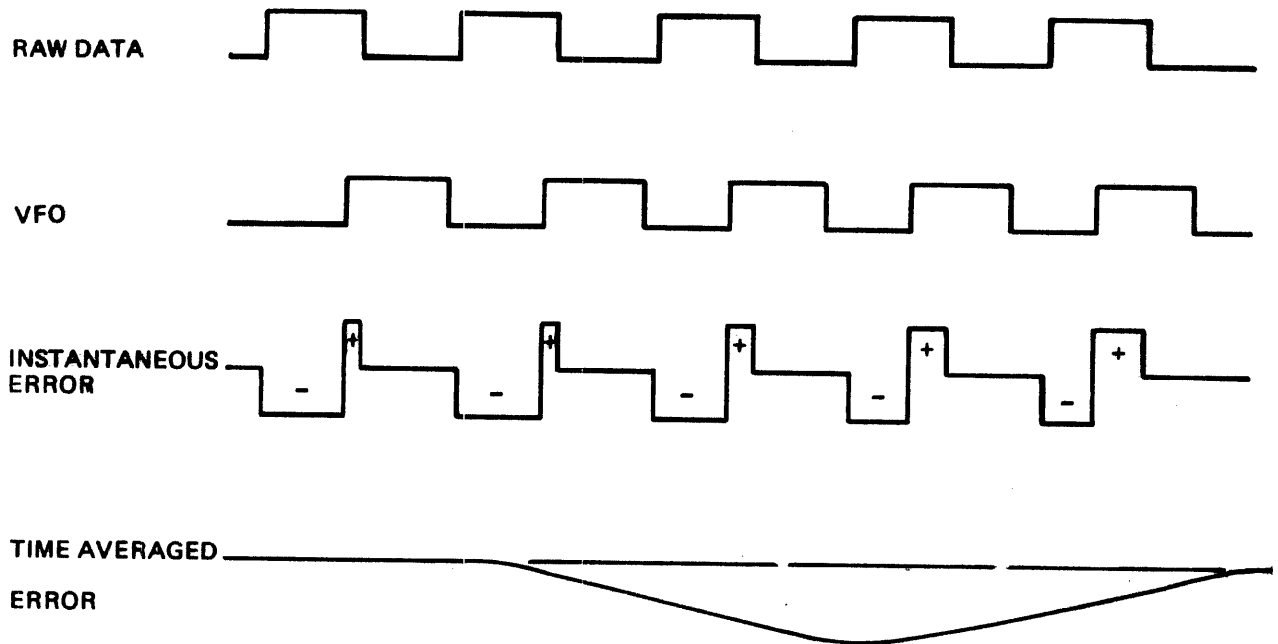


Figure 4-3. Phase Lock System

(Applies to 3 piggy-back Century Data boards only.)

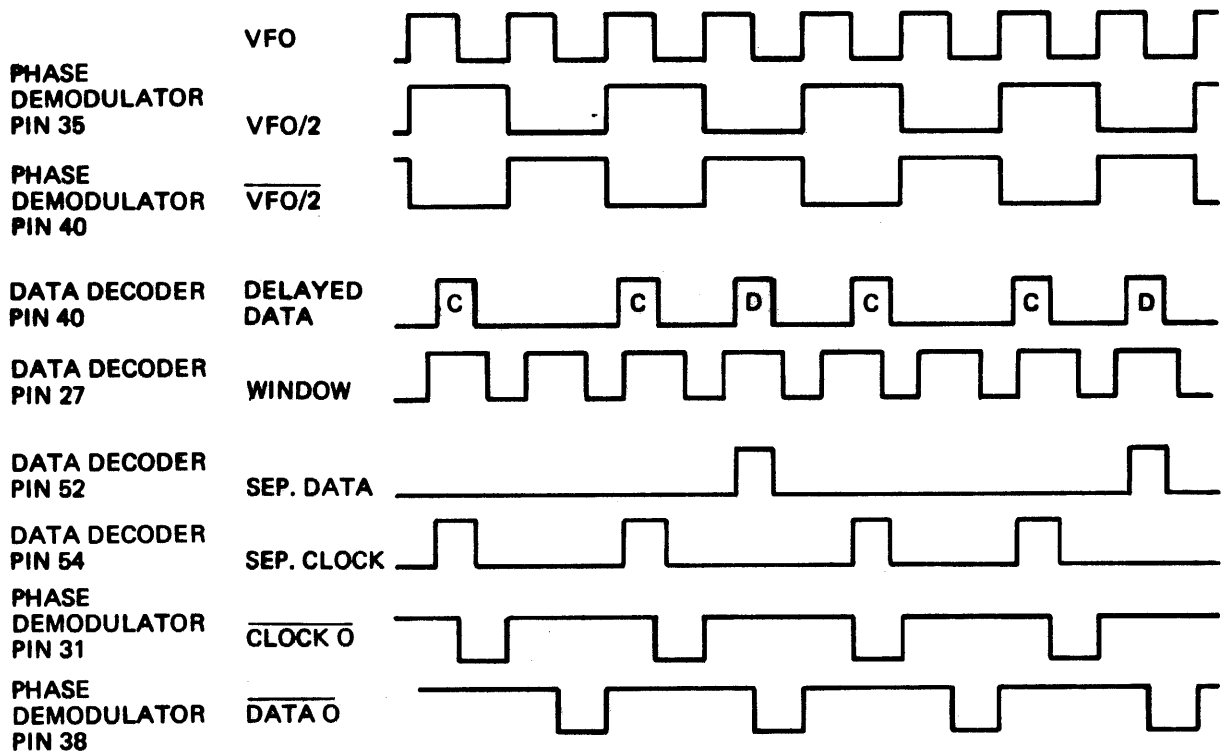


(Applies to 3 piggy-back Century Data boards only.)

Figure 4-4. Error Detection Operation

**Decoder:** The decoder receives as inputs delayed data, clock and data phase information and generates separated data and separated clock. A data window is generated by the decoder and is used to improve the resolution of the system. In adjusting the decoder the delay line output is chosen so that delayed data is positioned in the center of the VFO/2 signal. The window is then adjusted for a pulse width of 80 ns and is centered with respect to VFO/2 also. Since these signals are derived from the variable frequency oscillator they will track the frequency of the incoming data. The window serves as a strobe to define the sampling period for the data and clock bits. Because of pulse crowding the window may not always be in coincidence with delayed data and therefore separated data and separated clock will exhibit pulse width variations. To correct this the products of VFO/2 and VFO/2 prime, delayed data and the window are input to a pulse shaper network which outputs a 70 ns pulse. Maximum pulse crowding which can be tolerated is defined by the blanking interval formed by the window. Figure 4-5 shows the timing relationships of the decoder. Also shown to the right are the test point locations on the General Automation controller board.

There are several ways of implementing the phase detector into a system. The methods are varied and will be described in general terms only. The first function to be performed in any scheme is to orientate the phase lock system with respect to clocks and data. The important requirement here is to define data preambles and format so that data records may be unambiguously recognized. This includes an area in which the VFO may track and lock onto raw data, an area in which sufficient information is available to orientate the phase control and an area which uniquely defines the beginning of the data record. In order to orientate the phase detector an area of the record with prerecorded single frequency data (clocks only) may be used. Missing clocks can be detected logically by detecting the occurrence of 2 or more separated data pulses in the absence



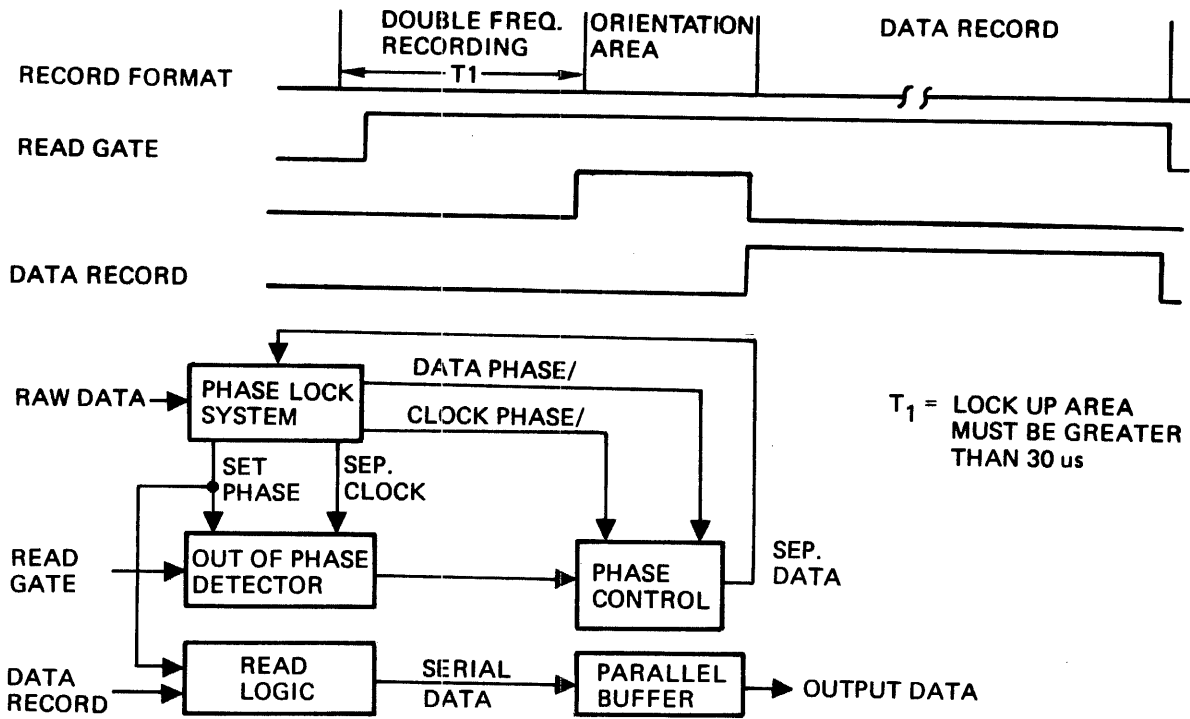
(Applies to 3 piggy-back Century Data boards only.)

Figure 4-5. Decoder Timing

of separated clock pulses. If this condition occurs the phase control flip-flop may be toggled to the opposite phase or alternately one input clock to the phase control may be inhibited. In order to provide timing signals for orientating the phase control two signals, clock phase prime and data phase prime are provided. Once the phase detector has been orientated the separated data output indicates the presence or absence of data during a bit cell time.

Figure 4-6 indicates one possible approach. The orientation information is assumed to be single frequency data (clocks only).

Orientation of the phase control flip-flop is necessary as the decoder logic requires that a data pulse occur when VFO/2 is true to be output as separated data. If the VFO/2 and data signals are  $180^\circ$  out of phase then data will be output on the separated clock line. An out of phase condition can occur whenever the phase lock system is enabled to track raw data. This condition arises from the fact that during lock up the phase lock system cannot distinguish between clock and data pulses in the incoming raw data signal. Figure 4-7 shows an out of phase condition and one method of phasing the phase control flip-flop.



(Applies to 3 piggy-back Century Data boards only.)

Figure 4-6. Implement the Phase Detector Into a System

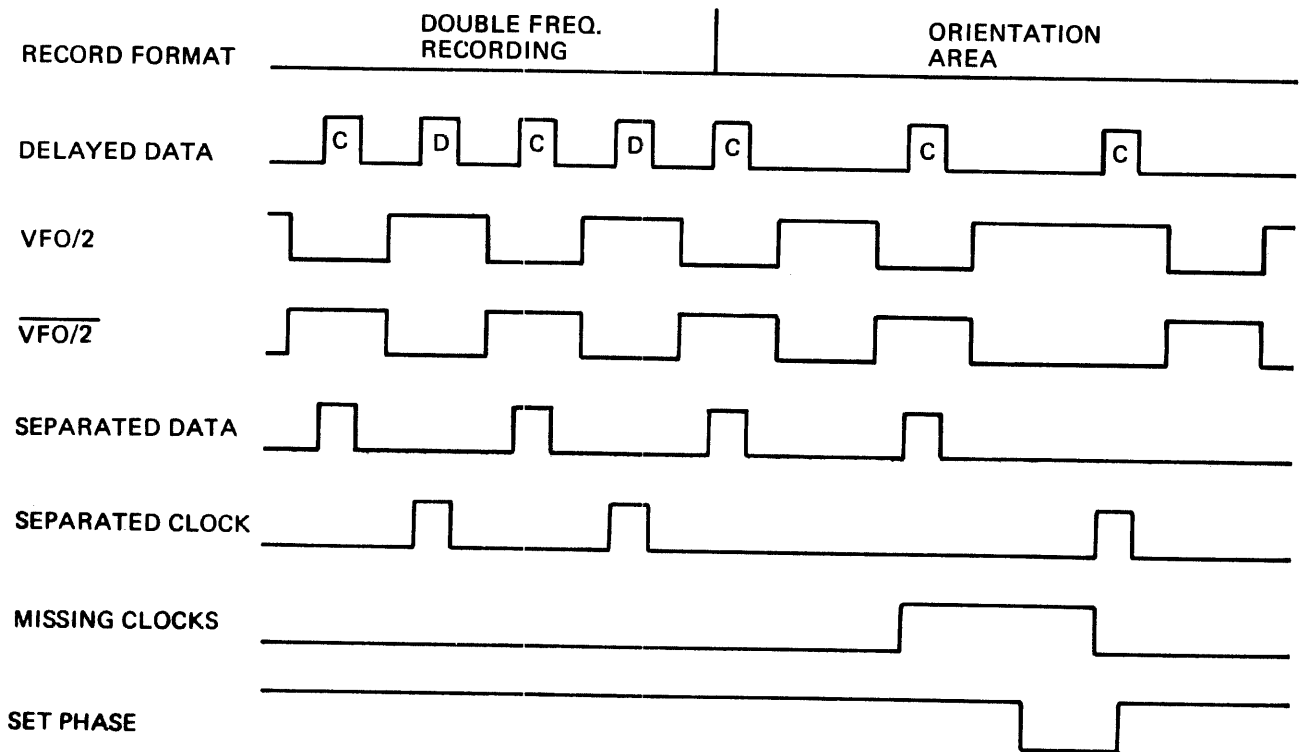


Figure 4-7. Out of Phase Condition Resulting from Tracking Raw Data

(Applies to 3 piggy-back Century Data boards only.)

Phase Lock Adjustment Procedure (Refer to figure 4-3). (Applies to 3 piggy-back Century Data boards only.)

a. Phase Demodulator

1. Ground pins 10 and 22 and adjust R23 until the VFO signal at pin 26 is 5 mHz.
2. Remove ground from pin 10 and adjust R17 until the VFO signal at pin 26 is 5 mHz.
3. Remove ground from pin 22.

b. Pulse Shaper

1. Apply an external 5 mHz square wave signal at pin 14.
2. Jumper pin 24 to pin 50.
3. View delayed data at pin 40 and VFO/2 at pin 35 of the decoder.
4. If delayed data is not positioned in the center of the VFO/2 signal, move the delay line jumper until delayed data is centered within the VFO/2 waveform.

c. Data Decoder

1. View the window strobe at pin 27 and the VFO/2 signal at pin 38 with the external 5 mHz signal applied to pin 14 of the Pulse Shaper.
2. Adjust R14 for a positive going window pulse width of 200 ns minus the pulse width of the delayed data pulse at pin 40.
3. Adjust R4 until the positive going window is centered with respect to the VFO/2 signal.
4. Remove the externally applied 5 mHz signal.

#### 4.4 THEORY OF OPERATION

Timing and flow charts for the model 1343 disk controller are presented in this section. Refer to figure 4-8 for a block diagram of the disk controller. The information in this section applies to both the GA 18/30 and the SPC-16. The bits associated with the 18/30 are always discussed or come before those associated with the SPC-16.

##### 4.4.1 CONTROL AND SEQUENCING

The control and sequencing circuits accept signals from both the processor (via the CIT interface) and the disk storage unit and produce the necessary control signals to perform data transfers between the processor and the disk storage unit.

The five commands associated with the model 1343 disk are:

- Initiate Write
- Initiate Read
- Control
- Sense Device
- Sense Interrupt



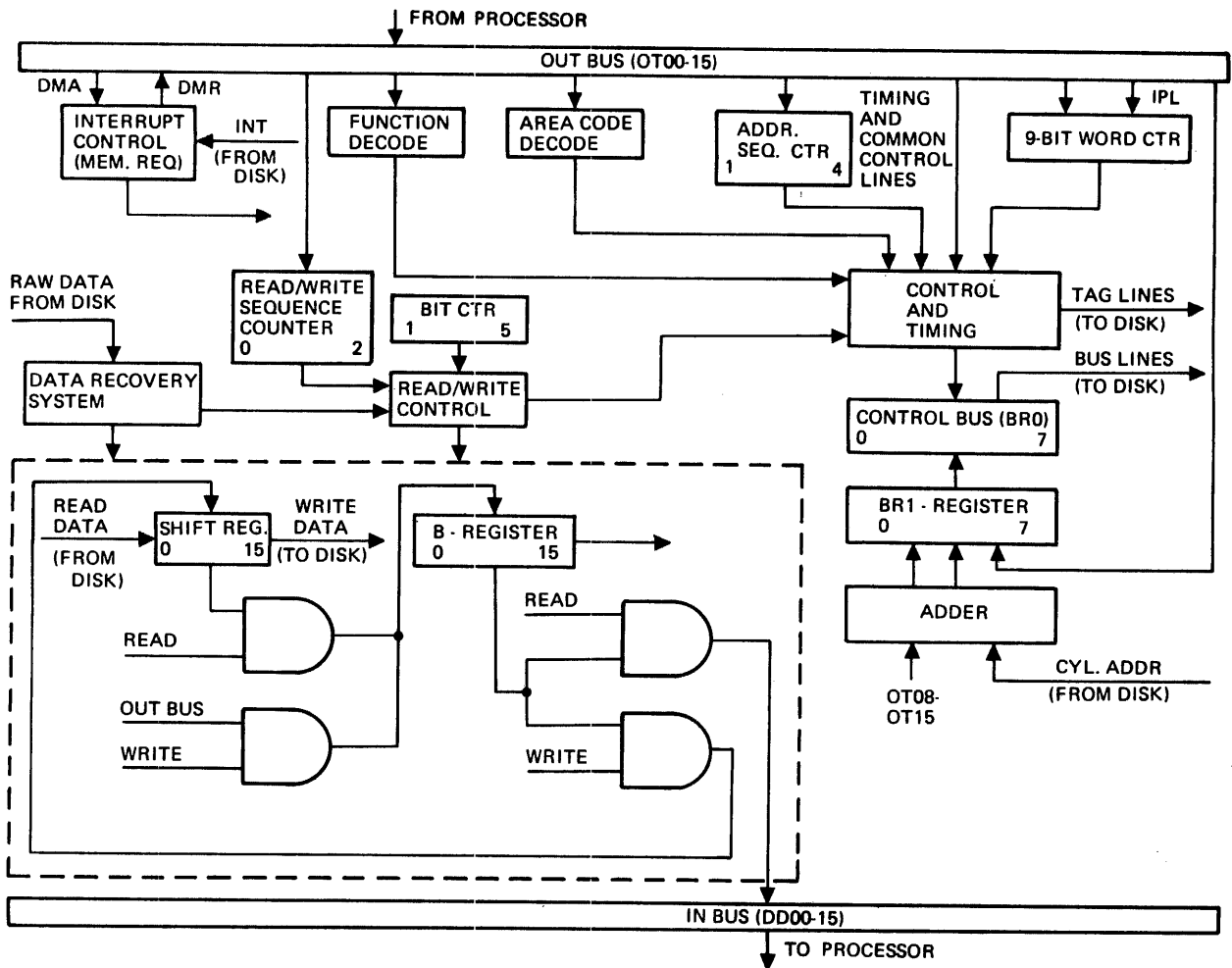


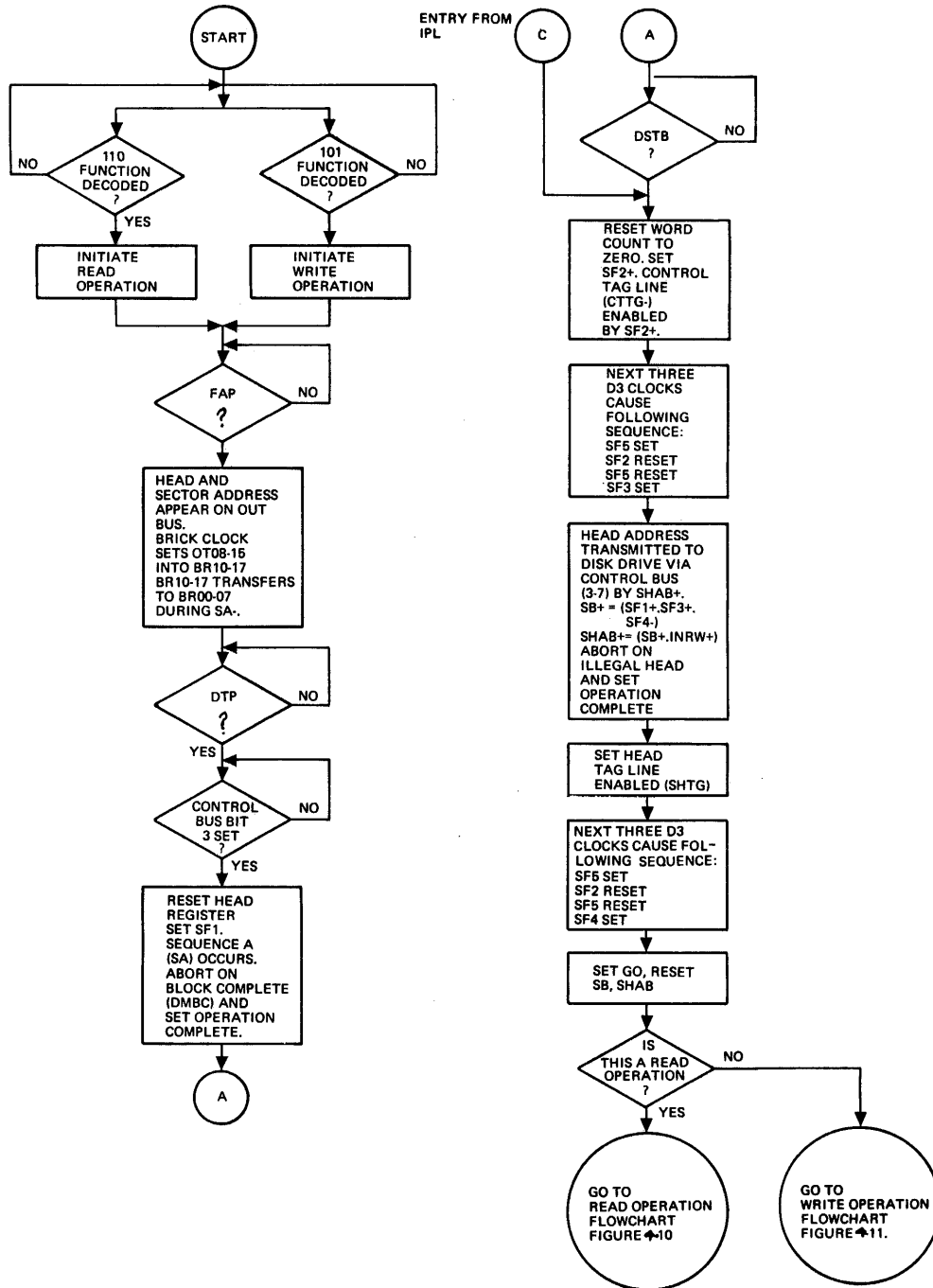
Figure 4-8. Disk Controller Block Diagram

Initiate Read/Initiate Write: Refer to figure 4-9 for a flowchart of that portion common to both the Initiate Read and the Initiate Write command. The signals needed to generate the control functions are also shown at approximately the correct time. If the operation being performed is a read operation, go to the read operation flowchart, figure 4-10. Go to the write operation flowchart, figure 4-11 if the operation being performed is a write operation.

Note that CMPR- is required in both operations so that the operation does not start in the middle of the sector.

The command initiation timing for an Initiate Read or Initiate Write command is shown in figure 4-12.

The timing associated with the Initiate Read and Read Check command is presented in figure 4-13. Figure 4-14 contains the timing associated with the Initiate Write command.



**Figure 4-9. Initiate Read/Initiate Write**

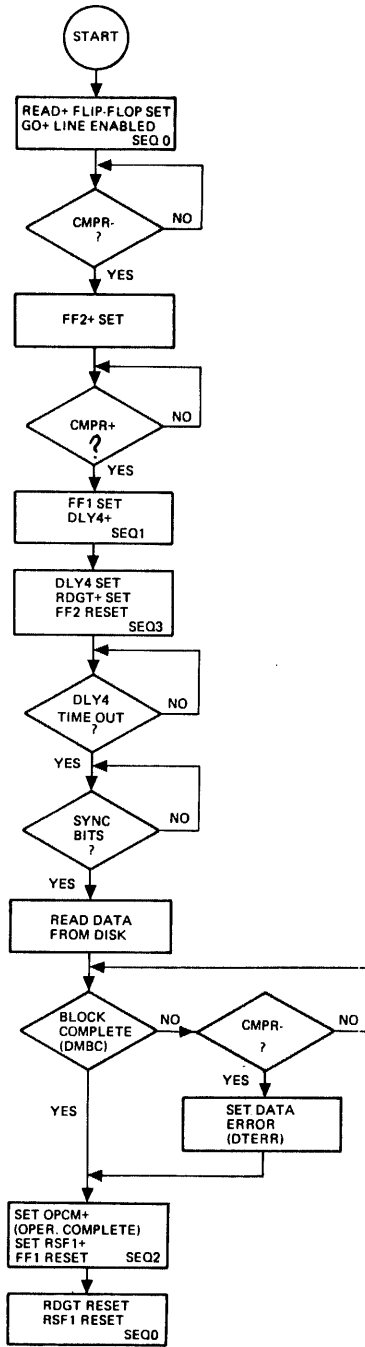


Figure 4-10. Read Operational Flowchart

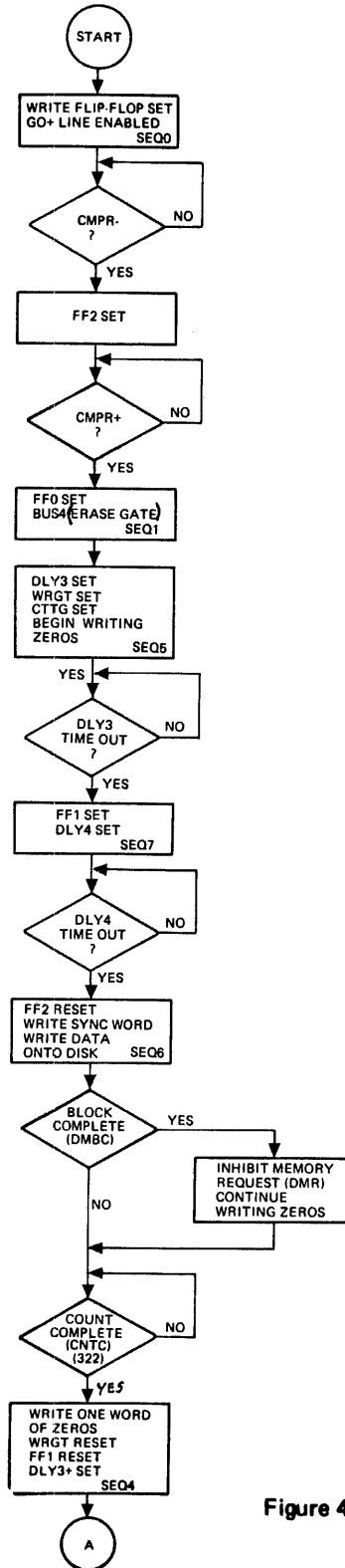
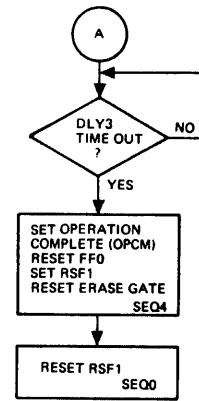


Figure 4-11. Write Operation Flowchart



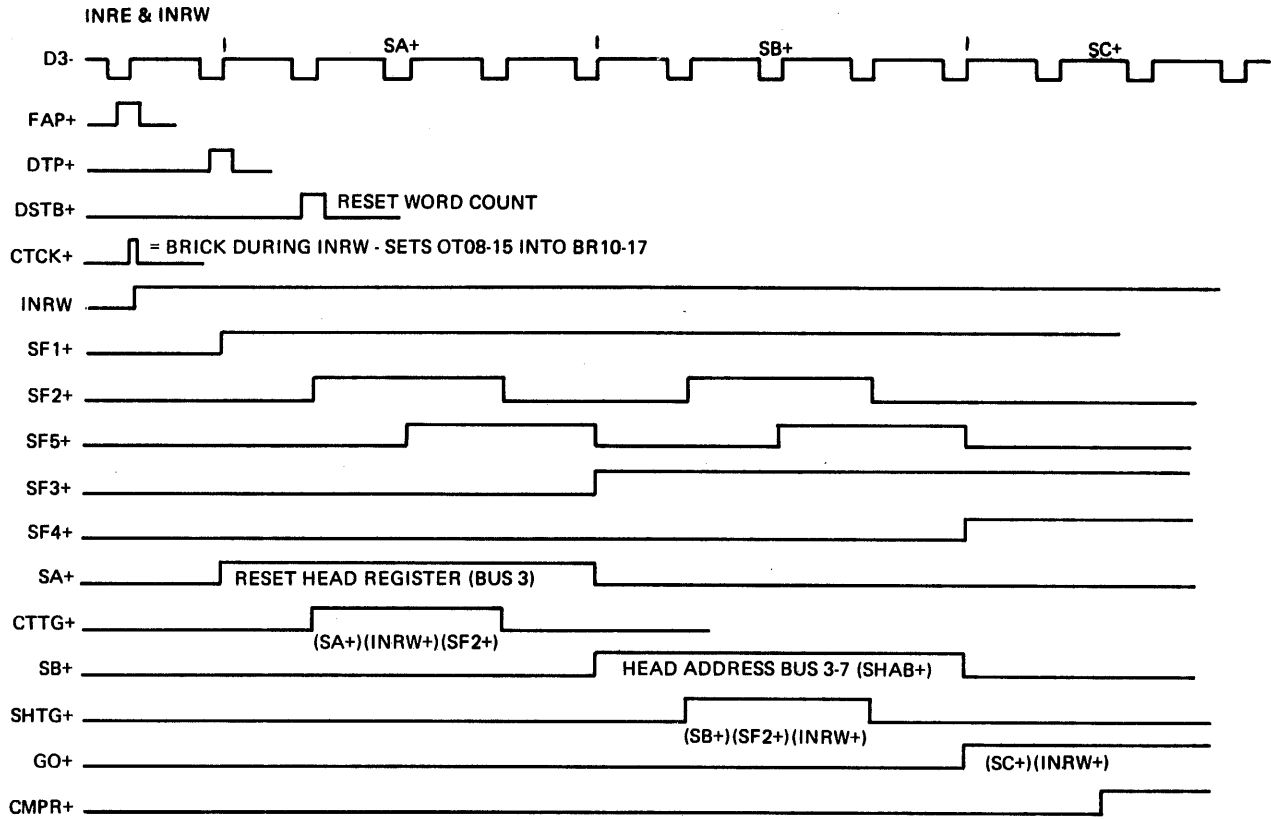


Figure 4-12. Initiate Read/Initiate Write Command Initiation Timing

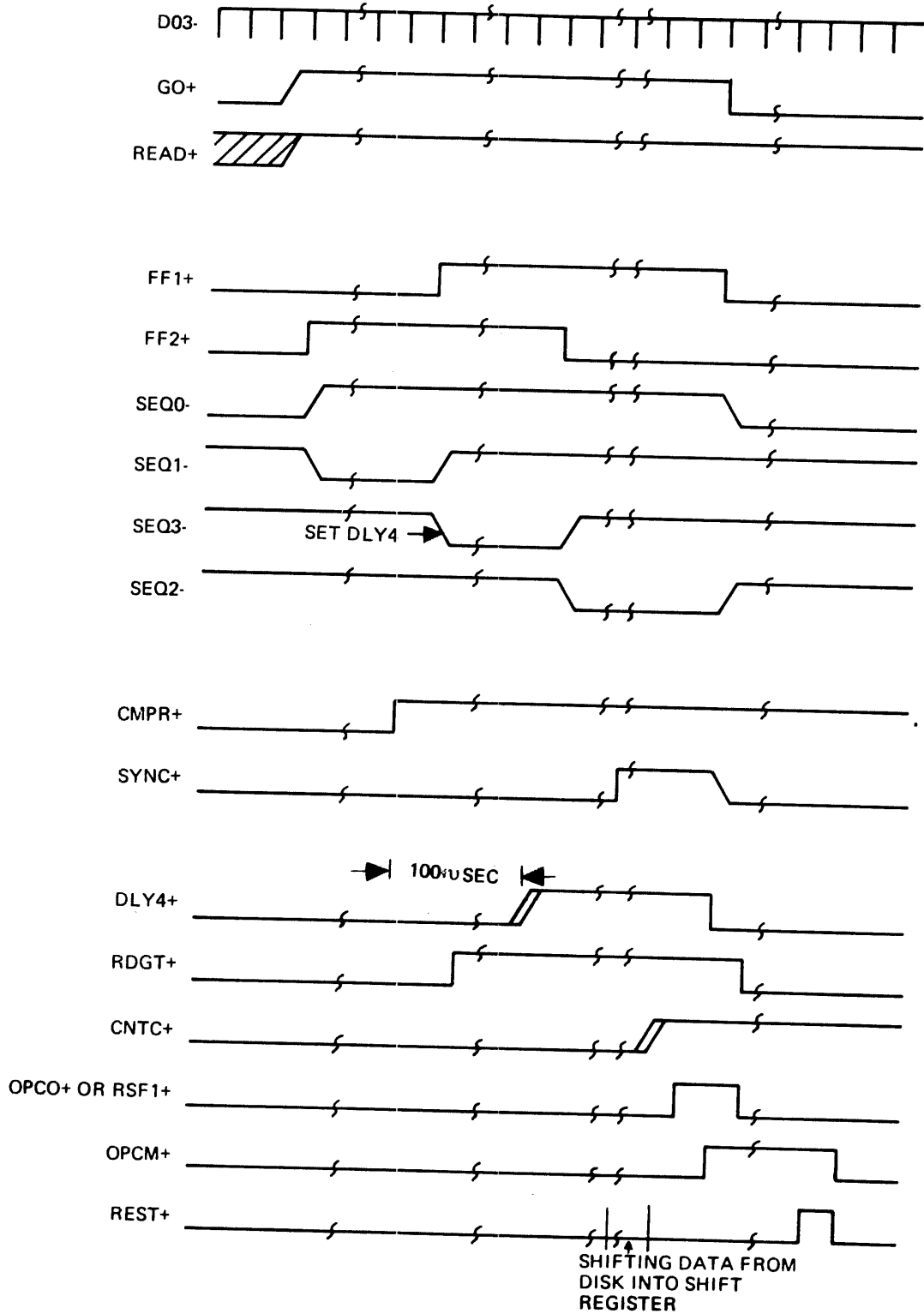


Figure 4-13. Initiate Read/Read Check Command Timing

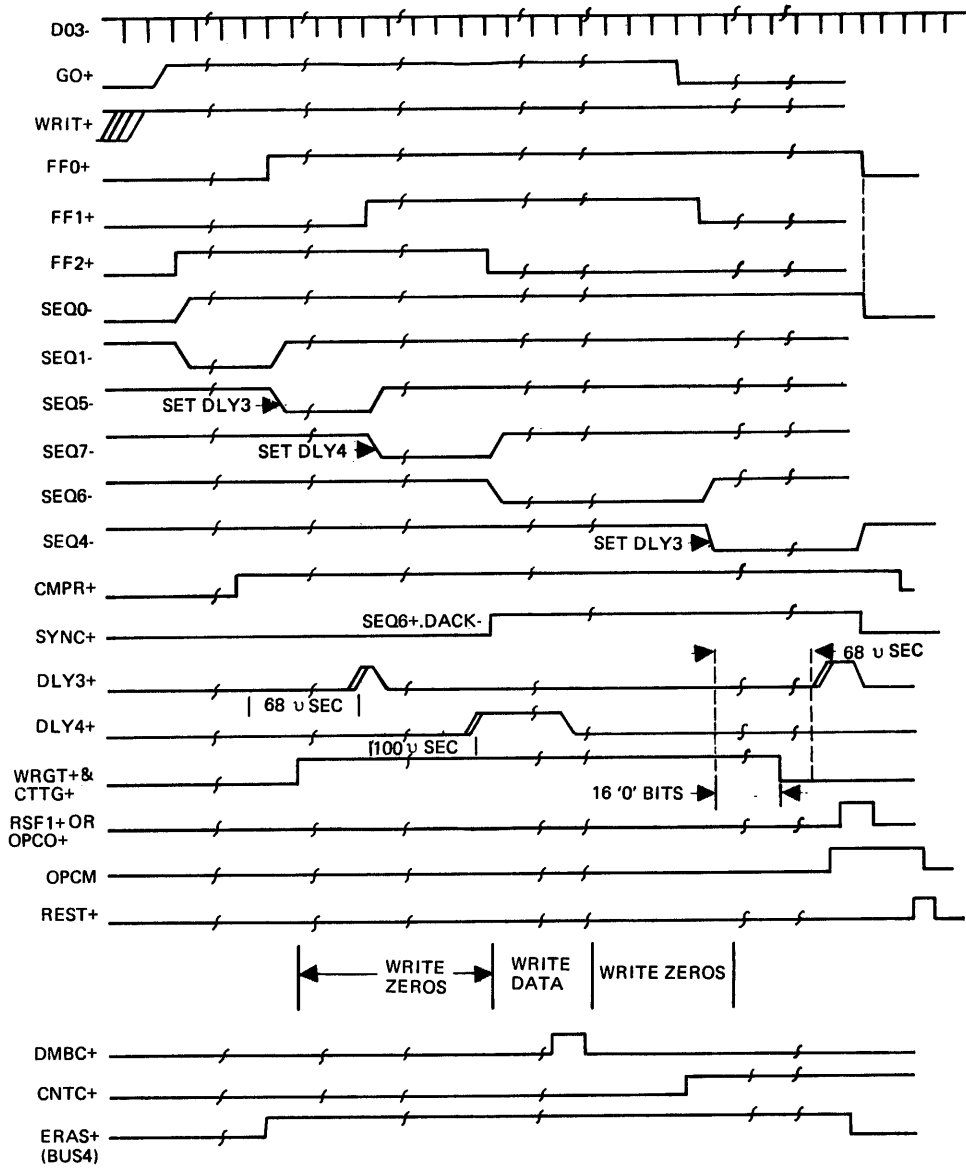


Figure 4-14. Initiate Write Operation Timing



Control: Refer to the control command flowchart, figure 4-15. The decode of bits 8 and 15 (o, 7) determine the operation to be performed. If the controller is busy when this command is received, the command is ignored. The flowchart of the restore and seek operation is shown in figure 4-15 and 4-16. The timing diagram associated with the control command is shown in figure 4-17.

Initiate Program Load: The flowchart associated with the initiate program load (IPL) operation is shown in figure 4-18. The timing diagram of this operation is shown in figure 4-19.

#### 4.4.2 STATUS GATES

Sense Device Command: The status gates are used to gate the disk controller or disk storage unit status into the processor in response to a sense device signal (SEND+). Refer to the sense device command flowchart, figure 4-20. Also refer to the sense device timing diagram, figure 2-3.

The status condition of the various bits are gated onto the in bus by SENS+. The device status word is then transmitted to the processor accumulator via the CIT interface. In the 18/30 if bit 15 of the IOCC2 is set to a ONE, bit 1 is reset. In the SPC-16, if bit zero of the first object word is set to a ONE, bit 1 is reset.

In the 18/30, bit zero is set to a ONE if any of bits 5, 7, 9, 10 and 11 is reset when all of the individual indicators are reset. In the SPC-16, bit 15 is set to a ONE if any of bits 5, 6 and 8 is reset when all the individual indicators are reset.

In the 18/30, bit one is set to a ONE upon completion of an Initiate Read or Initiate Write operation to indicate operation complete. This bit is reset by the Sense Device command with IOCC2 bit 15 equal to ONE directed to the storage unit indicating an operation complete status. In the SPC-16, bit 14 is set to a one upon completion of an Initiate Read or Initiate Write operation to indicate operation complete. This bit is reset by the Sense Device command with bit zero of the first object word equal to ONE directed to the storage unit.

Bit two (13) is set to a ONE when the storage unit is not properly sequenced up, or an unsafe condition exists in the storage unit, or the storage unit is busy performing a Seek, Initiate Read or Initiate Write operation.

Bit three (12) is set to a ONE during the time the storage unit is performing a Seek, Initiate Read or Initiate Write operation.

Bit four (11) is unused and will be zero.

Storage Protect Error (Initiate Read): Bit five is set to a ONE if an attempt is made to write data from disk into a protected area of core memory. This applies to the 18/30 only. Bit 10 is not used in the SPC-16.

Bit six (9) is unused and will be zero.

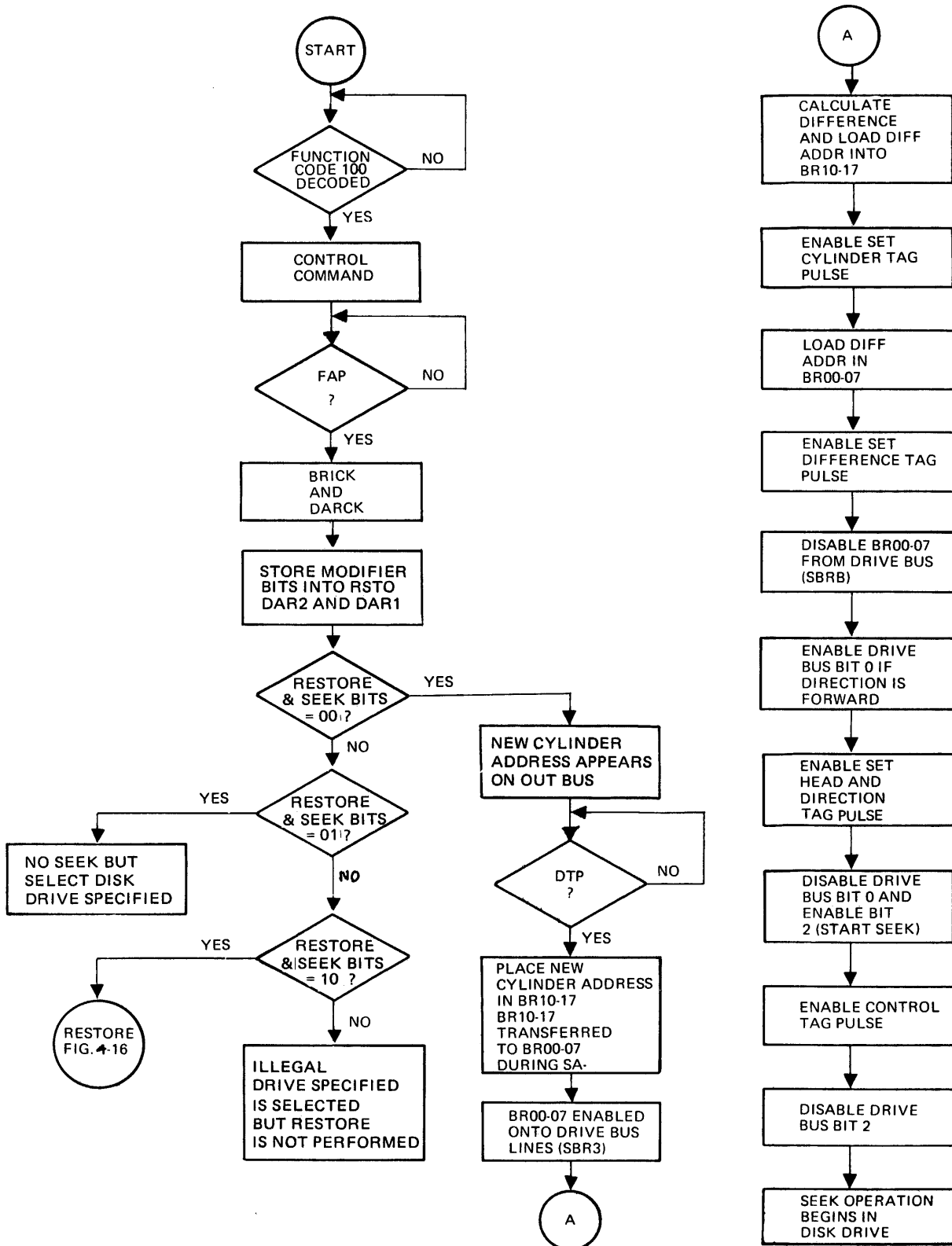


Figure 4-15. Control Command Flowchart



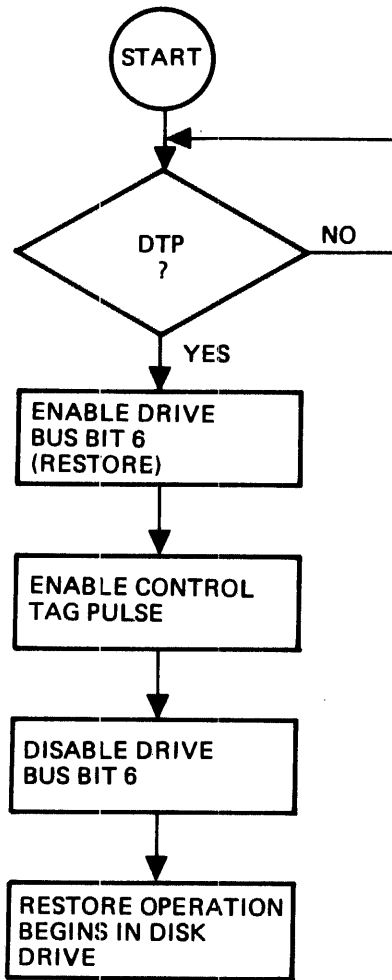


Figure 4-16. Restore Operation Flowchart

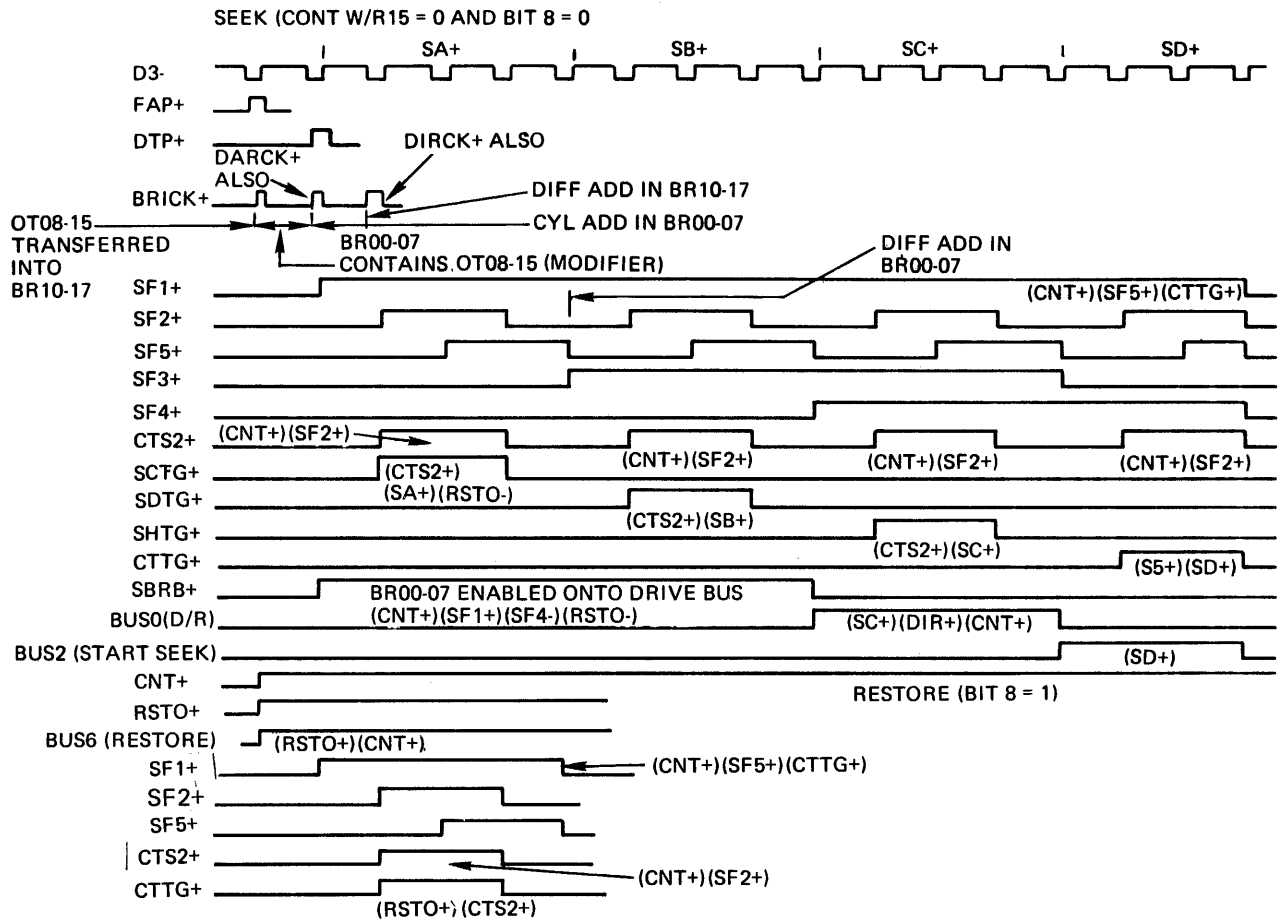


Figure 4-17. Control Command Timing

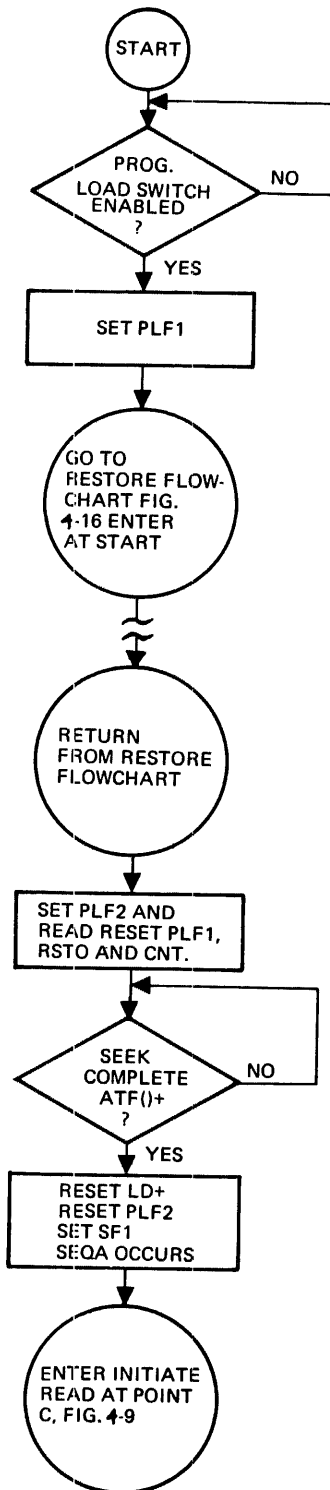


Figure 4-18. IPL Operation Flowchart

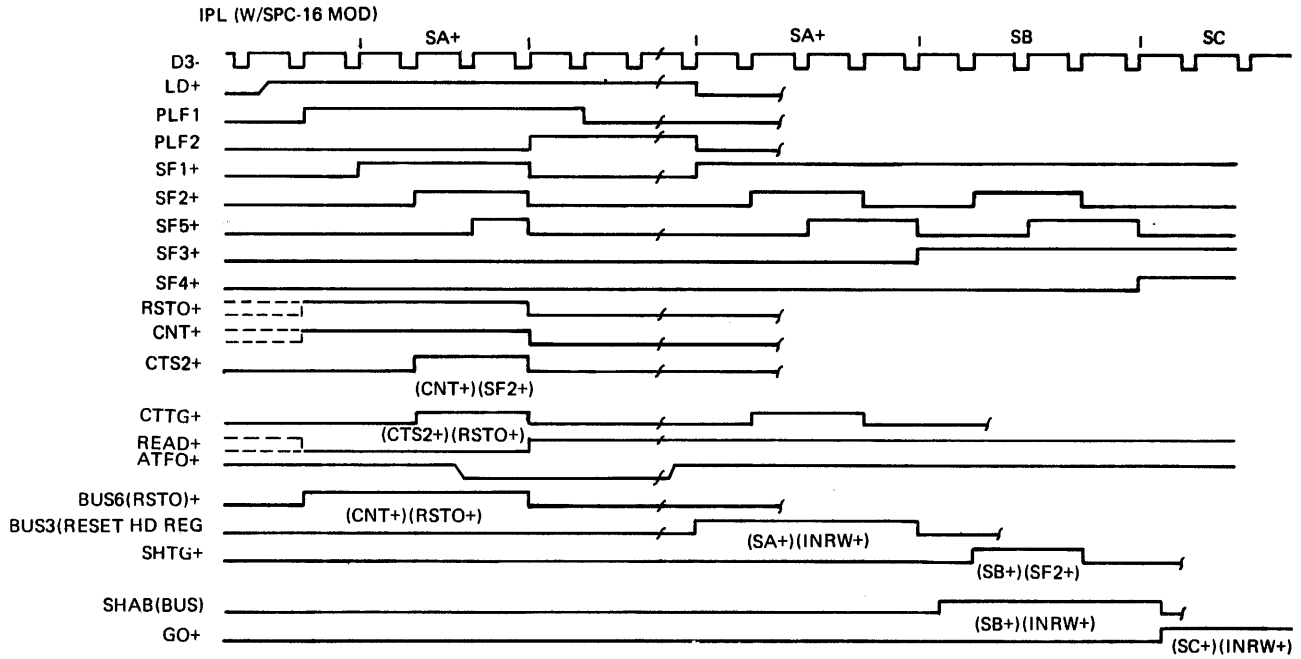


Figure 4-19. IPL Operation Timing

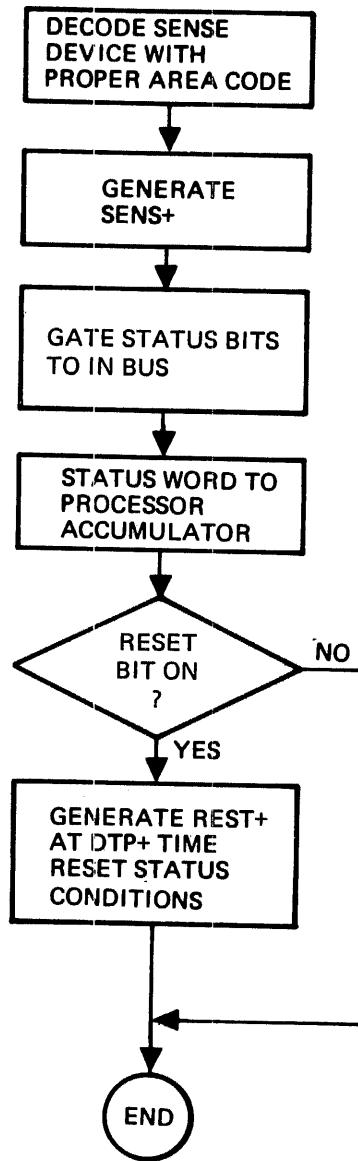


Figure 4-20. Sense Device Command Flowchart

Bit seven (8) is set to a ONE if a MOD 4 data check error is detected during execution of an Initiate Read (SCW bit 0 equals 0 or 1), or if the end of sector is detected before the specified number of words have been transferred during an Initiate Read (SCW bit 0 equals 1), or it may be set to a ONE if a word count greater than 322 is specified during an Initiate Write. Data error due to end of sector also sets the operation complete status and causes a read/write operation complete interrupt.

Bit eight (7) is unused and will be zero.

Bit nine (6) is set to ONE if a request to the processing system's memory is not honored in time, resulting in an erroneous or incomplete record written in core or on the disk.

Bit ten (5) is set to a ONE if a cylinder address greater than 202 is attempted, or if a seek is directed to a storage unit that is busy executing a previously specified seek, or if the storage unit senses a maladjustment but is still able to position properly. These conditions also cause an operation complete status and a seek complete interrupt. This bit is also set to a ONE if a seek operation has not progressed to completion within 180 milliseconds, or if the storage unit detects a condition in its access mechanism which prevents it from positioning properly. These conditions within the storage unit may cause the unit to go off line and require manual intervention, in which case there is no operation complete status or interrupt. This bit is reset by successful execution of a seek operation.

Bit eleven (4) is set to a ONE to indicate an end of cylinder condition.

Bit twelve (3) is unused and will be zero.

Bits 13, 14 and 15 (0, 1, 2) depict the current status of the sector counter. These bits are updated as the disk rotates. Since the sector actually read or written is the one following the period of active compare, the bits will indicate the next sector which can be accessed.

#### 4.4.3 INTERRUPT LOGIC

An operation complete condition causes the controller to send an interrupt request, INT(-), to the processor on the designated interrupt level. The processor responds with a SENI command requesting the interrupt level status word (ILSW). The request is presented to the controller as SIN(+) which is ANDed with the operation complete condition to establish the associated ILSW bits. If the operation complete condition is true, interrupt status bit DD01 is true. This signal is then sent to the processor to indicate the interrupt condition.

#### 4.4.4 WRITE DATA AND READ DATA

Figure 4-21 shows the timing for the Write Data (WRD) and Read Data (RDTA) signals. Note that the double frequency write data (WCX) signal is generated by gating alternate OSC- pulses as clocks and using the write data signal (WRD+) to provide an additional pulse between clocks as data '1' bits. The diagram shows the pattern for data of 1, 0, 1, 0, 0, 0, 0 during a write operation. Read Data (RDTA) is generated from the separated data (SDAT+) and separated clock (SCLK+) signals provided by the phase lock system. SDAT+ provided a dc set signal to the data flip-flop which is reset by the following data clock DACK-.

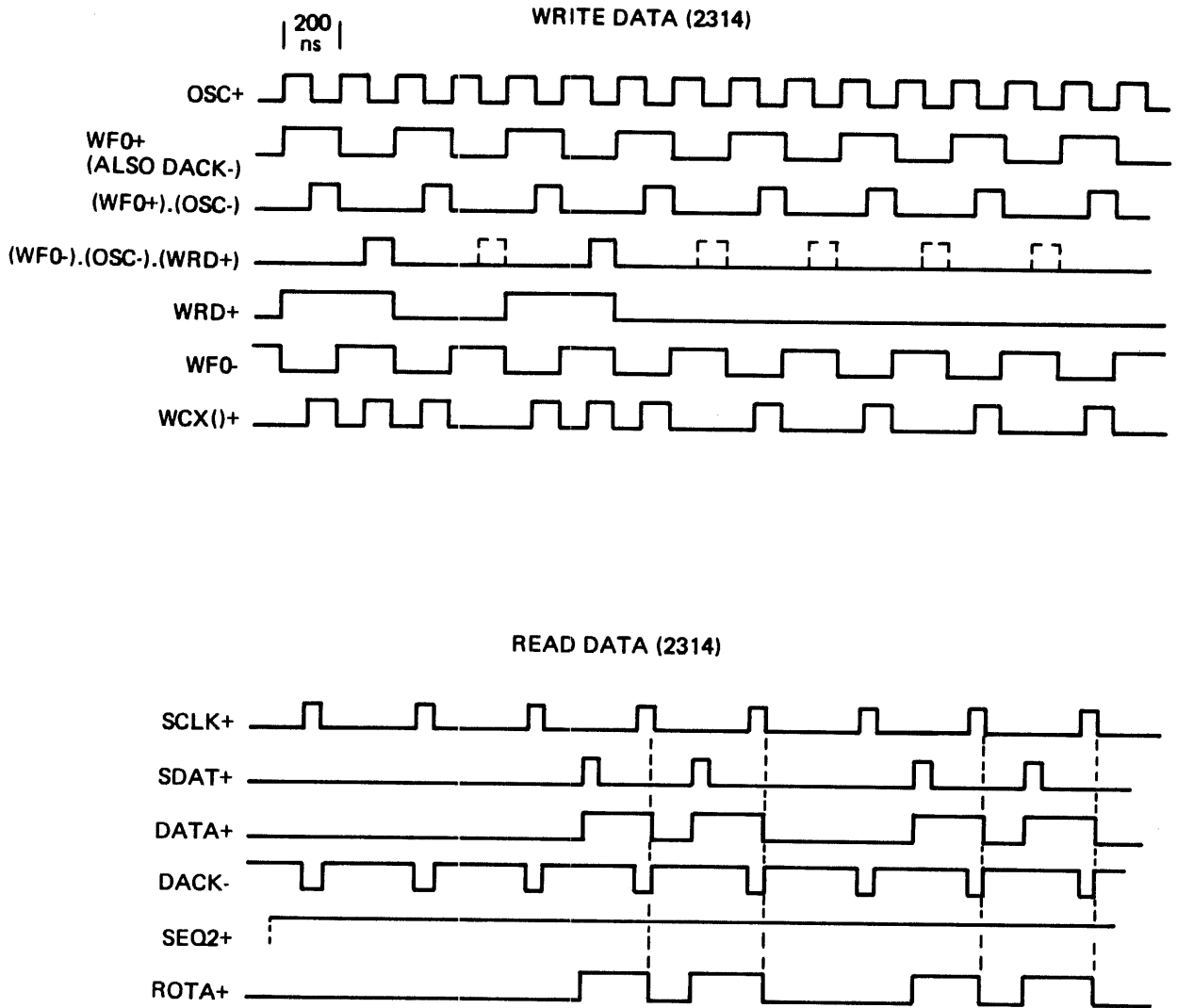


Figure 4-21. Write Data and Read Data



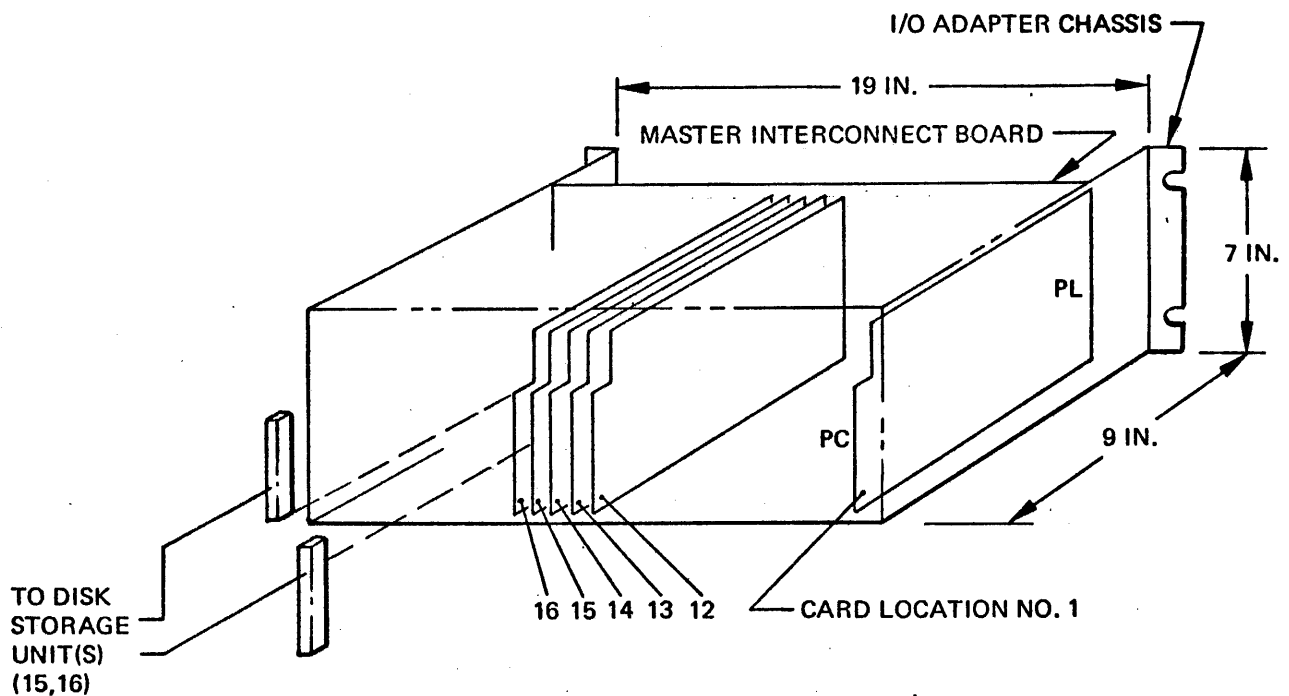
### APPENDIX A INSTALLATION

#### GENERAL

Installation of the model 1343 disk controller is normally done at the factory. The following information is given for planning purposes.

#### PREINSTALLATION REQUIREMENTS

Once the basic computer system is installed, additional input/output (I/O) adapter hardware may be required to complete the disk drive capability. Figure A-1 shows a typical controller installation. Table A-1 presents I/O adapter card locations of the various controllers available.



**NOTE**  
Refer to 18/30 or SPC-16 I/O Interface Manual for Processor to I/O Adapter Connection Information.

Figure A-1. Disk Controller Installation





Table A-1. I/O Adapter Card Locations

Location	Model Number	Description
1	1310-6703	Power board (See note, page A-1)
2		
3		
4		
5	1311-6000	Card reader
6	1322-6000	Tape punch
7	1321-6000	Tape reader
8	1353-6000	Line printer
9	1353-6000	Line printer
10	1313-6000	Card punch
11	1313-6000	Card punch
12	1343-6000	Disk control
13	1343-6000	Disk DB & WC
14	1343-6000	Disk data
15	1343-6000	Disk signal
16	1343-6000	Disk DC
17	1343-6000	Disk CD board
18	1343-6000	Disk CD board
19	1343-6000	Disk CD board
20	Spare	
21	Spare	

The controller cards are installed in I/O adapter chassis card positions 12, 13, 14, 15, 16, 17, 18 and 19. The cards are aligned with the mounting guides with the component side of each card facing away from slot 1. Moderate pressure applied to each card is sufficient to insert the card into the 80-pin backplane connector of the chassis. Even pressure should be applied along the rear edge of the card during insertion to prevent damage to the card guides or connector. Cables from the disk storage unit are connected to the controller cards in card positions 15 and 16.

## GENERAL AUTOMATION USER CORRECTION REQUEST

Document Number: \_\_\_\_\_

Today's Date: \_\_\_\_\_

Document Title: \_\_\_\_\_

Page Number: \_\_\_\_\_

Describe change or correction requested:

Name and Address of Requester: \_\_\_\_\_

\_\_\_\_\_  
\_\_\_\_\_

(Leave blank below this line)

Request Examined by: \_\_\_\_\_ Date: \_\_\_\_\_

Accepted ( ) Rejected ( )

If Rejected, Reason: \_\_\_\_\_

\_\_\_\_\_  
\_\_\_\_\_

**YOUR COMMENTS, PLEASE . . .**

This publication serves as a reference for systems analysts, programmers and operators of General Automation systems. Your answers to the questions on the back of this form help us produce better publications for your use.

Fold

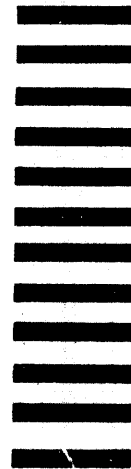
Fold

FIRST CLASS  
PERMIT NO. 423  
ANAHEIM, CALIF.

**BUSINESS REPLY MAIL**  
No Postage Necessary if Mailed in the United States

Postage Will Be Paid By . . .

General Automation, Inc.  
1055 East St.  
Anaheim, Calif. 92805



Cut Along Line

Attention: Technical Publications

Fold

Fold



General Automation, Inc.  
1055 East St.  
Anaheim, Calif. 92805

Additional Comments: