GIMIX 64K BYTE CMOS STATIC RAM BOARD W/BATTERY BACK-UP
for the SS-50/SS-50C bus

Using the latest in memory technology, the GIMIX 64K BYTE CMOS STATIC RAM BOARD combines the best features of previous memory boards on one board.

FULLY STATIC MEMORY with its inherent low soft error rate and freedom from alpha-particle induced errors. No complicated refresh timing or clocks required for data retention. Fully compatible with any of the 6800/6809 DMA techniques.

HIGH SPEED 200ns. memorys for guaranteed operation at 2MHz. with no wait states or clock stretching required.

ULTRA-LOW POWER CMOS RAM requires less than 1/4 AMP (250 Ma.) at 8V. for a fully populated 64K BYTE board. Less power supply loading and heat generation for cool, efficient operation.

NON-VOLATILE using an on-board nickel-cadmium battery. The board retains data even with system power removed. With the battery fully charged, the contents of the memory remain intact for a minimum of 21 days.

HIGH DENSITY permits greater memory expansion to meet the needs of todays sophisticated, multi-user/multi-tasking operating systems.

ADDRESSABLE in two 32K sections that have their own decoding for both the regular and extended (SS-50C) address lines. Each section can be addressed to any 32K boundary in the address range (1M BYTE with extended addressing). The 32K sections are divided into four 8K blocks that can be individually enabled or disabled. Disabled sections do not occupy any address space.

RELIABLE like all GIMIX products, the 64K BYTE CMOS STATIC RAM is designed with reliability in mind. Series damping resistors, a fully gridded power and ground layout, and generous power supply decoupling, all contribute to reliability and data integrity. An unsafe voltage detect circuit inhibits writes to the board, when the 8V. supply falls below a preset level, to prevent loss of data during the transition between system and battery power.

The GIMIX 64K BYTE STATIC RAM BOARD is ideally suited to a wide variety of applications.

Its high density and ultra-low power consumption make it possible to greatly expand systems with a few available bus slots and limited power supply capabilities.

The battery back-up feature is useful where data loss due to power failure cannot be tolerated, or as a replacement for disk or tape storage where conditions such as environment prohibit their use. Since the entire board can be hardware write protected by a switch located at the top of the board, it can also be used to emulate PROM or ROM memory. This is especially useful during firmware developement where frequent software changes must be made.

When the board is used in conjunction with a device such as the GIMIX MISSING CYCLE DETECTOR BOARD, which monitors the A.C. line and generates an interrupt when a power failure occurs, critical data can be stored and system integrity maintained during either expected or unexpected power outages.

ADDRESSING

The board is addressed as two separate 32K blocks. DIP-switches are used to select the base address of each block, the extended address (SS-50C) for each block if required, and to enable or disable 8K sections within each block.

BASE ADDRESS SELECT (S3)

The base address of each 32K block can be set to either $0000 (lower 32K) or $8000 (upper 32K). DIP-switch S3 sections 1 and 6, see figure 1, select the base address for blocks 1 and 2 respectively. A switch set ON (CLOSED) selects the lower 32K and a switch set OFF (OPEN) selects the upper 32K.

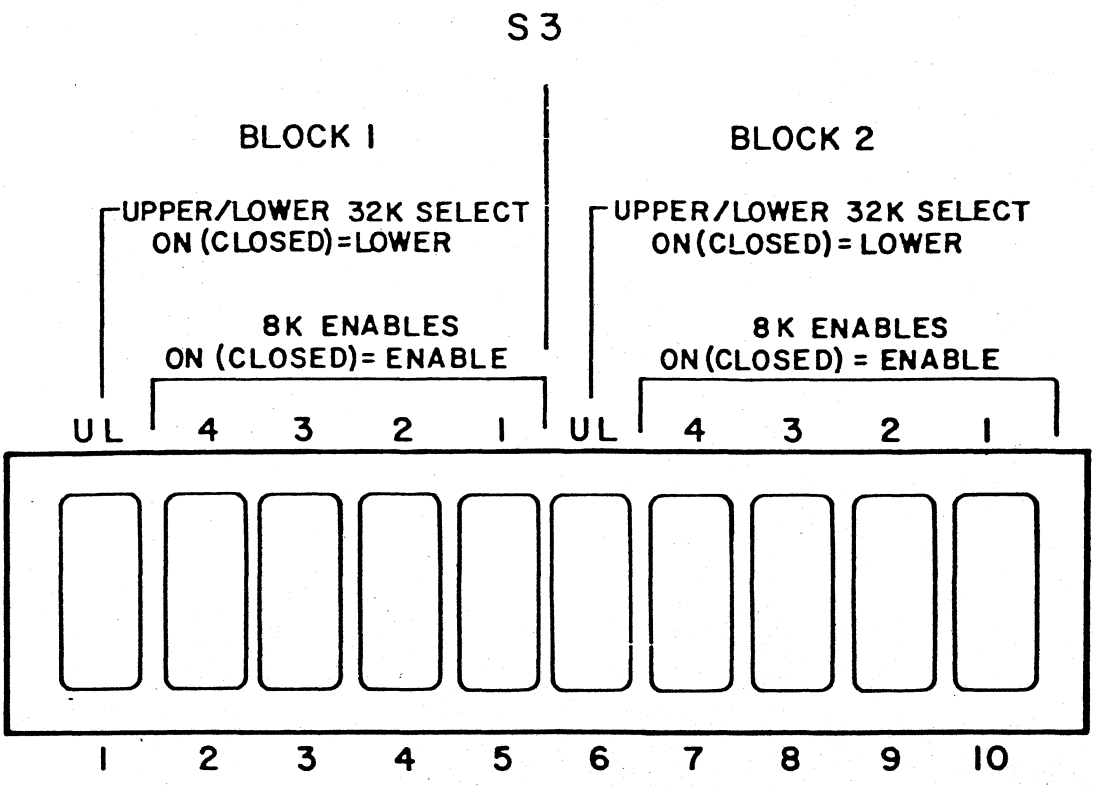
8K SECTION ENABLES (S3)

Each 32K block is divided, on even 8K boundaries, into four 8K sections. Each 8K section can be individually enabled or disabled as required. DIP-switch S3 sections 2, 3, 4, 5, 7, 8, 9, and 10, see figure 1, enable and disable 8K sections as shown in the following table.

BLOCK	SWITCH	SECTION ADDRESS UPPER 32K	LOWER 32K
1	S3-2	$E000-$FFFF	$6000-$7FFF
1	S3-3	$COOO-$DFFF	$4000-$5FFF
1	S3-4	$A000-$BFFF	$2000-$3FFF
1	S3-5	$8000-$9FFF	$0000-$1FFF
2	S3-7	$E000-$FFFF	$6000-$7FFF
2	S3-8	$COOO-$DFFF	$4000-$5FFF
2	S3-9	$A000-$BFFF	$2000-$3FFF
2	S3-10	$8000-$9FFF	$0000-$1FFF

A switch set ON (CLOSED) enables the associated 8K section.
A switch set OFF (OPEN) disables the associated 8K section.

When an 8K section is disabled, the address space that it would normally occupy is available for other boards or devices in the system. This makes it possible to leave gaps in the address space for I/O devices, disk controllers, PROM/ROM, etc. On boards that are not fully populated, 56K versions for example, the switch corresponding to the unpopulated section of the board should be OFF (OPEN). Unpopulated sections of the board will occupy address space and cause possible buffer conflicts unless they are disabled.



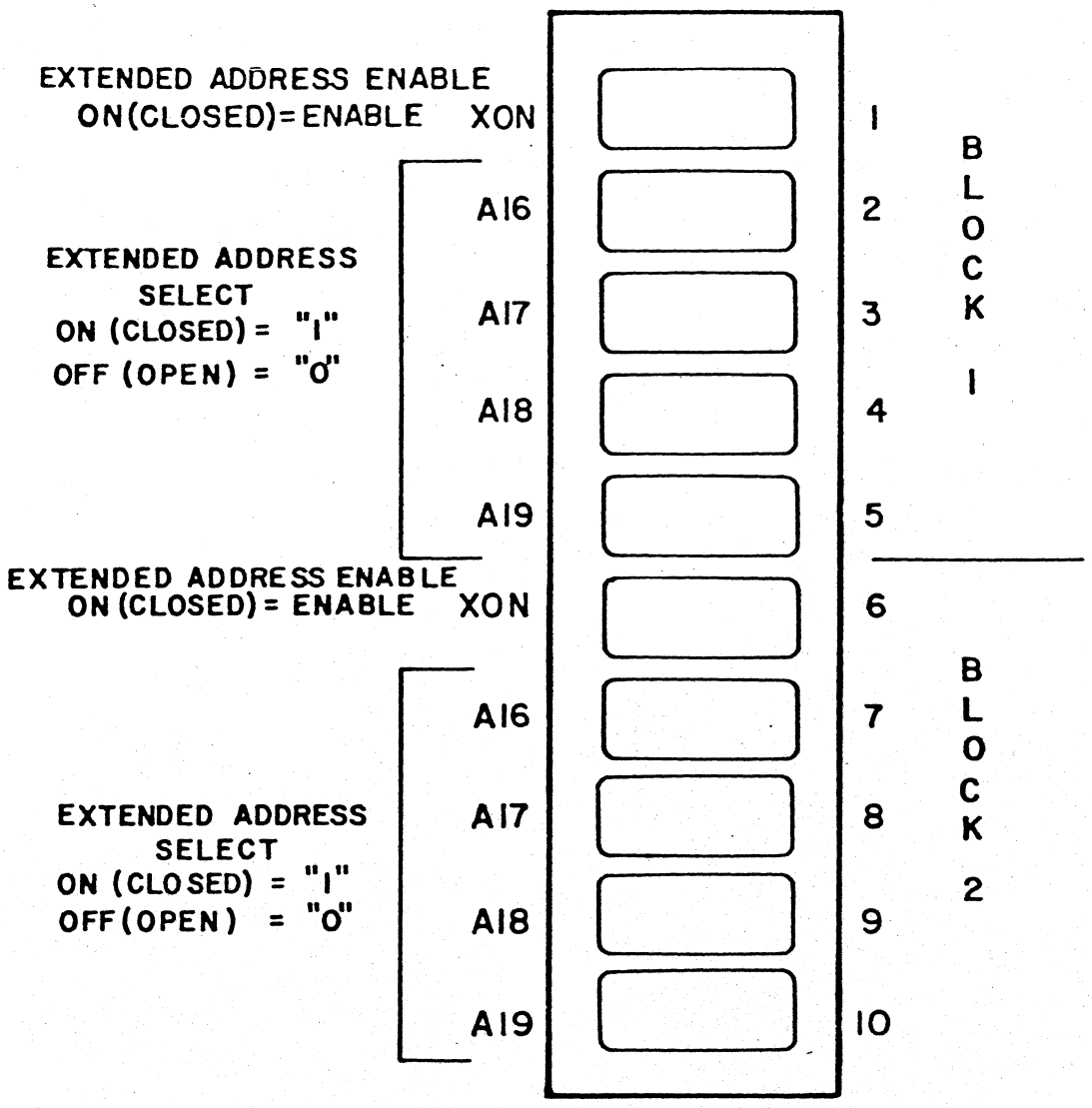
BASE ADDRESS SELECT

FIG. 1

EXTENDED ADDRESSING (S2)

Separate extended address decoding is provided for each of the two 32K blocks. The blocks can be set to the same extended address (bank), different extended addresses, or extended addressing can be disabled for one or both blocks. DIP-switch S2 sections 1 and 6, see figure 2, enable or disable extended address decoding for blocks 1 and 2 respectively. A switch set ON (CLOSED) enables extended address decoding for the associated block. A switch set OFF (OPEN) disables extended address decoding for the associated block.

DIP-switch S2 sections 2, 3, 4, and 5 correspond to extended address lines A16, A17, A18, and A19. If extended address decoding for block 1 is enabled (S2-1 = ON), these switches must be set to the binary equivalent of the desired bank address ($0 through $F). A switch set ON (CLOSED) corresponds to a "1" in that bit position. A switch set OFF (OPEN) corresponds to a "0". If extended address decoding for block 2 is enabled (S2-6 = ON), DIP-switch S2 sections 7, 8, 9, and 10 which also correspond to extended address lines A17 through A19 respectively, must be set to the desired bank address for block 2.



EXTENDED ADDRESS SELECT
FIG. 2

ADDRESSING EXAMPLES

Figures 3 and 4 show illustrate two possible address configurations.

Figure 3 shows the proper switch settings for 56K of contiguous memory from $0000 to $DFFF, with extended addressing disabled. Note that switch S3 section 7, which disables the upper 8K section of block 2, must be OFF (OPEN), even if no memory chips are installed This is the normal configuration for a 56K system using FLEX™ or OS-9™ level 1.

Figure 4 shows the proper switch settings for addressing the board as two 32K blocks, both addressed from $0000 to $7FFF, on two separate banks, 0 and 1.

ADDRESSING EXAMPLES

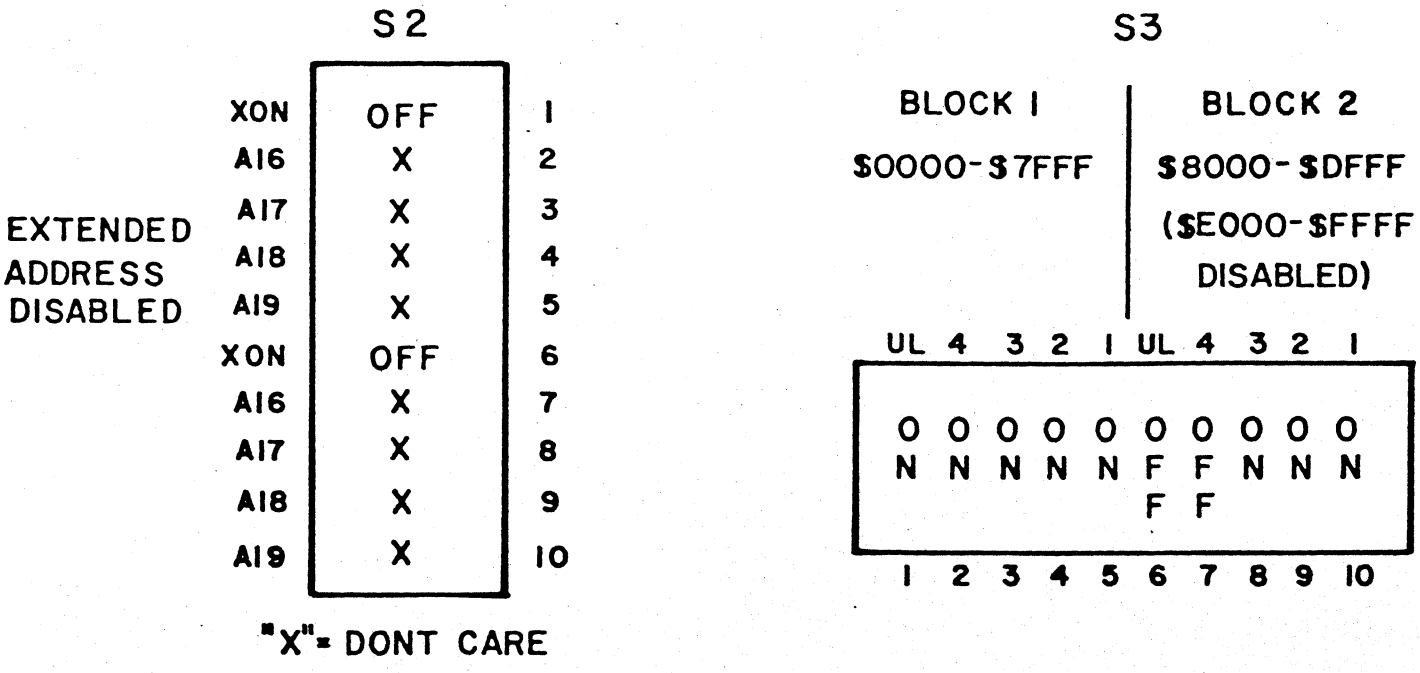


FIG.3: 56K CONTIGUOUS MEMORY $0000-$DFFF NO EXT. ADD.

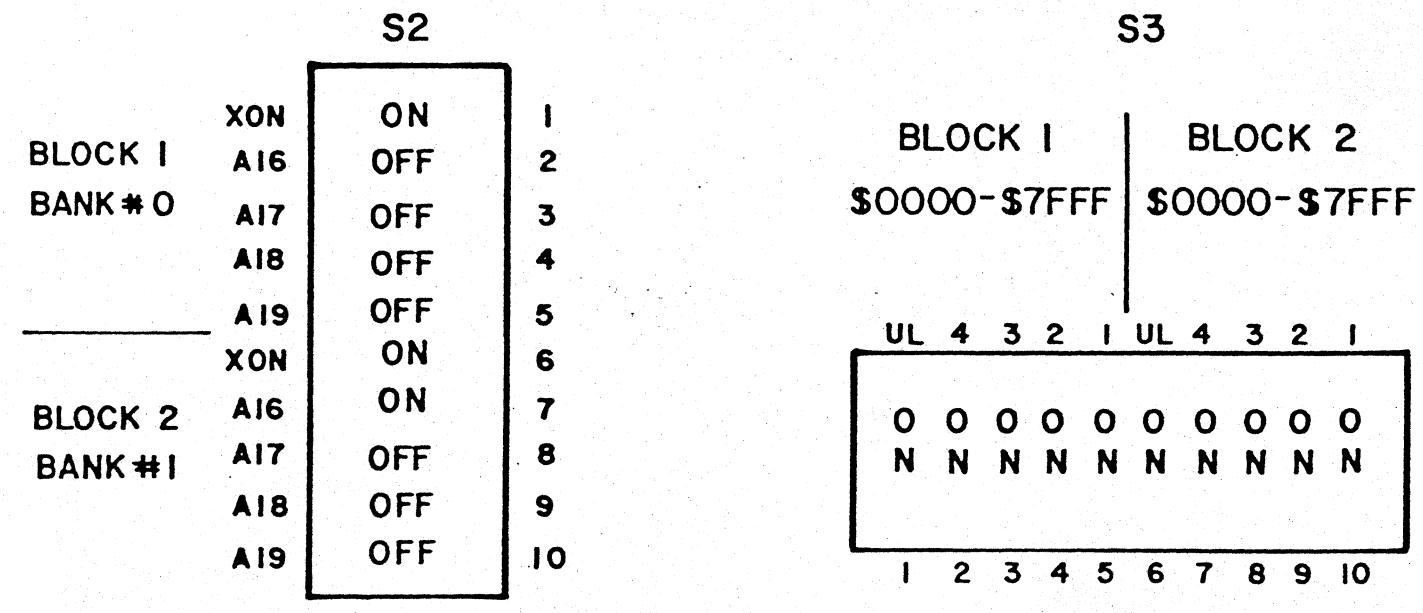


FIG. 4: TWO SEPARATE 32K BANKS $0000-$7FFF BANKS 0 & 1

WRITE PROTECT

WRITE PROTECT SWITCH (S1)

The write protect switch (S1), located at the upper right corner of the board, disables the write circuitry and prevents the system from writing data to the memory. When the switch is moved to the left position (toward the memory array) the board is write enabled and data can be written to as well as read from the memory. When S1 is moved to the the right, the board is write protected and data cannot be written to the memory.

BATTERY BACK-UP

The on-board Nickel-cadmium battery provides the power required to retain data in the CMOS memorys when system power is removed. Data remains intact for a minimum of 21 days with a fully charged battery. The battery is trickle charged whenever system power is applied to the board and the battery ON/OFF jumper is in the ON position. The transition between system and battery power is automatic. An adjustable unsafe voltage circuit monitors the +8V bus and inhibits memory accesses whenever the bus voltage falls below a preset safe level. This prevents false writes to the memory when the system bus is in an undefined state during power-up and down.

BATTERY ON/OFF JUMPER (JA-2)

JA-2 provides a means for disconnecting the battery when battery operation is not desired or when parts are removed from or installed in the board. Figure 5 shows the proper positions of the jumpers for battery ON and OFF.

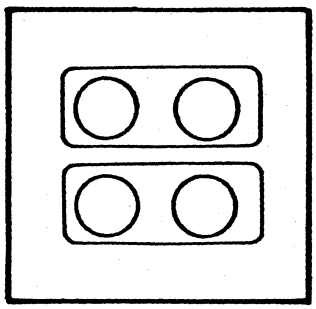
> CAUTION: When the battery ON/OFF jumper (JA-2) is in the ON position, power is applied to the memory array and the CMOS decoders at all times, even when the board is removed from the system. Before removing or installing parts at these locations the battery ON/OFF jumper must be placed in the OFF position to prevent possible damage to the parts. Use caution when handling the board to prevent shorting the battery terminals together or to other parts of the circuit or damage to the battery or the board may occur.

VOLTAGE THRESHOLD ADJUSTMENT (R2)

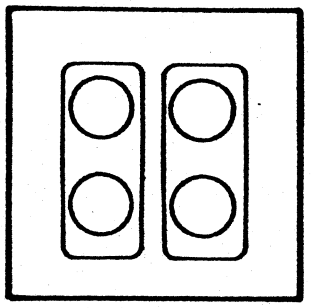
The voltage at which the unsafe voltage detector activates is determined by the setting of trimmer resistor R2. This adjustment is factory set at a voltage just above the point where the on-board voltage regulator falls out of regulation, approximately 7 volts, and should not need readjustment under normal circumstances.

> NOTE: In certain SS-50 systems with marginal power supplies, the bus voltage may be too low to allow proper operation of the board. These systems will require modifications to their power supplies to provide sufficient voltage. The nominal +8V bus voltage should be somewhat above the setting of the unsafe voltage threshold to provide for normal voltage fluctuations.

JA-2

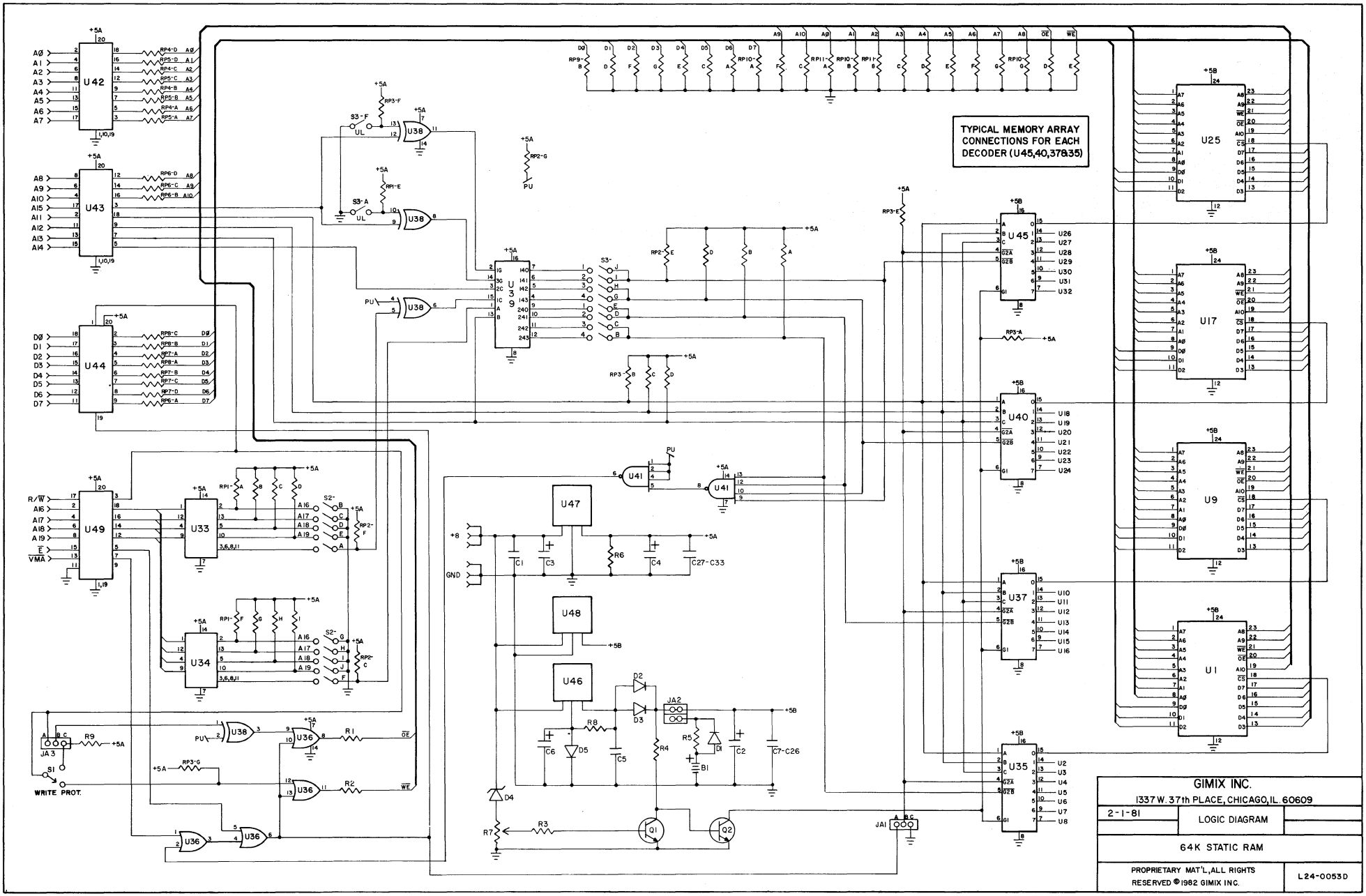


BATTERY ON



BATTERY OFF

FIG. 5


TYPICAL MEMORY ARRAY CONNECTIONS FOR EACH DECODER (U45,40,37835)
GIMIX INC.
1337 W. 37th PLACE, CHICAGO, IL. 60609
2-1-81
LOGIC DIAGRAM
64K STATIC RAM
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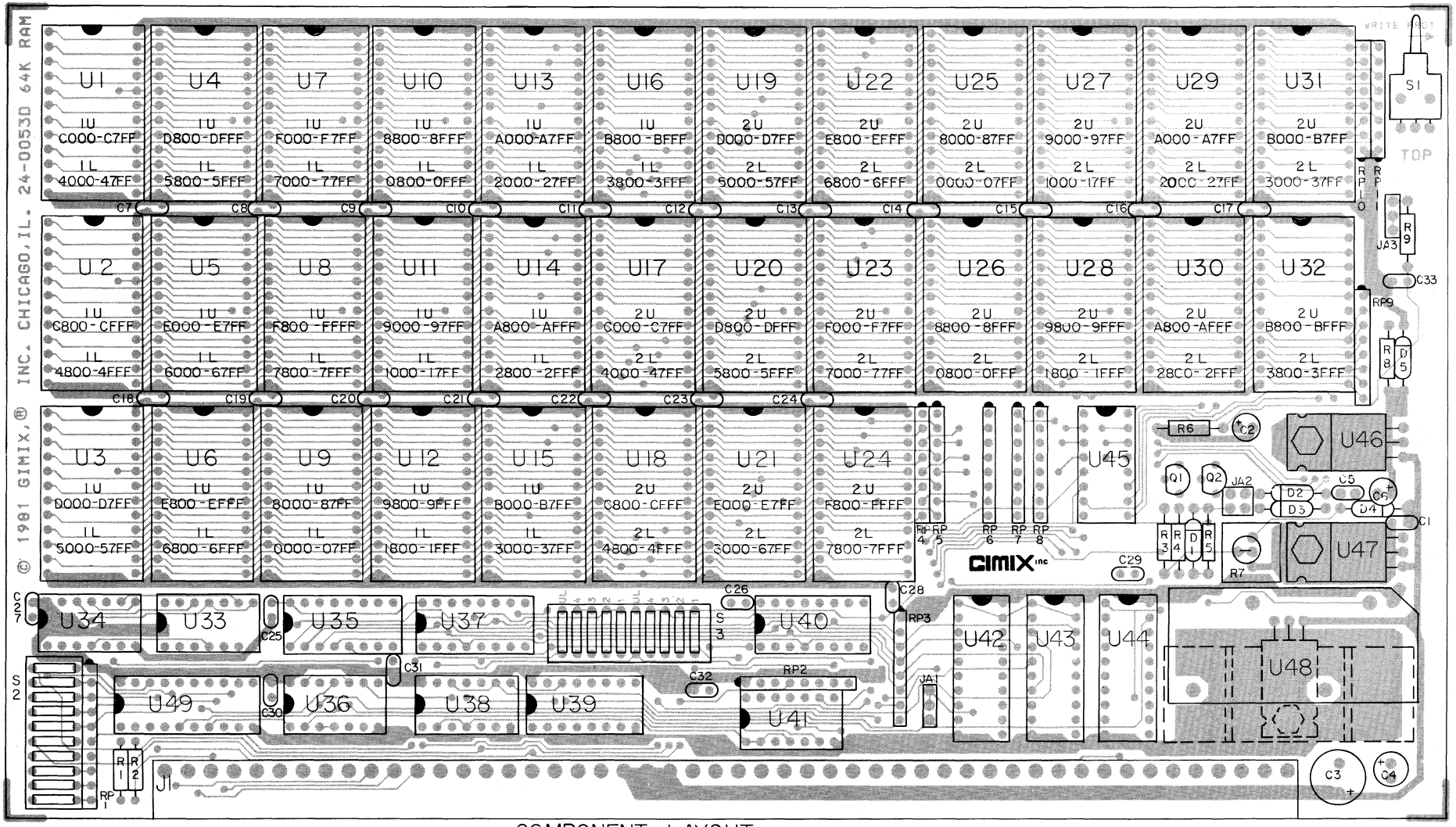
L24-0053D
WRITE PROT.



COMPONENT LAYOUT

IF S3-1 IS OFF, USE ADDRESSES LABLED 1U
IF S3-1 IS ON, USE ADDRESSES LABLED 1L

IF S3-6 IS OFF, USE ADDRESSES LABLED 2U
IF S3-6 IS ON, USE ADDRESSES LABLED 2L