HEWLETT hp PACKARD

MANUAL OF DIAGNOSTICS

DIAGNOSTIC PROGRAM PROCEDURES

HP 2100 MEMORY PROTECT TEST

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HP 2100 MEMORY PROTECT TEST

This diagnostic test program confirms proper operation of Memory Protect for the Hewlett-Packard 2100 computer.

The program is designed for maximum testing speed. The operator may repeat each function test within the diagnostic as often as desired; or he may run the entire program, stopping at the end of each function test to evaluate the results.

HARDWARE CONFIGURATION

The Memory Protect Test may be used only in the HP 2100 Computer. The diagnostic requires a teleprinter for I/O instruction testing and for reporting errors and messages to the operator.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

Memory Protect Test software requires an SIO Teleprinter Driver which should be configured prior to operation. All program options (suppress printout, suppress halts, etc.) are entered by the switch register, as shown in Table MP-1.

If any errors occur, the program types a message and halts with a MEMORY DATA error code displayed. Exceptions to this are trap cell halts $1060xx_8$ (located in low memory 2_8 - 77_8) and a special halt 107000_8. (Trap cell halts are irrecoverable and are beyond the scope of this diagnostic.) If the special halt occurs, press RUN and the error will be printed on the teleprinter.

The diagnostic checks the memory protect feature which interrupts a string of chained indirect jumps (after the second level). However, the memory protect feature will not interrupt a series of jump indirect instructions.

For example, this program:

```
LABEL JMP ABC,I
ABC   DEF BCDE
BCDE  JMP CDE,I
CDE   DEF LABEL
```

loops endlessly without interrupting. The same holds true for the JSB instruction.

This diagnostic does not test the PRL feature of memory protect. This feature must be checked by some other method.

PROGRAM ORGANIZATION

The diagnostic program consists of the routines described below:

BI/O — Tests the ability to set and clear the flags and control bits, and the interrupt operation of the teleprinter. This section contains the PRESET test for the teleprinter.

MPIO — Tests the memory protect I/O instructions, the A- and B-registers, the PRESET switches, memory protect interrupting but failing to protect memory, and indirect addressing through protected areas.

CIJI — Tests the suppress interrupt function for two levels of chained indirect JMP and JSB instructions and then interrupts the sequence during the third level.

FR — Tests memory protection turn-on and then indirectly jumps from below the fence to one instruction above the fence for all of memory above 400_8. Tests for legal and illegal interrupts when executing violation and non-violation instructions on both side of the fence for all memory above 400_8. At the same time the violation register is checked for all memory above 400_8.

NVI — Tests all non-violation instructions.

VI — Tests all violation instructions including the halt instruction that is specially coded (107000_8).

OPERATING INSTRUCTIONS

a. Configure the SIO teleprinter driver and load the diagnostic program using the Basic Binary Loader.

b. Load address 000100_8.

c. Set switch register bits 0-5 to the select code of the teleprinter I/O channel.

d. Select desired options from Table MP-1 by setting the appropriate bits of the switch register.

e. Press RUN.

f. When the program advances to the PRESET test, a message is printed and the computer halts. The operator must press both PRESET switches, then press RUN. The program then advances to the second PRESET test. The program prints a message then loops until operator presses HALT, INTERNAL PRESET, and RUN. The loop is timed to last for about 15 seconds regardless of when the buttons are pushed, before proceeding to the next test.

g. During execution of the function tests, the program again halts and prints self-explanatory messages on the teleprinter. Both of the PRESET tests are omitted if the automatic option (bit 15 of switch register set) is selected. After the program has advanced through all the tests, a message indicates completion of the diagnostic program. If the automatic option was selected, the completion message is omitted.

MESSAGE ANALYSIS

All messages to the operator typed on the teleprinter are prefixed by an alpha-numeric code. An H prefix indicates an operating instruction while an E prefix indicates an error message.

All halts are coded and may be found in Table MP-2 opposite the appropriate MEMORY DATA value.

If errors occur in test FR, the teleprinter should be allowed to print many of the errors (the fence register increments). This will be helpful in diagnosing the error.

Table MP-1

Program Options -- Switch Register Settings

SWITCH REGISTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Descriptions
0-5	Select code for the teleprinter I/O channel.
6-10	Spares
11	Set on to omit error halts.
12	Set on to run, then halt after each separate test within the diagnostic (with the appropriate messages typed on the teleprinter). This allows the operator to continue on to the next test or repeat the last test by setting bit 14.
13	Set on to suppress all messages on the teleprinter (except end-of-diagnostic messages).
14	Set on to recycle the current test instead of advancing to the next test within the diagnostic.
15	Set on to recycle the entire program (omitting both PRESET tests). Or, set off to execute all tests and halt with the appropriate message on the teleprinter at the end of the diagnostic.

Table MP-2

Diagnostic Messages

MEMORY DATA	ROUTINE	MESSAGE	COMMENTS
102001	BI/O	E1.CLF DID NOT CLEAR FLAG OR SFS CAUSED SKIP WITH FLAG CLEAR	Test the ability to clear the teleprinter flag and test the SFS instruction.
102002	BI/O	E2.SFC DID NOT SKIP WITH FLAG CLEAR	Test the ability of the SFC instruction.
102003	BI/O	E3.STF DID NOT SET FLAG, OR SFC CAUSED SKIP WITH FLAG SET	Test the ability to set the teleprinter flag and test the SFC instruction.
102004	BI/O	E4.SFS DID NOT SKIP WITH FLAG SET	Test the SFS instruction.
102005	BI/O	E5.DID NOT INTERRUPT	Test the teleprinter interrupt capability.
102006	BI/O	E6.THE RETURN ADDRESS IS NOT CORRECT	Test the return address that was placed in the teleprinter trap cell.
102007	BI/O	H7.PRESS INTERNAL AND EXTERNAL PRESET, THEN PRESS RUN	
102010	BI/O	E1Ø.EXTERNAL PRESET DID NOT SET THE FLAG	The test failed.
102011	BI/O	H11.END BI/O.	Select program options and press RUN.
102012	MPIO	E12.A AND B REGISTER TEST FAILED WHEN INSTRUCTION *xxxxxx* WAS EXECUTED AT MEMORY LOCATION *xxxxxx*. FENCE REGISTER WAS SET TO *xxxxxx*	Test if MP allows use of the A- and B Registers.

Table MP-2 (cont.)

Diagnostic Messages

MEMORY DATA	ROUTINE	MESSAGE	COMMENTS
(No halt)	MPIO	H13.PRESS HALT, THEN PRESS INTERNAL PRESET, THEN PRESS RUN IN LESS THAN 15 SECONDS	Test the ability for PRESET.
102014	MPIO	E14.INTERNAL PRESET DID NOT TURN OFF MEMORY PROTECT.	Test failed.
102016	MPIO	E16.ERROR: PHASE ONE OF INSTRUCTION FOLLOWING A JSB,I MP VIOLATION WAS EXECUTED.	Test failed.
102017	MPIO	E17.NO MEMORY PROTECT INTERRUPT OCCURED DURING THE INDIRECT JUMP INTERRUPT GATE TEST	Proceed with test and consult schematic.
102020	MPIO	E2Ø.INDIRECT ADDRESSING THROUGH PROTECTED AREA FAILED.	Test failed.
102021	MPIO	E21.I/O TRAP CELL INSTRUCTION ERROR	Test failed.
102022	MPIO	E22.NON I/O TRAP CELL INSTRUCTION ERROR	Test failed.
102024	MPIO	H24.END MPIO	Select program options and press RUN.
102025	CIJI	E25.NO INTERRUPT AFTER SECOND LEVEL OF JMP INDIRECT CHAIN	Test failed.
102026	CIJI	E26.INCORRECT RETURN ADDRESS FOR CHAINED INDIRECT JMP INTERRUPTS.	Test failed.

Table MP-2 (cont.)

Diagnostic Messages

MEMORY DATA	ROUTINE	MESSAGE	COMMENTS
102027	CIJI	E27.NO INTERRUPT AFTER THIRD LEVEL OF JSB INDIRECT CHAIN	Test failed.
102030	CIJI	E3Ø.INCORRECT RETURN ADDRESS FOR CHAINED INDIRECT JSB INTERRUPTS.	Test failed.
102031	CIJI	H31.END CIJI	Select program options and press RUN.
102032	FR	E32.ILLEGAL INTERRUPT. FENCE REGISTER IS *xxxxxx*, VIOLATION REGISTER IS *xxxxxx* AND INSTRUCTION IS *xxxxxx*	Allow many printouts of this message.
102033	FR	E33.NO INTERRUPT. FENCE REGISTER IS *xxxxxx*	Failure occurred in FR test. Repeat test.
102034	FR	E34.VIOLATION REGISTER INCORRECT. IS *xxxxxx* AND SHOULD BE *xxxxxx*	Failure occurred in FR test. Repeat test.
102037	FR	H37.END FR	Select programs options and press RUN.
102040	NVI	E4Ø.INTERRUPT OCCURRED WHILE EXECUTING LEGAL INSTRUCTION *xxxxxx*. FENCE REGISTER IS *xxxxxx* AND VIOLATION REGISTER IS *xxxxxx*	Test failed.
102047	NVI	H47.END NVI.	Select program options and press RUN.

Table MP-2 (cont.)

Diagnostic Messages

MEMORY DATA	ROUTINE	MESSAGE	COMMENTS
102050	VI	E5Ø.NO MEMORY PROTECT INTERRUPT AFTER EXECUTING INSTRUCTION *xxxxxx* AT LOCATION *xxxxxx* AND FENCE AT *xxxxxx*	Test failed.
102051	VI	E51.NO MEMORY PROTECT INTERRUPT AFTER EXECUTING EAU INSTRUCTION *xxxxxx* AT LOCATION *xxxxxx* AND FENCE AT *xxxxxx*	Test failed.
102053	VI	H53.END VI	Select programs options and press RUN.
102060	MPIO	E6Ø.NO INTERRUPT OCCURRED WHEN MEMORY PROTECT WAS VIOLATED	
102061	MPIO	E61.PROTECTED MEMORY WAS VIOLATED AND THE MEMORY PROTECT INTERRUPT OCCURRED AT THE SAME TIME.	
102062	MPIO	E62.NO MEMORY PROTECT INTERRUPT. STC OR OTA INSTRUCTIONS MAY HAVE FAILED OR MP OPTION MAY NOT BE INSTALLED	
102063	MPIO	E63.MEMORY PROTECT INTERRUPT LOCATION DOES NOT AGREE WITH VIOLATION REGISTER. LIA INSTRUCTION MAY HAVE FAILED.	
102064	MP	E64.MEMORY PROTECT LOCATION DOES NOT AGREE WITH VIOLATION REGISTER. LIB INSTRUCTION MAY HAVE FAILED	

Table MP-2 (cont.)

Diagnostic Messages

MEMORY DATA	ROUTINE	MESSAGE	COMMENTS
102065	MPIO	E65.NO MEMORY PROTECT INTERRUPT. STC OR OTB INSTRUCTIONS MAY HAVE FAILED	
102070	INITIALIZATION	E7Ø.PLEASE DISABLE THE LOADER	Failure in Initialization Program. Corrective action.
102071	VI	E71.RESET DOUBLE STORE FAILED	
102077	END	H77.MEMORY PROTECT DIAGNOSTIC HAS BEEN COMPLETED	End of test. Press RUN to recycle the diagnostic.
1060*xx*	any	(none)	Trap cell interrupt. M= memory address when interrupted, *xx*=the trap cell location.
107000	any	(none)	Press RUN for error printout.

HP 2100 EXTENDED ARITHMETIC UNIT TEST

HP Product No. HP 24214

HEWLETT PACKARD

11000 Wolfe Road
Cupertino, California 95014

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HP 2100 EXTENDED ARITHMETIC UNIT TEST

The program tests the 2100 EAU instruction set (i.e., DLD, DST, MPY, DIV, etc.) by running non-EAU subroutines and EAU instructions with the same arguments and comparing the actual results with the expected results.

HARDWARE CONFIGURATION

This program runs on an HP 2100 computer with a minimum of 4K of core. A teleprinter can optionally be included to report diagnostic messages during execution of the program; 4K of core is required if a teletype is used.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

Since the actual EAU results are compared with the expected results obtained by running the non-EAU routines, the diagnostic should be executed only after the following diagnostics have been successfully executed:

- 2100 Memory Reference Instruction Test
- 2100 Alter-Skip Instruction Test
- 2100 Shift-Rotate Instruction Test
- 2100 TTY Test (if a teleprinter is used)

If a teleprinter is used, the SIO teleprinter driver is loaded and configured first. Then the diagnostic program is loaded and optionally configured by setting the switch register as shown in Table EAU-1. The configuration process loads the hardware switch register bit settings into an internal switch register, which is read by the diagnostic during execution (if hardware switch register bit 0 is set OFF).

To modify the program options during execution, set the switch register bit 0 ON and set the other program option bits according to Table EAU-1. With switch register bit 0 set ON, the diagnostic ignores the internal switch register and reads the hardware switch register to determine program control. The program can be reconfigured at any time by starting the program at location 111_8*, setting the switch register program option bits and pressing RUN. (See Operating Instructions, step h.)

To avoid reconfiguring the driver and diagnostic before subsequent uses, load the SIO System Dump program and use it to punch a paper tape copy of the configured driver and diagnostic.

To start a run of the diagnostic after configuration is complete or after a configured tape has been loaded, set the computer to the starting address, select program options by setting the switch register as listed in Table EAU-1 and press RUN.

If an error is detected, the program prints a message on the teleprinter and/or halts with a MEMORY DATA error code displayed, depending upon the switch register settings. (See Diagnostic Messages.)

If a trap cell halt occurs, the computer displays 1060*xx* (*xx* = the trap cell location). The cause of the halt must be determined by the user; after the error is corrected, the user restarts the program from location 100_8.

LIMITATIONS

This diagnostic is a unit diagnostic. No system interaction with Direct Memory Access (DMA), Memory Protect, or Memory Parity is checked. However, the DST instruction is tested in the 2100 Memory Protect Test.

**The program can be configured starting at 2_8 only after loading and before the SIO System Dump is loaded or the program is run for the first time.*

PROGRAM ORGANIZATION

This diagnostic consists of ten sections; each tests one of the ten EAU instructions:

Test Number (octal)	Name	
1	DLD	(Double Load)
2	DST	(Double Store)
3	MPY	(Multiply)
4	DIV	(Divide)
5	ASR	(Arithmetic Long Shift Right)
6	ASL	(Arithmetic Long Shift Left)
7	LSR	(Logical Long Shift Right)
10	LSL	(Logical Long Shift Left)
11	RRR	(Rotate A and B Right)
12	RRL	(Rotate A and B Left)

The diagnostic executes the ten sections in sequence. One pass through the diagnostic is defined as 1500 loops through the ten sections. A loop is defined as execution of all ten sections with a new argument generated for each section (program option bit 6 set OFF for all ten instructions). If program option bit 6 is set ON at any time before or during any execution of the ten sections, the loop is not counted toward the 1500 which constitute a pass.

MEMORY ALLOCATION

The arguments generated before each instruction test (as long as program option bit 6 is set OFF) are located in specific areas of core. (See Figure EAU-1.)

Before each EAU instruction test (except DLD) the A- and B-Registers are loaded with the contents of RNA and RNB respectively. For DLD, RNA and RNB are expected to be in the A- and B-Registers after the instruction is executed.

Bit 0 of the contents of RNE and RNO are set into the E and OV Register, respectively, before each EAU instruction. RNM holds the multiplier for the MPY instruction and the divisor for the DIV instruction.

The expected and actual results of each instruction test are also stored in memory in fixed locations. Figure EAU-1 shows where they are stored.

To check an instruction using specific arguments (supplied by the user), the argument storage locations can be set manually through the front panel. Once the arguments have been loaded into core, the diagnostic is run with program option bit 6 set ON. For shift/rotate tests, the shift value is set in SHFT (memory location 117_8).

112	RNA	A-Register contents	working arguments before instruction is executed
113	RNB	B-Register contents	
114	RNE	E-Register contents	
115	RNM	Multiplier/divisor	
116	RNO	OV-Register contents	
117	SHFT	shift count for shift/rotate instruction	
120	IL#	# indirect addressing levels (0 = direct)	
121	EA	expected A-Register result	or expected double store result
122	EB	expected B-Register result	
123	EE	expected E-Register result	
124	EO	expected O-Register result	
125	AA	actual A-Register result	
126	AB	actual B-Register result	
127	AE	actual E-Register	
130	AO	actual O-Register result	
131	SA	actual double store results	
132	SB		

Figure EAU-1. Fixed Core Locations For Arguments And Results

The E-Register (loaded with bit 0 of RNE before the EAU instruction is executed) is not expected to change after execution of the EAU instruction and an error condition occurs if it does not remain intact.

The OV-Register (overflow) is loaded with bit 0 of RNO before execution. The OV-Register is tested after instruction execution in the same way as the E-Register, with the expected results shown in Figure EAU-2.

DST, DLD, RRR, RRL, LSR, LSL	should not change
ASR, MPY	should always be 0
DIV	Should be 0 unless a divide error occurred, then it should be 1
ASL	should be 0 unless a significant bit was shifted out, then it should be 1.

Figure EAU-2. OV-Register Expected Results

DIAGNOSTIC MESSAGES

Two kinds of messages, general and error, are typed on the system teleprinter. The general messages are typed only if program option bits 1 and 10 are set OFF. The general messages are:

Message	Description
EAU DIAGNOSTIC	An introductory message printed only at the beginning of the diagnostic.
EOT *x*	This message is printed before an "end-of-test" halt (program option bit 15 set ON). *x* is the octal test number.
END OF PASS *x*	The "end-of-pass" message is printed at the end of a diagnostic cycle where *x* is the decimal pass count.

Error messages are printed if the hardware includes a teleprinter and only if both program option bits 1 and 11 are set OFF. All error messages are prefixed with "E-*x*," where *x* is the octal number of the test where the error occurred. The prefix is followed by the mnemonic instruction name. If the instruction test is in the shift/rotate group, the octal shift count follows; if the instruction was not shift/rotate, the indirect addressing counter, IL = *x*, is indicated, where *x* is the number of indirect addressing levels.

If the register or core results fail to match the expected results, the actual contents and the expected contents are printed. Only registers that failed are printed; all others are assumed correct. For all instruction tests except DLD and DST, the original contents before execution of the B- and A-Registers are listed as part of the error message, whether the registers failed during execution or not. The E- and OV-Registers are never listed unless they failed.

For Example:

E-1 DLD IL=4 B,A = 052352 122516 SB 052352 066421 E=0 SB 1 OV=1 SB 0

Error in test 1. The instruction was DLD (indirect). The indirect addressing level was 4. The EAU hardware instruction returned B- and A-register values of 052352 122516 while B- and A-register values of 052352 066421 were expected. EAU instruction execution also returned E- register and OV-register equal to 0 and 1, respectively; the expected values were 1 and 0 respectively.

E-11 RRR 20 B,A WAS 000007 000003 B,A = 000003 000006 SB 000003 000007

Error in test 11. The instruction was RRR 20. The original B- and A-register arguments before execution of the EAU instruction were 000007 000003. The EAU hardware instruction returned B- and A-register values of 000003 000006, the expected values were 000003 000007. The expected E and OV-register values matched the actual E- and OV-register values, so they are not shown in the error message.

E-5 ASR 20 B,A WAS 154056 166602 OV=0 SB 1

Error in test 5. The instruction was ASR 20. The original arguments before execution were 154056 166602. The actual OV-register result was 0, but should be 1.

The abbreviations used in the above messages are:

Abbreviation	Meaning
A	A-Register
B	B-Register
E	If at beginning, signifies error message; otherwise, E-Register.
OV	OV-Register (overflow indicator)
M	Core memory
SB	Should be
IL	Indirect addressing level

The B-Register contents is always listed before the A-Register contents. Memory, B- and A-Register contents are listed as six octal digits. The octal shift field is two digits.

COMPUTER HALTS

If bit 14 is set OFF, the computer halts when an error occurs with the actual register results loaded into the A,B,E and OV-Registers. (For a DST instruction, A,B contain the results actually double stored.) After an error halt, check the memory locations listed in Figure EAU-1 to find the working arguments and the expected results. In this way, instruction results can be checked without a teleprinter.

Other halts and their causes are listed below in Figure EAU-3.

Memory Data	Meaning
1020*xx*	Error halts (*xx* = test #)
102076	End of test halt. A- and B-registers contain test #.
102077	End of pass halt
1060*xx*	Unexpected trap cell halt (*xx* = select code)
107000	Start of configuration halt
107077	End of configuration halt

Figure EAU 3. Computer Halts

Table EAU-1

Program Options--Switch Register Settings

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Functions
0	Set ON to use the external hardware switch register settings. Set OFF to use the internal switch register settings.
1	Set ON to indicate that no teleprinter is available. Set OFF to indicate that a teleprinter is being used.
2-5	Spares
6	Set ON to suppress the number generator at the beginning of each instruction test. Set OFF to generate new arguments for each execution of an instruction test.
7	Set ON to suppress the indirect addressing portions of the instruction tests. Set OFF to execute the indirect addressing portions of the instruction tests.
8	Set ON to repeat the current test with new arguments if bit 6 is set OFF.
9	Set ON to break out of any test which finds an error.
10	Set ON to suppress non-error messages.
11	Set ON to suppress error messages.
12	Set ON to halt the program at the end of a pass. (MEMORY DATA = 102077_8.)
13	Set ON to repeat the current test with the same arguments each time.
14	Set ON to suppress halting the program upon finding an error.
15	Set ON to halt the program at the end of a test. (MEMORY DATA = 102076_8 and A- and B-Registers contain the octal test number.)

OPERATING INSTRUCTIONS

a. If a configured version of the diagnostic tape is available, skip directly to step h.

b. Use the Basic Binary Loader to load the SIO teleprinter driver (if a teleprinter is available) and configure that driver. Then use the Basic Binary Loader to load the diagnostic.

c. Set a starting address of 2_8.

d. Press RUN. The computer halts with 107000_8 displayed.

e. Set the switch register for the desired program options according to Table EAU-1.

f. Press RUN. The computer halts with 107077_8. The internal switch register now contains the desired options.

g. If desired, use the SIO System Dump program to punch a copy of the configured diagnostic. If not, skip to step i.

h. Use the Basic Binary Loader to load the configured diagnostic tape.

i. Set a starting address of 100_8.

j. If program options other than those set in the internal switch register are to be used, set switch register bit 0 ON, then select the desired program options by setting the switch register bits according to Table EAU-1.

k. Press INTERNAL PRESET, EXTERNAL PRESET and RUN.
   1. If program option bits 1 and 10 are both set OFF, the diagnostic types a preamble message and starts the first test.
   2. To access a specific test, set program option bit 15 ON. The program halts at the end of each test with 102076_8 displayed in the DISPLAY REGISTER. The octal test number is in both the A- and B-registers. Press RUN to continue the next test. If necessary, set program option bits 11 and 14 ON to suppress error halts and error messages until the desired test is reached. When the test is reached, set program option bit 15 OFF, and set program option bit 8 ON. The test is looped with new arguments each time.

3. Normally, the program should be run with all program option bits set OFF. If an error is found, the program prints a message. If no error is found, the program cycles once every 41 sec. (approximately). If errors do occur, set the program option bits according to Table EAU-1.

1. To reconfigure the internal switch register, set starting address of 111_8 and perform steps d through g.

APPENDIX A
DIAGNOSTIC CONTROL

The following is a description of diagnostic control within the DLD, DST and ASR tests. Control for the MPY and DIV tests is similar to the DLD test. The ASR test is representative of all shift/rotate instruction tests.

DLD Test

DLD tests the "double load" instruction as follows:

a. If program option bit 6 is set OFF, the program generates new arguments. If program option bit 6 is set ON, then previously generated arguments are used.

b. The indirect addressing level counter is cleared.

c. The expected results (obtained by the non-EAU routine) are computed for later comparison.

d. The actual EAU instruction is modified to reflect the level of indirect addressing (level 0 is direct).

e. The E- and OV-Registers are loaded with bit 0 of generated arguments RNE and RNO respectively.

f. The A- and B-Registers are cleared.

g. The DLD EAU instruction is executed and the expected results compared with the actual results.

h. If no errors exist, the program continues with step i; if an error is found, DLD test performs the following:

    1. If program option bit 1 is set OFF (indicating that a teleprinter is available) and if program option bit 11 is set OFF (indicating that error messages are to be printed), then an error message is printed on the teleprinter. If either program option bit 1 or 11 is set ON, the error message is bypassed.

2. If the program option bit 14 is set ON, the program jumps to step 3. If program option bit 14 is set OFF, then the program halts. Press RUN to continue the program.

3. If program option bit 9 is set ON, the program jumps to step k. Otherwise, the program continues below.

i. If program option bit 13 is set ON, the program loops back to step e. Otherwise, it continues below.

j. If program option bit 7 is set ON, the indirect addressing tests are skipped. If program option bit 7 is set OFF, then the program increments the indirect addressing level counter. If the counter value is less than 5, the program loops back to step d. If the counter is equal to 5, then the program continues below.

k. If bit 15 is set OFF the program jumps to step 1 below; otherwise, the following occurs:

1. If option bits 1 and 10 are set OFF, the "EOT 1" message is printed. If either program option bit 1 or 10 is set ON, the message is by-passed.

2. The program halts with 102076_8 in MEMORY DATA. The A- and B-Registers contain the test number (1). Press RUN to continue.

l. If program option bit 8 is set OFF, the program continues on to the next EAU instruction test. If program option bit 8 is set ON, the program loops back to step a.

DST Test

DST tests the "double store" instruction as follows:

a. If program option bit 6 is set OFF, new arguments are generated. If program option bit 6 is set ON, then previously generated arguments are used.

b. The indirect addressing level counter is cleared.

c. The EAU instruction is modified to reflect the level of indirect addressing (level 0 is direct).

d. The expected results (obtained by the non-EAU routine) are computed and stored.

e. The DST EAU instruction is executed and the expected results compared with the actual results.

f. If no errors exist, the program jumps to step g. If errors are found, DST performs the following:

   1. If program option bits 1 and 11 are both set OFF, an error message is printed. If either bit 1 or 11 is set ON, the message is suppressed.

   2. If program option bit 14 is set OFF, the computer halts with 102002_8 in MEMORY DATA. The program continues when the operator presses RUN. If program option bit 14 is set ON, the program does not halt.

   3. If program option bit 9 is set ON, the program jumps to step i. If program option bit 9 is set OFF, then the program continues below.

g. If program option bit 13 is set ON, then the program repeats the test using the same arguments (loops to step d). If program option bit 13 is set OFF, the program continues below.

h. If program option bit 7 is set ON, the indirect addressing tests are skipped. If program option bit 7 is set OFF, the indirect addressing level counter is incremented. If the counter value is less than 5, the program loops back to step c.

i. If program option bit 15 is set OFF, then the program jumps to step j; otherwise, the following occurs:

   1. If program option bits 1 and 10 are both set OFF, then "EOT 2" message is printed. If either program option bit 1 or 10 is set ON, the message is bypassed.

   2. The program halts with 102076_8 in MEMORY DATA. The A- and B-Registers contain the test number (2). Press RUN to continue.

j. If program option bit 8 is set OFF, the program continues on to the next instruction test. If program option bit 8 is set ON, the program loops back to step a.

ASR Test

ASR tests the "arithmetic long shift right" instruction as follows:

a. If program option bit 6 is set OFF, new arguments are generated.
If program option bit 6 is set ON, then previously generated arguments are used.

b. The shift counter is cleared if switch 6 was OFF.

c. The non-EAU subroutine is executed to obtain the expected results.

d. The actual EAU instruction is modified to reflect the shift level.

e. The registers are initialized.

f. The EAU instruction is executed and the expected results compared with the actual results.

g. If no errors exist, the program jumps to step h.
If an error is found, ASR performs the following:

1. If program option bits 1 and 11 are both set OFF, then an error message is printed on the teleprinter. If either program option bit 1 or 11 is set ON, the message is bypassed.

2. If program option bit 14 is set ON, the program jumps to step 3.
If program option bit 14 is set OFF, the program halts with 102005_8 in MEMORY DATA.
The program continues when the operator presses RUN.

3. If program option bit 9 is set ON, the program jumps to step j.
Otherwise, it continues below.

h. If program option bit 13 is set ON, the program loops back to step d. Otherwise, it continues below.

i. If program option bit 6 was ON at the beginning of the instruction test, the program skips to step j. Otherwise, the program increments the shift counter and checks to see if the counter value is equal to 20. If it is less than 20, the program loops back to step c. Otherwise, it continues below.

j. If program option bit 15 is set OFF, the program skips to step k; otherwise, the following occurs:

   1. If program option bits 1 and 10 are OFF, the "EOT 5" message is printed. Otherwise, the message is bypassed.

   2. The program halts with 102076_8 in MEMORY DATA. The A- and B-Registers contain the test number (5). Press RUN to continue.

k. If program option bit 8 is set OFF, the program continues on to the next test. If program option bit 8 is set ON, the program loops back to step a.

HP 2100 LOW MEMORY ADDRESS TEST
AND
HP 2100 HIGH MEMORY ADDRESS TEST

HP Product No. HP 24211
and
HP Product No. HP 24212

11000 Wolfe Road
Cupertino, California 95014

Manual of Diagnostics
Diagnostic Program Procedure
02100-90008

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HP 2100 MEMORY ADDRESS TESTS

These two diagnostic programs, the HP 2100 Low Memory Address Test and the HP 2100 High Memory Address Test, check the memory address register of an HP 2100 computer and any user-specified area of core. The Low-Test occupies lower memory to test upper memory addresses, while the High-Test occupies upper memory to test lower memory addresses.

HARDWARE CONFIGURATION

These diagnostic programs are run on an HP 2100 computer only. A punched tape reader is the only peripheral device used, when possible, to load the selected program into core. Errors are reported by displays in the computer front panel registers.

When either program is run, the P.E. switch (S2) on the I/O buffer board should be set to HALT.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

Either the Low- or the High- Memory Address Test may be run first, followed by the other. The Basic Binary Loader (if useable) places each program into core at the desired time; otherwise, either program may be loaded through the front panel.

When the Low-Test is used, operation is started at location 0100_8 to test any user-specified area in the range of addresses 0144_8 through the upper limit of memory. (The program resides in locations 0100_8 through 0143_8.)

When the High-Test is used, operation is started at location 3600_8 to test any user-specified area below address 3600_8 (except address 0 and 1) or above 3643_8. (The program resides in locations 3600_8 through 3643_8.)

After the desired Memory Address Test has been loaded, the user specifies the first then the last address to be tested.

> *NOTE: Neither Memory Address Test program checks the limits of the first and last addresses specified. The user should take care to avoid destruction of the program or the Basic Binary Loader.*

The program then runs continuously until an error is detected or the user changes control either to terminate the program or to change the area to be tested. The EXTEND button light changes state every 20 program cycles to show that the program is looping successfully.

To test each address in the area specified, the program begins by writing the address number into each location throughout the test area. Then it returns to the first address to start a continuous loop in which each address is tested by reading the content and checking for a difference between the address and the content. The loop runs through the last address then returns to the first address.

If a difference is detected, the program halts with MEMORY DATA 102077_8 in the computer DISPLAY REGISTER, the current address in the A-Register (press A to display) and the content of that address in the B-Register (press B to display). To resume the program, the user presses RUN again.

OPERATING INSTRUCTIONS

a. Set the P.E. switch (S2) on the I/O buffer board to HALT.

b. Use the Basic Binary Loader (BBL) to load the desired Memory Address Test. Or, if the BBL is not useable, load the program manually through the front panel* from the listing on page MAT-4 or MAT-5.

c. If the Low Memory Address Test was just loaded, set the starting address 100_8; otherwise, set the starting address 3600_8.

*The required steps are described in the *SOFTWARE OPERATING PROCEDURES* manual.

d. Press INTERNAL and EXTERNAL PRESET then press RUN. The program halts with MEMORY DATA 102000_8 displayed.

e. Press S, set the DISPLAY REGISTER to the first address to be tested, then press RUN. The program halts with MEMORY DATA 102001_8 displayed.

f. Press S, set the DISPLAY REGISTER to the last address to be tested, then press RUN. The program runs until a difference is detected or the user changes control.

g. The user may change control of the program either to terminate execution (press HALT) or to change the first and last addresses to be tested (set switch register* bit 15 on). If bit 15 is set on, the program halts with MEMORY DATA 102000_8 displayed. Now perform steps e through g again.

h. When this program is terminated, set the P.E. switch (S2) on the I/O buffer board to the desired position.

*While a program is running, the HP 2100 computer S button is lit to indicate the switch register is controlled through the DISPLAY REGISTER. Thus, to set a switch register bit press that bit in the DISPLAY REGISTER.

```
PAGE 0002 #01  2100  LOW MEMORY ADDRESS TEST


0001                    ASMB,A,B,L,T,C
0003  00100             ORG 100B
0004  00100 002500  BEGIN CLA,CLF
0005  00101 070142      STA CNT       RESET F REGISTER INDICATOR
0006  00102 102000      HLT 0         HALT TO GET STARTING ADDRESS
0007  00103 102501      LIA 1         INPUT AND
0008  00104 070140      STA FWA         SAVE STARTING ADDRESS
0009  00105 102001      HLT 1         HALT TO GET ENDING ADDRESS
0010  00106 106501      LIB 1         INPUT AND
0011  00107 074141      STB LWA         SAVE ENDING ADDRESS
0012  00110 060140  WRITE LDA FWA
0013  00111 170000  WRIT1 STA A,I     IN EACH LOCATION IN THE RANGE,
0014  00112 050141      CPA LWA         STORE IT'S ADDRESS
0015  00113 024116      JMP READ
0016  00114 002004      INA
0017  00115 024111      JMP WRIT1
0018  00116 060140  READ  LDA FWA     FROM EACH CORE LOCATION IN THE
0019  00117 164000  READ1 LDB A,I       RANGE, READ IT'S CONTENTS &
0020  00120 050001      CPA B             CHECK THAT IT IS THE SAME AS
0021  00121 002001      RSS                 IT'S ADDRESS
0022  00122 102077      HLT 77B       ERROR: A=ADDRESS, B=BAD CONTENTS
0023  00123 050141      CPA LWA
0024  00124 024127      JMP FNSH
0025  00125 002004      INA
0026  00126 024117      JMP READ1
0027  00127 060142  FNSH  LDA CNT
0028  00130 002004      INA           STEP COUNTER
0029  00131 050143      CPA .20         IF 20, RESET IT & CHANGE F
0030  00132 002600      CLA,CME
0031  00133 070142      STA CNT
0032  00134 102501      LIA 1
0033  00135 002020      SSA           CHECK SWITCH 15
0034  00136 024100      JMP BEGIN       SET - GET NEW ADDRESSES
0035  00137 024110      JMP WRITE       CLEAR - DO ANOTHER LOOP
0036*
0037  00140 000000  FWA   NOP         FIRST WORD ADDRESS
0038  00141 000000  LWA   NOP         LAST WORD ADDRESS
0039  00142 000000  CNT   NOP         COUNTER
0040  00143 000024  .20   DEC 20
0041  00000         A     EQU 0       A REGISTER
0042  00001         B     EQU 1       B REGISTER
0043                    END
** NO ERRORS*
```

```
0001                    ASMB,A,B,L,T,C
0003  03600             ORG 3600B
0004  03600 002500 BEGIN CLA,CLF
0005  03601 073642       STA CNT       RESET E REGISTER INDICATOR
0006  03602 102000       HLT 0         HALT TO GET STARTING ADDRESS
0007  03603 102501       LIA 1         INPUT AND
0008  03604 073640       STA FWA         SAVE STARTING ADDRESS
0009  03605 102001       HLT 1         HALT TO GET ENDING ADDRESS
0010  03606 106501       LIB 1         INPUT AND
0011  03607 077641       STB LWA         SAVE ENDING ADDRESS
0012  03610 063640 WRITE LDA FWA
0013  03611 170000 WRIT1 STA A,I       IN EACH LOCATION IN THE RANGE,
0014  03612 053641       CPA LWA         STORE IT'S ADDRESS
0015  03613 027616       JMP READ
0016  03614 002004       INA
0017  03615 027611       JMP WRIT1
0018  03616 063640 READ  LDA FWA       FROM EACH CORE LOCATION IN THE
0019  03617 164000 READ1 LDB A,I         RANGE, READ IT'S CONTENTS &
0020  03620 050001       CPA B             CHECK THAT IT IS THE SAME AS
0021  03621 002001       RSS                 IT'S ADDRESS
0022  03622 102077       HLT 77B       ERROR: A=ADDRESS, B=BAD CONTENTS
0023  03623 053641       CPA LWA
0024  03624 027627       JMP FNSH
0025  03625 002004       INA
0026  03626 027617       JMP READ1
0027  03627 063642 FNSH  LDA CNT
0028  03630 002004       INA           STEP COUNTER
0029  03631 053643       CPA .20         IF 20, RESET IT & CHANGE E
0030  03632 002600       CLA,CME
0031  03633 073642       STA CNT
0032  03634 102501       LIA 1
0033  03635 002020       SSA           CHECK SWITCH 15
0034  03636 027600       JMP BEGIN       SET = GET NEW ADDRESSES
0035  03637 027610       JMP WRITE       CLEAR = DO ANOTHER LOOP
0036*
0037  03640 000000 FWA   NOP           FIRST WORD ADDRESS
0038  03641 000000 LWA   NOP           LAST WORD ADDRESS
0039  03642 000000 CNT   NOP           COUNTER
0040  03643 000024 .20   DEC 20
0041  00000       A     EQU 0         A REGISTER
0042  00001       B     EQU 1         B REGISTER
0043                    END
** NO ERRORS*
```

HP 2100 SHIFT-ROTATE INSTRUCTION TEST

HP Product No. HP 24210

HEWLETT hp PACKARD

11000 Wolfe Road
Cupertino, California 95014

Manual of Diagnostics
Diagnostic Program Procedure
HP 02100-90017

June 1971

HP 2100 SHIFT-ROTATE INSTRUCTION TEST

This diagnostic program checks all the code combinations of the Shift-Rotate Instruction Group as defined in the Consolidated Coding Table. The secondary objective is checking instructions and conditions affecting the overflow register. Also included as a special case is a check of eight individual rotate instruction codes involving the E-register. These instructions are tested individually and not as part of any combination. The D/E (Disable/Enable) fields of these instructions are set to zero. (See Figure SFT-4, Consolidated Coding Table.)

HARDWARE CONFIGURATION

The program runs on any core size HP 2100 computer and does not use a teleprinter.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

This program should be run only after the Memory-Reference Instruction Test and the Alter-Skip Instruction Test as instructions in these groups are used to test the shift-rotate group. The program uses no shift-rotate instructions except for those being tested.

To run the program the user loads the program with the Basic Binary Loader, sets the Starting Address 100_8 and presses RUN. The program now tests all shift-rotate instructions, checking each valid instruction 14 times. First, seven different data patterns are checked in either the A- or B-register depending on the instruction, with the E-register clear, then the seven different data patterns are checked in either the A- or B-register depending on the instruction, with the E-register set.

After execution of each shift rotate instruction, the program checks the contents of the A- or B-register and the E-register and checks that the instruction did or did not skip as expected.

A detected failure results in a halt and an information display. MEMORY DATA contains the coded halt $10200x_8$. x is an octal digit with bit meanings as follows:

bit 0 = 1,A- or B-register error.

bit 1 = 1,E-register error.

bit 2 = 1,Instruction skipped or did not skip as expected.

The information should also be displayed after the error halt:

A-register--Actual A- or B-register result.

B-register--Expected A- or B-register result.

E-register--Actual E-register result.

After RUN is pressed, another halt occurs and this information should be displayed:

MEMORY DATA--Second display halt (102000_8) identification.

A-register--Octal code of failing shift-rotate instruction;
bit 11 of the instruction identifies the register
0=A-register, 1=B-register.

B-register--Original data pattern in the A- or B-register.

E-register--Original contents of the E-register.

Following the second display halt, the program continues if switch register bit 0 is clear. If switch register bit 0 is set, the original values are restored in the E- and A- or B-registers, and another halt (102076_8) occurs. The next instruction executed is the failing instruction. The result can be observed by single stepping.

The program now executes overflow register tests, a string of individual tests. Errors here result in a unique coded error halt. (See Table SFT-2). No provisions are available for repeating overflow register tests.

After all instructions have been tested, the program normally loops continuously until an error is detected. If switch register bit 15 is set, the computer halts with 102077_8 displayed in MEMORY DATA and a 32 bit pass count contained in the A- and B-registers, with the most significant bits in the B-register.

Unexpected Changes In The A- Or B-Registers

If a change occurs in the B-register after executing a skip-rotate instruction involving the A-register or vice versa, the computer halts with 103000_8 displayed in MEMORY DATA if the A-register changed unexpectedly, or with 103001_8 displayed in MEMORY DATA if the B-register changed unexpectedly. The unexpected change is left in the register, and the other register contains the octal code of the shift-rotate instruction. Normally when the operator presses RUN, the program bypasses the other results usually checked. If switch register bit 0 is set, the computer halts with 102076_8 displayed in MEMORY DATA. The failing instruction is the next instruction executed. The results can be observed by single stepping.

A fixed non-symmetrical data pattern of 043210_8 is placed in the register (A- or B-) not expected to change before each skip-rotate instruction is executed.

OPERATING INSTRUCTIONS

a. Load the HP 2100 Shift-Rotate Instruction Test with the Basic Binary Loader.

b. Set Starting Address 100_8.

c. Press RUN.
   The program executes according to the switch register options selected.

Table 1

Switch Register Options

Bit if Set	Meaning
0	Repeat a failing shift-rotate but halt 102076_8 before its execution. (Does not apply to the overflow register tests.)
15	Halt 102077_8 at the end of pass (diagnostic cycle). A pass count is contained in the B- and A-registers (most significant bits in B-register).

Table SFT-2

Summary of Program Halts

MEMORY DATA	Comments
10200X	Shift Rotate Instruction error halt.
102000	Display halt following error halt.
102076	Halt before repeating failing Shift-Rotate instruction.
102077	End of pass halt (A- and B-registers contain the number of passes completed after the halt).
102040	CLO-SOC combination failed.
102041	CLO-SOS combination failed.
102042	STO-SOS combination failed.
102043	STO-SOC combination failed.
102044	STO-SOS,C combination failed.
102045	SOS,C did not clear OV.
102050	A was 077777 and INA did not set OV.
102051	A was 177777 and INA set OV.
102052	Sum of 077777 & 077777 in A did not set OV.
102053	Sum of 100000 & 100000 in A did not set OV.
102054	Sum of 077777 & 100000 in A set OV.
102055	Sum of 177777 & 177777 in A set OV.
102056	Sum of 000000 & 000000 in A set OV.
102060	B was 077777 and INB did not set OV.
102061	B was 177777 and INB set OV.
102062	Sum of 077777 & 077777 in B did not set OV.
102063	Sum of 100000 & 100000 in B did not set OV.
102064	Sum of 077777 & 100000 in B set OV.
102065	Sum of 177777 & 177777 in B set OV.
102066	Sum of 000000 & 000000 in B set OV.
103000	Unexpected change in A-register.
103001	Unexpected change in B-register.

Figure SFT-1
Consolidated Coding Table

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEMORY REFERENCE INSTRUCTIONS															
D/I	AND	001		0	Z/C	← Memory Address →									
D/I	XOR	010		0	Z/C										
D/I	IOR	011		0	Z/C										
D/I	JSB	001		1	Z/C										
D/I	JMP	010		1	Z/C										
D/I	ISZ	011		1	Z/C										
D/I	AD*	100		A/B	Z/C										
D/I	CP*	101		A/B	Z/C										
D/I	LD*	110		A/B	Z/C										
D/I	ST*	111		A/B	Z/C										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHIFT-ROTATE GROUP INSTRUCTIONS															
0	SRG	000		A/B	0	D/E	*LS	000		†CLE	D/E	‡SL*	*LS	000	
				A/B	0	D/E	*RS	001			D/E		*RS	001	
				A/B	0	D/E	R*L	010			D/E		R*L	010	
				A/B	0	D/E	R*R	011			D/E		R*R	011	
				A/B	0	D/E	*LR	100			D/E		*LR	100	
				A/B	0	D/E	ER*	101			D/E		ER*	101	
				A/B	0	D/E	EL*	110			D/E		EL*	110	
				A/B	0	D/E	*LF	111			D/E		*LF	111	
				NOP	000			000			000			000	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALTER-SKIP GROUP INSTRUCTIONS															
0	ASG	000		A/B	1	CL*	01	CLE	01	SEZ	SS*	SL*	IN*	SZ*	RSS
				A/B	1	CM*	10	CME	10						
				A/B	1	CC*	11	CCE	11						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAC AND INPUT/OUTPUT INSTRUCTIONS															
1	MAC	000		A/B	0										
1	IOG	000		A/B	1	H/C	HLT	000		← Select Code →					
					1	0	STF	001							
					1	1	CLF	001							
					1	0	SFC	010							
					1	0	SFS	011							
				A/B	1	H/C	MI*	100							
				A/B	1	H/C	LI*	101							
				A/B	1	H/C	OT*	110							
				0	1	H/C	STC	111							
				1	1	H/C	CLC	111							
					1	0	STO	001			000			001	
					1	1	CLO	001			000			001	
					1	H/C	SOC	010			000			001	
					1	H/C	SOS	011			000			001	

Notes: 1) * = A or B. Use with bit 11 as Ø (A-Register) or 1 (B-Register).

2) D/I, A/B, Z/C, D/E, H/C coded: 0/1.

3) † CLE: Only this bit is required.

4) ‡ SL*: Only this bit and bit 11 (A/B as applicable) are required.

HP 2100 MEMORY REFERENCE INSTRUCTION TEST

HP Product No. HP 24209

11000 Wolfe Road
Cupertino, California 95014

Manual of Diagnostics
Diagnostic Program Procedure
02100-90018

June 1971

HP 2100 MEMORY REFERENCE INSTRUCTION TEST

The HP 2100 Memory Reference Instruction Test program confirms that all 14 memory reference instructions operate correctly. This program should be the first one run in an HP 2100 computer, followed by the HP 2100 Alter-Skip Instruction Test and the HP 2100 Shift-Rotate Instruction Test programs.

HARDWARE CONFIGURATION

This program is run in any HP 2100 computer. No peripheral devices are used; errors and messages to the user are read from the program listing at the end of this text, according to the location at which a halt occurs.

PROGRAM ORGANIZATION

The program includes one pre-test routine and ten test modules.

The pre-test routine is a loop that confirms operation of four instructions and the switch register: LIA 1 (load the contents of the switch register into the A-register), HLT (halt), OTA 1 (output the contents of the A-register to the switch register), and JMP LPØ (jump back to the start of the routine).

After the pre-test routine, the main portion of the Memory Reference Instruction Test program is started. The ten test modules perform the following functions:

BASIC TESTS

> Checks for proper operation of simple alter-skip instructions that are used later within this module and within other modules. After the simple alter-skip instructions, this module tests simple uses of each memory reference instruction.

MEMORY REFERENCES TO A & B

Checks operation of each memory reference instruction through the A- and B-registers.

E & OV REGISTER CHECKS

Checks the results in the extend and overflow registers after execution of ADA and ADB instructions.

INDIRECT ADDRESSING TESTS

Tests each memory reference instruction for one and two levels of indirect addressing.

INDIRECT ADDRESSING TO PAGE 1

Test each memory reference instruction for indirect addressing to page 1 from the base page (page 0).

NOTE: The base page (page 0) includes locations 0 through 1777_8, and page 1 includes locations 2000_8 through 3777_8.

INDIRECT ADDRESSING TO THE BASE PAGE (PAGE 0)

Tests each memory reference instruction for indirect addressing to the base page (page 0) from page 1.

REGISTER INTERACTION TESTS

Confirms that each memory reference instruction affects only the proper register(s). For example, an LDA instruction must not change the B, E, or OV (overflow) registers.

INDIRECT ADDRESSING VIA THE A & B REGISTERS

Tests each memory reference instruction for indirect addressing via the A- and B-registers.

ITERATIVE TESTS

Repeats each memory reference instruction in a loop 65K times to ensure it executes consistently. If an intermittent failure exists, this routine possibly will find it.

DATA PATTERN TESTS

Checks the load, store, and compare instructions throughout two pages (2K) of memory (less the last 100_8 locations). Then this routine checks the ADA, ADB, IOR, XOR, and AND instructions for execution with 10 pairs of arbitrary arguments.

Normally after each module has completed its tests, the program advances to the next module through an NOP (no operation) instruction. However, the user may consult the listing of this program (at the end of this text) and change any NOP instruction (through front panel access) to a HLT or a JMP instruction, if needed.

ERROR ANALYSIS

If the program detects an error, it halts with 102000_8 displayed. To determine the error, press M to display the halt address, then consult the program listing, at the rear of this text.

In most cases, two steps are used to determine what specific failure occurred. First, read the comments in the program listing for that halt. Then use the INSTRUCTION STEP button to step through the program one-instruction-at-a-time from the instruction following the *preceding* halt. Carefully check the results of each instruction after each press of the INSTRUCTION STEP button. After the error has been analyzed, the program may be resumed by setting the next instruction address, pressing INTERNAL and EXTERNAL PRESET, then pressing RUN.

At the end of a complete cycle, the program tests bit 15 of the switch register. If that bit is set on, the program halts with 102077_8 displayed. If bit 15 is set off, the program restarts at the Basic Tests module.

A complete cycle of the program occurs in 30 to 40 seconds.

If the computer halts with 107077_8 in the DISPLAY REGISTER, the program has advanced to an unused location. (When the program is loaded, all unused locations are set to the special halt instruction 107077_8.) Isolate the program module that caused the error by patching and by trial and error. For example, the NOP instruction at the end of a program module may be changed to an HLT or a JMP instruction.

NOTE: It may be necessary to reload the program first.

OPERATING INSTRUCTIONS

a. Use the Basic Binary Loader to load the HP 2100 Memory Reference Instruction Test program.

NOTE: If the Basic Binary Loader does not appear to operate correctly, refer to the SOFTWARE OPERATING PROCEDURES manual.

b. The pre-test routine (summarized in the Program Organization section of this text) can be used or skipped. To use it, skip to step f, otherwise proceed directly to step c.

c. Start the main portion of the HP 2100 Memory Reference Instruction Test program:

   1. Set the starting address 100_8.
   2. Clear the switch register.
   3. Press INTERNAL and EXTERNAL PRESET then press RUN.

d. The program runs continuously until an error is detected or it is halted as described in step e.

e. To halt the program at the end of a complete cycle (102077_8 is displayed), set switch register bit 15 on. (While the program is running the S button is lit, indicating that the switch register may be set through the DISPLAY REGISTER.) Or, to halt the program at any time, press HALT/CYCLE.

f. To use the pre-test routine, consult the listing of the program at the rear of this text. The pre-test routine resides in memory locations 10_8 through 13_8. Use the INSTRUCTION STEP button to step through this routine one-instruction-at-a-time. Carefully check the results of each instruction after each press of the INSTRUCTION STEP button. When finished, return to step c.

```
0001                    ASMB,A,B,L,T
LP0       000010
START     000100
X1        000453
X2        000454
X4        000503
X5        000515
RTN1      000522
RTN2      000526
P3        000531
RTN3      000532
P4        000542
RTN4      000543
X20       000644
X21       000654
X22       000665
X23       000675
X24       000704
IR1       001301
IR2       001303
RA3       001307
RA4       001320
JMP2      001612
.P3       001615
.P4       001616
M1        001625
M2        001626
.0        001627
.1        001630
EVEN1     001631
ODD1      001632
K1        001633
PMAX      001634
BIT15     001635
HLT0      001636
H7077     001637
T1        001640
ADDR1     001641
ADDR3     001642
ADDR4     001643
JR1       001644
JR2       001645
JR3       001646
JR4       001647
A         000000
B         000001
ADDR2     001650
ADDRY     001651
ADDR7     001652
IA1       001653
IA2       001654
IA3       001656
IA4       001657
IA5       001661
IA6       001662
IA7       001663
```



```
IA8       001664
IA9       001665
IA10      001666
K7        001667
IR11      001670
IR12      001671
IR13      001672
IR14      001673
ADR13     001674
ADR14     001675
.P1       001676
.P2       001677
K10       001700
K11       001701
K12       001702
T2A       001703
JMP1A     001704
SR1A      001705
.ADR3     001706
P99A      001707
FCA       001710
LCA       001711
JSB7      001712
JMP5      001716
PG1       001777
P6        002062
P7        002065
P9        002066
P99       002223
X99       002224
RA11      002542
RA12      002545
P13       002551
X13       002552
P14       002566
X14       002567
LP1       002623
LP2       002632
LP3       002641
LP4       002650
LP5       002657
LP6       002667
LP7       002677
LP8       002707
LP9       002717
LP10      002726
LP11      002736
LP12      002746
LP13      002756
LP14      002766
LP15      002776
LP16      003006
LP17      003015
LP18      003024
LP19      003034
LP20      003052
```

```
LP21     003070
LP22     003106
LP23     003124
LP24     003142
LP25     003160
LP26     003176
LP27     003214
Z1       003217
Z2       003220
PT1      003247
PT2      003257
PT3      003260
PT4      003274
PT5      003275
A1A      003362
A2A      003363
SUMA     003364
IORA     003365
XORA     003366
ANDA     003367
K10A     003370
K11A     003371
T1A      003372
K12A     003373
JMP5A    003374
JSB7A    003375
P7A      003376
TBLA     003377
TBL.1    003400
TBL.2    003406
TBL.3    003414
TBL.4    003422
TBL.5    003430
TBL.6    003436
TBL.7    003444
TBL.8    003452
TBL.9    003460
TB.10    003466
TBLE     003474
T2       003475
SR1      003476
JMP1     003500
**  NO ERRORS*
```



```
0001                ASMB,A,B,L,T
0003*
0004  00002                ORG 2
0005* THE FOLLOWING SOURCE LINES ARE SUPPRESSED
0006*     UNL            SUPPRESS SOURCE LISTING
0007*    REP 1982       PUT 107077 HALTS IN CORE
0008*     OCT 107077       LOCATIONS 2 THRU 3677 (2K)
0012                       LST           RESUME SOURCE LISTING


0014* THE FOLLOWING IS A SIMPLE LOOP WHICH CAN BE USED TO CHECK THE
0015* SWITCH REGISTER, HLT INSTRUCTION, & JMP INSTRUCTION.
0016*
0017  00010                ORG 10B
0018  00010 102501  LP0    LIA 1         SWITCH REGISTER TO A REG.
0019  00011 102000         HLT 0         T=102000, A=SW. REG. CONTENTS
0020  00012 102601         OTA 1         SW. REG. ← A REG.
0021  00013 024010         JMP LP0       DO AGAIN
```

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```
0023  00100                ORG 100B
0024*
0025* CHECK SIMPLE ALTER-SKIP INSTRUCTIONS
0026*
0027  00100 002001  START RSS
0028  00101 102000        HLT 0          RSS FAILED
0029*
0030  00102 002400        CLA
0031  00103 002002        SZA
0032  00104 102000        HLT 0          CLA/SZA FAILED
0033*
0034  00105 002400        CLA
0035  00106 002003        SZA,RSS
0036  00107 002001        RSS
0037  00110 102000        HLT 0          CLA/SZA,RSS FAILED
0038*
0039  00111 006400        CLB
0040  00112 006002        SZB
0041  00113 102000        HLT 0          CLB/SZB FAILED
0042*
0043  00114 006400        CLB
0044  00115 006003        SZB,RSS
0045  00116 002001        RSS
0046  00117 102000        HLT 0          CLB/SZB,RSS FAILED
0047*
0048* CHECK CPA INSTRUCTION
0049*
0050  00120 002400        CLA
0051  00121 051627        CPA ,0
0052  00122 002001        RSS
0053  00123 102000        HLT 0          CLA/CPA ,0 FAILED
0054*
0055  00124 002400        CLA
0056  00125 051625        CPA M1
0057  00126 102000        HLT 0          CLA/CPA M1 FAILED
0058*
0059  00127 003400        CCA
0060  00130 051625        CPA M1
0061  00131 002001        RSS
0062  00132 102000        HLT 0          CCA/CPA M1 FAILED
0063*
0064  00133 002404        CLA,INA
0065  00134 002003        SZA,RSS
0066  00135 102000        HLT 0          CLA,INA/SZA,RSS FAILED
0067*
0068  00136 002404        CLA,INA
0069  00137 051630        CPA ,1
0070  00140 002001        RSS
0071  00141 102000        HLT 0          CLA,INA/CPA ,1 FAILED
0072*
0073* CHECK LDA & CPA INSTRUCTIONS
0074*
0075  00142 061627        LDA ,0
0076  00143 051627        CPA ,0
0077  00144 002001        RSS
0078  00145 102000        HLT 0          LDA ,0/CPA ,0 FAILED
```

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```
0079*
0080  00146 061625        LDA M1
0081  00147 051625        CPA M1
0082  00150 002001        RSS
0083  00151 102000        HLT 0          LDA M1/CPA M1 FAILED
0084*
0085  00152 061631        LDA EVEN1
0086  00153 051631        CPA EVEN1
0087  00154 002001        RSS
0088  00155 102000        HLT 0          LDA EVEN1/CPA EVEN1 FAILED
0089*
0090  00156 061632        LDA ODD1
0091  00157 051632        CPA ODD1
0092  00160 002001        RSS
0093  00161 102000        HLT 0          LDA ODD1 /CPA ODD1 FAILED
0094*
0095  00162 002400        CLA
0096  00163 051625        CPA M1
0097  00164 102000        HLT 0          CLA/CPA M1 FAILED
0098*
0099  00165 061631        LDA EVEN1
0100  00166 051632        CPA ODD1
0101  00167 102000        HLT 0          LDA EVEN1/CPA ODD1 FAILED
0102*
0103*
0104* CHECK STA INSTRUCTION
0105*
0106  00170 002400        CLA
0107  00171 071640        STA T1
0108  00172 051640        CPA T1
0109  00173 002001        RSS
0110  00174 102000        HLT 0          CLA/STA T1/CPA T1 FAILED
0111*
0112  00175 003400        CCA
0113  00176 071640        STA T1
0114  00177 051640        CPA T1
0115  00200 002001        RSS
0116  00201 102000        HLT 0          CLA/STA T1/CPA T1 FAILED
0117*
0118  00202 061631        LDA EVEN1
0119  00203 071640        STA T1
0120  00204 051640        CPA T1
0121  00205 002001        RSS
0122  00206 102000        HLT 0          LDA EVEN1/STA T1/CPA T1 FAILED
0123*
0124  00207 061632        LDA ODD1
0125  00210 071640        STA T1
0126  00211 051640        CPA T1
0127  00212 002001        RSS
0128  00213 102000        HLT 0          LDA ODD1/STA T1/CPA T1 FAILED
0129*
0130*
0131* CHECK AND INSTRUCTION
0132*
0133  00214 003400        CCA
0134  00215 011625        AND M1
```

```
0135  00216 051625        CPA M1
0136  00217 002001        RSS
0137  00220 102000        HLT 0          CCA/AND M1/CPA M1 FAILED
0138*
0139  00221 002400        CLA
0140  00222 011625        AND M1
0141  00223 002002        SZA
0142  00224 102000        HLT 0          CLA/AND M1/SZA FAILED
0143*
0144  00225 002400        CLA
0145  00226 011627        AND .0
0146  00227 002002        SZA
0147  00230 102000        HLT 0          CLA/AND .0/SZA FAILED
0148*
0149  00231 003400        CCA
0150  00232 011627        AND .0
0151  00233 002002        SZA
0152  00234 102000        HLT 0          CCA/AND .0/SZA FAILED
0153*
0154* CHECK IOR INSTRUCTION
0155*
0156  00235 002400        CLA
0157  00236 031627        IOR .0
0158  00237 002002        SZA
0159  00240 102000        HLT 0          CLA/IOR .0/SZA FAILED
0160*
0161  00241 002400        CLA
0162  00242 031625        IOR M1
0163  00243 051625        CPA M1
0164  00244 002001        RSS
0165  00245 102000        HLT 0          CLA/IOR M1/CPA M1 FAILED
0166*
0167  00246 003400        CCA
0168  00247 031625        IOR M1
0169  00250 051625        CPA M1
0170  00251 002001        RSS
0171  00252 102000        HLT 0          CCA/IOR M1/CPA M1 FAILED
0172*
0173  00253 003400        CCA
0174  00254 031627        IOR .0
0175  00255 051625        CPA M1
0176  00256 002001        RSS
0177  00257 102000        HLT 0          CCA/IOR .0/CPA M1 FAILED
0178*
0179* CHECK XOR INSTRUCTION
0180*
0181  00260 002400        CLA
0182  00261 021627        XOR .0
0183  00262 002002        SZA
0184  00263 102000        HLT 0          CLA/XOR .0/SZA FAILED
0185*
0186  00264 003400        CCA
0187  00265 021627        XOR .0
0188  00266 051625        CPA M1
0189  00267 002001        RSS
0190  00270 102000        HLT 0          CCA/XOR .0/CPA M1 FAILED
```



```
0191*
0192  00271 002400        CLA
0193  00272 021625        XOR M1
0194  00273 051625        CPA M1
0195  00274 002001        RSS
0196  00275 102000        HLT 0          CLA/XOR M1/CPA M1 FAILED
0197*
0198  00276 003400        CCA
0199  00277 021625        XOR M1
0200  00300 002002        SZA
0201  00301 102000        HLT 0          CCA/XOR M1/SZA FAILED
0202*
0203* CHECK CPB INSTRUCTION
0204*
0205  00302 006400        CLB
0206  00303 055627        CPB .0
0207  00304 002001        RSS
0208  00305 102000        HLT 0          CLB/CPB .0 FAILED
0209*
0210  00306 006400        CLB
0211  00307 055625        CPB M1
0212  00310 102000        HLT 0          CLB/CPB M1 FAILED
0213*
0214  00311 007400        CCB
0215  00312 055625        CPB M1
0216  00313 002001        RSS
0217  00314 102000        HLT 0          CCB/CPB M1 FAILED
0218*
0219  00315 006404        CLB,INB
0220  00316 006003        SZB,RSS
0221  00317 102000        HLT 0          CLB,INB/SZB,RSS FAILED
0222*
0223  00320 006404        CLB,INB
0224  00321 055630        CPB .1
0225  00322 002001        RSS
0226  00323 102000        HLT 0          CLB,INB/CPB .1 FAILED
0227*
0228* CHECK LDB & CPB INSTRUCTIONS
0229*
0230  00324 065627        LDB .0
0231  00325 055627        CPB .0
0232  00326 002001        RSS
0233  00327 102000        HLT 0          LDB .0/CPB .0 FAILED
0234*
0235  00330 065625        LDB M1
0236  00331 055625        CPB M1
0237  00332 002001        RSS
0238  00333 102000        HLT 0          LDB M1/CPB M1 FAILED
0239*
0240  00334 065631        LDB EVEN1
0241  00335 055631        CPB EVEN1
0242  00336 002001        RSS
0243  00337 102000        HLT 0          LDB EVEN1/CPB EVEN1 FAILED
0244*
0245  00340 065632        LDB ODD1
0246  00341 055632        CPB ODD1
```

```
0247  00342 002001        RSS
0248  00343 102000        HLT 0          LDB ODD1/CPB ODD1 FAILED
0249*
0250  00344 006400        CLB
0251  00345 055625        CPB M1
0252  00346 102000        HLT 0          CLB/CPB M1 FAILED
0253*
0254  00347 065631        LDB EVEN1
0255  00350 055632        CPB ODD1
0256  00351 102000        HLT 0          LDB EVEN1/CPB ODD1 FAILED
0257*
0258* CHECK STB INSTRUCTION
0259*
0260  00352 006400        CLB
0261  00353 075640        STB T1
0262  00354 055640        CPB T1
0263  00355 002001        RSS
0264  00356 102000        HLT 0          CLB/STB T1/CPB T1 FAILED
0265*
0266  00357 007400        CCB
0267  00360 075640        STB T1
0268  00361 055640        CPB T1
0269  00362 002001        RSS
0270  00363 102000        HLT 0          CCB/STB T1/CPB T1 FAILED
0271*
0272  00364 065631        LDB EVEN1
0273  00365 075640        STB T1
0274  00366 055640        CPB T1
0275  00367 002001        RSS
0276  00370 102000        HLT 0          LDB EVEN1/STB T1/CPB T1 FAILED
0277*
0278  00371 065632        LDB ODD1
0279  00372 075640        STB T1
0280  00373 055640        CPB T1
0281  00374 002001        RSS
0282  00375 102000        HLT 0          LDB ODD1/STB ODD1/CPB T1 FAILED
0283*
0284* CHECK ADA INSTRUCTION
0285*
0286  00376 002400        CLA
0287  00377 041625        ADA M1
0288  00400 051625        CPA M1
0289  00401 002001        RSS
0290  00402 102000        HLT 0          CLA/ADA M1/CPA M1 FAILED
0291*
0292  00403 003400        CCA
0293  00404 041625        ADA M1
0294  00405 051626        CPA M2
0295  00406 002001        RSS
0296  00407 102000        HLT 0          CCA/ADA M1/CPA M2 FAILED
0297*
0298  00410 061632        LDA ODD1       A=125252
0299  00411 041632        ADA ODD1       A=052524
0300  00412 051633        CPA K1
0301  00413 002001        RSS
0302  00414 102000        HLT 0          LDA ODD1/ADA ODD1/CPA K1 FAILED
```



```
0303*
0304  00415 061631        LDA EVEN1      A = 052525
0305  00416 041631        ADA EVEN1      A = 125252
0306  00417 051632        CPA ODD1
0307  00420 002001        RSS
0308  00421 102000        HLT 0          LDA EVEN1/ADA EVEN1/CPA ODD1 FAI
0309*
0310* CHECK ADB INSTRUCTION
0311*
0312  00422 006400        CLB
0313  00423 045625        ADB M1
0314  00424 055625        CPB M1
0315  00425 002001        RSS
0316  00426 102000        HLT 0          CLB/ADB M1/CPB M1 FAILED
0317*
0318  00427 007400        CCB
0319  00430 045625        ADB M1
0320  00431 055626        CPB M2
0321  00432 002001        RSS
0322  00433 102000        HLT 0          CCB/ADB M1/CPB M2 FAILED
0323*
0324  00434 065632        LDB ODD1       B=125252
0325  00435 045632        ADB ODD1       B=052524
0326  00436 055633        CPB K1
0327  00437 002001        RSS
0328  00440 102000        HLT 0          LDB ODD1/ ADB ODD1/CPB K1 FAILED
0329*
0330  00441 065631        LDB EVEN1      B=125252
0331  00442 045631        ADB EVEN1      B=052525
0332  00443 055632        CPB ODD1
0333  00444 002001        RSS
0334  00445 102000        HLT 0          LDB EVEN1/ADB EVEN1/CPB ODD1 FAI
0335*
0336* CHECK JMP INSTRUCTION
0337*
0338  00446 024450        JMP *+2
0339  00447 102000        HLT 0          JMP FAILED
0340*
0341* CHECK JSB INSTRUCTION
0342*
0343  00450 002400        CLA
0344  00451 070454        STA X2         NOP LOCATION X2
0345  00452 014454        JSB *+2
0346  00453 102000  X1    HLT 0          JSB FAILED
0347  00454 000000  X2    NOP
0348  00455 060454        LDA X2
0349  00456 051641        CPA ADDR1      ADDR1 = ADDRESS X1
0350  00457 002001        RSS
0351  00460 102000        HLT 0          JSB FAILED - BAD RETURN ADDRESS
0352*
0353* CHECK ISZ INSTRUCTION
0354*
0355  00461 002400        CLA
0356  00462 071640        STA T1         T1=0
0357  00463 035640        ISZ T1
0358  00464 002001        RSS
```

```
0359  00465 102000        HLT 0          ISZ FAILED - UNEXPECTED SKIP
0360  00466 065640        LDB T1
0361  00467 055630        CPB .1
0362  00470 002001        RSS
0363  00471 102000        HLT 0          ISZ FAILED - T1 NOT 1
0364*
0365  00472 003400        CCA
0366  00473 071640        STA T1         T1=177777
0367  00474 035640        ISZ T1
0368  00475 102000        HLT 0          ISZ FAILED - DID NOT SKIP
0369  00476 061640        LDA T1
0370  00477 002002        SZA
0371  00500 102000        HLT 0          ISZ FAILED - T1 NOT 0
0372*
0373  00501 002400        CLA
0374  00502 071640        STA T1         T1=0
0375  00503 002004  X4    INA
0376  00504 002003        SZA,RSS
0377  00505 024515        JMP X5
0378  00506 035640        ISZ T1
0379  00507 002001        RSS
0380  00510 102000        HLT 0          ISZ FAILED - UNEXPECTED SKIP
0381  00511 051640        CPA T1
0382  00512 024503        JMP X4
0383  00513 102000        HLT 0          ISZ FAILED - T1 NOT INCREMENTED
0384  00514 024503        JMP X4
0385*
0386  00515 000000  X5    NOP ***** MODULE LOOP
```



```
0388  00516 061644        LDA JR1        A ← JMP RTN1
0389  00517 065636        LDB HLT0       B ← 102000
0390  00520 024000        JMP A
0391  00521 102000        HLT 0          JMP A FAILED
0392*
0393  00522 061636  RTN1  LDA HLT0       A ← 102000
0394  00523 065645        LDB JR2        B ← JMP RTN2
0395  00524 024001        JMP B
0396  00525 102000        HLT 0          JMP B FAILED
0397*
0398  00526 002400  RTN2  CLA            A ← NOP
0399  00527 065646        LDB JR3        B ← JMP RTN3
0400  00530 014000        JSB A
0401  00531 102000  P3    HLT 0          JSB A FAILED
0402  00532 051642  RTN3  CPA ADDR3      ADDR3 = LOCATION P3
0403  00533 002001        RSS
0404  00534 102000        HLT 0          BAD RETURN ADDRESS IN A
0405*
0406  00535 061636        LDA HLT0       A ← 102000
0407  00536 065647        LDB JR4
0408  00537 074002        STB 2          2 ← JMP RTN4
0409  00540 006400        CLB            B ← NOP
0410  00541 014001        JSB B
0411  00542 102000  P4    HLT 0          JSB B FAILED
0412  00543 055643  RTN4  CPB ADDR4      ADDR4 = LOCATION P4
0413  00544 002001        RSS
0414  00545 102000        HLT 0          BAD RETURN ADDRESS IN B
0415*
0416  00546 061637        LDA H7077      H7077 = 107077
0417  00547 070002        STA 2          RESTORE HALT TO LOCATION 2
0418*
0419  00550 065631        LDB EVEN1
0420  00551 060001        LDA B
0421  00552 051631        CPA EVEN1
0422  00553 002001        RSS
0423  00554 102000        HLT 0          LDA B FAILED
0424*
0425  00555 061632        LDA ODD1
0426  00556 064000        LDB A
0427  00557 055632        CPB ODD1
0428  00560 002001        RSS
0429  00561 102000        HLT 0          LDB A FAILED
0430*
0431  00562 007400        CCB
0432  00563 002400        CLA
0433  00564 070001        STA B
0434  00565 006002        SZB
0435  00566 102000        HLT 0          STA B FAILED
0436*
0437  00567 003400        CCA
0438  00570 006400        CLB
0439  00571 074000        STB A
0440  00572 002002        SZA
0441  00573 102000        HLT 0          STB A FAILED
0442*
0443  00574 061631        LDA EVEN1
```

```
0444  00575 065631        LDB EVEN1
0445  00576 050001        CPA B
0446  00577 002001        RSS
0447  00600 102000        HLT 0          CPA B FAILED
0448  00601 054000        CPB A
0449  00602 002001        RSS
0450  00603 102000        HLT 0          CPB A FAILED
0451*
0452  00604 065625        LDB M1
0453  00605 002400        CLA
0454  00606 030001        IOR B
0455  00607 051625        CPA M1
0456  00610 002001        RSS
0457  00611 102000        HLT 0          IOR B FAILED
0458*
0459  00612 007400        CCB
0460  00613 002400        CLA
0461  00614 020001        XOR B
0462  00615 051625        CPA M1
0463  00616 002001        RSS
0464  00617 102000        HLT 0          XOR B FAILED
0465*
0466  00620 007400        CCB
0467  00621 061631        LDA EVEN1
0468  00622 010001        AND B
0469  00623 051631        CPA EVEN1
0470  00624 002001        RSS
0471  00625 102000        HLT 0          AND B FAILED
0472*
0473  00626 065631        LDB EVEN1
0474  00627 002400        CLA
0475  00630 040001        ADA B
0476  00631 051631        CPA EVEN1
0477  00632 002001        RSS
0478  00633 102000        HLT 0          ADA B FAILED
0479*
0480  00634 061632        LDA ODD1
0481  00635 006400        CLB
0482  00636 044000        ADB A
0483  00637 055632        CPB ODD1
0484  00640 002001        RSS
0485  00641 102000        HLT 0          ADB A FAILED
0486*
0487  00642 002400        CLA
0488  00643 006400        CLB
0489  00644 006004  X20     INB          B←B+1: NEXT EXPECTED A CONTENTS
0490  00645 006002        SZB            EXPECT ISZ TO CAUSE SKIP IF 0
0491  00646 024654        JMP X21        NO SKIP EXPECTED
0492  00647 034000        ISZ A
0493  00650 102000        HLT 0          ISZ A FAILED - DID NOT SKIP
0494  00651 002002        SZA
0495  00652 102000        HLT 0          ISZ FAILED - A NOT 0
0496  00653 024665        JMP X22          END OF LOOP
0497  00654 034000  X21   ISZ A
0498  00655 002001        RSS
0499  00656 102000        HLT 0          ISZ A FAILED - UNEXPECTED SKIP
```



```
0500  00657 050001        CPA B
0501  00660 024644        JMP X20
0502  00661 102000        HLT 0          ISZ A FAILED - BAD CONTENTS IN A
0503  00662 024644        JMP X20
0504*
0505  00663 002400        CLA
0506  00664 006400        CLB
0507  00665 002004  X22     INA          A←A+1: NEXT EXPECTED B CONTENTS
0508  00666 002002        SZA            EXPECT ISZ TO CAUSE SKIP IF 0
0509  00667 024675        JMP X23        NO SKIP EXPECTED
0510  00670 034001        ISZ B
0511  00671 102000        HLT 0          ISZ B FAILED - DID NOT SKIP
0512  00672 006002        SZB
0513  00673 102000        HLT 0          ISZ FAILED - B NOT 0
0514  00674 024704        JMP X24          END OF LOOP
0515  00675 034001  X23   ISZ B
0516  00676 002001        RSS
0517  00677 102000        HLT 0          ISZ B FAILED - UNEXPECTED SKIP
0518  00700 054000        CPB A
0519  00701 024665        JMP X22
0520  00702 102000        HLT 0          ISZ B FAILED - BAD CONTENTS IN B
0521  00703 024665        JMP X22
0522*
0523  00704 061631  X24   LDA EVEN1
0524  00705 050000        CPA A
0525  00706 002001        RSS
0526  00707 102000        HLT 0          CPA A FAILED
0527*
0528  00710 065632        LDB ODD1
0529  00711 054001        CPB B
0530  00712 002001        RSS
0531  00713 102000        HLT 0          CPB B FAILED
0532*
0533  00714 061632        LDA ODD1
0534  00715 060000        LDA A
0535  00716 050000        CPA A
0536  00717 002001        RSS
0537  00720 102000        HLT 0          LDA A/CPA A FAILED
0538*
0539  00721 065631        LDB EVEN1
0540  00722 064001        LDB B
0541  00723 054001        CPB B
0542  00724 002001        RSS
0543  00725 102000        HLT 0          LDB B/CPB B FAILED
0544*
0545  00726 003400        CCA
0546  00727 070000        STA A
0547  00730 051625        CPA M1
0548  00731 002001        RSS
0549  00732 102000        HLT 0          STA A FAILED
0550*
0551  00733 065632        LDB ODD1
0552  00734 074001        STB B
0553  00735 055632        CPB ODD1
0554  00736 002001        RSS
0555  00737 102000        HLT 0          STR B FAILED
```

```
0556*
0557  00740 061631        LDA EVEN1
0558  00741 040000        ADA A           052525 + 052525 = 125252
0559  00742 051632        CPA ODD1
0560  00743 002001        RSS
0561  00744 102000        HLT 0           ADA A FAILED
0562*
0563  00745 065632        LDB ODD1        125252 + 125252 = 052524
0564  00746 044001        ADB B
0565  00747 055633        CPB K1
0566  00750 002001        RSS
0567  00751 102000        HLT 0           ADB B FAILED
0568*
0569  00752 003400        CCA
0570  00753 030000        IOR A
0571  00754 051625        CPA M1
0572  00755 002001        RSS
0573  00756 102000        HLT 0           IOR A FAILED
0574*
0575  00757 003400        CCA
0576  00760 010000        AND A
0577  00761 051625        CPA M1
0578  00762 002001        RSS
0579  00763 102000        HLT 0           AND A FAILED
0580*
0581  00764 003400        CCA
0582  00765 020000        XOR A
0583  00766 002002        SZA
0584  00767 102000        HLT 0           XOR A FAILED
0585*
0586  00770 000000        NOP ***** MODULE LOOP
```



```
0588  00771 000040        CLE
0589  00772 002040        SEZ
0590  00773 102000        HLT 0           CLE/SEZ FAILED
0591*
0592  00774 000040        CLE
0593  00775 002041        SEZ,RSS
0594  00776 002001        RSS
0595  00777 102000        HLT 0           CLE/SEZ,RSS/RSS FAILED
0596*
0597  01000 002300        CCE
0598  01001 002041        SEZ,RSS
0599  01002 102000        HLT 0           CCE/SEZ,RSS FAILED
0600*
0601  01003 002300        CCE
0602  01004 002040        SEZ
0603  01005 002001        RSS
0604  01006 102000        HLT 0           CCE/SEZ/RSS FAILED
0605*
0606  01007 103101        CLO
0607  01010 102201        SOC
0608  01011 102000        HLT 0           CLO/SOC FAILED
0609*
0610  01012 103101        CLO
0611  01013 102301        SOS
0612  01014 002001        RSS
0613  01015 102000        HLT 0           CLO/SOS/RSS FAILED
0614*
0615  01016 102101        STO
0616  01017 102301        SOS
0617  01020 102000        HLT 0           STO/SOS FAILED
0618*
0619  01021 102101        STO
0620  01022 102201        SOC
0621  01023 002001        RSS
0622  01024 102000        HLT 0           STO/SOC/RSS FAILED
0623*
0624  01025 102101        STO
0625  01026 103301        SOS C
0626  01027 102000        HLT 0           STO/SOS C FAILED
0627  01030 102201        SOC
0628  01031 102000        HLT 0           SOS,C DID NOT CLEAR OV
0629*
0630* CHECK E & OV RESULTS FOR ADA INSTRUCTION
0631*
0632  01032 000040        CLE
0633  01033 103101        CLO
0634  01034 061634        LDA PMAX        ADD 077777 + 000001
0635  01035 041630        ADA .1
0636  01036 051635        CPA BIT15
0637  01037 002001        RSS
0638  01040 102000        HLT 0           SUM NOT 100000
0639  01041 002040        SEZ
0640  01042 102000        HLT 0           E NOT 0
0641  01043 102301        SOS
0642  01044 102000        HLT 0           OV NOT 1
0643*
```

```
0644  01045 000040        CLE
0645  01046 103101        CLO
0646  01047 061625        LDA M1          ADD 177777 + 177777
0647  01050 041625        ADA M1
0648  01051 051626        CPA M2
0649  01052 002001        RSS
0650  01053 102000        HLT 0           SUM NOT 177776
0651  01054 002041        SEZ,RSS
0652  01055 102000        HLT 0           E NOT 1
0653  01056 102201        SOC
0654  01057 102000        HLT 0           OV NOT 0
0655*
0656  01060 000040        CLE
0657  01061 103101        CLO
0658  01062 061625        LDA M1          ADD 177777 + 000001
0659  01063 041630        ADA .1
0660  01064 002002        SZA
0661  01065 102000        HLT 0           SUM NOT 000000
0662  01066 002041        SEZ,RSS
0663  01067 102000        HLT 0           E NOT 1
0664  01070 102201        SOC
0665  01071 102000        HLT 0           OV NOT 0
0666*
0667  01072 000040        CLE
0668  01073 103101        CLO
0669  01074 002400        CLA
0670  01075 041627        ADA .0          ADD 000000 + 000000
0671  01076 002002        SZA
0672  01077 102000        HLT 0           SUM NOT 000000
0673  01100 002040        SEZ
0674  01101 102000        HLT 0           E NOT 0
0675  01102 102201        SOC
0676  01103 102000        HLT 0           OV NOT 0
0677*
0678  01104 000040        CLE
0679  01105 103101        CLO
0680  01106 061634        LDA PMAX        ADD 077777 + 0777777
0681  01107 041634        ADA PMAX
0682  01110 051626        CPA M2
0683  01111 002001        RSS
0684  01112 102000        HLT 0           SUM NOT 177776
0685  01113 002040        SEZ
0686  01114 102000        HLT 0           E NOT 0
0687  01115 102301        SOS
0688  01116 102000        HLT 0           OV NOT 1
0689*
0690  01117 000040        CLE
0691  01120 103101        CLO
0692  01121 061635        LDA BIT15       ADD 100000 + 100000
0693  01122 041635        ADA BIT15
0694  01123 002002        SZA
0695  01124 102000        HLT 0           SUM NOT 000000
0696  01125 002041        SEZ,RSS
0697  01126 102000        HLT 0           E NOT 1
0698  01127 102301        SOS
0699  01130 102000        HLT 0           OV NOT 1
```



```
0700*
0701  01131 000040        CLE
0702  01132 103101        CLO
0703  01133 061635        LDA BIT15       ADD 100000 + 077777
0704  01134 041634        ADA PMAX
0705  01135 051625        CPA M1
0706  01136 002001        RSS
0707  01137 102000        HLT 0           SUM NOT 177777
0708  01140 002040        SEZ
0709  01141 102000        HLT 0           E NOT 0
0710  01142 102201        SOC
0711  01143 102000        HLT 0           OV NOT 0
0712*
0713  01144 002300        CCE             E ← 1
0714  01145 102101        STO             OV ← 1
0715  01146 061630        LDA .1
0716  01147 041630        ADA .1
0717  01150 002041        SEZ,RSS
0718  01151 102000        HLT 0           E NOT 1
0719  01152 102301        SOS
0720  01153 102000        HLT 0           OV NOT 1
0721*
0722* CHECK E & OV RESULTS FOR ADB INSTRUCTION
0723*
0724  01154 000040        CLE
0725  01155 103101        CLO
0726  01156 006400        CLB
0727  01157 045627        ADB .0          ADD 000000 + 000000
0728  01160 006002        SZB
0729  01161 102000        HLT 0           SUM NOT 000000
0730  01162 002040        SEZ
0731  01163 102000        HLT 0           E NOT 0
0732  01164 102201        SOC
0733  01165 102000        HLT 0           OV NOT 0
0734*
0735  01166 000040        CLE
0736  01167 103101        CLO
0737  01170 065634        LDB PMAX        ADD 077777 + 077777
0738  01171 045634        ADB PMAX
0739  01172 055626        CPB M2
0740  01173 002001        RSS
0741  01174 102000        HLT 0           SUM NOT 177776
0742  01175 002040        SEZ
0743  01176 102000        HLT 0           E NOT 0
0744  01177 102301        SOS
0745  01200 102000        HLT 0           OV NOT 1
0746*
0747  01201 000040        CLE
0748  01202 103101        CLO
0749  01203 065634        LDB PMAX        ADD 077777 + 000001
0750  01204 045630        ADB .1
0751  01205 055635        CPB BIT15
0752  01206 002001        RSS
0753  01207 102000        HLT 0           SUM NOT 100000
0754  01210 002040        SEZ
0755  01211 102000        HLT 0           E NOT 0
```

```
0756  01212 102301        SOS
0757  01213 102000        HLT 0           OV NOT 1
0758*
0759  01214 000040        CLE
0760  01215 103101        CLO
0761  01216 065625        LDB M1          ADD 177777 + 177777
0762  01217 045625        ADB M1
0763  01220 055626        CPB M2
0764  01221 002001        RSS
0765  01222 102000        HLT 0           SUM NOT 177776
0766  01223 002041        SEZ,RSS
0767  01224 102000        HLT 0           E NOT 1
0768  01225 102201        SOC
0769  01226 102000        HLT 0           OV NOT 0
0770*
0771  01227 000040        CLE
0772  01230 103101        CLO
0773  01231 065625        LDB M1          ADD 177777 + 000001
0774  01232 045630        ADB .1
0775  01233 006002        SZB
0776  01234 102000        HLT 0           SUM NOT 000000
0777  01235 002041        SEZ,RSS
0778  01236 102000        HLT 0           E NOT 1
0779  01237 102201        SOC
0780  01240 102000        HLT 0           OV NOT 0
0781*
0782  01241 000040        CLE
0783  01242 103101        CLO
0784  01243 065635        LDB BIT15       ADD 100000 + 100000
0785  01244 045635        ADB BIT15
0786  01245 006002        SZB
0787  01246 102000        HLT 0           SUM NOT 000000
0788  01247 002041        SEZ,RSS
0789  01250 102000        HLT 0           E NOT 1
0790  01251 102301        SOS
0791  01252 102000        HLT 0           OV NOT 1
0792*
0793  01253 000040        CLE
0794  01254 103101        CLO
0795  01255 065635        LDB BIT15       ADD 100000 + 077777
0796  01256 045634        ADB PMAX
0797  01257 055625        CPB M1
0798  01260 002001        RSS
0799  01261 102000        HLT 0           SUM NOT 177777
0800  01262 002040        SEZ
0801  01263 102000        HLT 0           E NOT 0
0802  01264 102201        SOC
0803  01265 102000        HLT 0           OV NOT 0
0804*
0805  01266 002300        CCE             E ← 1
0806  01267 102101        STO             OV ← 1
0807  01270 065630        LDB .1
0808  01271 045630        ADB .1
0809  01272 002041        SEZ,RSS
0810  01273 102000        HLT 0           E NOT 1
0811  01274 102301        SOS
```



```
0812  01275 102000        HLT 0           OV NOT 1
0813*
0814  01276 000000        NOP ***** MODULE LOOP
```

```
0816* CHECK JMP INDIRECT
0817*
0818  01277 125653        JMP IA1,I     IA1 = DEF IR1
0819  01300 102000        HLT 0         JMP,I FAILED - 1 INDIRECT LEVEL
0820*
0821  01301 125654  IR1   JMP IA2,I
0822  01302 102000        HLT 0         JMP,I FAILED - 2 INDIRECT LEVELS
0823*
0824* CHECK JSB INDIRECT
0825*
0826  01303 002400  IR2   CLA
0827  01304 071307        STA RA3       RA3 ← NOP
0828  01305 115656        JSB IA3,I     IA3 = DEF RA3
0829  01306 102000        HLT 0         JSB,I FAILED - 1 INDIRECT LEVEL
0830  01307 000000  RA3   NOP
0831  01310 061307        LDA RA3
0832  01311 051650        CPA ADDR2     ADDR2 = DEF RA3-1
0833  01312 002001        RSS
0834  01313 102000        HLT 0         JSB,I FAILED - BAD RETURN ADDR.
0835*
0836  01314 002400        CLA
0837  01315 071320        STA RA4       RA4 ← NOP
0838  01316 115657        JSB IA4,I
0839  01317 102000        HLT 0         JSB,I FAILED - 2 INDIRECT LEVELS
0840  01320 000000  RA4   NOP
0841  01321 061320        LDA RA4
0842  01322 051651        CPA ADDRY     ADDRY = DEF RA4-1
0843  01323 002001        RSS
0844  01324 102000        HLT 0         JSB,I FAILED - BAD RETURN ADDR.
0845*
0846* CHECK LDA INDIRECT
0847*
0848  01325 002400        CLA
0849  01326 161661        LDA IA5,I     IA5 = DEF M1,  M1 = 177777
0850  01327 051625        CPA M1
0851  01330 002001        RSS
0852  01331 102000        HLT 0         LDA,I FAILED - 1 INDIRECT LEVEL
0853*
0854  01332 002400        CLA
0855  01333 161662        LDA IA6,I     IA6 = DEF IA5,I
0856  01334 051625        CPA M1
0857  01335 002001        RSS
0858  01336 102000        HLT 0         LDA,I FAILED - 2 INDIRECT LEVELS
0859*
0860* CHECK LDB INDIRECT
0861*
0862  01337 006400        CLB
0863  01340 165661        LDB IA5,I     IA5 = DEF M1, M1 = 177777
0864  01341 055625        CPB M1
0865  01342 002001        RSS
0866  01343 102000        HLT 0         LDB,I FAILED - 1 INDIRECT LEVEL
0867*
0868  01344 006400        CLB
0869  01345 165662        LDB IA6,I     IA6 = DEF IA5,I
0870  01346 055625        CPB M1
0871  01347 002001        RSS
```



```
0872  01350 102000        HLT 0         LDB,I FAILED - 2 INDIRECT LEVELS
0873*
0874* CHECK CPA INDIRECT
0875*
0876  01351 061631        LDA EVEN1     EVEN1 = 052525
0877  01352 151663        CPA IA7,I     IA7 = DEF EVEN1
0878  01353 002001        RSS
0879  01354 102000        HLT 0         CPA,I FAILED - 1 INDIRECT LEVEL
0880*
0881  01355 061631        LDA EVEN1
0882  01356 151664        CPA IA8,I     IA8 = DEF IA7,I
0883  01357 002001        RSS
0884  01360 102000        HLT 0         CPA,I FAILED - 2 INDIRECT LEVELS
0885*
0886* CHECK CPB INDIRECT
0887*
0888  01361 065631        LDB EVEN1     EVEN1 = 052525
0889  01362 155663        CPB IA7,I     IA7 = DEF EVEN1
0890  01363 002001        RSS
0891  01364 102000        HLT 0         CPB,I FAILED - 1 INDIRECT LEVEL
0892*
0893  01365 065631        LDB EVEN1
0894  01366 155664        CPB IA8,I     IA8 = DEF IA7,I
0895  01367 002001        RSS
0896  01370 102000        HLT 0         CPB,I FAILED - 2 INDIRECT LEVELS
0897*
0898* CHECK STA INDIRECT
0899*
0900  01371 003400        CCA           A ← 177777
0901  01372 171665        STA IA9,I     IA9 = DEF T1
0902  01373 051640        CPA T1
0903  01374 002001        RSS
0904  01375 102000        HLT 0         STA,I FAILED - 1 INDIRECT LEVEL
0905*
0906  01376 002400        CLA           A ← 000000
0907  01377 171666        STA IA10,I    IA10 = DEF IA9,I
0908  01400 051640        CPA T1
0909  01401 002001        RSS
0910  01402 102000        HLT 0         STA,I FAILED - 2 INDIRECT LEVELS
0911*
0912* CHECK STB INDIRECT
0913*
0914  01403 007400        CCB           B ← 177777
0915  01404 175665        STB IA9,I     IA9 = DEF T1
0916  01405 055640        CPB T1
0917  01406 002001        RSS
0918  01407 102000        HLT 0         STB,I FAILED - 1 INDIRECT LEVEL
0919*
0920  01410 006400        CLB           B ← 000000
0921  01411 175666        STB IA10,I    IA9 = DEF T1
0922  01412 055640        CPB T1
0923  01413 002001        RSS
0924  01414 102000        HLT 0         STB,I FAILED - 2 INDIRECT LEVELS
0925*
0926* CHECK ADA INDIRECT
0927*
```

```
0928  01415 061631        LDA EVEN1     EVEN1 = 052525
0929  01416 141663        ADA IA7,I     IA7 = DEF EVEN1
0930  01417 051632        CPA ODD1      EXPECT A = 125252
0931  01420 002001        RSS
0932  01421 102000        HLT 0         ADA,I FAILED - 1 INDIRECT LEVEL
0933*
0934  01422 061631        LDA EVEN1
0935  01423 141664        ADA IA8,I     IA8 = DEF IA7,I
0936  01424 051632        CPA ODD1
0937  01425 002001        RSS
0938  01426 102000        HLT 0         ADA,I FAILED - 2 INDIRECT LEVELS
0939*
0940* CHECK ADB INDIRECT
0941*
0942  01427 065631        LDB EVEN1     EVEN1 = 052525
0943  01430 145663        ADB IA7,I     IA7 = DEF EVEN1
0944  01431 055632        CPB ODD1      EXPECT B = 125252
0945  01432 002001        RSS
0946  01433 102000        HLT 0         ADB,I FAILED - 1 INDIRECT LEVEL
0947*
0948  01434 065631        LDB EVEN1
0949  01435 145664        ADB IA8,I     IA8 = DEF IA7,I
0950  01436 055632        CPB ODD1
0951  01437 002001        RSS
0952  01440 102000        HLT 0         ADB,I FAILED - 2 INDIRECT LEVELS
0953*
0954* CHECK AND INDIRECT
0955*
0956  01441 003400        CCA
0957  01442 111663        AND IA7,I     IA7 = DEF EVEN1
0958  01443 051631        CPA EVEN1
0959  01444 002001        RSS
0960  01445 102000        HLT 0         AND,I FAILED - 1 INDIRECT LEVEL
0961*
0962  01446 003400        CCA
0963  01447 111664        AND IA8,I     IA8 = DEF EVEN1
0964  01450 051631        CPA EVEN1
0965  01451 002001        RSS
0966  01452 102000        HLT 0         AND,I FAILED - 2 INDIRECT LEVELS
0967*
0968* CHECK IOR INDIRECT
0969*
0970  01453 002400        CLA
0971  01454 131663        IOR IA7,I     IA7 = DEF EVEN1
0972  01455 051631        CPA EVEN1
0973  01456 002001        RSS
0974  01457 102000        HLT 0         IOR,I FAILED - 1 INDIRECT LEVEL
0975*
0976  01460 002400        CLA
0977  01461 131664        IOR IA8,I     IA8 = DEF IA7,I
0978  01462 051631        CPA EVEN1
0979  01463 002001        RSS
0980  01464 102000        HLT 0         IOR,I FAILED - 2 INDIRECT LEVELS
0981*
0982* CHECK XOR INDIRECT
0983*
```



```
0984  01465 003400        CCA
0985  01466 121663        XOR IA7,I     IA7 = DEF EVEN1
0986  01467 051632        CPA ODD1
0987  01470 002001        RSS
0988  01471 102000        HLT 0         XOR,I FAILED - 1 INDIRECT LEVEL
0989*
0990  01472 003400        CCA
0991  01473 121664        XOR IA8,I     IA8 = DEF IA7,I
0992  01474 051632        CPA ODD1
0993  01475 002001        RSS
0994  01476 102000        HLT 0         XOR,I FAILED - 2 INDIRECT LEVELS
0995*
0996* CHECK ISZ INDIRECT
0997*
0998  01477 003400        CCA
0999  01500 071640        STA T1        T1 = 177777
1000  01501 135665        ISZ IA9,I     IA9 = DEF T1
1001  01502 102000        HLT 0         ISZ,I FAILED - 1 INDIRECT LEVEL
1002  01503 061640        LDA T1
1003  01504 002002        SZA
1004  01505 102000        HLT 0         ISZ,I FAILED - 1 INDIRECT LEVEL
1005*
1006  01506 003400        CCA
1007  01507 071640        STA T1        T1 = 177777
1008  01510 135666        ISZ IA10,I    IA10 = DEF IA9,I
1009  01511 102000        HLT 0         ISZ,I FAILED - 2 INDIRECT LEVELS
1010  01512 061640        LDA T1
1011  01513 002002        SZA
1012  01514 102000        HLT 0         ISZ,I FAILED - 2 INDIRECT LEVELS
1013*
1014  01515 000000        NOP ***** MODULE LOOP
```

```
1016  01516 161676        LDA .P1,I      .P1 = DEF TBL,1,  TBL,1 = 015366
1017  01517 051700        CPA K10        K10 = 015366
1018  01520 002001        RSS
1019  01521 102000        HLT 0          LDA,I FAILED
1020*
1021  01522 165677        LDB .P2,I      .P2 = DEF TBL,2,  TBL,2 = 051463
1022  01523 055701        CPB K11        K11 = 051463
1023  01524 002001        RSS
1024  01525 102000        HLT 0          LDB,I FAILED
1025*
1026  01526 061701        LDA K11        K11 = 051463
1027  01527 151677        CPA .P2,I      .P2 = DEF TBL,2,  TBL,2 = 051463
1028  01530 002001        RSS
1029  01531 102000        HLT 0          CPA,I FAILED
1030*
1031  01532 065700        LDB K10        K10 = 015366
1032  01533 155676        CPB .P1,I      .P1 = DEF TBL,1,  TBL,1 = 015366
1033  01534 002001        RSS
1034  01535 102000        HLT 0          CPB,I FAILED
1035*
1036  01536 003400        CCA
1037  01537 171703        STA T2A,I      T2A = DEF T2
1038  01540 151703        CPA T2A,I
1039  01541 002001        RSS
1040  01542 102000        HLT 0          STA,I/CPA,I FAILED
1041*
1042  01543 065631        LDB EVEN1      EVEN1 = 052525
1043  01544 175703        STB T2A,I
1044  01545 155703        CPB T2A,I
1045  01546 002001        RSS
1046  01547 102000        HLT 0          STB,I/CPB,I FAILED
1047*
1048  01550 003400        CCA
1049  01551 171703        STA T2A,I      T2A = DEF T2
1050  01552 135703        ISZ T2A,I
1051  01553 102000        HLT 0          ISZ,I FAILED - DID NOT SKIP
1052  01554 161703        LDA T2A,I
1053  01555 002002        SZA
1054  01556 102000        HLT 0          ISZ,I FAILED - T2 NOT 0
1055*
1056  01557 002400        CLA
1057  01560 131676        IOR .P1,I      .P1 = DEF TBL,1,  TBL,1 = 015366
1058  01561 051700        CPA K10        K10 = 015366
1059  01562 002001        RSS
1060  01563 102000        HLT 0          IOR,I FAILED
1061*
1062  01564 003400        CCA
1063  01565 121676        XOR .P1,I      .P1 = DEF TBL,1,  TBL,1 = 015366
1064  01566 051702        CPA K12        K12 = 162411
1065  01567 002001        RSS
1066  01570 102000        HLT 0          XOR,I FAILED
1067*
1068  01571 003400        CCA
1069  01572 111676        AND .P1,I      .P1 = DEF TBL,1,  TBL,1 = 015366
1070  01573 051700        CPA K10        K10 = 015366
1071  01574 002001        RSS
```



```
1072  01575 102000        HLT 0          AND,I FAILED
1073*
1074  01576 002400        CLA
1075  01577 141677        ADA .P2,I      .P2 = DEF TBL,2,  TBL,2 = 051463
1076  01600 051701        CPA K11        K11 = 051463
1077  01601 002001        RSS
1078  01602 102000        HLT 0          ADA,I FAILED
1079*
1080  01603 006400        CLB
1081  01604 145676        ADB .P1,I      .P1 = DEF TBL,1,  TBL,1 = 015366
1082  01605 055700        CPB K10        K10 = 015366
1083  01606 002001        RSS
1084  01607 102000        HLT 0          ADB,I FAILED
1085*
1086  01610 125704        JMP JMP1A,I    JMP TO JMP1(INDIRECT), THEN JMP2
1087  01611 102000        HLT 0          JMP,I FAILED
1088*
1089  01612 002400  JMP2  CLA
1090  01613 171705        STA SR1A,I     SR1A = DEF SR1  < SR1 ← NOP>
1091  01614 115705        JSB SR1A,I
1092  01615 102000  .P3    HLT 0          JSB,I FAILED
1093  01616 161705  .P4    LDA SR1A,I
1094  01617 051706        CPA .ADR3      .ADR3 = DEF .P3
1095  01620 002001        RSS
1096  01621 102000        HLT 0          JSB,I FAILED - BAD RETURN ADDRES
1097*
1098  01622 000000        NOP ***** MODULE LOOP


1100  01623 025777        JMP PG1        GOTO END OF PAGE 0
1101  01624 102000        HLT 0          JMP FAILED


1103  01625 177777  M1    DEC -1
1104  01626 177776  M2    DEC -2
1105  01627 000000  .0    DEC 0
1106  01630 000001  .1    DEC 1
1107  01631 052525  EVEN1 OCT 52525      ALL EVEN BITS 1'S
1108  01632 125252  ODD1  OCT 125252     ALL ODD BITS 1'S
1109  01633 052524  K1    OCT 52524
1110  01634 077777  PMAX  OCT 77777
1111  01635 100000  BIT15 OCT 100000
1112  01636 102000  HLT0  HLT 0
1113  01637 107077  H7077 OCT 107077
1114  01640 000000  T1    NOP            TEMPORARY STORAGE
1115  01641 000453  ADDR1 DEF X1
1116  01642 000531  ADDR3 DEF P3
1117  01643 000542  ADDR4 DEF P4
1118  01644 024522  JR1   JMP RTN1
1119  01645 024526  JR2   JMP RTN2
1120  01646 024532  JR3   JMP RTN3
1121  01647 024543  JR4   JMP RTN4
1122  00000         A     EQU 0          A REGISTER
1123  00001         B     EQU 1          B REGISTER
```

PAGE 0027 #01 INDIRECT ADDRESSING TO PAGE 1

```
1124*
1125  01650 001306  ADDR2 DEF RA3-1
1126  01651 001317  ADDRY DEF RA4-1
1127  01652 003217  ADDR7 DEF Z1
1128  01653 001301  IA1   DEF IR1
1129  01654 101655  IA2   DEF *+1,I
1130  01655 001303        DEF IR2
1131  01656 001307  IA3   DEF RA3
1132  01657 101660  IA4   DEF *+1,I
1133  01660 001320        DEF RA4
1134  01661 001625  IA5   DEF M1
1135  01662 101661  IA6   DEF IA5,I
1136  01663 001631  IA7   DEF EVEN1
1137  01664 101663  IA8   DEF IA7,I
1138  01665 001640  IA9   DEF T1
1139  01666 101665  IA10  DEF IA9,I
1140  01667 034075  K7    DEC 14397
1141*
1142  01670 002542  IR11  DEF RA11
1143  01671 002545  IR12  DEF RA12
1144  01672 002552  IR13  DEF X13
1145  01673 002567  IR14  DEF X14
1146  01674 002551  ADR13 DEF P13
1147  01675 002566  ADR14 DEF P14
1148*
1149  01676 003400  .P1   DEF TBL,1
1150  01677 003406  .P2   DEF TBL,2
1151  01700 015366  K10   OCT 015366
1152  01701 051463  K11   OCT 051463
1153  01702 162411  K12   OCT 162411
1154  01703 003475  T2A   DEF T2
1155  01704 003500  JMP1A DEF JMP1
1156  01705 003476  SR1A  DEF SR1
1157  01706 001615  .ADR3 DEF .P3
1158  01707 002223  P99A  DEF P99
1159  01710 000002  FCA   DEF 2          FIRST CORE ADDRESS
1160  01711 003677  LCA   DEF 3677B      LAST CORE ADDRESS (2K)
1161*
1162  01712 000000  JSB7  NOP            SUBROUTINE FROM PAGE 1
1163  01713 125715        JMP *+2,I      RETURN TO PAGE 1
1164  01714 102000        HLT 0          JMP,I FAILED
1165  01715 002066        DEF P9
1166  01716 125720  JMP5  JMP *+2,I      GO BACK TO PAGE 1
1167  01717 102000        HLT 0          JMP
1168  01720 002062        DEF P6



1170  01777               ORG 1777B
1171  01777 000000  PG1   NOP
```

PAGE 0028 #01 INDIRECT ADDRESSING TO BASE PAGE

```
1173  02000 163371        LDA K11A,I   K11 = DEF K11,  K11 = 051463
1174  02001 053406        CPA TBL,2     TBL,2 = 051463
1175  02002 002001        RSS
1176  02003 102000        HLT 0         LDA,I FAILED
1177*
1178  02004 167370        LDB K10A,I    K10A, = DEF K10,  K10 = 015366
1179  02005 057400        CPB TBL,1     TBL,1 = 015366
1180  02006 002001        RSS
1181  02007 102000        HLT 0         LDB,I FAILED
1182*
1183  02010 063400        LDA TBL,1     TBL,1 = 015366
1184  02011 153370        CPA K10A,I    K10A = DEF K10, K10 = 015366
1185  02012 002001        RSS
1186  02013 102000        HLT 0         CPA,I FAILED
1187*
1188  02014 067406        LDB TBL,2     TBL,2 = 051463
1189  02015 157371        CPB K11A,I    K11A = DEF K11,  K11 = 051463
1190  02016 002001        RSS
1191  02017 102000        HLT 0         CPB,I FAILED
1192*
1193  02020 061631        LDA EVEN1
1194  02021 173372        STA T1A,I     T1A = DEF T1
1195  02022 051640        CPA T1
1196  02023 002001        RSS
1197  02024 102000        HLT 0         STA,I/CPA FAILED
1198*
1199  02025 065632        LDB ODD1
1200  02026 177372        STB T1A,I     T1A = DEF T1
1201  02027 055640        CPB T1
1202  02030 002001        RSS
1203  02031 102000        HLT 0         STB,I/CPB FAILED
1204*
1205  02032 003400        CCA
1206  02033 071640        STA T1
1207  02034 137372        ISZ T1A,I     T1A = DEF T1
1208  02035 102000        HLT 0         ISZ,I FAILED - DID NOT SKIP
1209  02036 061640        LDA T1
1210  02037 002002        SZA
1211  02040 102000        HLT 0         ISZ,I FAILED - T1 NOT 0
1212*
1213  02041 002400        CLA
1214  02042 133371        IOR K11A,I    K11A = DEF K11,  K11 = 051463
1215  02043 053406        CPA TBL,2     TBL,2 = 051463
1216  02044 002001        RSS
1217  02045 102000        HLT 0         IOR,I FAILED
1218*
1219  02046 003400        CCA
1220  02047 123373        XOR K12A,I    K12A = DEF K12,  K12 = 162411
1221  02050 053400        CPA TBL,1
1222  02051 002001        RSS
1223  02052 102000        HLT 0         XOR,I FAILED
1224*
1225  02053 003400        CCA
1226  02054 113370        AND K10A,I    K10A = DEF K10,  K10 = 015366
1227  02055 053400        CPA TBL,1     TBL,1 = 015366
1228  02056 002001        RSS
```

```
1229  02057 102000        HLT 0          AND,I FAILED
1230*
1231  02060 127374        JMP JMP5A,I    JMP5A = DEF JMP5
1232  02061 102000        HLT 0          JMP,I FAILED
1233*
1234  02062 002400  P6    CLA
1235  02063 071712        STA JSB7       JSB7 = NOP
1236  02064 117375        JSB JSB7A,I    JSB7A = DEF JSB7
1237  02065 102000  P7    HLT 0          JSB,I FAILED
1238  02066 061712  P9    LDA JSB7
1239  02067 053376        CPA P7A        P7A = DEF P7
1240  02070 002001        RSS
1241  02071 102000        HLT 0          JSB,I FAILED - BAD RETURN ADDRES
1242*
1243  02072 000000        NOP ***** MODULE LOOP
```



```
1245* THIS SECTION CHECKS THAT ALL OTHER REGISTERS REMAIN UNCHANGED
1246* WHEN A MEMORY REFERENCE INSTRUCTION IS EXECUTED.
1247*
1248  02073 006400        CLB
1249  02074 000040        CLE
1250  02075 103101        CLO
1251  02076 061625        LDA M1         M1 = 177777
1252  02077 006002        SZB
1253  02100 102000        HLT 0          LDA - B CHANGED
1254  02101 002040        SEZ
1255  02102 102000        HLT 0          LDA - E CHANGED
1256  02103 102201        SOC
1257  02104 102000        HLT 0          LDA - OV CHANGED
1258  02105 051625        CPA M1
1259  02106 002001        RSS
1260  02107 102000        HLT 0          CPA FAILED
1261  02110 006002        SZB
1262  02111 102000        HLT 0          CPA - B CHANGED
1263  02112 002040        SEZ
1264  02113 102000        HLT 0          CPA - E CHANGED
1265  02114 102201        SOC
1266  02115 102000        HLT 0          CPA - OV CHANGED
1267*
1268  02116 002400        CLA
1269  02117 000040        CLE
1270  02120 103101        CLO
1271  02121 065631        LDB EVEN1      EVEN1 = 052525
1272  02122 002002        SZA
1273  02123 102000        HLT 0          LDB - A CHANGED
1274  02124 002040        SEZ
1275  02125 102000        HLT 0          LDB - E CHANGED
1276  02126 102201        SOC
1277  02127 102000        HLT 0          LDB - OV CHANGED
1278  02130 055631        CPB EVEN1
1279  02131 002001        RSS
1280  02132 102000        HLT 0          CPB FAILED
1281  02133 002002        SZA
1282  02134 102000        HLT 0          CPB - A CHANGED
1283  02135 002040        SEZ
1284  02136 102000        HLT 0          CPB - E CHANGED
1285  02137 102201        SOC
1286  02140 102000        HLT 0          CPB - OV CHANGED
1287*
1288  02141 061632        LDA ODD1       ODD1 = 125252
1289  02142 007400        CCB
1290  02143 002300        CCE
1291  02144 103101        STO
1292  02145 071640        STA T1
1293  02146 002041        SEZ,RSS
1294  02147 102000        HLT 0          STA - E CHANGED
1295  02150 102301        SOS
1296  02151 102000        HLT 0          STA - OV CHANGED
1297  02152 055625        CPB M1
1298  02153 002001        RSS
1299  02154 102000        HLT 0          STA - B CHANGED
1300  02155 051640        CPA T1
```

```
1301  02156 002001        RSS
1302  02157 102000        HLT 0           STA FAILED
1303*
1304  02160 065631        ISB EVEN1       EVEN1 = 052525
1305  02161 002400        CLA
1306  02162 000040        CLE
1307  02163 103101        CLO
1308  02164 075640        STB T1
1309  02165 002002        SZA
1310  02166 102000        HLT 0           STB = CHANGED
1311  02167 002040        SEZ
1312  02170 102000        HLT 0           STB = E CHANGED
1313  02171 102201        SOC
1314  02172 102000        HLT 0           STB = OV CHANGED
1315  02173 055640        CPB T1
1316  02174 002001        RSS
1317  02175 102000        HLT 0           STB FAILED
1318*
1319  02176 103101        CLO
1320  02177 000040        CLE
1321  02200 002400        CLA
1322  02201 006400        CLB
1323  02202 026204        JMP *+2
1324  02203 102000        HLT 0           JMP FAILED
1325  02204 002002        SZA
1326  02205 102000        HLT 0           JMP = A CHANGED
1327  02206 006002        SZB
1328  02207 102000        HLT 0           JMP = B CHANGED
1329  02210 002040        SEZ
1330  02211 102000        HLT 0           JMP = E CHANGED
1331  02212 102201        SOC
1332  02213 102000        HLT 0           JMP = OV CHANGED
1333*
1334  02214 002400        CLA
1335  02215 072224        STA X99         X99 ← NOP
1336  02216 003400        CCA
1337  02217 007400        CCB
1338  02220 102101        STO
1339  02221 002300        CCE
1340  02222 016224        JSB *+2
1341  02223 102000  P99    HLT 0          JSB FAILED
1342  02224 000000  X99    NOP
1343  02225 002041        SEZ,RSS
1344  02226 102000        HLT 0           JSB = E CHANGED
1345  02227 102301        SOS
1346  02230 102000        HLT 0           JSB = OV CHANGED
1347  02231 051625        CPA M1
1348  02232 002001        RSS
1349  02233 102000        HLT 0           JSB = A CHANGED
1350  02234 055625        CPB M1
1351  02235 002001        RSS
1352  02236 102000        HLT 0           JSB = B CHANGED
1353  02237 062224        LDA X99
1354  02240 051707        CPA P99A        P99A = DEF P99
1355  02241 002001        RSS
1356  02242 102000        HLT 0           JSB = BAD RETURN ADDRESS
```



```
1357*
1358  02243 002400        CLA
1359  02244 006400        CLB
1360  02245 041625        ADA M1          < E, OV, A CHECKED ELSEWHERE>
1361  02246 006002        SZB
1362  02247 102000        HLT 0           ADA = B CHANGED
1363*
1364  02250 002400        CLA
1365  02251 006400        CLB
1366  02252 045632        ADB ODD1        < E, OV, B CHECKED ELSEWHERE>
1367  02253 002002        SZA
1368  02254 102000        HLT 0           ADB = A CHANGED
1369*
1370  02255 002400        CLA
1371  02256 006400        CLB
1372  02257 103101        CLO
1373  02260 000040        CLE
1374  02261 031631        IOR EVEN1       EVEN1 = 052525
1375  02262 021632        XOR ODD1        ODD1 = 125252
1376  02263 011625        AND M1          M1 = 177777
1377  02264 006002        SZB
1378  02265 102000        HLT 0           IOR OR XOR OR AND = B CHANGED
1379  02266 102201        SOC
1380  02267 102000        HLT 0           IOR OR XOR OR AND = OV CHANGED
1381  02270 002040        SEZ
1382  02271 102000        HLT 0           IOR OR XOR OR AND = E CHANGED
1383  02272 051625        CPA M1
1384  02273 002001        RSS
1385  02274 102000        HLT 0           IOR/XOR/AND = RESULT NOT 177777
1386*
1387  02275 003400        CCA
1388  02276 071640        STA T1          T1 ← 177777
1389  02277 002400        CLA
1390  02300 006400        CLB
1391  02301 000040        CLE
1392  02302 103101        CLO
1393  02303 035640        ISZ T1
1394  02304 102000        HLT 0           ISZ FAILED = DID NOT SKIP
1395  02305 002002        SZA
1396  02306 102000        HLT 0           ISZ = A CHANGED
1397  02307 006002        SZB
1398  02310 102000        HLT 0           ISZ = B CHANGED
1399  02311 002040        SEZ
1400  02312 102000        HLT 0           ISZ = E CHANGED
1401  02313 102201        SOC
1402  02314 102000        HLT 0           ISZ = OV CHANGED
1403*
1404  02315 000000        NOP ***** MODULE LOOP
```

```
1406  02316 061661        LDA IA5       IA5 = DEF M1,  M1 = 177777
1407  02317 160000        LDA A,I
1408  02320 051625        CPA M1
1409  02321 002001        RSS
1410  02322 102000        HLT 0         LDA A,I FAILED
1411*
1412  02323 065663        LDB IA7       IA7 = DEF EVEN1,  EVEN1 = 052525
1413  02324 160001        LDA B,I
1414  02325 051631        CPA EVEN1
1415  02326 002001        RSS
1416  02327 102000        HLT 0         LDA B,I FAILED
1417*
1418  02330 065661        LDB IA5       IA5 = DEF M1,  M1 = 177777
1419  02331 164001        LDB B,I
1420  02332 055625        CPB M1
1421  02333 002001        RSS
1422  02334 102000        HLT 0         LDB B,I FAILED
1423*
1424  02335 061663        LDA IA7       IA7 = DEF EVEN1,  EVEN1 = 052525
1425  02336 164000        LDB A,I
1426  02337 055631        CPB EVEN1
1427  02340 002001        RSS
1428  02341 102000        HLT 0         LDB A,I FAILED
1429*
1430  02342 006400        CLB
1431  02343 075640        STB T1        T1 ← 0
1432  02344 061665        LDA IA9       IA9 = DEF T1
1433  02345 170000        STA A,I
1434  02346 065640        LDB T1
1435  02347 055640        CPB T1
1436  02350 002001        RSS
1437  02351 102000        HLT 0         STA A,I FAILED
1438*
1439  02352 002400        CLA
1440  02353 071640        STA T1        T1 ← 0
1441  02354 065665        LDB IA9       IA9 = DEF T1
1442  02355 174001        STB B,I
1443  02356 061640        LDA T1
1444  02357 051640        CPA T1
1445  02360 002001        RSS
1446  02361 102000        HLT 0         STB B,I FAILED
1447*
1448  02362 002400        CLA
1449  02363 071640        STA T1        T1 ← 0
1450  02364 003400        CCA           A ← 177777
1451  02365 065665        LDB IA9       IA9 = DEF T1
1452  02366 170001        STA B,I
1453  02367 065640        LDB T1
1454  02370 055625        CPB M1
1455  02371 002001        RSS
1456  02372 102000        HLT 0         STA B,I FAILED
1457*
1458  02373 006400        CLB
1459  02374 075640        STB T1        T1 ← 0
1460  02375 007400        CCB           B ← 177777
1461  02376 061665        LDA IA9       IA9 = DEF T1
```



```
1462  02377 174000        STB A,I
1463  02400 061640        LDA T1
1464  02401 051625        CPA M1
1465  02402 002001        RSS
1466  02403 102000        HLT 0         STB A,I FAILED
1467*
1468  02404 061665        LDA IA9       IA9 = DEF T1
1469  02405 071640        STA T1
1470  02406 150000        CPA A,I
1471  02407 002001        RSS
1472  02410 102000        HLT 0         CPA A,I FAILED
1473  02411 065665        LDB IA9       IA9 = DEF T1
1474  02412 075640        STB T1
1475  02413 154001        CPB B,I
1476  02414 002001        RSS
1477  02415 102000        HLT 0         CPB B,I FAILED
1478*
1479  02416 061665        LDA IA9       IA9 = DEF T1
1480  02417 071640        STA T1
1481  02420 065665        LDB IA9
1482  02421 150001        CPA B,I
1483  02422 002001        RSS
1484  02423 102000        HLT 0         CPA B,I FAILED
1485  02424 154000        CPB A,I
1486  02425 002001        RSS
1487  02426 102000        HLT 0         CPB A,I FAILED
1488*
1489  02427 061663        LDA IA7       IA7 = DEF EVEN1
1490  02430 041631        ADA EVEN1     EVEN1 = 052525
1491  02431 071640        STA T1
1492  02432 061663        LDA IA7
1493  02433 140000        ADA A,I
1494  02434 051640        CPA T1
1495  02435 002001        RSS
1496  02436 102000        HLT 0         ADA A,I FAILED
1497*
1498  02437 065661        LDB IA5       IA5 = DEF M1
1499  02440 045625        ADB M1        M1 = 177777
1500  02441 075640        STB T1
1501  02442 065661        LDB IA5
1502  02443 144001        ADB B,I
1503  02444 055640        CPB T1
1504  02445 002001        RSS
1505  02446 102000        HLT 0         ADB B,I FAILED
1506*
1507  02447 002400        CLA
1508  02450 065661        LDB IA5       IA5 = DEF M1,  M1 = 177777
1509  02451 140001        ADA B,I
1510  02452 051625        CPA M1
1511  02453 002001        RSS
1512  02454 102000        HLT 0         ADA B,I FAILED
1513*
1514  02455 006400        CLB
1515  02456 061663        LDA IA7       IA7 = DEF EVEN1,  EVEN1 = 052525
1516  02457 144000        ADB A,I
1517  02460 055631        CPB EVEN1
```

```
1518  02461 002001          RSS
1519  02462 102000          HLT 0           ADB A,I FAILED
1520*
1521  02463 061661          LDA IA5         IA5 = DEF M1,  M1 = 177777
1522  02464 130000          IOR A,I
1523  02465 051625          CPA M1
1524  02466 002001          RSS
1525  02467 102000          HLT 0           IOR A,I FAILED
1526*
1527  02470 002400          CLA
1528  02471 065663          LDB IA7         IA7 = DEF EVEN1,  EVEN1 = 052525
1529  02472 130001          IOR B,I
1530  02473 051631          CPA EVEN1
1531  02474 002001          RSS
1532  02475 102000          HLT 0           IOR B,I FAILED
1533*
1534  02476 061661          LDA IA5         IA5 = DEF M1, M1 = 177777
1535  02477 110000          AND A,I
1536  02500 051661          CPA IA5
1537  02501 002001          RSS
1538  02502 102000          HLT 0           AND A,I FAILED
1539*
1540  02503 061631          LDA EVEN1       EVEN1 = 052525
1541  02504 065661          LDB IA5         IA5 = DEF M1,  M1 = 177777
1542  02505 110001          AND B,I
1543  02506 051631          CPA EVEN1
1544  02507 002001          RSS
1545  02510 102000          HLT 0           AND B,I FAILED
1546*
1547* CHECK CMB INSTRUCTION BEFORE TESTING XOR A,I
1548*
1549  02511 065631          LDB EVEN1       B ← 052525
1550  02512 007000          CMB
1551  02513 055632          CPB ODD1
1552  02514 002001          RSS
1553  02515 102000          HLT 0           CMB FAILED
1554  02516 007000          CMB
1555  02517 055631          CPB EVEN1
1556  02520 002001          RSS
1557  02521 102000          HLT 0           CMB FAILED
1558*
1559  02522 065661          LDB IA5         IA5 = DEF M1,  M1 = 177777
1560  02523 007000          CMB
1561  02524 061661          LDA IA5
1562  02525 120000          XOR A,I
1563  02526 050001          CPA B
1564  02527 002001          RSS
1565  02530 102000          HLT 0           XOR A,I FAILED
1566*
1567  02531 061631          LDA EVEN1       EVEN1 = 052525
1568  02532 065661          LDB IA5         IA5 = DEF M1,  M1 = 177777
1569  02533 120001          XOR B,I
1570  02534 051632          CPA ODD1
1571  02535 002001          RSS
1572  02536 102000          HLT 0           XOR B,I FAILED
1573*
```



```
1574  02537 061670          LDA IR11        IR11 = DEF RA11
1575  02540 124000          JMP A,I
1576  02541 102000          HLT 0           JMP A,I FAILED
1577*
1578  02542 065671  RA11     LDB IR12        IR12 = DEF RA12
1579  02543 124001          JMP B,I
1580  02544 102000          HLT 0           JMP B,I FAILED
1581*
1582  02545 002400  RA12     CLA
1583  02546 072552          STA X13         X13 ← NOP
1584  02547 061672          LDA IR13        IR13 = DEF X13
1585  02550 114000          JSB A,I
1586  02551 102000  P13      HLT 0           JSB A,I FAILED
1587  02552 000000  X13      NOP
1588  02553 051672          CPA IR13
1589  02554 002001          RSS
1590  02555 102000          HLT 0           JSB A,I FAILED - A REG, CHANGED
1591  02556 065674          LDB ADR13       ADR13 = DEF P13
1592  02557 056552          CPB X13
1593  02560 002001          RSS
1594  02561 102000          HLT 0           JSB A,I FAILED - BAD RETURN ADDR
1595*
1596  02562 006400          CLB
1597  02563 076567          STB X14         X14 ← NOP
1598  02564 065673          LDB IR14        IR14 = DEF X14
1599  02565 114001          JSB B,I
1600  02566 102000  P14      HLT 0           JSB B,I FAILED
1601  02567 000000  X14      NOP
1602  02570 055673          CPB IR14
1603  02571 002001          RSS
1604  02572 102000          HLT 0           JSB B,I FAILED - B REG, CHANGED
1605  02573 065675          LDB ADR14       ADR14 = DEF P14
1606  02574 056567          CPB X14
1607  02575 002001          RSS
1608  02576 102000          HLT 0           JSB B,I FAILED - BAD RETURN ADDR
1609*
1610  02577 061633          LDA K1
1611  02600 071640          STA T1          T1 = K1 = 052524
1612  02601 061665          LDA IA9         IA9 = DEF T1
1613  02602 134000          ISZ A,I
1614  02603 002001          RSS
1615  02604 102000          HLT 0           ISZ A,I FAILED - IT SKIPPED
1616  02605 065640          LDB T1
1617  02606 055631          CPB EVEN1       EVEN1 = 052525
1618  02607 002001          RSS
1619  02610 102000          HLT 0           ISZ A,I FAILED - T1 NOT 052525
1620*
1621  02611 007400          CCB
1622  02612 075640          STB T1          T1 = 177777
1623  02613 065665          LDB IA9         IA9 = DEF M1,  M1 = 177777
1624  02614 134001          ISZ B,I
1625  02615 102000          HLT 0           ISZ B,I FAILED - DID NOT SKIP
1626  02616 061640          LDA T1
1627  02617 002002          SZA
1628  02620 102000          HLT 0           ISZ B,I FAILED - T1 NOT 0
1629*
```

```
1630  02621 000000          NOP ***** MODULE LOOP
```



```
1632* THESE TESTS TRY TO FIND INTERMITTANT ERRORS
1633*
1634* LDA/CPA ITERATIVE TESTS
1635*
1636  02622 006400          CLB
1637  02623 061631  LP1     LDA EVEN1       A=052525
1638  02624 051631          CPA EVEN1
1639  02625 002001          RSS
1640  02626 102000          HLT 0           LDA/CPA FAILED
1641  02627 034001          ISZ B
1642  02630 026623          JMP LP1
1643*
1644  02631 006400          CLB
1645  02632 061632  LP2     LDA ODD1        A=125252
1646  02633 051632          CPA ODD1
1647  02634 002001          RSS
1648  02635 102000          HLT 0           LDA/CPA FAILED
1649  02636 034001          ISZ B
1650  02637 026632          JMP LP2
1651*
1652* LDB/CPB ITERATIVE TESTS
1653*
1654  02640 002400          CLA
1655  02641 065631  LP3     LDB EVEN1       B=052525
1656  02642 055631          CPB EVEN1
1657  02643 002001          RSS
1658  02644 102000          HLT 0           LDB/CPB FAILED
1659  02645 034000          ISZ A
1660  02646 026641          JMP LP3
1661*
1662  02647 002400          CLA
1663  02650 065632  LP4     LDB ODD1        B=125252
1664  02651 055632          CPB ODD1
1665  02652 002001          RSS
1666  02653 102000          HLT 0           LDB/CPB FAILED
1667  02654 034000          ISZ A
1668  02655 026650          JMP LP4
1669*
1670* LDA/STA/CPA ITERATIVE TESTS
1671*
1672  02656 006400          CLB
1673  02657 061631  LP5     LDA EVEN1       A=052525
1674  02660 071640          STA T1
1675  02661 051640          CPA T1
1676  02662 002001          RSS
1677  02663 102000          HLT 0           LDA/STA/CPA FAILED
1678  02664 034001          ISZ B
1679  02665 026657          JMP LP5
1680*
1681  02666 006400          CLB
1682  02667 061632  LP6     LDA ODD1        A=125252
1683  02670 071640          STA T1
1684  02671 051640          CPA T1
1685  02672 002001          RSS
1686  02673 102000          HLT 0           LDA/STA/CPA FAILED
1687  02674 034001          ISZ B
```

```
1688  02675 026667          JMP LP6
1689*
1690* LDB/STB/CPB ITERATIVE TESTS
1691*
1692  02676 002400          CLA
1693  02677 065631  LP7     LDB EVEN1       B=052525
1694  02700 075640          STB T1
1695  02701 055640          CPB T1
1696  02702 002001          RSS
1697  02703 102000          HLT 0           LDB/STB/CPB FAILED
1698  02704 034000          ISZ A
1699  02705 026677          JMP LP7
1700*
1701  02706 002400          CLA
1702  02707 065632  LP8     LDB ODD1        B=125252
1703  02710 075640          STB T1
1704  02711 055640          CPB T1
1705  02712 002001          RSS
1706  02713 102000          HLT 0           LDB/STB/CPB FAILED
1707  02714 034000          ISZ A
1708  02715 026707          JMP LP8
1709*
1710* AND ITERATIVE TESTS
1711*
1712  02716 006400          CLB
1713  02717 061631  LP9     LDA EVEN1
1714  02720 011632          AND ODD1
1715  02721 002002          SZA
1716  02722 102000          HLT 0           AND FAILED
1717  02723 034001          ISZ B
1718  02724 026717          JMP LP9
1719*
1720  02725 006400          CLB
1721  02726 061631  LP10    LDA EVEN1
1722  02727 011631          AND EVEN1
1723  02730 051631          CPA EVEN1
1724  02731 002001          RSS
1725  02732 102000          HLT 0           AND FAILED
1726  02733 034001          ISZ B
1727  02734 026726          JMP LP10
1728*
1729  02735 006400          CLB
1730  02736 061632  LP11    LDA ODD1
1731  02737 011632          AND ODD1
1732  02740 051632          CPA ODD1
1733  02741 002001          RSS
1734  02742 102000          HLT 0           AND FAILED
1735  02743 034001          ISZ B
1736  02744 026736          JMP LP11
1737*
1738* IOR ITERATIVE TESTS
1739*
1740  02745 006400          CLB
1741  02746 061631  LP12    LDA EVEN1
1742  02747 031632          IOR ODD1
1743  02750 051625          CPA M1
```



```
1744  02751 002001          RSS
1745  02752 102000          HLT 0           IOR FAILED
1746  02753 034001          ISZ B
1747  02754 026746          JMP LP12
1748*
1749  02755 006400          CLB
1750  02756 061632  LP13    LDA ODD1
1751  02757 031631          IOR EVEN1
1752  02760 051625          CPA M1
1753  02761 002001          RSS
1754  02762 102000          HLT 0           IOR FAILED
1755  02763 034001          ISZ B
1756  02764 026756          JMP LP13
1757*
1758  02765 006400          CLB
1759  02766 061631  LP14    LDA EVEN1
1760  02767 031631          IOR EVEN1
1761  02770 051631          CPA EVEN1
1762  02771 002001          RSS
1763  02772 102000          HLT 0           IOR FAILED
1764  02773 034001          ISZ B
1765  02774 026766          JMP LP14
1766*
1767  02775 006400          CLB
1768  02776 061632  LP15    LDA ODD1
1769  02777 031632          IOR ODD1
1770  03000 051632          CPA ODD1
1771  03001 002001          RSS
1772  03002 102000          HLT 0
1773  03003 034001          ISZ B           IOR FAILED
1774  03004 026776          JMP LP15
1775*
1776* XOR ITERATIVE TESTS
1777*
1778  03005 006400          CLB
1779  03006 061631  LP16    LDA EVEN1
1780  03007 021631          XOR EVEN1
1781  03010 002002          SZA
1782  03011 102000          HLT 0           XOR FAILED
1783  03012 034001          ISZ B
1784  03013 027006          JMP LP16
1785*
1786  03014 006400          CLB
1787  03015 061632  LP17    LDA ODD1
1788  03016 021632          XOR ODD1
1789  03017 002002          SZA
1790  03020 102000          HLT 0           XOR FAILED
1791  03021 034001          ISZ B
1792  03022 027015          JMP LP17
1793*
1794  03023 006400          CLB
1795  03024 061631  LP18    LDA EVEN1
1796  03025 021632          XOR ODD1
1797  03026 051625          CPA M1
1798  03027 002001          RSS
1799  03030 102000          HLT 0           XOR FAILED
```

```
1800  03031 034001        ISZ B
1801  03032 027024        JMP LP18
1802*
1803* ADA ITERATIVE TESTS
1804*
1805  03033 006400        CLB
1806  03034 000040  LP19  CLE
1807  03035 103101        CLO
1808  03036 061631        LDA EVEN1
1809  03037 041632        ADA ODD1      052525 + 125252 = 177777
1810  03040 051625        CPA M1
1811  03041 002001        RSS
1812  03042 102000        HLT 0         SUM NOT 177777
1813  03043 002040        SEZ
1814  03044 102000        HLT 0         E NOT 0
1815  03045 102201        SOC
1816  03046 102000        HLT 0         OV NOT 0
1817  03047 034001        ISZ B
1818  03050 027034        JMP LP19
1819*
1820  03051 006400        CLB
1821  03052 102101  LP20  STO           OV=1
1822  03053 002300        CCE           E=1
1823  03054 061632        LDA ODD1
1824  03055 041631        ADA EVEN1     125252 + 052525 = 177777
1825  03056 051625        CPA M1
1826  03057 002001        RSS
1827  03060 102000        HLT 0         SUM NOT 177777
1828  03061 002041        SEZ,RSS
1829  03062 102000        HLT 0         E NOT 1
1830  03063 102301        SOS
1831  03064 102000        HLT 0         OV NOT 1
1832  03065 034001        ISZ B
1833  03066 027052        JMP LP20
1834*
1835  03067 006400        CLB
1836  03070 000040  LP21  CLE           E=0
1837  03071 103101        CLO           OV=1
1838  03072 061631        LDA EVEN1     052525 + 052525 = 125252
1839  03073 041631        ADA EVEN1
1840  03074 051632        CPA ODD1
1841  03075 002001        RSS
1842  03076 102000        HLT 0         SUM NOT 125252
1843  03077 002040        SEZ
1844  03100 102000        HLT 0         E NOT 0
1845  03101 102301        SOS
1846  03102 102000        HLT 0         OV NOT 1
1847  03103 034001        ISZ B
1848  03104 027070        JMP LP21
1849*
1850  03105 006400        CLB
1851  03106 000040  LP22  CLE           E=0
1852  03107 103101        CLO           OV=0
1853  03110 061632        LDA ODD1      125252 + 125252 = 052524
1854  03111 041632        ADA ODD1
1855  03112 051633        CPA K1
```



```
1856  03113 002001        RSS
1857  03114 102000        HLT 0         SUM NOT 052524
1858  03115 002041        SEZ,RSS
1859  03116 102000        HLT 0         E NOT 1
1860  03117 102301        SOS
1861  03120 102000        HLT 0         OV NOT 1
1862  03121 034001        ISZ B
1863  03122 027106        JMP LP22
1864*
1865* ADB ITERATIVE TESTS
1866*
1867  03123 002400        CLA
1868  03124 000040  LP23  CLE           E=0
1869  03125 103101        CLO           OV=0
1870  03126 065631        LDB EVEN1
1871  03127 045632        ADB ODD1      052525 + 125252 = 177777
1872  03130 055625        CPB M1
1873  03131 002001        RSS
1874  03132 102000        HLT 0         SUM NOT 177777
1875  03133 002040        SEZ
1876  03134 102000        HLT 0         E NOT 0
1877  03135 102201        SOC
1878  03136 102000        HLT 0         OV NOT 0
1879  03137 034000        ISZ A
1880  03140 027124        JMP LP23
1881*
1882  03141 002400        CLA
1883  03142 002300  LP24  CCE           E=1
1884  03143 102101        STO           OV=1
1885  03144 065632        LDB ODD1
1886  03145 045631        ADB EVEN1     125252 + 052525 = 177777
1887  03146 055625        CPB M1
1888  03147 002001        RSS
1889  03150 102000        HLT 0         SUM NOT 177777
1890  03151 002041        SEZ,RSS
1891  03152 102000        HLT 0         E NOT 1
1892  03153 102301        SOS
1893  03154 102000        HLT 0         OV NOT 1
1894  03155 034000        ISZ A
1895  03156 027142        JMP LP24
1896*
1897  03157 002400        CLA
1898  03160 000040  LP25  CLE           E=0
1899  03161 103101        CLO           OV=0
1900  03162 065631        LDB EVEN1
1901  03163 045631        ADB EVEN1     052525 + 052525 = 125252
1902  03164 055632        CPB ODD1
1903  03165 002001        RSS
1904  03166 102000        HLT 0         SUM NOT 125252
1905  03167 002040        SEZ
1906  03170 102000        HLT 0         E NOT 0
1907  03171 102301        SOS
1908  03172 102000        HLT 0         OV NOT 1
1909  03173 034000        ISZ A
1910  03174 027160        JMP LP25
1911*
```

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1912  03175 002400         CLA
1913  03176 000040  LP26    CLE             E=0
1914  03177 103101          CLO             OV=0
1915  03200 065632          LDB ODD1
1916  03201 045632          ADB ODD1        125252 + 125252 = 052524
1917  03202 055633          CPB K1
1918  03203 002001          RSS
1919  03204 102000          HLT 0           SUM NOT 052524
1920  03205 002041          SEZ,RSS
1921  03206 102000          HLT 0           E NOT 1
1922  03207 102301          SOS
1923  03210 102000          HLT 0           OV NOT 1
1924  03211 034000          ISZ A
1925  03212 027176          JMP LP26
1926*
1927* JSB ITERATIVE TEST
1928*
1929  03213 006400          CLB
1930  03214 002400  LP27    CLA
1931  03215 073220          STA Z2          Z2 ← NOP
1932  03216 017220          JSB **2         JSB FAILED - DID NOT JUMP
1933  03217 102000  Z1      HLT 0
1934  03220 000000  Z2      NOP
1935  03221 063220          LDA Z2
1936  03222 051652          CPA ADDR7       ADDR7 = ADDRESS Z1
1937  03223 002001          RSS
1938  03224 102000          HLT 0           JSB FAILED - BAD RETURN ADDRESS
1939  03225 034001          ISZ B
1940  03226 027214          JMP LP27
1941*
1942* ADA & ISZ ITERATIVE TEST
1943*
1944  03227 002400          CLA
1945  03230 071640          STA T1
1946  03231 041667          ADA K7          000000 + 034075 * 65K = 000000
1947  03232 035640          ISZ T1
1948  03233 027231          JMP *-2
1949  03234 002002          SZA
1950  03235 102000          HLT 0           ADA OR ISZ FAILED
1951*
1952* ADB & ISZ ITERATIVE TEST
1953*
1954  03236 006400          CLB
1955  03237 075640          STB T1
1956  03240 045667          ADB K7          000000 + (64K) * 034075 = 000000
1957  03241 035640          ISZ T1
1958  03242 027240          JMP *-2
1959  03243 006002          SZB
1960  03244 102000          HLT 0           ADB OR ISZ FAILED
1961*
1962  03245 000000          NOP ***** MODULE LOOP
```



```
1964* LDA/CPA - ALL OF CORE - 1ST 2 PAGES
1965*
1966  03246 065710          LDB FCA         1ST CORE ADDRESS = 000002
1967  03247 160001  PT1     LDA B,I
1968  03250 150001          CPA B,I
1969  03251 002001          RSS
1970  03252 102000          HLT 0           LDA/CPA FAILED:  B = ADDRESS
1971  03253 055711          CPB LCA         LAST CORE ADDRESS = 003677
1972  03254 027257          JMP PT2
1973  03255 006004          INB             NEXT CORE ADDRESS
1974  03256 027247          JMP PT1         CONTINUE
1975*
1976* LDB/CPB/STB/CPB - ALL OF CORE - 1ST 2 PAGES
1977*
1978  03257 061710  PT2     LDA FCA         1ST CORE ADDRESS = 000002
1979  03260 164000  PT3     LDB A,I
1980  03261 154000          CPB A,I
1981  03262 002001          RSS
1982  03263 102000          HLT 0           LDB/CPB FAILED:  A = ADDRESS
1983  03264 174000          STB A,I
1984  03265 154000          CPB A,I
1985  03266 002001          RSS
1986  03267 102000          HLT 0           STB/CPB FAILED:  A = ADDRESS
1987  03270 051711          CPA LCA         LAST CORE ADDRESS = 003677
1988  03271 027274          JMP PT4
1989  03272 002004          INA             NEXT CORE ADDRESS
1990  03273 027260          JMP PT3         CONTINUE
1991*
1992* ADA - ADB - IOR - XOR - AND USING TABLE VALUES
1993*
1994  03274 067377  PT4     LDB TBLA        FWA TABLE
1995  03275 077362  PT5     STB A1A         ARG 1 ADDRESS
1996  03276 006004          INB
1997  03277 077363          STB A2A         ARG 2 ADDRESS
1998  03300 006004          INB
1999  03301 077364          STB SUMA        SUM ADDRESS
2000  03302 006004          INB
2001  03303 077365          STB IORA        IOR RESULT ADDRESS
2002  03304 006004          INB
2003  03305 077366          STB XORA        XOR RESULT ADDRESS
2004  03306 006004          INB
2005  03307 077367          STB ANDA        AND RESULT ADDRESS
2006  03310 163362          LDA A1A,I
2007  03311 143363          ADA A2A,I
2008  03312 153364          CPA SUMA,I
2009  03313 002001          RSS
2010  03314 102000          HLT 0           ADA FAILED
2011  03315 167362          LDB A1A,I
2012  03316 147363          ADB A2A,I
2013  03317 157364          CPB SUMA,I
2014  03320 002001          RSS
2015  03321 102000          HLT 0           ADB FAILED
2016  03322 163362          LDA A1A,I
2017  03323 133363          IOR A2A,I
2018  03324 153365          CPA IORA,I
2019  03325 002001          RSS
```

```
2020  03326 102000          HLT 0           IOR FAILED
2021  03327 163362          LDA A1A,I
2022  03330 123363          XOR A2A,I
2023  03331 153366          CPA XORA,I
2024  03332 002001          RSS
2025  03333 102000          HLT 0           XOR FAILED
2026  03334 163362          LDA A1A,I
2027  03335 113363          AND A2A,I
2028  03336 153367          CPA ANDA,I
2029  03337 002001          RSS
2030  03340 102000          HLT 0           AND FAILED
2031  03341 067367          LDB ANDA
2032  03342 006004          INB
2033  03343 057474          CPB TBLE
2034  03344 002001          RSS             END OF TABLE
2035  03345 027275          JMP PT5
2036*
2037  03346 000000          NOP ***** MODULE LOOP



2039* END OF DIAGNOSTIC CYCLE
2040*
2041  03347 002400          CLA
2042  03350 002020          SSA
2043  03351 102000          HLT 0           CLA/SSA FAILED
2044*
2045  03352 061635          LDA BIT15
2046  03353 002020          SSA
2047  03354 002001          RSS
2048  03355 102000          HLT 0           LDA BIT15/SSA/RSS FAILED
2049*
2050  03356 102501          LIA 1
2051  03357 002020          SSA
2052  03360 102077          HLT 77B         END OF PASS HALT
2053  03361 024100          JMP START       DO AGAIN



2055  03362 000000  A1A      NOP       ARGUMENT POINTER
2056  03363 000000  A2A      NOP       ARGUMENT POINTER
2057  03364 000000  SUMA     NOP       SUM POINTER
2058  03365 000000  IORA     NOP       IOR RESULT POINTER
2059  03366 000000  XORA     NOP       XOR RESULT POINTER
2060  03367 000000  ANDA     NOP       AND RESULT POINTER
2061  03370 001700  K10A     DEF K10
2062  03371 001701  K11A     DEF K11
2063  03372 001640  T1A      DEF T1
2064  03373 001702  K12A     DEF K12
2065  03374 001716  JMP5A    DEF JMP5
2066  03375 001712  JSB7A    DEF JSB7
2067  03376 002065  P7A      DEF P7
2068*
2069  03377 003400  TBLA     DEF TBL,1       1ST TABLE ADDRESS
2070  03400 015366  TBL,1    OCT 15366       ARG 1 - 1ST PAIR
2071  03401 127541          OCT 127541      ARG 2
```



```
2072  03402 145127          OCT 145127      SUM
2073  03403 137767          OCT 137767      IOR RESULT
2074  03404 132627          OCT 132627      XOR RESULT
2075  03405 005140          OCT 5140        AND RESULT
2076  03406 051463  TBL,2   OCT 51463       ARG 1 - 2ND PAIR
2077  03407 031465          OCT 31465
2078  03410 103150          OCT 103150
2079  03411 071467          OCT 71467
2080  03412 060006          OCT 60006
2081  03413 011461          OCT 11461
2082  03414 161271  TBL,3   OCT 161271      ARG 1 - 3TH PAIR
2083  03415 025636          OCT 25636       ARG 2
2084  03416 007127          OCT 7127        SUM
2085  03417 165677          OCT 165677      IOR RESULT
2086  03420 144447          OCT 144447      XOR RESULT
2087  03421 021230          OCT 21230       AND RESULT
2088  03422 105560  TBL,4   OCT 105560      ARG 1 - 4TH PAIR
2089  03423 133410          OCT 133410
2090  03424 041170          OCT 41170
2091  03425 137570          OCT 137570
2092  03426 036170          OCT 36170
2093  03427 101400          OCT 101400
2094  03430 141655  TBL,5   OCT 141655      ARG 1 - 5TH PAIR
2095  03431 035334          OCT 35334
2096  03432 177211          OCT 177211
2097  03433 175775          OCT 175775
2098  03434 174561          OCT 174561
2099  03435 001214          OCT 1214
2100  03436 175752  TBL,6   OCT 175752      ARG 1 - 6TH PAIR
2101  03437 137257          OCT 137257
2102  03440 135231          OCT 135231
2103  03441 177757          OCT 177757
2104  03442 042505          OCT 42505
2105  03443 135252          OCT 135252
2106  03444 032047  TBL,7   OCT 32047       ARG 1 - 7TH PAIR
2107  03445 041163          OCT 41163
2108  03446 073232          OCT 73232
2109  03447 073167          OCT 73167
2110  03450 073124          OCT 73124
2111  03451 000043          OCT 43
2112  03452 066144  TBL,8   OCT 66144       ARG 1 - 8TH PAIR
2113  03453 143106          OCT 143106
2114  03454 031252          OCT 31252
2115  03455 167146          OCT 167146
2116  03456 125042          OCT 125042
2117  03457 042104          OCT 42104
2118  03460 122241  TBL,9   OCT 122241      ARG 1 - 9TH PAIR
2119  03461 045032          OCT 45032
2120  03462 167273          OCT 167273
2121  03463 167273          OCT 167273
2122  03464 167273          OCT 167273
2123  03465 000000          OCT 0
2124  03466 156336  TB,10   OCT 156336      ARG 1 - 10TH PAIR
2125  03467 146755          OCT 146755
2126  03470 125313          OCT 125313
2127  03471 156777          OCT 156777
```

```
2128  03472 010463         OCT 10463
2129  03473 146314         OCT 146314
2130  03474 003474  TBLE   DEF *          LWA TABLE
2131*
2132  03475 000000  T2     NOP            TEMPORARY STORAGE
2133  03476 000000  SR1    NOP            SUBROUTINE FROM BASE PAGE
2134  03477 025616         JMP ,P4          GO BACK
2135  03500 025612  JMP1   JMP JMP2       GO BACK TO BASE PAGE
2136*
2137                       END
** NO ERRORS*
```

HP 2100 ALTER-SKIP INSTRUCTION TEST

HP Product No. HP 24208

HEWLETT hp PACKARD

11000 Wolfe Road
Cupertino, California 95014

Manual of Diagnostics
Diagnostic Program Procedure
HP 02100-90019

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HP 2100 ALTER-SKIP INSTRUCTION TEST

This program checks all instruction code combinations of the Alter-Skip Instruction group as defined in the Consolidated Coding Table.

HARDWARE CONFIGURATION

The program runs on an HP 2100 computer with any memory core size and does not use a teleprinter.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

This program should be run only after the Memry Ref. Instruction Test (HP 24209) as instructions from the Memory Reference group are used to test the Alter-Skip group.

To start the program the user loads the program with the Basic Binary Loader, sets Starting Address 100_8, and presses RUN.

The program begins by executing a string of basic tests that check the ability to clear, set, and test the E-Register. A basic test failure results in a unique MEMORY DATA halt. (See Table ALT-2.) This error should be corrected before proceeding further with testing. No provisions are available for repeating Basic Tests.

Next the program executes the extended tests that test the full set of alter-skip instruction code combination using simple E-register instructions (CLE -- CCE -- CME -- SEZ and SEZ,RSS) and the memory reference instructions.

Each valid instruction combination is checked 18 times. First nine different data patterns are checked in the A- or B-register (depending on the instruction), with the E-register clear. Then the nine different data patterns are checked in the A- or B-register (depending on the instruction) with the E-register set.

After the execution of the instruction, the program checks the contents of the A- or B-, and the E-register and checks if the instruction did or did not skip as expected. A detected failure results in a halt and an information display. MEMORY DATA contains $10200x_8$ where x is an octal digit with bit meanings as follows:

bit 0 = 1,A- or B-register error
bit 1 = 1,E-register error.
bit 2 = 1,Instruction skipped or did not skip as expected.

This information should also be displayed after the halt:

A-register -- Actual A- or B-register result.
B-register -- Expected A- or B-register result.
E-register -- Actual E-register result.

After RUN is pressed another halt occurs and this information should be displayed:

MEMORY DATA - Second display halt (102000_8) identification
A-Register - Octal code of failing alter-skip instruction; bit 11 of the instruction identifies the register:
0 = A-register,
1 = B-register,
B-register - Original data pattern in the A- or B-register.
E-register - Original contents of the E-register.

Following the second display halt, the program continues if switch register bit 0 is clear. If switch register bit 0 is set, the original values are restored in the E- and A- or B-registers, and another halt (102076_8) occurs. The next instruction executed is the failing instruction. The result can be observed by single stepping.

After all instructions have been tested, the program normally loops back and repeats the basic and extended tests until an error is detected. If switch register bit 15 is set, the program halts with 102077_8 displayed in MEMORY DATA. A 32 bit pass count is contained in the A- and B-registers, with the most significant bits in the B-register.

Unexpected Changes In A- or B-Registers

If a change occurs in the B-register after executing an alter-skip instruction involving the A-register or vice versa, the computer halts with 103000_8 displayed in MEMORY DATA if the A-register changed unexpectedly, or with 103001_8 displayed in MEMORY DATA if the B-register changes unexpectedly. The unexpected change is left in the register, and the other register contains the octal code of the alter-skip instruction. When the operator presses RUN the program bypasses the other results normally checked. However, if switch rigister bit 0 is set, the computer halts with 102076_8 displayed in MEMORY DATA and the failing instruction is repeated.

A fixed non-symmetrical data pattern of 043210_8 is placed in the register (A- or B-) not expected to change before each alter-skip instruction is executed. (This procedure does not apply to the basic tests.)

OPERATING INSTRUCTIONS

a. Load the HP 2100 Alter-Skip Instruction Test with the Basic Binary Loader.

b. Set Starting Address 100_8.

c. Press RUN.
   The program executes according to the switch register options selected.

Table ALT-1
Switch Register Options

Switch If Set	Meaning
0	Repeat a failing alter-skip instruction but halt 102076_8 before its execution. (Does not apply to the basic tests.)
15	Halt 102077_8 at the end-of-pass (diagnostic cycle). A pass count is contained in the B- and A-registers (most significant bits in B-register).

Table ALT-2.

Summary Of Program Halts

MEMORY DATA	Comments
10200*X*	Alter-skip instruction error halt.
102000	Display halt following error halt.
102076	Halt before repeating failing Alter-Skip instruction.
102077	End-of-pass halt. The A- and B-registers contain the number of passes completed.
102040	RSS instruction failed.
102041	CLE SEZ sequence failed.
102042	CLE SEZ,RSS sequence failed.
102043	CCE SEZ,RSS sequence failed.
102044	CCE SEZ sequence failed.
102045	CLE CME SEZ,RSS sequence failed.
102046	CCE CME SEZ sequence failed.
103000	Unexpected change in A-register after executing an alter-skip instruction.
103001	Unexpected change in B-register after executing an alter-skip instruction.

Figure ALT-1
Consolidated Coding Table

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEMORY REFERENCE INSTRUCTIONS															
D/I	AND		001	0	Z/C	← Memory Address →									
D/I	XOR		010	0	Z/C										
D/I	IOR		011	0	Z/C										
D/I	JSB		001	1	Z/C										
D/I	JMP		010	1	Z/C										
D/I	ISZ		011	1	Z/C										
D/I	AD*		100	A/B	Z/C										
D/I	CP*		101	A/B	Z/C										
D/I	LD*		110	A/B	Z/C										
D/I	ST*		111	A/B	Z/C										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHIFT-ROTATE GROUP INSTRUCTIONS															
0	SRG		000	A/B	0	D/E	*LS		000	†CLE	D/E	‡SL*	*LS		000
				A/B	0	D/E	*RS		001		D/E		*RS		001
				A/B	0	D/E	R*L		010		D/E		R*L		010
				A/B	0	D/E	R*R		011		D/E		R*R		011
				A/B	0	D/E	*LR		100		D/E		*LR		100
				A/B	0	D/E	ER*		101		D/E		ER*		101
				A/B	0	D/E	EL*		110		D/E		EL*		110
				A/B	0	D/E	*LF		111		D/E		*LF		111
				NOP	000				000		000				000
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALTER-SKIP GROUP INSTRUCTIONS															
0	ASG		000	A/B	1	CL*	01	CLE	01	SEZ	SS*	SL*	IN*	SZ*	RSS
				A/B	1	CM*	10	CME	10						
				A/B	1	CC*	11	CCE	11						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAC AND INPUT/OUTPUT INSTRUCTIONS															
1	MAC		000	A/B	0										
1	IOG		000	A/B	1	H/C	HLT		000	← Select Code →					
					1	0	STF		001						
					1	1	CLF		001						
					1	0	SFC		010						
					1	0	SFS		011						
				A/B	1	H/C	MI*		100						
				A/B	1	H/C	LI*		101						
				A/B	1	H/C	OT*		110						
				0	1	H/C	STC		111						
				1	1	H/C	CLC		111						
					1	0	STO		001		000			001	
					1	1	CLO		001		000			001	
					1	H/C	SOC		010		000			001	
					1	H/C	SOS		011		000			001	

Notes: 1) * = A or B. Use with bit 11 as Ø (A-Register) or 1 (B-Register).

2) D/I, A/B, Z/C, D/E, H/C coded: 0/1.

3) †CLE: Only this bit is required.

4) ‡SL*: Only this bit and bit 11 (A/B as applicable) are required.

HP 2100 POWER FAIL DIAGNOSTIC

HP Product No. HP 24206

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HP 02100-90020

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HP 2100 POWER FAIL DIAGNOSTIC

This program confirms proper operation of the power fail interrupt for the Hewlett-Packard 2100 computer.

HARDWARE CONFIGURATION

This program requires any core size HP 2100 computer (with at least 4K if a teleprinter is included), and optionally a teleprinter.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

If a teleprinter is to be used, the SIO Teleprinter driver is loaded and configured. Then the user loads the diagnostic program with the Basic Binary Loader, sets starting address 100_8, selects the desired options to be used for the run of the diagnostic (see Table PF-1), presses INTERNAL and EXTERNAL PRESET, then RUN.

If a teleprinter is available, the program prints a header message, and, after execution of its first routine, goes into a waiting loop, which checks the location addresses in the unused portion of core. Next the user simulates a power failure and restoration of power. The program, upon restart, first confirms proper power fail interrupt (i.e., that the length of time between the power failure and computer shutdown exceeds 500 microseconds) then executes secondary tests to insure register recovery and protection of the contents of core memory from a power failure.

If an error is detected, the program reports the error on the teleprinter (if included) then halts with a coded MEMORY DATA display.

An unexpected interrupt causes irrecoverable halt with a $1060xx_8$ MEMORY DATA display, where *xx* = the trap cell location. Analysis of this error is beyond the scope of this diagnostic.

PROGRAM ORGANIZATION

This program performs the series of routines described below:

START — START begins by printing a preamble message (see Table PF-2,HØ), checks that the LOADER ENABLE is clear, and fills unused core with each location's address.

BKGND — The Background routine increments the right half (bits 0-7) of the switch register two or three times each second and verifies the contents of all unused core memory once each increment by comparing the contents with the core location addresses.

PWRFL — The Power Fail Interrupt routine calls RSTRT if power is being restored. If power is failing, this routine saves registers and estimates time before power is off.

RSTRT — The Restart routine is entered through PWRFL. It verifies proper operation of PWRFL and increments the cycle count. The last part of PWRFL and all the associated counters are rebuilt in case power-off occurred during a core-fetch.

MESSAGE ANALYSIS

An H prefix indicates an operating instruction or comment, and an E prefix indicates an error condition. The MEMORY DATA column indicates where coded halts occur. The last two octal digits in the coded halts correspond to the message number. The COMMENTS column notes the operator action to be performed, meaning of the messages, or probable area malfunctioning. The ROUTINE column specifies the program routine containing the message or halt.

OPERATING PROCEDURES

To Configure The Diagnostic

a. If the teleprinter is included, load the SIO Teleprinter driver with the Basic Binary Loader and configure the driver.

b. Load the HP 2100 Power Fail Diagnostic tape with the Basic Binary Loader.

To Make Tape Of The Configured Diagnostic

a. If a High Speed Tape Punch is available, load the SIO Tape Punch driver with the Basic Binary Loader and configure the driver.

b. If a High Speed Tape Punch is not available, turn on the teleprinter tape punch.

c. Load the SIO System Dump.

d. Set Starting Address 2_8.

e. Set switch register bit 15.

f. Press RUN.

g. A configured HP 2100 Power Fail Diagnostic Tape is punched. The computer halts with 102077_8 displayed. To make additional copies of the configured HP 2100 Power Fail Diagnostic Tape, press RUN.

To Load And Execute The Diagnostic

NOTE: Eliminate step a if continuing from configuration.

a. Load the configured HP 2100 Power Fail Diagnostic Tape with the Basic Binary Loader.

b. Set Starting Address 100_8.

c. Select the desired options from Table PF-1 by setting the appropriate bits of the switch register.

d. Press INTERNAL PRESET.

e. Press EXTERNAL PRESET.

f. Press RUN.

   If a teleprinter is available, the program prints a header message.

g. BKGND executes, incrementing the right half (bits 0-7) of the switch register two or three times each second. The program is now ready to process a power fail interrupt.

h. The user must cause a power failure. A suggested way is:

   1. Turn off the POWER switch.

   2. Remove the power cord from the electrical outlet.

   3. Decrease the line voltage below 100 Vac.

i. Restore power.

   NOTE: The user may test the EPRS line by holding down the EXTERNAL PRESET switch.

j. If the halt mode or EPRS line is being tested:

   1. Set Starting Address 110_8.

   2. Press RUN.

k. RSTART verifies proper operation of the power fail option. The cycle count (cycle count=steps g-k) is incremented and the program returns to step g.

Table PF-1

Switch Register Options

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits

0-7 Reserved to indicate program count.

8 Spare.

9 If the teleprinter is available, setting bit 9 causes the program to print out the number of power failures since the test started.

10 Spare.

11 If set, all messages for the teleprinter will be suppressed.

12 Spare.

13 If set when program begins, the teleprinter driver is assumed to not have been loaded and the teleprinter will not be used during the program.

14 Set off to halt after each error.

15 Set on to halt the program.

Table PF-2

Diagnostic Messages

MEMORY DATA	ROUTINE	MESSAGE	COMMENTS
(no halt)	START	HØ HP 21ØØ POWER FAIL DIAGNOSTIC	Header message.
102001	START	E1 CLEAR LOADER ENABLE	This switch is on HP 2100 console.
102002	BKGND	E2 CHANGED CORE, ADDRESS = *xxxxxx* CONTENTS = *yyyyyy*	Echocheck fail in unused core. Values are in octal and should be equal.
102003	RSTRT	E3 SHUTDOWN ROUTINE DID NOT COMPLETE. SHOULD COMPLETE *xxxx* MICRO-SECONDS, COMPLETED *xxxx* MICROSECONDS.	Primary power fail interrupt test failed. Values are in decimal.
(no halt)	BKGND	H4 THERE HAVE BEEN *xxxx* TESTS OF THE POWER FAIL CIRCUITRY	Dump of cycle count due to switch register bit 9. Value is in decimal.
102005	RSTRT	E5 POWER FAIL ROUTINE NOT ENTERED	No interrupt after last power fail.
102006	PWRFL	(none)	Power did not fail following a power fail interrupt or flag logic failed on restart.
102007	BKGND	E7 B-REGISTER NOT EQUAL TO COUNT, B = *xxxxxx* COUNT = *xxxxxx*	B-register should be equal to right half (bits 0-7) of switch register.
102010	RSTRT	E1Ø UNDEFINED SHUTDOWN ERROR	
102040	BKGND	(none)	Halt due to switch register bit 15.
1060*xx*	ANY	(none)	Trap cell halt. M-register = memory address when interrupted, *xx* = trap cell location.

HP 2100 MEMORY PARITY CHECK TEST

HP Product No. 24198

HEWLETT hp PACKARD

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Diagnostic Program Procedure
HP 02100-90021

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HP 2100 MEMORY PARITY CHECK TEST

This diagnostic confirms proper operation of the Memory Parity Check circuitry for an HP 2100 computer. If an error exists, the program identifies the faulty function. Each error found should be corrected and retested before the next function is tested.

HARDWARE CONFIGURATION

This Memory Parity Check diagnostic requires any core size HP 2100 computer.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

The diagnostic is loaded and configured in two phases:

a. Program configuration is done by switch register settings in Table MP-1.

b. Options to be used for a normal run of the diagnostic are selected by setting the switch register as listed in Table MP-2, then pressing RUN. These settings become an internal switch register. If any option is changed during the run, the internal switch register may be overridden by setting switch register bit 0 or other appropriate bit(s) as listed in Table MP-2.

After the configuration procedures are complete, the SIO System Dump program may be used to make a permanent copy of the configured diagnostic.

If an error is detected, the program halts with a value displayed in MEMORY DATA. (See Table MP-3.) The cause of trap cell halt $1060xx_8$, located in low memory 2_8 -77_8, should be determined before the diagnostic is restarted.

PROGRAM ORGANIZATION

The diagnostic consists of the series of routines described below:

CONF — CONF configures the diagnostic for the proper core memory size and select code (I/O channel) and sets the internal switch register for the options selected at configuration time.

START — START sets trap cell halts in locations 2_8 -77_8. Before INIT starts, the program halts with 102002_8 displayed to allow the user to connect terminal E1 to E2 and E3 to E4 on the Memory Data Control Board.

INIT — INIT loads even parity data into special locations. Because Memory Parity Check requires odd parity data, the incorrect even parity data is used by the following test routines to check the Memory Parity Check circuitry.

TESTA — TESTA confirms that bit 15 of the A-register is not set when the violation register is loaded after power turn-on at the end of INIT, and that a parity error can be detected. If a parity error is detected, TESTA halts, the front panel PARITY ERROR light goes on and 000001_8 is contained in the B-register. If a parity error is not detected, TESTA halts, the PARITY ERROR light remains off, and 102005_8 displayed. When the user presses INTERNAL PRESET after a parity error halt, the PARITY ERROR light on the front panel and the parity bit light on the Memory Data Control board go off. Then switch S2 on the I/O buffer board is set to its INTERRUPT mode and the user presses RUN to advance the diagnostic to the next test.

NOTE: From this point the program runs without operator intervention unless an error occurs.

TESTB TESTB checks the interrupt ability on detection of a parity error. TESTB must be error-free before the other tests can be made.

TESTC TESTC tests the ability of a CLF 5 instruction to inhibit parity error interrupts. A CLF 5 instruction is issued to turn off the interrupt circuitry, then an even parity word generated by INIT is accessed. An interrupt should not occur.

TESTD TESTD tests inhibition of parity error interrupts when protected or non-existent memory is accessed. TESTD attempts to read the contents of the highest location in core (detected by CONF), seen as all zeros (even parity) when the LOADER ENABLE lamp is off. It then attempts to read from non-existent core (if any). A parity error interrupt should not occur in either case.

TESTE TESTE tests inhibition of parity error interrupts during phase 3 of an STA instruction. An STA instruction is used to write an even parity value into memory. An interrupt should not occur. If an interrupt occurs, the diagnostic halts.

TESTH TESTH tests priority control by generating an I/O interrupt on the I/O channel selected during program configuration of the diagnostic. That interrupt is immediately followed by a parity error interrupt which inhibits the I/O interrupt. If the I/O interrupt occurs first or the I/O interrupt fails to follow the parity error interrupt (or if neither occurs), the diagnostic halts.

TESTI TESTI causes certain locations, previously set to even parity by INIT, to extensively exercise the parity tree. For each location TESTI performs the following tests:

a. Is parity error detected?

b. Does interrupt occur?

c. Is the location's address strobed into the Memory Protect violation register?

The routine also checks to see that a read/write type instruction (LDB) does not restore good parity to a location containing a parity error and that a clear/write type instruction (STB) does restore good parity.

END — END halts the diagnostic with 102077_8 displayed.

NOTE: This END routine has provisions for return of execution control to a suitable executive program, if present.

LIMITATIONS

This diagnostic does not analyze errors in the Memory Protect violation register. Such errors can occur because of bit failures in the violation register and/or loss of the strobe pulse from the Memory Parity Check circuitry. If the diagnostic halts with 102007_8 displayed (see Table MP-3), the 2100 Memory Protect Test (HP 24222) program should be executed. The error is identified as either the Memory Parity Check or the Memory Protect circuits.

If the program enters an uncontrollable loop caused by the absence of either the IAK or the ENF functions, it cannot report an error.

MESSAGE ANALYSIS

All halts display a MEMORY DATA value. If data is to be read, that data is displayed in the A-register and, when needed, the B-register. Refer to Table MP-3.

OPERATING INSTRUCTIONS

NOTE: At least one standard I/O board must be installed in an I/O slot, Switch S1 on the I/O Control W/DMA board must be set to the ARS position, and Switch S2 on the I/O Buffer board must be set to the interrupt position.

To Configure The Diagnostic

a. Store all zeros in memory location 5_8.

b. Load the HP 2100 Memory Parity Check Test with the Basic Binary Loader.

c. Set Starting Address 2_8.

d. Specify the program configuration by setting the switch register as listed in Table MP-1, then press RUN. If the settings are correct, the computer halts with 107074_8 displayed.

e. Select the internal switch register options by setting the switch register as listed in Table MP-2, then press RUN. The computer halts with 107077_8 displayed in MEMORY DATA.

NOTE: The external switch register is always selected if switch register bit 0 is set.

To Make A Tape Of The Configured Diagnostic

a. If a High Speed Tape Punch is available, load the SIO Tape Punch driver with the Basic Binary Loader and configure the driver.

b. If a High Speed Tape Punch is not available, load the SIO Teleprinter driver with the Basic Binary Loader and configure the driver.

c. Load SIO System Dump.

d. Set Starting Address 2_8.

e. Set switch register bit 15.

f. Press RUN.

g. A configured HP 2100 Memory Parity Check Test tape is punched. The computer halts with 102077_8 displayed. To make additional copies of the configured Memory Parity Check Test Tape, press RUN.

To Load And Execute The Diagnostic

NOTE: Eliminate step a if continuing from step e, To Configure The Diagnostic.

a. Load the configured Memory Parity Check Test tape with the Basic Binary Loader after storing all zeros in location 5_8.

b. Set Starting Address 100_8.

c. Press INTERNAL and EXTERNAL PRESET.

d. Press RUN. The diagnostic executes according to the options selected.

e. Before INIT starts, the diagnostic halts with 102002_8 displayed. If the parity bit light on the Memory Data Control board is on, a circuit error exists and must be fixed, then the diagnostic is restarted.

   If the light is off:

   1. Turn off the computer power.
   2. Connect E1 to E2 and E3 to E4 on the Memory Data Control board with clip leads.
   3. Turn on computer power.
   4. Set Starting Address 110_8.
   5. Clear the switch register.
   6. Press INTERNAL and EXTERNAL PRESET.
   7. Press RUN.

f. The computer halts at the end of INIT with 102003_8 displayed in MEMORY DATA.

   1. Turn off computer power.
   2. Remove clip leads installed in step e2, To Load And Execute The Diagnostic.
   3. Set switch S2 on the I/O buffer board to the HALT position.
   4. Turn on computer power.
   5. Set Starting Address 111_8.
   6. Clear the switch register.
   7. Press INTERNAL and EXTERNAL PRESET.
   8. Press RUN.

g. TESTA halts if the board is working properly. At that time the front panel PARITY ERROR and the Memory Data Control board parity bit lights should be on. Press INTERNAL PRESET and check that the PARITY ERROR light and the parity bit light turn off. (If either light does not function as described, check the parity error detect circuitry, then restart the diagnostic.) Then display the B-register, it should contain 000001_8.

h. To select options other than those in the internal switch register, set switch register bit 0. Select the desired options by setting the switch register as listed in Table MP-2.

i. Set switch S2 on the I/O buffer board to INTERRUPT.

j. Press EXTERNAL PRESET.

k. Press RUN.

l. After all tests are completed, the computer halts with 102077_8 displayed. To run the diagnostic again, select desired options and perform steps d through k of the procedure "To Load And Execute The Diagnostic."

Table MP-1

Program Configuration--Switch Register Settings

Switch Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits

0-5 Set to select code of the standard interface board.

6 Set if Memory Protect is not available.

7-15 Spares.

Table MP-2

Options--Switch Register Settings

Switch Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits

0 Set to override the internal switch register and to change an option.

1-11 Spares.

12 Set to halt at the end of a complete diagnostic cycle.

13 Set so that after a complete diagnostic cycle, tests requiring operator intervention in future cycles of the diagnostic are eliminated. (Tests eliminated are INIT and TESTA.)

14-15 Spares.

Table MP-3

Diagnostic Messages

MEMORY DATA	Test	Message
102002	INIT	Perform step e, of the procedure "To Load And Execute The Diagnostic."
102003	INIT	Perform step f, of the procedure "To Load And Execute The Diagnostic."
102004	TESTA	Parity error interrupt indicator (bit 15) not reset by power turn-on.
102005	TESTA	Computer failed to halt on parity error.
102006	TESTB	Parity error did not cause interrupt at address shown in A-register. Interrupt function not working, or parity tree is faulty.
102007	TESTB	Parity error memory address is incorrect. Expected address is in A-register, actual in B-register. Perform Memory Protect Test to determine if source of error is in Memory Protect or Parity Error circuitry.
102010	TESTC	CLF 5 did not inhibit parity error interrupt.
102011	TESTD	A parity error interrupt caused by accessing protected memory.
102020	TESTE	A parity error interrupt caused during phase 3 of an STA instruction.
102027	TESTD	A parity error interrupt caused by accessing non-existent memory.
102040	TESTH	Parity error failed to take priority over I/O interrupt.

Table MP-3 (cont.)

MEMORY DATA	Test	Message
102041	TESTH	Neither parity error nor I/O interrupt received in priority test.
102042	TESTH	No I/O interrupt received in priority test.
102043	TESTI	Parity error interrupt indicator (bit 15) not set on parity error.
102044	TESTI	Parity error did not cause interrupt at address shown in A-register. Interrupt function not working or parity tree is faulty.
102045	TESTI	Parity error memory address is incorrect. Expected address is in A-register, actual in B-register. Perform 2100 Memory Protect Test to determine if source of error is in Memory Protect or Parity Error circuitry.
102046	TESTI	Parity error at address shown in A-register restored to good parity by an STB instruction.
102047	TESTI	Parity error at address shown in A-register not restored to good parity by a STB instruction.
102077	END	Diagnostic has been completed.
1060*xx*	any	Trap cell interrupt. M-register = memory address when interrupts, *xx* = the trap cell location.
107070	CONF	LOADER was enabled; verify LOADER ENABLE lamp is off and press RUN.
107072	CONF	Program configuration error halt. Set correct bits in switch register (see Table MP-1) and press RUN.

Table MP-3 (cont.)

MEMORY DATA	Test	Message
107074	CONF	Select the internal switch register for desired options by setting the switch register as listed in Table MP-2 then press RUN.
107077	CONF	Configuration steps completed. Use SIO System Dump or: Set Starting Address 100_8, press INTERNAL and EXTERNAL PRESET then RUN.

HP 2100 LOW MEMORY PATTERN TEST
AND
HP 2100 HIGH MEMORY PATTERN TEST

HP Order No. 24193

and

HP Order No. 24194

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HP 2100 MEMORY PATTERN TESTS

These two diagnostic programs, the HP 2100 High Memory Pattern Test and the HP 2100 Low Memory Pattern Test, check core memory of an HP 2100 computer for failures. The High Memory Pattern Test occupies upper memory to test lower memory locations, and the Low Memory Test occupies lower memory to test upper memory locations.

HARDWARE CONFIGURATION

These diagnostic programs are run on an HP 2100 computer, with 2K or larger memory size. No peripheral devices are used; errors and messages to the user are reported by MEMORY DATA error code displays.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

Either the High Memory Pattern Test or the Low Memory Pattern Test may be run first, by using the Basic Binary Loader to place the desired program into core.

When the Low Memory Pattern Test is used, operation starts at location 2_8 to test any area of memory from location 621_8 through the upper limit of memory. The upper limit may include the area occupied by the Basic Binary Loader (the last 100_8 locations), if the LOADER ENABLE button is lit when the test sequences are started.

> *NOTE: The Basic Binary Loader is destroyed if the Low Memory Pattern Test checks that area. After the tests are complete, the user must restore the Basic Binary Loader by performing the steps given in the* Software Operating Procedures *manual.*

When the High Memory Pattern Test is used, operation starts at location 2000_8 to test any area of memory from location 2_8 through 1777_8.

> *NOTE: If the High Memory Pattern Test area includes location 4_8, 5_8, or 6_8 the instruction stored in that location by the START routine is destroyed. If power failure or parity error causes an interrupt to that location during the tests, the content at that moment is executed as an instruction, which produces unpredictable results.*

After the desired Memory Pattern Test has been loaded, the user selects program options before starting the program. See Table MPT-1. One selection directs the program to test either a standard area or a user-determined area of memory. If the standard area is selected, the program assumes the computer has 8K of memory and tests locations 621_8 through 17677_8 for the Low Memory Test or locations 2_8 through 1777_8 for the High Memory Pattern Test. The user may change the test area selection at any time.

If an error is detected, the program halts with a MEMORY DATA error code displayed and, when necessary, with data in the A- and B-registers. After an error halt, the user consults Table MPT-2 to learn the cause and location of the error and the corrective action.

Data displayed for each error may be saved in an area of memory set aside for a "table of errors," if that program option is selected. Three consecutive locations are used for each error, to save the failing address, the correct pattern, and the erroneous pattern. Data for a failing address is saved in the table of errors only once, regardless of when an error for that address is found.

The table of errors begins at location 621_8 for the Low Memory Pattern Test or 2575_8 for the High Memory Pattern Test, and may continue through 3677_8. As the Low Memory Pattern Test makes entries in its table of errors, it shifts its first tested address up from 621_8 to prevent destruction of the table of errors; the High Memory Pattern Test does not shift its first address because its table of errors is not within the tested area.

If the number of error entries needed in the table of errors exceeds the bounds available, the program halts with 102006_8 displayed. If the user suspects this limitation is about to occur, he may halt the program to display the next available address in the table and the number of errors already saved. The table of errors may be reset to 0 at any time. See Table MPT-1.

If a power fail interrupt occurs during the Low Memory Pattern Test, the computer halts with 103004_8 displayed. The cause of a power failure must be determined and corrected before the program is run or restarted.

Parity Errors

Because the computer includes Memory Protect and Memory Parity Check features, switch S2 on the I/O Buffer board should be set to INTERRUPT. Thus, a parity error causes an interrupt to a parity error subroutine within the Memory Pattern Test.

If the parity error is within the area occupied by the program, the program halts with the error address in the A-register (press A to display the error address), and the contents of that address in the B-register (press B to display the contents). To correct the error, the user may either consult a listing of the program, load the correct instruction into the B-register, and press RUN; or he may reload the program (through the Basic Binary Loader), set the correct starting address, and press RUN. The program again attempts to execute the instruction. If the error repeats, the location is faulty and must be repaired before the program can be run.

If the parity error is within the area to be tested by the Memory Pattern Test, it is not reported by the parity error subroutine; it is reported as a pattern test failure by the main program.

If Memory Protect is not available, the program must be run with program option bit 11 set on and the I/O Buffer board switch S2 set to HALT. If a parity error is detected, the program halts with the PARITY ERROR lamp on. The user should attempt to correct the error by reloading the program

(through the Basic Binary Loader) setting the correct starting address, and pressing RUN. If the error repeats, the location is faulty and must be repaired before the program can be run.

NOTE: When the Parity Check board switch S2 is set to HALT, no distinction between the area occupied by the program and the area to be tested is made; any parity error causes a halt.

If Memory Protect and Memory Parity Check are both not available, a memory failure in the area occupied by the program may affect either data or program instructions; the results are unpredictable.

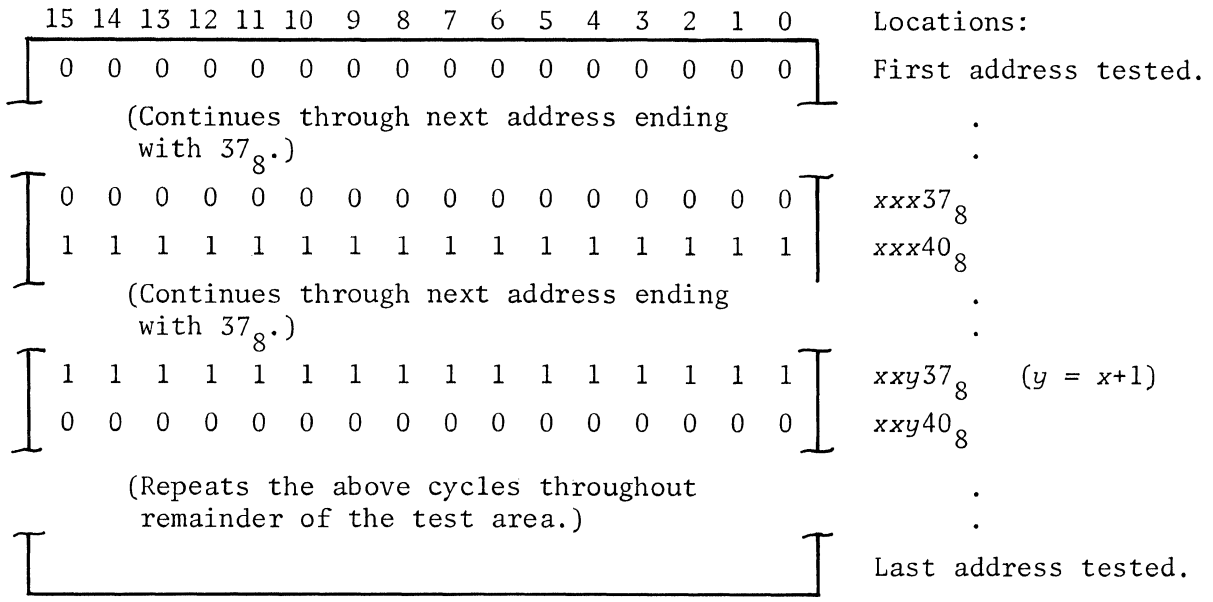
PROGRAM ORGANIZATION

The High and Low Memory Pattern Tests perform the series of routines described below:

START — This routine interprets the program options set by the user into the switch register (see Table MPT-1) and sets up the initial values for the program variables.

TEST 1 (Word Checkerboard Test)

This routine writes, then tests, word checkerboard patterns throughout the specified area of memory to be tested. The first word checkerboard pattern is a series of words with all 16 bits set to 0 (or to 1) alternated with a series of words with all 16 bits set to 1 (or to 0), throughout the test area as shown on the next page.



The *First* Word Checkerboard Pattern

Then each location is tested by the following steps:

a. The contents of the location are read and checked for errors. If an error is found, the appropriate report is made and the remaining test steps are skipped.

b. The contents are complemented and that complement is written back into the location.

c. The new contents are read and checked for errors.

d. The content is re-complemented and written back into the location.

After all locations have been tested, the routine writes the alternate word checkerboard pattern throughout the test area then tests each location again.

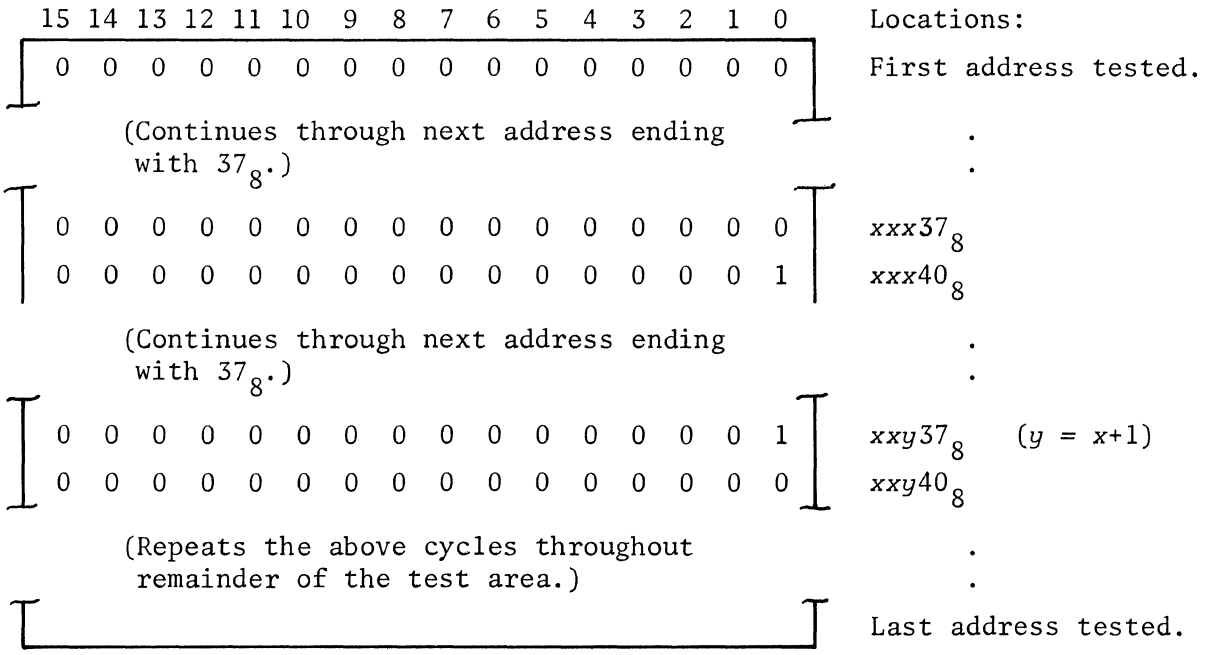
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Locations:
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	First address tested.
(Continues through next address ending with 37_8.)																. .
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	$xxx37_8$
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	$xxx40_8$
(Continues through next address ending with 37_8.)																. .
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	$xxy37_8$ ($y = x+1$)
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	$xxy40_8$
(Repeats the above cycles throughout remainder of the test area.)																. .
																Last address tested.

The *Alternate* Word Checkerboard Pattern

The write/test sequence is performed a total of 32 times, 16 times for the first checkerboard pattern and 16 times for the alternate checkerboard pattern.

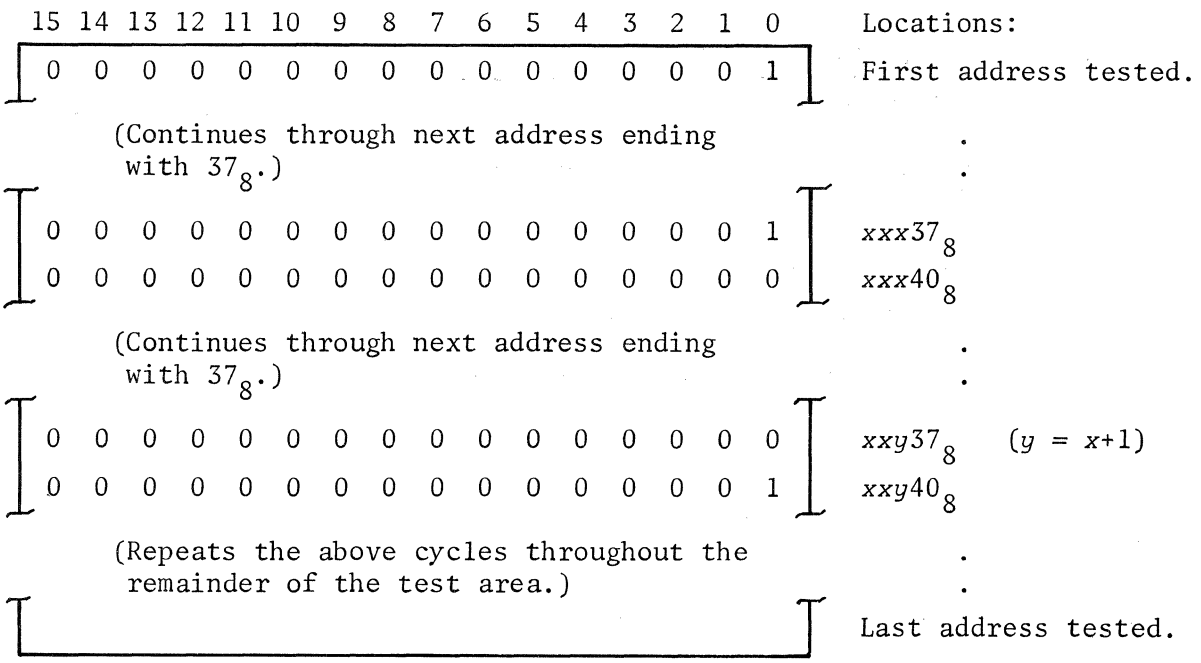
TEST 2 (Bit 0 Checkerboard Test)

This routine writes, then tests, bit 0 checkerboard patterns throughout the specified area to be tested. The first bit 0 checkerboard pattern is a series of words with all 16 bits set to 0 alternated with a series of words with bits 15 through 1 set to 0 and bit 0 set to 1, throughout the test area, as shown on the next page.



The *First* Bit 0 Checkerboard Pattern

Then each location is tested by the same steps described for Test 1. After all locations have been tested, the routine writes the alternate of the first bit 0 checkerboard pattern throughout the test area then tests each location again.



The *Alternate* Bit 0 Checkerboard Pattern

After the first bit 0 checkerboard pattern and its alternate have been written and tested, the single bit set to 1 is shifted one bit position to the left to create the second bit 0 checkerboard pattern. Thus, the second bit 0 checkerboard pattern is a series of words with 16 bits set to 0 alternated with a series of words with bits 15 through 2 set to 0, bit 1 set to 1, and bit 0 set to 0. Then the second bit 0 checkerboard pattern and its alternate are written and tested as described above.

The write/test sequence is performed a total of 32 times, to test each of 16 bit 0 checkerboard patterns and their alternates.

TEST 3 (Bit 1 Checkerboard Test)

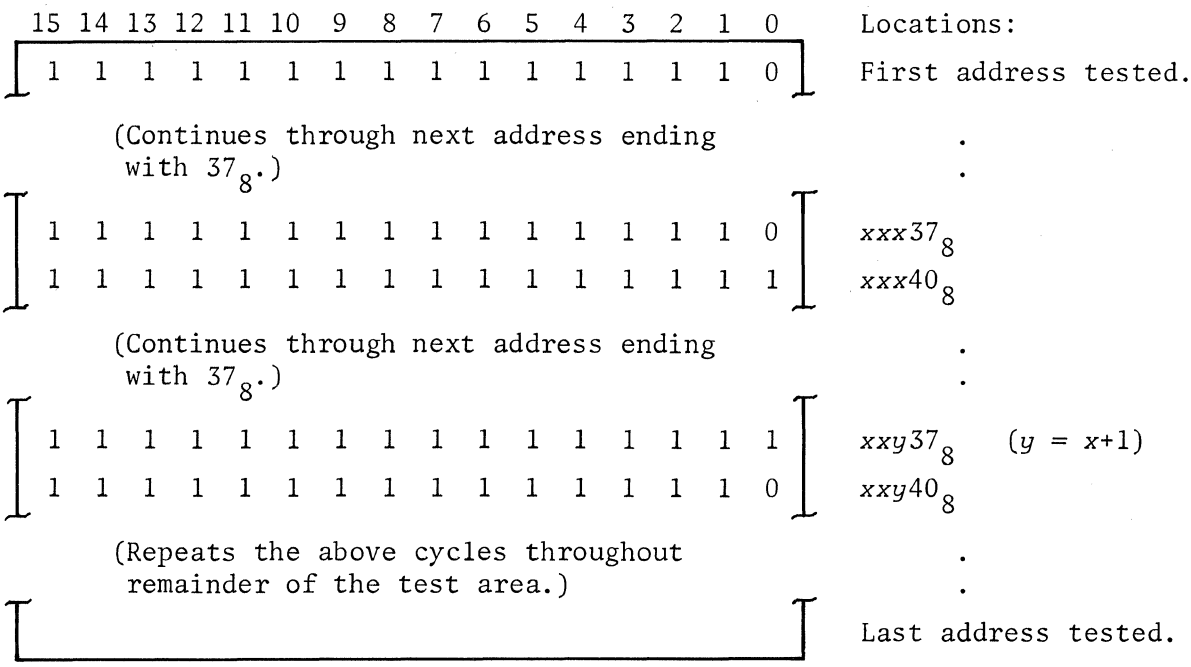
This routine writes, then tests, bit 1 checkerboard patterns throughout the specified area to be tested, similarly to the manner of Test 2. The first bit 1 checkerboard pattern is a

series of words with all 16 bits set to 1 alternated with a series of words with bits 15 through 1 set to 1 and bit 0 set to 0, throughout the test area.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Locations:
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	First address tested.
(Continues through next address ending with 37_8.)																. .
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	$xxx37_8$
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	$xxx40_8$
(Continues through next address ending with 37_8.)																. .
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	$xxy37_8$ ($y = x+1$)
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	$xxy40_8$
(Repeats the above cycles throughout the remainder of the test area.)																.
																Last address tested.

The *First* Bit 1 Checkerboard Pattern

Then each location is tested by the same steps described for Test 1. After all locations have been tested, the routine writes the alternate of the first bit 1 checkerboard pattern throughout the test area then tests each location again.



The *Alternate* Bit 1 Checkerboard Pattern

After the first bit 1 checkerboard pattern and its alternate have been written and tested, the single bit set to 0 is shifted one position to the left to create the second bit 1 checkerboard pattern. Thus, the second bit 1 checkerboard pattern is a series of words with all 16 bits set to 1 alternated with a series of words with bits 15 through 2 set to 1, bit 1 set to 0, and bit 0 set to 1. Then the second bit 1 checkerboard pattern and its alternate are written and tested as described above.

The write/test sequence is performed a total of 32 times, to test each of 16 bit 1 checkerboard patterns and their alternates.

OPERATING INSTRUCTIONS

a. Use the Basic Binary Loader to load the desired Memory Pattern Test.

b. Set the starting address 2_8 if the Low Memory Pattern Test was loaded in step a, otherwise set the starting address 2000_8.

c. If the User-Determined Area program option is to be used (see Table MPT-1), set only switch register bit 15 on, then perform steps d through h. Otherwise, skip directly to step g.

d. Press RUN. The program halts with 102001_8 displayed.

e. Set the switch register to the address of the first location to be tested, then press RUN. Do not set a value less than that contained in the A-register. The program halts with 102002_8 displayed.

f. Set the switch register to the address of the last location to be tested, then press RUN. The program halts with 102004_8 displayed.

g. Select the program options to be used by setting the switch register as listed in Table MPT-1.

h. If the Low Memory Pattern Test is to include the Basic Binary Loader area (the last 100_8 locations in memory), press to light the LOADER ENABLE button.

i. Press RUN to start the diagnostic according to the program options selected in step g.

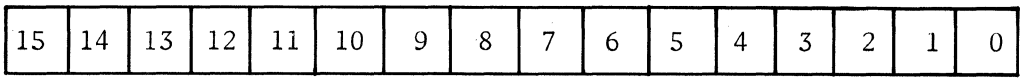
j. The boundaries of the area tested may be changed at any time. To do so, set switch register bit 15 on, then set bit 5 on. The program halts with 102001_8 displayed. Restart the diagnostic by performing steps e through i.

MESSAGE ANALYSIS

All halts display a value from MEMORY DATA. Refer to Table MPT-2 to analyze the halt conditions, then press RUN to resume the diagnostic program.

Table MPT-1

Program Options--Switch Register Settings



Bit	Function
0	Set on (at any time) to hold the current checkerboard pattern in Test 2 or Test 3. This bit should be used with bit 12 or 13 on.
1	Set on to store data for each error in the table of errors.
2	Spare.
3	Set on to reset the table of errors to zero upon return to the start of the program. This bit should be used with bit 6 on.
4	Set on to suppress error halts.
5	Set on momentarily (at any time) to immediately return to the start of the program. If bit 6 is off, the program restarts.
6	Set on to halt upon return to the start of the program. The A-register contains the next available address in the table of errors and the B-register contains the number (in octal) of errors already saved.
7	Set on to halt at the end of the program.
8-10	Spares.
11	Set on if Memory Protect is not available.
12	Set on to skip Test 1 and Test 2 and loop continuously on Test 3. If bit 13 or 14 is also set on, this bit takes precedence.
13	Set on to skip Test 1 and Test 3 and loop continuously on Test 2. If bit 14 is also set on, this bit takes precedence.
14	Set on to skip Test 2 and Test 3 and loop continuously on Test 1. This bit is subordinate to bit 12 or bit 13.
15	Set on to test a user-determined area, rather than the standard test area.

Table MPT-2

Diagnostic Halts

MEMORY DATA	Routine	Meaning
102001	START	Set switch register to the address of the first location to be tested, then press RUN. Do not set a value less than that contained in the A-register (press A to display).
102002	START	Set the switch register to the address of the last location to be tested, then press RUN.
102003	START	The last location address specified is smaller than the first location address specified. Set the switch register to the correct first location address and press RUN.
102004	START	Select program options from Table MPT-1 and press RUN.
102005	any	Table of errors display. The A-register (press A) contains the next available address in the table of errors and the B-register (press B) contains the number of errors (octal) already saved.
102006	any	The table of errors is full.
102007	any	A parity error has been detected in the area of memory occupied by the diagnostic program. The A-register (press A) contains the error address and the B-register (press B) contains the content of that address. Load the B-register with the correct content, reset the program options in the switch register, and press RUN. Or, if the correct content cannot be determined, reload and restart the program.
102010	TEST 1 or TEST 2 or TEST 3	First pattern read error. The A-register contains the pattern written into core, and the B-register contains the pattern read from a given location. Press RUN to display the location address from the A-register.
102011	TEST 1 or TEST 2 or TEST 3	First pattern read error address display. The A-register (press A) contains the address of the faulty location. Press RUN to resume the diagnostic program.

Table MPT-2. Diagnostic Halts (cont.)

MEMORY DATA	Routine	Meaning
102020	TEST 1 or TEST 2 or TEST 3	Alternate pattern read error. The A-register contains the pattern written into core, and the B-register contains the pattern read from a given location. Press RUN to display the location address from the A-register.
102021	TEST 1 or TEST 2 or TEST 3	Alternate pattern read error address display. The A-register (press A) contains the address of the faulty location. Press RUN to resume the diagnostic program.
102030	TEST 1 or TEST 2 or TEST 3	Complement pattern read error. The A-register contains the complement pattern written into core after a successful first or alternate pattern read test, and the B-register contains the pattern read from the same location. Press RUN to display the location address from the A-register.
102031	TEST 1 or TEST 2 or TEST 3	Complement pattern read error address display. The A-register (press A) contains the address of the faulty location. Press RUN to resume the diagnostic program.
102077	any	Diagnostic program is complete. To restart, select program options from Table MPT-1 and press RUN.
103004	any	Power Fail Interrupt.

HP 2100 INTERRUPT TEST

HP Product No. HP 24215

11000 Wolfe Road
Cupertino, California 95014

Manual of Diagnostics
Diagnostic Program Procedure
HP 02100-90025

June 1971

HP 2100 INTERRUPT TEST

This diagnostic program tests the 2100 interrupt priority structure, the interrupt capability of any of the I/O slots, and the Central Interrupt Register.

HARDWARE CONFIGURATION

This diagnostic requires any core size 2100 computer (a minimum of 4K memory if a teleprinter is included), I/O interface cards, and optionally, a teleprinter and priority jumper cards.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

The switch register is used to select options and control the program.

Errors and program messages are indicated by teleprinter messages, by program halts, or both. When appropriate, after a program halt, information about program errors is contained in the A- and B-Registers (see Table INT-2).

The select codes of the I/O slots to be tested are user-defined. They are entered by the teleprinter or the switch register.

PROGRAM ORGANIZATION

Initially four tests are run to check the ability to clear, set, and test the interrupt system.

Then the program decides whether or not to accept new slot parameters, i.e., the select codes of all I/O slots to be tested. A halt or message for new slot parameters occurs if the slot parameter buffer is empty (after loading the program) and/or if switch register bit 15 is set. See "OPERATING INSTRUCTIONS, *NOTE*" and the procedure, "To Load And Execute The Diagnostic."

Next the program checks that no interrupt occurs if the flags and control flip-flops of each given select code are set, but the interrupt system is off. An unexpected interrupt results in a halt with 1030*xx* displayed; (*xx*) is the select code of the bad slot. The user should not continue if this happens.

Each select code in the slot buffer is then checked individually to see that each slot interrupts, that a second interrupt does not occur, and that no unexpected interrupts occur. The contents of the central interrupt register are also checked following the interrupt unless switch register bit 13 is set.

The failure of a slot to interrupt results in a halt with 102005_8 displayed. Incorrect contents in the central interrupt register results in a halt with 102006_8 displayed. A double interrupt results in an irrecoverable halt with 102007_8 displayed. An unexpected interrupt results in a halt with 1060*xx* displayed; the user should not continue if this happens.

Then all select codes in the slot buffer are tested as a group. All given flag and control flip-flops are set and the interrupt system is turned on. The interrupts should occur in the order expected: lowest select code first, next lowest second, etc. If an expected interrupt does not occur, the computer halts with 102010_8 displayed. An unexpected interrupt results in an irrecoverable halt with 102011_8 displayed.

Following the last interrupt, an end-of-pass message is printed (unless switch register bit 14 or 10 are set) and an end-of-pass halt occurs (unless switch register bit 9 is set). A pass is one diagnostic cycle since the last input of slot parameters. The program then loops back and repeats all tests.

OPERATING INSTRUCTIONS

NOTE: All I/O slots to be tested must be specified by the user and contain an interface card with control and flag logic capable of generating interrupts. Empty I/O slots between the highest and lowest priority interrupt and capable interface cards must be filled with priority jumper cards. If switch register bit 14 is clear, input of I/O slot select codes is by teleprinter. If switch register bit 14 is set, input of I/O slot select codes is via the switch register.

To Configure The Diagnostic

a. Load the SIO teleprinter driver (if available) with the Basic Binary Loader and configure the driver.

b. Load the HP 2100 Computer Interrupt Test with the Basic Binary Loader.

To Make A Tape Of The Configured Diagnostic

NOTE: This procedure may also be used after completing the procedure, "To Load and Execute The Diagnostic" and one pass of the diagnostic.

a. If a High Speed Tape Punch is available, load the SIO Tape Punch driver with the Basic Binary Loader and configure the driver.

b. If a High Speed Tape Punch is not available, turn on the teleprinter tape punch.

c. Load the SIO System Dump.

d. Set Starting Address 2_8.

e. Set switch register bit 15.

f. Press RUN.

g. A configured HP 2100 Interrupt Test tape is punched. The computer halts with 102077_8 displayed in MEMORY DATA. To make additional copies of the configured HP 2100 Interrupt Test Tape, press RUN.

To Load And Execute The Diagnostic

NOTE: Eliminate step a if continuing from step b, To Configure The Diagnostic.

a. Load the configured HP 2100 Interrupt Test with the Basic Binary Loader.

b. Set the switch register to the desired options. (See Table INT-1.)

c. Set Starting Address 100_8.

d. Press RUN. The computer either halts with 107000_8 displayed in MEMORY DATA, or the teleprinter types a "?". The user must now enter the select codes of all I/O slots to be tested.

e. If a 107000_8 halt is received, enter the select codes via the switch register as follows:

1. Enter each select code by setting the value in switch register bits 5-0 and press RUN. An accepted input is indicated by a halt with 107001_8 displayed.

2. Each select code must be in the range of 10_8-77_8 and does not have to be in sequence.

NOTE: If a select code entered is less than 10_8 (but not 00_8) or is duplicated, the computer halts with 107000_8 displayed in MEMORY DATA. The user must re-enter all select codes.

3. Terminate the input by entering a select code 00 in switch register bits 5-0. Successful input is indicated by a halt and 107077_8 displayed in MEMORY DATA.

4. Press RUN to continue the program.

f. If a "?" was typed, enter the select codes via the teleprinter as follows:

1. Type, in any order, the select codes of all I/O slots to be tested, terminating each line by CARRIAGE RETURN, LINEFEED.

2. Each select code entry must be in the range 10_8-77_8 and up to 72 characters can be input on one line. CARRIAGE RETURN, LINEFEED, commas, and spaces are ignored in scanning.

NOTE: If a select code entered is less than 10_8 (but not 00) or is duplicated, the teleprinter responds with "INP?". The user must re-enter all select codes.

3. Terminate input by typing a select code of 00.

Table INT-1

Switch Register Settings

Switch	
15	Enter new slot parameters.
14	If set, indicates that a teleprinter is <u>not</u> being used. If not set, indicates use of a teleprinter.
13	Suppress testing of central interrupt register.
12	Suppress error messages.
11	Suppress error halts.
10	Suppress end-of-pass message.
9	Suppress end-of-pass halt.
8-6	Spares.
5-0	Select code of slots to be tested (entry field).

Table INT-2

Halts and Messages

NOTE: If a program halt occurs and data is assoicated, the data is contained in the A and/or B-registers. If a message is printed (see Table INT-1 bits 10,12), and data is associated, the data is included in the message.

MEMORY DATA	Message	Comments
	21ØØ INTP. TEST	Introductory message.
	?	Enter select codes by teleprinter.
	INP?	Error in teleprinter input - Re-enter all select codes, press RUN.
107000		Enter first select code by switch register; or error occurred - Re-enter all select codes, press RUN.
107001		Enter next select code by switch register. Press RUN.
107077		All select codes in buffer; press RUN to continue.
102001	E-1 CLF Ø - SFC Ø	Error = can't clear, set, or test interrupt system
102002	E-2 CLF Ø - SFS Ø	
102003	E-3 STF Ø - SFC Ø	
102004	E-4 STF Ø - SFS Ø	
1030*xx*		Unexpected interrupt occurred on slot *xx* with the interrupt system off. Do not continue further.
102005	E-5 NI SC = *xx*	Error: No interrupt on select code *xx* (in A-register after halt).
102006	E-6 CIR = *xxxxxx* SB = *yyyyyy*	Error: Central interrupt register contents are *xxxxxx*, - (in A-Register after halt) should be *yyyyyy* (in B-Register after halt).

Table INT-2. Halts And Messages (cont.)

MEMORY DATA	Message	Comments
102007	E-7 DI SC = *xx*	Irrecoverable error: A double interrupt occurred on slot with select code *xx* (in A-register after halt).
1060*xx*		Error: An unexpected interrupt occurred on slot *xx*. Do not continue further.
102010	E-1Ø NI SC = *xx*	Error: No interrupt on slot with select code *xx* (in A-register after halt).
102011	E-11 UI SC = *xx* SB*yy*	Irrecoverable error: Unexpected interrupt with select code *xx* (in A-Register after halt). Expected an interrupt with select code *yy* (in B-register after halt).
102007		End of pass halt. (Octal pass count in A- and B-Registers after halt with the least significant bits in the A-Register.)
	EOP *x*	End of pass message. *x* = decimal pass count.

HP 2610A/2614A LINE PRINTER DIAGNOSTIC

HP Order No. 24275

11000 Wolfe Road
Cupertino, California 95014

Manual of Diagnostics
HP 02100-90130

June 1972

HP 2610A/2614A LINE PRINTER DIAGNOSTIC

The HP 2610A/2614A Line-printer Diagnostic program verifies proper operation of the HP 2610 Low-speed Printer or the HP 2614 High-speed Printer. The diagnostic contains eight individual tests. The tests can be run in serial combinations or singly. Using the switch register, the operator selects test options and other program options, such as test-section looping, teletype-message suppressing, and error-halt suppressing.

HARDWARE REQUIREMENTS

This diagnostic program is used in the HP 2100, HP 2114, HP 2115, and HP 2116 Computers. An optional test feature may be run if direct memory access (DMA) hardware is available. In addition to the HP 2610 or HP 2614 Line Printers, the 12845A line-printer interface is required. The teletype is used for error messages and operator communication. Program loading is done through a paper-tape reader, which can be a photoreader or the paper-tape reader of the teletype.

SOFTWARE REQUIREMENTS

This diagnostic is an absolute binary program. It is loaded using the basic binary loader (BBL). Before execution, the program must be configured. (See the configuration section test under "Test Sections".) The SIO teletype driver is used for the teletype.

TEST SECTIONS

The test sections are described as follows:

- Configuration Section

  This section configures the diagnostic program to the available hardware. The operator enters configuration parameters through the teletype in response to requests from the diagnostic.

- Initialization and Control Section

  After the interrupt system is initialized and the program header message is printed, the main control section is entered. The main control section executes tests according to the program options set by the operator.

- Test 1: Basic I/O Test

  Tests select-code decoding logic, flag control and sensing logic, and interrupt and interrupt control logic.

- Test 2: Preset and Status Test

  Verifies the interface response to the PRESET computer function; verifies MASTER CLEAR by the line printer START, STOP and POWER ON switches. Whenever MASTER CLEAR is not operating properly, a line of m's will be printed after the message "next line must be blank".

- Test 3: Character Set Test

  Prints one line of each printing character. Verifies that codes 0 through 40_8 produce blank output on the line printer.

- Test 4: Ripple Print Test

  Prints lines of all the printing characters, shifting the character set by one character each time a line is printed.

- Test 5: Triangular Print Test

  Prints 132 lines in a triangular pattern. The first line contains 132 characters; each successive line contains one less character. If the test is successful, unused printing positions contain blanks.

- Test 6: Vertical-format Control Test

  Vertical-format control functions are divided into two groups. The first group consists of the line-counter functions. The second group consists of the eight functions provided by the Vertical Format Control Unit (VFU).

  Line-counter functions tested are suppress space, single space, double space, triple space, space 18 lines, and space 45 lines.

  VFU testing is defined by test option bit 9. If bit 9 is set, the complete test, producing 18 pages of printout, verifies all holes on each VFU tape channel. If bit 9 is clear, the short test lists only one punch on each channel. See Table 1 for a list of the VFU control codes.

  Each format control test includes a line specifying the format control function to follow; the automatic-spacing test; and a completion message giving the elapsed time of the printing and spacing operations combined.

Table 1. Vertical-format Control Codes

Octal Code		Command
	Line Counter Functions	
00		Suppress space
01		Single space
02		Double space
.		.
.		.
.		.
77		Space 63 lines
	VFU Control Functions	
100	VFU Channel 1	Top of form
101	VFU Channel 2	Bottom of form
102	VFU Channel 3	Single space with form step over
103	VFU Channel 4	Double space with form step over
104	VFU Channel 5	Triple space with form step over
105	VFU Channel 6	Next 1/2 page with line 4 or 34
106	VFU Channel 7	Next 1/4 page with line 4, 19, 34, or 49
107	VFU Channel 8	Next 1/6 page with line 4, 14, 24, 34, 44, or 54

o Test 7: DMA Operation Test

This test is executed only if the operator answers YES to the question

H3 DMA? YES OR NO

output during the test configuration. (See instructions h and i in Operating Procedures.) If the operator answers NO and later selects Test 7, the message

NO DMA IN SYSTEM

is printed on the TTY. The print pattern produced is identical to that produced by test 3. The line-printer buffer is filled through the DMA hardware. Only the relationship of the service request logic of the line printer interface to the corresponding timing is tested.

NOTE: This test presumes the DMA hardware is working correctly.

o Test 8: Manual Printing Test

In this test the operator specifies three parameters for the print operation: the number of lines, the character(s), and the vertical-format control code to be used. (See Table 1 for vertical-format control codes.) The number of lines must be between 1 and 999. Printing starts at "top of form" and the spacing executes after printing. The result is that the position of the first printed line does not necessarily correspond to the format control code.

OPERATING PROCEDURES

a. Confirm that the interface card is properly installed and the line printer is properly connected.

b. Turn on the line printer (POWER ON/START). If the configured diagnostic tape is available, go to step k; if the configured diagnostic tape is not available, go to step c.

c. Load and configure the SIO teleprinter driver; then load the diagnostic program from paper tape using the BBL.

d. Load the program counter (P register) with the address 110_8. Press RUN. The following configuration dialogue occurs:

H1 TYPE SELECT CODE (OCTAL)

e. Key in the I/O select code of the line-printer interface, followed by a carriage return and line feed. The teletype prints the following message:

H2 TYPE TIME CONSTANT

f. Input 252 for HP 2100, 248 for HP 2114 or 2115, and 311 for HP 2116; then input a carriage return and line feed. The teletype prints:

H3 DMA? YES OR NO

g. Type YES if DMA present or NO, if DMA not present, followed by a carriage return and line feed. The teletype prints:

H4 CHARACTER SET? TYPE 64 OR 96

h. Input the size of the line-printer character set, 64 or 96, followed by a carriage return and line feed. The 96-character set has lowercase alphamerics plus additional special symbols. The teletype then prints:

H5 ENTER SWITCH REGISTER OPTIONS, PRESS RUN

i. Select the desired program options (see Table 2) by setting the appropriate bits in the switch register. Setting the appropriate bits establishes default-program option switch settings. These settings are in effect (stored in the internal switch register) when the configured program is started at step k. Press RUN. The teletype prints:

H6 DIAGNOSTIC CONFIGURED

j. The CPU halts with 107077_8 in the MEMORY DATA register. If desired, punch a copy of the configured diagnostic program by using the SIO System Dump program. The SIO Paper Tape Punch Driver must be loaded and configured before the System Dump program is loaded. Otherwise, go to step 1.

k. Use the BBL to load the configured diagnostic program. Set the Program Counter (P register) to 100_8.

1. Press PRESET INTERNAL and PRESET EXTERNAL (or simply PRESET if computer is not HP 2100). At this point the default program options in the internal switch register (see step i) may be overriden by setting switch register bit 0. Set switch register bit 0 off if default options are desired.

m. Press RUN. The diagnostic executes according to the options selected. For the complete diagnostic to run without operator intervention, the following options must be in effect:

- o Tests 2 and 8 are not selected (switches 2 and 8 are clear).
- o Error halts are suppressed (switch 14 is set).
- o Diagnostic does not halt at end of each test section (switch 15 is clear).

NOTE: If error halts are not suppressed, press RUN to continue the test after each halt. Only the error message producing the first halt is valid. Succeeding error messages must be interpreted with caution.

After completion of each test, the following message is typed:

TEST COMPLETED

Following a complete cycle of the diagnostic program, the program halts with 102077_8 in the MEMORY DATA register.

n. To restart the test from the beginning, select new test options and press RUN. The program may be reconfigured at any time by starting CPU from address 110_8.

Table 2. Program Options: Switch Register Settings

Bit	Function
0	Set to override the internal switch register and read program options from hardware switch register.
1	Set to execute the Basic I/O test.
2	Set to execute the Preset and Status Test.
3	Set to execute the Character Set Test.
4	Set to execute the Ripple Print Test.
5	Set to execute the Triangular Printing Test.
6	Set to execute the Vertical Format Control Test.
7	Set to execute the DMA Operation Test.
8	Set to execute the Manual Printing Test.
9	Set to execute the long form of the Vertical-format Control Test.
10	Set to suppress nonerror messages.
11	Set to suppress all messages.
12	Set to halt the diagnostic at the end of a complete test cycle.
13	Set to loop on current test.
14	Set to suppress error halts.
15	Set to halt at the end of each test.

DIAGNOSTIC MESSAGES

Messages from the teletype are classed in two categories:

1. Control dialogue with test operator always preceded by the letter H.

2. Line printer error (test failure), always preceded by the letter E.

See Table 3 for the list of the messages that may be output on the teletype during the course of the test.

Table 3. Diagnostic Messages

Memory Data Setting	Program Segment	Message	Comments
No halt	Conf	H1 TYPE SELECT CODE (OCTAL)	Select code of line printer interface
No halt	Conf	H2 TYPE TIME CONSTANT	252 for 2100, 248 for 2114/2115, 311 for 2116
No halt	Conf	H3 DMA? YES OR NO	DMA available?
No halt	Conf	H4 CHARACTER SET? TYPE 64 OR 96	Character set specification
102076	Conf	H5 ENTER SWITCH REGISTER OPTIONS, PRESS RUN	Enter through switch register
102077	Conf	H6 DIAGNOSTIC CONFIGURED	Ready to execute
102001	T1	E1 CLF OR SFS FAILED	Test ability of clear flag and test SFS
102002	T1	E2 SFC FAILED - FLAG CLEAR	Test ability of SFC instruction
102003	T1	E3 STF OR SFC FAILED	Test ability to set flag and test SFC instruction
102004	T1	E4 SFS FAILED - FLAG SET	Test SFS instruction

Table 3 (cont). Diagnostic Messages

Memory Data Setting	Program Segment	Message	Comments
102005	T1	E5 FAILED TO INTERRUPT	Test interrupt logic
102006	T1	E6 RETURN ADDRESS INCORRECT	Wrong return address after interrupt
102007	T1	E7 FLAG BUFFER FAILED TO RESET	Check interrupt acknowledge logic
102010	Any	E10 PRINT TIME OUT	Line printer time out
102011	Any	E11 BUFFER LOAD TIME OUT	Line printer time out
102070	T2	H7 PRESS PRESET AND RUN	
102071	T2	H8 PRESS POWER ON (LP) PRESS RUN	
102072	T2	H9 PRESS START (LP) PRESS RUN	
102012	T2	E12 FLAG NOT SET AFTER PRESET	POPIO malfunction
102013	T2	E13 CONTROL SET AFTER PRESET	CRS malfunction
102014	T2	E14 STATUS ERROR - READY	Line printer interface malfunction
102015	T2	E15 STATUS ERROR - NOT READY	Line printer interface malfunction
102016	T1	E16 SKIP ON NON-SKIP I/O INSTRUCTION	Check skip logic
102017	T1	E17 CLC FAILED	Check clear control logic
No halt	T8	H12 TYPE # OF LINES	$1 \leqslant \# \leqslant 999$
No halt	T8	H13 TYPE CHARACTER CODE (OCTAL)	
No halt	T8	H14 TYPE FORMAT CONTROL CODE (OCTAL)	
102020	T7	E20 DMA TIME OUT	Check DMA logic

SOFTWARE MANUAL CHANGES

HP 2610A/2614A LINE PRINTER DIAGNOSTIC

(02100-90130)
Dated June 1972

Updates to this publication as well as changes to the Manual Change Sheet itself are listed below.

October 1972

Change Number	Page	Instructions
1	5	Revise the text under Test 8, Manual Printing Test, to add an optional time delay: In this test the operator specifies four parameters: the number of lines, the character, the vertical format control code to be used and the time delay inserted between the initiation of the printing of each line.
2	10	Insert the following line before the last line on the page: No halt T8 H15 TYPE TIME DELAY (MSEC)

HP 2100 TAPE PUNCH TEST

Order No. HP 24190

HEWLETT hp PACKARD

11000 Wolfe Road
Cupertino, California 95014

Manual of Diagnostics
HP 02753-90093

April 1971

HP 2100 TAPE PUNCH TEST

This diagnostic confirms proper operation of the HP 2753 High Speed Tape Punch with the 12597A-03 Interface Kit and the HP 2100 computer with 2K or larger memory by performing a complete functional check. The program also allows the user to generate tapes containing "worst case" data patterns and special characters to aid in hardware analysis.

HARDWARE CONFIGURATION

This diagnostic program requires a 2100 computer, a teleprinter, a 2753 High-Speed Tape Punch, and optionally an HP 2737, HP 2748, or an HP 2758 High Speed Tape Reader.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

To run the diagnostic, the operator selects the appropriate switch options from Table TP-1 and presses RUN.

If an error is detected, the program prints a message on the teleprinter. All messages and their meanings are listed in Table TP-2.

If a trap cell halt occurs, $1020xx_8$ is displayed. (xx is the trap cell location.) The cause of a trap cell halt must be determined by the user; after the error is corrected, the diagnostic program is restarted.

After the functional test is complete, the computer halts. The punch may now be used to generate a standard test tape from data in memory. This test tape is then read to check for proper operation of the tape punch.

A special test tape, consisting of a single character continuously punched may also be prepared, to diagnose specific malfunctions.

PROGRAM ORGANIZATION

ABLEX — Sets the I/O instructions to the Select Code for the High Speed Tape Punch.

FUNCTIONAL TEST — Checks the ability of the PRESET to initialize properly, then checks the punch and interrupt capabilities. The routine initializes a punch operation, forcing an immediate interrupt, and analyzes the response. A completion message is typed. Forty leader characters are punched to feed out the character (377) punched in the forced interrupt. The computer then halts with 102001_8 displayed to allow user analysis.

OPTION ANALYSIS — Allows the operator to use the switch register (Table TP-1) either at the start or end of the program to select these options: punching and/or reading the character stored in switches 8-15 of the switch register, running the punch test under Interrupt Control, and specifying the character to be punched or read.

SELECTED OPERATION — Performs the punching and reading for both special character and standard tapes. A special character tape contains a continuous punching of character set into switch register bits 8-15. A standard data tape contains data in seventeen foot sequences separated by a fifteen leader character gap called a resync point. This resync point provides a convenient starting point for tape testing. Also, when an extremely bad tape is encountered and no identifiable tape data pattern can be established (5 consecutive data errors), the tape forward spaces to a resync point before continuing the data test. The seventeen foot

area of tape is composed of eight groups of data each containing eight data blocks. The data blocks contain different numbers of characters as listed below:

Block	Characters
1	40
2	20
3	50
4	2
5	99
6	10
7	30
8	5

The data pattern of the data blocks is modified by the program using this character table:

001
200
002
100
004
040
010
020

The actual data starts with the character 377_8 (Ch. A1). 377 is modified by the addition of the first table character, 001_8. This character (Ch. A2) is punched, complemented, and its complement is punched. Character A2 is then modified by the next table entry, 200_8. This character (Ch. A3) is punched, complemented, and the complement is punched. This process is repeated until

the last character table entry, 020_8, is used. Then the table is referenced back to the character 001_8 and modification continues until character A_n. This entire process takes up seventeen feet of tape and is repeated after each resync point.

Example of initial data sequence:

Character		
1	377	
2	000	(377 +1)
3	377	Complement
4	200	(000 + 200)
5	177	Complement
6	202	(200 + 002)
7	175	Complement
8	302	(202 + 100)
9	075	Complement
10	071	Complement

LIMITATIONS

The program does not test for low tape status while punching with switch seven set ON.

After a roll of tape has been punched the program detects the low tape status and prints the message TAPE LOW. Using a small roll of tape enables the user to test the low tape status sooner.

OPERATING INSTRUCTIONS

a. Set the teleprinter and high-speed tape punch ON.

b. Load the SIO Teleprinter driver using the Basic Binary Loader or the Basic Binary Disc Loader, then configure that driver.

c. If a high speed tape reader is to be used to check the punched test tape, load the SIO Tape Reader driver using the BBL or BBDL, then configure that driver.

d. Load the HP 2100 Tape Punch Test using the BBL or the BBDL.

e. Set a starting address 2_8.

f. Set the Tape Punch select code (I/O address) in bits 5-0 of the switch register.

g. Press RUN. The diagnostic halts with 102000 in MEMORY DATA when the configuration is complete.

h. If desired, use the SIO System Dump program to punch a copy of the configured teleprinter driver (and the tape reader driver if loaded) along with the configured diagnostic tape.

i. Set the starting address 100_8.

j. Press EXTERNAL PRESET and RUN to execute the functional test section.

k. At the completion of the functional test, the teleprinter types "FUNCTIONAL TEST COMPLETED" and the computer halts with 102001 in MEMORY DATA.

To punch a standard test tape and use it to test the punch unit, proceed as follows:

l. Set switch register bit 0 ON.

m. Press RUN. The tape punch punches out a standard test tape with six inches of leader and trailer. When sufficient tape has been punched, set switch register bit 7 on. Punching terminates at the next resync point.

n. Tear off the tape from the tape punch, rewind it and place it in the tape reader device.

o. Set switch register bit 0 OFF.

p. Press RUN. The test tape is read into the computer and checked. Errors are printed on the teleprinter.

q. When END OF TAPE or other termination conditions occur, the computer halts with 102001 in MEMORY DATA. Execute steps 1 through q for retesting.

To punch and check a special tape, containing only one puched character, perform the following steps:

r. Set switch register bit 2 ON.

s. Set the octal code of the character to be punched in switch register bits 15-8.

t. Press RUN. The special character test tape is punched with six inches of leader and trailer. To terminate the punching operation, set switch register bit 6 ON.

u. Tear off the tape from the tape punch device, rewind it and place it in the tape reader device.

v. Set switch register bit 2 OFF.

w. Press RUN. The tape is read by the computer and checked. Errors are reported as in the standard test tape except that no character number is reported.

To reconfigure the diagnostic, restart the program at address 2_8.

To start the functional tests, start the computer at address 100_8.

To execute at the option analysis section, start the program at address 110_8.

Table TP-1

Program Options--SWITCH REGISTER Settings

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bits	Function
0	If set ON, punch a standard or special data tape (according to bit 2) with or without interrupt control (according to bit 1). If set OFF, read either the standard test tape or the special test tape (according to bit 2) from the High Speed Tape reader or the Teleprinter Tape Reader.* Reading is not performed under interrupt control.
1	If set ON, punching operations are run under interrupt control. The operating procedure for the program is not changed. If set OFF, punching operations are run under non-interrupt control.
2	If set ON, punch the character stored in bits 8 through 15 (bit 0 ON), or read the character stored in bits 8 through 15 (bit 0 OFF). If set OFF, tape being punched or read is the standard test tape. Changing the content of the switches during program operation has no effect on the data pattern as the switches are only modified upon program start or TERMINATE.
3	Set ON to momentarily interrupt the test at any time without affecting the test or data sequence. Set OFF to continue the test.
4	Set ON to interrupt the test before processing the 15 leader characters (during either a punch or a read) that comprise a resync gap on the tape. Set OFF to continue the test. If an option change is desired, set the terminate switch (bit 6) ON before setting bit 4 OFF. Make the changes, then set bit 6 OFF to continue.

* The tape is read in four character blocks and then checked. Thus the character is error may not be the one under the read head during error printouts.

Table TP-1 (cont). Program Options--SWITCH REGISTER Settings

Bits	Function
5	Set ON to interrupt a read operation if an error is found during data tape analysis. Set OFF to continue reading, but set ON immediately thereafter to continue "error interrupt." If the tape is removed for inspection during an error pause, reload the tape carefully to insure that no data character is re-read or skipped.*
6	Set ON to terminate the current operation in an orderly manner. When termination occurs, a "TERMINATE" message is typed and the program halts with 102001_8 displayed. Make option changes at this time (if desired) as the program restarts at the option analysis section when RUN is pressed. Set OFF to continue testing at the option analysis section of the program.
7	Set ON to terminate punching or reading at the resync gap. The switch may be set at any time during the operation; the program terminates as described.
8-15	Set bits 8-15 to the special character to be punched in or read from the special test data tape (bit 2 set ON).

* The tape is read in four character blocks and then checked. Thus the character in error may not be the one under the read head during error printouts.

Table TP-2

Diagnostic Messages

Messages	Meaning	Action
CLF ERROR	The Punch Flag flip-flop is set but the CLF instruction did not clear it.	
EMBEDDED LEADER -TERMINATE-	Three consecutive leader characters read in a data block.	Space tape to next resync point. Press RUN.
FLAG CLEAR ON PRESET	The Punch Flag flip-flop is not set.	Set STARTING ADDRESS 100_8. Press EXTERNAL PRESET. Reset the options in the switch register. Press RUN.
FUNCTIONAL TEST COMP	Functional Test completed.	Check teleprinter messages for equipment status. a. To rerun the Functional routine: Set STARTING ADDRESS 100_8. Press EXTERNAL PRESET. Reset the options in the switch register. Press RUN. b. To continue the run of the program, set the desired switch options (see Table TP-1) and press RUN.
G *xxxxxxxx* B *xxxxxxxx xx xx*	Character error.	G *xxxxxxxx* is a good data pattern where: *xxxxxxxx* is a good character. B *xxxxxxxx xx xx* is a bad data pattern where: *xxxxxxxx* is a bad character. *xx* is the character of the data block that is an error. *xx* is the number of characters in the data block.

Table TP-2. (cont). Diagnostic Messages

Messages	Meaning	Action
INTERRUPT ON PRESET	Erroneous interrupt in Functional Test.	Set STARTING ADDRESS 100_8. Press EXTERNAL PRESET. Press RUN.
LONG LEADER	More than fifteen leader characters at a resync point.	Check tape for correct data resequencing. Press RUN.
NO INTERRUPT FLAG SET	An interrupt situation forced by the program did not occur.*	Terminate the diagnostic program.
RESYNC ERROR- 5 CONSECUTIVE ERRORS	Five consecutive errors are detected.	Space tape to next resync point. Restart routine.
SHORT LEADER -TERMINATE-	Fifteen leader characters have not been read at a resync point.	Backspace tape in the leader area and press RUN.
STF ERROR	The Punch Flag flip-flop is clear but the STF instruction did not set it. Program halts.	
SYSTEM CLF Ø ERROR	The system flag flip-flop is set but the CLF flag instruction did not clear it.	Check other error messages for possible failure association.
TAPE LOW	Tape supply is low.	Install a new tape supply.
-TERMINATE-	Diagnostic program is terminated, switch six is ON, bad data characters, embedded leader, "End-of-Tape" or "Tape Low."	Change any desired options or check the tape for positioning at the resync leader. Press RUN.

*At the time of the forced interrupt, the STF 0, STF (punch), CLF 0, CLF (punch), SFC 0, SFC (punch) and SFS (punch) commands have been tested. OTA and STC can be checked by looking for character of value 377 on the punch tape.

HP 2892A CARD READER DIAGNOSTIC

HP Order No. 24267

HEWLETT hp PACKARD

11000 Wolfe Road
Cupertino, California 95014

Manual of Diagnostics
HP 02892-90006

August 1972

Introduction

This diagnostic confirms proper operation of the HP 2892A Card Reader and the HP 12924A Interface in HP 2114, 2115, 2116, or 2100A Computers. Designed for ease of testing, the program allows the user to select a set of tests and execute them in order or to repeat a specific test for extensive testing of card-reader functions.

HARDWARE CONFIGURATION

The diagnostic can be run on the HP 2114, 2115, 2116, or 2100A Computers with or without DMA. The computer must have a minimum memory size of 4K. If the diagnostic is run on any computer other than the HP 2100A, a system console device must be used to configure it. If the diagnostic is run on an HP 2100A Computer without an I/O console device, it is configured by default to operate only according to the conditions described in "Program Organization."

PROGRAM ORGANIZATION

Scope

The program tests basic card-reader functions first and, on the basis of results from these tests, proceeds to test the more complex functions. The operator should correct errors discovered during early stages of operation before continuing with the more complex tests.

Priority logic (PRH and PRL) is not tested during execution of this diagnostic. However, during testing of the interface board, trap-cell halts can occur if an interrupt occurs on a select code other than the card-reader select code. For proper testing of the select-code decoding logic, the card-reader select code should *not* be a multiple of 10_8 (10_8, 20_8, 30_8. . .).

Running Modes

Card readers use a hardware data buffer and a hardware status word. Table 1 shows the relationship between one character of data from a column in a data card and the corresponding bits in the card reader data buffer. Table 2 lists the status bits of the card reader and their meanings as used by the diagnostic program.

Table 1. Data Word Format

Data Buffer Bit	Card Data Row
0	9
1	8
2	7
3	6
4	5
5	4
6	3
7	2
8	1
9	0
10	11
11	12

Table 2. Status Word Format

Bit	Meaning
0	Card reader (CR) in test, not ready, or busy mode
1	Trouble during read. Pick, light current, card motion, or timing error
2	Card reader off line
3	Lost data
4	Not used
5	Hopper empty or stacker full
6	Stacker full
7	END-OF-FILE switch on and hopper empty
8	Pick flip-flop set
9	Error (L/D)
10	Reserved
11	Motion check/pick check
12	No read-in-progress
15	End-of-process

WITH CONSOLE DEVICE. The program can be operated with or without a teleprinter (I/O console device). If a teleprinter is used, the operator must first load and configure the SIO teleprinter driver (or the equivalent driver for the I/O console device used instead of a teleprinter). Then the operator loads the HP 2892A Card Reader Diagnostic tape and configures the diagnostic in two steps. First he enters the desired program options into the switch register; the program diagnostic configuration section loads these selected options into the internal software register. Next the operator answers the series of questions output by the program (detailed in "Operating Instructions"). Once the questions are correctly answered, the program halts. If desired, the operator can load and execute the SIO System Dump to obtain a paper-tape copy of the configured SIO driver and configured diagnostic program.

WITHOUT CONSOLE DEVICE. The operator has two options for diagnostic operation:

Option 1: Option 1 allows the operator to use the diagnostic with the default configuration. He loads the diagnostic program into memory and sets a starting address of 100_8, thus bypassing the configuration section.

To run the diagnostic in the default mode the operator must operate with

- An HP 2100A Computer without DMA
- A card-reader select code of 13_8
- A blank special data test card
- The external hardware switch register only

NOTE: Since the configuration section is bypassed, no software switch register is created.

Option 2: To change the default configuration to run on a computer with a timing cycle different from that of the HP 2100A. (Delay constants for the HP 2100A, 2114, 2115, and 2116 Computers are shown in Table 3.)

Table 3. Computer Timing Constants

Computer Type	Delay Constant
2100A	-252
2114	-248
2115	-248
2116	-311

Option 2 enables the user to run the diagnostic without an I/O console but to change the default configuration (for example, to run on a computer with a cycle timing different than that of the HP 2100A).

Table 4 describes the values which must be loaded into specific locations in the diagnostic to modify the default configuration. The left column shows the labels of program locations. The right column describes what values can be inserted into the location to configure the diagnostic.

Consult a source listing of the diagnostic (the program is written in assembly language) for the exact address of the locations specified in Table 4 and change the values of the locations according to the desired configuration by using the computer switch register and front-panel buttons. For information on modifying memory locations through the computer front panel, consult Software Operating Procedures *HP 2114 Front Panel Procedures (5951-1372)*, *HP 2115/2116 Front Panel Procedures (5951-1370)*, or *HP 2100A Front Panel Procedures (5951-1371)*.

Table 4. Program Configuration Locations

Program Label	Action
ISWR	Set ISWR – 0 to select program options from the internal software switch register.
	Set ISWR – 1 to select program options from the external hardware switch register.
TCNT	Set TCNT equal to one of the constants specified in Table 4, depending upon the computer being used.
CRILA to CRILE	The addresses of all instructions referring to the card-reader select code are between CRILA and CRILE. Change the six least-significant bits (5 to 0) of each of the words specified to the card-reader octal select code.
DMAF	Set DMAF = 0 if DMA is not available.
	Set DMAF = 1 if DMA is available.
SPDBA	SPDBA points to the special test card data buffer. Load the special data images desired, starting at the address located in SPDBA.

Error and Information Messages

During execution the diagnostic prints error and information messages on the teleprinter (see Appendix A for error and information messages). The diagnostic halts (to allow operator response) after it prints an information message shown in Appendix A.

If program option bit 10 is set, the diagnostic suppresses all nonerror messages except those marked with an asterisk (in Appendix A). However, setting bit 10 does not suppress the halt associated with a nonerror message.

If program option bit 14 is cleared, the diagnostic halts after printing an error message, displaying 102075_8 in the MEMORY DATA register and the octal step number in the A register.

If program option bit 15 is set, the diagnostic executes the current step, displays 102076_8 in the MEMORY DATA register, the octal step number in the A register, prints the octal step number on the teletype, and halts. The operator presses RUN to resume running the diagnostic at that step.

If a teleprinter is not available, the operator must rely on the coded halts displayed in the MEMORY DATA register and the octal step numbers displayed in the A register. By consulting the appropriate step number (prefixed by E or H) in Appendix A, the operator can determine the correct response to the halt.

TEST SECTIONS

The program is divided into nine sections. Each section is comprised of one or more uniquely numbered steps. Each step performs one or more functions or tests. Sections 1 through 9 are selected by setting program option bits 1 through 9, respectively. The user can halt after each step by setting program option bit 15 or loop through a step or group of steps by setting program option bit 13. Some of the sections below require specially modified cards for complete testing, although the user can run the diagnostic in a shortened testing mode requiring a standard test deck and little operator intervention.

Configuration Section

The configuration section configures the program for the particular hardware devices being used, loads the program option switch-register settings into the internal software switch register and stores the special test card data for use by section 6. If the operator chooses not to execute the configurations section, the diagnostic configures itself for an HP 2100A Computer without DMA, card-reader select code 13_8, and a blank special data test card for section 6. Program options are specified through the external hardware switch register only; no software switch register is created in default configuration.

Initialization Section

The initialization section sets trap-cell halts in all unused locations. The halts are $1060xx_8$ where xx_8 is the trap-cell location. Finally, the section prints the introductory header message at the start of diagnostic execution (if program option bits 10 and 11 are clear). The operator must set program option bit 11 if no teleprinter is used; otherwise, the program will loop continuously waiting to output a message.

Control Section

The control section monitors the program options set in the switch register and selects the corresponding sections for execution. After the program executes the initialization section, the control section scans the switch register and executes the sections selected. If program option bit 12 is clear, the control section scans the switch register again after one cycle of execution through the selected sections. If program option bit 12 is set, the program halts with 102077_8 in MEMORY DATA at the end of one cycle through the selected sections after printing the message DIAGNOSTIC COMPLETED. The user may execute another cycle through the selected sections by pressing RUN or restart the program at any time by setting a starting address of 2000_8 and pressing RUN. The control section scans the switch register and executes the selected sections.

Basic I/O (BI/O) Section

The basic I/O (BI/O) is selected by setting program option bit 1. It tests the select code decoding logic, flag control and sensing logic, and the interrupt and interrupt control logic. Any errors discovered are reported by one of the error messages numbered from E2 through E14 in Appendix A.

Status Indicator (STEST) Section

The status indicator test (STEST) is selected by setting program option bit 2. This test checks the RESET switch functions, manual front-panel button functions and the status indicator bit functions. Specially modified cards, required for the test, are loaded into the card-reader hopper in the order listed below.

1. A card cut in half, and the two halves taped together to form a double-thick "half-card" to check the card motion circuitry (see Figure 1). This card is placed in the card-reader stacker. Two unmodified cards, used with this special card, are placed in the hopper.

2. A card with a ¼-inch-square notch cut from the leading edge of the card checks the light current error circuits (see Figure 2).

3. Two cards taped together from approximately column 40 to column 80 to check the pick mechanism (see Figure 3).

During execution of STEST, halts 102016_8 through 102071_8 (in the computer MEMORY DATA register) occur to allow the operator to prepare for the next test segment. If a teleprinter is available and program option bits 10 and 11 are clear, a message is printed on the teleprinter along with the halt. The user should refer to Table 3 for the meaning of the halt and follow the appropriate instructions.

NOTE: The user can avoid the special cards test in this section by setting program option bits 15 and 1. The other tests in the section are still executed.

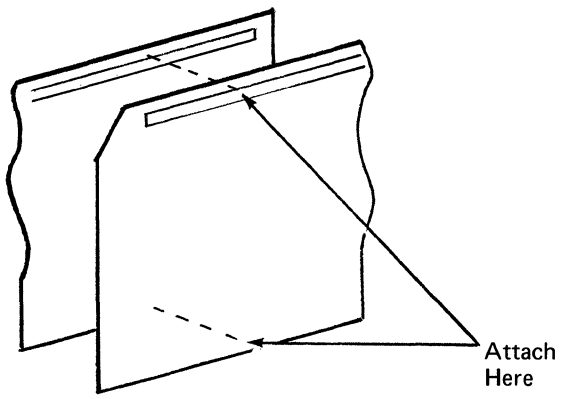


Figure 1. Torn Card in Stacker

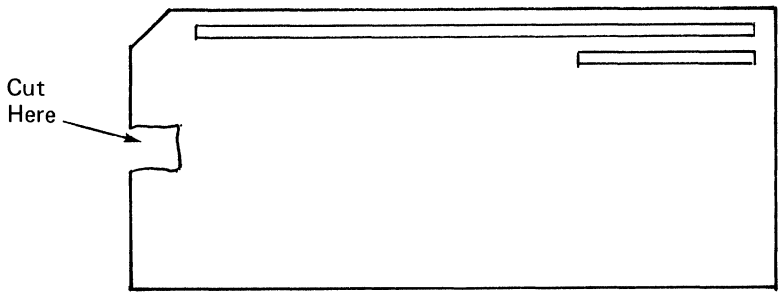


Figure 2. Notched Card in Hopper

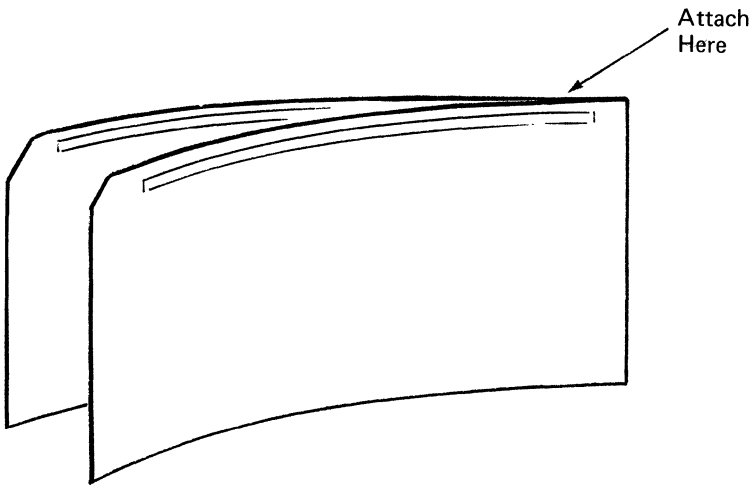


Figure 3. Joined Cards in Hopper

Functional (FTEST) Section

The functional test (FTEST), selected by setting bit 3, tests much of the card-reader interface control and status logic (except priority logic PRH and PRL) without requiring any operator intervention. Several of the tests performed in the STEST section are repeated so that card reader and interface functions can be tested without special cards or operator intervention. Error messages and halts (specified in Appendix A) indicate the function of the tests and the possible error conditions which may occur during the tests.

Standard Data (STDT) Section

The standard data test (STDT), selected by setting program option bit 4, tests the data paths in the card reader and interface. The user loads a special test deck, provided with the diagnostic, which is punched in a "worst-case" pattern. The program reads the data from the card reader and compares it to the expected data stored as part of the program. The program outputs the data read and expected if the two do not agree (if a teletype is used and if program option bit 11 is clear). If no teletype is used and program option bit 14 is clear, the program halts with 102075_8 in the computer MEMORY DATA register with the appropriate octal message number displayed in the A register. Consult Appendix A for the meaning of the halt. This test section terminates after the program reads 50 cards or if the operator clears program option bit 4 before the 50 cards are read. If the operator sets bit 13 (loop on last step), the program ignores the card count and reads and compares card-reader data continuously until the operator clears program option bit 4.

To ensure that the program executes the data compare test (step 133) when the loop option (program option bit 13) is set, the operator sets program option bit 15 before executing the standard data section (see Table 4). The program halts at the end of each step with 102076_8 in the computer MEMORY DATA register and the octal step number in the A register. When the program halts with 133_8 displayed in the A register, the operator sets program option bit 13 (bit 15 is clear) and presses RUN. The program then reads and compares continuously.

Read Rate (RRT) Section

The read-rate test (RRT), selected by setting program option bit 5, does not terminate if bit 5 is clear during section execution. The section reads 50 cards at the maximum rate, then determines the maximum rate and prints it on the teleprinter. The test is terminated when the program reads 50 cards. This section requires a teleprinter to report the calculated reading rate.

Special Data (SPDT) Section

The special data test (SPDT), selected by setting program option bit 6 and terminated by clearing bit 6, performs the same function as the standard data section, except that the data read is compared with the special data card entered during program configuration. If no special data was input during configuration (or if the program is running under default configuration), the program compares the data read to a zero (all blank) card.

Flag Count (FCT) Section

The flag-count test (FCT) is selected by setting program option bit 7 and terminated by clearing bit 7. It reads cards and counts the number of flags from each card. If the card does not generate 80 flags, the teleprinter indicates the number of flags that were detected. When the test is terminated, that is, either when all the cards in the hopper are read or bit 7 is clear, the teleprinter prints the total number of cards read and the number of cards with missing flags.

Time Pick Rate (TPR) Section

When the timed pick rate test (TPR) is selected (by setting program option bit 8), the section requests the operator to type in a pick rate from 1 to 600 cards per minute. After the operator types in the pick rate (followed by a carriage return), the section outputs a pick command at the specified rate. The diagnostic does not check status either before or after a pick command; this section can be used under any card-reader malfunction conditions. The card-reader flag is cleared each time a pick command is given.

This test requires a teleprinter device.

List Option Section

Selecting the list option test (by setting program option bit 9) enables the user to list the standard test data (stored in the program) and special test data (defined during program configuration) as well as read and list any cards desired from the reader. When control enters this section, a message is printed requesting the operator to specify the list mode. The operator responds by typing an A for ASCII list or a B for binary list followed by a carriage return. After the response, the section asks for the list type. The user responds by typing ST (list the standard test card data), SP (list the special test card data defined during configuration), or RL (read the cards and list them) followed by a carriage return.

After the second user response, the section lists the standard or special test data or reads and lists the cards in the reader. If the operator responds with B, the test lists 12 bits per card column (80 columns per card) on a line, one column per line (12 row on the left). If the operator specifies mode A, the Hollerith punch codes produced by an IBM 029 Keypunch are converted to their corresponding ASCII characters. The five exceptions to the keypunch key and ASCII character correspondance are as follows:

ASCII Symbol	029 Key	Hollerith Punches
[	Cent mark (¢)	12-8-2
\	0-8-2	0-8-2
]	Not mark (¬)	11-8-7
↑	Vertical bar (|)	12-8-7
←	Underscore (_)	0-8-5

Hollerith punches regarded as invalid by the program are interpreted as a question mark (?). The section terminates and control returns to the control section after the standard test card data or the special test card data is listed. The section continues to read and list cards (if that option was choosen) until program option bit 9 is cleared.

Operating Procedures

SWITCH REGISTER SETTINGS

Switch register settings for program options are summarized in Table 5.

Table 5. Switch Register Settings

Bit	Meaning
0	Set to select program option control from the external hardware switch register. Clear to select program option control from the internal software switch register.
1	Set to execute the Basic I/O (BI/O) Section.
2	Set to execute the Status Indicator (STEST) Section.
3	Set to execute the Functional (FTEST) Section.
4	Set to execute the Standard Data (STDT) Section.
5	Set to execute the Read Rate (RRT) Section.
6	Set to execute the Special Data (SPDT) Section.
7	Set to execute the Flag Count (FCT) Section.
8	Set to execute the Timed Pick Rate (TPR) Section.
9	Set to execute the List Section.
10	Set to suppress nonerror messages (except for those messages identified by an asterisk in Appendix A).
11	Set to suppress printing of all error messages.
12	Set to halt execution after one cycle through the program and print DIAGNOSTIC COMPLETE message. Clear to execute multiple cycles of the program without halting after each cycle.
13	Set to loop the currently executing program step.
14	Set to suppress error halts.
15	Set to halt at the end of the currently executing step.

OPERATING INSTRUCTIONS

If a tape copy of the *configured* HP 2892A Card Reader Diagnostic is available, skip to step g below. To configure the diagnostic program, start at step a.

a. Use the Basic Binary Loader (BBL) to load the SIO teleprinter driver, then configure the driver.

b. Use the BBL to load the unconfigured diagnostic tape. To run the diagnostic in default configuration, skip to step f. To configure the diagnostic without using the teleprinter, perform the steps outlined in Table 5 and continue with step f. Otherwise, if a teleprinter is available, continue with step c.

c. Set a starting address of 2_8.

d. Set the switch register to the desired options according to Table 5. (If the operator sets bit 0, the program ignores the internal switch register during execution and reads options from the external switch register only).

e. Press the PRESET button(s), then press RUN. The program prints the internal switch register settings in binary form and outputs the series of questions shown below. Type the answer to each question on the teleprinter keyboard, followed by pressing the return and linefeed keys after each answer. If the operator response is invalid, the program types INVALID INPUT. Retype the entry.

Message	Response
1. ENTER COMPUTER TIMING CONSTANT. 3 DIGITS.	Type the appropriate positive constant from Table 3 for the computer being used. Do not type the minus signs.
2. CR SELECT CODE?	Type the card reader octal select code.
3. DMA AVAILABLE?	Type YES or NO.
4. ENTER SPECIAL TEST CARD?	Type YES if a special data test card will be used in Section 6. Otherwise, type NO.

If the operator responds NO to question 4, the special data test (section 6) uses a blank (all zero) card with an 80-column range. The program prints no further messages except the CONFIGURATION COMPLETE message. If the operator responds YES to question 4, the program asks the following questions:

5. ENTER WITH READER?	To enter the special data through the card reader, type YES. To enter the special data through the switch register, type NO.

If the operator types YES to question 5, the program prints

LOAD CARD. START CR. PRESS RUN.

and halts with 107001_8 in the MEMORY DATA register. Place the special data card in the reader and start the reader. Press RUN. The program reads the card.

If the operator types NO to question 5, the program prints

CLEAR SWITCH REGISTER.

Clear all switch-register bits, then set bits 0 through 11 to the desired column bit pattern. Set bit 15, then clear it. One column of data enters into the program each time switch 15 is set and cleared (toggled). If switch 14 is set when bit 15 is toggled, the program terminates data entry and sets the remaining undefined columns to the bit pattern in switches 0 through 11. Data entry is also terminated after column 80 has been defined.

After the operator enters the special data (either through the card reader or the switch register), the program types

6. LIST SPECIAL DATA?	Type YES to list the special data; otherwise, type NO.

If the operator responds YES to question 6, the program asks

ASCII OR BINARY LIST?

Respond with either ASCII or BINARY, as desired. The program prints the special data. In ASCII mode, invalid character codes are printed as a question mark (?); otherwise, the ASCII character responding to the code is printed. The program prints

CONFIGURATION COMPLETE

and halts with 107077_8 in the MEMORY DATA register.

f. Use the SIO System Dump program to punch a copy of the configured test tape (and the configured SIO teleprinter driver if it was loaded). If a tape copy is not desired, skip to step h.

g. Use the BBL to load the configured diagnostic tape.

h. Set a starting address of 100_8.

i. If test options other than those specified during configuration are desired, set the external switch register according to Table 5.

j. Press the PRESET button(s), then press RUN. The diagnostic executes according to the program options selected.

1. To skip the "special cards" test in the STEST section, set program option bits 15 and 1 after the computer halts with 102057_8 displayed.

2. To terminate error printing during message output in the STDT and SPDT sections, set program option bits 13 and 1. Message output stops immediately and the section halts with 102067_8 displayed in the MEMORY DATA register. When the operator presses RUN, the diagnostic starts execution at the beginning of the section.

APPENDIX A
Diagnostic Error Messages

Message Number[1]	Memory Data	Program Segment	Comment
-----	102000	INIL	I/O buss not zero. Check interface board IOBI outputs.
H1	-----	INIL	Header message.
E2	-----	BI/O	No skip on SFS or SFC. Check select code decode and skip logic.
E3	-----	BI/O	Skips on SFS and SFC. Check skip logic.
E4	-----	BI/O	CLF failed, no skip on flag clear after CLF. Check CLF logic.
E5	-----	BI/O	STF failed, no skip on flag set after STF. Check STF logic.
E6	-----	BI/O	Flag set with STF with select code other than the reader's. Check select code decode logic.
E7	-----	BI/O	Does not interrupt. Check control, flag buffer, and IRQ logic.
E10	-----	BI/O	Card reader interrupts with interrupt system off. Check IEN logic.
E11	-----	BI/O	Two interrupts on one flag. Check interrupt acknowledge logic.
E12	-----	BI/O	Interrupts after CLC 0. Control or CRS malfunction.
E13	-----	BI/O	Interrupts after CLC. Control or CLC malfunction.
E14	-----	BI/O	STC CR, C does not clear card reader flag.
H15	-----	BI/O	Basic I/O tests completed.
H16	102016	STEST	Press EXTERNAL PRESET, then press RUN.

[1]Messages in this appendix identified with an asterisk (*) are not suppressed when program option bit 10 is set. The prefix E indicates the message is an error message. An H prefix signifies a general information message.

Message Number	Memory Data	Program Segment	Comment
E17	-----	STEST	Preset did not set card reader flag. POPIO malfunction.
E20	-----	STEST	Preset did not clear card reader control. CPU malfunction.
E21	-----	STEST	No EOP (bit 15) status.
H22	102022	STEST	Turn READER POWER off. Press RUN. (This is a not ready status test).
E23	-----	STEST	Card reader in OFF LINE mode or busy or not ready; possible off line logic malfunction.
E24	-----	STEST	Ready status indicated. Ready logic malfunction.
H25	102025	STEST	Turn READER POWER on. (Note that the EOF indicator lamp is off.) Press RUN.
E26	-----	STEST	Card reader in OFF LINE mode or off line logic malfunction.
E27	-----	STEST	Ready status indicated.
E30	-----	STEST	STC does not set pick pending status. Check pick logic.
H31	102031	STEST	Set ON LINE/OFF LINE switch to OFF LINE. Press RUN.
E32	-----	STEST	OFF LINE mode status indicated.
E33	-----	STEST	OFF LINE mode does not clear pick pending status.
E34	-----	STEST	EOP is not set when card reader is set to OFF LINE mode with pick pending. Check logic associated with 32A pin 3.
H35	102035	STEST	Set reader to ON LINE mode. Place one card in input hopper. Start reader (press). Observe that status indicators are off and that the reader motor starts. Press RUN.
E36	-----	STEST	Status should be correct. Erroneous status conditions should be corrected before continuing.
H37*	-----	STEST	Extend stacker arm to limit and observe HOPPER/ STACKER indicator on reader. If card reader does not stop, press STOP on card reader. Card reader must be not ready before the program continues.
E40	-----	STEST	No stacker full status. Check bit 6 logic.

Message Number	Memory Data	Program Segment	Comment
H41	102041	STEST	Card reader must be not ready to begin next test.
E42	-----	STEST	CLC card reader does not clear pick status.
H43	102043	STEST	Start card reader. Press RUN.
E44	-----	STEST	Card reader not ready. The card reader must be ready to start next test.
E46	-----	STEST	No hopper empty status. Check bit 5 logic.
H47	102047	STEST	Press EOF switch on card reader. Note that the EOF indicator lamp turns on. Press the EOF switch again and note that EOF indicator lamp turns off. Press the EOF switch again and press RUN.
E50	-----	STEST	No EOF and hopper empty status. Check EOF and bit 7 logic.
E52	-----	STEST	PRESET does not clear EOF. Check control reset logic.
H53	102053	STEST	Place short card in reader and start reader. Set ON LINE switch. Press RUN.
E54	-----	STEST	No error (LIGHT/DARK) or trouble status. Check error (LIGHT/DARK) logic.
E55	-----	STEST	No error status (LIGHT/DARK). Check bit 9 logic.
E56	-----	STEST	No trouble status with error (LIGHT/DARK) status. Check bit 1 logic.
H57	102057	STEST	Place a deck consisting of two normal cards, a notched card, and a double card (in that order) in the reader. Start card reader. Press RUN.
H60	102060	STEST	Observe that MOTION CHECK indicator light is on. Start card reader. Press RUN.
E61	-----	STEST	No MOTION CHECK/PICK CHECK or trouble status. Check card motion logic.
E62	-----	STEST	No MOTION CHECK/PICK CHECK status. Check bit 11 logic.
E63	-----	STEST	No trouble status with MOTION CHECK/PICK CHECK status. Check bit 1 logic.
H64	102064	STEST	Observe that READ CHECK indicator light is on. Start card reader. Press RUN.

Message Number	Memory Data	Program Segment	Comment
E65	-----	STEST	No error (LIGHT/DARK) status. Check error (LIGHT/DARK) logic.
E66	-----	STEST	No error (LIGHT/DARK) status. Check bit 10 logic.
E67	-----	STEST	No trouble status with error (LIGHT/DARK) status. Check bit 1 logic.
E70	-----	STEST	No EOP after 875.0 milliseconds with pick failure. Check interface pick failure timer and EOP logic.
H71	102071	STEST	Observe that PICK CHECK indicator light is on. Remove double card, press RUN.
E72	-----	STEST	No pick failure or trouble status. Check pick failure logic.
E73	-----	STEST	No MOTION CHECK/PICK CHECK (pick fail = card motion = track jam) status with trouble status. Check bit 11 logic.
E74	-----	STEST	No trouble status with MOTION CHECK/PICK CHECK status. Check bit 1 logic.
E75	-----	STEST	Interface pick failure timer period is less than 675.0 milliseconds.
E76	-----	STEST	Interface pick failure timer period is greater than 875.0 milliseconds.
E77	-----	STEST	Setting EOP does not clear pick pending status.
E100	-----	STEST	Indications are that no pick failure occurred.
H101	-----	STEST	Status indicators test completed.
E103	-----	FTEST	Card reader in OFF LINE mode or off line status malfunction.
H104	102004	FTEST	Ready status indicated. Card reader ready or off line status malfunction. Correct condition. Press RUN.
E105	-----	FTEST	No pick pending status indicated after an STC card reader.
E106	-----	FTEST	EOP not clear after an STC card reader.
E107	-----	FTEST	Pick status not clear after a CLC 0. Check CRS and pick FF logic.
E110	-----	FTEST	Pick status not clear after a CLC card reader.

Message Number	Memory Data	Program Segment	Comment
E111	-----	FTEST	No EOP status after a CLC 0.
H112	102012	FTEST	Load cards and start card reader. Press RUN.
H113	102013	FTEST	Not ready status indicated. Card reader must be ready to start next test.
E115	-----	FTEST	Flag not set when EOP set.
E116	-----	FTEST	EOP interrupt occurred more than 100 milliseconds after pick command.
E117	-----	FTEST	READ-IN-PROCESS set when card reader is not ready.
E120	-----	FTEST	LIA clears flag with DATA-IN-REGISTER set. Check logic associated with 33A pin 12.
E121	-----	FTEST	Time from eightieth data interrupt to EOP interrupt was less than 3.0 milliseconds.
E122	-----	FTEST	Time from eightieth data interrupt to EOP interrupt was greater than 4.0 milliseconds.
E123	-----	FTEST	No EOP after 500.0 milliseconds when reading with DMA.
E124	-----	FTEST	STC sets pick status when READ-IN-PROCESS is set.
E125	-----	FTEST	Data flag not serviced by DMA. EOP clear when interrupt occurs when reading with DMA.
H126	-----	STDT	Standard data tests completed.
H127	-----	SPDT	Special data tests completed.
E130	-----	STDT, SPDT FTEST, FCT	Eighty data interrupts were not detected before the EOP interrupt.
E131	-----	STDT, SPDT FTEST, FCT	DMA did not service 80 data flags before the EOP interrupt.
E132	-----	STDT, SPDT	Data flag not serviced by DMA. EOP not set when interrupt occurs when reading with DMA.
E133	-----	STDT, SPDT	Column data not as expected. Prints column number, expected data, and actual data.
H134	-----	TPR	Timed pick rate segment completed.
H135	-----	FCT	Flag count segment completed.

Message Number	Memory Data	Program Segment	Comment
H136*	-----	LIST	List mode request; respond with A for ASCII or B for binary list.
H137*	-----	RRT	Read rate in cards per minute is output.
E140	-----	STEST	STC CR sets pick status when card reader is in OFF LINE mode.
H141*	-----	FCT	The number of cards read and the number of cards with erroneous flag count are printed.
H142*	-----	TPR	Type in the pick rate in cards per minute. Pick rates from 1 to 600 cards per minute are allowed.
E143	-----	ALL	No EOP or EOP interrupt within 900.0 milliseconds after a pick command.
E144	-----	ALL	No EOP interrupt within 900.0 milliseconds after a pick command and an EOP status true.
H145	102045	ALL	Card reader not ready or in OFF LINE mode. Correct condition. Press RUN.
H146	102046	ALL	Pick failure. Correct condition. Press RUN.
H147*	-----	LIST	List type request. Respond with ST to list standard test card image, SP to list special test card image, or RL to read and list cards.
H150	102050	STDT	Load standard data test deck. Start card reader and press RUN.
H151	-----	RRT	Read rate test completed.
H152	102052	SPDT	Load special data test deck. Start card reader and press RUN.
E153	-----	FTEST	No READ-IN-PROGRESS not status. Check bit 12 logic.
E154	-----	FTEST	No EOP within 900.0 milliseconds after pick command.
E155	-----	FTEST	No READ-IN-PROGRESS not status after EOP interrupt. Check that setting EOP clears pick FF.
E156	-----	FTEST	READ-IN-PROGRESS not status true after pick command.
E157	-----	FTEST	Status bit 12 clear after a CLC 0. Check to ensure if CRS clear READ-IN-PROGRESS FF.

Message Number	Memory Data	Program Segment	Comment
E160	-----	FTEST	Second interrupt occurs when flag is left set. Confirm that flag delays further setting of flag buffer.
E161	-----	FTEST	Pick FF not clear after first data interrupt. Confirm that index mark clears pick FF.
E162	-----	FTEST	Flag not cleared by LIA after a data interrupt. Check logic associated with 15B pin 10.
E163	-----	FTEST	Flag cleared by LIA after data flag has been serviced. Confirm that DATA-IN-REGISTER is cleared by LIA.
E164	-----	FTEST	No lost data error when a data flag is not serviced by an LIA. Check that DIR and DS set lost data FF.
E165	-----	FTEST	CLC 0 did not clear lost data status. Check logic associated with 32B pin 6.
E166	-----	FTEST	Eighty data interrupts were not detected before the EOP interrupt.
E167	-----	FTEST	No lost data error. EOP and DATA-IN-REGISTER did not set lost data status.
E170	-----	FTEST	STC does not clear timing lost data status. Check logic associated with 53D pin 9.
E171	-----	FTEST	No lost data error when an OTA is given and DATA-IN-REGISTER set. Check logic associated with 23A pin 2.
E172	-----	FTEST	No lost data error with index mark and status mode. Check logic associated with U11 pin 12.
E173	-----	STDT, SPDT, FTEST, FCT	Lost data error when reading with DMA.
E174	-----	STEST	EOP not clear after STC CR.
ALL E's	102075	ALL	This halt occurs after each error message is printed unless switch 14 is set.
H176	102076	-----	Switch 15 set. Halt at end of test. Number of last test is printed.
H177	102077	END	Diagnostic completed. Program can be restarted (skipping INIL segment) by pressing RUN.
H200	-----	FTEST	Functional tests completed.
E201	-----	STDT, SPDT, FTEST, FCT	Lost data error when reading under interrupt control.

Message Number	Memory Data	Program Segment	Comment
-----	1060*xx*	-----	Trap-cell interrupt on select code *xx*.
-----	107000	CFIG	Configuration segment cannot be restarted. Reload program to reconfigure.
-----	107001	CFIG	Load card with special data format. Start reader and press RUN.
-----	107077	CFIG	Configuration complete. Start program by pressing RUN.

HP 2100A TAPE READER TEST

Order No. HP 24189

HEWLETT PACKARD

11000 Wolfe Road
Cupertino, California 95015

Manual of Diagnostics
HP 5951-1363

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HP 2100A TAPE READER TEST

The Tape Reader Test program confirms proper operation of a punched tape reader (HP 2748 or HP 2758) and interface kit (HP 12597A-002) with an HP 2100A computer. If any operational errors are found, the program may be used to isolate the problem.

HARDWARE REQUIREMENTS

This diagnostic program is used in the 2100A computer. A teleprinter must be used to report errors and messages to the user and to punch test tapes.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

The SIO teleprinter driver is loaded and configured first. The diagnostic program is loaded, configured, then started. It first performs a Functional Test in which the basic functions of the tape reader are checked:

- Initialization of the interface board by the computer EXTERNAL PRESET button.
- Proper command responses by the interface board and the computer I/O control circuits.
- Operation of the interrupt control circuits.

After the Functional Test is complete, the program halts to allow switch register settings to select program options (see Table TRT-2) for the start of the Operational Test. First, a standard test data tape is punched on the teleprinter, then read to test the tape reader and the interface board for data transfer. If any errors are found, the Operational Test may be used to punch then read a special test data tape to isolate any transfer problem. If a trap cell halt occurs, the computer halts with 1020*xx* (*xx* = trap cell location) in MEMORY DATA Register. The cause is determined by the user; after the error is corrected, the diagnostic is restarted.

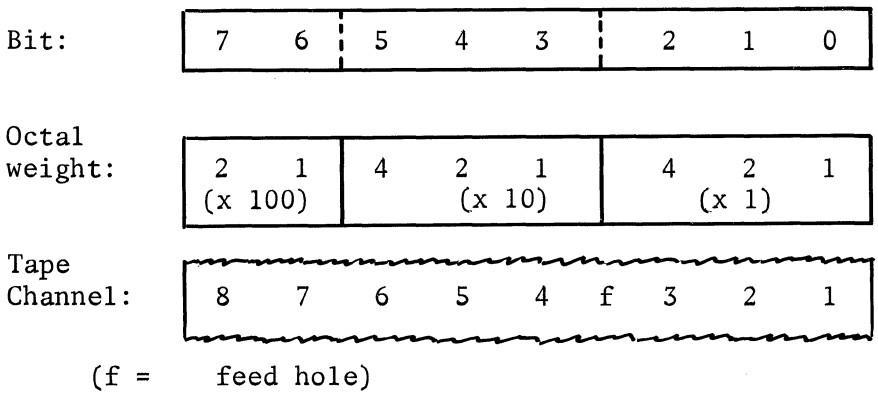
TEST DATA TAPES

The contents of the standard test data tape are defined in the diagnostic program. Those contents are three identical 55 character data records (separated by at least 15 blank feed-frames) that present the most difficult data patterns for both continuous and start-stop reading of tapes. The 55 character data records are described below and in Table TRT-1.

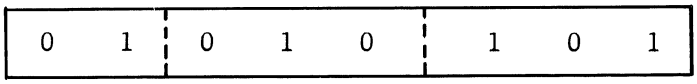
The contents of the special test data tape are determined by the user, according to errors reported when the diagnostic program reads the standard test data tape. This tape contains one character punched repetitively until a desired length of tape is reached. Several special test data tapes (each for a different character) may be punched then read to check reader operation.

Standard Test Data Records

Each of the three 55 character data records in the standard test data tape contains bits 7 through 0 of 55 words punched into tape channels (punch levels) as follows:

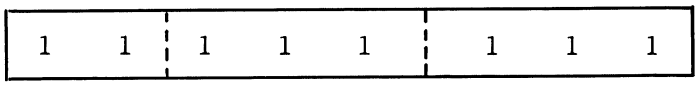


Thus, the octal value 125_8 is set into bits 7 through 0 as:

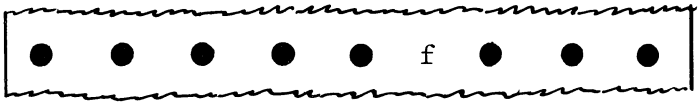


and punched as a tape character:

Or, the octal value 377_8 is set into bits 7 through 0 as:



and punched as a tape character:



Each of the 55 characters in the three standard test data records is identified either as a "single character" (SC) or a "character" (FC = first character, *xx* = character number, LC = last character) within one of four "test blocks" (TB*x* = test block number *x*). (See Table TRT-1.)

Standard Test Data Additional Tests

When the standard test data tape is read, the tests listed below are made if program option bit 1 (in the switch register) is set off. The tests are bypassed by setting program option bit 1 on. (When the special test data tape is read, these tests should be bypassed; they are not useful then.)

1. Between the following characters (see Table TRT-1) the program stops then restarts the reader:

1 and 2	12 and 13	40 and 41
2 and 3	13 and 14	45 and 46
3 and 4	33 and 34	46 and 47
4 and 5	34 and 35	49 and 50
		52 and 53

These tests check the reader's control circuits.

2. Between the following characters the program inserts one of four delay times:

47 and 48	51 and 52
48 and 49	53 and 54
50 and 51	54 and 55

The four delay times are:

1. During the first, fifth, ninth, etc. reading of a 55 character record, 0.5 milliseconds.
2. During the second, sixth, tenth, etc. reading, 0.75 milliseconds.
3. During the third, seventh, eleventh, etc. reading 1.00 milliseconds.
4. During the fourth, eighth, twelfth, etc, reading, 1.25 milliseconds.

The delay is between the flag signal and the drive signal, to check the reader's response time.

Special Test Data

The special test data, determined by the user, consists only of continuous repetition of any character on the punched tape. The same assignments of octal digits to tape channels are used. The user specifies any character in switch register bits 15 through 8 when he selects the program options to punch then read the special data test tape. (See Table TRT-2.)

Error Reports

If an error is detected during the Functional Test, the program prints a message on the teleprinter then continues. After all functional checks have been made, the Functional Test prints its completion message. All Functional Test messages and their meanings are listed in Table TRT-3.

If an error is detected during the Operational Test while reading the standard test data tape, the program prints a two-line message:

G *vvvvvvvv*
B *vvvvvvvv ww xx yyyy zzzzzzzzzz*

Where:

G *vvvvvvvv* = the correct character that should have been transmitted,

B *vvvvvvvv* = the incorrect character transmitted by the reader,

ww = the character number (see Table TRT-1) within the field of 55 characters,

xx = the identity of the character (see Table TRT-1);

FC = first character of a test block,

Ø3 = (for example) character #3 of a test block,

LC = last character of a test block,

SC = a single character (not part of a test block),

yyyy = the flag-to-drive delay time in milliseconds (see Standard Test Data Additional Tests),

NOTE: This field is not printed if there is no delay.

zzzzzzzzzz = the type of error:

BIT ERROR = one or more bits have been missed, but the sequence of reading is correct.

NOTE: After three "BIT ERROR" messages are printed followed by a "RESYNC" message, the program skips the tape through the next field of blank feed-frames to start reading a new record.

REREAD CH = the character transmitted is identical to the last one transmitted. This causes the program to print "RESYNC" then skip through the next field of blank feed-frames to start reading a new record.

MISSED CH = the character just read is out of proper sequence. This causes the program to print "RESYNC" then skip through the next field of blank feed-frames to start reading a new record.

If an error is detected while reading a special test data tape, the program prints a short two-line message:

G *vvvvvvvv*
B *vvvvvvvv*

Where:

G *vvvvvvvv* = the correct character that should have been transmitted,
B *vvvvvvvv* the incorrect character transmitted by the reader.

OPERATING INSTRUCTIONS

a. If the tape reader to be tested is in good operating condition and this program is only to confirm that condition, skip to step c and use that reader to load the program. Otherwise, the teleprinter tape reader mechanism should be used to load the program, beginning with step b.

b. Check the type of loader program by displaying the contents of location $0x7701_8$ (x = 0 for a 4K memory, 1 for an 8K memory, 3 for 16K, etc). If the contents are 063770_8, the Basic Binary Loader (BBL) is in core; if the contents are 002401_8, the Basic Binary Disc Loader (BBDL) is in core. Accordingly, in one of the following sets of locations change bits 5 - 0

(but no other bits) to the select code of the teleprinter rather than the punched tape reader):

BBL		BBDL	
Location	Content	Location	Content
0*x*7763	1067*cc*	0*x*7744	1037*cc*
0*x*7764	1023*cc*	0*x*7745	1023*cc*
0*x*7766	1025*cc*	0*x*7747	1074*cc*

(cc = select code of teleprinter or punched tape reader.*)*

c. Place the SIO teleprinter driver tape in the tape reader device to be used (see steps a and b) and ready that reader.

d. Use the Basic Binary Loader or the Basic Binary Disc Loader to load the driver, then configure that driver.

e. Place the HP 2100A Tape Reader Test tape in the tape reader device to be used (see steps a and b) and ready that reader.

f. Load the tape using the Basic Binary Loader or Basic Binary Disc Loader.

g. Set the starting address 2_8.

h. Set the tape reader select code (I/O address) in bits 5-0 of the switch register.

i. Press RUN. The diagnostic halts with 102000_8 in MEMORY DATA when the configuration is complete. Use the SIO System Dump program to punch copies of the configured driver and test, if wanted.

j. Load any binary punched tape in the reader, press EXTERNAL PRESET, then RUN to execute the functional test section. Upon completion, the program types out "FUNCTIONAL TEST COMPLETE" and halts with 102001_8 in MEMORY DATA.

From this point on, the Operational Test executes according to program options selected by the user through switch register settings listed in Table TRT-2.

k. If a standard test data tape has not yet been punched, set switch register (program option) bit 0 only on then perform steps 1 through p. Otherwise, skip to step q.

l. Perform the following steps to punch a length of blank (feed-frames only) tape on the teleprinter:

   1. Turn off the tape punch unit (on an HP 2752, press the OFF button; on an HP 2754, set the MODE switch to K).
   2. Set the teleprinter to LOCAL.
   3. Turn on the tape punch unit (on an HP 2752, press the ON button; on an HP 2754, set the MODE switch to T).
   4. Punch at least three inches of blank tape. (On an HP 2752, press the HERE IS key as many times as needed; on an HP 2754, press and hold four keys in this order: SHIFT, CTRL, @, and REPT as long as needed.)
   5. Turn off the tape punch unit (as in step 1-1).
   6. Set the teleprinter to LINE.

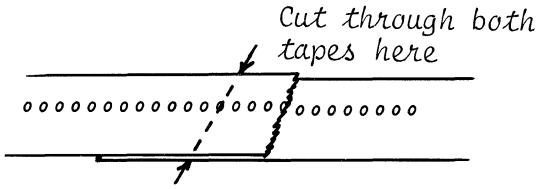
m. Turn on the teleprinter tape punch unit (as in step 1-3).

n. Press RUN. The program punches the standard test data tape then halts.

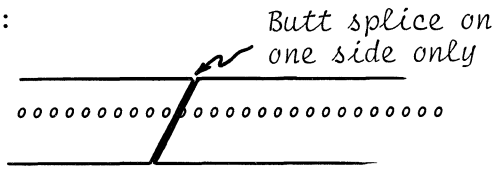
o. Perform step l again, to punch a length of trailer tape, then proceed to step p.

p. Form the standard test data tape into a loop:

   1. Overlap the ends of the tape by at least five blank feed-frames, carefully to align the holes, then cut through the overlap diagonally:



   2. Butt splice the diagonal cut ends with clear mending tape on one side only:



q. Place the looped standard test data tape into the tape reader to be tested then ready that reader. Be sure the tape is properly positioned (the feed holes are nearest the reader panel and the printed arrow points from left-to-right).

r. Set all switch register bits off.

s. Press RUN. The program reads the standard test data tape continuously with stop-start and flag-to-drive delay tests.

t. After allowing the tape loop to be read at least twice, set switch register bit 1 on to switch the program to the "No-stop Read" mode. Tape reading continues but without the stop-start and delay tests.

u. When wanted, terminate the standard test data tape reading by setting switch register bit 4 on. The program prints "-TERMINATE-" on the teleprinter then halts.

If no errors were reported during steps t and u, the tape reader has been throughly tested and the program may be considered complete.

If errors were reported, one or more special test data tapes may now be prepared then read to test any particular character.
Proceed to step v.

v. To punch a special test data tape, set all switch register bits off then set bits 0 and 2 on and set bits 15 through 8 for the desired character (see Table TRT-2).

w. Perform step 1, then proceed to step x.

x. Press RUN. The program types "TAPE LENGTH?". Type in the desired loop length number (between 10 and 99 inches) followed by pressing the return and linefeed buttons. The program types "TURN ON TTY PUNCH. PRESS RUN" and halts with 102002_8 in MEMORY DATA.

y. Press RUN. The computer punches the desired length of the tape plus leader and trailer and then halts. Turn off tape punch (HP 2752) or set MODE switch to K (HP 2754).

z. Form the special test data tape into a loop:

1. The special test data tape must not have any blank feed-frames, so overlap the ends of the tape by at least five data frames. Carefully align the punched holes, then cut through the overlap diagonally, as shown in step p-1.
2. Butt splice the diagonal cut ends with clear mending tape on one side only, as shown in step p-2.

aa. Place the looped special test data tape into the tape reader to be tested then ready that reader. Be sure the tape is properly positioned (the feed holes are nearest the reader panel and the printed arrow points from left-to-right).

bb. Set switch register bits 1 and 2 on. (Switch 0 off.)

cc. Press RUN. The program reads the special test data tape continuously until terminated by setting switch register bit 4 on.

NOTE: Errors may be reported when the area of tape where the splice is located is read. This cannot be avoided, either because the splicing tape picks up dust or the splice may not quite exactly align the holes. Ignore such error reports. If many error messages are being printed, avoid all error messages by setting program bit 6 on. This will enable an oscilloscope to be used to monitor the tape reader and interface board circuits.

dd. When wanted, terminate the special test data tape reading by setting switch register bit 4 on. The program prints "-TERMINATE-" on the teleprinter then halts.

Now the program may be directed to read the standard test data tape again or to punch then read another special test data tape.

ee. To read the standard test data tape again, perform steps q through u.

ff. To punch then read another special test data tape, perform steps v through dd.

Additional Operating Instructions

a. During reading of the standard test data tape, if errors are being reported, switch register bit 5 may be set on. The program pauses in a waiting loop after the next RESYNC message is printed. This pause allows any changes to be made (such as placing another standard test data tape into the reader), after which the program may be resumed by setting that bit 5 off.

b. If a pause is needed when reading a special test data tape, switch register bit 3 may be set on. The program enters a waiting loop; the program can be resumed by setting that bit off.

c. The program can be set to perform an additional test of interrupt control during reading of either the standard or special test data tape. Set switch register bit 7 on, then start the reading.

   If the interface board fails this interrupt control test, the program loops with 177777_8 in the B-Register.

Table TRT-1

Standard Test Data Records Contents

Character Number	Identity	Octal value	Character Number	Identity	Octal value
1	SC	377	29	16 (TB2)	102
2	SC	201	30	17 "	044
3	SC	125	31	18 "	030
4	SC	252	32	LC "	231
5	FC (TB1)	333	33	SC	044
6	Ø2 "	155	34	SC	102
7	Ø3 "	066	35	FC (TB3)	201
8	Ø4 "	033	36	Ø2 "	377
9	Ø5 "	204	37	Ø3 "	252
1Ø	Ø6 "	037	38	Ø4 "	125
11	Ø7 "	340	39	Ø5 "	250
12	LC "	377	40	LC "	377
13	SC	127	41	FC (TB4)	000
14	FC (TB2)	201	42	Ø2 "	347
15	Ø2 "	102	43	Ø3 "	122
16	Ø3 "	145	44	Ø4 "	255
17	Ø4 "	132	45	LC "	211
18	Ø5 "	347	46	SC	152
19	Ø6 "	030	47	SC	235
20	Ø7 "	377	48	SC	052
21	Ø8 "	132	49	SC	367
22	Ø9 "	245	50	SC	010
23	1Ø "	030	51	SC	167
24	11 "	102	52	SC	030
25	12 "	044	53	SC	245
26	13 "	030	54	SC	044
27	14 "	201	55	SC	333
28	15 "	245			

NOTE: Each 55 character record is separated from another by at least 15 blank feed-frames.

Table TRT-2

Program Options -- SWITCH REGISTER Settings

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit	Function
0	PUNCH OR READ. Set on to punch, set off to read.
1	READ MODE. Set off to read with stop-start and delay tests, set on to read in the No-stop mode. Can be changed during the run.
2	TEST DATA. Set off to use standard data, set on to use special data as set into bits 15 through 8.
3	PAUSE.* Set off when the Operational Test is started. Can be set on while reading to pause the program momentarily. Set off to resume the program.
4	TERMINATE*. Set off when the Operational Test is started. To terminate the test, set this bit on. See "Operating Instructions" for full details.
5	PAUSE AFTER NEXT RESYNC. Set off when the Operational Test is started. Can be set on while reading the standard test data tape, to pause the program after the next "RESYNC" message is printed.
6	BYPASS ERROR MESSAGES. Set off when the Operational Test is started. Can be set on at any time to bypass all error messages. See "Operating Instructions" for full details.
7	TEST INTERRUPT CONTROL. Set on to include the additional test of interrupt control, as described in "Additional Operating Instructions;" set off to bypass the additional test.
8 - 15	SPECIAL DATA CHARACTER. Set before starting to punch or read a special test data tape, to specify the character to be used. Each bit set on is punched, bits 15 through 8 correspond to punch levels 8 through 1, respectively.

**PAUSE and TERMINATE take effect immediately when performing special tape functions, but only after every fourth data record when reading the standard test data tape.*

Table TRT-3

DIAGNOSTIC MESSAGES - FUNCTIONAL TEST

Message	Comments
BIT ERROR	A character read is in error (one or more bits dropped, for example), but the sequence of reading is correct. Three consecutive BIT ERROR messages are typed out if two or more characters are skipped.
FUNCTIONAL TEST COMPLETE	The functional test of the interface card is completed.
INTERRUPT ON PRESET (CONTROL)	An interrupt occurred in the preliminary steps of the functional test on the interface card. If there were no error type-outs prior to this, the control FF on the interface card was not reset when the EXTERNAL PRESET switch was pressed at the beginning of the test.
INVALID INPUT	An integer between 10 and 99 was not typed in after the tape length request. The tape length message is repeated.
MISSED CH	The character just read is out of place so it is assumed that at least one character was skipped. This is generally caused by feedhole phototransistor sensitivity or improper setting of pinch roller tension. Following this type-out, a RESYNC message is typed, the program automatically positions the test tape to the next group of leader characters, and the testing is restarted.

Table TRT-3 (cont.)

Message	Comments
NO NORMAL INTERRUPT	An interrupt signal was not received from the interface card within 30 milliseconds after the drive signal was sent to the tape reader. If there were no error type-outs prior to this, the circuits in the tape reader which supply the flag signal to the interface card or the interrupt logic on the interface card are suspected.
READER CLF ERROR (CLF OR SFC)	The flag FF on the interface card did not respond to a clear flag (CLF) instruction, or the skip on flag clear (SFC) instruction used in testing the flag FF did not function properly on the interface card.
READER FLAG OFF - PRESET	The flag FF (reader flag) on the interface card did not set when the EXTERNAL PRESET switch was pressed.
READER STF ERROR (STF OR SFS)	The flag FF on the interface card did not respond to a set flag (STF) instruction, or the skip on flag set (SFS) instruction used in testing the flag FF did not function properly on the interface card.
REREAD CH	The character read is identical to the last character read, so it is assumed to be a reread of that character. This is generally caused by tape reader noise. Following this type-out, a RESYNC message is typed, the program automatically positions the test tape to the next group of leader characters, and the testing is restarted.

Table TRT-3 (cont.)

Message	Comments
RESYNC	Character sequence errors or three consecutive bit errors have been detected. The program automatically positions the test tape to the next group of leader characters, and the testing is restarted.
TAPE LENGTH?	When punching the special test tape, the program requests the length desired. The length must be in integer inches between 10 and 99.
-TERMINATE-	Switch 4 of the computer switch register is placed in the on position and the test is terminated. The test can be continued if the computer RUN switch is pressed.
TURN ON TTY PUNCH. PRESS RUN.	Occurs before the punching of the special test tape on the Teleprinter Punch. The computer halts with 102002 in MEMORY DATA.

HP 2100 TTY TEST

HP Product No. 24201

11000 Wolfe Road
Cupertino, California 95014

Manual of Diagnostics
Diagnostic Program Procedure
HP 5951-1365

July 1971

HP 2100 TTY TEST

This diagnostic program confirms proper operation of Buffered Teleprinter Interface Cards in Interface Kits, as listed below:

Interface Card	Interface Kit
HP 02116-6168	HP 12531B
HP 12531-6001	HP 12531B
HP 12531-60022	HP 12531C

NOTE: This program does not test the HP 12531A Serial Teleprinter Interface Kit nor its HP 02116-6007 Interface Card.

HARDWARE CONFIGURATION

This program is used in any HP 2100 computer. No peripheral device other than the teleprinter is required, and no driver program is required.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

Before using the program, the user must check that the interface card to be tested is installed in an unbroken priority string. That is, each I/O slot of higher-priority has either another interface card or a priority jumper card installed. This is necessary because the program tests the interface card for receipt of priority.

Only the diagnostic program need be loaded for testing. No driver program is required. After the program is loaded, it is configured to the select code of the interface card to be tested. Then the tests are run as described in the following paragraphs. After the tests are complete, the program may be configured again, without reloading, to the select code of another teleprinter interface card, if more than one is installed in the computer.

To start a run of the program, the user sets the starting address, clears the switch register, presses INTERNAL and EXTERNAL PRESET, then presses RUN. The program begins by entering a loop in which it waits for the user to set the switch register to select a program option, as listed in Table TTY-1.

The Basic Test routine must be used first, to determine the ability of the interface card and the teleprinter to print error reports. After the errors, if any, found by that routine have been corrected, the Punch And Read routine may be used. Any errors found by the Punch And Read routine will be printed on the teleprinter. Or, the Print And Keyboard routine may be used next, to test communications to and from the user.

Each of the routines repeats continuously (unless an error is found) until the user clears the switch register. Then the program returns to the loop to await selection of another program option.

If a trap cell halt occurs, an unexpected interrupt from another device has occurred. The computer halts with $1060xx_8$ displayed. (xx = the select code of the device that interrupted.) The cause of the trap cell halt must be determined by the user before the program is restarted.

PROGRAM LIMITATIONS

The Direct Memory Access (DMA) portion of the interface card is not tested by this program.

Four types of priority string errors can exist on the interface card:

1. Does the card receive priority? Tested by this program.
2. Can the card be denied priority? To make this test, extract an unused higher-priority card then run this test program. An EØ7 error should occur. (See Table TTY-2.)
3. Does the card deliver priority? Test this only by running a test program for a lower priority interface card to some other device.

4. Can the card deny priority? Not tested by this program.

The preset portion of the interface card is not tested by this program.

PROGRAM ORGANIZATION

The HP 2100 TTY Test program consists of the following routines:

INITIALIZE — Inserts the select code of the buffered teleprinter interface card into all I/O instructions in the program. This routine also sets a trap cell halt instruction into all unused select code memory locations.

BASIC TEST — Performs 15 (17_8) tests of the flag, control, and interrupt circuits and, for any error found, stores a number corresponding to the test made in an error buffer. At the end of the tests, the routine attempts to print a report of the error numbers on the teleprinter. If the interface card is unable to operate properly, or if the program option (bit 1) to halt at the beginning of the error buffer is selected, the routine halts with 102055_8 displayed. The user then examines the 15 (17_8) locations of the error buffer plus the 16th location for the address at which error E17 occurred. The 17th error buffer location contains 177777_8 to signal the end of the error buffer. Table TTY-2 lists the error messages, the error buffer contents, and their meanings.

PUNCH AND READ — Tests the teleprinter's tape punch and tape reader mechanisms. Because the teleprinter may be used to punch tapes in binary or octal codes as well as ASCII codes, the routine begins by punching all combinations of the eight bits that are data output to the teleprinter. After a leader, the eight-bit combinations, and a trailer have been punched, the routine is used to read the tape back to see that the tape inputs match the outputs. Differences are reported as they are found.

PRINT AND KEYBOARD — Tests the printer and keyboard mechanisms of the teleprinter. All 64 ASCII characters of the keyboard are printed twice, then the routine requests the operator to type any of those characters on the keyboard at a slow rate. Each character typed by the user is "read" by the routine then printed back to the user for visual checking.

ERROR ANALYSIS

As previously described, all errors detected by the Basic Test routine are analyzed by referring to Table TTY-2. Any errors found by the Punch And Read routine are reported by a message "OUTPUT = *xxxxxxxx* INPUT = *yyyyyyyy*" (where *xxxxxxxx* is the eight-bit combination output to the punch, and *yyyyyyyy* is the eight-bit combination input from the punched tape). Any errors that occur in the Print And Keyboard routine must be detected by the user as the keyboard is used.

OPERATING INSTRUCTIONS

1. Confirm that the teleprinter interface card(s) to be tested are installed in an unbroken priority string and that the teleprinter is properly connected. If any changes need to be made, be sure to turn off computer power.
2. Turn on the teleprinter: On an HP 2752, set the LINE-OFF-LOCAL switch to LINE and press the tape punch mechanism's OFF button. On an HP 2754, set the ON LINE-OFF-LOCAL switch to ON LINE and set the MODE switch to KT.
3. Use the Basic Binary Loader to load the HP 2100 TTY Test program.
4. Set the starting address 100_8.
5. Set the switch register to the teleprinter select code.
6. Press INTERNAL and EXTERNAL PRESET then press RUN. The program runs briefly, the teleprinter cycles briefly, then the program halts with MEMORY DATA 102001_8 in the DISPLAY REGISTER.

7. Clear the switch register (press S then press CLEAR DISPLAY).

8. Press RUN.

9. The program is now running in a loop, waiting for selection of a program option. (See Table TTY-1.) While the program is running, the S button is lit to indicate that the switch register is controllable through the DISPLAY REGISTER.

10. Select the Basic Test routine by setting program option bit 3 on.

    If the routine halts with 102055_8 in the DISPLAY REGISTER, an attempt to print a report of errors failed. Determine the error(s) by pressing INCREMENT M 17 times. The first 15 presses display, in the DISPLAY REGISTER, either the number of the test that found the error or 0 to signal that the test did not find an error. (See Table TTY-2.) The 16th press displays 0 if the 15th press displayed 0 or the address at which the illegal interrupt (E17) occurred. The 17th press displays 177777_8 which signals the end of the error buffer. Now press RUN.

11. To terminate the Basic Test routine, set program option bit 3 off.

12. Select the Punch And Read routine by setting program option bit 4 on. The routine prints a message then halts with MEMORY DATA 102002_8 in the DISPLAY REGISTER. If the teleprinter in use is an HP 2752, press its tape punch mechanism ON button; otherwise go directly to step 13.

    NOTE: Be sure the tape punch mechanism has at least 10 feet of blank tape in its supply.

13. Press RUN. The routine punches a tape; during punching it prints some characters. Those characters may be checked later against the characters that are printed when this tape is read back by the routine. (See step 17.)

14. When the routine halts with MEMORY DATA 102003_8 in the DISPLAY REGISTER, remove the tape from the tape punch mechanism and place it in the tape reader mechanism.

15. If the teleprinter in use is an HP 2752, press its tape punch mechanism OFF button; otherwise go directly to step 16.

16. Ready the tape reader mechanism then press the computer RUN button.

17. As the routine reads the tape, it prints reports of errors found and/or the same characters printed during the punch phase. Then it prints its end message; during that message set program option bit 4 off to terminate the routine.

18. Select the Print And Keyboard routine by setting program option bit 5 on. The routine prints a message then prints two sets of the 64 characters it allows the user to type. Then it prints the request "USE KEYBOARD SLOWLY (5 CHS./SEC.)"

19. Type any of the characters printed by the routine in any combination, but do not type as fast as normal. The routine receives each character then prints the character. Continue this step as long as desired, and check that each character printed is the one typed.

20. To terminate the Print And Keyboard routine, set program option bit 5 off.

21. To terminate the program, clear the switch register then set bit 0 on. The program halts at the starting address with MEMORY DATA 102000_8 in the DISPLAY REGISTER. Now the program may be used again for another teleprinter; return to step 5.

Table TTY-1

Program Options--Switch Register Settings

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit	Function
0	Set on to terminate the program and halt at the starting address.
1	Set on to halt at the beginning of the error buffer without attempting to print the error report(s). This halt occurs whether or not errors were found.
2	Set on to suppress program information messages.
3	Set on to use the Basic Test routine.
4	Set on to use the Punch and Read routine.
5	Set on to use the Print And Keyboard routine.
6-15	Spares.

Table TTY-2

Error Messages and Error Buffer Contents

Message*	Error Buffer Content (octal)	Test Failure Indicated
EØ1	1	SFC *xx* true after CLC Ø,C
EØ2	2	SFS *xx* false after CLC Ø,C
EØ3	3	SFC *xx* false after CLF *xx*
EØ4	4	SFS *xx* true after CLF *xx*
EØ5	5	SFC *xx* false after CLF *xx* and STC *xx*
EØ6	6	SFS *xx* true after CLF *xx* and STC *xx*
EØ7	7	No interrupt after STC *xx*, STF *xx*, STF Ø
E1Ø	10	SFC *xx* true after interrupt
E11	11	SFS *xx* false after interrupt
E12	12	Data clock on TTY card too fast
E13	13	Data clock on TTY card too slow
E14	14	Data buffer error
E15	15	Clock Enable flip-flop set
E16	16	Clock Enable flip-flop not set
E17	17	Illegal interrupt from TTY
PROGRAM ADDRESS = *aaaaaa*	*aaaaaa*	Follows error E17 report, *aaaaaa* = program address where the illegal interrupt occurred.

NOTE: xx = select code of the teleprinter card being tested.

*Printed only if program option bit 1 is off or the attempt to print messages succeeds.

HP 2100A TIME BASE GENERATOR TEST

HP Product No. HP 24213

HEWLETT hp PACKARD

11000 Wolfe Road
Cupertino, California 95014

Manual of Diagnostics
Diagnostic Program Procedure
HP 12539-90005

October 1971

HP 2100A TIME BASE GENERATOR TEST

This diagnostic program confirms proper operation of the HP 12539 Time Base Generator (TBG) interface cards.

HARDWARE CONFIGURATION

The diagnostic program requires a 2100A computer with at least 2K of core (or 4K if a teleprinter is included), a HP 12539 Time Base Generator interface card, and optionally a teleprinter.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

This program is controlled by program options set into an *internal switch register* at configuration time, or by overriding that internal switch register during a run of the program. During any program run, the computer's S button is lit to indicate that the DISPLAY REGISTER is functioning as a switch register. If the DISPLAY REGISTER bit 0 is on, the *internal switch register* is overridden and the other bits are interpreted for program options, as listed in Table GEN-1.

This diagnostic performs the following tests:

Tests 1 through 4

Check the ability to clear, set, and test the interrupt system:

Test 1 checks the CLF Ø, SFC Ø combination.
Test 2 checks the CLF Ø, SFS Ø combination.
Test 3 checks the STF Ø, SFC Ø combination.
Test 4 checks the STF Ø, SFS Ø combination.

Test 5

Checks the absence of an interrupt when the TBG flag flip-flop is set, the TBG control flip-flop set, and the interrupt system is off. A failure here results in an irrecoverable halt 102005_8.

Test 6 through 11

Check the ability to clear, set, and test the TBG flag:

Test 6 checks the CLF TBG, SFC TBG combination.
Test 7 checks the CLF TBG, SFS TBG combination.
Test 10 checks the STF TBG, SFC TBG combination.
Test 11 checks the STF TBG, SFS TBG combination.

Test 12

The select code screen test sets the flag of every select code (10 through 77) except the TBG select code and checks that the TBG flag is not set in the process.

Test 13

Checks the ability of the TBG to interrupt by setting the flag and control flip-flops and turning on the interrupt system. The interrupt in Test 13 should not occur before a string of instructions affecting priority are executed.

Test 14

Checks that the interrupt occurred where expected.

Test 15

Checks that the contents of the Central Interrupt Register is the TBG select code.

Test 16

Checks that another interrupt does not occur when the interrupt system is turned back on. A failure here results in an irrecoverable halt 102016_8.

Test 17

Checks that the TBG flag is still set following the interrupt.

Test 20

Checks that, with the TBG control and flag flip-flops set and the interrupt system on, there is no interrupt following a CLC TBG instruction. A CLC TBG instruction should reset the TBG control flip-flop.

Test 21

Indirectly checks that a CLC Ø instruction resets the TBG control flip-flop.

Test 25

Checks that EXTERNAL PRESET switch on the 2100A sets the TBG flag (POPIO signal line).

NOTE: Test 25 requires a response from the operator and has an initializing halt. It is bypassed if switch 2 is set.

Test 30

Checks that a STC TBG instruction resets the error flip-flop.

Test 31

This is the 1 ms relative timing test.

Test 32

Checks that the error flip-flop is still reset following the interrupt in Test 31.

Test 33

Checks that the TBG flag flip-flop is still set following the interrupt in Test 31.

Test 34

Checks that, with the TBG control and flag flip-flops left unchanged from Test 31, another interrupt does not occur when the interrupt system is turned back on. The set flag flip-flop should inhibit the resetting of the flag buffer flip-flop. This test waits a minimum of 1.2 ms for the unexpected interrupt.

TEST 35

Checks that the error flip-flop is not set.

NOTE: With the TBG control and flag flip-flops left on from Test 31, at least 1.2 ms have elapsed since the interrupt in Test 31.

Test 36

Checks that a STC TBG instruction now resets a set error flip-flop.

Test 37

Indirectly checks that the OTB TBG instruction resets the TBG control flip-flop. This should prevent an interrupt if the TBG flag, TBG control flip-flop, and the interrupt system were on.

Test 40

This is the 0.1 ms relative timing test and is bypassed if switch 4 is set.

Test 42

This is the 10 ms relative timing test.

Test 43

This is the 100 ms relative timing test.

Test 44

This is the 1 sec relative timing test.

Test 45

This is the 10 sec relative timing test and is run only if switch 8 is set and switch 4 is reset.

Test 46

This is the 100 sec relative timing test and is run only if switch 7 is set and switch 4 is reset.

Test 47

This is the 1000 sec relative timing test and is run only if switch 6 is set and switch 4 is reset.

Relative Timing Tests

The relative timing tests check that an interrupt occurs in the 2100A within 1% of the time obtained by counting while waiting for the interrupt. An interrupt is assumed not to occur if it does take place within an interval 20% greater than the expected interval. If an interrupt does occur, but the actual count is not within 1% of the expected count, the error indications give the actual and expected count. The expected counts, tolerances, and count representations are:

TEST	INTERVAL	EXPECTED COUNT	1% TOLERANCE IN COUNTS	EACH COUNT REPRESENTS
31	1 ms	255	5*	3.92 us
40	0.1 ms	25	1*	3.92 us
42	10 ms	2551	25	3.92 us
43	100 ms	25510	255	3.92 us
44	1 sec	1000	10	1 ms
45	10 sec	10000	100	1 ms
46	100 sec	10000	100	10 ms
47	1000 sec	10000	100	100 ms

**NOTE: The first pulse which the decade dividers sees could come anytime from 0 to 0.01 ms after the control flip-flop sets. This represents an error of 10% on the 0.1 ms interval and 1% on the 1 ms interval. Thus, the test tolerance for Test 31 is 2% or 5 counts and Test 40 is timed between 2 interrupts.*

LIMITATIONS

The program does not check the SRQ signal to the DMA or the priority lines PRH and PRL. PRH and PRL may be tested with the 2100A Interrupt Test, HP 24215.

MESSAGE ANALYSIS

Error and program messages are indicated by printed messages on the teleprinter and/or by coded computer halts. (See Table GEN-2.) All teleprinter message data is in octal except for the end-of-pass count and the actual and expected counts in the error messages for the relative timing tests.

Program messages occur only if switches 1 and 10 are reset and include an introductory message, a message to the operator before test 25, and an end of pass message.

Error messages are printed only if switch 1 and 11 are reset.

OPERATING INSTRUCTIONS

NOTE: The program can be run with the optional jumper on the interface card in the W2 position. This reduces the time required to check the four upper decade dividers. If jumper W2 on the interface card is used, set switch 4 to indicate to the program that the jumper is in that position. At the completion of testing, the W2 jumper must be removed if the card is to function properly.

To Configure the Diagnostic

a. Optionally load the SIO Teleprinter driver with the Basic Binary Loader and configure the driver.

b. Load the 2100A Time Base Generator Test Tape with the Basic Binary Loader.

c. Set Starting Address 2_8 or 111_8.

d. Press RUN. The computer halts and 107000_8 is displayed in MEMORY DATA.

e. Set the switch register to the Time Base Generator Select Code.

f. Press RUN.

1. If the computer halts with 107000_8 displayed in MEMORY DATA, the select code was not in the range 10_8-77_8. Go to step e.

2. If the computer halts with 107001_8 displayed in MEMORY DATA, enter the contents of the internal switch register into the external switch register and press RUN.

3. When the computer halts with 107077_8 displayed, configuration is complete. To start the program, press RUN and go to step c of the procedure, *To Load And Execute The Diagnostic*.

NOTE: The program can be configured from location 111_8 at any time. It can be configured from location 2_8 only after loading and before the diagnostic has been run since running destroys the link in location 2_8.

To Make A Tape Of The Configured Diagnostic

a. If a High Speed Tape Punch is available, load the SIO Tape Punch driver with the Basic Binary Loader and configure the driver.

b. If a High Speed Tape Punch is not available, turn on the teleprinter tape punch.

c. Load the SIO System Dump.

d. Set Starting Address 2_8.

e. Set switch register bit 15.

f. Press RUN.

g. A configured 2100A Time Base Generator Test tape is punched. The computer halts with 102077_8 displayed in MEMORY DATA. To make additional copies of the configured 2100A Time Base Generator Test Tape, press RUN.

To Load And Execute The Diagnostic

a. Load the configured 2100A Time Base Generator Test Tape with the Basic Binary Loader.

b. Set Starting Address 100_8.

c. If program options other than those set into the internal switch register during the procedure *To Configure The Diagnostic* are to be used, perform these steps:

   1. Press S.
   2. Set the program option bits of the DISPLAY REGISTER according to Table GEN-1.

d. Press RUN.

NOTE: To access and loop on a specific test, set switch register bit 15. The computer halts and 102076_8 is displayed in MEMORY DATA at the end of each test, with the test number contained in the A-register. Once the desired test is reached, reset switch register bit 15 and set bit 13. The program now loops on this test until bit 13 is reset. If necessary, set switch register bits 14 and 11 to suppress all error indications until the desired test is reached.

This information does not apply to tests 14, 15, 16, 17, 32, 33, 34, and 35. (See Table GEN-1, Note under Switch 13.)

Table GEN-1

Program Options--Switch Register Settings

SWITCH	MEANING IF SET
15	HALT 102076_8 AT END OF TEST (test number contained in A-register after halt.)
14	SUPPRESS ERROR HALTS
13	REPEAT LAST TEST
	NOTE: Tests 13, 14, 15, 16 and 17 all loop back to Test 13 if switch 13 is set. Tests 31, 32, 33, 34, and 35 all loop back to Test 31 if switch 13 is set.
12	HALT 102077_8 AT END OF PASS (pass count contained in the A- and B-registers after halt.)
11	SUPPRESS ERROR MESSAGES
10	SUPPRESS NON-ERROR MESSAGES
9	
8	INCLUDE 10 SECOND RELATIVE TIMING TEST
7	INCLUDE 100 SECOND RELATIVE TIMING TEST
6	INCLUDE 1000 SECOND RELATIVE TIMING TEST
5	
4	INDICATES OPTIONAL JUMPER IS IN W2 POSITION
3	
2	SKIP TEST 25 (requires operator response)
1	INDICATES THAT NO TELETYPE IS AVAILABLE
0	OVERRIDE THE INTERNAL SWITCH REGISTER

Table GEN 2

Diagnostic Messages

NOTE: If a program halt occurs (see Table GEN-1 bit 14), and data is associated, the data is contained in the A- and/or B-registers. If a message is printed (see Table GEN-1 bits 10 and 11), any data associated is included in the message.

MEMORY DATA	Message	Comment
	21ØØA TBG DIAGNOSTIC	Header message.
102000	PRESS EXT. PRESET, PRESS RUN	Initializing halt for Test 25. To skip Test 25 for subsequent passes, set switch register bit 2. (See Table GEN-1.)
102001	E-1 CLF Ø - SFC Ø	Cannot clear, set, or test interrupt system.
102002	E-2 CLF Ø - SFS Ø	(Same as 102001)
102003	E-3 STF Ø - SFC Ø	(Same as 102001)
102004	E-4 STF Ø - SFS Ø	(Same as 102001)
102005	E-5 INTP.! IEN?	Irrecoverable halt - program interrupted with TBG flag and control flip-flops set but with interrupt system off. Check IEN signal line.
102006	E-6 CLF *x* - SFC *x*	Cannot clear, set, or test TBG flag. *x* = TBG select code.
102007	E-7 CLF *x* - SFS *x*	(Same as 102006)
102010	E-1Ø STF *x* - SFC *x*	(Same as 102006)
102011	E-11 STF *x* - SFS *x*	(Same as 102006)
102012	E-12 FLG *x* set by STF *y*	Select code screening test: *x* = TBG select code. *y* (in A-register at halt) = select code causing the TBG flag to set.

Table GEN-2 (cont.)

MEMORY DATA	Message	Comment
102013	E-13 NO INTP.	Did not interrupt with TBG flag set, TBG control flip-flop set, and interrupt system on.
102014	E-14 INTP. ADDR. = *x* SHOULD BE *y*	Interrupted at wrong time: *x* (in A-Register at halt) = actual return address left in interrupt subroutine; *y* (in B-Register at halt) = expected return address. Possibly a priority-affecting instruction did not hold off the interrupt.
102015	E-15 CENT. INTP. REG. = *x*	*x* (in A-Register at halt) = contents of central interrupt register.
102016	E-16 INTP.! IAK?	Irrecoverable halt - interrupted after interrupt system was turned back on. Check IAK signal line.
102017	E-17 FLAG NOT SET	TBG flag reset following interrupt.
102020	E-2Ø INTP'D FOLLOWING CLC *x*	CLC *x* instruction did not reset control flip-flop. *x* = TBG select code.
102021	E-21 INTP'D FOLLOWING CLC Ø	CLC Ø instruction did not reset TBG control flip-flop. Check CRS signal line.
102025	E-25 FLAG SET! POPIO?	EXTERNAL PRESET did not set TBG flag. Check POPIO signal line.

Table GEN-2 (cont.)

MEMORY DATA	Message	Comment
102030	E-3Ø STATUS NOT Ø, IS *x*	STC TBG instruction did not reset error flip-flop or input lines other than bit 4 not 0. *x* (in A-Register at halt) = actual status (input line contents); Ø (in B-Register at halt) = expected status.
102031	E-31 {W1 / W2} 1 MS TEST {NO INTP / *x/y*}	1 ms relative timing test error (Test 31). *x* (in A-Register at halt) = actual count; *y* (in B-Register at halt) = expected count. (One or the other of the items in brackets { }, but not both, are printed.) At the halt, if the E-Register = 0, there was no interrupt; if the E-Register = 1, there was an interrupt.
102032	E-32 STATUS AFTER 1ST INTP. NOT Ø IS *x*	Error flip-flop should not be set immediately after the interrupt in Test 31. *x* (in A-Register at halt) = actual status (input line contents); Ø (in B-Register at halt) = expected status.
102033	E-33 FLAG NOT SET	TBG flag not set following interrupt in Test 31.
102034	E-34 2ND 1 MS INTP.	Another interrupt occurred following the interrupt in Test 31. Possibly, the TBG flag buffer flip-flop was not inhibited.

Table GEN-2 (cont.)

MEMORY DATA	Message	Comment
102035	E-35 STATUS NOT 2Ø, IS *x*	Error flip-flop (bit 4) not set and/or other input lines not 0. *x* (in A-Register at halt) = actual status (input line contents); $2Ø_8$ (in B-Register at halt) = expected status.
102036	E-36 STATUS NOT Ø, IS *x*	A set error flip-flop not reset by a STC TBG instruction and/or other input lines not 0. *x* (in A-Register at halt) = actual status (input line contents); expected status in B-Register at halt.
102037	E-37 INTP. FOLLOWING OTB *x*	OTB TBG instruction did not reset TBG control flip-flop. *x* = TBG select code.
102040	E-4Ø W1 Ø.1 MS TEST {NO INTP. / *x/y*}	Halts 102040 through 102047 and messages E-4Ø through E-47 are
102042	E-42 {W1 / W2} 1Ø MS TEST {NO INTP. / *x/y*}	Relative Timing Test errors: *x* (in A-Register at halt) =
102043	E-43 {W1 / W2} 1ØØ MS TEST {NO INTP. / *x/y*}	actual count; *y* (in B-Register at halt) = expected count. At
102044	E-44 {W1 / W2} 1 SEC TEST {NO INTP. / *x/y*}	the halt, if E-Register = 0, there was no interrupt; if E-
102045	E-45 W1 1Ø SEC TEST {NO INTP. / *x/y*}	Register = 1, there was an interrupt. (One or the other
102046	E-46 W1 1ØØ SEC TEST {NO INTP. / *x/y*}	of the items in brackets { }, but not both, are printed.)
102047	E-47 W1 1ØØØ SEC TEST {NO INTP. / *x/y*}	

Table GEN-2 (cont.)

MEMORY DATA	Message	Comment
102076		End of test halt. A-Register contains the test number.
102077		End of pass halt. The pass count is contained in the A- and B-Register with the B-Register containing the most significant bits.
1060*xx*		Unexpected trap cell halt. *xx* = select code.
107000		Start of configuration halt. Enter select code of TBG *NOTE: Also occurs if entered select code is not in range 10_8-77_8.*
107001		Configuration halt. Enter contents of internal switch register.
107077		End of configuration halt. To start the program press RUN.

HP 2100 GENERAL PURPOSE REGISTER TEST

HP Product No. 24196

This diagnostic program is used to test the interface board(s) in any of the following interface kits:

HP 12554	16 Bit Duplex Register (Positive Logic)
HP 12554-01	16 Bit Duplex Register (Negative Logic)
HP 12566	Microcircuit Interface (Ground-true output)
HP 12566-01	Microcircuit Interface (Ground-true output, party-line)
HP 12566-02	Microcircuit Interface (Positive-true)
HP 12597	8-Bit Duplex Register (Positive Logic)
HP 12597-01	8-Bit Duplex Register (Negative Logic)
HP 12597-02	Punched Tape Reader Interface
HP 12597-03	Tape Punch Interface
HP 12602	Optical Mark Reader Interface
HP 12875	Processor Interconnect Kit

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Manual of Diagnostics

Diagnostic Program Procedure

HP 12554-90026

July 1971

HP 2100 GENERAL PURPOSE REGISTER TEST

The HP 2100 General Purpose Register Test checks operation of several types of interface boards as listed on the title page of this text.

HARDWARE CONFIGURATION

This program is run on an HP 2100 computer with 4K or more memory. A teleprinter should be used to report errors and messages to the user.

Each interface board tested by this program has circuit jumpers installed in positions described in the Operating and Service Manual for that particular board. The normal installation of the jumpers may have to be changed temporarily while this diagnostic program is run, then returned to normal after the program is complete. Refer to Appendix A of this text for the jumper positions allowed for the board to be tested.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

The teleprinter SIO driver, if used, is loaded and configured first. Then the diagnostic program is loaded and configured in three phases:

1. Hardware configuration is specified by setting the switch register as listed in Table GR-1, then pressing RUN.
2. Data bits are selected for testing by setting switch register bits corresponding to those bits on, then pressing RUN.
3. Program options for a normal run of the program are selected by setting the switch register as listed in Table GR-2, then pressing RUN. These settings become an internal switch register. If any program option set in the internal switch register is to be changed during a run of the program, the internal switch register may be overridden by setting front panel switch register bit 0 on, then setting other bits as listed in Table GR-2.

After the diagnostic program is configured, a permanent copy of the program (and the teleprinter SIO driver, if included) can be made to eliminate the configuration steps for subsequent uses of the program. To do so, load and run the SIO System Dump program before the diagnostic program.

If the diagnostic program detects an error, it prints an error message on the teleprinter and/or halts with a MEMORY DATA value displayed. (Exceptions to this are trap cell halts 1060*xx*, in locations 2_8-77_8 and halts 102017_8 and 102020_8, none of which print a message. See Table GR-3. The cause of any special halt should be determined by the user before the diagnostic program is run or restarted.) If a teleprinter is not available, the MEMORY DATA display is checked against Table GR-3 to determine the error or message. If data associated with the halt is to be read, that data is displayed from the A- and/or B-Register. All program halt displays and their meanings are summarized in Table GR-3.

PROGRAM ORGANIZATION

This program consists of the following routines:

INITIALIZE — This routine sets trap cell halts into all locations within the range 2_8 through 77_8 not used by this diagnostic program, and prints the start-of-diagnostic message on the teleprinter (if available). If an unexpected interrupt to a trap cell location occurs, the computer halts with 1060*xx* displayed (*xx* = the trap cell location). The user should determine the cause of the trap cell halt before the program is run or restarted.

BI/O — The basic I/O routine checks all flag instructions and the ability to enable and disable interrupts. BI/O also tests the ability to interrupt by forcing an interrupt, checking the return address for correct location, and checking the interrupt acknowledge. Next, BI/O checks the control reset

BI/O (cont.)

instructions. Finally, BI/O performs the PRESET test, if that program option is selected. Before the PRESET test starts, the program halts with 102007_8 displayed to allow the user to press INTERNAL and EXTERNAL PRESET, then press RUN. The PRESET test checks for flag set, interrupts disabled, control bit cleared, and output buffer register cleared.

DB

The data buffer test checks the input and output buffers by comparing inputs and outputs for all possible combinations of the data bits specified in the second phase of program configuration. Those bits not specified for testing are masked off and are not included in this test.

NOTE: If an error occurs during this test, either one of two methods may be used to trouble-shoot the error. See "Error Analysis."

END

This routine prints the end-of-diagnostic message on the teleprinter (if available) and restarts the program if it is to run again. (See Table GR-2 bit 12.)

NOTE: This END routine has provisions for return to a suitable executive program if present.

Limitations

This diagnostic program has several limitations that apply to any of the interface boards:

- It does not check the gating functions of jumpers W9 through W12 in the HP 12554-60023 and HP 12554-60024 boards or jumpers W6 through W8 in the HP 12566-6001 and HP 12566-6002 boards.
- It does not check the Device Command flip-flop reset signal carried, when CLC or CRS signals occur, by jumper W13 in the HP 12554-60023 and HP 12554-60024 boards or jumper W9 in the HP 12566-6001 and HP 12566-6002 boards.

- The DMA portion of an interface board is not tested.
- Four possible priority string errors can exist in an interface board. Each is tested for a board as follows:

  1. Does the board receive priority? Tested by running this diagnostic program.
  2. Can the board be denied priority? To make this test, the user must extract an unused higher-priority board then run this program and expect a halt with 102005_8 displayed. (See Table GR-3.)
  3. Does the board deliver priority? This can be tested only by running a diagnostic program for a lower priority board to some other device.
  4. Can the board deny priority? Not tested by this program.

OPERATING INSTRUCTIONS

a. Install a test connector on the interface board to be tested. (See Appendix A.) The test connector should be a 24-pin connector that mates with board's 48-pin edge, to short all output pins to the adjacent input pins. If the board is for an HP 12566, HP 12566-01, HP 12566-02, or HP 12875 kit, the test connector must also have pin 22 connected to pin 23.

b. Install the board in an input/output slot; every slot of higher-priority must contain either an interface board or a priority jumper board. The teleprinter (if used) and any other input/output devices must be properly installed and their driver programs loaded and configured before this General Purpose Register Test is loaded and run.

c. If a configured copy of the diagnostic program is available, skip directly to step h.

d. Use the Basic Binary Loader to load the SIO teleprinter driver, then configure that driver.

e. Use the Basic Binary Loader again, to load the HP 2100 General Purpose Register Test (unconfigured).

f. Set the starting address 2_8, then configure the program in three phases:

   1. To specify the hardware configuration, set the switch register as listed in Table GR-1, then press RUN. If the settings are correct, the program halts with 102075_8 displayed.

   2. To specify the bits to be tested (for example, all 16 bits for a 16-Bit duplex register), set the corresponding bits in the switch register on, then press RUN. The program halts with 102076_8 displayed.

   3. To select program options in the internal switch register, set the switch register as listed in Table GR-2, then press RUN. The program halts with 107077_8 displayed.

g. If a permanent copy of the configured program (and the SIO teleprinter driver) is wanted, use the SIO System Dump program to punch a configured HP 2100 General Purpose Register Test tape. If not, skip directly to step i.

h. Use the Basic Binary Loader to load the configured HP 2100 General Purpose Register Test tape.

i. Set the starting address 100_8.

j. If program options other than those set in the internal switch register (step f, phase 3) are to be used, set switch register bit 0 on, then set other switch register bits for the desired program options, as listed in Table GR-2.

k. Press INTERNAL and EXTERNAL PRESET and press RUN. The program begins execution according to the program options selected.

l. If the PRESET test within the BI/O routine is to be performed, the program prints a message and/or halts with 102007_8 displayed. Press INTERNAL and EXTERNAL PRESET, then press RUN.

m. After all tests have been run, the program prints a message on the teleprinter (if available) to report that it has finished. Then, if program option bit 12 is set on (see Table GR-2), the program halts with 102077_8 displayed.

ERROR ANALYSIS

All program messages printed on the teleprinter are prefixed by an alphanumeric code. An H prefix indicates an operating instruction, and an E prefix indicates an error message.

All program halts display a MEMORY DATA value. Refer to Table GR-3 to analyze the halt conditions, then press RUN to resume the program.

If a trap cell halt occurs in the teleprinter channel, change the program options to suppress all teleprinter messages (see Table GR-2, bits 0 and 11), then restart the program at the starting address 100_8.

If an error halt occurs during the Data Buffer test (DB), choose either of two methods to trouble-shoot the error:

a. Repeat the last test pattern continuously by changing the program option. (See Table GR-2, bits 0 and 13.)

b. Use a trouble-shooting routine included in the diagnostic program. Set the starting address 1000_8, set any desired data bit pattern into the switch register, then press RUN. The trouble-shooting routine then continuously repeats that data bit pattern output and input for signal tracing on an oscilloscope.

Table GR-1
Hardware Configuration--Switch Register Settings

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit	Function
0-5	Set to the select code of the interface board to be tested.
6	Spare.
7	Set on if a teleprinter is not available.
8-15	Spares.

Table GR-2
Program Options--Switch Register Settings

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit	Function
0	May be set on at any time after configuration to override the internal switch register for the current run of the program. This bit must be used to change any program option selected in the internal switch register.
1-5	Spares.
6	Set on to continuously repeat the last data bit pattern output in the Data Buffer test (DB).
7	Spare.
8	Set on to omit the Data Buffer Test (DB), or to exit from DB during a run.
9	Set on to suppress start and stop messages.
10	Set on to omit the PRESET test (within BI/O).
11	Set on to suppress all teleprinter messages.
12	Set on to halt the program at the end of a complete cycle.
13	Set on to recycle the current test instead of advancing to the next test.
14	Set on to suppress error halts.
15	Set on to halt at the end of each separate test within the program (with the appropriate message on the teleprinter). The user decides whether to set bit 13 to repeat the last test performed.

Table GR-3

Diagnostic Messages

MEMORY DATA	Test	Message	Comments
102001	BI/O	E1. CLF DID NOT CLEAR FLAG OR SFS CAUSED SKIP WITH FLAG CLEAR	Test the ability to clear the flag and test the SFS instruction.
102002	BI/O	E2. CLF DID NOT CLEAR FLAG OR SFC CAUSED NO SKIP WITH FLAG CLEAR	Test the ability of the SFC instruction.
102003	BI/O	E3. STF DID NOT SET FLAG, OR SFC CAUSED SKIP WITH FLAG SET	Test the ability to set the flag and test the SFC instruction.
102004	BI/O	E4. STF DID NOT SET FLAG OR SFS CAUSED NO SKIP WITH FLAG SET	Test the SFS instruction.
102005	BI/O	E5. DID NOT INTERRUPT	Test the interrupt capability.
102006	BI/O	E6. THE RETURN ADDRESS IS NOT CORRECT	The return address that resulted from the interrupt is incorrect.
102007	BI/O	H7. PRESS PRESET, THEN PRESS RUN	Press INTERNAL and EXTERNAL PRESET.
(no halt)	INIT	H8. START GENERAL PURPOSE REGISTER DIAGNOSTIC	Message suppressed if bit 9 set.
102010	BI/O	E1Ø. PRESET DID NOT SET THE FLAG	EXTERNAL PRESET failed.
102011	BI/O	H11. END BI/O	Select program options (see Table GR-2) and press RUN.
102012	DB	H12. END DATA BUFFER TEST	Select program options (see Table GR-2) and press RUN.
102013	BI/O	E13. PRESET DID NOT SET FLAG AND DID NOT DISABLE INTERRUPTS	INTERNAL and EXTERNAL PRESET failed.

Table GR-3. Diagnostic Messages (cont.)

MEMORY DATA	Test	Message	Comments
102014	BI/O	E14. INTERRUPT ACKNOWLEDGE DID NOT WORK. TEST ABORTED	Remaining tests of BI/O are skipped.
102015	BI/O	E15. CLC Ø DID NOT CLEAR CONTROL	CLC Ø instruction did not reset control flip-flop.
102016	BI/O	E16. PRESET DID NOT CLEAR CONTROL	EXTERNAL PRESET failed.
102017	BI/O	(none)	CLF Ø did not disable interrupts or SFS Ø caused a bad skip.
102020	BI/O	(none)	CLF Ø did not disable interrupts or SFC Ø did not skip.
102021	BI/O	E21. STF Ø DID NOT ENABLE INTS OR SFC Ø CAUSED BAD SKIP	STF Ø did not enable interrupts or SFC Ø caused a bad skip.
102022	BI/O	E22. STF Ø DID NOT ENABLE INTS OR SFS Ø DID NOT SKIP	STF Ø did not enable interrupts or SFS Ø did not skip.
102023	DB	E23. OUTPUT = *xxxxxx*. INPUT = *xxxxxx*	Data received from input buffer does not equal data sent to output buffer. A-register contains output data, B-register contains input data.
102027	BI/O	E27. PRESET DID NOT DISABLE INTERRUPTS	INTERNAL PRESET failed.
102041	DB	E41. NO DEVICE COMMAND OR DEVICE FLAG DOES NOT SET FLAG	Test Device Command and ability of Device Flag to set flag.
102044	BI/O	E44. PRESET DID NOT RESET OUTPUT DATA BITS TO ZERO	POPIO (B) should clear output data register when EXTERNAL PRESET is pressed.

Table GR-3. Diagnostic Messages (cont.)

MEMORY DATA	Test	Message	Comments
102045	BI/O	E45. CLC ON CHANNEL DID NOT CLEAR CONTROL	Test ability of CLC on selected channel to clear the control flip-flop.
102046	BI/O	E46. INTERRUPTED AFTER CLF Ø	CLF Ø should prevent interrupts. Check IEN signal.
102074	CONF.	(none)	Configuration error halt. Set correct bits in switch register (see Table GR-1) and press RUN.
102075	CONF.	(none)	Set switch register to specify data bits to be tested.
102076	CONF.	(none)	Set internal switch register for desired program options (see Table GR-2).
102077	END	H77. DIAGNOSTIC HAS BEEN COMPLETED	End of diagnostic. To repeat, set program options (see Table GR-2) and press RUN.
1060*xx*	any	(none)	Trap cell interrupt. M = memory address when interrupted, *xx* = the trap cell location.
107077	CONF	(none)	Configuration complete. Use SIO System Dump or set starting address 100_8, press INTERNAL and EXTERNAL PRESET and press RUN.

APPENDIX A
DIAGNOSTIC PROGRAM REQUIRED JUMPER INSTALLATIONS

Each of the interface boards that may be tested by the General Purpose Register Diagnostic program must have, during a run of the program, an allowed combination of circuit jumper positions installed. The combinations allowed are listed below, according to the type of interface board to be tested:

HP 12554 16-Bit Duplex Register (Positive Logic)

Any one of six different combinations is allowed:

Positions under Combination Number

Jumper Number	1	2	3	4	5	6
W4	B	B	A/B	A	A	A/B
W5	B	A	A/B	A	B	A/B
W6	A/B	A	C	A/B	A	C
W7	A	A	A	B	B	B

NOTE: Jumpers not listed may be installed in any position described in the Operating and Service Manual for this board.

HP 12554-01 16-Bit Duplex Register (Negative Logic)

Any one of six different combinations is allowed:

Positions under Combination Number

Jumper Number	1	2	3	4	5	6
W4	A/B	A	A/B	A/B	B	A/B
W5	A	A	A/B	B	A	A/B
W6	B	A	C	B	A	C
W7	B	B	B	A	A	A

NOTE: Jumpers not listed may be installed in any position described in the Operating and Service Manual for this board.

HP 12566 Microcircuit Interface (Ground-true output)

(Same as HP 12566-02)

HP 12566-01 Microcircuit Interface (Ground-true output, party-line)

(Same as HP 12566-02)

HP 12566-02 Microcircuit Interface (Positive-true)

Any one of six different combinations is allowed:

		1	2	3	4	5	6
Jumper Number	W1	B	A	A	A	B	B
	W2	A	B	C	C	C	C
	W3	A	B	B	B	A	A
	W4	B	B	A	B	A	B

NOTE: Jumpers not listed may be installed in any position described in the Operating and Service Manual for these boards.

HP 12597 8-Bit Duplex Register (Positive Logic)

Only one combination is allowed:

W1	A	W7	connected
W2	A	W8	removed
W3	connected	W9	removed
W4	connected	W10	removed
W5	connected	W11	removed
W6	connected	W12	removed

HP 12597-01 8-Bit Duplex Register (Negative Logic)

Only one combination is allowed:

W1	A	W7	removed
W2	A	W8	removed
W3	connected	W9	removed
W4	connected	W10	connected
W5	removed	W11	connected
W6	removed	W12	connected

HP 12597-02 Punched Tape Reader Interface

(Same as HP 12597.)

HP 12597-03 Tape Punch Interface

(Same as HP 12597.)

HP 12602 Optical Mark Reader Interface

Only one combination is allowed:

W1	connected	W8	connected
W2	connected	W9	connected, then removed*
W3	connected	W10	connected
W4	B	W11	connected
W5	B	W12	connected
W6	B	W13	A
W7	A	W14	B

HP 12875 Processor Interconnect Kit

(Same as HP 12566-01.)

*Jumper W9 in the HP 12602 board is connected only during a run of the diagnostic. When the board is returned to normal use, W9 must be removed.

HP 2100 DMA DIAGNOSTIC

HP Product No. HP 24195

HEWLETT hp PACKARD

11000 Wolfe Road
Cupertino, California 95014

Manual of Diagnostics
Diagnostic Program Procedure
HP 12578-90014

July 1971

HP 2100 DMA DIAGNOSTIC

The test program for the Direct Memory Access option can be used in two modes. In the Long Test Mode, all functions of the DMA are tested, and any functions specific to the select code under test are tested. The Short Test Mode tests only the functions of the select code being tested. All select codes can be tested by installing the proper register card in the I/O slot for the select code to be tested and changing a diagnostic program option.

HARDWARE CONFIGURATION

This diagnostic test program runs on any HP 2100 computer with at least 4K of memory. To test the DMA thoroughly, a Micro-Circuit Register must be used. Although the test program can run with only a teleprinter, certain restrictions are imposed. (See Program Limitations.) A special edge connector is required for the Micro-Circuit Register.

The Micro-Circuit Register, HP 12566, must have the following jumper configuration:

W1-B W2-A
W3-A W4-B
W5 through W8 - IN
W9-A

The special edge connector must be wired as follows:

A-1	K-9	U-17
B-2	L-10	V-18
C-3	M-11	W-19
D-4	N-12	X-20
E-5	P-13	Y-21
F-6	R-14	AA-22-23
H-7	S-15	BB-24
J-8	T-16	

Connector HP 1251-0332 can be used, with pin 22 shorted to pin 23.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

When a teleprinter is used, the SIO teleprinter driver is loaded and configured before the diagnostic program. Then the diagnostic program is loaded and configured.

A permanent copy of the configured program (and the SIO teleprinter driver, if included) eliminates repeating the configuration steps for subsequent uses of the diagnostic. To make a copy, load the SIO System Dump program and run it before running the diagnostic program.

The Long Test Mode, selected by setting program option bit 7 off, should be done for at least one select code to check all DMA functions; using the Micro-Circuit Register the Long Test Mode requires over three minutes of run time. After operation of the DMA functions is confirmed, the remaining select codes can be checked by the Short Test Mode. In the Short Test Mode functions specific to the select code being tested are checked (SRQ lines to each DMA channel and select code lines generated by each DMA channel).

If an error is detected during operation, the program prints a message on the teleprinter, then halts with a MEMORY DATA value in the DISPLAY REGISTER. (Exceptions to this are trap cell halts $1060xx_8$ located in low memory 2_8-77_8 and halts for which a printed message is not appropriate or necessary.) The cause of any of these halts should be determined by the user before the program is run or restarted.

To repeat any test, set program option bit 13 on after an error halt then press RUN.

To reconfigure after running the program, use the re-start address 111_8 instead of the starting address 2_8.

PROGRAM LIMITATIONS

When the Micro-Circuit Register is not available, the teleprinter interface board can be used; however, 8-bit data transfers are made rather than 16-bit transfers, checking only the eight low-order bits. If the register board is used without the teleprinter, the diagnostic test program tests all sixteen

bits; but errors must be interpreted from MEMORY DATA and the contents of the A- and B-Registers, according to Table DMA-3, after an error halt.

The Short Test Mode, consiting of tests T.17 and T.20, tests only the functions of the select code being tested, so the Long Test Mode should be used on at least one select code.

This diagnostic program does not check the maximum data rate specification of the DMA.

Since each channel is tested individually, no testing of simultaneous operation is done.

PROGRAM ORGANIZATION

This diagnostic program performs the following routines.

CONFIG	Inputs and stores hardware information supplied by the operator through the switch register during configuration time. Also stores selected program options in an internal switch register.
INIT	Sets trap cell halts in locations 2_8-77_8 and prints the start-of-diagnostic message on the teleprinter.
T.1	Tests the DMA flag instructions.
T.2	Tests the ability to enable and disable the interrupt system.
T.3	Tests the DMA interrupt capability by forcing an interrupt, checking the return address for the correct location, and checking the interrupt acknowledge
T.4	Tests the control reset instructions.

T.5 If program option bit 9 is set off, tests the PRESET functions. Before the PRESET test starts, the program halts with 102027_8 in the DISPLAY REGISTER, to allow the user to press INTERNAL and EXTERNAL PRESET.

T.6 Tests DMA interrupt priority. Checks priority of DMA channel 1 (DMA1) over DMA channel 2 (DMA2) and over the I/O select code under test (which contains MCR or teleprinter interface card). Checks ability of DMA PH5 signal to inhibit I/O interrupts. Checks DMA 2 priority over I/O select code under test.

T.7 Tests the ability to set and read the word count registers for all numbers up to the maximum word count (65,535).

T.10 Tests the word count increment function (rollover) by setting the word count registers to minus one and forcing a data transfer which should cause the DMA to interrupt.

T.11 Tests the direct memory address registers by making DMA output transfers from every available location in memory.

T.12 Tests the ability of the DMA to set an interface control flip-flop when bit 15 of the DMA program control word has bet set to a one.

T.13 Tests the ability of the DMA to clear an interface control flip-flop when bit 13 of the DMA program control word has been set to a one.

T.14 Tests the ability of DMA generated signal to clear interface flag after transfer.

T.15 Tests the DMA output capability with all possible 16-bit data patterns and their complements if MCR is used, or with all possible 8-bit patterns and their complements if TTY interface is used.

T.16 Tests the DMA input capability with the same data patterns used in T.15

NOTE: The Long Test Mode (program option bit 7 set off) performs all tests, the Short Test Mode (bit 7 set on) performs only tests T.17 and T.21.

T.17 Used in the Short Test Mode, this routine uses subroutines in T.15 to output one word through each DMA channel.

T.21 Tests the DMA for illegal response to incorrect select codes.

END If program option bit 12 is set on, END prints the end-of-diagnostic message on the teleprinter and halts, or if bit 12 is set off, END restarts the program.

NOTE: This END routine has provisions for return of execution control to a suitable executive program, if present.

OPERATING INSTRUCTIONS

NOTE: This procedure presumes the use of a Micro-Circuit Register. The register card must have jumpers wired as described under HARDWARE CONFIGURATION and must be connected through an edge connector, also described in that section. If the register card is not used, install the teleprinter interface card in the slot to be tested; limitations described will apply.

a. Install the register card in the I/O slot to be tested. If the Long Test Mode is to be used, make sure that all I/O slots of Higher priority have either an interface card or a priority jumper installed.

b. If the test program is being run for the first time and a teleprinter is available, use the Basic Binary Loader (BBL) to load the teleprinter driver then configure the driver. Then use BBL again to load this diagnostic program. If a configured HP 2100 DMA Diagnostic tape is available, skip the following configuration procedure (steps c through f); load the configured tape using BBL, and start at step g.

NOTE: A teleprinter driver is required for SIO System Dump.

c. Set the starting address 2_8 then press INTERNAL and EXTERNAL PRESET.

d. Set the switch register for program configuration as listed in Table DMA-1 then press RUN. The program halts with MEMORY DATA 107076_8 in the DISPLAY REGISTER.

e. Set the switch register for desired program options as listed in Table DMA-2 then press RUN. The program halts with MEMORY DATA 107077_8 in the DISPLAY REGISTER.

f. To punch a configured HP 2100 DMA Diagnostic tape, use SIO System Dump, then continue with the procedure. If a configured tape is not required, skip this step.

g. Set the starting address 100_8.

h. If program options other than those set into the internal switch register by step e are to be used, set program option bit 0 on, then set the other program option bits as listed in Table DMA-2.

i. Press INTERNAL and EXTERNAL PRESET then press RUN. The program executes according to the program options selected. If program option bit 6 is set on, the program halts with 103013_8 in the DISPLAY REGISTER. Set bits 5-0 of the switch register to the select code to be tested then press RUN.

j. If the PRESET test (T.5) is to be performed, the program halts with 102027_8 in the DISPLAY REGISTER. Press INTERNAL and EXTERNAL PRESET then press RUN.

k. Upon completion of all tests, the program prints a message and/or halts with 102077_8 in the DISPLAY REGISTER. Turn computer POWER OFF, move the register card to the next select code to be tested, then turn POWER ON again. (If the teleprinter card has been moved, reload and reconfigure its SIO driver.) Begin test on new select code at step g. Repeat steps g through k until all select codes have been tested.

ERROR ANALYSIS

All halts display a MEMORY DATA value in the DISPLAY REGISTER. Refer to Table DMA-3 to analyze the halt conditions, then press RUN to continue the diagnostic program.

If a trap cell halt occurs on the teleprinter select code, change the program option to suppress all teleprinter messages (see Table DMA-2), then restart at location 100_8.

Table DMA-1

Hardware Configuration--Switch Register Settings

Bits	Function
0-5	Set to the Register Card (or teleprinter select code interface).
6	Set on if teleprinter is not available.
7-15	Spares.

Table DMA-2

Program Options-- Switch Register Settings

Bits	Function
0	Set on to override the internal switch register, to change a program option. This bit has no effect when set on in the internal switch register.
1-5	Spares.
6	Set on to halt at the beginning of the program, to allow entry of a new select code.
7	Set on to use the Short Test Mode, otherwise the Long Test Mode is to be used.
8	Set on if a teleprinter interface card is to be used to test the select code, otherwise the program assumes a Micro-Circuit Register card is to be used.
9	Set on to omit the PRESET test (T.5).
10	Set on to suppress non-error messages.
11	Set on to suppress all messages.
12	Set on to halt the program after a complete cycle.
13	Set on to loop on the current test instead of advancing to the next test.
14	Set on to suppress error halts.
15	Spare.

TABLE DMA-3

Diagnostic Messages

MEMORY DATA	Test	Message*	Comments
(no halt)	INIT.	HØ. START DMA DIAGNOSTIC	Initial Message.
102001	T.1	E1. CLF6 OR SFS6 ERR	DMA1--Test the ability to clear the flag and test the SFS instruction.
102002	T.1	E2. CLF6 OR SFC6 ERR	DMA1--Test the ability to clear the flag and test the SFC instruction.
102003	T.1	E3. STF6 OR SFC6 ERR	DMA1--Test the ability to set the flag and test the SFC instruction.
102004	T.1	E4. STF6 OR SFS6 ERR	DMA1--Test the ability to set the flag and test the SFS instruction.
102005	T.1	E5. CLF7 or SFS7 ERR	DMA2--Test the ability to clear the flag and test the SFS instruction.
102006	T.1	E6. CLF7 OR SFC7 ERR	DMA2-- Test the ability to clear the flag and test the SFC instruction.
102007	T.1	E7. STF7 OR SFC7 ERR	DMA2--Test the ability to set the flag and test the SFC instruction.
102010	T.1	E1Ø. STF7 OR SFS7 ERR	DMA2--Test the ability to set the flag and test the SFS instruction.
102011	T.2	(none)	CLF Ø did not disable interrupts or SFS Ø caused a bad skip.
102012	T.2	(none)	CLF Ø did not disable interrupts or SFCØ did not skip.
102013	T.2	E13. STFØ OR SFCØ ERR	STF Ø did not enable interrupts or SFC Ø caused bad skip.

*"H" Message is informational
"E" Message indicates an error.

TABLE DMA-3 (Cont.)

MEMORY DATA	Test	Message	Comments
102014	T.2	E14. STFØ OR SFSØ ERR	STF Ø did not enable interrupts or SFS Ø did not skip.
102015	T.3	E15. NO D1 INT	Test the interrupt capability of DMA1.
102016	T.13	E16. NO D2 INT	Test the interrupt capability of DMA2.
102017	T.3	E17. D1 RTN ADDR ERR	DMA1--The return address that resulted from the interrupt is incorrect.
102020	T.3	E2Ø. D2 RTN ADDR ERR	DMA2--The return address that resulted from the interrupt is incorrect.
102021	T.3	E21. D1 IAK ERR	DMA1--Interrupt acknowledge failed.
102022	T.3	E22. D2 IAK ERR	DMA2--Interrupt acknowledge failed.
102023	T.4	E23. D1 CLCØ ERR	DMA1--CLC Ø instruction failed to reset the control flip-flop.
102024	T.4	E24. CLC6 ERR	DMA1--Test ability of CLC 6 instruction to clear the control flip-flop.
102025	T.4	E25. D2 CLCØ ERR	DMA2--CLC Ø instruction failed to reset the control flip-flop.
102026	T.4	E26. CLC7 ERR	DMA2--Test ability of CLC 7 instruction to clear the control flip-flop.
102027	T.5	(None)	Press INTERNAL and EXTERNAL PRESET switches, then press RUN.
102031	T.5	(None)	EXTERNAL PRESET failed to set DMA1 flag.

TABLE DMA-3 (Cont.)

MEMORY DATA	Test	Message	Comments
102032	T.5	(None)	EXTERNAL PRESET failed to set DMA2 flag.
102035	T.6	E35. D1-D2 PRIORITY ERR	DMA1 failed to take priority over DMA2.
102036	T.6	E36. D2-IO PRIORITY ERR	DMA2 failed to take priority over I/O select code being tested.
102037	T.6	E37. D1-IO PRIORITY ERR	DMA1 failed to take priority over I/O select code being tested.
102040	T.7	E4Ø. WC1 IS *xxxxxx*, SHOULD BE *xxxxxx*	Word count readback from DMA1 is different from output word. A-Register (press A) contains output word, B-Register (press B) contains input word.
102041	T.7	E41. WC2 IS *xxxxxx*, SHOULD BE *xxxxxx*	Word count readback from DMA2 is different from output word. A-Register (press A) contains output word, B-Register (press B) contains input word.
102042	T.10	E42. NO D1 INT	With interrupt system enabled, DMA1 failed to interrupt after word transfer.
103043	T.10	E43. NO D2 INT	With interrupt system enabled, DMA2 failed to interrupt after word transfer.
102044	T.10	E44. WC1 IS *xxxxxx*, SHOULD BE ZERO	DMA1 word count register was not zero when interrupt occurred. B-Register (press B) contains word count.
102045	T.10	E45. D1 INT LOC IS	DMA1 interrupted from wrong location after transfer. A-Register (press A) contains correct location, B-Register (press B) contains incorrect location.

TABLE DMA-3 (Cont.)

MEMORY DATA	Test	Message	Comments
102046	T.10	E46. WC2 IS *xxxxxx*, SHOULD BE ZERO	DMA2 word count register was not zero when interrupt occurred. B-Register (press B) contains word count.
102047	T.10	E47. D2 INT LOC IS *xxxxxx*, SHOULD BE *xxxxxx*	DMA2 interrupted from wrong location after transfer. A-Register (press A) contains correct location, B-Register (press B) contains incorrect location.
102050	T.11, T.15-T.17	E5Ø. D1 FLG CLR	DMA1 flag was not set after output transfer. A-Register (press A) contains program return address.
102051	T.11	E51. D1 OUT=*xxxxxx*, IN=*xxxxxx*, ADDR=*xxxxxx*	DMA1 made a bad output transfer, or is not transferring data from every memory location. A-Register (press A) contains expected output, B-Register (press B) contains read-in from MCR. Then, if a TTY is not used, press RUN.
102052	T.11	(None)	Non-TTY halt for E51 output address. A-Register (press A) contains address.
102053	T.11, T.15-T.17	E53. D2 FLG CLR	DMA2 flag was not set after output transfer. A-Register (press A) contains program return address.
102054	T.11	E54. D2 OUT=*xxxxxx*, IN=*xxxxxx*, ADDR=*xxxxxx*	DMA2 made a bad output transfer, or is not transferring data from every memory location. A-Register (press A) contains expected output, B-Register (press B) contains read-in from MCR. Then, if a TTY is not used, press RUN.
102055	T.11	(None)	Non-TTY halt for E54 output address. A-Register (press A) contains address.

TABLE DMA-3 (Cont.)

MEMORY DATA	Test	Message	Comments
102056	T.12	E56. D1 CTL WRD ERR	DMA1 Bit 15 of Control Word = 1, but DMA did not set interface control flip-flop after transfer.
102057	T.12	E57. D1 CTL WRD ERR	DMA1 Bit 15 of Control Word = Ø, but DMA set interface control flip-flop after transfer.
102060	T.12	E6Ø. D2 CTL WRD ERR	DMA2 Bit 15 of Control Word = 1, but DMA did not set interface control flip-flop after transfer.
102061	T.12	E61. D2 CTL WRD ERR	DMA2 Bit 15 of Control Word = Ø, but DMA set interface control flip-flop after transfer.
102062	T.13	E62. D1 CTL WRD ERR	DMA1 Bit 13 of Control Word = 1, but DMA did clear interface control flip-flop after transfer.
102063	T.13	E63. D1 CTL WRD ERR	DMA1 Bit 13 of Control Word = Ø, but DMA cleared interface control flip-flop after transfer.
102064	T.13	E64. D2 CTL WRD ERR	DMA2 Bit 13 of Control Word = 1, but DMA did not clear interface control flip-flop after transfer.
102065	T.13	E65. D2 CTL WRD ERR	DMA2 Bit 13 of Control Word = Ø, but DMA cleared interface control flip-flop after transfer.
102067	T.15	E67. D1 OUT. GOOD=*xxxxxx*, BAD=*xxxxxx*	DMA1 made a bad output transfer. A-Register (press A) contains expected output, B-Register (press B) contains read-in from MCR.

TABLE DMA-3 (Cont.)

MEMORY DATA	Test	Message	Comments
102071	T.15, T.17	E71. D2 OUT. GOOD=*xxxxxx*, BAD=*xxxxxx*	DMA2 made a bad output transfer. A-Register (press A) contains expected output, B-Register (press B) contains read-in from MCR.
102073	T.16,	E73. D1 IN. GOOD=*xxxxxx* BAD=*xxxxxx*	DMA1 made a bad input transfer. A-Register (press A) contains expected input, B-Register (press B) contains actual input.
102074	T.14	E74. D1--I/O FLG SET	DMA1 I/O Flag should be cleared by DMA after a transfer
102077	END	H77. END DIAGNOSTIC	End of diagnostic. To repeat on same I/O select code set program options and press RUN.
103000	T.3	E1ØØ. D1 IAK ERR	IAK should only clear DMA1 flag buffer, not flag.
103003	T.3	E103. DR IAK ERR	IAK should only clear DMA2 flag buffer, not flag.
103005	T.6	E1Ø5. PH5 ERR	PH5 signal did not inhibit I/O interrupts.
103012	T.14	E112. D2--I/O FLG SET	DMA2 I/O Flag should be cleared by DMA after a transfer.
103013	INIT.	(None)	Enter new select code to be tested into switch register bits 5-0 and press RUN.
103014	INIT.	(None)	Set program option bits in the switch register (Table DMA-2) and press RUN.
103015	T.16	E115. D2 IN. GOOD=*xxxxxx*, BAD=*xxxxxx*	DMA2 made a bad input transfer. A-Register (press A) contains expected input, B-Register (press B) contains actual input.

TABLE DMA-3 (Cont.)

MEMORY DATA	Test	Message	Comments
103016	T.2	E116. D1 CLFØ ERR	DMA1 interrupted with interrupt system disabled.
103017	T.2	E117. D2 CLFØ ERR	DMA2 interrupted with interrupt system disable.
103020	T.7	(None)	A-Register (press A) contains data resulting from LIA Ø. Should be zero.
103021	T.21	E121. D1 SC ERR	STF 1 set the DMA1 flag flip-flop.
103022	T.21	E122. D1 SC ERR	STF 16 set the DMA1 flag flip-flop.
103023	T.21	E123. D2 SC ERR	STF 1 set the DMA2 flag flip-flop.
103024	T.21	E124. D2 SC ERR	STF 17 set the DMA2 flag flip-flop.
103025	T.21	E125. D1 SC ERR	OTA 1 set the DMA1 word count register.
103026	T.21	E126. D1 SC ERR	OTA 12 set the DMA1 word count register.
103027	T.21	E127. D2 SC ERR	OTA 1 set the DMA2 word count register.
103030	T.21	E13Ø. D2 SC ERR	OTA 13 set the DMA2 word count register.
103031	T.7	E131. D1 CRS ERR	CRS did not clear DMA1 register card control flip-flop.
103032	T.7	E132. D2 CRS ERR	CRS did not clear DMA2 register card control flip-flop.
103033	T.14	E133. STF6 ERR	STR6 failed to turn off DMA1.
103034	T.14	E134. STF7 ERR	STF7 failed to turn off DMA2.

TABLE DMA-3 (Cont.)

MEMORY DATA	Test	Message	Comments
103035	T.6	E135. NO I/O INT	No interrupt on I/O select code. Check PRL7 signal.
1060*xx*	A11	(None)	Trap cell interrupt. M = memory address when interrupted, *xx* = trap cell location.
107074	CONFIG	(None)	Press LOADER ENABLE button to turn it off then press RUN.
107075	CONFIG & INT	(None)	The select code (switch register bits 5-Ø) is invalid. (Valid codes are 10_8-77_8.) Set the correct select code then press RUN.
107076	CONFIG	(None)	Set internal switch register for desired program options (see Table DMA-2) then press RUN.
107077	CONFIG	(None)	Configuration complete. Use SIO System Dump or set the starting address 100_8, select desired program options, press INTERNAL and EXTERNAL PRESET then press RUN.

HEWLETT PACKARD

DIAGNOSTIC PROGRAM PROCEDURES

7970/13183

MAGNETIC TAPE DIAGNOSTIC

(NINE-TRACK 1600 CPI PHASE-ENCODED FORMAT)

Diagnostic Part Number

13031

Note

This manual should be retained with and considered part of the Hewlett-Packard Manual of Diagnostics.

13183-90002

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CONTENTS

TABLES

7970/13183
MAGNETIC TAPE DIAGNOSTIC
(NINE-TRACK 1600 CPI PHASE-ENCODED FORMAT)

1. INTRODUCTION.

2. This diagnostic program tests the combined performance of the HP 7970E Digital Magnetic Tape Unit and its corresponding HP 13183A Interface Kit. All tests are modular and most can be put into a test loop to check out individual functions of the tape unit and interface combination. The program can be used to test all parameters and characteristics of the tape unit by using the interface circuitry.

3. HARDWARE REQUIREMENTS.

4. This diagnostic program can be initialized for any HP 2100 Series (2100, 2114, 2115, or 2116) Computer and HP 7970E Digital Magnetic Tape Unit (12-1/2, 25, 37-1/2, or 45 ips) interfaced with an HP 13183A Interface Kit. The diagnostic is compatible with the HP system software. A teleprinter is also required to run the diagnostic. The teleprinter uses the standard SIO driver program.

5. OPERATING PROCEDURES.

6. The following procedure is to be used when running the main diagnostic tests.

Note

All addresses and register indications are in octal notation.

a. Load the teleprinter SIO driver using the basic binary loader.

b. Load address 000002.

c. Load the I/O select code of the teleprinter in the switch register.

d. Press PRESET and RUN.

e. Load the 13031 Diagnostic Tape using the basic binary loader.

f. Load address 000100.

g. Set switch register switches 0 thru 4 with the I/O select code of the mag tape 1 printed-circuit assembly.

h. Press PRESET and RUN. Computer should halt with a T-register indication of 102000.

i. Set the switch register with the computer type and tape drive speed as follows:

(1) Set switches 14 and 15 for the type of computer.

COMPUTER	SW 15	SW 14
2116	Clear	Clear
2100	Clear	Set
2114/2115	Set	Clear

(2) Set switches 0 thru 3 for the tape drive speed.

SPEED	SW 3	SW 2	SW 1	SW 0
12.5 ips	Clear	Clear	Clear	Set
25 ips	Clear	Clear	Set	Clear
37.5 ips	Clear	Set	Clear	Clear
45 ips	Set	Clear	Clear	Clear

j. Press PRESET and RUN. Computer should halt with a T-register indication of 102001.

k. Select the desired options controlled by the switch register; refer to table 1.

l. Press PRESET and RUN. The program is now entered automatically and can still be altered by using the switch control settings in table 1. Also, the initialization section is now released; the program must be reloaded if any of the initialization parameters are to be changed.

Note

On the first pass of the diagnostic program after the program was loaded and initialized, the program automatically off-lines all tape units on the controller. Every pass thereafter, the rewind off-line test is optional, depending on whether switch 9 is set or clear.

m. To enter the operator service routines, halt the main diagnostic and enter the appropriate starting address (500 or 1100). Table 2 lists detailed information for switch settings and running the operator service routines.

Table 1. Main Diagnostic Switch Control Settings

SWITCH	STATE	FUNCTION
0 thru 3	Clear	Auto select option (Note 1).
0	Set	Select Unit 0. } (Note 2)
1	Set	Select Unit 1. } (Note 2)
2	Set	Select Unit 2. } (Note 2)
3	Set	Select Unit 3. } (Note 2)
4	Set	Inhibits extended data test.
5		Not used.
6	Set	Execute write enable test.
7	Set	Inhibits rewind and load point sense tests (Note 5).
8	Clear	Executes DMA write/read tests (Note 4).
9	Set	Executes rewind off-line test.
10		Not used.
11	Set	Overrides all error halts.
12	Set	Halts and prints diagnostic cycles complete.
13	Set	Loops on the last test completed and inhibits error message.
14	Set	Halts the diagnostic program on errors and prints error message.
15	Set	Halts after current test.

NOTES:

1. When errors occur while in the auto-select mode and multiunit operation, the diagnostic program will indicate which unit caused the errors.
2. If more than one of the select control switches (0 thru 3) are set, only the first one (starting with 0) is used to select the unit.
3. Optional tests are controlled by switches 4 thru 9.
4. Switch 8 is used for systems without the DMA option.
5. Switch 7 set inhibits tests 16 thru 22.

Table 2. Switch Settings and Functions for Operator Service Routines

SWITCH	STATE	FUNCTION
DMA TRANSFER TEST (STARTING ADDRESS = 000500)		
0 thru 7	---------	Define the characters being written on tape: set = 1, clear = 0.
15	Set	Terminates the program operation.
COMMAND EXERCISE TEST (STARTING ADDRESS = 001100)		
0	Set	Write command is issued (WCC) (Note 4).
1	Set	Write file marks (WFM).
2	Set	Read Record command is issued (RRF).
3	Set	Forward Space Record command is issued (FSR).
4	Set	Forward Space File command is issued (FSF).

Table 2. Switch Settings and Functions for Operator Service Routines (Continued)

SWITCH	STATE	FUNCTION
COMMAND EXERCISE TEST (STARTING ADDRESS = 001100) (Continued)		
5	Set	Clear command is issued (CLR).
6	Set	Gap command is issued (GAP).
7	Set	Backspace Record command is issued (BSR).
8	Set	Backspace File command is issued (BSF).
9	Set	Rewind command is issued (REW).
10	Set	Rewind Off-Line command is issued (RWO).
11	Set	Clear command is issued (CLR).
12	Set	Allows approximately a 10 ms time period after the command is issued before issuing the next command.
13	Set	Same as switch 12 except the time period is 15 ms.
14	Set	Same as switch 12 except the time period is 30 ms.
15	Set	Terminates the operation except when switch 0 is set. (If switch 0 is set, program must be restarted from address 001100.)

NOTES:

1. Any of the first six commands (0 thru 5) may be combined with any of the last six commands (6 thru 11), or any of the commands may be used alone.
2. If more than one control switch is set in either of the groups, only the first switch command will be issued, starting with switch 0 in the first group and switch 6 in the second.
3. If no switches are set when computer is in a run mode, program will become uncontrollable.
4. If the operation becomes uncontrollable from the switch register, the routine may be stopped by halting the computer and pressing PRESET. Operation may be restarted by loading address 001100.
5. Switches 0 and 9 set and all other switches clear causes the tape unit to write an ID burst, rewind, write an ID burst, rewind.....(loop continues until switch 15 is set).

7. TEST DESCRIPTIONS.

8. Table 3 lists the individual tests that make up the complete diagnostic and a short description of each of the tests.

9. MESSAGE ANALYSIS.

10. Except for initialization halts, all halts cause a printout on the teleprinter. Normal program halts are listed in table 4. When an error is detected, the diagnostic program causes a message to be printed in the following format:

```
4 TEST # 16
STATUS WAS RW,
AND IT SHOULD BE CB, TB, RW,
```

The first digit in the first line is the program cycle number or the number of times the diagnostic has been repeated. This is followed by the test number (table 2). The second line contains the test status. The third line contains what the status should have been during the test, if any. The following status mnemonics may appear in the second and third lines.

- OF: The selected tape unit is off-line or in load.
- DE: A data error was detected during data transfer.
- FP: File protect, no write ring on the tape spool.
- CR: The issued command was rejected.
- TM: Data timing error.
- ET: End-of-tape marker was sensed.
- LP: Load point marker was sensed.
- FM: A file mark was read.
- CB: Controller busy.
- TB: The selected tape unit was busy.
- RW: The selected tape unit was rewinding.
- OB: The last record read contained an odd byte.
- SE: Single track error was detected during data transfer.

Table 3. Test Descriptions

TEST NUMBER	DESCRIPTION
	UNIT SELECT AND OFF-LINE STATUS
1	Unit select 0 logic test. Unit 0 is selected and status is taken to assure that only unit 0 select status bits are set.
2	Rewind Off-Line command is given to unit 0. The status is taken to assure that the unit is off-line and that off-line status is present.
3	Unit select 1 logic test. Unit 1 is selected and the status is taken to assure that only unit 1 select lines are set.
4	Off-line status is taken for unit 1 similar to test number 2.
5	Unit select 2 logic test. A select command to unit 2 is issued and status is taken to assure that the select lines for unit 2 only have been set.
6	The off-line status for unit 2 is tested similar to test number 2.
7	Unit select 3 logic. A select command is issued to unit 3 and status is taken to assure that only unit 3 select lines are set.
8	The off-line status for unit 3 is tested similar to test number 2.
	CONTROLLER I/O CHANNEL TESTS
9	The Clear command is issued to the controller and a delay period is waited before the clear status is checked.
10	The data channel flag is set by the computer, and then tested to assure that the flag has been set.
11	The data channel flag is cleared by the computer, and then tested to assure that the flag has been cleared.
12	The command channel flag is set by the computer, and then tested to assure that the flag has been set.
13	The command channel flag is cleared by the computer, and then tested to assure that the flag has been cleared.
14	An interrupt condition is set up for the data channel to test the flag, control, and interrupt logic for that channel.
15	A valid interrupt condition is set for the command channel to test the flag, control, and interrupt logic of that channel.
	REWIND LOAD POINT TESTS (NOTE 1)
16	A Rewind command is issued to the controller and status is taken to assure that the controller returns a rewind and tape unit busy status.

Table 3. Test Descriptions (Continued)

TEST NUMBER	DESCRIPTION
	REWIND LOAD POINT TESTS (NOTE 1) (Continued)
17	At the end of rewind (test 16), the status is taken to assure that the load point has been sensed.
18	The reject status is tested at load point by issuing a Backspace Record command. Status is then taken to assure that the reject bit has been set.
19	The minimum rewind reset time is tested by issuing a Rewind command at load point. A delay period is waited before taking status and checking the controller busy bit.
20	The maximum rewind reset time is tested by waiting another short delay period after test 19 to assure that the controller busy status has been cleared.
21	The generation of a valid identification burst is tested by writing a two-byte record of all "1's" from load point. The tape is then rewound to load point and a Read command is given to read the two-byte record. The record is then compared to assure that only the two bytes that were written were read back.
22	The Backspace Record command is tested by backspacing the two-byte record previously written in test 21. Status is then taken to assure that only the record was backspaced.
	INITIAL WRITE/READ TESTS
23	A 32-byte record of all "0's" is written with all "1's" in the parity channel. The status is taken to assure that there were no data or single track errors.
24	The 32-byte record previously written in test 23 is read back to check for data errors.
25	A 200-byte record simultaing 1600 flux-reversal-per-inch data is written and checked for data errors.
26	The 200-byte record previously written in test 25 is read back and checked for errors.
	STATUS AND TIMING TESTS
27	The select reject status is tested by issuing a Select command to the controller while the controller and tape drive are backspacing a record.
28	The motion reject status is checked by issuing a backspace record to the controller while the controller and tape drive are reading a record forward.
29	The data timing error status is forced and checked by not transferring data from the controller to the computer during the read operation in test 28.
30	The odd byte status is tested during a read of the last single record file which was generated for the record and file spacing test. A normal read is started, and after the first word has been transferred to the computer, a delay time period is started. At the end of the delay period, a dynamic status is taken on the controller to check for the odd byte status during the second byte period of the next word.

Table 3. Test Descriptions (Continued)

TEST NUMBER	DESCRIPTION
	STATUS AND TIMING TESTS (Continued)
31	The status is taken to check for a data error status which was forced during test 30.
32	Two file marks are backspaced over and status is taken. The status is analyzed to see that the file mark bit has been set.
	RECORD AND FILE SPACING TESTS
33	The backspace file test is done during test 32.
34	The forward space file operation is checked by forward spacing over the first file mark and taking status to be sure that the file mark has been sensed. Then the first record of that file is read to verify that the record is in the particular file that was spaced into.
35	The record that was just read is backspaced and status is taken to assure that just that record had been backspaced.
36	The record previously backspaced in test 35 is forward spaced over. Then the file mark at the end of that record is forward spaced over and status is taken to verify that the file mark was detected and that the record was forward spaced.
37	The clear time during a backspace operation is tested by starting a backspace on a record previously written. A Clear command is issued and a delay time period started. After the delay period has been completed, the status is taken to check that the controller is still busy. Then, after another short delay, the status is taken again to ensure that the busy bit has been cleared by this time.
38	The 3-inch gap is tested by starting to write a gap and file mark and starting a delay time period. After the first delay period has been timed, status is taken to see that the controller is still busy with the Gap command. After the second short delay period, status is again taken to verify that the controller is not busy and that the file mark has been written.
39	The interrecord gap is tested by writing two, two-byte records, then backspacing over these records. The records are then read, and the flag from the first record starts a delay period. After the delay period, the flag is checked again to see that it has not been set by the second record.
40	The interrecord gap creep time test is tested similar to test 39, except that the second record is rewritten ten times to verify that the rewrites do not cause the gap to creep back and thus shorten the interrecord gap.
	DATA TRANSFER TESTS
41 thru 61	These tests are write/read operations that transfer a single track rotating bit pattern using DMA. Varying lengths of records (seven) starting with 16 bytes and ending with 1024 bytes are transferred. The record is written and checked for errors and then is reread twice to assure that there are no data errors and that no single-track errors have been caused by the tape drive (other than normal tape errors). Tests 41, 44, 47, 50, 53, 56, and 59 are write tests; the others are read tests.

Table 3. Test Descriptions (Continued)

TEST NUMBER	DESCRIPTION
	DATA TRANSFER TESTS (Continued)
62 thru 82	These are the same write/read tests as 41 thru 61 except the data is in a channel sawtooth pattern, DMA transfer only. Tests 62, 65, 68, 71, 74, 77, and 80 are write tests; the others are read tests.
83 thru 103	These are the same write/read tests as 41 thru 61 except the pattern is a track sawtooth. Tests 83, 86, 89, 92, 95, 98, and 101 are write tests; the others are read tests.
104 thru 124	These are the same write/read tests as 41 thru 61 except a random data pattern is transferred. Tests 104, 107, 110, 113, 116, 119, and 122 are write tests; the others are read tests.
200 (Note 2)	The write-enable ring is removed by the operator, after which a Write command is given to the controller. The status is taken and checked for the presence of the file protect and command reject bits.

NOTES:

1. Switch 7 set inhibits test 16 thru 22.
2. This test is enabled or inhibited by the switch register.

Table 4. Program Halts

T-REGISTER INDICATION	HALT
102000	Initialization halt number 1.
102001	Initialization halt number 2.
102010	Rewind/off-line halt.
102011	Select halt, selected tape unit not on-line.
102055	Error halt.
102056	File protect test halt.
102076	Normal halt after current test.
102077	Normal halt after complete program cycle.

11. Errors detected during write operations provide one of the following two messages preceding the cycle and test number:

REWRITE REQUIRED or nn REWRITE

REWRITE REQUIRED indicates that the record was written and a data error was detected during a read-after-write operation, and the record then was backspaced and rewritten with no data errors. The printout nn REWRITE indicates that a normal rewrite was attempted and data errors occurred a second time. The tape was then backspaced, gapped, and rewritten, all "nn" times. For example, the printout 10 REWRITES occurs during write operations only, and indicates that read after write parity errors, caused by faulty write-read circuits, were detected. Ten rewrites of the record had been attempted without success and the program halted with a T-register indication of 102055 (computer switch 11 was not set).

12. When the auto select mode is being used, all the error messages are preceded by the unit number as follows:

```
UNIT NO. Ø
4 TEST # 18
STATUS WAS LP,
AND IT SHOULD BE CR, LP,
```

13. Errors detected during read operations provide additional information with the error messages previously described above. Line 4 provides the word number of the word in error and the record length in words. Lines 5 and 6 provide the word that was in error followed by the good word or the word that should have been in the record.

```
5 TEST # 24
STATUS WAS DE, OB,
AND IT SHOULD BE CLEAR
WORD # 5 OF A 16 WORD RECORD
WORD IN ERROR IS  1000  0000  0000  0001
AND IT SHOULD BE  0000  0000  0000  0000
```

14. Also, in a read operation if a single track error has been detected and corrected by the tape unit, the following message appears before the test number:

SINGLE TRACK ERROR DETECTED

15. After the first eight tests are completed and during the first cycle of the diagnostic program, the following message is printed:

PUT TAPE UNIT(S) ON LINE

This message is also printed each time the rewind off-line test option is select with switch 9.

16. The message

SELT'D T.U. OFF LINE

indicates that the tape unit selected was off-line or, in the case of auto select, all the tape units were off-line or busy.

17. The message

E.O.T.
n CYCLES

indicates that an end-of-tape marker was detected during the nth cycle of the diagnostic program. The tape was rewound to load point, and the program continued running.

18. The message

CMND REJTD
6 TEST # n

indicates that during test number "n" a command was issued to the controller and was rejected because the controller was still busy with the previous operation. This is also an indication that test number "n-1" may be in error.

19. PROGRAM ORGANIZATION.

20. MAIN DIAGNOSTIC.

21. The program is first initialized for the I/O configuration of the system being tested. The program then runs the series of tests that constitute the main diagnostic. All tests in the program sequence have ascending stop numbers. The program can be run in two modes, auto-select and switch-register control (manual).

22. Unless an error is detected, the program makes one complete diagnostic test, then recycles. However, if an error is detected, an error message is printed out along with the associated test number. The program then continues with the rest of the test unless the error would cause a sequence error in the complete diagnostic test. In this case, the program is restarted automatically.

23. After a complete sequence of tests, the diagnostic program will recycle and continue until the program is halted by switch-register control or by pressing the computer HALT pushbutton. When halted under switch register control, the program will print out the number of diagnostic cycles completed. If the diagnostic detects an end-of-tape condition, the program will automatically rewind the tape and restart the diagnostic at the load point.

24. The program can also be halted after an error has been detected and recorded. Most tests can be halted when finished and the test (or short sequence of tests) inserted into a loop through the use of another control switch. (Some tests cannot be looped due to program restrictions.) When the program is stopped after a current test, either by error halt or switch control, the test number is displayed in the B-register, with the A-register containing controller and tape unit status.

25. Selection of tape units can be done by switch-register settings or by an auto-select mode. In auto-select, although any number of tape units up to four may be on-line, the program will begin with unit 0 and select the first one found to be on-line. If all units are off-line or busy, the program will try the select sequence twice before printing out SELT'D T.U. OFF-LINE. In the switch-register control mode, only the unit specified will be selected.

26. OPERATOR SERVICE ROUTINES.

27. Two separate operator service routines of the diagnostic allow the operator to perform certain checkout procedures and unit operations. The two routines are the DMA transfer test (DMATR) and the command exercise test (CE).

28. DMA TRANSFER TEST. The DMATR test has a starting address of 500 and is used as an extended method for checking the DMA transfer mode of the interface. Switches 0 through 7 determine the bit pattern of the bytes to be written.

29. The program writes a 2048-byte record, then backspaces and reads the record twice. Each time, the switch register byte is compared with each byte read into the core buffer. If data errors occur, the program halts with 102055 in the T-register and the word in error in the A-register. No status is taken during the write or read operation.

30. Setting switch 15 brings the program to a normal halt with the T-register indicating 102076. Leaving switch 15 cleared allows the program to continue transferring records until an end-of-tape condition is detected, at which time the tape automatically rewinds.

31. COMMAND EXERCISE TEST. The CE test starts at address 1100 and outputs individual commands to the controller and tape unit. Any of the first six commands in table 2 can be combined with any of the last six, or with any single command. The routine has the option of using the flags for termination of operations or as a timer. In the timer operations, three fixed time periods are available. These are approximately 10 milliseconds, 15 milliseconds, and 30 milliseconds. Normal termination of operations in this routine is achieved by setting switch 15.

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7970/13183
MAGNETIC TAPE DIAGNOSTIC

UPDATING SUPPLEMENT FOR DIAGNOSTIC PROGRAM PROCEDURES

22 JANUARY 1973

MANUAL IDENTIFICATION

Manual Part Number: 13183-90002

Manual Printed: April 1972

SUPPLEMENT DESCRIPTION

The purpose of this supplement is to adapt the manual to revised diagnostics and to correct manual errors. Enter the new information (or the change number, if more convenient) into the appropriate places in the manual identified at left.

DIAGNOSTIC PART NO.	REVISION	CHANGES
13031-60001	B	1 thru 5
13031-60001	C	1 thru 9

Changes 1 thru 5 dated 17 July 1972.

Changes 6 thru 9 dated 15 Sept. 1972.

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CHANGE

DESCRIPTION

1 Page 2, table 1.

a. Change the entry for switch 10:

STATE, SET; FUNCTION, INHIBITS ERROR MESSAGES.

2 Page 2, table 2. Add the following:

DATA TRANSFER TEST (STARTING ADDRESS = 001000_8)		
SWITCH	**STATE**	**FUNCTION**
0-7	---	Defines the tape byte that is written, depending on the state of the switch; set = 1, reset = 0.
8*	Set	Fixed length record of 2 bytes.
9*	Set	Fixed length record of 4 bytes.
10*	Set	Fixed length record of 8 bytes.
11*	Set	Fixed length record of 16 bytes.
13*	Set	Fixed length record of 32 bytes.
14*	Set	Fixed length record of 64 bytes.
8-14	Cleared	Infinite length record.
15	Set	Terminates infinite length record normally then halts and halts after current fixed length record.
*Any combinations of switches 8-14 may be set resulting in different lengths than stated above. The length is determined by the sum of the BCD weights (SW 8 = 1, SW 9 = 2, SW 10 = 4,...SW 14 = 32) multiplied by 2.		

3 Page 3, paragraph 10. Change the mnemonic entries as follows:

TM to TE; FM to TM

4 Page 5, table 3.

a. Change the description of test no. 21 as follows: The generation of a valid ID burst is tested by writing a tape mark from load point. The tape is then rewound to load point and a Forward Space File command is given to space over the tape mark. The status is checked to assure that only the file mark status is present.

b. Change the description for test no. 22 as follows: The Backspace Record command is tested by backspacing the tape mark previously written in test 21. Status is then taken to assure that only the tape mark was backspaced.

CHANGE	DESCRIPTION
5	Page 6, table 3. Change the first sentence of the description for test no. 39 as follows: The interrecord gap is tested by writing two, two-byte records and a file mark, then backspacing over these records.
6	Page 2, table 1. Add the following note for switch 9: Unavoidable on first cycle, unless tape drive is off-line.
7	Page 3, paragraph 10. Insert the following as the second-to-last sentence: The expected status may or may not differ from actual status, depending on test.
8	Page 7, paragraph 11. Insert the following after the third sentence: When starting the diagnostic from location 100, or restarting it from location 2000, REWRITE REQUIRED will frequently be printed. The message should be ignored at least once; it is caused by old data on the tape.
9	Page 8, paragraph 30. Insert the following after the first sentence: The diagnostic program can be restarted if all register contents are preserved.