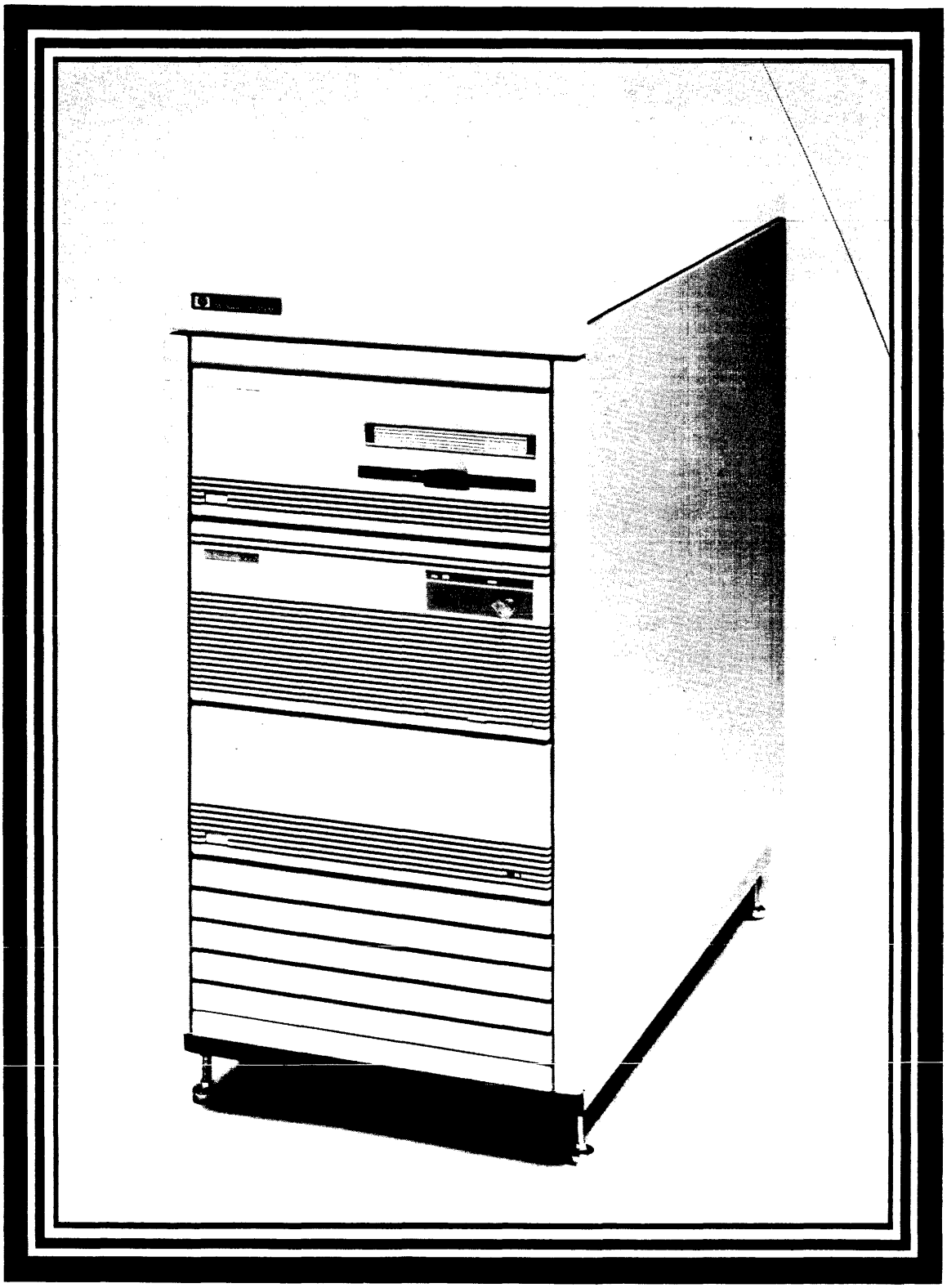
HP 3000 Computer Systems

Series 37
System Processing Unit

Self-Paced Hardware Training Guide



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June, 1984

Computer Support Division
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Printing History

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The dates on the title page change only when a new edition or a new update is published. No information is incorporated into a reprinting unless it appears as a prior update; the edition does not change when an update is incorporated.

The software code printed alongside the date indicates the version level of the software product at the time the manual or update was issued. Many product updates and fixes do not require manual changes and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one to one correspondence between product updates and manual updates.

First Edition..... June 1984

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Introduction

The HP 3000 Series 37 System Processor Unit (SPU) is a low-end member of the HP 3000 product line. The simple and highly integrated design allows product training for the CEs to be accomplished with a self-paced course.

The self-paced course is designed to be a self-contained two-day course. It requires only a supported terminal and the Series 37 SPU. On the third day, a TSE gives a lecture. The third day exercises include questions and answers from the contents of the two-day course. It also includes a discussion of MPE and DUS changes and some lab time to become familiar with the entire system.

PREREQUISITES

Despite its simple design, the Series 37 is a highly complex computer system that requires training beyond that which is possible in a self-study course. The CE 232A course or equivalent experience and six months of field experience are prerequisites of the self-study course. It contains necessary background information, such as HP-IB configurations, basic MPE, and the Diagnostic Utility System (DUS). The Series 37 course covers only the hardware that is unique to the Series 37 SPU.

COURSE OBJECTIVES

When you have successfully completed this course, you will be able to:

- Operate the Series 37 SPU and identify its unique features
- Configure and install a Series 37 SPU in the mini-rack
- Troubleshoot and repair the Series 37 SPU
- Remove and replace all field replaceable assemblies
- Describe the unique features of the Series 37 Synchronous Intermodule Bus (SIMB)
- Identify the components of the Remote Operators Interface (ROI)

MATERIALS NEEDED TO TAKE THIS COURSE

The self-paced program requires that you have the following materials, tools, and equipment (part numbers in parenthesis).

Self-Paced Hardware Training Package

- This HP Series 37 Self-Paced Hardware Training Guide (32450+49A-90001)
- Final Review Package. (You should give this to your supervisor or administrator before beginning the course). (32450+49A-90003)

Tools and Equipment

- Series 37 SPU
- Terminal
- Optional mini-rack cabinet (30463A)
- One of the following disc drives:
    - HP 7945
    - HP 7912/14
    - HP 7933
    - HP 7935
- One of the following tape drives:
    - HP 9144
    - HP 7974

The following extra boards should be available for running diagnostics:

- Peripheral Interface Controller (PIC) (30459A)
- Terminal Interface Controller (TIC) (30460A)
- Series 37 Board Extractor Tool (30457-80004)
- Load Board (30457-60015)
- Video Cartridge Recorder
- Video cartridge of SPU and Extender installation in Raven cabinet
- Diagnostic Utility System (DUS) on magnetic tape reel or cartridge tape- most current version

- MPE on magnetic tape reel or cartridge tape - most current version
- Modem Loopback Connector (30146-60002)
- RS-232-C Loopback Connector (30148-60002)
- Standard 2-meter HP-IB cable
- Hardwired 25 pin-to-3 pin cable (ATP type) (31052-60001)
- Standard terminal modem cable (part number is terminal-dependent)
- Standard hand tools, to include numbers 0, 1, and 2 Posidriv screwdrivers
- Volt-ohmmeter (HP 3465/3466 or equivalent)
- Antistatic Wrist Strap

Documentation

HP 3000 Diagnostic Manual Set (30070-60080) - most current version

HOW TO USE THIS GUIDE

This self-paced guide contains all of the instruction for this course. It directs you to read the text, to perform lab projects, and to answer questions that test your understanding of the material.

Follow these guidelines for taking this course and using this guide:

- Give the sealed Final Review Package to your supervisor or administrator.
- Study the lessons in sequence.
- Read and observe all warnings and cautions before performing the defined procedures.
- Within each lesson, work through the lesson in the order that the material is presented. Read the introductory material, then perform the lab project and answer the quiz questions. (Lab and quiz answers are included in Appendix C.) If you correctly answer at least 80% of each quiz, proceed to the next lesson. If your score is less than 80%, review the lesson and then answer the questions again.
- After completing the course, answer the questions in the Final Review examination (which you should get from your supervisor or administrator). If your score is less than 80, review the lessons in which you are weakest and then answer the Final Review questions again.
- Keep track of your progress on the Course Completion Summary.

NOTE

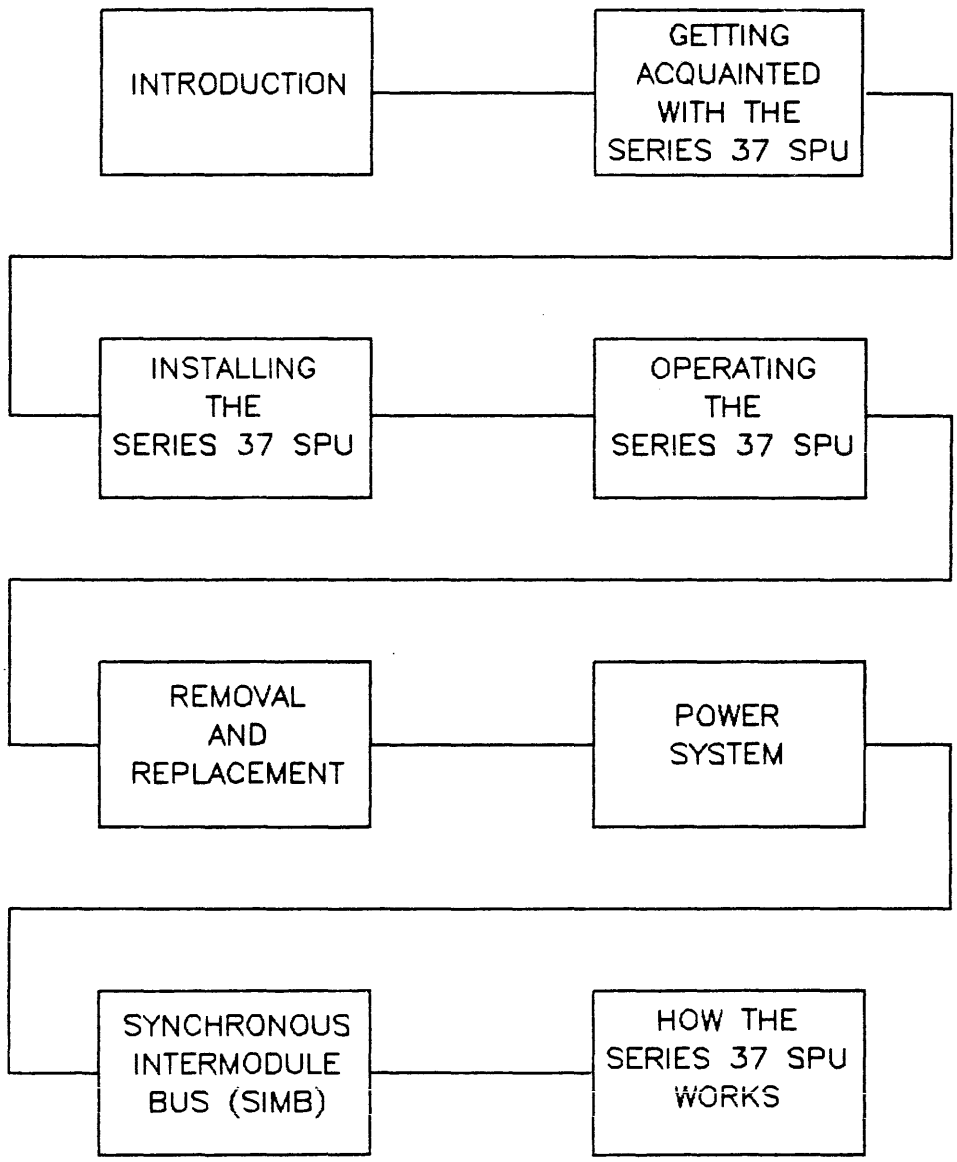
This guide is intended for use by qualified service personnel only. Normal safety precautions must be observed at all times while servicing electronic equipment.

Course Structure

The sequence below explains the plan of this self-paced guide. The elements of the flowchart are the major points to be covered to repair the Series 37 SPU to the module/component level. This guide does not intend to develop good electronic technicians. It is designed to teach a good technician to repair the Series 37 SPU to the module/component level.

WARNING

Always remove power before opening the Series 37 SPU. If servicing requires that the power be on while protective covers are removed, proceed only with extreme caution. Failure to do so can result in severe injury.



Course Completion Checklist

HP 3000 Computer Systems
Series 37 System Processing Unit
Self-Paced Hardware Training Guide

Lesson Title	Date Completed	Time Required	Supervisor's Initials
1. Getting Acquainted With the Series 37 SPU	_____	_____	_____
2. Installation	_____	_____	_____
3. Operating the Series 37 SPU	_____	_____	_____
4. Removal and Replacement	_____	_____	_____
5. Power System	_____	_____	_____
6. Synchronous Intermodule Bus (SIMB)	_____	_____	_____
7. How the Series 37 SPU Works	_____	_____	_____

Program Completion Date _____

Student's Signature _____

Company Name _____

Address _____

_____

_____

Final Review Administered By: _____ Date: _____

If your organization is interested in an HP co-operative support program, complete this form and attach your completed final review package. Contact your local HP sales representative for further information.

Getting Acquainted With The Series 37 SPU

Lesson 1

OVERVIEW

This lesson briefly describes the characteristics of the Series 37 SPU and its position in the HP 3000 product line.

LEARNING OBJECTIVES

When you have successfully completed this course, you will be able to:

- Describe the basic configuration of the standard system.
- List the maximum number of users that can be supported.
- Identify the configuration restrictions that apply to the I/O Extender.

INTRODUCTION

The HP 3000 Series 37 is a new low-end member of the HP 3000 product line. It is a highly integrated, low priced, high-reliability computer that runs MPE. It offers customers a low priced system that can be upgraded to the top of the product line.

Figure 1-1 is a simplified block diagram of the Series 37 System Processing Unit (SPU). The SPU uses gate array and CMOS VLSI technology extensively to achieve its small size. The Series 37 supports from one to 28 users and up to one megabyte of main memory with the performance of a Series III. The standard Series 37 supports seven users with 512k of main memory and a Peripheral Interface Controller (PIC). The one remaining slot can contain an additional Terminal Interface Controller (TIC), another PIC, or an additional 512k of memory. The system can be extended to 10 slots by adding an I/O Extender. The I/O Extender is physically connected to the Series 37 SPU and can be populated with additional I/O boards. Note that memory is not supported in the Extender.

The Series 37 SPU consists of a five-slot card cage, a power supply, and battery backup circuitry. The boards that make up the SPU are installed in the following slots:

Slot 5 Central Processing Unit (CPU) *

Slot 4 Peripheral Interface Controller (PIC) **

Slot 3 Optional 512k Memory, TIC, or PIC ***

Slot 2 512k Memory *

Slot 1 Terminal Interface Controller (TIC) *

* Must be installed in this slot

** Must be installed here if there is no I/O Extender. If there is an I/O Extender in the system, a PIC or a TIC can be installed, or the slot can be blank.

*** This slot can be blank

The Series 37 is small enough to set on a desk top. It can also be racked in a mini-rack with other supported peripherals. The Series 37 is designed to be installed by the customer. At first introduction, it will be installed only by HP personnel. Customer installation will be implemented when there are peripherals available that can be installed by the customer.

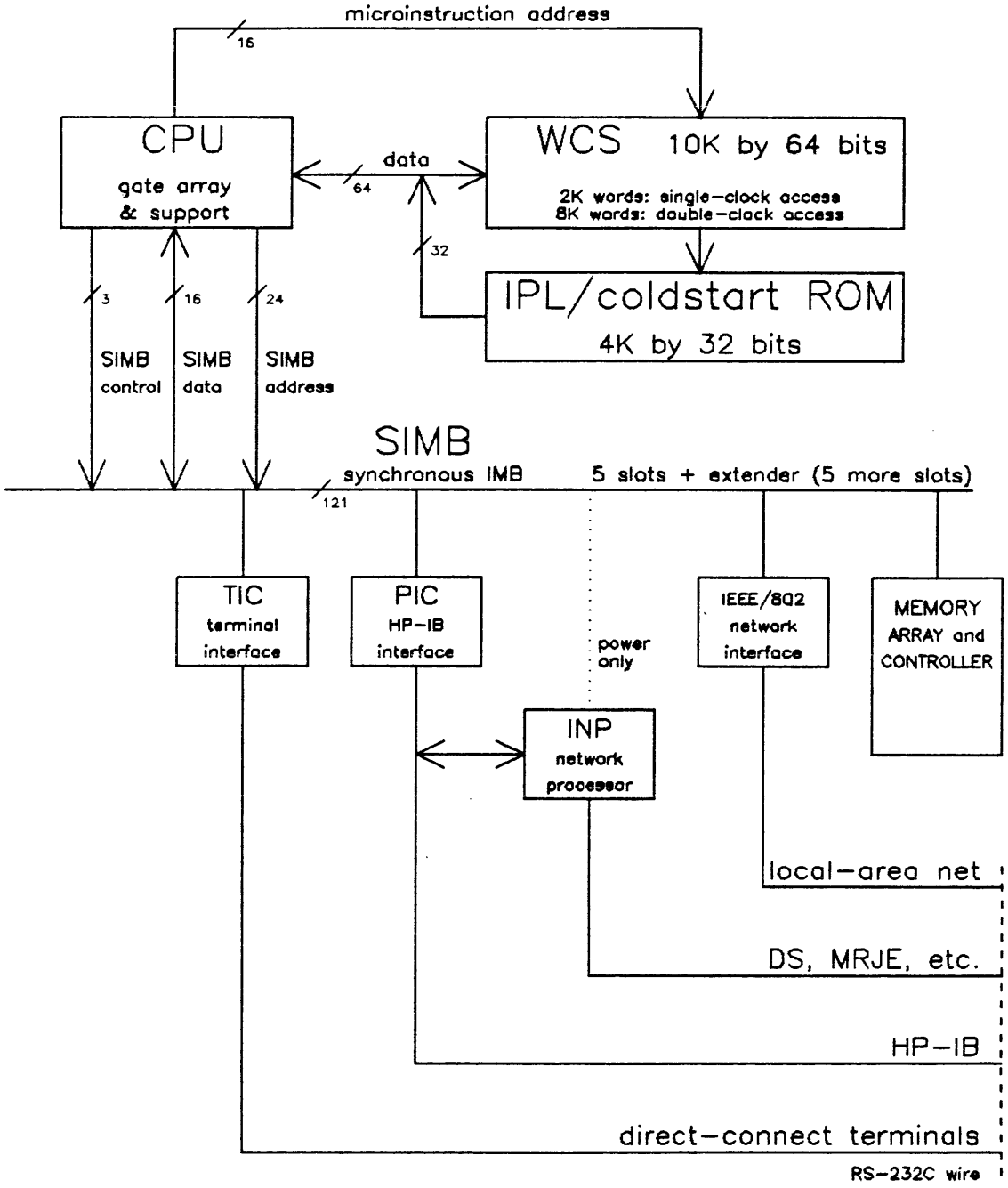


Figure 1-1. Series 37 SPU Simplified Block Diagram

LESSON 1 QUIZ

1. How many optional slots are there in the standard system? 1
2. What is the maximum number of users that can be supported? 28
3. Can you install memory in the I/O Extender? NO

Installing the Series 37 SPU

Lesson 2

OVERVIEW

This lesson describes the HP 32449A installation policy. It also describes how to install the HP 32450A and the I/O Extender. The rules for configuring the Series 37 SPU card cage are also provided.

LEARNING OBJECTIVES

When you have successfully completed this lesson, you will be able to:

- Install the HP 32450A.
- Connect the I/O Extender to the HP 32450A.
- Correctly cable the system.
- Configure the SPU and I/O Extender card cages.

INTRODUCTION

The Series 37 SPU is the first customer-installable HP 3000. There are two versions of the product. The HP 32450A is CE installable. The HP 32449A is customer installable.

The HP 32449A is an integrated version of the Series 37. It is shipped installed in the mini-rack. It is bundled with the HP 9144A cartridge tape drive and a customer-installable disc drive. The shipment of the tape and disc is coordinated with the shipment of the customer-installable system. The mini-rack is shipped already set up to accomodate these peripherals and a second optional disc drive. No other HP-IB peripherals are supported on the HP 32449A unless they are installed by a CE and unless site preparation has been performed. All other supported peripherals on the system, such as terminals, printers, and plotters, have RS-232 interfaces and are customer installable. Note that the I/O Extender and a second PIC are not supported in the customer-installable configuration.

HP 32449A INSTALLATION POLICY

There are several reasons why the HP 32449A product is customer installable. The major reasons are described below.

Installation Procedure

Installation of the HP 32449A and the peripherals that are customer installable does not require special tools, adjustments, or alignments. The peripherals are lightweight, low-power devices that require no special wiring.

Single Power Source

The Series 37 SPU and the customer installable HP-IB peripherals are low-power devices. This allows them to be connected to a single AC power source by means of the power strip in the mini-rack. Because of the single power source, the Series 37 SPU can run on normal office AC power without requiring special wiring or line conditioning. The single power source also eliminates the possibility of transmission errors caused by a ground loop between HP-IB devices.

All of this reduces the need for site preparation. However, sites that do not have normal office environments or those with unstable power may require site preparation, line conditioning, or special AC wiring. The Series 37 SPU should be installed on a dedicated circuit free from copiers, microwave ovens, and heavy motors.

RS-232 Peripherals

Because of the nature and speed of an RS-232 interface, the peripherals do not have to be on the same AC circuit, as do HP-IB peripherals. This eliminates the need for site preparation of these peripherals, as long as they are low-power devices.

External HP-IB Peripherals

No customer-installable external peripherals are supported on the Series 37. In general, these peripherals are higher powered devices that require additional AC circuits. Because of the current draw and the need for multiple AC circuits, site preparation must be performed to ensure long-term reliability.

INSTALLING THE HP 32450A AND THE I/O EXTENDER

The procedure for connecting the I/O Extender to the HP 32450A and the procedure for installing components in the mini-rack are shown on the video tape. The following paragraphs complete the procedure for system installation by providing the external cabling and the AC power specifications.

Serial Port Cabling

Refer to Appendix B for the list of supported RS-232 cables. The specifications for the RS-232 are listed at the end of the discussion of the TIC in the "How the Series 37 SPU Works" lesson.

HP-IB Cabling

The standard Series 37 configuration includes one PIC PCA. It can support from one through eight devices. For performance reasons, eight devices are seldom installed on one channel. Seven PIC PCAs could be installed on one system with an I/O Extender. However, this is not practical because there would be no room for additional memory, TICs, or Intelligent Network Processors (INP).

A typical system contains two or three PICs. The design of the PIC is similar to the General Interface Controller (GIC) in that seven device loads are built on the PCA. The HP-IB specifications state that one meter of cable can be added for each device load. This implies that a maximum of seven meters of cable can initially be added . This is not true because some devices have internal cables whose length must be included. It is best to use only the cable that is shipped with each device. You will then remain well within the specifications. If additional cable is required, it can be added, provided you do not exceed one meter per device load. Note that each PIC has its own HP-IB interface and is completely separate from other PICs. The rule of seven device loads per PIC applies to each installed PIC PCA.

When adding additional cable, do not connect two HP-IB cables together. For example, if you need a two-meter cable between two devices, use one two-meter cable. Do not connect two one-meter cables.

A "star" configuration, a "daisy chain" configuration, or a combination of the two can be configured on any PIC. Any combination is supported as long as the cable length specification is not exceeded. The "daisy chain" is the preferred configuration because it produces less noise.

If both a disc and a printer are on the same HP-IB interface, connect the disc closer to the SPU than the printer.

AC Power

The input electrical specifications of the Series 37 SPU or the I/O Extender are shown below. If an SPU and I/O Extender are installed in one system, both the current and power requirements specified below are doubled.

VOLTAGE	Single phase Nominal operating range: 100-120Vac or 220-240Vac Maximum operating range: 85-135Vac or 170-270Vac
CURRENT	4 amps maximum at 110Vac
POWER	270 watts maximum at maximum output load
FREQUENCY	45 to 66 Hz.
HOLD-UP	One cycle of input AC can be dropped without causing a Power Fail condition.
POWER LINE DISTURBANCE	The computer will perform correctly in normal and common modes under the following pulse conditions:

Volts	1000 V (peak)	1000 V (peak)
Width	10 usec	100 nsec
Rise	1.5 usec	100 nsec
Fall	1.5 usec	100 nsec

RULES FOR CONFIGURING THE SERIES 37 CARD CAGE

The card cage configuration guidelines are listed below.

- The CPU PCA must be installed in slot 5 of the SPU.
- The first TIC PCA must be installed in slot 1 of the SPU with an RS-232 connector assembly.
- The first 512k byte memory PCA must be installed in slot 2 of the SPU. If a second memory PCA is installed, it must be installed in slot 3.
- No memory can be installed in the I/O Extender.
- A maximum of four TIC PCAs can be installed in the system.
- There must be at least one slot between TICs or any other assembly that has a connector on the right side.
- A TIC cannot be installed in slot 5 of either the SPU or the I/O Extender.

LESSON 2 QUIZ

1. What AC power feature allows the HP 32449A system to be installed without site preparation?
   Low power
2. Is it possible to install three TIC assemblies in the I/O Extender? Explain your answer.
   NO NOT ENOUGH Slots
3. What is the preferred HP-IB cabling configuration?
   DAISY CHAIN
4. What is the general rule for installing HP-IB cables that will ensure that you do not violate the maximum cable length specifications? 1 meter per Device LOAD only use CABLE Shipped w/ System
5. What are the primary factors that make site preparation for the HP 32450A mandatory?
   1. per. NOT PART OF BASIC 37
   2. ABNORMAL ENVIRONMENT

Answers in Appendix C.

Operating the Series 37 SPU

Lesson 3

OVERVIEW

This lesson describes the operation of the console, the function of the keyswitch, and the function of the front panel LEDs. The Remote Operators Interface and the maintenance microcode are also described.

LEARNING OBJECTIVES

When you have successfully completed this lesson, you will be able to:

- Operate the Front Panel Keyswitch.
- Connect and operate the local and remote consoles.
- Execute and interpret Self Test results.
- Troubleshoot the SPU using the Display Indicator.
- Identify the hardware configuration using available tools.

SPU FRONT PANEL DESCRIPTION

The System Processor Unit (SPU) front panel is shown in figure 3-1. The four-position key switch is used to select the control modes and power distribution of the SPU. The indicator lights show what power configuration is active and in what mode the system is running. The single digit LED display shows the status of the SPU when the self-test routines are executed. The display remains blank when the system is executing operational software.

Front Panel Key Switch

The front panel key switch is used to select the power configuration and the mode of operation of the SPU. You can select either the normal mode or the maintenance mode of operation. Table 3-1 shows the key switch positions, the modes of operation, and the associated actions.

Front Panel Status Indicators

The front panel status indicators display the state of the SPU during operation.

The AC indicator is lit if AC power is applied to the SPU. Power is applied to the battery charger. The indicator is lit in all keyswitch positions.

The DC indicator is lit if DC power is present in the SPU. It is lit if the key switch is in positions 1, 2, or 3.

The BATTERY indicator is lit if the SPU is operating on battery backup power and if AC power is not present. This condition can occur if the front panel switch is in positions 1, 2, or 3.

The RUN indicator is lit only when the Channel Program Service Request (CSRQ) signal is asserted. It is not lit if TIC or memory operations are being executed. During normal operation, it will appear to be lit continuously because channel programs are executed frequently. The indicator will flicker when TIC or memory diagnostics are run. It can be lit when the key switch is in positions 1, 2, or 3.

The REMOTE indicator is lit if the key switch is in position 3. This allows a terminal connected to port 7 via a modem to control the system.

Front Panel LED

The front panel LED displays a single hexadecimal error code that indicates what components are failing. The codes are displayed only when the system is in the self-test mode. There are two test modes. Self-test is run first. The normal sequence of displayed LED codes is 0, 1, 5, 1, 5, B, C, A. Self-test is then complete. If an error is detected, the error detection loop is executed.

The valid hexadecimal codes and their meaning are shown in table 3-2. The LEDs display one digit at a time. If a two-digit error code is displayed, the digits of the code flash alternately. If no error code is displayed, the SPU is executing operational software.

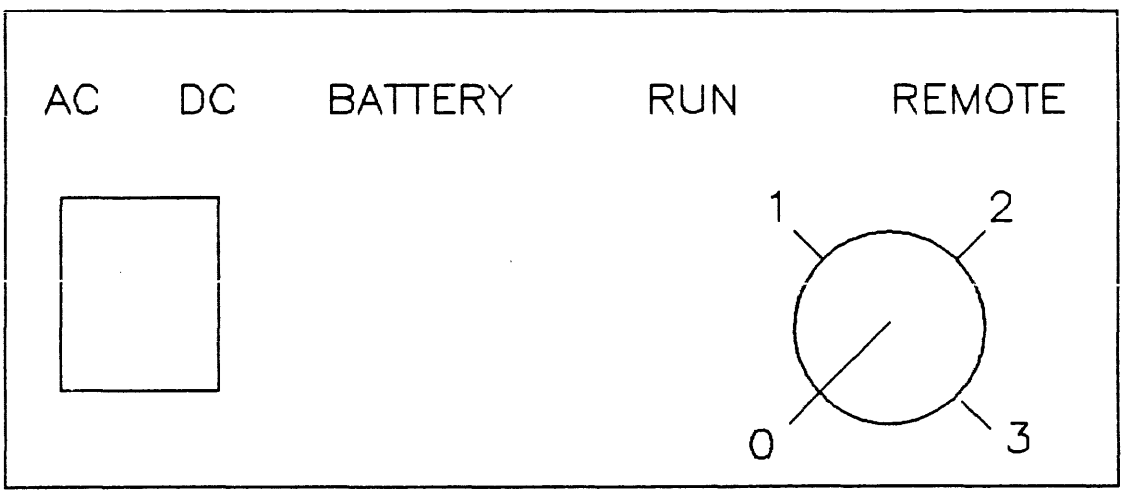


Figure 3-1. SPU Front Panel

Table 3-1. Key Switch Definitions

KEY SWITCH POSITION	MODE	ASSOCIATED ACTION
0	DC Off	DC power is off. Battery DC is off. AC power is applied. Power is applied to the battery charger.
1	Normal	The system console is on port 0, channel 1. Control B (maintenance mode) sequences can not be executed in this mode.
2	Local	The system console on channel 1, port 0 is active and can execute the Control B sequence.
3	Remote	The terminal on channel 1, remote port (port 7) is the active console and can execute the Control B sequence. The local console on port 0 monitors and displays remote console data transfers.

Table 3-2. Front Panel LED Codes and Descriptions

LED CODE	DESCRIPTION
0	~~ROM code loads into WCS.~~
1	Not used. LOAD Rom code into WCS
2	Not used. Vertical Checking Failed
5	Processor chip, WCS, RFILE tests executing. 5→1→5 means more code loading more tests Run
0	Maintenance code entered. Multi-bit memory error occurred.
B	A steady "B" means the memory test is executing. A flashing "B" means the memory failed the test.
C	A steady "C" means the Console TIC in slot 1 is being tested. A flashing "C" followed by a "1" means the Console TIC failed. If only a flashing "C" occurs, speed sensing of the terminal failed.
D	IOMAP NOT Run on PON
E	These error codes show that the TIC or PIC in the indicated extender slot has failed. The "E" and the slot number flash alternately.
A	All tests passed.
Blank	DUS or MPE is being loaded or had been loaded.

5, A, B, C FAIL Diag will Loop

I/O EXTENDER DESCRIPTION

The standard Series 37 SPU has a five-slot backplane, in which the four standard boards are installed (CPU, PIC, TIC, and memory). One slot remains available for either memory or I/O expansion. The I/O extender increases the total number of slots from five to ten. The five additional slots can be used only for I/O expansion. Memory is supported only in slots 2 and 3 of the SPU.

Comparison of Extender to SPU

The Extender is identical to the SPU, with the following exceptions:

- The CPU board and Memory board cannot be installed in the Extender.
- There is no keyswitch on the Extender. Power is controlled from the SPU by means of the interconnect cable.
- There are no RUN or REMOTE indicators on the front panel of the Extender.
- There are minor hardware differences in the card cages to allow them to be connected together.

The backplanes, power supplies, battery packs, and rear panels are identical. Both the SPU and Extender backplane slots are numbered from 1 through 5.

Battery Backup

The battery backup system is identical to that in the Series 37 SPU. However, it is used to save the contents of critical RAMs on I/O boards rather than save the contents of main memory.

I/O Extender Service Note

WARNING

Always turn off DC power first. Then remove AC power before servicing the Series 37.

DC power in the Extender is controlled by the keyswitch on the SPU. The SPU and the Extender are connected via the flat interconnect cable. If DC power is turned off and the interconnect cable is removed, DC power in the Extender will be turned on if the AC power has not been removed. This will also happen if the Display Board cable in the SPU is removed. Under these circumstances, if AC power is later removed, the battery backup will be turned on, keeping the memory voltages up.

Because of power supply loading requirements, the Extender is not supported without at least one I/O board being installed. If the Extender is unpopulated, it is not guaranteed that DC power will come up.

EXTENDER FRONT PANEL DESCRIPTION

The Extender front panel is shown in figure 3-2. The Extender front panel status indicators are a subset of the SPU status indicators.

The AC indicator is lit if AC power is applied to the Extender. The DC indicator is lit if DC power is present in the Extender.

The BATTERY indicator is lit if the Extender is operating on battery backup power and if AC power is not present.

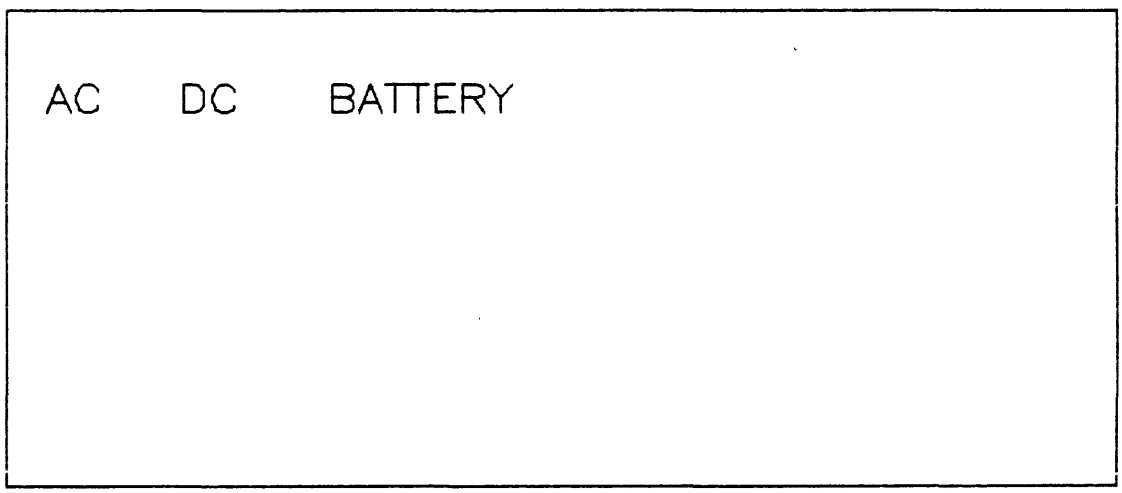


Figure 3-2. Extender Front Panel

MINIMUM REQUIREMENTS FOR TERMINALS

Refer to Appendix B for the list of HP terminals that are supported on the Series 37 system. Non-HP terminals can also be used if they are compatible with the HP terminals. Some of the minimum requirements are listed below.

- The system console must be connected to port 0 on the TIC installed in slot 1 (channel 1) of the SPU. MPE and DUS expect this configuration.
- The ENQ/ACK handshake capability must be present.
- The console must operate at one or more of the following standard baud rates: 110, 300, 600, 1200, 2400, 4800, 9600, 19200.
- The console must have either 8N1 (eight data bits, no parity, one stop bit) or 701 (seven data bits, no parity, one stop bit, and the eighth bit set to zero).
- 80 character input buffer
- Full duplex
- It must be capable of issuing a Control B sequence and other supported sequences.
- It must be capable of accepting a DC1 as a line turn-around character.

Connecting Hardwired Terminal to Series 37

Refer to Appendix B for information on cabling a supported terminal to the RS-232-C hardwired ports.

Connecting Terminal to Series 37 Modem Port

Refer to Appendix B for information on cabling a supported terminal to the RS-232-C modem port. Note that the qualifications for a local terminal are the same for a terminal connected to the modem port.

MAINTENANCE MODE MICROCODE

Introduction

The maintenance mode microcode contains the code for interpreting maintenance commands and the Series 37 Self Test. Unlike earlier versions of HP 3000 computers, there is no special maintenance processor. The maintenance microcode resides on the CPU board. The Control B detection logic is located on the TIC. Only the TIC in slot 1 (channel 1) of the SPU card cage can have the Control B logic enabled. To enable the logic, the key switch must be in the Local or Remote position. Note also that only the console connected to port 0 (local) or port 7 (remote) can execute the Control B sequence.

When the Control B sequence is initiated, software execution is halted and the `H for help->` prompt is displayed. The maintenance microcode then begins execution. Note that the MPE environment is protected only if you execute a Run, Help or Speed command. If any other commands are executed, MPE is not protected.

Microcode Load Sequence

The ROM code is made up of executable ROM code and two types of loadable ROM code - executable code and ROM-based messages. The executable ROM code is used to load the first series of self tests from ROM into WCS upon power-up. Control is then passed to the code loaded into Writeable Control Store (WCS). WCS is RAM located on the CPU board that is used to store microcode.

This code tests the CPU chip and parts of WCS. It then loads the Code Loader and the second series of tests into Slow WCS. These tests check additional portions of the CPU chip, fast WCS, and the CPU register file. When these tests are successfully completed, the maintenance panel code is loaded into WCS and enabled. The Self Test Executive is then loaded into WCS and control is passed to it.

The Self Test Executive determines if an Auto Restart after power failure is to be performed. If a normal power-on sequence occurred, it then tests all of memory. A subset of the memory tests is run if an auto-restart is being executed. The Self Test Executive then tests all of the I/O cards installed in the system and speed senses the system console. The slot numbers of the failing cards is displayed on the LED of the SPU front panel. If the console is successfully speed sensed, the test results are displayed on the console and a prompt is issued, unless Auto Warmstart is specified. If Auto Warmstart is specified, control is passed to the Loader code and the Start device number is displayed.

Power-on Self Test

When power is applied to the SPU, the ROM-based Power-on Self Test is executed. Self Test loads all of the code in ROM 3 into WCS. The code in WCS is then executed.

The basic CPU chip test, a general WCS test, and a ROM code loader are in ROM 3. This code tests some of the Series 37 CPU chip functions. The last function performed by the CPU chip test is to test all of Slow WCS and to load two more CPU test modules. These modules test the remaining CPU chip functions. When these tests are complete, the Mainframe Panel module, the Control module, and the Test Executor module are loaded. Control is then passed to the Test Executor.

The Test Executor loads the memory tests, the PIC test, and the TIC tests. The memory tests are then executed. If a failure occurs, the memory tests are repeated and error code B is displayed on the LED

display. When the memory tests are successfully executed, the console TIC and all of the other boards in the SPU are tested. The results are displayed on the LED display. If the console TIC passes and the console speed senses, the pass/fail information is also displayed on the console. If the console fails to speed sense, the tests are looped and displayed on the LED display. If the failure occurs because the console was offline, putting the console online will result in the console being speed sensed. When the console has been speed sensed and the results have been displayed on the console, the Control module begins execution.

Control Module Options

The Control module initializes the TIC and displays the `H for help->` prompt if the Automatic Warmstart or Power Fail Auto-restart functions are not being executed. The following functions can then be performed:

Automatic Warmstart
Power Fail Auto-restart
Load/Start
Dump
Help
Run
Speed
Test

Automatic Warmstart

If MPE has been brought up and properly shut down and if the key switch is in the Normal or Remote position, the power-on microcode performs an automatic warmstart to the default device. If the key switch is in the Remote position and the remote console is connected by a modem, Self Test will loop until the modem connection is established. The microcode can then perform speed sensing with the remote console. This allows Self Test to complete and Warmstart to begin. If the CPU, memory, or the system console TIC fail Self Test, it loops on the test that detected the failure. If these boards pass Self Test, Warmstart is attempted.

If the PIC or a TIC other than the system console TIC fails Self Test, information about the failure is output to the console. You can then attempt to start the system.

Retry Auto-Restart

A subset of the memory test is executed after the Power-on CPU test if the Auto-restart flag is set. When this test is successfully executed, all of the I/O boards are tested. Communication is established with the console. Execution is then transferred to the Auto-restart entry in the Loader module. The WCS boot code is executed with the Auto-restart flag and the Load/Restart flag set and the Start device number set in the Register file.

If Auto-restart fails because the disc is not ready, up to four retries will be made. If none of the retries are successful, the `H for help->` prompt is displayed. You can type the `AR` (Autorestart) command to initiate five more tries. Error information is displayed on the console.

Load/Start

You can perform a Load or Start using the default Load and Start device numbers stored in the Time of Century Clock (TOC) RAM. You can also enter different device numbers or change the default devices. If you enter the Load/Start command, you must confirm that you want to perform the Load or Start operation. The Load or Start operation is performed by loading the Load Execution code and the WCS

boot code, and transferring control to the Load Execution code. The Load Execution code tests for valid Load or Start parameters, updates the TOC RAM, and transfers control to the WCS boot code. If a parameter error occurred or if a change in parameters is requested, control is transferred back to the Control module. If the parameters are correct and if a Load or Start operation is to be executed, control is passed to the WCS boot code. It loads the HP 3000 instruction set from the disc or tape and continues with the Load or Start operation.

Once the Load/Start command is executed, a timer is set. If the target device does not become ready in the allowed time, a time-out error (WCS boot failure) is displayed on the screen.

The format of the Load command is:

L[oad] [channel,device[,{P[erm] C[hange]}]]

The parameters in brackets are optional. The parameters in braces are also optional but you can enter only one of the parameters. If you enter "P", Load is performed from the specified device. The new channel and device numbers are stored in the TOC. If you enter "C", no Load operation is performed. The TOC is updated with the specified device number.

The format of the Start command is:

ST[art] [channel,device[,{P[erm] C[hange]}]]

The parameters in brackets are optional. The parameters in braces are also optional but you can enter only one of the parameters. If you enter "P", Start is performed from the specified device. The new channel and device numbers are stored in the TOC. If you enter "C", no Start operation is performed. The TOC is updated with the specified device number.

Dump

Dump loads the dump routine from the specified device. Dump uses the Start default device number stored in the TOC RAM or the device specified by the operator. The Dump command asks you to confirm that you want to perform a dump. If so, Load or Start is performed by loading the Load Execution code. Control is then transferred to the Load Execution code.

The Load Execution code tests for valid Dump parameters and transfers control to microcode in WCS. If no microcode is loaded, control is returned to the Control module. If the parameters are correct, and the microcode is loaded, control is passed to the Dump code in the instruction set. The CPU loads the Dump code from the specified device and dumps the system.

The format of the Dump command is:

D[ump] [channel,device]

The parameters in brackets are optional.

Help

The Help command displays the version of the CPU microcode that is loaded or -------- if no microcode is loaded. It then displays the functions of the Control mode.

There are 16 possible responses to the `H for help->` prompt. They are listed in table 3-3. The channel and device for the Load, Start, and Dump commands must be specified unless the default device has been defined using the ",P" or ",C" options. The Dump command always defaults to the Start device. The ",P"

option updates the Load or Start device data in the TOC and loads or starts the system. The ",C" option updates the Load or Start data in the TOC but does not load or start the system. The valid channel numbers are 1 through 4 in the SPU and 9 through 13 in the Extender. If the system displays the `H for help->` prompt after a Halt command or Control B sequence has been executed, the Run command can be used to run the system. The AR command enables you to try another restart if the system has already attempted to restart the system. The remaining Load/Start-type commands (COL, COO, DIS, NEW, RELO, TAPE, UPDA, and WAR) use the Load or Start device number stored in the TOC RAM.

Table 3-3. Control Mode Commands

AR	Retry Auto Restart.
COLdstart	Perform COLdload using Load device with no dialog.
COOlstart	Perform COOlstart using Start device with no dialog.
DISc	Perform Start using Start device. Same as Start with no parameters.
DISk	Same as DISc.
DUmp	Perform Dump using the indicated or Start device.
Help	Display Help messages.
Load	Perform Load from load device or specified device with dialog.
NEWsystem	Perform Reload using Load device (only for factory MIT).
RELOad	Perform Reload using Load device with no dialog.
RUN	Run system after Control B halt.
SPeed	Perform speed sensing.
STart	Perform Warm/Coolstart from Start device or specified device with dialog.
TApe	Perform Load using Load device.
TEst	Go to Test mode.
UPDAte	Perform Update using Load device with no dialog.
WARmstart	Perform Warmstart using Start device with no dialog.

Run

Run returns execution to the software.

Speed

The Speed command executes under maintenance microcode. It starts a timer and allows you to change the baud rate. When you press the carriage return, the start bit is speed sensed.

Test

The Control mode code requests that you confirm that the Test mode is to be entered. If so, it loads the Test Executor module and transfers control to the Test entry point in the Test Executor module. If not, control is passed back to the Control module.

Test Mode

The Test Executor module displays the functions of the Test module and the `Test->` prompt. The functions are:

All
CPU
Exit
IOMAP
Memory
Channel
Help

All. This Test function executes in the following order:

CPU
Memory
Channel
IOMAP

You can loop this test up to 9999 times. The default is 1. Upon completion, you are returned to the `Test->` prompt.

CPU. This function tests all of the Bank registers, the TOC RAM locations, and ensures that the TOC and MPE timers are counting. It also displays LED codes 0 through F and tests the Watchdog timer function.

You can loop this test up to 9999 times. The default is 1. Upon completion, you are returned to the `Test->` prompt.

Exit. Control is returned to the Control module. The `H for help->` prompt is displayed.

IOMAP. This feature runs the memory size test portion of the memory test. It displays the size of memory, the Load, Start, and Dump devices, and then displays the types of cards installed in the system. The types of devices on the PIC are also displayed.

You can loop this test up to 9999 times. The default is 1. Upon completion, you are returned to the `Test->` prompt.

Memory. The full memory test is performed and a pass/fail message is displayed on the console. The number of the failing section is displayed if a failure occurs.

You can loop this test up to 9999 times. The default is 1. Upon completion, you are returned to the `Test->` prompt.

Channel. The appropriate test is run for each card installed in the SPU. If a failure occurs, the failure code is displayed next to the card description.

You can loop this test up to 9999 times. The default is 1. Upon completion, you are returned to the `Test->` prompt.

The Test response to the `H for help->` prompt displays the Self Test menu. You can then select from six

test options in addition to Help and Exit.

The Self Test options are shown below. Note that all of the information within the brackets is optional.

A[ll] [count]	A complete Power-on Self Test and several additional CPU tests are performed. The microcoded version of IOMAP is also run. All Self Tests are run [count] times.
C[PU] [count]	The CPU Power-on Self Test and additional tests of circuitry not tested during Power-on Self Test are performed. The CPU Self Test is run [count] times.
E[xit]	Exits the Test mode and re-enters the Control B mode.
I[OMAP] [count]	The Microcoded version of IOMAP is run. It displays the number of banks of memory and the devices in the TOC RAM. It identifies the I/O channels that are installed. IOMAP is run [count] times.
M[emory] [count]	Power-on Self Test is run on all of memory. For more exhaustive tests and additional failure information, run the MDIAG37 program in the Diagnostic Utility System (DUS).
CH[an] [count[,channel]]	Power-on Self Test is run on a specified I/O channel or on all channels. All channels are tested if no channel number is specified. For example, S tests all channels once. `CH 2,1` runs the tests on the TIC in slot 1. The test is executed twice.
PON [count]	Run or loop the Power-on Self-Test. The key switch must be in the Local position.

LESSON 3 QUIZ

1. What is the function of the Local keyswitch position? How does it differ from the Normal position?
   Allows CNTL-B Functions on Local Console
2. Under what conditions will the AC indicator on the front panel be lit?
   with power (AC) Applied
3. Under what conditions will the RUN indicator on the front panel be lit?
   when CSRQ is asserted
4. When using the Load/Start command, what is the difference between the "P" and the "C" parameters?
   P: Perm C= change
5. How must the SPU be configured to receive and execute a Control B sequence?
   Local for Console Remote hooked to modem for Remote Console
6. What commands can be issued to obtain the device addresses of the Load, Start, and Dump devices?
   IOMAP
7. List the correct command and options required to test a PIC PCA installed in slot 2 of the I/O Extender. TE, Ch, 1, 10
8. If you execute a Load command to a non-existent device and you do not want to wait for the time-out, how can you exit the state?
   Turn pwr off.
9. Under what circumstances will the front panel LED display be blank?
   Selftest passed
10. How can you verify the SPU configuration?
    I/O MAP

Answers in Appendix C.

CONSOLE OPERATION LAB

The following equipment is required for this lab:

A Series 37 SPU

A supported terminal

1. Connect a terminal to the Series 37 SPU. Configure the terminal as a local console.

2. Apply AC power and turn the keyswitch to the Normal position. Record the states of the front panel LEDs. AC, DC,

3. Turn the keyswitch to the DC OFF position. Turn off the power to the terminal. Turn the keyswitch to the Normal position.

Record the states of the front panel LEDs and compare them with the states previously recorded.

C, \ AC, DC

If the above states were displayed at a customer site, what failure conditions would be indicated?

4. Does the LED display indicate that Selftest is looping? (True or False)

5. Turn off the DC power on the Series 37 SPU. Turn on the terminal AC power. Reapply DC power by turning the keyswitch to the Remote position.

Record the states of the front panel LEDs.

6. Is the local console active?

7. Is Selftest looping?

8. Disconnect the terminal from the Series 37 SPU and reconnect it to the modem port. Is the console active? Verify this by typing "H" and then pressing the RETURN key.

Answers in Appendix C.

MAINTENANCE MICROCODE LAB

1. Connect the terminal to port 0. Turn the keyswitch to the Normal position. Execute a Load command and attempt to exit the hung state by issuing a Control B sequence (L 4,1).
   Does not work
2. Did the Control B sequence exit the loop?
   No unable to execute cntl-B in Pos 1
3. What must be done for the Control B to work?
   Put in pos2 (possib may [may not] work) try cycle pwr
4. From either the local or remote console, execute a Speed command and change the baud rate to 300 baud.

5. Now change the baud rate to 9600 baud.

6. Enter the Test mode and run five complete passes of all tests. List the commands required to do this.

7. Change the Load/Start device address in the TOC to 4,4 and 4,6 respectively.
   OK

Run IOMAP and verify the above settings.

Answers in Appendix C.

Removal and Replacement

Lesson 4

OVERVIEW

This lesson describes the removal and replacement of the assemblies in the SPU and the Extender. Assemblies or procedures that are unique to one unit are identified. Do not remove any of the assemblies at this time. You will remove and replace some of the assemblies when performing the lab exercise at the end of this lesson.

LEARNING OBJECTIVES

When you have successfully completed this lesson, you will be able to:

- Remove and replace all replaceable assemblies in the Series 37 SPU and the I/O Extender.

WARNING

Hazardous voltages are present inside the computer and the extender. Heed all WARNING - HAZARDOUS VOLTAGE labels.

CAUTION

The contents of memory will be lost when the main (line) and battery voltages are both off. Therefore, before proceeding, ensure that any contents of memory to be saved are stored on another medium for later retrieval.

CAUTION

Some of the semiconductor devices used in this equipment are susceptible to damage by static discharge. Depending on the magnitude of the charge, device substrates can be punctured or destroyed by contact or mere proximity to a static charge. These charges are generated in numerous ways, such as simple contact, separation of materials, and normal motions of persons working with static sensitive devices. When handling or servicing equipment containing static sensitive devices, adequate precautions must be taken to prevent device damage or destruction. Only those who are thoroughly familiar with industry accepted techniques for handling static

sensitive devices should attempt to service the boards with these devices. In all instances, measures must be taken to prevent static charge buildup on work surfaces and persons handling the devices.

The following paragraphs describe how to remove and replace the various assemblies in the SPU and the Extender.

REAR PANEL

Removal

Remove the rear panel as follows:

a. Refer to figure 4-1.

b. Using a number 1 Pozidriv screwdriver, loosen six captive screws and remove the rear panel.

c. Unplug the power cord from the fan on the rear panel.

Replacement

Replace the rear panel by reversing the removal procedure.

NOTE

Ensure that the fan power cord is positioned under the board in slot 1 before replacing the rear panel.

RS-232-C CONNECTOR ASSEMBLY.

Removal. Remove the RS-232-C connector assembly as follows:

a. Refer to figure 4-1.

b. Remove any attached device cables.

c. Press the detent tabs at one side of the connectors and press the RS-232-C connector assembly back through the rear panel.

Replacement. Replace the RS-232-C connector assembly as follows:

a. Refer to figure 4-1.

b. Position the connector assembly in the correct slots of the rear panel.

c. Orient the connector assembly so that the TIC PCA connector is positioned at the bottom of the assembly.

d. Carefully press the connector assembly into the slots, applying even pressure to the RS-232-C upper and lower boards.

RS-232-C BOARDS.

Removal. Remove each of the two RS-232-C boards as follows:

a. Refer to figure 4-2.

b. Using small pliers, compress the tabs on one of the I/O module clamps and separate one end of the upper RS-232-C board from the RS-232-C assembly.

c. Using small pliers, compress the tabs on the other I/O module clamp and separate the other end of the upper RS-232-C board from the RS-232-C assembly.

d. Using small pliers, compress the tabs on one of the I/O module clamps and separate one of the I/O module clamps from the lower RS-232-C board.

e. Using small pliers, compress the tabs on the other I/O module clamp and separate the other I/O module clamp from the lower RS-232-C board.

Replacement. Reassemble the RS-232-C assembly as follows:

a. Refer to figure 4-2.

b. Press the two I/O module clamps into the lower RS-232-C board.

c. Carefully align the board interconnect plug on the lower RS-232-C board with the board interconnect jack on the upper RS-232-C board.

d. Press the upper RS-232-C board onto the two I/O module clamps, being careful to apply even pressure at each end of the board.

I/O GROUND CLIPS.

Removal. Remove each of the four I/O ground clips in the RS-232-C assembly as follows:

a. Refer to figure 4-2.

b. Using a number 1 Pozidriv screwdriver, loosen two screws and remove the I/O ground clip.

Replacement. Replace each of the I/O ground clips be reversing the removal procedure.

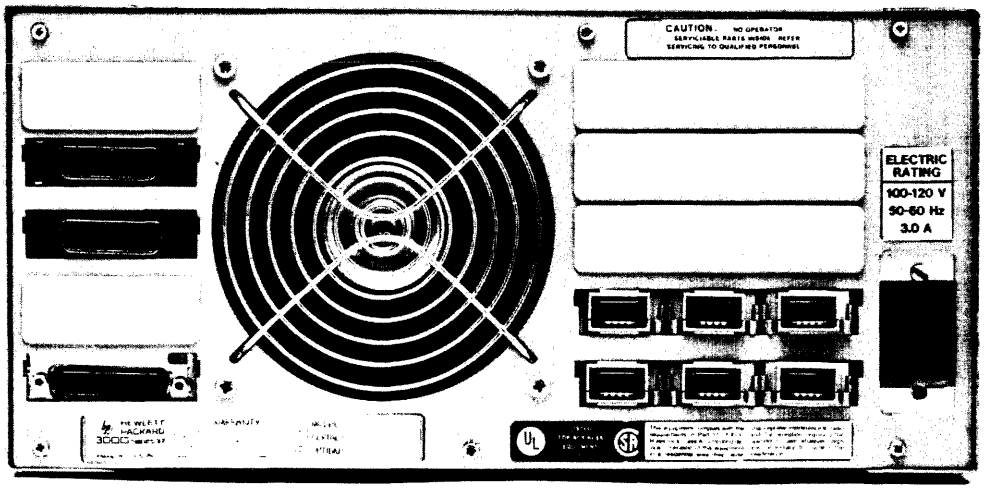


Figure 4-1. SPU Rear View

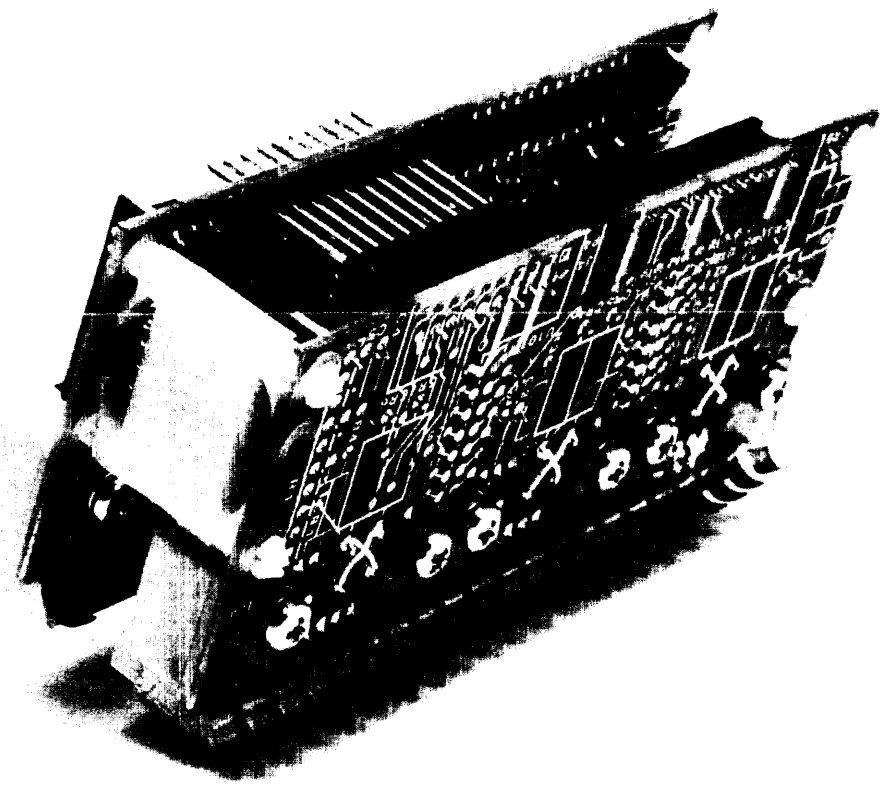


Figure 4-2. RS-232 Connector Assembly

TUBAXIAL FAN.

Removal. Remove the tubaxial fan from the rear panel as follows:

a. Refer to figure 4-1.

b. Using a number 2 Pozidriv screwdriver and an open-end wrench, remove four nuts, four lock washers, four flat washers, and four bolts, and remove the tubaxial fan, fan grill, and finger guard from the rear panel.

Replacement. Replace the tubaxial fan by reversing the removal procedure.

POWER SUPPLY

Removal

Remove the power supply as follows:

a. Refer to figure 4-3.

b. Remove two Philips screws.

c. Grasp the power supply by the handle and pull the power supply from the card cage.

Replacement

Replace the power supply as follows:

a. Align the top and bottom of the power supply board with the guides at the top and bottom of the card cage.

b. Press the power supply until it is firmly mounted in the power supply connector.

POWER SUPPLY FUSE.

Removal. Remove the power supply fuse as follows:

a. Refer to figure 4-4.

b. Grasp the fuse and remove it from the fuse holder.

Replacement. Replace the power supply fuse by reversing the removal procedure.

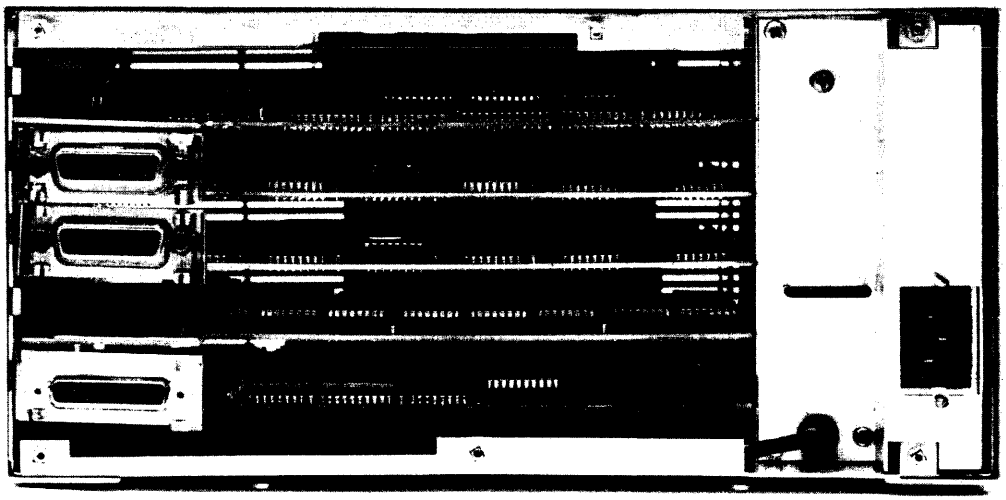


Figure 4-3. SPU Rear View, Rear Cover Removed

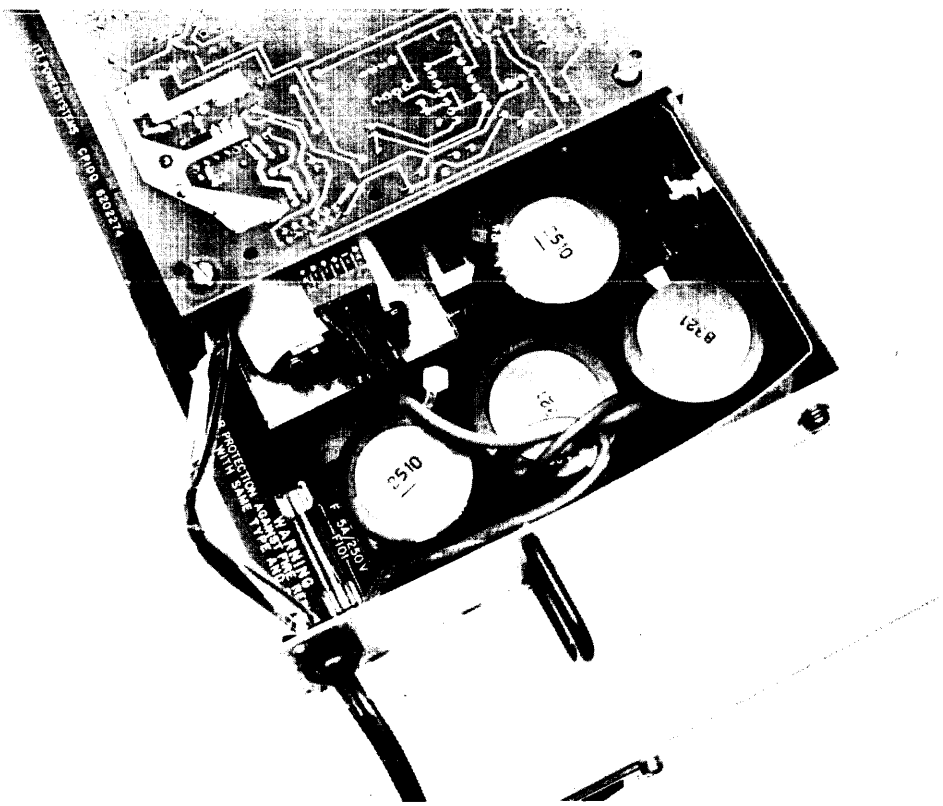


Figure 4-4. Power Supply Fuse and Configuration Switch

Lesson 4

nd Replacement

removal and replacement of the assemblies in the SPU and the Extender. iat are unique to one unit are identified. Do not remove any of the assemblies ɔve and replace some of the assemblies when performing the lab exercise at the

TIVES

completed this lesson, you will be able to:

ːe all replaceable assemblies in the Series 37 SPU and the I/O Extender.

WARNING

Ita ıre present inside the computer and the extender.
NIN - HAZARDOUS VOLTAGE labels.

CAUTION

f memory will be lost when the main (line) and battery ɔth off. Therefore, before proceeding, ensure that any nory to be saved are stored on another medium for later

CAUTION

conductor devices used in this equipment are susceptible to discharge. Depending on the magnitude of the charge, can be punctured or destroyed by contact or mere tic charge. These charges are generated in numerous ways, ontact, separation of materials, and normal motions of with static sensitive devices. When handling or servicing ıing static sensitive devices, adequate precautions must be d e damage or destruction. Only those who are ar industry accepted techniques for handling static

eplacement ement

ɔck washers,
om the rear

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label

Vac

ttom of the card

CAUTION

Observe anti-static procedures when removing or replacing the plug-in boards.

Removal

Remove a plug-in board as follows:

a. Insert the board extractor tool in the hole in the right front corner of the board.

b. Firmly pull the board out of the back plane connector.

c. Remove the board extractor tool and manually remove the board from the card cage.

Replacement

Replace a plug-in board as follows:

a. Align the plug-in board with the guides at the sides of the card cage.

b. Press the plug-in board until it is firmly mounted in the back plane connector.

FRONT PANEL

Removal

Remove the front panel as follows:

a. Remove the key from the keyswitch.

b. Using a number 0 Philips screwdriver, HP P/N 8710-0978, loosen the two captive screws at the top corners of the front panel.

c. Pull the panel away from the chassis.

Replacement

Replace the front panel by reversing the removal procedure.

BATTERY PACK

Removal

Remove the battery pack as follows:

a. Refer to figure 4-5.

b. Unplug the battery power cable from the battery/display panel connector.

c. Lift the battery pack away from the retaining brackets.

Replacement

Replace the battery pack by reversing the removal procedure.

BATTERY HOLDER

Removal

Remove the battery holder as follows:

a. Refer to figure 4-6.

b. Using a number 2 Pozidriv screwdriver, remove four screws and remove the battery holder.

Replacement

Replace the battery holder by reversing the removal procedure.

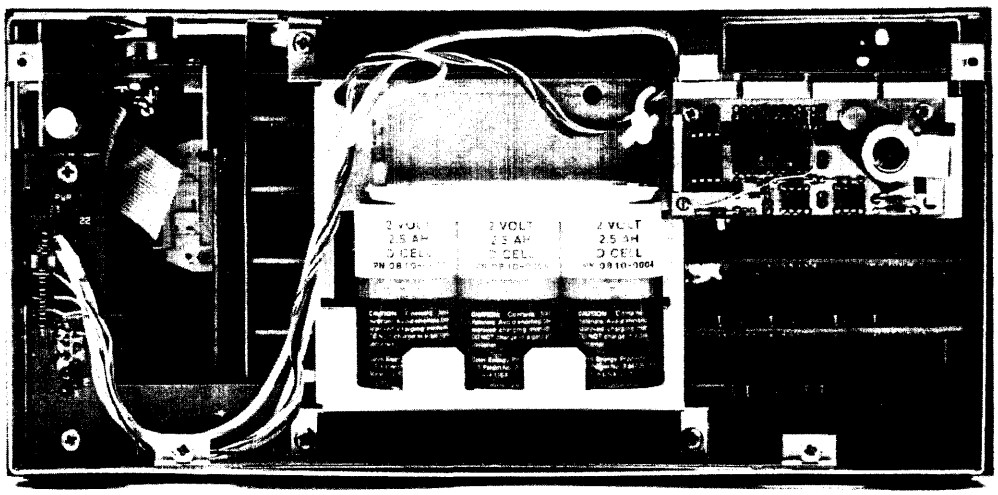

Figure 4-5. SPU Front View, Front Cover Removed

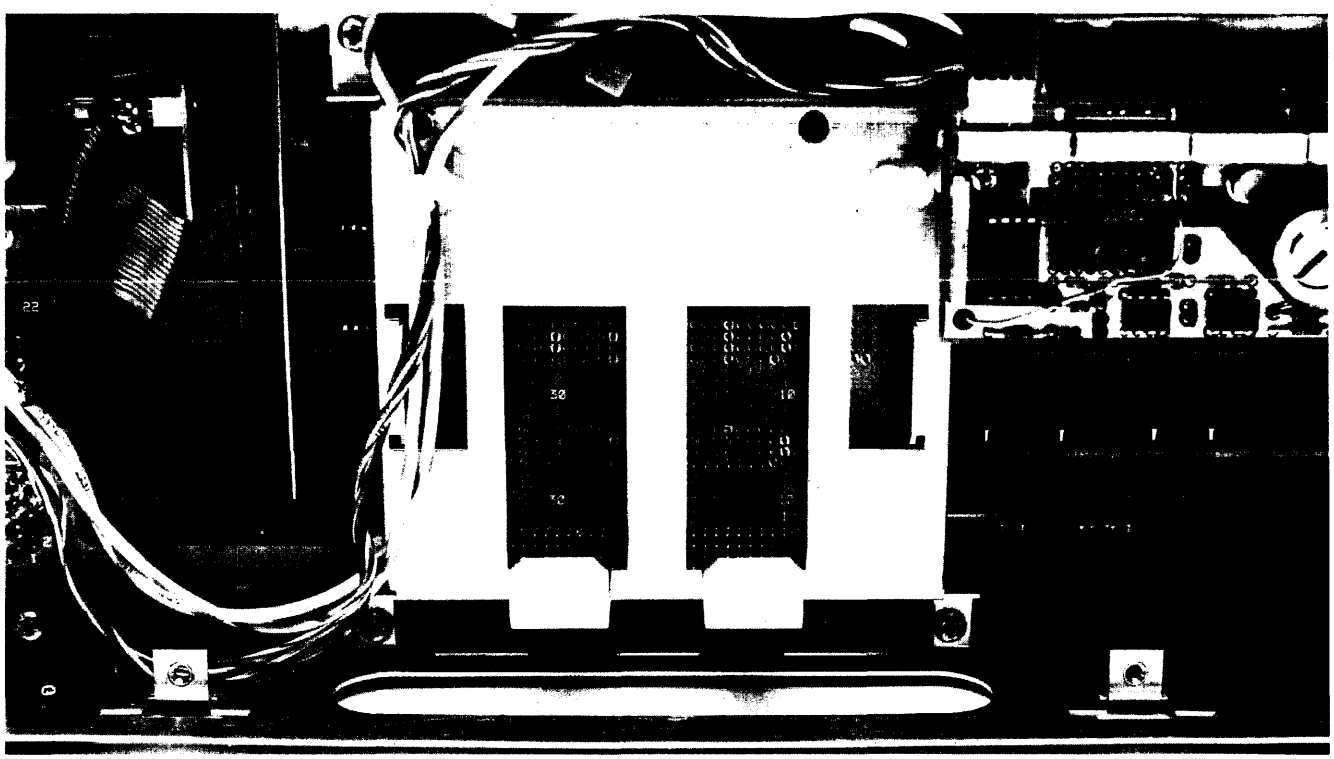

Figure 4-6. SPU Front View, Front Cover and Battery Pack Removed

BACKPLANE

Removal

Remove the backplane as follows:

a. Refer to figure 4-6.

b. Remove the rear panel, power supply, plug-in boards, battery pack, and battery holder as described above.

c. Using a number 2 Pozidriv screwdriver, remove the remaining two screws and remove the backplane.

Replacement

Replace the backplane as follows:

NOTE

If you are replacing the Extender backplane, install any boards, except the CPU, in slot 1 and slot 5. No CPU board can be installed in the Extender.

a. Refer to figure 4-6.

b. Replace the back plane by reversing the removal procedure but do not tighten the six mounting screws.

c. Insert the CPU board in slot 5 of the SPU card cage. Ensure that the board is firmly seated in the backplane connector.

d. Insert the TIC board in slot 1 of the SPU card cage. Ensure that the board is firmly seated in the backplane connector.

e. Using the replacement procedure described below, install the power supply in the card cage.

f. When the boards are securely mounted in the backplane and are correctly aligned, tighten the six mounting screws.

g. Verify correct alignment by installing the remaining boards.

DISPLAY PANEL

Removal

a. Refer to figure 4-5.

b. Unplug the display panel cable from the battery/display panel connector.

c. Using a number 1 Pozidriv screwdriver, remove the two screws and remove the display panel board.

Replacement

Replace the display panel board by reversing the removal procedure. Replace this board only after the back plane and the CPU board have been correctly installed and aligned.

DISPLAY PANEL LEDS.

Removal.

NOTE

The extender has the left-most pair of indicator LEDs. It does not have the right-most pair of indicator LEDs or the hexadecimal LED.

Remove the display panel LEDs as follows:

a. Refer to figure 4-5.

b. Firmly grasp the right-most pair of indicator LEDs and pull the LEDs away from the socket.

c. Firmly grasp the left-most pair of indicator LEDs and pull the LEDs away from the socket.

d. Firmly grasp the hexadecimal LED and pull the LED away from the socket.

Replacement. The location of pin 1 on each LED is identified by a notch on the plastic housing. Position the LED so that the notch is at the top right corner.

Replace the indicator LEDs and the hexadecimal LED by reversing the removal procedure.

MOUNTING FEET

Removal

Remove each of the mounting feet as follows:

a. Remove the front panel as described above.

b. Press down on the rear tab of the mounting foot until the tab is released from the card cage.

c. Push the mounting foot to the rear of the card cage until it is released from the card cage.

Replacement

Replace each of the mounting feet by reversing the removal procedure.

SPU/EXTENDER INTERCONNECT CABLE

Removal

Remove the SPU/Extender interconnect cable as follows:

a. Refer to figure 4-7.

b. Remove the SPU front panel previously described.

c. Remove the Extender front panel previously described.

d. Manually loosen four captive knurled bolts.

e. Grasp the top pair of knurled bolts and pull the interconnect cable away from the SPU front plane.

f. Grasp the bottom pair of knurled bolts and pull the interconnect cable away from the Extender front panel.

g. Remove the interconnect cable through the slot in the card cage.

Replacement

Replace the SPU/Extender interconnect cable by reversing the removal procedure. Note that there are keys at the top of each of the two connectors.

SPU COVER PLATE

Removal

The SPU cover plate covers the interconnect cable slot in the SPU card cage.

Remove the SPU cover plate as follows:

a. Refer to figure 4-6.

b. Using a number 1 Pozidriv screwdriver, remove two screws and remove the SPU cover plate.

Replacement

Replace the SPU cover plate by reversing the removal procedure.

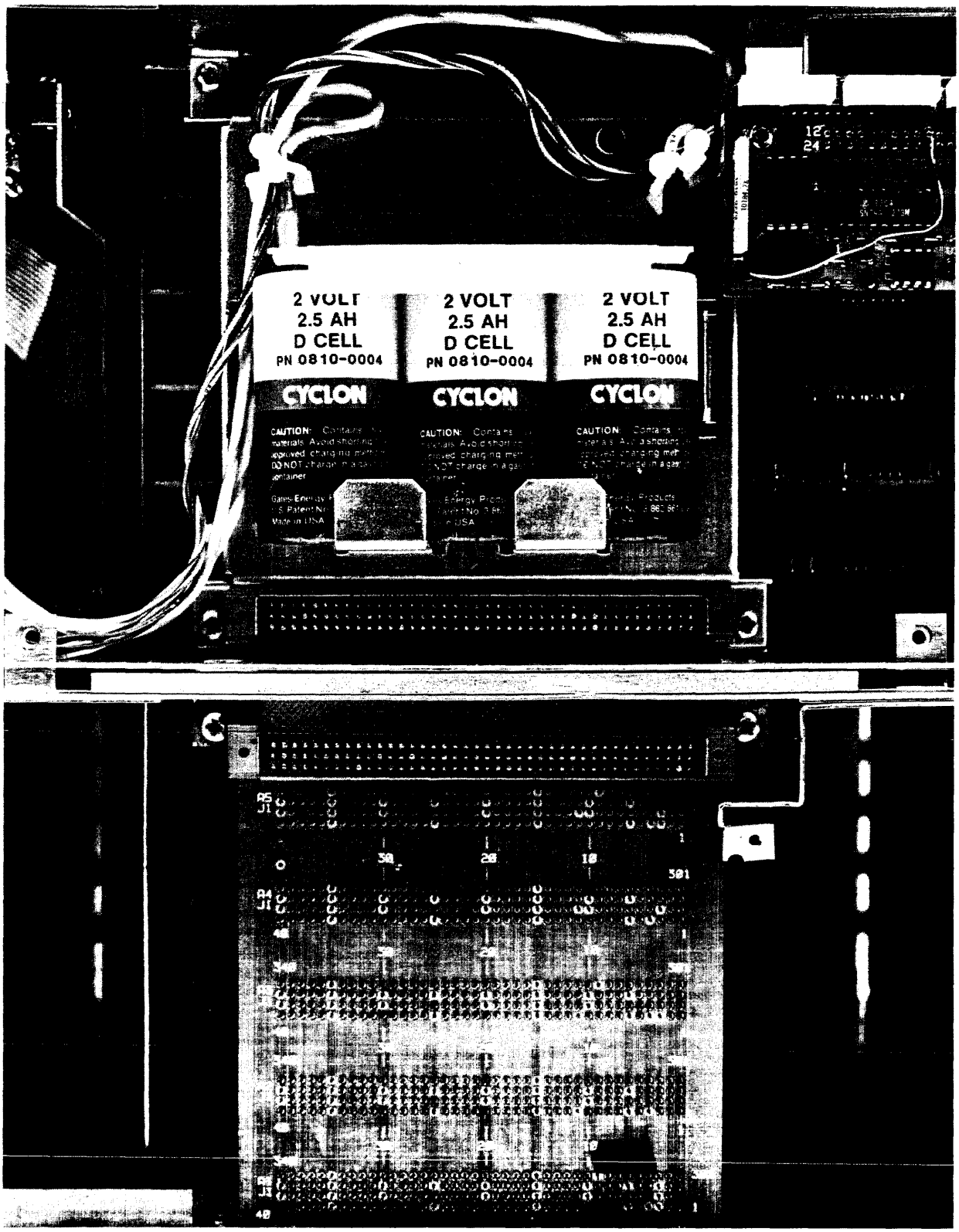

Figure 4-7. SPU/Extender Front View, Front Covers Removed

LESSON 4 QUIZ

1. The lithium battery used in the Time of Century Clock (TOC) circuitry is a field replaceable item. (True or False).

2. If one port fails on an RS-232-C connector assembly, it is necessary to replace the entire assembly (all six ports). (True or False)

3. There are field replaceable parts in the power supply. (True or False).

4. List the steps required to install a new backplane.
Remove Back pnl, BBS, P.S. Battery w/o 2 screws Remove Bk pln

Amswers in Appendix C. 6 screws no tighten
Replace Bk plane ^ install tie, cpu Bd
CK Bd Align tighten screw then Reinstall all else

REMOVAL AND REPLACEMENT LAB

The following equipment is required for this lab:

A Series 37 SPU

CAUTION

Some of the semiconductor devices used in this equipment are susceptible to damage by static discharge. Depending on the magnitude of the charge, device substrates can be punctured or destroyed by contact or mere proximity to a static charge. These charges are generated in numerous ways, such as simple contact, separation of materials, and normal motions of persons working with static sensitive devices. When handling or servicing equipment containing static sensitive devices, adequate precautions must be taken to prevent device damage or destruction. Only those who are thoroughly familiar with industry accepted techniques for handling static sensitive devices should attempt to service the boards with these devices. In all instances, measures must be taken to prevent static charge buildup on work surfaces and persons handling the devices.

1. Remove the following assemblies from the Series 37 SPU:

    a. Display Panel

    b. Battery Pack

    c. Power Supply

    d. Plug-in Boards

    e. Back Plane

    f. RS-232-C and RS-422-C Connector Assemblies

2. Reassemble the Series 37 SPU using the removal and replacement procedure. Do not install the plug-in boards.

3. Perform the following card cage build-up procedure:

    a. Install the CPU PCA in the appropriate slot.

    b. Power up the system and record the state of the hexadecimal LED.

    c. Turn off DC power and remove the AC power cord. Install the memory PCA in the appropriate slot.

    d. Power up the system and record the state of the hexadecimal LED.

e. Turn off DC power and remove the AC power cord. Install the TIC PCA in the appropriate slot. Install the connector assembly. Connect a terminal to port 0.

f. Power up the system and record the state of the hexadecimal LED Note whether the status is displayed on the terminal.

g. Turn off DC power and remove the AC power cord. Install the PIC PCA in the appropriate slot.

h. Power up the system and record the state of the hexadecimal LED. Observe the terminal display.

i. Turn off DC power and remove the AC power cord. Remove the memory PCA.

j. Power up the system and record the state of the hexadecimal LED.

k. Is any information displayed on the terminal? (Yes or No).

l. What conclusions can you make about the execution of Selftest?

Answers in Appendix C.

Power System

Lesson 5

OVERVIEW

This lesson describes the operating characteristics of the power system, the input power characteristics, and the output power characteristics.

LEARNING OBJECTIVES

When you have successfully completed this lesson, you will be able to:

- Identify and locate power supply components, such as connectors, switches, fuses, battery, temperature sensors, and test points.
- Describe the power supply operating features and the control signals VON, +BIAS, -BBK, and -OTS.
- Describe the power supply interface to the system and the interface signals -OTW, -PSW, and -OTS.
- Identify the available diagnostic tools.

POWER SYSTEM FUNCTIONAL DESCRIPTION

General Description

Figure 5-1 is a block diagram of the power system. The power system consists of the power supply and the battery backup pack. The power supply outputs six power levels and five control signals. The battery backup supplies +5Vdc at 3 amps for approximately 20 minutes if a power outage occurs.

DC Overvoltage Protection

Each voltage output from the power supply provides overvoltage protection by means of a crowbar circuit. The crowbar circuit prevents a voltage greater than the specified maximum.

AC Input Overvoltage Protection

The power supply is protected from damage if the AC line voltage exceeds the safe operating limit. It is protected from damage if a high power line condition occurs or if the input voltage selector switch is set incorrectly. If these conditions occur, the input fuse will blow. A 5A 250V fuse is used in both 115Vac and 230Vac operation.

Overcurrent Protection

An overcurrent condition initiates current foldback to zero for all output voltages except +5Vdc. Voltages return to normal when the overcurrent condition no longer exists. Overcurrent is defined as current 25% over the maximum rated current of any output. The +5Vdc overcurrent protection current limits for 0.5 to 1 second. After this, it latches off, turning off the power supply.

Overheating Protection

Two thermal sensors are located on the main P.C. board near the front of the power supply. These sensors measure the ambient air temperature. The Overtemp Warning (OTW) sensor closes when the internal temperature of the computer reaches 45 degrees C. The Overtemp Shutdown (OTS) sensor closes when the internal temperature of the computer reaches 60 degrees C.

45°C = 113°F

60 C = 140°F

Fault Resets

A fault condition occurs if overvoltage, overcurrent, or overheating conditions occur. If any fault condition occurs, the power supply shuts down all DC outputs, including the +5Vdc output that would otherwise be supported by the Battery Backup module. You can recover from a fault by cycling the ON/OFF switch after removing the fault.

Battery Charger

The charger circuit charges a lead-acid battery pack. The pack supports the +5B output when AC voltage is low. The charger provides +7.2Vdc to the pack at a nominal 0.5 amps. It is a constant voltage type and keeps the battery at a constant voltage as long as the AC line is up. The charger is not shut down if you turn the ON/OFF switch to the OFF position. When a power fail occurs and the battery backup is the only source of power to the +5B output, the battery pack voltage is monitored. When this voltage drops below +5.5Vdc, the battery backup is taken out of the circuit by a relay. This prevents the battery from completely discharging, protecting it from damage. AC power must be restored and the ON/OFF switch must be cycled to reconnect the relay. Note that when the ON/OFF switch is in the OFF position (the +VON line is low) and AC power is absent, there is a delay of about one second before the battery disconnect relay is opened.

Battery Backup

If the +VON line remains high (true) and the 6-volt battery has adequate charge, the +5B output will remain within specification. This provides memory backup voltage until battery capacity is depleted. The battery provides approximately 15 minutes of memory support for one megabyte at a discharge current of three amperes. The power-fail auto-restart capabilities of the computer are enabled after AC power returns to normal, if the battery capacity is not depleted.

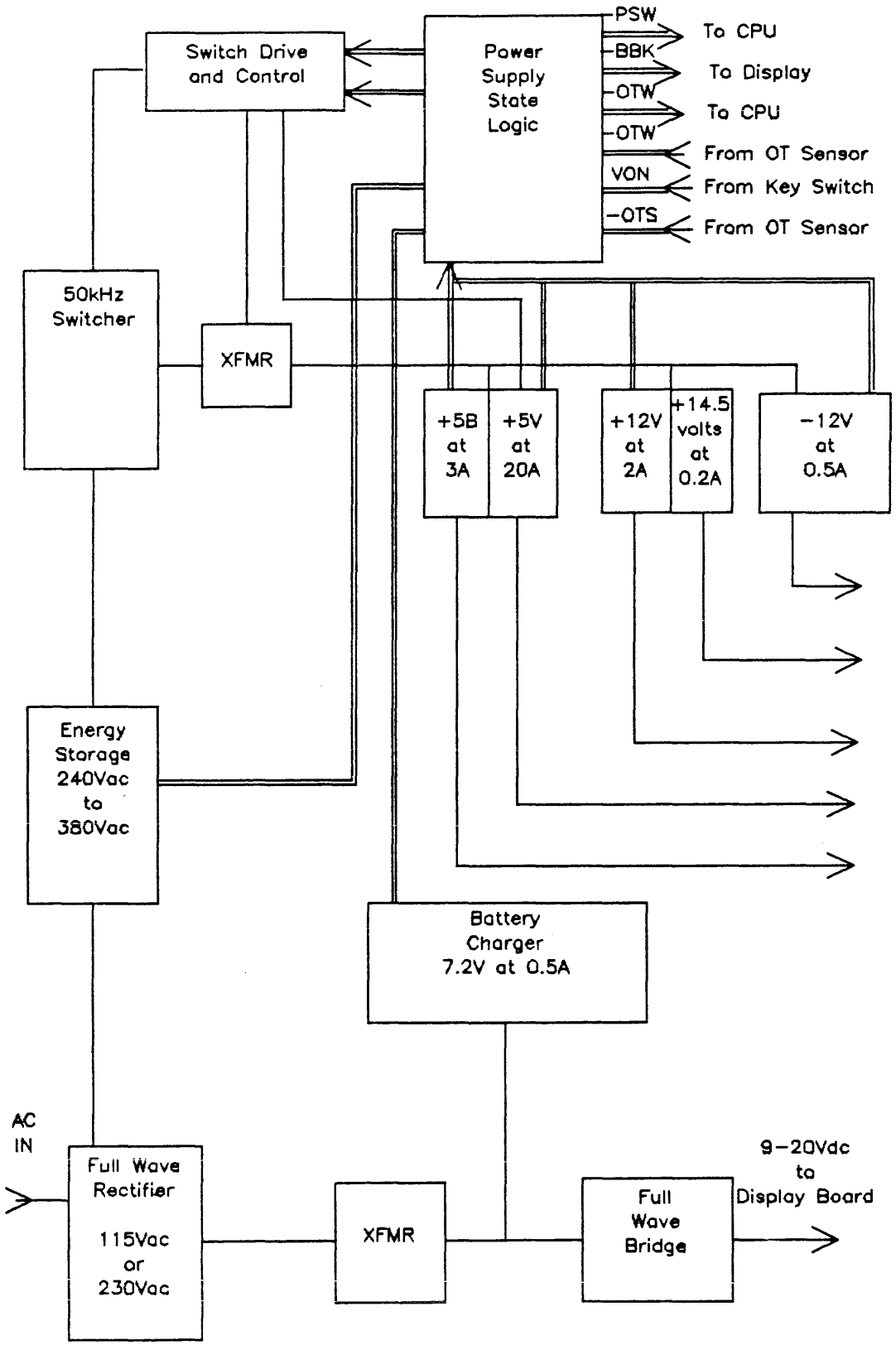

Figure 5-1. Power System Block Diagram

Input Power Specifications

The input electrical specifications of the power supply are shown below.

VOLTAGE	Single phase Nominal operating range: 100-120Vac or 220-240Vac Maximum operating range: 85-135Vac or 170-270Vac
CURRENT	4 amps maximum at 110Vac
POWER	270 watts maximum at maximum output load
FREQUENCY	45 to 66 Hz.
HOLD-UP	One cycle of input AC can be dropped without causing a Power Fail condition.
POWER LINE * DISTURBANCE	The computer will perform correctly in normal and common modes under the following pulse conditions:

	TYPICAL	WORST CASE
Volts	1000 V (peak)	1000 V (peak)
Width	10 usec	100 usec
Rise	1.5 usec	100 nsec
Fall	1.5 usec	100 nsec

* NOTE: This specification indicates the amount of abnormal energy that can be handled by the AC input circuitry without causing a system failure. The worst case pulse specified above represents this energy handling capability. Therefore, if one or more of the specified parameters vary so that the energy level of the pulse increases, then the system may fail.

Output Specifications

Output power and control signals interface to the power supply through one connector that connects directly to the computer backplane. The output power specifications are defined in the following table. The control signals are defined in the following section.

Output Power Specifications

OUTPUTS	+5	+12	+14F	+5B	-12	+BIAS
VOLTAGE (DC)	+5.0	+12.6	+14.5	+5	-12	9-20V pk
MAX CURRENT (amperes)	20	2.0	0.2	3	1.25	0.05
MIN CURRENT (amperes)	1.5	0.04	0.1	0.05	0.05	0.02
REGULATION (over output current and line voltage range)	+/-2%	+/-2%	+/-15%	+/-3%	+/-5%	full wave rectified
DYNAMIC LOAD VOLTAGE REGULATION (load change: 50% to 100%)	+/-3%	+/-3%	+/-10%	+/-3%	+/-3%	
DYNAMIC LOAD RECOVERY TIME	0.5 msec	0.5 msec		0.5 msec	0.5 msec	
RIPPLE AND NOISE (max. p-p)	50 mv	100 mv		50 mv	100mv	
OVERVOLTAGE PROTECTION (crowbar turn-on)	5.8Vdc	14Vdc		5.8Vdc	-14Vdc	

The +14F output is used to power the DC fan. The +5B output is the battery backup +5 Vdc voltage. It is output at a maximum of three amperes when it is supplied only by the battery. When AC is present, the output is derived from and is in addition to the current specified for the +5 output. Ripple and noise are defined as the effective peak-to-peak noise measured into a resistive load located at the output terminals of the supply.

Output Control Signals

The output control signals, the signal line characteristics, and the interface connector pin-outs are described below.

Power Supply Warning (-PSW). The Power Supply Warning (-PSW) line is used to monitor the voltage in the main input capacitors. Whenever -PSW is high, all DC output voltages produced by the power supply will be within their specified operating ranges. The line is set high when the line voltage has reached the minimum operating voltage. If the line voltage drops below the minimum operating voltage for more than one cycle, the -PSW line is set low. The output voltage must remain within specified tolerances for a minimum of three milliseconds after the -PSW line is set low. The -PSW signal sent by the power supply must remain true for 500 microseconds after a power low condition is detected. The power supply sends -PSW to the CPU via the backplane. When -PSW is low, the CPU will have an interrupt pending. This results in the execution of a power-fail routine that saves the registers required for recovery in battery-supported memory.

OverTemp Shutdown (-OTS). The OverTemp Shutdown (-OTS) line shuts down the power supply if an overtemperature condition occurs. The temperature must be greater than 60 degrees C. All voltages will be latched off, except the float voltage to the battery and the +BIAS voltage. The state of this sensor is sent to the CPU via the power supply/backplane interface connector. The line originates at the high temperature sensor contacts, located at the front of the main PCA of the power supply. It is set closed if an overheat condition exists. The state of the sensor is interfaced directly to the power supply and is translated to a TTL high/low state for supply control. After the sensor closes, the power supply initiates a 500-millisecond time delay. After this, all DC voltages, except +BIAS, are latched off.

OverTemp Warning (-OTW). The OverTemp Warning (-OTW) line originates at the maximum operating temperature range sensor, located near the OTS sensor on the power supply. It is set closed (-OTW is set low) when the temperature exceeds 45 degrees C. The state of this sensor is sent to the CPU via the power supply/backplane interface connector. The signal is used by the CPU to issue an operator warning message.

DC Voltages On (+VON). The DC Voltages On (+VON) signal originates at the front panel switch of the SPU. It turns the DC outputs on and off. When the switch is in the power-off state, the signal looks like a contact closure to ground. When it is in the power-on state, it looks like an open circuit pulled up to +5B. A 5k ohm pull-up resistor to +5B is provided within the power supply. At this point, +5B is fed by the battery charging circuit. Therefore, the battery does not need to be operational to power on the system. When +VON is set true, a one-second delay occurs before all DC voltages reach their nominal levels, if the required load (1.5A minimum) is on the output.

Battery Backup Mode (-BBK). The Battery Backup Mode (-BBK) line is a TTL logic signal that is set low when the power supply is in the Battery supply mode. This mode occurs when AC power is lost to the power supply (-PSW is low) while DC power is on (+VON is high). If AC power returns before the battery capacity is depleted, the line is set high and all power supply output voltages automatically return to normal.

Power System Timing

Figure 5-2 is a timing diagram of the power system. The true condition on this diagram is the high state.

If the AC line voltage drops, power to the battery charger circuit also drops. Twenty milliseconds later, the Power Supply Warning line (PSW) and the Battery Backup line (BBK) are set true. This indicates that an AC line failure has occurred. The PSW line will remain true for a minimum of 500 microseconds. It can remain true indefinitely. The DC voltages will remain within the specified tolerances for a minimum of three milliseconds after the PSW line is set true.

If an overtemperature condition exists and the OTS line is set true, the DC voltages will remain within the specified tolerances for 0. 5 seconds.

Signal Line Characteristics

It is important that no pull-up resistors or other impedance be placed on the -PSW or +VON signal lines. This would cause the signals to appear to be at a logic low state when the power supply is turned on. Any external impedance will prevent the power supply from turning on. The electrical characteristics of the signal lines are defined below.

SIGNAL	MAXIMUM VOLTAGE	MAX. SINK CURRENT
-PSW	5.25	-10mA
-OTS	5.50	-10mA
-OTW	5.25	-10mA
+VON	5.50	+0.55mA
-BBK	5.25	-10mA

NOTE: Signal current is designated (-) into the power supply and (+) out of the power supply. Signal state is designated (-) low true and (+) high true.

Interface Connector Pinouts

The pinout configuration for the power supply to the computer backplane connector is shown below.

PIN	LEVEL	PIN	LEVEL	PIN	LEVEL
1	+12V	9	GND	17	+5SR**
2	+5B	10	+5V	18	-BBK
3	-12V	11	+5V	19	-OTS
4	+5B	12	+5V	20	-OTW
5	GND	13	+5V	21	-BATT
6	GND	14	+5SNS*	22	+BIAS
7	GND	15	-PSW	23	+BATT
8	GND	16	+VON		

* +5 volt sense line

** +5 volt sense return line

Power Supply Diagnostic Tools

A Load and Detection board is available as part of this product. When this board is plugged into a backplane slot, it provides the minimum load on all backplane output voltages (+5v, +5B, -12V, and +12V). The board has a voltage indicator LED for each backplane voltage. It also has two ground test

LESSON 5 QUIZ

1. Which of the following statements correctly describe the power supply?

   a. The maximum input current is 4 amperes at 110 VAC.

   b. AC input overvoltage protection is achieved with a resetable breaker switch and fuse.

   c. DC overvoltage protection is achieved by means of a crowbar circuit.

   d. A DC overcurrent condition is recoverable for all outputs, except +5v, by simply removing the cause.

   e. A DC overcurrent condition on +5V latches off all output voltages.

   f. A fault condition occurs if overvoltage, +5V overcurrent, or overheating conditions occur.

   g. A fault condition recovery is completed only by cycling the ON/OFF switch.

   h. The battery charger maintains a 7.2V output to the back-up battery at all times if AC power is applied.

   i. When in the battery backup mode, the battery is taken out of the circuit by a relay if its output drops below 5.5 VDC.

   j. A 5A 250V fuse is used in both 115Vac and 230Vac operation.

2. Describe the use and operation of each of the following control signals.

   a. -PSW (Power Supply Warning) LINE V > MIN OPT V
      ALL DC V's IN SPEC

   b. -OTW (Over Temperature Warning) @ 45°C OTW ON

   c. -OTS (Over Temperature Shutdown) @ 60°C OTS

   d. +VON (DC Voltages On) on FNT PNL → Allows P.S to come-up

   e. -BBK (Battery Backup Mode) $-\overline{PSW}$ · VON →

3. List the tools provided with this product for diagnosing the power supply.
   LOAD & DETECTION BD.

Answers in Appendix C.

POWER SYSTEM LAB

The following equipment is required for this lab:

A Series 37 SPU

A supported terminal

A digital voltmeter

A Load and Detection board

1. Remove the power supply from the card cage and locate the line voltage select switch. Note its position. Locate the input line fuse and the two temperature sensors. Remove the fuse and verify continuity with a digital voltmeter. If the fuse is OK, reinstall it. If not, replace it. Measure the resistance of both of the temperature sensors. (They should have high impedance.)

2. Power on the Series 37 SPU (keyswitch in positions 1, 2, or 3) and disconnect the power cord. This simulates an AC power failure and forces the system into the battery back-up mode. Note the state of the front panel indicator LEDs. They should be in the following states:

```
AC - off
DC - off
BATTERY - on
RUN - off
REMOTE - off
```

3. Measure -BBK, -PSW, and +VON on the power supply backplane connector.

4. Plug in the AC cord. Note that the system should return to the typical powered on state. It should run Power-on Selftest.

5. With the SPU powered on, measure and record the voltages of the following signals at the power supply backplane connector:

-PSW
-OTS
-OTW
+VON
-BBK
+5V
+5B
-12V
+12V
+BIAS
+5 SENSE
+5 SENSE RETURN
-BATT
+BATT

6. Apply AC power to the Series 37 SPU. Set the keyswitch to the 0 position. Record the states of the

indicators on the display panel.

7. Turn the keyswitch to a DC ON position. Record the states of the indicators on the display panel.

8. With DC power applied, disconnect the AC power cord and record the status of the indicators on the display panel.

9. Turn the keyswitch to the 0 position and record the states of the indicators on the display panel.

10. Wait a few seconds and return the keyswitch to a DC ON position. What happens?

11. What can you conclude about the operation of the Series 37 SPU?

12. Remove the AC power cord. Remove all of the boards in the card cage. Install the Load and Detection board into one of the lower card cage slots. Reconnect the AC power cord. Turn on the DC power. Record the states of the LEDs on the Load and Detection board. Measure all of the voltages at the test points on the Load and Detection board.

Turn off the DC power. Remove the AC power cord and the Load and Detection board. Reassemble the SPU.

Answers in Appendix C.

Synchronous Intermodule Bus (SIMB)

Lesson 6

OVERVIEW

This lesson describes the function of the SIMB in the SPU, the SIMB signals, the function of the Bus Monitor, and a brief overview of the I/O system.

LEARNING OBJECTIVES

When you have successfully completed this lesson, you will be able to:

- Match backplane slot numbers with channel numbers.
- List the features of the SIMB and the I/O structure.

INTRODUCTION

The SIMB is a fully synchronous backplane for communicating between the CPU, I/O, and one or more memory modules. The SIMB provides the necessary control, parity checking, and data transfers to the processor.

The SIMB is similar to the Intermodule Bus (IMB) used in the HP 3000 series 30/33, 40/44 and 64 computers. It provides enhanced performance, increased reliability, and simplified interface requirements. The Bus Arbitrator of the IMB is replaced by a Bus Monitor.

The SIMB has the following characteristics:

32-bit data bus
28-bit address (512 megabyte addressability)
fully synchronous operation
extensive error detection
supports interleaved memory

SIMB Signal Description

The SIMB signal groups are summarized below. There are 107 signal lines and 30 additional lines for power distribution. There are:

3 Opcode lines
28 Address lines
32 Data lines

8 Parity lines
8 FROM lines

Handshake lines
-ACCESS
-MEMBUSY
-CHANBSY
-GLOBAL
–MEMREQ

Interrupt lines
-CSRQ
-IRQ

Status Lines
PON
-PFW
-PER (Channel Address/Data Parity Error)
-MER (Memory Uncorrectable Data Error)
-DNV (Data Not Valid)

Priority Lines
Seven-line priority tree for channels and CPU
(4 PRI, 1 PRO, CARRY IN, CARRY OUT)

Two-line daisy-chained priority tree for memory modules
(1 PRI, 1 PRO)

One line for memory to hold off all channels and CPU

Channel Identification Lines

Four lines that assign unique channel numbers to each slot

Clock Lines

One asymmetrical master clock
One symmetrical double-speed clock

Power Supply Support Lines

VON
-PSW
-OTS
-OTW

Opcode Lines

The three OP lines (-OP0 through -OP2) indicate the operation being performed on the SIMB. The OP lines must be asserted during the same clock cycle the -ACCESS line is asserted. The same module must assert both the OP lines and the -ACCESS line. The valid opcodes are:

000 Memory Read Word
001 Memory Write Word (16 bit)
010 Memory control/Read Status
011 Memory Write Word (32 bit)

100 I/O Read
101 I/O Data
110 I/O Write
111 Memory Data

Address Lines

The address lines (-ADDR04 through -ADDR31) make up the 28-bit address bus. The most significant bit is 04 rather than 00 to maintain proper bit alignment between the data lines and the address lines.

The following bit assignments are used for memory addressing.

BITS	4-7	8-15	16-31
	not used	bank address bits	memory address

The following bit assignments are used for I/O commands.

BITS	16-19	20-23	24-27	28-31
	Command	K field number	Path number	Channel

Data Lines

The data lines (-DATA00 through -DATA 31) make up the bi-directional 32-bit data path for the SIMB. Bit 00 is the most significant bit. Bit 31 is the least significant bit.

Parity Lines

The parity lines that correspond to the address lines are PA0 through PA3. The parity lines that correspond to the data lines are PD0 through PD3

Module From Lines

The Module From lines are FRMCHN0 through FRMCHN3 and FRMPTH0 through FRMPTH3. The From lines identify which module is on the bus during an access. They are asserted by the module. The FRMCHN lines contain the four bits that correspond to the channel number of the card. The FRMPTH lines contain the four bits corresponding to the path on the card that is accessing the bus.

Handshake Lines

The -ACCESS line is asserted whenever the bus contains data that must be acted upon by a module, such as the CPU, memory, or channel. The line can be held true for only one cycle. This increases the bus bandwidth.

The -MEMBUSY line is asserted by memory when it cannot accept another Read or Write. All memory modules share the same -MEMBUSY line. If one module is busy, it will hold off accesses by the other modules.

If the -CHANBSY line is asserted, a channel cannot accept an incoming command from the CPU. If the channel is in this state, it must assert -CHANBSY during the cycle immediately following the ACCESS cycle containing the command. The CPU must wait at least one cycle before retrying the command. It must continue to retry the command until the channel stops asserting -CHANBSY.

The -GLOBAL line is asserted by the CPU whenever it is sending a global I/O command across the SIMB. The -GLOBAL line holds off accesses by memory or channels during a global operation, which is the only multi-clock operation that takes place on the SIMB.

Interrupt Lines

The interrupt lines are synchronized by the CPU. The Channel Service Request line (-CSRQ) is asserted by a channel whenever it wants the Channel Program Processor to start or abort an I/O transfer.

The Interrupt Request line (-IRQ) is asserted by a channel whenever it wants to interrupt the CPU to indicate that an I/O transfer has been completed or aborted.

Status Lines

The Status lines are PON, -PFW, -PER, and -MER. The Power On line (PON) is asserted by the Bus Monitor at least 20 milliseconds after power is applied to the system. The Power Fail Warning line (-PFW) is asserted by the Bus Monitor at least eight milliseconds before power drops below minimum operation level margins. The Parity Error line (-PER) is asserted by the Bus Monitor during the cycle immediately following the ACCESS cycle in which a parity error was detected. If a module detects a parity error on a transfer, it must abort its I/O and request service from the CPU by asserting the -CSRQ or -IRQ lines. The Memory Error line (-MER) line is asserted by memory whenever it encounters an uncorrectable data error. The Data Not Valid line (-DNV) is asserted by the channel if it cannot complete an I/O command.

Priority Lines

There are eight Priority lines. They are -PRI0 through -PRI3, -PRO, -MEMPRO, -MEMPRI, and -MEMREQ. There are two sets of priority lines in the system. One set is for memory and the other set is for the CPU and the channels. Memory needs its own set for two reasons. Memory must have overriding priority over all other modules to ensure that it can put Read data on the bus for a requesting module. The SIMB supports multiple memory controllers so a mechanism is implemented so the multiple controllers have priority among themselves.

The memory priority structure consists of a two-wire daisy-chained tree with an extra line to hold off all other modules when memory is on the bus.

A memory controller that needs the bus asserts its PRO line and -MEMREQ line one cycle before it requires the bus.

The Priority lines -PRI0 through -PRI3 are used to arbitrate between the channels and the CPU. The CPU has the lowest priority. The priority of the channels increases the farther they are physically from the CPU. When the I/O Extender is added, the cards in the SPU have the highest priority.

Channel Identification Lines

The four Channel Identification lines, -ID0 through -ID3, are used to assign unique channel numbers to each slot.

Clock Lines

Two clock lines are used in the SIMB. The CLOCK line is an asymmetrical 170 nanosecond master clock. The 2XCLK is a double-speed clock used by high speed sequencing logic, such as a memory controller.

Power Supply Support Lines

The two Power Supply Support lines, VON and -PSW, are used only by the Bus Monitor.

The VON line is used in multiple-SIMB systems with separate power supplies. The master supply brings the slave power supplies up and down with the VON line. The -PSW line is the status line from the power supply to the Bus Monitor.

Bus Monitor Description

The Bus Monitor oversees the operation of the SIMB. It is physically located on the CPU. The Bus Monitor is responsible for:

- Providing clock signals to the backplane
- Checking for parity on the SIMB
- Intercepting the -PSW signal from the power supply and synchronize the PON and -PFW signals.

Bus Request Logic

Before any module, such as the CPU, memory, or channel, can access the SIMB, the module must first issue a request to itself. If the module is the highest priority module requesting the SIMB, it will be allowed to assert the Priority Out lines (PO), which will disable lower priority modules from getting service. Once the requesting channel controls the bus, the following events and signals occur:

-ACCESS is asserted whenever the bus contains valid data that must be acted upon by a module. The op code and the data on the address bus and the data bus must be valid. Data and addresses can only be transferred during the Access cycle.

-MEMBSY is an OR-tied line that is asserted whenever memory cannot accept another Read or Write request. When a channel detects -MEMBSY during an access, it must wait and retry the Access operation after -MEMBSY is deasserted.

-CHANBSY indicates that a channel cannot accept an incoming command from the CPU. If the channel must assert -CHANBSY, it must do so during the Access cycle. The CPU must then wait until the next Access cycle to retry the command.

-GLOBAL is asserted by the CPU whenever it sends out a Global command. The -GLOBAL line holds off accesses by memory or the channels.

-FROM lines. The eight FROM lines are asserted by the module that is on the bus during the Access cycle. The lines identify the module on the bus. The memory controller latches all eight bits during a memory access. They identify the channel that matches the request for either returned data on a Read operation or for error reporting.

Parity Lines PA0-3 and PD0-3. Even parity is used. This means that an undriven bus will have undriven parity. All parity bits must be valid during the Access cycle. Table 6-1 shows the parity bits associated with the corresponding op code, address, and data bits.

Table 6-1. Parity Bits and Op Code, Address, and Data Bits

PA0	Opcode 00-02 and Address 04-07
PA1	Address 08-15
PA2	Address 16-23
PA3	Address 24-31
PD0	Data 00-07
PD1	Data 08-15
PD2	Data 16-23
PD3	Data 24-31

Bus Priority

The SIMB utilizes a priority tree structure to determine which module is allowed access to the bus. In the CPU card cage, slot 1 (channel 1) has the highest priority. Slot 5, which is reserved for the CPU PCA, has the lowest priority. PCAs in the SPU have a higher priority than those in the Extender. In the Extender, the lowest channel number has the highest priority. Figure 6-1 shows the channel numbers associated with the slots.

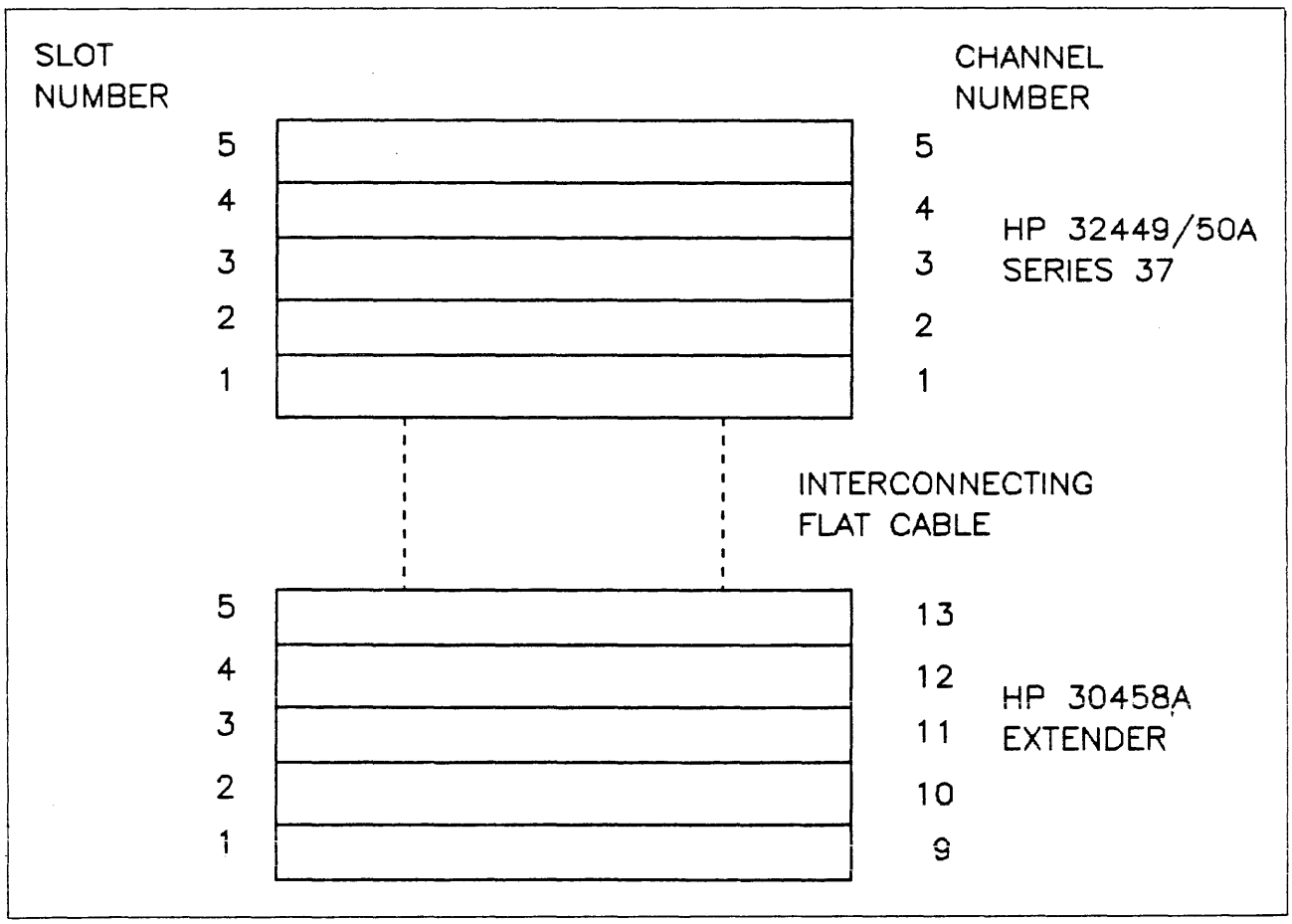

Figure 6-1. SPU/Extender Slot/Channel Assignments

I/O System Overview

The Bus Monitor description identifies the unique characteristics of the SIMB that distinguish the Series 37 machine from the HP3000 machines that use the IMB. Most of the other aspects of I/O operation are identical. A summary of the major functions are listed below.

Channel Program Execution

Nearly all transactions with I/O devices are accomplished without software interrupts because the I/O interface is accomplished with channel programs. Software is responsible for setting up a channel program. The execution of this program is performed by the CPU's microcode. The CPU's channel microcode is devoted to I/O tasks. It implements the necessary algorithms for decoding the channel instructions and executing the required I/O operations. Once the channel program is running, device control and data flow are normally carried to completion with no software intervention and without altering the system environment. If special situations arise, software may alter the channel program or halt its execution.

The execution of a channel instruction generally results in several transactions with a channel. It is necessary to specify several IMB commands in order to communicate the desired action to the channel. When the SIMB operation is related to I/O rather than memory, as defined by the bus opcode, the SIMB Address bus has the following format:

4 - 15	Not used
16 - 19	I/O Command. This identifies the function the channel is to perform. The bus opcode determines whether the operation is a Read or Write.
20 - 23	K Field. Selects the desired register on the I/O channel.
24 - 27	Path number. This is normally zero. Paths will be used on future I/O boards to identify and communicate with a second channel on that board. For example, the channel number would identify the card and the path number would identify one of the two channels on the card.
28 - 31	Channel number.

I/O Usage and Interrupts

The I/O interrupt system provides the means for devices and channels to request service. The request facilities are described below.

Channel Program Service Request (CSRQ). The CSRQ is an OR-tied line on the SIMB that channels assert to request channel program service for devices. Priorities may vary from channel to channel between assertions of CSRQ. For the PIC, the following conditions will generate a CSRQ:

DMA Terminates
Parallel Poll (from a device)
ABI Interrupt (HP-IB processor chip on the PIC)
Request to start or halt a channel program
Time out condition
DMA Abort (due to an error condition, SIMB parity error, double-bit memory error, etc.)

Interrupt Request. IRQ is an OR-tied line on the IMB that is connected to the CPU and all I/O channels. It is asserted to generate a CPU external interrupt request. Device and channel conditions requesting service will first have the channel assert CSRQ. The CSRQ microcode will determine whether a software interrupt is required.

Parallel Poll

The general HP-IB standard allows devices to request service in two ways:

Parallel Poll Request. Each device connected to the HP-IB is assigned one of the eight data bits to assert to indicate a positive response to the poll.

When no other operations are being performed on the HP-IB, the channel sets the bus to a paralled poll state (ATN and EOI are asserted). Devices must assert a logical 1 on their assigned data line to request service. The PIC examines the response and issues a CSRQ for the highest priority device requesting service.

LESSON 6 QUIZ

1. How do devices connected to the HP-IB request service?
   Polling on their respective DATA line (parallel pole)
2. What are the two ways in which channels request service?
   CBRQ & IRQ
3. The SIMB requires all data and addresses to be valid during the Access cycle.

4. If the TIC attached to the system console and another non-memory PCA simultaneously request access to the SIMB, which of the two PCAs will be granted access first? Why?
   TIC it has highest priority
5. Which of the SIMB buses is used to send I/O commands to I/O channels?

6. How are channel numbers assigned in the Series 37 SPU?
   1-5 w/ 5=CPU low pri 1 = highest pri.
7. What signal lines are used to determine the channel numbers?
   ID Ø → ID3

Answers in Appendix C.

How the Series 37 SPU Works

Lesson 7

OVERVIEW

This lesson describes the functions, logical blocks, and major signals of the Central Processor Unit (CPU) PCA, the Memory PCA, the Peripheral Interface Controller (PIC) PCA, and the Terminal Interface Controller (TIC) PCA. Figure 1-1 is a simplified block diagram of the SPU. It shows how the PCAs discussed in this lesson work together.

OVERALL LEARNING OBJECTIVES

When you have successfully completed this lesson, you will be able to:

- Describe the basic functions of each of the major assemblies.
- Identify the card configuration.
- Describe the basic interface characteristics, such as cabling and baud rates.
- Identify the major diagnostic tools for each of the major assemblies.

Control Store

The Control Store consists of ROMs and RAMs to store the microinstructions. It also contains a state machine to control reading and writing the storage elements. The RAMs make up the Writeable Control Store (WCS). There are 2k by 64 bits of fast RAM and 8k by 64 bits of slow RAM. The Control Store also contains 8k by 32 bits of ROM.

ROM is used to store Power-on Self-test, the Maintenance Mode code, and the Initial Microcode Loader (IML). The micro-instructions, used to execute the HP3000 instruction set, are loaded and stored in RAM using the IML. High usage micro-routines are stored in fast RAM.

The Control Store is activated via the state machine and processor micro-instruction fetch hardware. The access time for fast RAM is one clock cycle or 170 nanoseconds. The access time for slow RAM is two clock cycles or 340 nanoseconds. ROM access time is eight clock cycles or 1360 nanoseconds.

Register File

The Register File consists of 256 16-bit wide registers implemented in two fast static RAMs. 240 registers are used for temporary storage during microcode execution. Sixteen registers are used for external interfaces, such as Bank, Status Display, Interrupt Vector, Control Store Word 0 through 3, Maintenance Panel Interface (MPI), MPE Timer, Operand A and B, and Time of Century (TOC).

Register file access is controlled solely by microcode. Access time is one clock cycle - 170 nanoseconds.

Time of Century (TOC) Clock

The Time of Century (TOC) clock is a battery backed up real-time clock that runs continuously whether the system is powered on or not. The TOC provides calendar time from ten thousandths of seconds to months. The clock is used by a subsystem to determine calendar time. It provides RAM storage of LOAD, START, and DUMP channel and device numbers for use by the Initial and Dump subsystems. It also provides TOC test and control registers, and system status storage in RAM. The contents of the TOC RAM locations can be displayed when the system is in the maintenance mode.

TOC RAM LOCATION	CONTENTS
8	Not used
9	Year information
10*	LAST-HALT information
11	Warmstart channel and device number
12	Coldload channel and device number
13	Not used
14	Not used
15	Not used

*See next page.

TOC RAM location 10 (address 01010) is reserved for microcode use. The contents of the location identify the last reason for a system halt and help determine if a power-fail recovery should be attempted. The values 00 through 14 indicate that a hardware failure has occurred in the SPU. The values $7F and $80 indicate that the system has been halted because of a software fault.

The contents of byte 10 in the TOC are defined below.

VALUE	INDICATION
00-0F	System last stopped with a HALT00 through HALT15 instruction.
10	System last stopped due to a WCS parity error.
11	System last stopped due to a SIMB parity error.
12	System last stopped due to a double-bit memory error.
13	System last stopped due to an out-of-bounds memory address.
14	System last stopped due to a watchdog timer timeout.
15-7E	Reserved for future failure modes.
7F	MPE UP status removed by software. Disables power-fail auto-restart and enables auto-warmstart.
80	System was running MPE or other software. Enables power-fail auto-restart and disables auto-warmstart.
81-FF	Unused. May contain random power-up pattern.

The TOC chip is accessed and controlled by microcoded Register File Read and Write operations.

Interrupt Process

The CPU and the microcode process interrupts on an immediate basis or on a polled basis. Immediate interrupts force microcode execution to jump to the microcoded interrupt handler at the completion of the current micro-instruction. Polled interrupts are serviced between the execution of machine instructions. At that time, microcode execution jumps to the microcoded interrupt handler.

The interrupt handler fetches the interrupt vector from the register file and uses priority decoding to determine which interrupt to service. The immediate and polled interrupts are listed below.

IMMEDIATE

Maintenance Panel Interrupt
WCS Parity Error
Warmstart (includes Control-B sensed by TIC at channel 1)
Multi-bit Memory Error
SIMB Parity Error
Watchdog TImer Error

POLLED

Memory Bounds Violation

Data Not Valid (DNV) from PIC
Channel Service Request (CSRQ)
Interrupt Request (IRQ)
Interrupt Timer
Overtemp Warning
Overtemp Shutdown

Synchronous Intermodule Bus (SIMB) and Monitor

The SIMB provides all necessary bus control and data transfers transparent to the processor. Data transmitted and received across the SIMB for the processor is stored in the operand locations of the Register File. Refer to the Synchronous Intermodule Bus (SIMB) description for more detailed information.

The Bus Monitor oversees the SIMB. It provides clock signals to the backplane. It checks parity on the SIMB.

The Monitor circuitry is physically located on the CPU board for packaging convenience. It is not a functional part of the CPU.

Power Supply Monitor (PSM)

The Power Supply Monitor (PSM) provides the +PON and -PFW signals for system initialization and MPE power fail/recovery routines. The PSM receives a power supply warning signal (-PSW) from the power supply when the AC voltage has been below a limit for a specified length of time. The -PFW signal is then asserted. The PSM waits approximately three milliseconds for the system to execute power fail housekeeping and then deasserts the +PON line.

Status Display

The Status Display consists of a one-digit hexadecimal dot matrix LED that displays self-test status and the progress of coldload execution. The Status Display also consists of five indicator LEDs that indicate CPU activity, remote console active, AC power on, DC power on, and Battery Backup mode.

The dot matrix LED is controlled by Write commands to a Register file location.

The indicator LEDs are controlled by signals from the power supply, the CPU, and the keyswitch. The indicator LEDs are controlled by the following signals.

RUN	LED intensity is proportional to the Channel Service Request (CSRQ) frequency.
DC	LED is controlled by the +5V signal.

AC	LED is controlled by the AC BIAS signal from the power supply.
BATTERY	LED is controlled by the +5B signal and the -BBK signal.
REMOTE	LED is controlled directly by the -REMACTIVE signal from the TIC and indirectly by the -REMOTE signal from the keyswitch.

MPE Timer

The MPE timer circuit is used by the operating system for accounting and timing purposes, such as I/O timeouts. The timer is controlled and accessed by microcode Write and Read operations to Register File locations.

Bank Register

There are four 16-bit registers that provide the five most significant bits for memory addressing. These five bits are the bank address.

CPU Diagnostic Tools

The following diagnostic tools are available with this product for diagnosing CPU problems.

1. PON Selftest
2. Maintenance Mode Selftest - CPU test

CPU Quiz

1. Which of the following statements correctly describe the CPU?

   a. The processor is a one-chip gate array that utilizes a pipeline micro-machine architecture.

   b. The clock cycle is 190 nanoseconds.

   c. Processor performance is 0.25 MIPS.

   d. Control Store consists of both writeable and read-only storage.

   e. Power-on Selftest, the Initial Microcode Loader and the Maintenance Mode Code is RAM based.

   f. All interrupts are processed on a priority polled basis.

   g. The SIMB, SIMB Monitor, and Power Supply Monitor circuitry do not perform CPU functions but reside on the CPU board.

2. The TOC clock is used to keep real time and to store important system startup information under battery backup. (True or ~~False~~)

3. How can information obtained from TOC RAM location 10 (LAST-HALT information) be used to diagnose a system problem? By Decoding contents the LAST HALT will show up

4. What is the function of the Power Supply Monitor?
   PON & PPW
5. How is the hexadecimal LED status display used?
   Show Self Test Status
6. Give the name of the signal directly controlling each of the following front panel indicator LEDs.

   RUN CSRQ

   DC +5VDC

   AC AC BIAS

   BATTERY $\overline{BBK}$ + (+5B)

   REMOTE Rem Active + Remote Key

7. List the tools provided with this product for CPU analysis.
   PON test
   CPU self test MAINT mode

MEMORY BOARD DESCRIPTION

Learning Objectives

When you have successfully completed this portion of this lesson, you will be able to:

- Describe the major memory functions.
- Identify all major components and special components.
- Identify the available diagnostic tools.

General Description

The memory boards interface to the Synchronous Intermodule Bus (SIMB). Each memory board is made up of a controller and an array on one board. Each array contains 512k bytes using 64k RAMs. The memory system supports both a 16-bit and a 32-bit data bus. Each board in the memory system inspects 28 address bits and responds to an address range based on its identification code. The identification code is the same as the channel number. Up to two boards can be installed in the system. If two boards are installed, the memory is interleaved, resulting in improved performance. The memory system can buffer a maximum of two memory requests, which results in improved performance. These two requests are Access A and Access B. There are seven functional blocks in a memory board. See figure 7-2 for a functional block diagram of the memory board.

Memory Array Section

Each memory array on a board is made up of two blocks - 0 and 1. Each block is made up of a data array (MRAY) and a check bit array (CKRAY). Each block is driven by one set of RAS and CAS lines. Each MRAY has 32 RAM chips. Each CKRAY has seven RAM chips. Therefore, each board has a memory array consisting of a total of 78 RAMs. In each case, one chip represents one data bit or check bit. Write and Read operations require an average of four cycles per word for execution.

See figure 7-3 for the physical arrangement of the RAMs and their block and bit assignments.

Address Section

The Address section, MEMADD, holds address information from the backplane until memory can use it. At that time, it issues the address information to the array and the Control section. It also keeps track of memory refresh.

The Address section of the Memory board is made up of five elements. They are the Address registers, the FROM registers, a FROM code parity generator, the Refresh counter, and the RAS/CAS multiplexer.

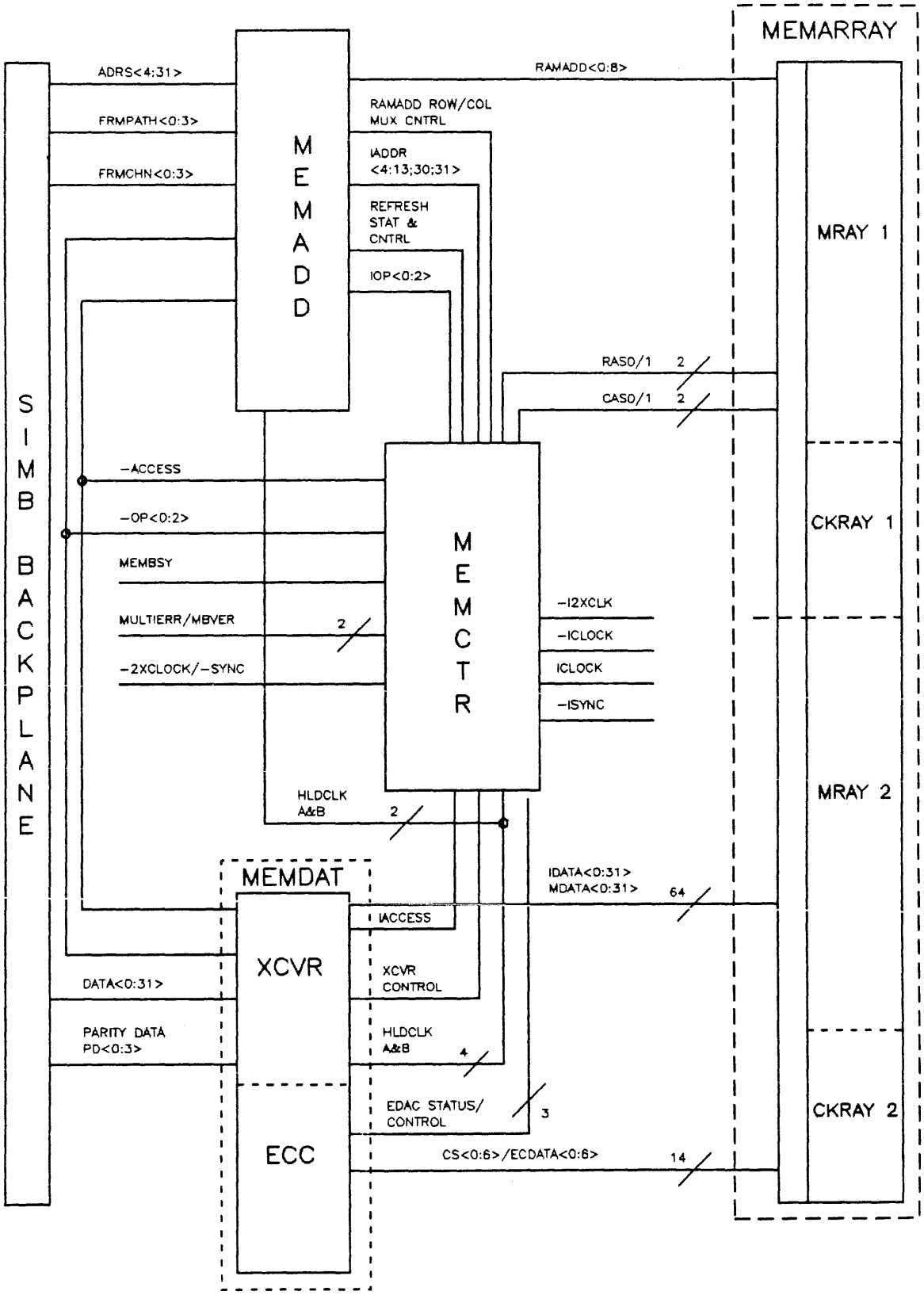

Figure 7-2. Memory Block Diagram

U1002 0/0	U902 1/0	U802 0/8	U702 1/8	U602 0/16	U502 1/16	U402 0/24	U302 1/24	U202 0/C0	U102 1/C0
U1003 0/1	U903 1/1	U803 0/9	U703 1/9	U603 0/17	U503 1/17	U403 0/25	U303 1/25	U203 0/C1	U103 1/C1
U1004 0/2	U904 1/2	U804 0/10	U704 1/10	U604 0/18	U504 1/18	U404 0/26	U304 1/26	U204 0/C2	U104 1/C2
U1005 0/3	U905 1/3	U805 0/11	U705 1/11	U605 0/19	U505 1/19	U405 0/27	U305 1/27	U205 0/C3	U105 1/C3
U1006 0/4	U906 1/4	U806 0/12	U706 1/12	U606 0/20	U506 1/20	U406 0/28	U306 1/28	U206 0/C4	U106 1/C4
U1007 0/5	U907 1/5	U807 0/13	U707 1/13	U607 0/21	U507 1/21	U407 0/29	U307 1/29	U207 0/C5	U107 1/C5
U1008 0/6	U908 1/6	U808 0/14	U708 1/14	U608 0/22	U508 1/22	U408 0/30	U308 1/30	U208 0/C6	U108 1/C6
U1009 0/7	U909 1/7	U809 0/15	U709 1/15	U609 0/23	U509 1/23	U409 0/31	U309 1/31		

Figure 7-3. Memory RAM Location Diagram

Data Section

The Data section is organized so that either 16-bit or 32-bit bus transactions can take place. Data is accepted and output from the SIMB by six registers for Access A and six registers for Access B.

The Data section, MEMDAT, is made up of three elements - the Read/Write Data transceivers, the Error Correction circuit, and the Data Parity Generator.

The Error Correction circuitry is located on one chip. The Error Detection and Correction (EDAC) chip corrects single-bit errors and detects multiple-bit errors. Under certain error conditions, some error patterns with more than two incorrect bits will not be detected.

The Data Parity Generator generates four parity bits. One bit is associated with each byte of a 32-bit word in memory. Note that data is organized on a 32-bit basis in memory and on a 16-bit basis in the rest of the system.

Control Section

The Control section determines if an A-Access or a B-Access is being done. It also phases in the Refresh function, provides the timing for the RAMs, and generates all of the control signals for the latches and buffers on the board. The signals are also used for initiating error correction.

The Control section also determines if the address referenced by a pending request resides on the board under its control, the other board, or none of the boards (a memory bounds violation). When two memory boards are installed, the memory system is automatically interleaved. The memory assignments for each board are such that when sequential accesses of memory are made, the accesses switch between boards after each pair of words. Therefore, when interleaved, board selection is controlled by bit 30 of the address. Note that bit 31 is the least significant bit.

The control signals for the latches, buffers, and error correction are implemented in Programmable Logic Arrays (PLA). There are four PLAs in the system.

Memory Operations

The memory operations are controlled by the opcodes. The functions associated with each memory op code are shown below:

OP CODE	ADDRESS BIT 31	FUNCTION
0	do not care	Read (16-bit)
1	do not care	Write (16-bit)
2	0	*Read error latch
2	1	*Write (16-bit) with old check bits and return new check bits
3	0	Write (32-bit) to initialize check bits
3	1	*Write (16-bit) with old check bits

* Functions performed for diagnosis

Read (Opcode = 0)

If a Read operation is specified, data is input into the 32-bit MDATA latch. The data is then put on the IDATA bus. If no errors are detected, then IDATA is latched onto the data bus (DATA) of the SIMB. Only bits 0 through 15 are read by the SIMB. How the data is latched is controlled by the value of address bit 31.

If address bit 31 is set to 0, the upper 16 bits (0 - 15) of memory are mapped into the upper 16 bits (0 - 15) of the SIMB.

If address bit 31 is set to 1, the lower 16 bits (16 - 31) of memory are mapped into the upper 16 bits of the SIMB.

Write (Opcode = 1)

If a Write operation is specified, data is transferred in the opposite direction from that of the Read operation - from the SIMB to the MDATA latch.

Refresh

Refresh is accomplished with a divide-by-100 counter. A Refresh operation takes place every 99 cycles. Each refresh operation increments a refresh counter, which rolls over every 256 counts. A 64k RAM is refreshed every two milliseconds for seven address lines.

Initialization

Before memory can be accessed in a normal manner, a 32-bit Write (opcode 3) operation must be performed to every memory location. This sets the correct syndrome bits for each memory location.

Memory Logging

Memory logging is a facility that allows MPE to create a file of the most recent memory errors. A single-entry error latch in memory is read by MPE every 10 minutes. Unlike the other HP 3000 systems, the Series 37 cannot save data about more than one error. It can only save the most recent error in the error latch. This facility uses the following programs:

Memory Error Logging Process (MEMLOG)
Memory Log Analysis Program (MEMLOGAN)
Memory Error Logging Interval Update Program (MEMTIMER)

Refer to the MPE System Utilities Reference Manual for user interface information. The format of each entry in the file created by MPE is shown below.

```
-------------------------------------------------
|       ADDRESS       |  ERROR TYPE     |  ERROR  |
-------------------------------------------------
| BOARD  |   ROW    |  TYPE BIT CHIP  |  COUNT  |
-------------------------------------------------
```

BOARD — The board ID number is displayed as 0 or 1. Board 0 resides in slot 2 and board 1 resides in slot 3.

ROW — This identifies the row in which the faulty RAM is located. It is not displayed if there is a multiple bit error.

TYPE — Type of error detected. They are:

Check - Check bit error

Data - Data bit error

Multiple bit - Error in more than one bit error

If a multiple bit error is indicated, no bit or chip information is given.

BIT	If TYPE = Check, BIT indicates the failing check bit (0 through 6). If TYPE = Data, BIT indicates the failing data bit (0 through 31).
CHIP	Indicates the chip on which the error occurred, in the format Un. The variable n indicates the chip number.
COUNT	The number of logging intervals during which this error was detected at least once. It does not accurately indicate the number of times an error was actually detected.

Memory Diagnostic Tools

The following diagnostic tools are available with this product for diagnosing memory problems.

1. PON selftest
2. Maintenance Mode Selftest - Memory test
3. DUS memory diagnostic (MDIAG37)
4. Memory logging facility

Memory Quiz

1. Which of the following statements correctly describe the Series 37 memory system.

✓a. Each board has a controller and an array section.

~~b.~~ Each board contains 256k bytes using 64k RAMs.

~~c.~~ It only supports a 16-bit data bus.

✓d. Only two memory boards can be supported in each system.

~~e.~~ When two boards are installed, interleaving must be enabled using a hardwired jumper.

✓ f. Performance is improved by interleaving and by the ability to buffer two requests.

2. The Error Detection and Correction (EDAC) chip performs which of the following functions:

✓ a. Detects single-bit errors.

✓ b. Corrects single-bit errors.

✓c. Detects double-bit errors.

~~d.~~ Corrects double-bit errors.

~~e.~~ detects all multiple bit errors.

✓f. Reports detected errors to Error latch.

3. The Error latch can store more than one error at a time. (True or [redacted])

4. The memory logging system logs errors stored in the Error latch at specific time intervals. Therefore, not all errors that have occurred may be logged. (True or [redacted])

5. A memory board responds to specific addresses, depending upon the backplane slot in which it is installed and whether interleaving is active. ([redacted] or False)

6. List the tools provided with this product for Memory analysis.
MDIAG37 , POR1 . . .

Answers in Appendix C.

Memory Lab

1. Run Power-on Selftest with memory installed and note the information displayed on the Selftest LED.

2. Remove the installed memory board(s) and run Power-on Selftest and note how the failure mode is displayed on the Selftest LED.

PERIPHERAL INTERFACE CONTROLLER (PIC) DESCRIPTION

Learning Objectives

When you have successfully completed this portion of this lesson, you will be able to:

- Describe the major functional blocks of the PIC.
- Identify the major differences between the GIC and the PIC.
- Describe the basic functions of the PIC.

General Description

The Peripheral Interface Controller (PIC) PCA is a hardware input/output channel. The PIC interfaces with the Synchronous Intermodule Bus (SIMB). It provides the electrical and functional interface necessary to control and communicate with the byte-oriented devices on the HP-IB. The channel is controlled by standard I/O instructions or by the execution of channel programs.

The PIC is similar to the General Input/Output Controller (GIC) with the following exceptions:

It interfaces with the SIMB and does not support a Channel Program Processor.

It does not have front plane configuration switches.

The PIC acts as an SIMB slave to I/O commands issued on the SIMB by the CPU. It is controlled primarily by reads and writes of its internal registers and cannot autonomously perform any device control sequence over the HP-IB. A Direct Memory Access (DMA) facility can be invoked to assume control of the HP-IB interface during data transfers. Afterwards, control is switched back to the system. DMA performs byte packing and unpacking and operates through the SIMB state machine to reference full words of main memory.

The PIC supports up to eight HP-IB devices with I/O channel programs. The channel acts a controller-in-charge of the HP-IB. To support the devices, there are registers for masking and normalizing parallel poll responses, generating channel program service requests, and generating system interrupts for each device.

Figure 7-4 is a block diagram of the PIC. The PIC is made up of three main blocks They are the:

SIMB interface logic
PIC control logic
HP-IB interface logic

The SIMB interface logic is made up of the bus drivers and receivers necessary to interface the internal circuitry of the PIC with the SIMB. It also consists of the bulk of the priority logic that connects directly to the SIMB.

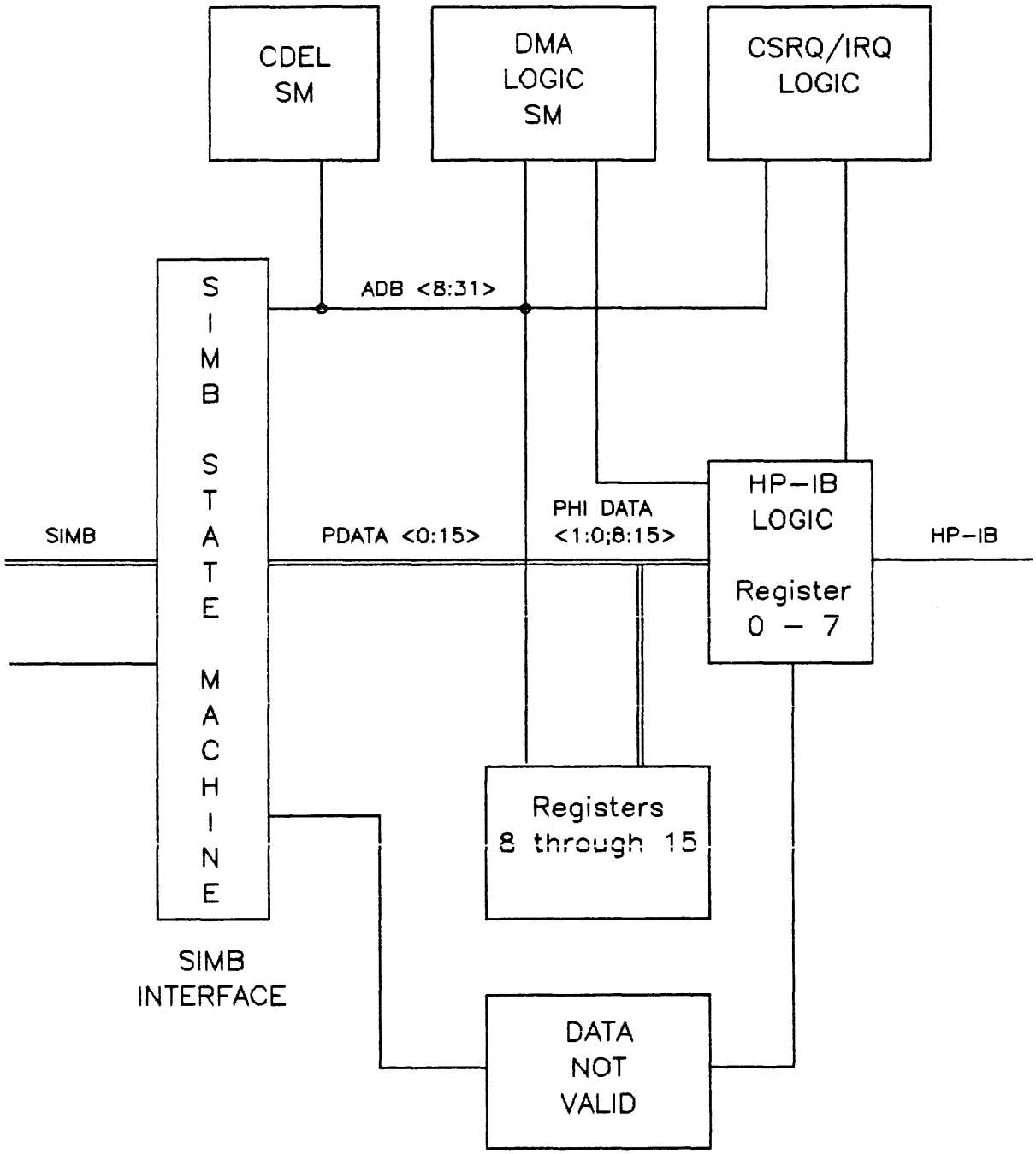

Figure 7-4. PIC Block Diagram

The PIC control logic is made up of four major blocks. They are:

SIMB Control Logic
- SIMB State Machine
- DMA Control Logic
- DMA State Machine

Internal PIC Registers
Command Execution State Machine
CSRQ/IRQ Response Logic

The HP-IB interface logic consists of the Advanced Bus Interface (ABI) chip and the HP-IB transceivers that interface to the HP-IB. The ABI chip is fully compatible with the PHI chip on the GIC PCA. The only difference is that the ABI can generate and perform a cyclical redundancy check (CRC) on HP-IB transfers. This feature will not initially be implemented. To use this feature, both the SPU and the attached peripherals must have this feature enabled.

SIMB Interface Logic

The PIC interfaces the internal circuitry of the PIC with the SIMB. It handles the priority encoding of interrupt and channel service requests for eight devices. It directs Channel Service requests to the CPU. It contains Data-Not-Valid logic to prevent SIMB lock-ups if data is not ready when accessed or if the HP-IB interface is referenced while DMA is active.

PIC Control Logic

The PIC Control logic is made up of four major blocks: SIMB Control logic, Internal PIC Registers, the Command Execution State Machine, and the CSRQ/IRQ Response logic.

SIMB Control Logic

The SIMB Control logic is made up of the SIMB State Machine and the DMA State Machine.

SIMB State Machine. The SIMB State Machine executes data transfers between buffers on the PIC and main memory at the request of the DMA logic. It can also execute data transfers in response to SIMB I/O commands. When the DMA logic requests a memory Read or Write cycle, the SIMB State Machine requests access to the SIMB. If the requested operation is a memory Read, the SIMB State Machine waits for the requested data before notifying the DMA State Machine that the operation has been completed. Otherwise, the SIMB State Machine notifies the DMA State Machine that the operation has completed on the clock cycle after the Access cycle. At this time, the DMA State Machine lowers its Request line.

The SIMB Interface logic also detects errors that occur during the memory cycle. If a bus parity error, memory parity error, or memory bounds violation occurs during a memory request cycle performed by the PIC while DMA is active, a status bit is set in Register B and DMA is aborted.

DMA State Machine. The DMA State Machine is a 20-state synchronous machine that manages data transfers between the HP-IB and memory. It accesses memory via the SIMB after the transfer has been initiated by a sequence of SIMB commands to the PIC.

Internal PIC Requests

There are 16 addressable registers on the PIC. They are used to control the PIC, report status, and configure the channel for sending and receiving data or commands. Control of the PIC is achieved by Read and Write operations to the internal registers.

Command Execution Logic

The PIC Command Execution logic is made up of the SIMB Acceptor logic and the Command Decoding and Execution Logic (CDEL). The SIMB Acceptor logic detects and captures SIMB commands and data that are addressed to the PIC. It signals the Command Decoding and Execution Logic (CDEL) to start when it detects a command addressed to the PIC. The channel number of the PIC is determined by the PIC's physical location in the SIMB backplane. The PIC path number is hard-wired on the PIC PCA to zero.

The Acceptor logic latches the SIMB address, data, opcode and FROM lines at the start of a SIMB transaction. When the command has been executed, the Command Execution State Machine signals the Acceptor logic that the channel is no longer busy and can accept additional SIMB commands.

The CDEL performs two functions. It decodes and executes the SIMB commands. The commands are executed by the Command Decode and Execution Logic State Machine (CDELSM). It is linked to the SIMB State Machine and the DMA State Machine to prevent conflicts and to synchronize the various PIC functions.

CSRQ/IRQ Request Logic

The Channel Service Request (CSRQ) logic generates channel service requests and selects what information is to be returned when the next Obtain Service Information (OBSI) SIMB command occurs. The inputs are:

- DMA activity
- ABI INTERRUPT, CONTROLLER-IN-CHARGE, and DMA REQUEST lines
- Contents of the New Status register
- HP-IB lines ATN and EOI
- Flags to indicate occurrence of OBSI
- Bits 8 and 13-15 in Register B. Bits 13-15 contain the device number.

The Interrupt Request logic (IRQ) is made up of the Interrupt Register and associated logic. The Interrupt Register is a addressable channel register that has one bit per device. A bit is set to queue an interrupt request for that device. When an interrupt request for a device is recognized, its bit in the Interrupt register is cleared by another Write operation to Register C. Device 0 has the highest priority. Note that devices cannot initiate an IRQ. Only channel programs and diagnostic software can set an IRQ for a device. Devices can generate CSRQs if the ABI is configured to interrupt when a parallel poll response is detected on the HP-IB.

Configuring the HP-IB

When the peripherals to be put on the HP-IB channel have been determined, set their Select switches to the unique device addresses. Determine the device address by the order of priority you want for the device.

When the peripherals are configured, they must be interconnected with HP-IB cables and attached to the PIC. HP-IB cables are available in 1, 2, 4, and 8 meter lengths. Refer to the Installation lesson for HP-IB cabling information.

All of the HP-IB devices attached to the system must be powered on when the PIC begins operation. The HP-IB should operate with fewer than half of the HP-IB devices powered off. However, speed will be degraded and maximum transfer rates cannot be guaranteed.

PIC Diagnostic Tools

The following diagnostic tools are available with this product for diagnosing PIC problems.

1. PON selftest
2. Maintenance Mode Selftest - PIC test
3. DUS diagnostic (PICDIAG)
4. DMA Exerciser

PIC Quiz

1. List the three major blocks of the PIC? What are their basic functions?
   SIMB I/F
   HPIB I/F
   CNTL
2. List the major differences between the PIC and the GIC.
   NO FAT PAC config ; I/F to SIMB NOT Supp → Chnl prgm proc
3. Because of its ABI chip, the PIC is not compatible with devices that have PHI chips (true or false).
4. It is not advisable to run the Series 37 SPU with devices on the HP-IB powered off (true or false).
5. What means does the CPU PCA use to control the PIC?
   The PIC acts as a slave to the CPU Thru the SIMB
6. The DMA state machine can read and write single bytes of memory (true or false).
7. Device 7 on the HP-IB is the lowest priority device (true or false).
8. What is the maximum number of devices that a PIC can support?
   8
9. List the tools provided with this product for PIC analysis.
   PIC DIAG ROM CPU test - PIC

Answers in Appendix C.

PIC Lab

The following equipment is required for this lab:

A Series 37 SPU

A supported terminal

1. Enter the Test environment and run one complete pass of Selftest. Record the states of the Selftest LED indicator and the PIC channel address displayed on the CRT.

2. Turn DC power off and disconnect the AC power cord. Remove the PIC from the card cage and reassemble the Series 37 SPU. Repeat step 1 above.

Are there any differences in the results? Explain your findings.

3. Run the slot test and specify channel 4. Write down the results.

4. Turn DC power off and disconnect the AC power cord. Insert the PIC in slot 3. Repeat steps 2 and 3 above.

What conclusions can you make about the PIC and Selftest?

Answers in Appendix C.

TERMINAL INTERFACE CONTROLLER (TIC) DESCRIPTION

Learning Objectives

When you have successfully completed this portion of the lesson, you will be able to:

- Describe the major functional blocks of the TIC.
- Describe the basic functions of the TIC.

General Description

The Terminal Interface Controller (TIC) PCA is a hardware input/output channel that interfaces the Series 37 computer with up to seven asynchronous devices. The TIC is a VLSI version of the Advanced Terminal Processor (ATP), used in other HP3000 computers. The primary difference betwween the two is that the TIC is implemented on one board. It contains the functions of the System Interface Board (SIB) and the Asynchronous Interface Board (AIB). Each TIC can support up to eight devices. Because of limited space on the connector panel, each TIC supports one modem port and six hardware ports.

The standard TIC is shipped with an RS-232 connector assembly. The modem port comes directly from the main TIC assembly and is not affected by either of the plug-in connector assemblies.

The Series 37 computer supports up to four TIC boards. Up to 28 asynchronous devices can be supported. An optional I/O extender is required if more than two TICs are used in the system. Each TIC interfaces to asynchronous devices by means of a connector assembly. The 25-pin D-type connector is permanently attached to the TIC and protrudes through an opening on the rear panel. The TIC plug-in connector assembly is latched to the rear panel and is connected to the TIC by means of a 24-pin AMP-type connector when the rear panel is in place.

The SIB functions on the TIC are contained on a single VLSI gate array chip. This is the MIMI chip. The AIB functions on the TIC are dedicated to supporting the ten Port Controller Chips (PCC). Each TIC has eight ports - zero through seven. Port 6 is not used. Port 7 is the modem port. The system console must be connected to port 0 of the TIC installed in slot 1 (channel 1).

The TIC also contains the Control B Detection and Remote console interface circuitry. The circuitry is enabled only if a TIC is installed in slot 1 (channel 1) of the SPU and if the key switch is in the Local or Remote position.

Functional Description

Figure 7-5 is a block diagram of the TIC. The TIC transmits data between the system and the user terminals by means of direct memory accesses to the terminal buffers in main memory. Each of eight microcomputer chips (Port Controller Chip - PCC) controls one port. Each PCC requests a Memory Read to send data to its port. They request a Memory Write to send data from the port to memory. Upon receiving a special character from its port, the PCC interrupts the system. Two other microcomputer chips, the Modem Controller Chip (MCC) and the Modem Scanner Chip (MSC), control the modem handshake lines for port 7.

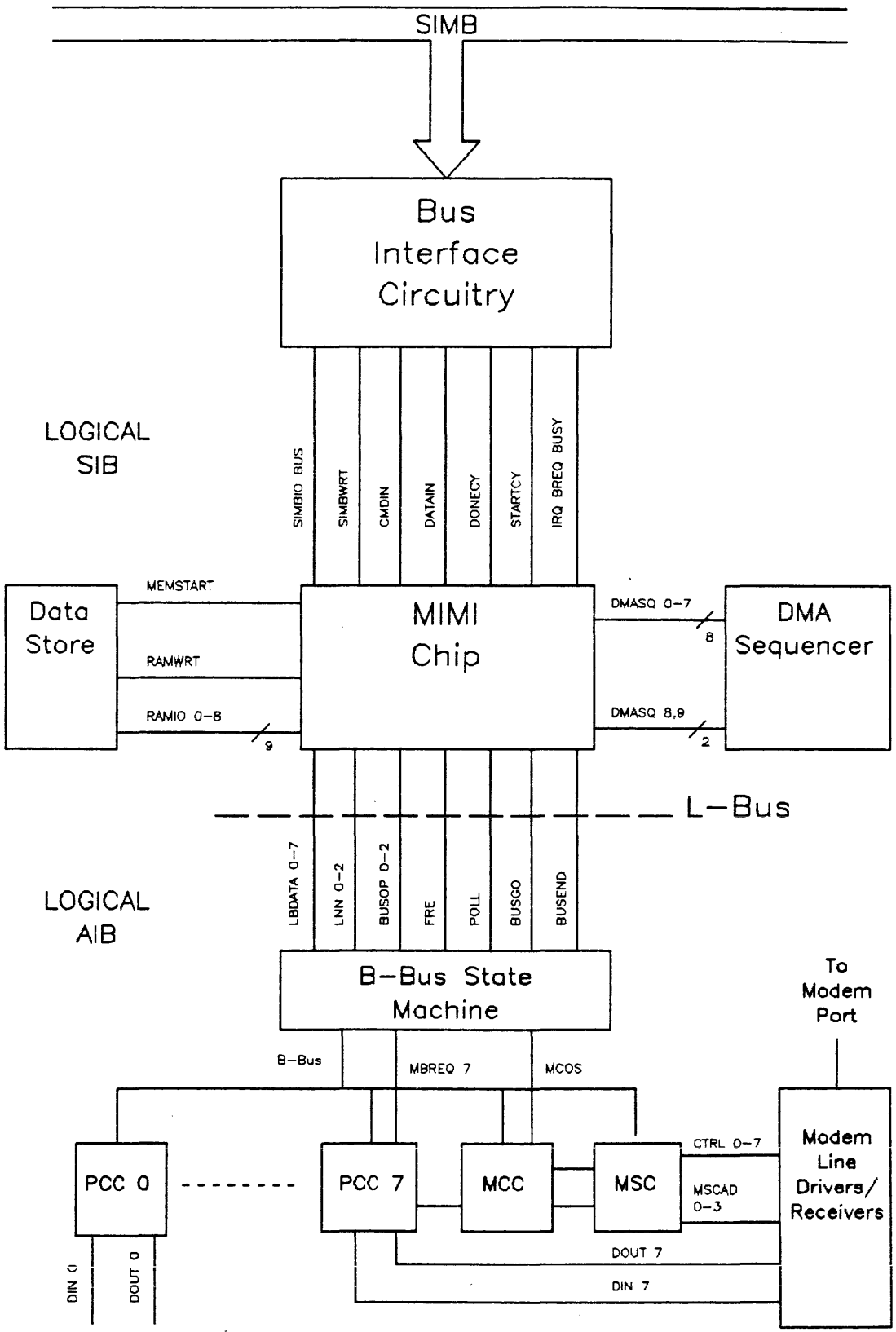

Figure 7-5. TIC Block Diagram

Control programs executed by the PCC enable the system to interact with the port. The PCC can only communicate with the system or the port via a control program. Control programs are similar to channel programs, except that the code is down-loaded to each PCC and executed by each PCC. The TIC does not execute channel programs nor does it issue Channel Program Service Requests (CSRQ). Instead, the TIC interrupts the system via an Interrupt Request (IRQ) when it requires software intervention.

Much of the circuitry on the TIC supports the PCCs. The B-Bus State Machine on the TIC handles data and interrupts between the PCCs and the system. It gates the information onto the L-Bus.

The remaining TIC controls interactions with the system. This is the same function the SIB performs in the ATP system. The MIMI chip performs most of the SIB functions shown below:

- Store DMA bank and address values for each PCC.
- Store Control Program bank and address values for each PCC.
- Execute DMA to carry data between main memory and the L-Bus.
- Store PCC interrupts in FIFO memory and report them to the system

Several circuits enable the MIMI chip to perform these operations. The Data Store is a 256 x 9-bit RAM. It stores DMA and Control Program bank and address values as well as interrupt information from the PCCs. The DMA Sequencer is a 2k x 8-bit PROM that controls DMA operation. Various registers and state machines outside the MIMI chip handle interactions with the SIMB, such as data flow, bus arbitration, parity generation, and global command response.

DMA Sequencer

The DMA Sequencer is a 2k x 8-bit PROM and an address register. It is a state machine sequencer that runs most of the MIMI chip operations. There are ten lines between the DMA Sequencer and the MIMI chip. These are the data and address lines DMASQ<0:9>. The MIMI chip sends a ten-bit address to the DMA Sequencer and then fetches two bytes of data from it. The latches in the MIMI chip pack the two bytes into 16 control bits to be used in the MIMI chip.

MIMI performs byte packing and unpacking and operates with the SIMB state machine to reference full words of main memory.

DMA performs three functions:

- Read Data Path. This function reads data from main memory to be sent to a connected terminal via a PCC.
- Write Data Path. This function reads data from a terminal via a PCC. The data is packed and written to main memory.
- Write Control. This function reads a control program from memory and writes it to a PCC. Note that the control program must be executing in the PCC before data can be read or written.

Before DMA can be invoked, SIMB registers 8 through 15 (DMA control registers) must be properly configured by the system.

Data Store

The Data Store is a 256 x 9-bit RAM and address register. Each PCC has SIMB registers 0 through 7 stored in the Data Store. It is also used to store interrupts from the PCCs.

L-BUS

The L-Bus is the same as the Lynx bus on the ATP. It is the logical separation between the SIB and AIB functions on the TIC.

B-Bus State Machine (BBUSSM)

The B-Bus State Machine runs and arbitrates the B-Bus. The B-Bus is used for all communication between the PCCs, the MCCs, and the L-Bus.

Port Controller Chips (PCC)

There are eight PCCs on the TIC. Each PCC controls one port. There are six hardwired ports and one modem port. Note that port 6 is unused. Each PCC speed senses with the connected device at one of the following eight baud rates:

19,200

9600

4800

2400

1200

600

300

110

Speed sensing is accomplished by executing an ENQ/ACK handshake with the connected device. For example, the PCC transmits an ENQ one baud rate at a time until a ACK is received from the device. If there is no response after transmitting at all of the baud rates, the PCC senses the line waiting to receive a Carriage Return. In this state, the PCC measures the width of the start bit to determine the baud rate. When the Carriage Return is received, the PCC will configure the port for the baud rate of the sending device.

The modem port does not speed sense the same way as the other ports do. It assumes that the device connected to it is set to 1200 baud. If it is not, sensing is accomplished by waiting for a Carriage Return.

The TIC has no configuration switches. The channel number assigned to a TIC is determined by the slot number in which it is installed.

Serial Link Specifications

RS-232 Direct Connect Specifications. The maximum supported cable length is 50 feet. RS-232 direct connect cable wiring is shown below.

PIN	SIGNAL NAME
1	AB Signal Ground
2	BA Transmit Data
3	BB Receive Data

RS-232 Modem Port Specifications. The maximum supported cable length is 50 feet. The modem port uses a standard RS-232-C 25-pin D-type connector. The pin numbers and the signals are shown below. The pin assignments in the connector are shown in figure 7-6.

PIN	SIGNAL NAME
1	AA Protective Ground
2	BB Received Data
3	BA Transmitted Data
4	CF Data Carrier Detect
5	CF Data Carrier Detect
6	CD Data Terminal Ready
7	AB Signal Ground
8	CA Request to Send
12	SCA Secondary Request to Send
19	SBB Secondary Received Data
20	CC Data Set Ready
21	CG Ring Indicator
22	CB Clear to Send
23	CH Speed Select

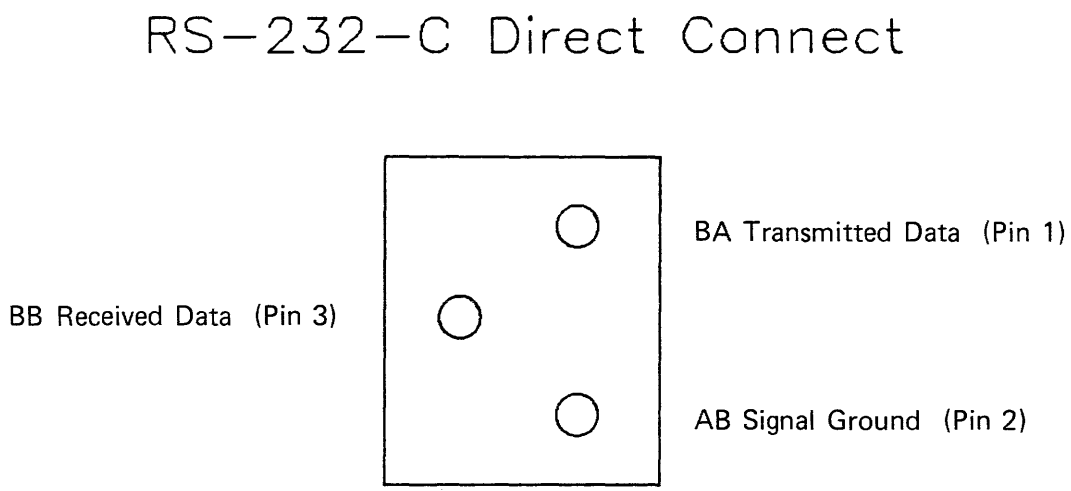

Figure 7-6. RS-232 Connector Pin Assignments

Service Features

Loop-Back. Test section 30 in the TIC offline diagnostic performs a loopback through either a loop-back connector or locally on the board by grounding the Loop test point on the TIC. If the board loop-back passes and the port loop-back fails, the probable cause of the failure is the connector board. The loop-back connectors and their associated part numbers are listed below.

LOOP-BACK CONNECTOR	PART NUMBER
3-Pin RS-232 Loop-Back Connector	30148-60002
Modem Loop-Back Connector	30146-60002

Remote Console Interface. Refer to the Remote Operator Interface paragraphs for this information.

Replaceable Assemblies. Refer to the Removal and Replacement lesson for this information. Note that both of the plug-in connector boards are assemblies. That is, they are composed of two PC boards. If one of the boards fail, it is not necessary to replace both of them.

TIC Diagnostic Tools

The following diagnostic tools are available with this product for diagnosing TIC problems.

1. PON selftest
2. Maintenance Mode Selftest - TIC test
3. DUS diagnostic (TICDIAG)
4. Terminal On-line Diagnostic Support Monitor (TERMDSM)

TIC Quiz

1. How many users can be physically attached to a TIC?
   7
2. How does the TIC get attention from the system?
   Asserts IRQ
3. If the only I/O operation being executed by the Series 37 is for the TIC, will the RUN indicator on the front panel be lit? Explain. No CSRQ is not Active
4. What are the three major functions performed by DMA on the TIC?
   Read & write DATA path write cntl
5. What is a Control program? How are they used?
   Pgm that runs on the PCC to comm between user & SYS
6. What conditions must be satisfied for a terminal to issue a Control B sequence and have the TIC execute it? Sw = 2 & be the console
7. Is it necessary for a system console to have ENQ/ACK handshake capabilities? Explain.
   yes
8. How can you distinguish between a TIC PCA failure and a connector board failure?
   grd the loop conn on TIC & Run test 30
9. List the tools provided with this product for TIC analysis.

TIC Lab

1. Connect the terminal to port 0. Turn DC power on by setting the keyswitch to position 2. When the `H for help->` prompt is displayed, execute a Speed command and set the baud rate to a value other than what it is now.

   When the Speed command has been successfully executed, reconnect the terminal to the modem port and enter the Remote mode.

   From the modem port, verify that the terminal is operational. Execute the Speed command and change the baud rate back to the original setting.

2. With the terminal still connected to the modem port, turn DC power off and then back on. Return the keyswitch to the Remote position. Verify that the terminal can still communicate with the system.

   Reconnect the terminal to port 0. Turn DC power off and back on. Return the keyswitch to the Remote position.

   Can the terminal communicate with the system?

   Reconnect the terminal to the modem port.

   Is it operational?

   What conclusion can you make from this exercise?

3. Turn DC power off and remove the AC power cord. Remove the TIC PCA from the card cage.

   Identify the loop pins on the PCA.

   Reassemble the Series 37 SPU without the TIC and apply DC power. Record the states of the self-test indicator.

   Remove the connector board assembly and reinstall the TIC. Reassemble the Series 37 SPU without the connector board assembly.

   Apply DC power and record the states of the self-test indicator.

4. Turn off DC power. Remove the AC power cord. Fully reassemble the Series 37 SPU.

REMOTE OPERATORS INTERFACE (ROI)

The Remote Operators Interface (ROI) enables the Series 37 to be controlled by a remote console. The capabilities of a remote console are the same as in the Maintenance Microcode paragraphs.

The local and remote console interfaces to the Series 37 and the operation of the key switch are described below.

Series 37 ROI Implementation

The Remote Operator Interface (ROI) is implemented on three different assemblies. The assemblies and their functions are described below.

The Display Panel Keyswitch controls the state of the ROI.

The CPU maintenance microcode controls the modem interface. When the keyswitch is set to the Remote position, a microcode jump is forced to the maintenance microcode. The microcode takes control of the modem interface. Data Terminal Ready (DTR) and Request to Send (RTS) are directly controlled by the microcode. The modem status lines Data Set Ready (DSR), Clear to Send (CTS), and Data Carrier Detect (DCD) are monitored. The TIC PCA contains the actual ROI hardware. The state of the hardware is controlled by the Remote signal from the keyswitch and by the microcode control of the modem port. Figure 7-7 is a block diagram of the ROI control logic.

Establishing a Remote Session

Refer to table 3-1 for the keyswitch definitions. If a session was established on port 7 before entering the Remote mode, the session is suspended while in the Remote mode. The input and output to port 7 are disabled.

Local/Remote Console Communication

In the Remote mode, the local keyboard is disabled and the input/output of the remote console is duplicated on the local console. The local console then becomes an output device.

Messages can be sent to and from the two consoles by toggling the SPU key switch between the Local and Remote positions. If you switch from the Remote to the Local position, the local console keyboard is enabled and the output is directed to both consoles. Note that the modem line connection is not affected. If you turn the key switch to the Normal position, you disconnect the remote console and disable the two-way conversation capability.

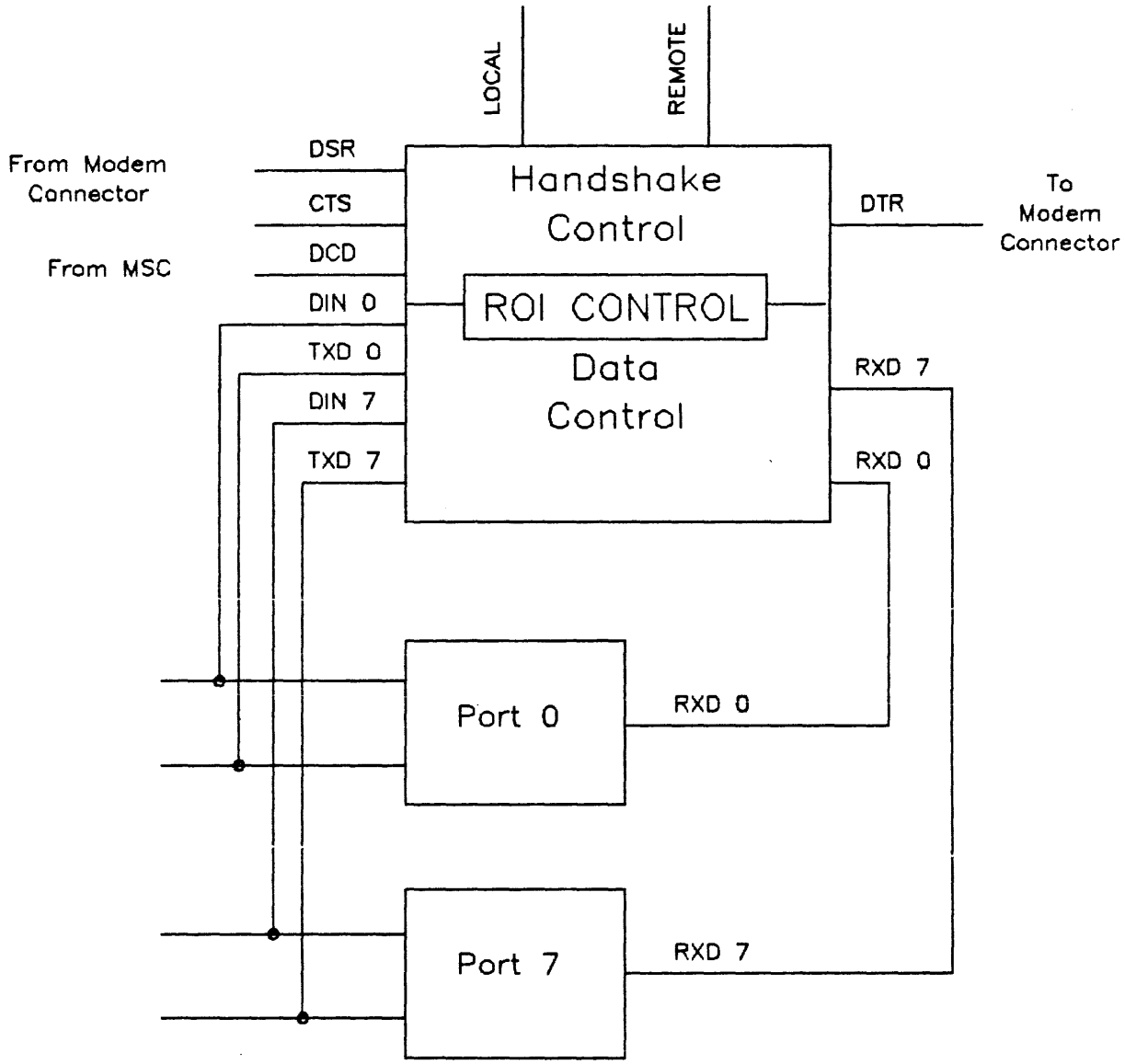

Figure 7-7. ROI Control Logic Block Diagram

Configuring the Baud Rate for ROI Operations

When switching from the Normal or Local mode to the Remote mode, Port Controller Chip (PCC) 0 is used to drive both the local and remote consoles. The baud rate of both consoles must match that of PCC 0. The three methods of setting the correct baud rate are listed below.

- If MPE is running, execute an MPE Speed command at the local console before switching to the Remote mode. Readjust the baud rate on the local console, switch to the Remote mode, and make the line connections.
- If you are in the Control B environment, execute a microcoded Speed command at the local console. Readjust the baud rate on the local console, switch to the Remote mode, and make the modem connection.
- When you turn the keyswitch from the Off position to the Remote position, the maintenance microcode speed senses the remote console if the following conditions are true:
    - The remote console is on-line, and
    - the modem status lines DSR and CTS are asserted. This will happen only if the remote console is hardwired to the port, if it is connected to a repeater, or if a modem is attached to a leased line. Note that if either or both of the DSR or CTS signals are not asserted when the Series 37 SPU keyswitch is set to the Remote position, the console attached to port 0 will be active. It will remain active until both of the signals are true. At that time, it will be necessary to switch to the Local mode and execute the microcoded Speed command if the baud rates of the two consoles do not match.

ROI and its Effect on the Modem Port

The state of the modem connection when the Series 37 is switched between the local or normal modes and the remote mode is described below. Physical action is shown in **bold-face type**. The results of the action are shown in this type face.

The sequence of events when no session has been initiated and the keyswitch is moved from the Local position to the Remote position and then to the Normal position is described below.

The SPU is in the Local mode and no session has been initiated on port 7. The keyswitch is rotated to the Remote position.

The maintenance microcode assumes control of the modem status lines and asserts the DTR and RTS lines.

A modem connection is established using the maintenance microcode. The keyswitch is toggled between the Local and Remote positions.

As the keyswitch is toggled, the modem status lines remain in the connected state. Two-way communication is enabled between the local and remote consoles as a result of toggling the keyswitch. This mode is the Local/Remote mode.

If the keyswitch is set to the Normal position, you exit the remote mode.

The DTR line is dropped. This disconnects the modem.

The following text describes the sequence of events when a session has been initiated and the keyswitch is moved from the Local or Normal position to the Remote position and then to the Normal position.

MPE is active and a session has been established on port 7 via a modem. The keyswitch is toggled from either the Normal or Local position to the Remote position.

The session on port 7 is still active. However, communication between the port and the terminal has been disabled. The terminal is now a remote console and is connected to port 0. The maintenance microcode controls the DTR line and the modem connection remains intact.

The keyswitch is toggled between the Local and Remote positions.

As the keyswitch is toggled, the modem status lines remain in the connected state. Two-way communication is enabled between the local and remote consoles as a result of toggling the keyswitch. This is the Local/Remote mode.

While you are still in the remote mode, set the keyswitch to the Normal position. You exit the remote mode.

The remote mode is aborted. The port is no longer a remote console port. It is now port 7. The original modem connection has been aborted and the connection must be reestablished for the session.

ROI Quiz

1. If the MPE Console command is used to change the console to port 5, will the console on port 5 have full console capabilities? Support your answer.

2. Why may it be necessary to issue a Speed command when switching from the Local or Normal mode to the Remote mode?

3. Assume that you are using the terminal attached to the modem port as a remote console (connected by the HP tele-support modem) and that power is lost. When AC power is restored, what will be the state of the remote console? Explain your answer.

4. Which three assemblies make up the Remote Operators Interface?

5. Assume that the HP tele-support modem is attached to the modem port. What baud rate should be used for the Speed command?

Diagnostics

Appendix A

INTRODUCTION

Appendix A describes the diagnostic programs available for the HP 3000 Series 37 SPU. A brief description of each diagnostic is provided. The minimum hardware configuration is defined. Each of the major steps of the diagnostic is described.

MEMORY DIAGNOSTIC

Introduction

The memory diagnostic MDIAG37 tests all memory and all control functions. It forces single-bit error detection and correction. You can control error handling, looping, printing messages, and test selection.

Required Hardware

The minimum configuration of the HP 3000 Series 37 hardware is required to run MDIAG37.

CPU
Memory (located in slot 2 of the SPU - must work well enough to initiate MDIAG37)
TIC
HP-IB tape drive
PIC (as a cold-load path to load DUS)

Test Descriptions

Test Section 1

Test Section 1 (steps 11 through 13) tests low memory and diagnostic capability. It also reads the syndrome information and checks the memory configuration. It automatically executes when you call MDIAG37.

Test Section 2

Test Section 2 (steps 21 and 22) performs a simple pattern test on all memory PCAs. It then checks the Error Detection and Correction circuit (EDAC) to ensure that the PCA will function correctly if single-bit errors are present.

Test Section 3

Test Section 3 (step 31) writes the bank and address of every location throughout available main memory. Each location is then read and verified. If this test fails, the unique addres capability has failed and duplicate bank and address locations have been written.

Test Section 4

Test Section 4 (step 41) writes alternate ones and zeros in ascending address order and the reads them back. The complement pattern is then written and read back. The error latch is read after testing both patterns to determine if any single-bit errors were detected.

Test Section 5

Test Section 5 (step 51) writes 64K data patterns into one 32-bit memory word in each block. Each chip on each PCA will be accessed to identify any malfunctioning chips. The data patterns are generated by using the 64K possible patterns in the lower 16 bits and the one's complement of the patern in the upper 16 bits. The error latch is checked after each word is read and verified.

Test Section 6

Test Section 6 (step 61) uses the lowest 32K bytes of memory as a data bank and copies it to every other 32K byte block of memory. The data in each block is then verified. The error latch is checked after each Verify operation.

Test Section 7

Test Section 7 (step 71) move first ones and then zeros through each 32K-byte block of memory. Each 32K-byte block of memory is set to all zeros. Each location is then read for a zero and then written to all ones. When the block contains all ones, the process is reversed. Each location is read for all ones and then written to zero. The error latch is checked after each 32K-byte block of memory is tested.

Test Section 8

Test Section 8 (steps 81 through 83) relocates the program and checks the area where the program was originally located (banks 0 and 1). It is then relocated to its original area.

Test Section 9

Test Section 9 (step 91) checks the error latch to make sure it has been cleared before the diagnostic program returns conrol to DUS.

TERMINAL INTERFACE CONTROLLER (TIC) DIAGNOSTIC

Introduction

The Terminal Interface Controller (TIC) diagnostic TICDIAG verifies the correct operation of all of the functions of the TIC. The TICDIAG routines are divided into two major groups to adequately test the hardware. The two groups are the System Interface Board (SIB) tests and the Asynchronous Interface Board (AIB) tests. The SIB and the AIB are sections on the TIC PCA. The SIB tests check the circuitry

between the SIMB and the L-Bus. They affect all ports. The AIB tests check the circuitry from the L-Bus to the cable connector and affect only one selected port at a time. The SIB tests, if selected, run before the AIB tests.

Required Hardware

The following minimum configuration of the HP 3000 Series 37 hardware is required to run TICDIAG.

CPU
Memory
TIC (located in slot 1 of the SPU-
must work well enough to
initiate TICDIAG)
HP-IB tape drive
PIC (as a cold-load path to load DUS)

Test Descriptions

The SIB and AIB tests are briefly described below. You cannot run the SIB test if only one TIC is installed. You cannot run the SIB test on the TIC to which the console is connected.

System Interface Board (SIB) Tests

Test 1. IMB-SIB COMMUNICATION - Tests the SIB to ensure that all allowable Intermodule Bus (IMB) commands work.

Test 2. INITIAL REGISTER VALUES - Tests the values that are obtained from the SIMB registers after initialization. The value of each register to be checked is read. thi svalue is then compared to the expected value of the register.

Test 3. ERROR CIRCUITRY - Tests the error circuitry on the SIB. It issues an illegal command and verifies that it is detected. It then checks the Error Clear mechanism of Register !A (Diagnostic Control Register).

Test 4. RESET/INIT - checks to ensure that an INIT command causes a reset of the registers and of the error detection circuitry.

Test 5. IRQ LOGIC - Tests the interrupt logic of the SIB.

Test 6. MEMORY - Tests the SIB memory by running a checkerboard test and an address test. The SIB memory is used as the DMA registers for the I/O ports.

Test 7. SEQUENCING - Single-steps the L-Bus State Machine and then checks the state after each cycle.

Test 8. TIMEOUT - Tests the L-Bus timeout logic, which terminates the wait for either BusEnd from the L-Bus, or HALT from the DMA state machine. The timeout occurs if the L-Bus handshake does not finish in the required time limit.

Test 9. BOARD ENABLE - Tests the Board Enable logic on the SIB section of the TIC PCA. This logic includes the Board Enable register and the L-Bus State Machine.

Test 10. PORT POINTER - Tests the Port Pointer logic.

Test 11. FREEZE - Tests the operation of the Freeze bit of Register !A. This bit causes the L-Bus State Machine to cycle between states 0 and 4, and causes the PCCs to halt.

Test 12. TIC BUS BUFFERS - Tests the L-Bus buffers.

Test 13. DIRECT COMMAND - Tests the data paths that carry a direct command to the L-Bus.

Test 14. FIFO - Tests the operation of the FIFO. Test 15. STATE COUNTER - Checks that the DMA state counter increments each time until it reaches the HALT command, at which time it is reset to zero.

Test 16. DMA ADDRESS COUNTER - Tests the DMA address counter by checking each bit carry as it counts.

Test 17. COMP/CTR LOOPBACK - Tests the DMA logic COMP register and address counter. It loads a pattern into memory, runs the DMA test that loads the DMA registers from memory, and then runs the test that dumps the registers back into memory.

Test 18. READ IMB - Verifies proper operation during an IMB Read operation.

Test 19. WRITE IMB - Verifies p@roper operation during an IMB Write operation.

Test 20. BEGIN FLAG/LEFT-RIGHT FLAG - Tests the operation of the Begin Flag and the Left-Right Flag circuitry on the SIB.

Asynchronous Interface Board (AIB) Tests

Test 21. PCC SELF-TEST - Performs a self-test on one port and checks the results returned from that port's PCC.

Test 22. PCC DUMP - checks the operation of a dump on a PCC.

Test 23. MCC SELF-TEST - Initiates a self-test of the MCC,PCC, and MSC if port 7 is to be tested on the TIC. The self-tests are initiated by disabling the MCC and MSC and then issuing an MCC self-test control order to set the most significant bit.

Test 24. MCC DUMP - Checks the operation of an MCC dump if port 7 is to be tested on the TIC.

Test 25. PCC/MCC COMMUNICATION - Tests the communication between the PCC and the MCC if port 7 is to be tested on the TIC.

Test 26. DIAGNOSTIC LOOPBACK - Executes the PCC's diagnostic loopback test. The diagnostic loopback control is used to test the hardware path from main memory to the PCC and back to main memory.

Test 27. BAUD RATE - Tests the baud rate logic on the AIB section of the TIC. It tests all of the baud rates on each port by determining how long it takes to do a blind write of a given number of characters.

Test 28. MODEM SIGNALS - Performs a loopback of the modem control signals for port 7 of the TIC. It also checks that the interrupt occurs and that it comes from the corect port.

Test 29. MSC PORT ADDRESSING - Tests the addressing of port 7 by the MSC. If an addressing error has occurred, it is detected when the wrong address is read from one or more ports.

Test 30. LOOPBACK - Executes a loopback through either a loopback hood or through the loopback circuitry on the TIC. The loopback circuitry is activated by placing a jumper on the test points near the backplane connector of the TIC PCA.

PERIPHERAL INTERFACE CONTROLLER (PIC) DIAGNOSTICS

Introduction

The Peripheral Interface Controller (PIC) diagnostic PICDIAG performs a basic function test of the PIC to verify that the PIC functions correctly. No communication to the HP-IB devices is attempted except to identify the cold-load device specified. If no device is attached or if the wrong device is attached, a message is displayed on the system console.

Required Hardware

The following minimum configuration of the HP 3000 Series 37 hardware is required to run PICDIAG.

CPU
Memory
TIC (located in slot 1 of the SPU - must work well enough to
initiate PICDIAG)
HP-IB tape drive
PIC (must work well enough to load PICDIAG)

Test Descriptions

There are nine test sections in the PICDIAG. They are briefly described below.

Test 1. REGISTER TEST (Steps 1 through 4) - The Register tests exercise only the the registers on the PIC. It verifies that the registers contain the correct values. The ABI registers are tested later.

Test 2. INTERRUPT TEST (Steps 5 through 10) - The Interrupt tests verify that the interrupt mechanism operates correctly.

Test 3. CONFIGURATION TEST (Steps 11 through 13) - The Configuration test verifies that the PIC Configuration registers contain the correct values.

Test 4. ABI VERIFICATION (Steps 14 through 17) - This test checks the ABI Interrupt register and the Interrupt Mask register.

Test 5. DMA STATE MACHINE TEST (Steps 18 through 32) - This test performs a Write from memory to the PIC FIFO. It then reads the data from the PIC FIFO into memory to simulate a forced DMA abort condition.

Test 6. CHANNEL SERVICE REQUEST TEST (Steps 33 through 39)

Test 7. ABE HSE TIMING TEST (Step 40) - This test verifies that the ABI meets minimum HP-IB speed specifications.

Test 8. HP-IB INTERFACE DRIVER TEST (Steps 41 through 44)

Test 9. ON-LINE DATA TEST (Step 45)

Cabling Information

Appendix B

Figure B-1 shows how to connect terminals and modems to the Series 37 SPU.

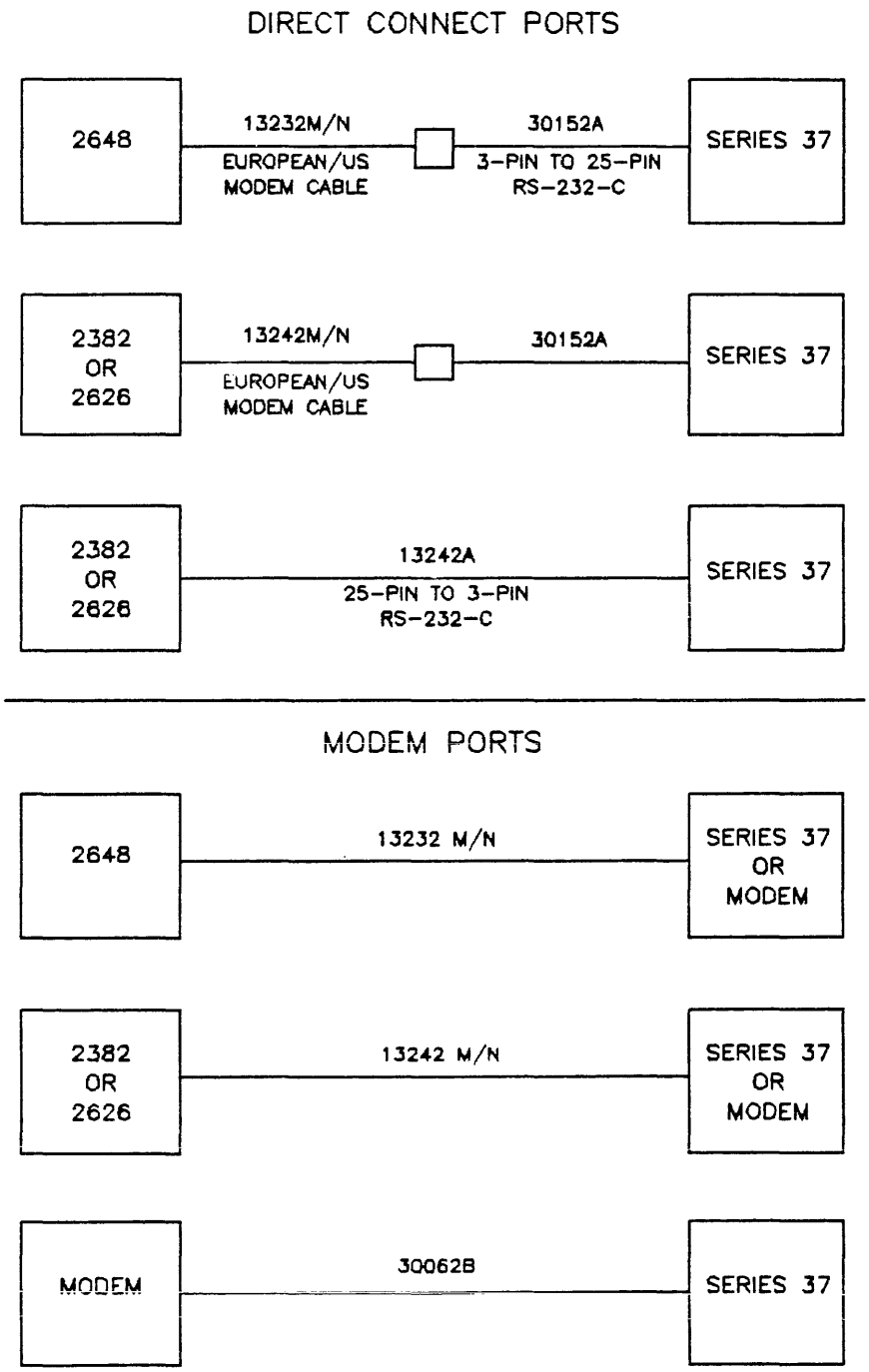

Figure B-1. Cabling Diagram

Quiz and Lab Answers

Appendix C

Lesson 1 Quiz

1. 1
2. 28
3. No

Lesson 2 Quiz

1. Single AC power source. The supported devices are low power, allowing them to be connected to a single power strip.
2. No.
3. Daisy chain since it generates less noise.
4. Use the cable that has been shipped with the device.
5. External HP-IB devices.

   The need for multiple AC circuits.

Lesson 3 Quiz

1. Allows the main console to issue a Control B sequence and have it executed. In the Normal position, the Control B sequence cannot be executed.
2. Whenever AC power is applied.
3. The Run indicator will be on any time a Channel Program Service Request (CSRQ) is issued.
4. Both update the addresses in the TOC. However, the "C" will not cause a Load or Start.
5. The SPU keyswitch must be in the Remote or Local position and the issuing terminal must be connected to port 0 or port 7 on the TIC installed in channel 1.
6. T[est] enters you into the Test mode. I[OMAP] runs IOMAP, which will obtain the information.
7. CH3,10. This will test the PIC in channel 10 (slot 2 of the Extender). The test will run three times.
8. Execute a Control B or cycle the power.
9. When loading or running software.

10. Run I[OMAP].

Console Operation Lab

3. The terminal did not speed sense or the TIC failed Selftest.
4. True
6. Yes
7. No
8. No. Because data carrier detect "DCD" and clear to send "CtS" are not asserted. There is no modem.

Maintenance Microcode Lab

2. No
3. Turn the keyswitch to Local.

Lesson 4 Quiz

1. False
2. False
3. True. The fuse.
4. Remove the front panel.

   Remove the rear panel.

   Remove all plug-in boards.

   Remove the battery and battery holder.

   Remove the display board cable.

   Remove the remaining screws and remove the backplane.

   Install the new backplane. Leave the screws loose.

   Install the power supply .

   Install a board in slot 1.

   Install a board in slot 5.

   Tighten the screws.

   Install the remaining assemblies.

Removal and Replacement Lab

3.k . No

3.l . Memory must be present and working before information can be displayed on the terminal

If memory is not present or not working, Selftest will loop between the memory test and the CPU test.

A PIC board does not have to be present for Selftest to successfully complete.

Lesson 5 Quiz

1. a, c, d, e, f, g, h, i, j.

2. a. -PSW notifies the system of the pending loss of DC power so that the registers required for recovery can be stored in battery backed up memory. -PSW is asserted at least three milliseconds before the SPU goes into the battery back-up mode.

   b. -OTW notifies the system that the ambient temperature near the power supply is equal to or greater than 45 degrees C. The signal originates from a sensor on the power supply. The sensor is in a closed circuit when activated.

   c. -OTS notified the system that the ambient temperature near the power supply is equal to or greater than 60 degrees C. It originates and operates in the same manner as -OTW. -OTS results in a power supply fault condition and no system recovery.

   d. +VON is used to control th power supply DC output voltages. When it is asserted, DC output is enabled. It is controlled by the front panel keyswitch.

   e. -BBK indicates to the user that the system is in the battery back-up mode. It does this by illuminating the front panel Battery LED. It is asserted when both -PSW and +VON are asserted.

3. Load and Detection board

Power System Lab

10 . Nothing.

11 . When DC power is on and AC power is removed, the battery LED will be lit. In this state, if the keyswitch is turned to the zero position, the battery LED will be turned off. The battery LED cannot be turned back on in this state by turning the keyswitch to the 1, 2, or 3 positions.

Lesson 6 Quiz

1. In HP 3000s they respond to a Parallel Poll by asserting the assigned Data bit.

2. IRQ and CSRQ.

3. Access cycle.

4. TIC. Because the TIC occupies channel 1, which has the highest priority.

5. SIMB address bus.

6. They are assigned a slot number - 1 through 5 in the SPU and 9 through 13 in the Extender.

7. Channel identification lines (ID0-ID3).

Lesson 7

CPU Board Quiz

1. c, d, g.

2. True.

3. If the system fails due to a detectable system fault, such as "WCS parity error", this can be determined from the last halt data even when the console display has been lost.

4. It converts the Power Supply warning (-PSW) signal to -PFW and controls +PON, so that the system initialization and power fail/recovery process functions correctly.

5. It is used only for displaying the state of selftest - the current test that is executing and the error conditions.

6. RUN - CSRQ
   DC - +VON
   AC - +BIAS
   BATTERY - -BBK and +5B
   REMOTE - -REMACTIVE directly and REMOTE (from keyswitch) indirectly.

7. PON Selftest and maintenance mode selftest - CPU test.

Memory Board Quiz

1. a, d, f.

2. a, b, c, f.

3. False

4. True

5. True

6. PON selftest, maintenance mode selftest - memory test,
   DUS memory diagnostic MDIAG37, and memory logging facility.

PIC Board Quiz

1. SIMB interface logic. It interfaces the PICs internal circuitry with the SIMB.

   PIC control logic. It controls the logic necessary to maintain the PICs internal registers, the SIMB control logic, the commmand execution state machine, and the CSRQ/IRQ logic.

   The HPIB interface interfaces the PIC circuitry with devices on the HP-IB.

2. The PIC interfaces to the SIMB. The GIC interfaces with the IMB.

   The PIC does not support a channel program processor.

   The PIC does not have frontplane configurator switches.

   The PIC has an ABI chip, The GIC has a PHI chip.

3. False.

4. True.

5. Reads and writes to the PICs internal registers.

6. False.

7. True.

8. Devices 0 through 7.

9. PON selftest, maintenance mode selftest - PIC test, DUS diagnostic (PICDIAG), and DMA Exerciser.

PIC Lab

Selftest will pass if a PIC is not present or is not operational, i.e. it does not respond to the CPUs roll call.

TIC Board Quiz

1. 7.

2. Issuing an IRQ.

3. No. The Run light on the display panel monitors CSRQ.

4. Read data. Data is read from memory and is sent to the connected device.

   Write data. Data is read from the connected device and is written into memory.

Write control. A control program is read from memory and is sent to the desired PCC.

5. A control program is downloaded from the memory to the PCCs. The PCCs must be executing a control program to be able to communicate with the system.

6. The terminal must be connected to port 0 on the TIC installed in channel 1 and the keyswitch must be in the local or remote position.

7. Yes. This is the method by which the TIC performs speed sensing. It also helps prevent data overruns on data sent to the terminal.

8. By running the offline diagnostics and selecting the loop-back option.

First use the loop-back connector on the desired port.

Next short the loop pins together on the TIC board and rerun the test.

If the first test fails and the second test passes, the Connector board is bad.

If both the first and the second tests fail, the TIC board is bad.

9. PON selftest, maintenance mode selftest - TIC test, and DUS diagnostic TICDIAG.

ROI Quiz

1. False. Only the console on port 0, channel 1 can issue a Control B sequence and have it executed.

2. The terminal on port 7 can be set to a different baud rate and/or a modem can be connected.

3. The remote console will be disabled. The power will have caused the modem to be disconnected. It will be necessary to reconnect the line.

4. SPU keyswitch, CPU maintenance microcode, and the TIC hardware installed in the channel.

5. 1200 baud.

Course Evaluation

Appendix D

Series 37 SPU

Student Name: _____ Date: _____

Company: _____

Address: _____

_____

Service Manager: _____

	Yes	No
Do you feel the course objectives were met?	☐	☐
Did you find the course easy to read and understand?	☐	☐
Do you feel you need additional training?	☐	☐
Would you purchase another self-paced course?	☐	☐

How would you rate the following:

(check one)	Excellent	Very Good	Good	Acceptable	Poor
Quality of tests and exercises?	☐	☐	☐	☐	☐
Quality of information provided?	☐	☐	☐	☐	☐
Quantity of information provided?	☐	☐	☐	☐	☐
Service Manual provided?	☐	☐	☐	☐	☐
Diagnostic tests?	☐	☐	☐	☐	☐
Quality of troubleshooting labs?	☐	☐	☐	☐	☐
Overall rating of the course?	☐	☐	☐	☐	☐

Was the level of the course ☐ trivial ☐ just right ☐ too technical?

Would you recommend this program to other people in your organization? ☐ Yes ☐ No

Why (why not)? _____

Additional Comments: _____

_____

_____

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