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High-Speed Dynamic Programmable Logic Array Chip

Abstract: This paper describes the circuit design of a programmable logic array chip using four-phase dynamic circuits, operating at a nominal cycle time of 230 nanoseconds. Bootstrap circuit techniques are used to obtain high function and performance by satisfying some special requirements of PLA designs. These include a simple means for two-bit partitioning of the data inputs, a noninverting buffer circuit between precharged arrays, and a fast, compact on-chip driver for heavily loaded arrays. Multiphase clocking enables the use of master/slave type JK flip-flops with minimum circuitry and power dissipation. A polarity hold function is provided at the outputs to allow interfacing the dynamic design to static output circuits.

Introduction

The circuit design of a programmable logic array (PLA) FET chip intended to provide engineering hardware for general systems applications is discussed. The techniques used provide optimum performance for the general requirements of array logic designs. Included are descriptions of the circuitry, the special features of PLA design, and the results of computer simulations for nominal and worst-case performances. The results are in good agreement with measured data.

The chip, typically operating at a 230 nanosecond cycle time using four-phase, externally generated clocks, has a nominal power dissipation of 150 mW. Configured with 18 logic inputs, 16 logic outputs, and 13 JK flip-flops, the inputs are two-bit partitioned and the outputs are provided off-chip through dynamic-to-static off-chip drivers. All logic inputs and outputs interface with medium speed DIP-TL (dual in-line packaged transistor logic) circuitry and similar array modules. The design has 70 product terms.

A programmable logic array [1, 2] is an orderly structure for handling combinatorial sequential logic functions. System designs in Boolean functions and state diagrams can be readily implemented into hardware.

The design discussed here contains two arrays cascaded to perform a logical AND-OR function. The arrays are personalized for a specific function at the gate mask level during processing. Outputs from the second (OR) array are delivered either off-chip or to a JK flip-flop located on the chip. The JK outputs are fed back to the AND array for sequential operations. Data inputs to the chip are two-bit partitioned [3, 4] before addressing the AND array. This technique consists of logically ANDing pairs of input data bits and their complements. It increases the logic capability of the design with only a small addition to circuitry and chip area.

Using n-channel, insulated-gate FET technology, the device's characteristics become similar to those described by Critchlow et al. [5]. When more than one logic decision was required within a single clock interval, four-phase dynamic circuits were used in conjunction with clock-ratioed devices.

Electrical performance was simulated using the Advanced Statistical Analysis Program (ASTAP) [6]. Analyses were made both with nominal conditions assumed and with detrimental skewing of the process parameters. Experimental measurements were also made on the completed hardware. A functional application of the chip was presented by Logue et al. [7] who implemented the functions of an existing terminal controller in array logic using seven of the PLA chips operating at a 1-μs cycle.

Functional description

Figure 1 is a diagram of the PLA design. The arrays are matrices of possible FET device sites. Metal input lines pass over all sites and serve as gate electrodes. The source and drain diffusions are perpendicular to these lines. Active devices are made by providing thin oxide at select locations during processing, thus requiring a unique gate mask for each application. The other masks used in the process are the same for each design.

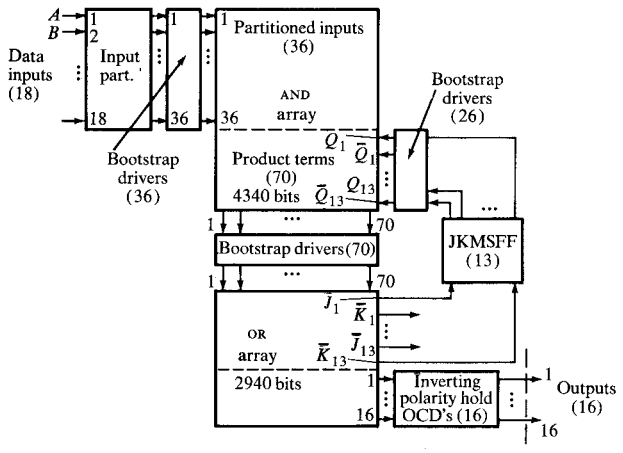


Figure 1 The PLA functional block diagram showing the number of circuits required in each section.

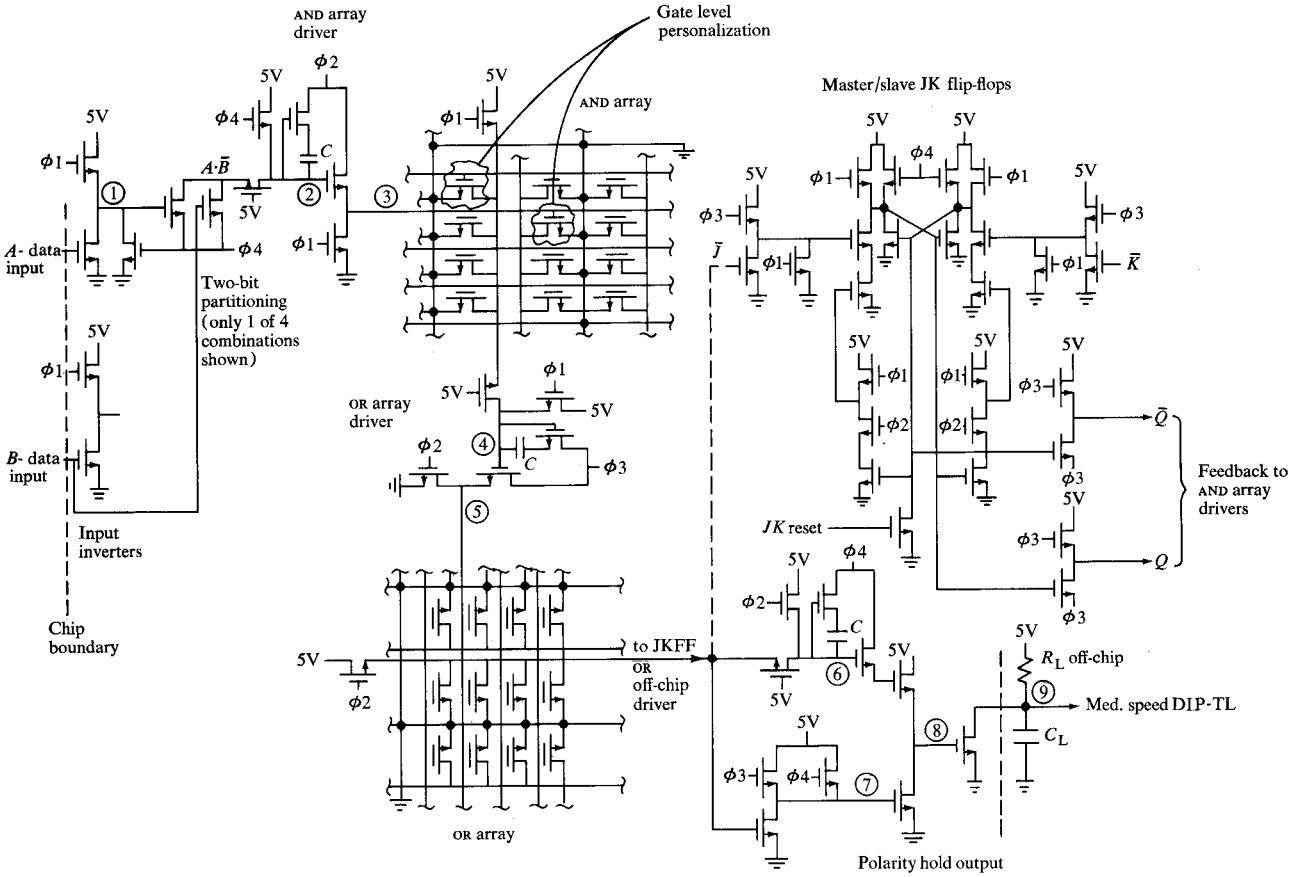
The PLA is structured to provide a logical AND-OR function with positive significant data. The arrays are NOR circuits. Logic inversions are implemented at the inputs and following the second array. Master/slave type JK flip-flops are used for on-chip storage to handle sequential data. The flip-flops receive their inputs from the OR array and feed back to the AND array. Outputs from the OR array are also delivered off-chip through inverting output drivers.

The drivers have a static latch with clocked inputs for dynamic-to-static interfacing. Inputs to the chip are two-bit partitioned before addressing the AND array. Two-bit partitioning is an ANDing of pairs of inputs and their complements into four logical combinations. The ANDing and the INVERT function are implemented in the AND array driver section. Table 1 lists the logic functions achievable with two-bit partitioning. It is compared to a non-partitioned input pair to illustrate the increased logic capability.

Circuit description

A schematic diagram of the circuitry is shown in Fig. 2. Four-phase dynamic circuits with nonoverlapping (above circuit switching threshold) clocks were used.

Figure 2 PLA circuit schematic showing the critical delay path through the chip. All of the separate circuits used for the design are included. Significant nodes in the path from chip input to output are numbered for reference to ASTAP analyses as follows: 1) Inverter output, 2) AND array driver bootstrap level, 3) AND array input, 4) OR array driver bootstrap level, 5) OR array input, 6) off-chip driver bootstrap level, 7) pre-driver input, 8) off-chip driver input, and 9) chip output.



The clocks are generated off-chip. A timing diagram for the clocks and data is shown in Fig. 3. The 500-ns clock frame is the minimum allowable PLA operating cycle when all process parameters and supply voltages are skewed to two-sigma worst-case switching values on their Gaussian distributions. The clock rise and fall times from zero to full voltage are shown as 20 ns.

The PLA's performance is achieved by the use of bootstrap circuits driving the arrays and in the output driver section of the chip. The same type of bootstrap circuit is used in all cases, supplying full clock levels to the arrays. It also serves as a noninverting buffer circuit between the arrays, thus enabling array precharging and utilizing the faster (than turn-off) turn-on transition during data processing.

The inputs to the chip must be valid at the start of clock phase 1. The input partitioning circuits are held off until this time. The input inverters have ratioed devices to deliver valid levels from the inputs to the partitioning circuits during phase 1. The bootstrap driver for the AND array is precharged at phase 4 and selectively discharged or left charged during clock phase 1 for bootstrapping. Bootstrapping occurs at phase 2, after which time the input data can be invalid until the start of the next cycle. The AND array and bootstrap driver for the OR array are unconditionally charged at phase 1 and are evaluated at phase 2. The array gates are held low through the bootstrap driver circuits during the precharge phase. The OR array and its drivers are the same types of circuits as used for the AND array but are clocked one clock pulse later in the cycle. The output of the OR array is delivered to either a JK flip-flop or an off-chip driver (OCD) circuit.

The JK circuit employs multiphase clocking to avoid race conditions and is a master/slave type flip-flop.

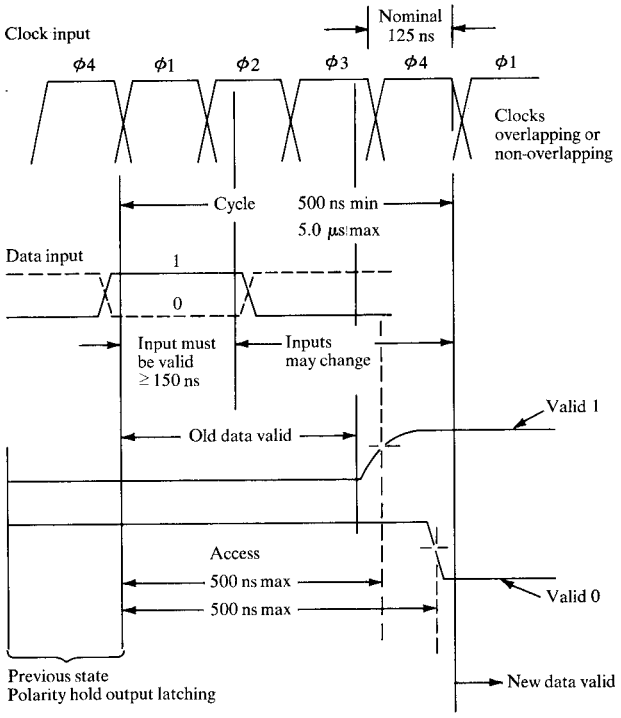


Figure 3 The PLA timing requirements showing four-phase clocking, input and output intervals, and logic levels at a cycle time of 500 nanoseconds.

Outputs from the OR array are first INVERTed with a ratioed circuit clocked at phase 3 time. This supplies the necessary INVERT function after the OR array and enables the precharge of that array while maintaining a low level at the inputs to the JK flip-flop circuit.

Table 1 Functionality of AND array: Two-bit partitioning vs non-partitioning at inputs.

Non-partitioned inputs	A $A \cdot B$	$\overline{A}$ $A \cdot \overline{B}$	B $\overline{A} \cdot B$	$\overline{B}$ $\overline{A} \cdot \overline{B}$	*Two-bit partitioned inputs*
DON'T CARE	0	0	0	0	DON'T CARE
B	0	0	0	1	$A + B$
$\overline{B}$	0	0	1	0	$A + B$
FALSE	0	0	1	1	A
A	0	1	0	0	$\overline{A} + B$
$A \cdot B$	0	1	0	1	B
$A \cdot B$	0	1	1	0	$A \equiv B$
FALSE	0	1	1	1	$A \cdot B$
$\overline{A}$	1	0	0	0	$\overline{A} + \overline{B}$
$\overline{A} \cdot B$	1	0	0	1	$A \oplus B$
$\overline{A} \cdot \overline{B}$	1	0	1	0	$\overline{B}$
FALSE	1	0	1	1	$A \cdot \overline{B}$
FALSE	1	1	0	0	$\overline{A}$
FALSE	1	1	0	1	$\overline{A} \cdot B$
FALSE	1	1	1	0	$\overline{A} \cdot \overline{B}$
FALSE	1	1	1	1	FALSE

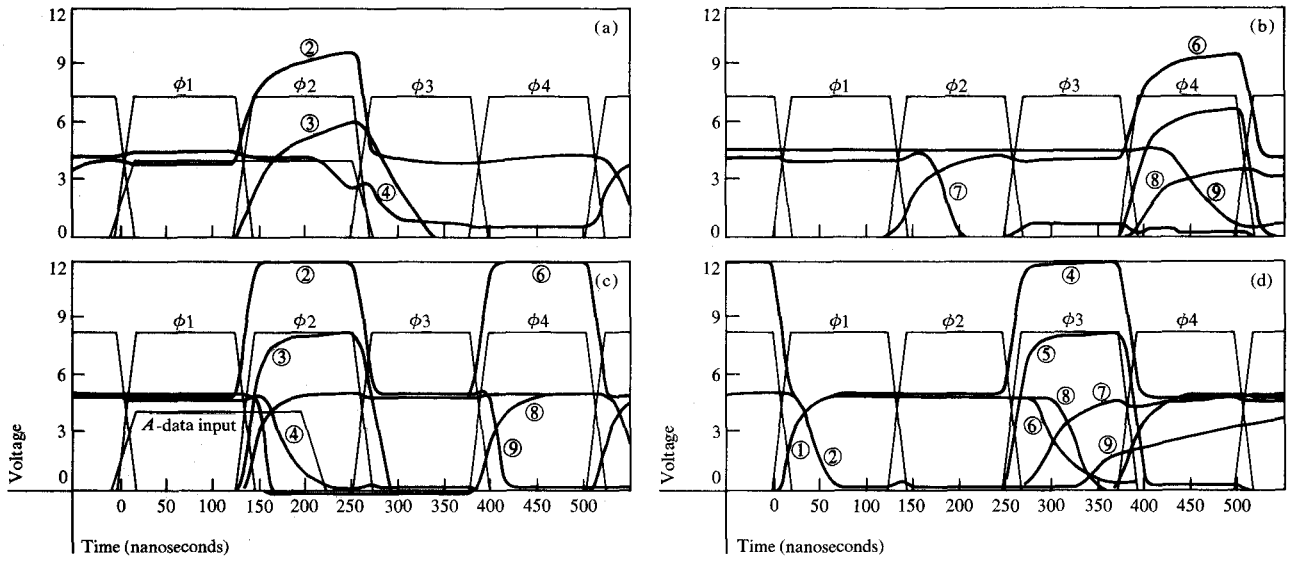


Figure 4 PLA transient response by ASTAP analysis showing one cycle of operation with worst-case skewing (two sigma on Gaussian distribution) of design parameters and typical circuit values. The curves are labeled corresponding to the node designations in Fig. 2. (a) Worst-case discharge of AND array, (b) worst-case discharge of output, (c) typical discharge of AND array and charge of output, and (d) typical discharge of OR array and charge of output.

The master section of the JK is a set/reset latch with positive significance at its inputs. The state of the latch from the preceding cycle is INVERTed and logically ANDed with its respective J or K input before addressing the latch.

Clocked load devices are used in the latch to conserve power. They are ratioed inverters, which permits processing the data through the JK circuit during phase 4. The outputs are delivered to AND array drivers and must be valid by phase 1. A buffer circuit clocked at phase 3 is used to isolate the long lines to the drivers from the internal nodes of the latch.

The OCD circuit provides a polarity hold function at the output to interface directly with static circuits. Its input is obtained from the OR array which is evaluated during phase 3. A valid logic 1 or 0 is attained at the output of the chip by the completion of the cycle. The output level remains the same unless it is changed during a subsequent clock frame.

The circuit is capable of driving either one medium speed DIP-TL circuit or several FET loads. The off-chip resistor is reduced in value to drive FET loads.

The bootstrap capacitor in the output circuit and the OR array are precharged during clock phase 2. The active device in the ratioed circuit is on and maintains a low level at the gate of the lower push-pull device. The output device retains its gate drive and the output inverter holds the same voltage level off-chip.

In the case where the input (OR array line) remains high during phase 3, the bootstrap capacitor has sufficient precharge to enable bootstrap action when phase 4 rises. The gate of the output device is charged to the supply voltage. If it had been high from the preceding clock frame, its charge is replenished at this time. In either case, the output capacitance is discharged to a valid down-level by the completion of the cycle and sufficient charge is retained at the gate of the output device to sink the current from the off-chip resistor and a medium speed DIP-TL circuit.

When the OR array line is discharged during phase 3, the gate of the lower device in the predriver is charged. The output has a necessarily earlier start for turn-off than for turn-on. A valid output 1 is obtained by the end of phase 4.

Circuit analysis

The transient performance of the design was simulated using the Advanced Statistical Analysis Program. The circuits were analyzed with the design parameters both nominal and skewed to two-sigma values on their Gaussian distributions. These values were used separately for each design parameter to obtain extreme worst-case conditions. On-chip tracking figures were assumed where applicable. All significant design parameters were included in the circuit models. The current equations used in the device model were presented by Critchlow et al. [5]. The n-channel technology used was similar to the technology described in their paper.

Figures 4(a) through 4(d) contain output plots of ASTAP simulations of the transient performance of the

design. The curves are labeled corresponding to the node designations in Fig. 2. Data flow from an input, through the arrays, and through an OCD are presented. Switching transitions from logic 1's to 0's for all circuits were modeled. The circuits were cycled for several clock intervals. One cycle of operation is shown. Simulations that were made on the JK flip-flop are not included.

The data path was divided into two sections for the worst-case analysis. Figure 4(a) shows the worst-case discharge of the AND array. The corresponding voltage levels in the OR array and the discharge of the outputs were simulated by a separate analysis shown in Fig. 4(b). The opposite switching conditions for each of the circuits are not shown but were also analyzed with two-sigma design variations. In all cases, the circuitry meets the 500-nanosecond cycle requirement.

Nominal circuit performance at a 500-nanosecond cycle time is shown in Figs. 4(c) and 4(d). For this analysis, the entire delay path through the chip was modeled in the same ASTAP program. The two figures show the two separate sets of switching transitions; a typical cycle time was estimated from these results and verified experimentally to be 230 nanoseconds.

The above data were obtained with typical loading assumed within the arrays. The input to the AND array was assumed to connect to 25 device gates. The product term modeled was the output of a twelve-way NOR circuit. In the analysis, only one of these twelve was driven high. The OR array was assumed to be loaded with 10 input gates and 26 drain loads at its output. The effects of other combinations of internal array loading are shown in Figs. 5(a) and 5(b) for the AND array and the OR array, respectively.

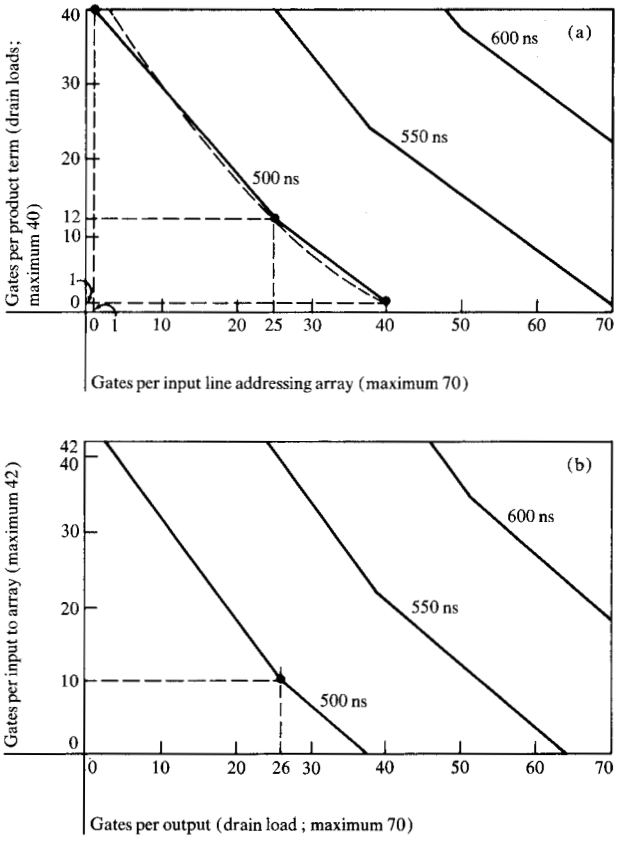


Figure 5 (a) Worst-case cycle time as a function of AND array loading. (b) Worst-case cycle time as a function of OR array loading.

Summary

A programmable logic array chip using FET, four-phase dynamic circuits has been designed and tested by ASTAP analysis and development hardware. The circuit techniques that were employed overcome basic array logic design problems. These include precharged arrays with no logic inversion between them, fast switching transitions to the heavily loaded arrays, and two-bit partitioning of data inputs without increasing the logic steps required. The multiphase clocking enables the use of master/slave type JK flip-flops with minimum circuitry and power dissipation. A polarity hold function is provided in the output driver to allow interfacing the dynamic design to static type output circuits.

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References

1. P. L. Gardner, "Functional Memory and Its Microprogramming Implication," *IEEE Trans. Comput.* **C-18,** 764 (1970).
2. W. N. Carr and J. P. Mize, *MOS/LSI Design and Application*, Texas Instruments Electronics Series, McGraw-Hill Book Company, Inc., New York, 1972, p. 229.
3. H. Fleisher, A. Weinberger, and V. D. Winkler, "The Writable Personalized Chip," *Comput. Des.* **9,** No. 6, 59 (1970).
4. H. Fleisher and L. Maissel, "Introduction to Array Logic," *IBM J. Res. Develop.* **19,** 98 (1975).
5. D. L. Critchlow, R. H. Dennard, and S. E. Schuster, "Design and Characteristics of n-Channel Insulated-gate Field-effect Transistors," *IBM J. Res. Develop.* **17,** 430 (1973).
6. "Advanced Statistical Analysis Program (ASTAP)," IBM User Installed Program, General Information Manual, *Report GH20-1271*, IBM Corporation, White Plains, New York, 1973, unlicensed document available through IBM Branch Offices.
7. J. C. Logue, N. F. Brickman, F. Howley, J. W. Jones, and W. W. Wu, "Hardware Implementation of a Small System in Programmable Logic Arrays," *IBM J. Res. Develop.* **19,** 110 (1975).

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