1904A Mk2/1904S/1903T FLOWCHARTS (CPU)

INDEX

Note:- Those marked * are unavailable at present.

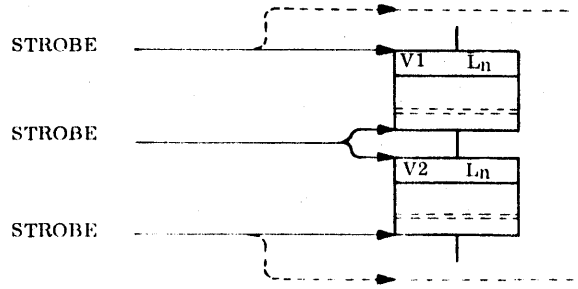
ISSUE 2

1. C.P.U.

The following rules are given as a guide to the interpretation of the 1904A and (C. P. U.) flow charts.

1) Approximate beat durations are indicated by the L classification shown in the upper right hand corner of each beat box. The value of the L classifications is as shown in Section (3). Where a store access is required (VR/VW), the time given assumes immediate store-access - the beat duration will be 'stretached' if the store is busy when first addressed.

2) A C.P.U. strobe is assumed to occur at the entry to and exit from each beat box. The strobe causing exit from one beat will be the same as that causing entry to the next - e.g.

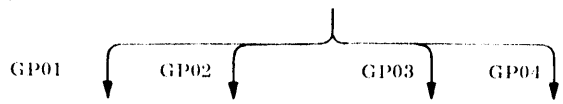


Hence the physical separation of the beat boxes on the charts does not imply any time delay.

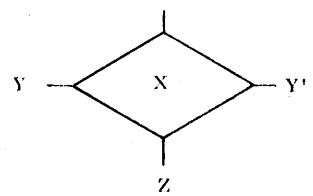
3) Actions shown above the double dotted lines in each box occur at the time of the entry strobe to that box - i.e. they are primed in the preceding beat. Actions below the dotted lines occur at the time of the exit strobe - i.e. they are primed by the entry strobe.

4) Where a path decision has to be taken, either of two formats may be used:

a) If the choice of paths depend purely upon conditions existing in the machine before entry to the flow chart (e.g. if the divergence of paths is a result of the grouping together of two or more similar orders on a single chart), the possible paths diverge from a common point and each is suitably annotated, e.g.



b) If the choice of paths depend upon conditions occurring as a result of operations within the scope of that particular flow chart (e.g. the setting or resetting of overflow in a previous beat, etc.,) the decisive waveform is represented within a diamond. If the state of the waveform denoted within the diamond is fulfilled, exit is made from the bottom apex; if the condition is not fulfilled, exit may be from either side, i.e.



if X, then exit via Z
if X, exit via Y (or Y^1).

In a few instances, all three exits are utilised and in these cases the emergent flowlines are indexed.

Where diamonds are utilised, the conditions determining the flow path will actually have been made during the preceding beat and hence the exit strobe of that beat may be synonymous with the entry strobe of any one of a possible total of three beats, one associated with each path. This means that the exit strobe from the beat wherein the decision is actually made will not occur before that decision as would seem apparent from the lay-out of the flow charts. The diamonds are, however, placed outside the beat boxes for reasons of clarity and the physical space which they occupy does not imply any time delay between strobes.

5) Where a sequence requires two or more sheets, the software 'merge' symbol is used to link subsequent pages.

6) Exit from one chart to another is made via a circle containing the mnemonic of the next sequence, with the FC number appended. The majority of sequences end at EOI and this is not referenced but implies entry to the Instruction Phase (F.C.1).

The only exception to this format for exit is where the machine clock is stopped, for example, due to a parity failure. In this case, waveform DIE is active and this is shown in an elongated circle.

7) The right hand column of each sheet is divided into waveform blocks, one for each of the maximum of five dissimilar beats shown on each sheet. Where two (or more) beats with the same mnemonic occur on the same sheet, only one waveform block is utilised, the small differences between beats being denoted in the conditions column.

The first column of each waveform block contains a list of signals active during a beat, dependent upon the conditions (if any) given in the Conditions column. The centre column lists the monitoring point for each waveform, with the format shown below:-

Plane	Row	Package	Pin No.	E. D. Page
X	X	XX	XX	XXX

Signals above the dotted line are active at the time of the entry strobe and, if staticised, are bracketed. Those below the lines are priming signals for the next beat and are staticised by the exit strobe.

8) The statement of intent (left-hand side of the main sheet) gives a brief description of the main purpose of each beat. This is expanded where necessary in the Comments column to include detailed explanation.

2. PERIPHERAL AUTONOMOUS CONTROL (P. A. C)

The following rules are given as a guide to the interpretation of the flow charts for the 1904A peripheral autonomous control (PAC).

1) Sheets FC200 to FC204 inclusive. These show the microprogram operations by which the various modes of transfer for the peripherals are obtained. They comprise decision diamonds for the microprogram functions and boxes to indicate the steps initiated by them.

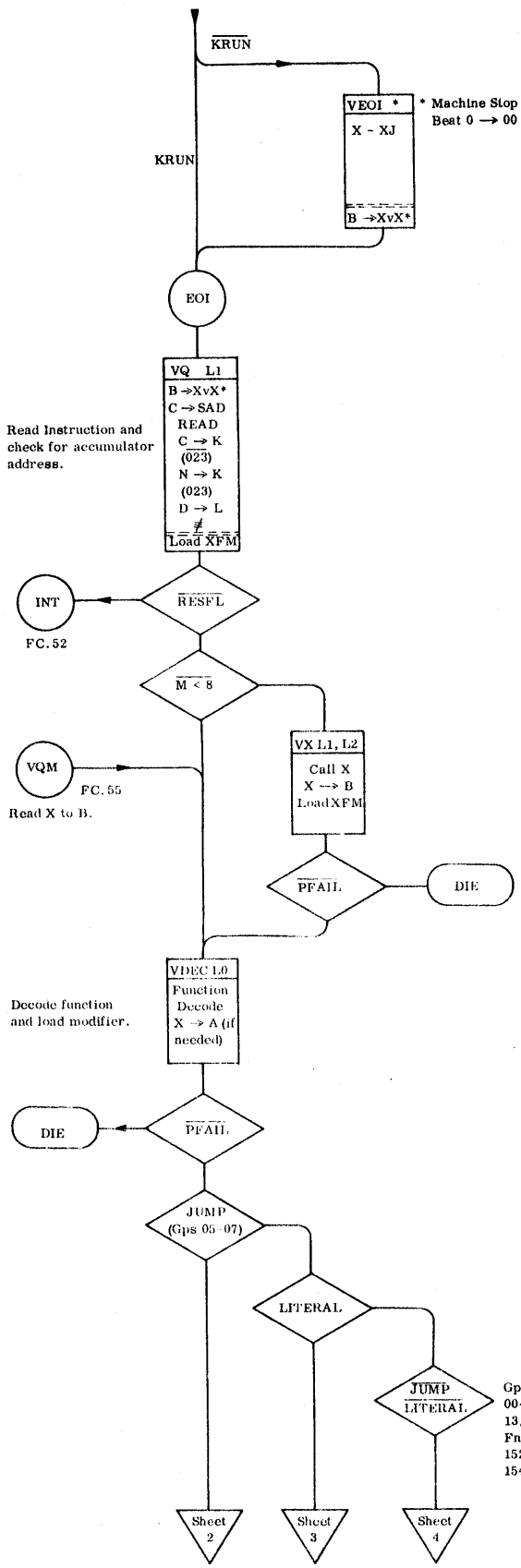
2) Sheet FC205 to FC212 inclusive give details for the various steps. Each step is represented by a box which contains mnemonics to describe the various operations which occur during the step. Each mnemonic is associated with the appropriate E. D. signal name at the right hand side of the chart and suitable comments are included.

Monitoring points for every signal on a chart are shown, together with their locations on the engineering drawings (EDs), in the right-hand column of the chart. The monitoring point in each instance refers to the signal source.

Entry to a step is dependent on the state of several signal inputs to an AND-gate but in general, a step is initiated by one critical signal, the other signals being normally active. In view of this, entry to a step is shown on a chart as being enabled by the critical signal but all the enabling signals for the step together with monitoring information are shown in the monitor signal section of the chart.

3. L CLASSIFICATION - BEAT DURATION TIMES

	1904A	1904S	1903T
L0	340 n. sec	250 n. sec	1450 nS
L1	480 "	300 "	480 nS
L2	= L1	400 "	= L1
L3	1. 2μ. sec	1. 2μ. sec	1. 2μS
L4	2. 3μ. sec	2. 3μ. sec	2. 3μS
L5	3. 4μ. sec	3. 4μ. sec	3.4μS



COMMENTS

VEOI will be entered if the previous order was run on "One Instruction" to allow the results (in B) to be written away to X or X* before the clock is stopped at EOI. In all other cases, KRUN is active, and EOI (and hence V0) is entered directly.

Also active at entry will be EVQ, GDLA, and EEC-SAD (if 023) I117L will be active if the previous order was 117. This puts P (sign extended) into A and P.

VQ: Dependent upon the previous instruction, the residual content of the B register may need to be written to accumulator X or X + 1, the conditions for this being:

B → X if EOI & $\overline{\text{ENDHES}}$ & (CG00$_V$I116$_V$I02N3:6$_V$CG10$_V$I110:2$_V$I170:4E$_V$I12N356).

B → X + 1 if EOI & $\overline{\text{ENDHES}}$ & (I040-3$_V$I111:3$_V$I114:5$_V$I116).

The new instruction is read from the absolute store address held in C (N if the previous order was an 023). During the store cycle this address is gated to the mill and compared, by a non-equivalence operation, with the datum which effectively subtracts the datum from the absolute address. If the remainder is <8, the address refers to a hardware accumulator otherwise to a store location. In either case, the store is read from the absolute address to B. Where M <8 is detected VX is entered; otherwise VDEC will be the next beat. The X, F and M registers are loaded from B by GXFM.

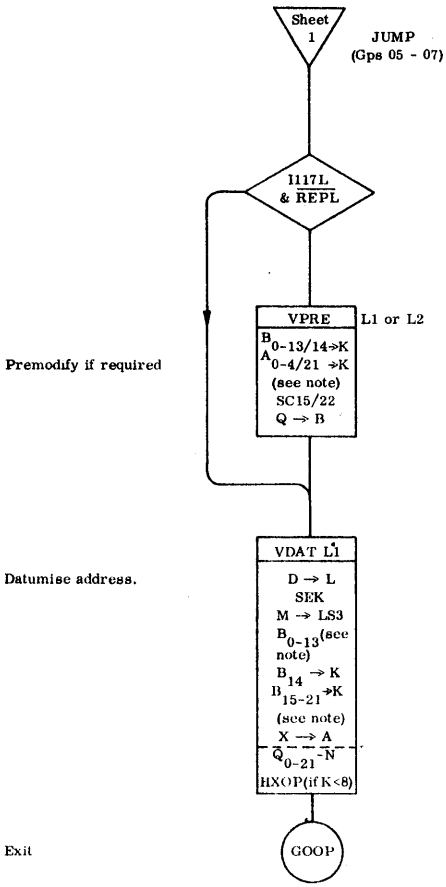
VX: Where M <8 is detected, VX is entered and this reads the contents of the accumulator whose address is held in LS3 (the l. s. 3 bits of the mill). This content overwrites B and X, F and M are also overwritten.

VDEC: decodes the content of the F register to give a signal CFx where x is the function number of the loaded instruction. A sign CGxx is also made where xx is the group number. There are 3 possible paths, as follows:-

EVDAT if: ($\overline{\text{LITERAL}}$ & $\overline{\text{I117L}}$ & RM = 0)$_V$(JUMP & I117L)$_V$ ($\overline{\text{REPL}}$ & JUMP)
EVMOD if: (I117L & LITERAL)$_V$(I117 & $\overline{\text{RM = 0}}$ & JUMP)
EVPRE if: (I117L & $\overline{\text{REPL}}$)

SEK (sign extended onto K) will be active if: (JUMP & I072:3 & EJ & F0 & RFM01)$_V$JUMP & I072:3 & F0 & (EJ$_V$$\overline{\text{CSM}}$).

VEOI / SIGNAL	M.P.	CONDITIONS
ERX - XJ	3F20:4/89	
EBAZ - X	3F25:8/90	} See Comments
EBAZ - X*	3F25:6/90	} See Comments
BEGNI	3C21:6/163	
EVQ	3A13:20/1	
GDLA	3F31:18/74	
EEC - SAD	2F6:18/92	$\overline{023}$
VQ		
(EC-SAD)	3C14:8/167	$\overline{023}$
(EN-SAD)	2E11:3/93	023
READ	2E4:12/162	
(ESIN-B)	6D4:21/248	
ECAX-K	3E10:10/67	$\overline{023}$
ED-L:1	3E21:25/75	$\overline{\text{CPR}}$. $\overline{\text{EXEC}}$
ED-L:2	3E21:22/75	
NEQV	3E21:12/75	
M < 8	2D11:11/142	M < 8
ERX - XJ	3F20:4/89	
(EBAZ-X)	3F25:8/90	} See Comments
(EBAZ-X*)	3F25:6/90	} See Comments
GXFM	2D16:7/60	
EM - LS3	3E19:3/91	
RESFL	2D7:6/32	DORLF
EVDEC	3A11:12/2	$\overline{\text{M < 8}}$
EVX	3A15:12/1	M < 8
VDEC		
CFx	Page 119	} See Comments
CGxx	Pages 120/1	} See Comments
(ERM-XJ)	3D15:25/112	
EHX-A	3D26:18/88	$\overline{\text{RM = 0}}$. $\overline{\text{JUMP}}$
(PCHECK)	3D15:17/112	
EVDAT	3A11:21/2	} See Comments
EVMOD	3A15:21/1	} See Comments
EVPRE	3A17:21/2	} See Comments
$\overline{\text{EECHAN}}$	3A6:9/17A	MODIFY
VX		
ELS3 - XJ	3F19:6/91	
(EHX-B)	3F14:15/87	
(PCHECK)	3D15:17/112	
GXFM	2D16:7/60	
EVDEC	3A11:12/2	
$\overline{\text{EECHAN}}$	3A6:9/17A	MODIFY



When a jump instruction (i.e. one in group 05, 06 or 07) is decoded by VDEQ a test is made for premodification. If required (and not in replaced jump mode) VPRE is entered.

VPRE: The address in B is gated to K and the premodifier is placed on L (from A). The sum of the two is then returned to B.

Note: $B_{0-13} \rightarrow K$
$B_{0-14} \rightarrow K$ if $\overline{EJM}$ v 072/3
SEK from if bit 13 if EJM. $\overline{072/3}$
" " " " 14 if (EJM. 072/3) v ESM. $\overline{EJM}$. 072

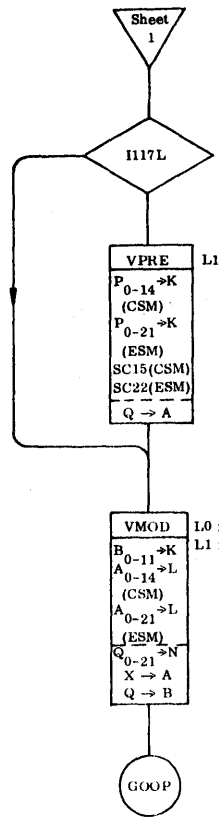
VDAT: The current datum is gated from D onto L and the address is placed on K from B. These are added in the mill and the final (datumised) address is loaded into N from the Q highway.

Note:

$B_{0-13} \rightarrow K$ - ($\overline{EJM}$ + 072/3 + 117L $\overline{PEPL}$
$B_{15-21} \rightarrow K$ - (117L (EJM + $\overline{CSM}$) PEPL + 072/3)

Exit to the relevant instruction microprogram is made via GOOP.

VPRE / SIGNAL	M.P	CONDITIONS
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3F33:23/72	
(EASX-L)	3F33:7/72	$\overline{CSM}$ v EJ
$\overline{EQAJ-B}$	3D13:21/79	
$\overline{EQKM-B}$	3D13:22/79	
$\overline{EQNQ-B}$	3D13:24/79	
$\overline{EQRZ-B}$	3D13:23/79	
EQ-B	3D13:15/79	
EVDAT	3A11:21/2	
GDLA	3F31:18/74	$\overline{072.3}$. $\overline{REL}$
VDAT		
(ED-L:1)	3E21:25/75	GDLA
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	$\overline{EJ}$ v ($\overline{I117L}$ & $\overline{REPL}$
(EBRX-K)	3E7:4/62	ESM & I117L & ($\overline{EJ}$ & CSM92) v (REPL & $\overline{I072:3}$)
$\overline{EQAQ-N}$	3E1:2/83	
EQRX-N	3E1:7/83	
GOOP	2B13:20/9	



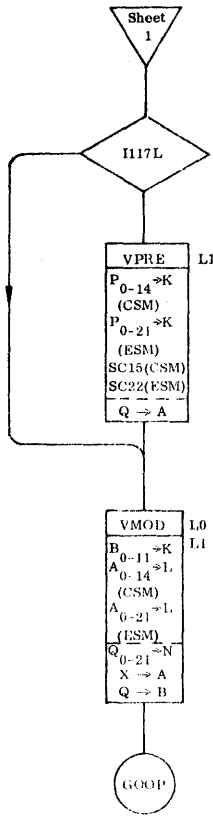
Premodify if required.

Modify

Exit

COMMENTS
VPRE: The N field is premodified by gating it along with the premodifier (in P) to the mill where the two are added. The result is gated to A.
VMOD: The modifier (in B) is added, in the mill, to the N field held in A. The result is strobed to both N and B.
Exit is made via GOOP.

VPRE SIGNAL	MP	CONDITIONS
EPAJ-K	3E9:3/66	$\overline{\text{JUMP}}$
EPKQ-K	3E9:5/66	
EPRX-K	3F9:25/66	$\overline{\text{JUMP}}$ & $\overline{\text{CSM}}$
(EAAQ-L)	3F33:25/72	JUMP & $\overline{\text{RM=0}}$
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	$\overline{\text{JUMP}}$ & $\overline{\text{RM=0}}$4
(EASX-L)	3F33:7/72	$\overline{\text{CSM}}$
SC15	3D15:6/112	EVMOD & CSM
SC22	3D3:22/112	EVMOD
EQAZ-A	3F29:23/81	$\overline{\text{JUMP}}$
EVMOD	3A15:21/1	$\overline{\text{JUMP}}$
VMOD		
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EAAQ-L)	3F33:25/72	$\overline{\text{I117L}}^{\text{V}}$
(EAAQ-L*)	3F33:23/72	$\overline{\text{RM=0}}^{\text{V}}$
(EAR-L)	3F33:21/72	($\overline{\text{I117L}}^{\text{V}}$ &
(EASX-L)	3F33:7/72	$\overline{\text{RM=0}}^{\text{V}}$ & $\overline{\text{CSM}}$
EQNIP2		
$\overline{\text{EQ-N}}$	3E1:8/83	
$\overline{\text{EQAQ-N}}$	3E1:2/83	
EQRX-N	3E1:7/83	
GOOP	2B13:20/9	
EHX-A	3D26:18/88	
EQBIP		
$\overline{\text{EQ-B}}$	3D13:15/79	
$\overline{\text{EQAJ-B}}$	3D13:21/79	
$\overline{\text{EQKM-B}}$	3D13:22/79	
$\overline{\text{EQNQ-B}}$	3D13:24/79	
$\overline{\text{EQRZ-B}}$	3D13:23/79	

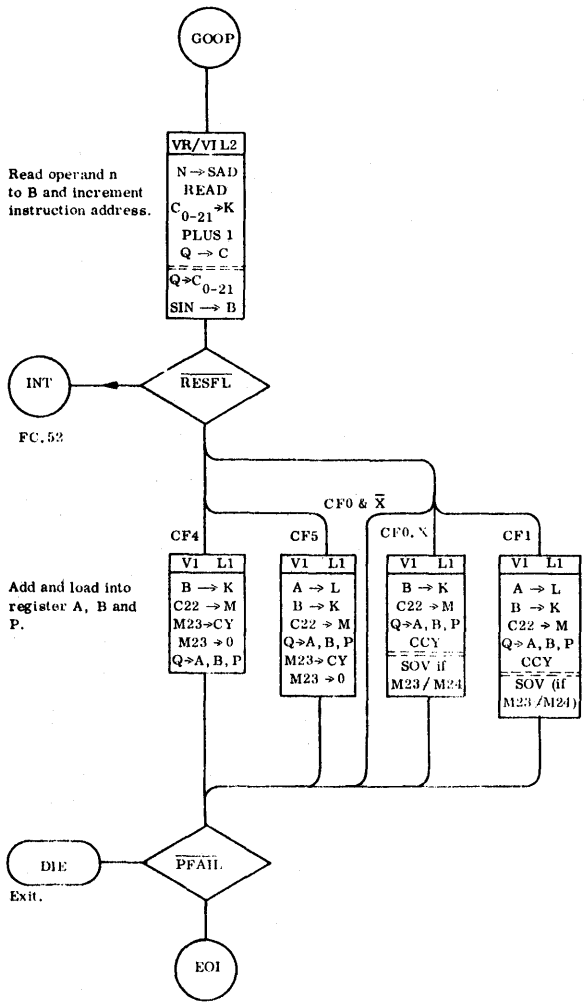


Premodify if required.

Modify

Exit

COMMENTS	VPRE / SIGNAL	MP	CONDITIONS
	ƐPAJ-K	3E9:3/66	$\overline{\text{JUMP}}$
	ƐPBQ-K	3E9:5/66	
	ƐPRX-K	3F9:25/66	$\overline{\text{JUMP}}$ & $\overline{\text{CSM}}$
	(ƐAAQ-L)	3F33:25/72	JUMP & $\overline{\text{RM=0}}$
	(ƐAAQ-L*)	3F33:23/72	
	(ƐAR-L)	3F33:21/72	$\overline{\text{JUMP}}$ & $\overline{\text{RM=04}}$
	(ƐASX-L)	3F33:7/72	$\overline{\text{CSM}}$
	SC15	3L15:6/112	ƐVMOD & CSM
	SC22	3D3:22/112	ƐVMOD
	ƐQAZ-A	5F29:23/81	$\overline{\text{JUMP}}$
	ƐVMOD	5A15:21/1	$\overline{\text{JUMP}}$
	VMOD		
VPRE: The N field is premodified by gating it along with the premodifier (in P) to the mill where the two are added. The result is gated to A.	(ƐBAJ-K)	3F7:26/62	
	(ƐBKM-K)	3F7:24/62	
	(ƐAAQ-L)	3F33:25/72	$\overline{\text{I117L}}^{\text{V}}$
	(ƐAAQ-L*)	3F33:23/72	$\overline{\text{RM=0}}^{\text{V}}$
	(ƐAR-L)	3F33:21/72	$\overline{\text{I117L}}^{\text{V}}$ &
	(ƐASX-L)	3F33:7/72	$\overline{\text{RM=0}}^{\text{V}}$ & $\overline{\text{CSM}}$
	ƐQNIP2		
	ƐQ-N	3E7:8/83	
	$\overline{\text{ƐQAQ-N}}$	3E1:2/83	
	ƐQRX-N	3E1:7/83	
	GOOP	2B13.20/9	
	ƐRX-A	3D26:18/86	
	ƐQPIP		
VMOD: The modifier (in B) is added, in the mill, to the N field held in A. The result is strobed to both N and Q.	ƐQ-B	3D13:15/79	
	$\overline{\text{ƐQAJ-B}}$	3D13:21/79	
	$\overline{\text{ƐQKM-B}}$	3D13:22/75	
	$\overline{\text{ƐQNQ-B}}$	3D13:24/79	
	ƐQAZ-B	3D13:23/79	
Exit is made via GOOP.			



Read operand n to B and increment instruction address.

FC.52

Add and load into register A, B and P.

Exit.

X = (MK I 1904A) or (C22)

i. e. omit V1 of 000 if MK II 1904A and CARRY.

COMMENTS

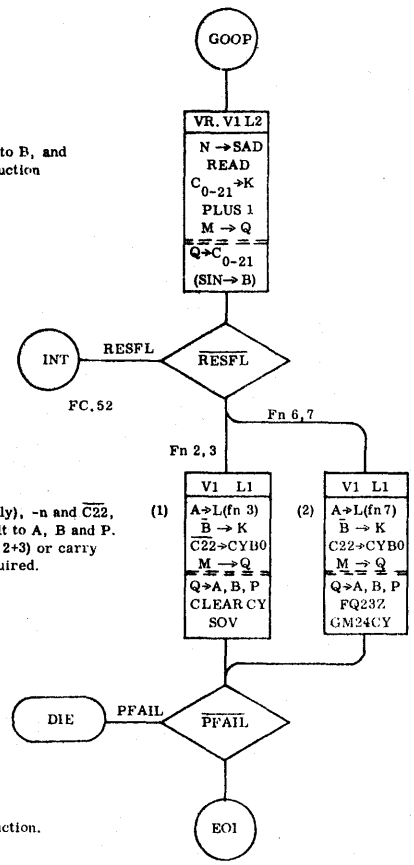
VR & VI: The operand x will be in register A from the Instruction Phase. Operand n is read to B from store location N. The instruction address is incremented by one and returned to register C.

V1: The arithmetic operation is carried out as follows:

000:- C22 + n → A, B & P. Overflow set
001:- C22 + n + x → A, B, & P. Overflow set
004:- as for 000, but carry set
005:- as for 001, but carry set and bit 23 cleared, i. e. (M23 → 0).

Exit occurs at EOI and the content of register B is loaded into accumulator X in the next beat.

VR & VI - SIGNAL	M.P	CONDITIONS
ELS3-XJ	3F19:6/91	HXOP
(EN-SAD)	2E11:3/93	
(READ)	2E4:12/162	
(ESIN-B)	6D4:21/248	
(ECAX-K)	3E10:10/67	
(PLUS 1)	3D24:8/109	$\overline{MAN}$
EQAX-C	3E17:12/25	$\overline{RESFL}$ $\overline{EN\text{-}SAD}$
RESFL	2D7:6/32	DORLF & $\overline{CPR}$
EM-Q	3C14:23/167	& $\overline{EXEC}$
EHX-B	3F14:18/87	HXOP
$\overline{GBKALL}$	3F6:21/61	EV1
GALALL	3D30:3/70	FO
EV1	3A16:12/8	$\overline{RESFL}$
ECYB0	3F2:25/96	
V1		
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBRX-K)	3F7:4/62	
(EBYZ-K)	3F7:25/62	
(EAAQ-L)	3F33:25/72	} F0
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
EQAZ-A	3F29:23/81	
$\overline{EQAJ\text{-}B}$	3D31:21/79	
$\overline{EQKM\text{-}B}$	3D13:22/79	
$\overline{EQNQ\text{-}B}$	3D13:24/79	
$\overline{EQRZ\text{-}B}$	3D13:23/79	
CCY	3F12:18/99	} $\overline{F2}$
SOV	2D7:18/32	
GM23CY	3F11:10/105	CF4:5
FQ23Z	3F22:25/101	F2
(PCHECK)	3D15:17/112	
EOI	2A16:15/41	
EM-Q	3C14:23/167	PGEN-RB24
PFAIL	6A6:21/214	PFAIL.PCHECK
DIE	3B33:25/44	$\overline{INHPFL}$
EBAZ-X	3F25:8/90	$\overline{ENDIES}$

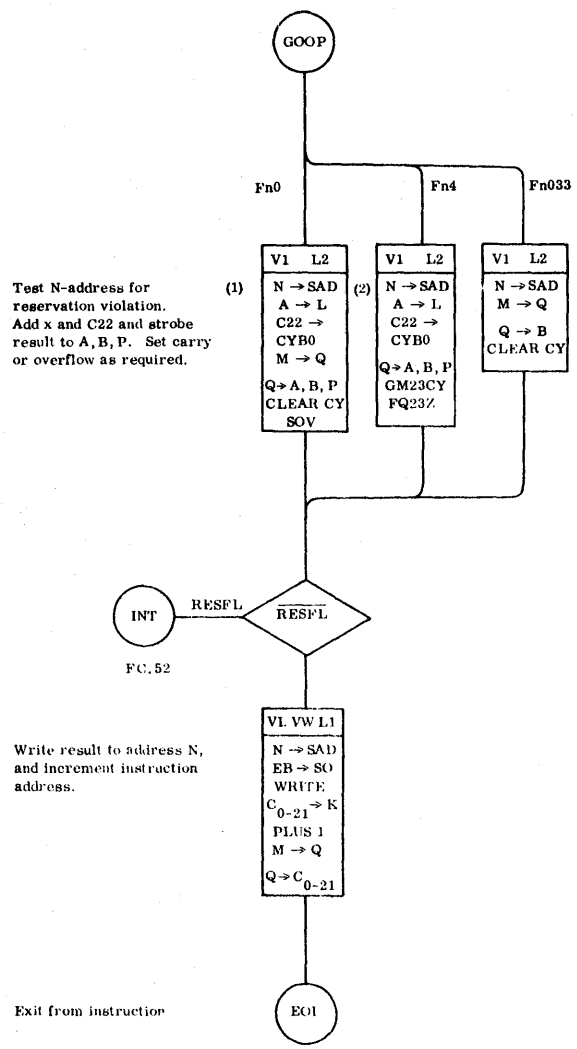


Read operand n to B, and increment instruction address.

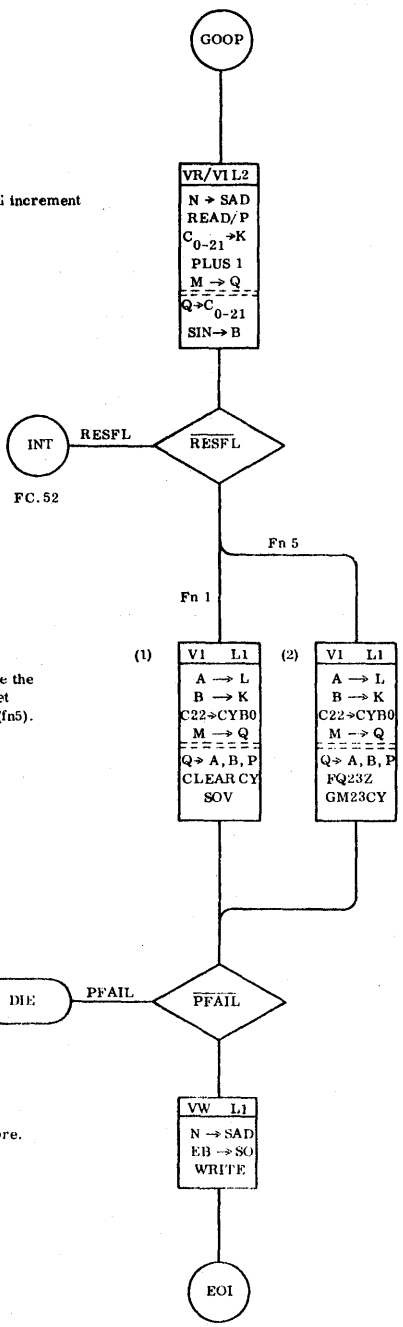
Add x (fn 3+7 only), -n and $\overline{C22}$, and strobe result to A, B and P. Set overflow (fn 2+3) or carry (fn 6+7), as required.

Exit from instruction.

COMMENTS	VLVR SIGNAL	M.P.	CONDITIONS
Relevant signals active in previous beat: EVR, EVI, EESIN-B.			
	(ELS3-XJ)	3F19:6/91	HXOP
	(EN-SAD)	2E11:3/93	
	(ESIN-B)	6D4:21/248	
	(READ)	2E4:12/162	
	(ECAX-K)	3E10:10/67	
	(PLUS 1)	3D24:8/10	
	EM-Q	3C14:23/167	
	EQAX-C	3E17:12/85	$\overline{\text{RESFL}}$
VR, VI: Operand n is read to B from store. The current instruction address is incremented in the mill (PLUS 1 forces data flow CYB0) and restored to C (bits 0-21).	RESFL	2D7:6/32	$\overline{\text{DORLF}}$. $\overline{\text{CPR}}$. $\overline{\text{EXEC}}$
	EHX-B	3F18:18/80	HXOP
	EV1	3A16:12/8	$\overline{\text{RESFL}}$
	GALALL	3D30:3/70	F0 (see comments)
	PNBAZ-K	2F17:24/94	
	EENC22	2E7:12/32	EV1
	V1		
V1:	(PCHECK)	3D15:17/112	
	(EAAQ-L)	3F33:25/72	
	(EAR-L)	3F33:21/72	See comments
	(EASX-L)	3F33:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	(ENBAZ-K)	3D3:9/112	
	(GNC22)	3D3:17/112	
Fn 2+3 (1) operate on a s.l. operand or the m.s. word of a d.l. operand (sets overflow).	PFAIL	6A6:21/214	PGEN=RB24
	DIE	3B33:25/44	PFAIL. PCHECK. $\overline{\text{INHPFL}}$
Fn 6+7 (2) operate on l.s. word of a d.l. operand.	EM-Q	3C14:23/167	
The A → L gating (x in A) is only requested for fns 3 and 7.	EQAZ-A	3F29:23/81	
	EQ-B	3D13:15/79	
	EQAJ-B	3D13:21/79	
1) CCY clears carry from a previous instruction in C22. If M23 ≠ M24, SOV sets overflow in C23.	EQKM-B	3D13:22/79	
	EQNQ-B	3D13:24/79	
	EQRZ-B	3D13:23/79	
2) FQ23Z clears the redundant sign bit from bit 23 of A, B and P. GM24CY sets carry from inverse (carry into mill slice 24).	EQAZ-P	3F3:18/84	
	CCY	3F12:18/99	$\overline{\text{F2}}$
	SOV	2D7:18/32	$\overline{\text{F2}}$
	GM24CY	2D7:9/32	CF6:7
	FQ23Z	3F22:25/101	F2
	EOI	2A16:15/41	
EOI: The result (in B) is written to accumulator X in the next beat.	EBAZ-X	3F25:8/90	$\overline{\text{ENDHES}}$



COMMENTS	V1 SIGNAL	MP	CONDITIONS
Relevant signals active in previous beat: GPB, EV1, ECYB0, GALALL.			
	(EN-SAD)	2E11:3/93	
	(EAAQ-L)	3F33:25/72	
	(EAR L)	3F33:21/72	
	(EASX-L)	3F33:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	EM-Q	3C14:23/167	
	EQAZ-A	3F29:23/81	
	EQ-B	3D13:15/79	
	$\overline{\text{EQAJ-B}}$	3D13:21/79	
	$\overline{\text{EQKM-B}}$	3D13:22/79	
	$\overline{\text{EQNQ-B}}$	3D13:24/79	
	$\overline{\text{EQRZ-B}}$	3D13:23/79	
	EQAZ-P	3F3:18/84	
	CCY	3F12:18/99	$\overline{\text{F2}}$. $\overline{\text{RESFL}}$
	SOV	2D7:18/32	$\overline{\text{F2}}$. $\overline{\text{RESFL}}$
	GM23CY	3F11:10/105	CF4:5
	FQ23Z	3F22:25/101	F2
	RESFL	2D7:6/32	DORLF. $\overline{\text{CPR}}$. $\overline{\text{EXEC}}$
	EVW	2B3:18/3	} $\overline{\text{RESFL}}$
	EVI	2B2:18/-	
	EEB-SO	2F7:17/106	$\overline{\text{IXOP}}$
VW, V1			
V1 Fn0 (1) operates on S. L. operand or m. s. part of d. c. operand (sets overflow). Fn4 (2) operates on l. s. part of d. c. operand. Note that in each case operand x is in A. 1) CCY clears any previous carry from C22, and SOV sets C23 if M23 ≠ M24. 2) Carry is set from bit 23 of the mill output (GM23CY) and the redundant sign bit is cleared from bit 23 of A, B and P (FQ23Z).	(EB-SO)	3F21:9/75	
	(WRITE)	2E4:6/162	
	(EN-SAD)	2E11:3/93	
	(ECAX-K)	3E10:10/67	
	(PLUS 1)	3D24:8/109	
	EM-Q	3C14:23/167	
	EQAX-C	3E17:12/85	$\overline{\text{RESFL}}$
	ELS3-XJ	3F19:6/91	
	EBAZ-X	3F25:8/90	IXOP
	EOI	2A16:15/41	
VW, V1 The result (in B) is written to store address N. The current instruction address is incremented by 1 in the mill (PLUS 1 forces data flow CYB0) and restored to C (bits 0-21).			



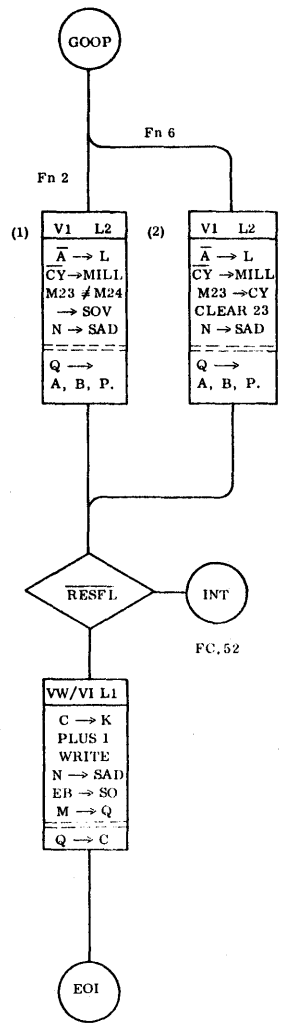
Read operand n to B, and increment instruction address.

Add n, x and c and strobe the result to A, B and P. Set overflow (fn1) or carry (fn5).

Write result (in B) to store.

Exit from instruction.

COMMENTS	VR. VI / SIGNAL	M.F.	CONDITIONS
Relevant signals active in previous beat: EVR, EVI, EESIN-B, GPC.			
	(ESIN-B)	6D4:21/248	$\overline{HXOP}$
	(EN-SAD)	2E11:3/93	
	(READ)	2E4:12/162	
	(ECAX-K)	3E10:10/67	
	(PLUS 1)	3D24:8/109	
	(PAUSE)	2E10:7/143	$\overline{INHPAUS}$
	EM-Q	3C14:23/167	
	ELS3-XJ	3F19:6/91	HXOP
	EHX-B	3F14:18/87	HXOP
	EQAX-C	3E17:12/85	$\overline{RESFL}$
	RESFL	2D7:6/32	$\overline{DORLF}$. $\overline{CPR}$. $\overline{EXEC}$
VR. VI: Operand n is read to B from store. The current instruction address is incremented in the mill (PLUS 1 forces data flow CYB0) and restored to C_{0-21}.			
	EVI	3A16:12/8	$\overline{RESFL}$
	GALALL	3D30:3/70	$\overline{F1}$
	GBKALL	3F6:21/61	$\overline{F0}$
	ECYB0	3F2:25/96	$\overline{F1}$
	V1		
	(PAUSE)	2E10:7/143	
	(PCHECK)	3D15:17/112	
	(EAAQ-L)	3F33:25/72	
	(EAR-L)	3F33:21/72	
	(EASX-L)	3F33:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3F7:24/62	
	(EBNP-K)	3E7:2/62	
	(EBQ-K)	3F7:23/62	
	(EBRX-K)	3F7:4/62	
	(EBYZ-K)	3F7:25/62	
	(GC22)	2F10:25/112	
	PFAIL	6A6:21/214	PGEN = RB24
	DIE	3B33:25/44	PFAIL.PCHECK. $\overline{INHPFL}$
V1: Fn1 (1) operates on a s.l. operand or the m.s. word of a d.l. operand.			
Fn5 (2) operates on the l.s. word of a d.l. operand.			
1) CCY clears carry from a previous instruction in C22. If M23 ≠ M24, SOV sets overflow in C23.			
2) The redundant sign bit is cleared from bit 23 of A, B and P. Carry is set from bit 23 of the mill output (GM23CY).			
	EM-Q	3C14:23/167	
	EQAZ-A	3F29:23/81	
	EB-Q	3D13:15/79	
	$\overline{EQAJ-B}$	3D13:21/79	
	$\overline{EQKM-B}$	3D13:22/79	
	$\overline{FQNQ-B}$	3D13:24/79	
	$\overline{EQRZ-B}$	3D13:23/79	
	EQAZ-P	3F3:18/84	
	CCY	3F12:18/99	$\overline{F2}$
	SOV	2D7:18/32	$\overline{F2}$
	GM23CY	3F11:10/105	CF4:5
	FQ23Z	3F22:25/101	F2
	EVW	2B3:18/3	
	EEB-SO	2F7:17/106	$\overline{HXOP}$
	VW		
	(PAUSE)	2E10:7/143	See Comments
	(EN-SAD)	2E11:3/93	
	(EB-SO)	3F21:9/75	
	(WRITE)	2E4:6/162	
	ELS3-XJ	3F19:6/91	HXOP
	EBAZ-X	3F25:8/90	HXOP
VW: The result (in B) is returned to store at address N.	EOI	2A16:15/41	
PAUSE is reset by UPEOW after approximately 500nS.			



Form - (x + c) and strobe result to A, B and P registers.

Increment instruction address. Write result of operation to store.

COMMENTS

Relevant signals active in previous beat:
GPB, EV1, ECYB0.

V1

Fn 2 (1) deals with s/l or m. s. part of d.l. operand.
Fn 6 (2) deals with l. s. part of d/l operand.

1) CCY forces $\overline{C22}$ —— i.e. clears any carry from previous inst.
If M23 ≠ M24, set overflow i.e. force C23.

2) FQ23Z clears bit 23 of A, B, and P register (not used in d.l. operands. GM24CY = $\overline{M24}$ → CY (C22). The result of the operation in the mill is sent to the A, B, and P registers.

Note:

a) Instead of using PLUS 1 to supply the end correction required by a negative operand, $\overline{CY}$ is produced (GNC22). Thus, $n' = -(x + c) = \bar{x} + c$.

b) GNC22 makes CYB0 in Data Flow if $\overline{RC22}$.

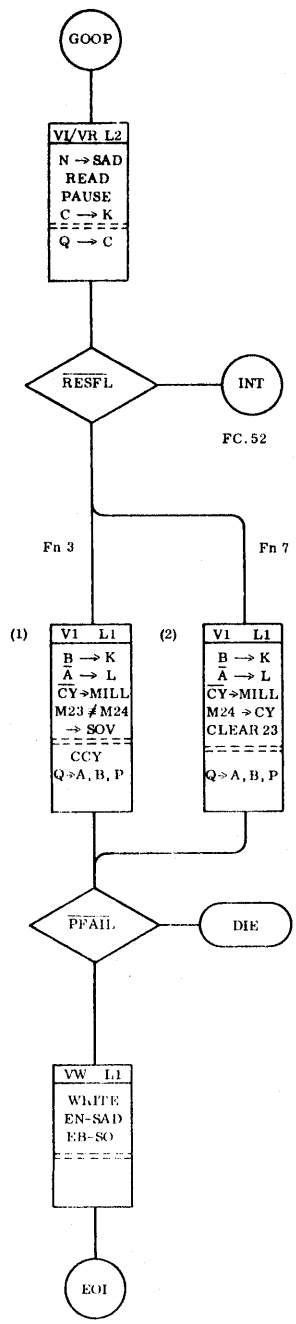
c) If K < 8 detected in instruction phase, HXOP is set and remains set until EOI.

Reservation Fail if D > SAD ≥ L.

VW/VI

Increment instruction address in the Mill and return to C register (PLUS 1) → data flow CYB0.
The store is addressed from the N register and the contents of B written to store.

VI / SIGNAL	M.P.	CONDITIONS
$\overline{ENALALL}$	3D31:7/73	
CCY	3F12:18/99	$\overline{F2}$. $\overline{RESFL}$ & $\overline{GPB}$
(GNC22)	3D3:17/112	
SOV	2D7:18/32	$\overline{F2}$
RC23	6C5:9/226	HM23 ≠ HM24
EM-Q	3C14:23/167	
EQAZ-P	3F3:18/84	
EQ-B	3D13:15/79	
$\overline{EQAJ-B}$	3D13:21/79	
$\overline{EQKM-B}$	3D13:22/79	
$\overline{EQNQ-B}$	3D13:24/79	
$\overline{EQRZ-B}$	3D13:23/79	
EQAZ-A	3F29:25/81	
FQ23Z	3F22:25/101	F2
GM24CY	2D7:9/32	CF6:7
(EN-SAD)	2F11:3/93	
(HXOP)	3C26:23/106	See Comment (c)
RESFL	2D7:6/32	$\overline{DORLF}$. $\overline{CPR}$. $\overline{EXEC}$
EEB-SO	2F7:17/106	$\overline{HXOP}$. EVW
EVI	2B2:18/4	
EVW	2B3:18/3	
VI/VW		
(ECAX-K)	3E10:10/67	
(PLUS 1)	3D24:8/109	
EM-Q	3C14:23/167	
EQAX-C	3E17:12/85	
(EN-SAD)	2E11:3/93	
(EB-SO)	3F21:9/75	$\overline{HXOP}$
WRITE	2E4:6/162	
(HXOP)	3C26:23/160	See Comments
ELS3-XJ	3F19:6/91	
EBAZ-X	3F25:8/90	HXOP
EOI	2A16:15/41	



Read operand n from store to B register and increment instruction address.

Form n - (x + c) and strobe result to A, B and P registers.

Write result (in B) to store.

COMMENTS

Relevant signals made in previous beat:
EVI, GPC, EVR, EESIN-B, ECYB0.

VI/VR: Read operand n from store to B.
Increment inst. addr. (in C) and return to C.

Reservation fail if D > SAD ≥ L.

V1:

Fn 3 (1) deals with s/l or m. s. part of d/l operand.
Fn 7 (2) deals with l. s. part of d/l operand.

1) CCY strobes $\overline{C22}$ - i. e. clears any carry from previous inst. If M23 ≠ M24 set overflow, i. e. force C23.

2) FQ23Z clears bit 23 of A, B and P register (not used in d/l). GM24CY = $\overline{M24}$ → CY (C22).

The result of the operation in the mill is sent to the A, B and P register.

Note

a) Instead of using PLUS 1, to supply the end correction required by a negative operand, $\overline{CY}$ is produced (GNC22). Thus, n' = - (x + c) = $\bar{x}$ + c.

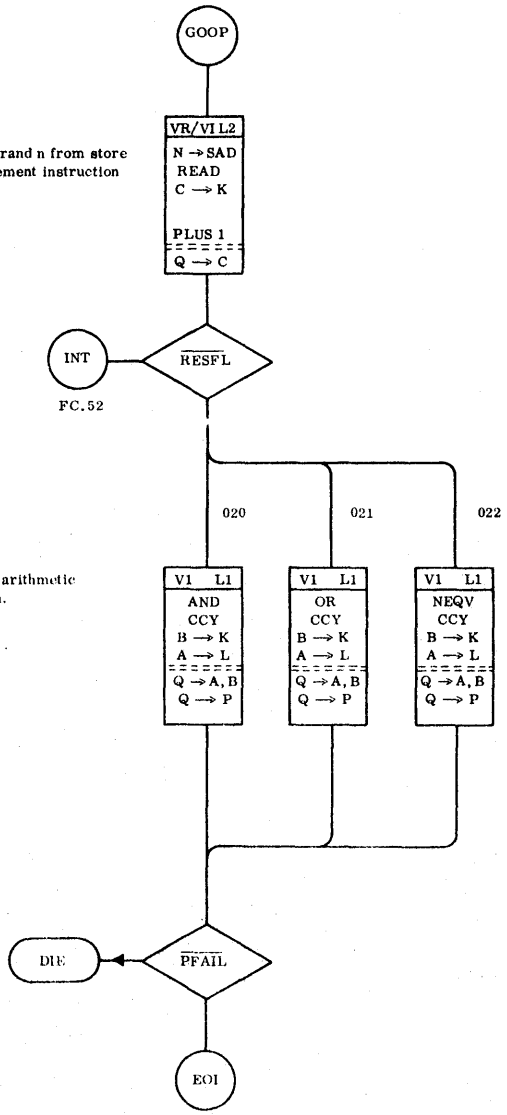
b) GNC22 makes CYB0 in data flow if $\overline{RC22}$.

c) If K < 8 detected in instruction phase, HXOP is set and remains set until EOI.

If parity fail, stop machine strobe (DIE).

Reservation fail if D > SAD ≥ L.

VI/VR SIGNAL	M.P.	CONDITIONS
(EN-SAD)	2E11:3/93	
(HXOP)	3C26:23/160	See Comments (c)
ELS3 XJ	3F19:6/91	HXOP
EHX-B	3F14:18/87	
(ESIN-B)	6D4:21/248	
RI	C5E1:20/284	$\overline{HXOP}$
RR	C5E1:23/284	
(PAUSE)	2E10:7/143	$\overline{HXOP}$. GPC
RESFL	2D7:6/32	DORLF. $\overline{CPR}$. $\overline{EXEC}$
(ECAX-K)	3E10:10/67	
(PLUS 1)	3D24:8/109	
EM-Q	3C14:23/167	
EQAX-C	3E17:12/85	
$\overline{GBKALL}$	3F6:21/61	
$\overline{ENA1ALL}$	3D31:7/73	
EENARXL	3E33:20/102	
EENC22	2E7:12/32	
EVI	2B2:18/5	$\overline{RESFL}$
V1		
(PCHECK)	3D15:17/112	
DIE	3B33:25/44	PCHECK. $\overline{PFAIL}$. $\overline{INHPFL}$
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3F7:4/62	
(EBYZ-K)	3F7:25/62	
(ENAAQ-L)	3C14:7/167	
(ENARX-L)	3D31:5/73	
(ENAYZ-L)	3D31:25/73	
(GNC22)	3D3:17/112	
CCY	3F12:18/99	$\overline{F2}$
SOV	2D7:18/32	$\overline{F2}$.
RC23	6C5:9/226	HM23 ≠ HM24
EM-Q	3C14:23/167	
EQAZ-P	3F3:18/84	
EQAZ-A	3F29:23/81	
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:25/79	
FQ23Z	3F29:25/101	F2
GM24CY	2D7:9/32	CF6:7
(HXOP)	3C26:23/160	See Comments
EEB SO	2F4:17/106	$\overline{HXOP}$. EVW
EVW	2B3:18/5	
VW		
(EN-SAD)	2E11:3/93	
(HXOP)	3C26:23/106	See Comments (c)
ELS3 XJ	3F19:6/91	HXOP
EBAZ-X	3F25:8/90	
EB SO	3F21:9/75	
WI	C5E1:21/284	$\overline{HXOP}$
LR	C5E1:22/284	
EOI	2A16:15/41	



Read operand n from store and increment instruction address.

Perform arithmetic operation.

Exit.

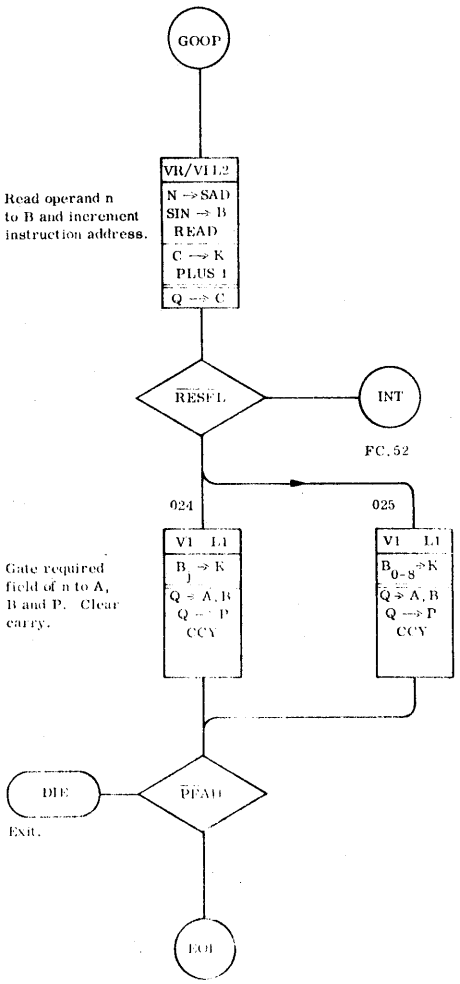
COMMENTS

Also active at entry will be: GPA, EVR, EVI, and EESIN-B.

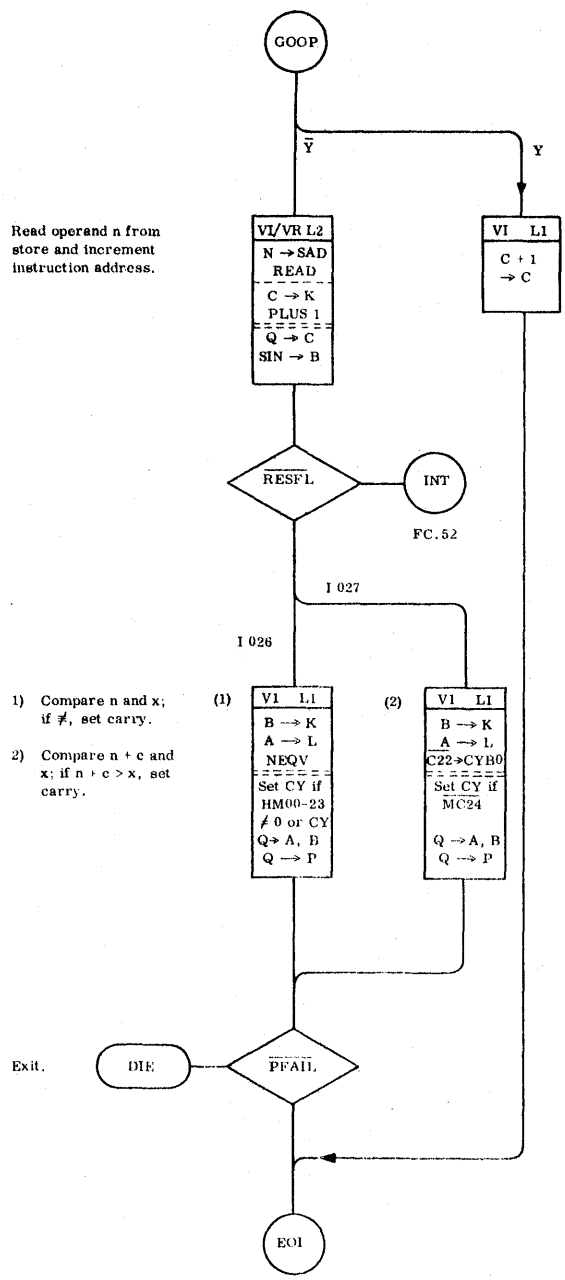
VR/VI: The operand n is read from the store to the B register and the instruction address is incremented and returned to C, operand x (in A from the Instruction Phase) is gated to the mill via the L highway.

V1: An arithmetic operation (AND, OR or NONEQUIVALENCE according to the function) is performed in the mill on x and n and the result gated via Q to the A, B and P registers. The final result of the operation in B is gated to accumulator X in the subsequent Instruction Phase, exit to which is made at EOI.

VR/VI / SIGNAL	M.P.	CONDITIONS
(EN-SAD)	2R11:3/93	
RESFL	2D7:6/32	DORLF & $\overline{\text{CPR}}$ & $\overline{\text{EXEC}}$
(ESIN-B)	6D4:21/248	
$\overline{\text{RI}}$	C5E1:20/284	
$\overline{\text{RR}}$	C5E1:23/284	
ECAX-K	3E10:10/67	
(PLUS 1)	3D24:8/109	
EQAX-C	3E17:12/85	
$\overline{\text{GBKALL}}$	3F6:21/61	
GALALL	3D30:3/70	
EVI	3A16:12/8	
EAND	2D18:25/95	CF0
EOR	3B33:12/44	CF1
ENEQV	3D20:17/107	CF2
V1		
(PCHECK)	3D15:17/112	
(AND)	3E21:6/75	CF0
(OR)	3D3:11/112	CF1
(NEQV)	3E21:12/75	CF2
CCY	3F12:18/99	
EQAZ-P	3F3:18/84	
EQ-B	3D13:15/79	
EQAZ-A	3F29:23/81	PFAIL & $\overline{\text{INHPFL}}$
DIE	3B33:25/44	
EOI	2A16:18/41	
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3F7:4/62	
(EBYZ-K)	3F7:25/62	
(EAAQ-L)	3F33:25/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	



COMMENTS	VR/VI SIGNAL	MP	CONDITIONS
Also active at entry will be: EVR, EVI, EESIN-B and GPA.			
	(EN-SAD)	2E11:3/93	
	READ	2E4:12/167	
	(ESIN-B)	6D4:21/248	
	ECAX-K	3E10:10/6[illegible]	
	(PLUS 1)	3D24:8/109	
	EQAX-C	3E17:12/86	
	EVI	3A16:12/8	
	EEBJ-K	3D7:17/71	I024
	EVI:25	/62	I025
	VI		
	(EBJ-K)	3E21:17/75	I024
	(EBAJ-K)	3F7:26/62	I025
VR/VI: The operand n is read from store to register B. During the store cycle, the instruction address is updated and returned to C.	EQAZ-A	3F29:23/81	
	EQAZ-P	3F3:18/84	
	EQAJ-B	3D13:21/79	
	EQKM-B	3D13:22/79	
	EQNQ-B	3D13:24/79	
	EQRZ-B	3D13:23/79	
	CCY	3F12:18/99	
	EOI	2A16:15/41	
V1: a) 024: a character B_J of the operand n is gated via K and the mill to A, B and P. b) 025: the n_e field (the l.s. 9 bits of n) is gated via K and the mill to A, B and P. In the Instruction Phase which follows (entered at EOI) the required n field is gated to the selected accumulator X.			



Read operand n from store and increment instruction address.

1) Compare n and x; if ≠, set carry.

2) Compare n + c and x; if n + c > x, set carry.

Exit.

Also active at entry will be:
EV1, CG02, CF6:7, GPA, EESIN-B and I026 or I027.

Y = 026 & $\overline{\text{MKI 1904A}}$ & C22

VI: Operand n is read from store to B. During the store cycle, the instruction address is incremented and returned to C.

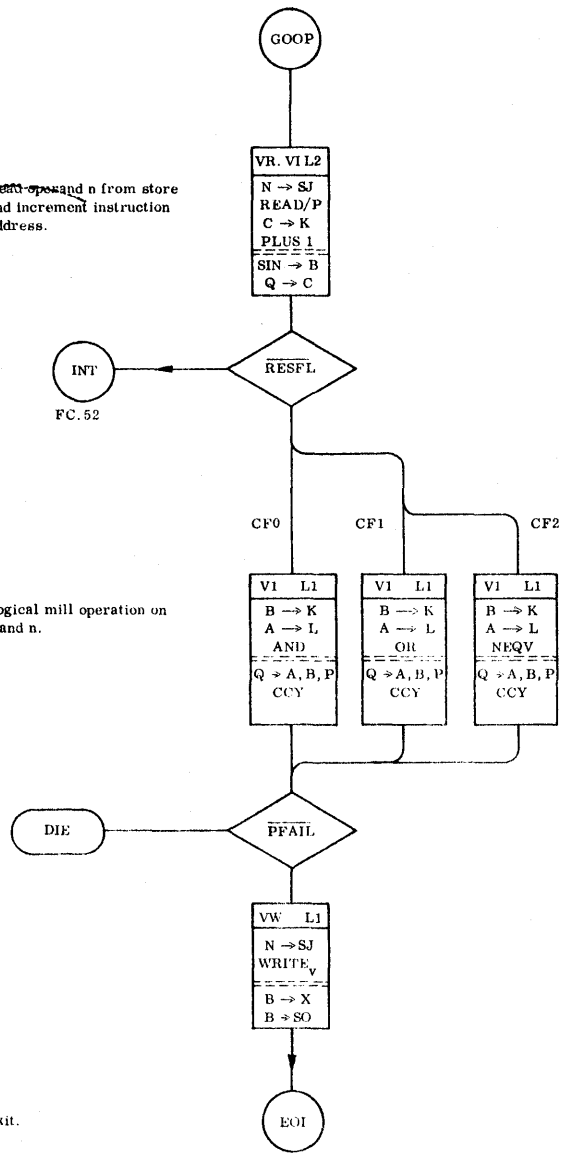
V1:

1) 026: n (in B) and x (in A from the previous Instruction Phase) are gated to the mill where a non-equivalence test is performed. If non-equivalence is found, carry (C22), is set.

2) 027: n + c is subtracted from x by gating $\overline{\text{n}}$ (i.e. B) and A to the mill and adding them. Carry is set in mill bit 23 (HM23) is a 1 i.e. if n + c > x.

In both cases, the content of the mill is gated to the A, B and P registers. Exit is made to the Instruction Phase at EOI.

COMMENTS	VI SIGNAL	M.P.	CONDITIONS
	(EN-SAD)	2E11:3/93	
	(READ)	2E4:12/162	
	(ESIN-B)	6D4:21/248	
	ECAX-K	3E10:10/67	
	(PLUS 1)	3D24:8/109	
	EQAX-C	3E17:12/85	
	EV1	3A16:12/8	
	GALALL	3D30:3/70	
	$\overline{\text{GBKALL}}$	3F6:21/61	
	PNBAZ-K	2F17:24/94	
	EENC22	2E7:12/32	
	V1		
	(EAAQ-L)	3F33:25/72	
	(EAAQ-L*)	3F33:23/72	
	(EAR-L)	3F33:21/72	
	(EASX-L)	3F33:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3F7:24/62	
	(EBNP-K)	3E7:2/62	I026
	(EBQ-K)	3F7:23/62	
	(EBRX-K)	3F7:4/62	
	(EBYZ-K)	3F7:25/62	
			I027
	EQAZ-A	3F29:23/81	
	$\overline{\text{EQAZ-P}}$	3F3:18/84	
	$\overline{\text{EQAJ-B}}$	3D13:21/79	
	$\overline{\text{EQKM-B}}$	3D13:22/79	
	$\overline{\text{EQNQ-B}}$	3D13:24/79	
	GM24CY	2D7:9/32	I027
	GNC22	3D3:17/112	
	$\overline{\text{ENBAZ-K}}$	3D3:4/112	
	$\overline{\text{EQRZ-B}}$	3D13:23/79	
	EOI	2A16:15/41	

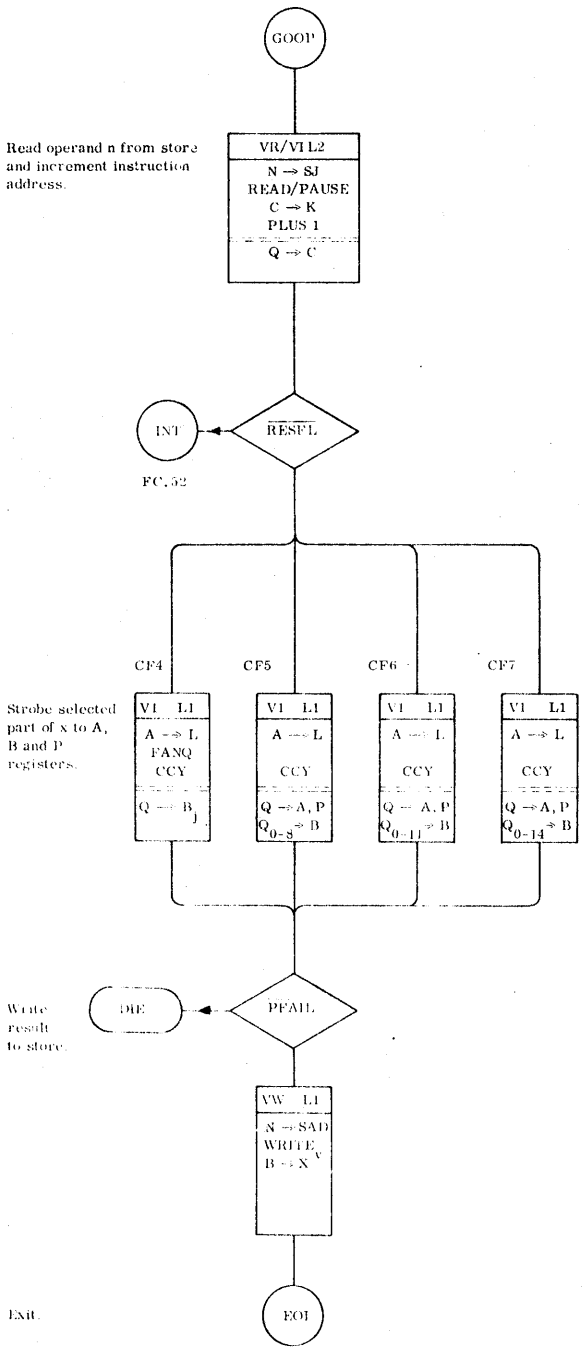


Read operand n from store and increment instruction address.

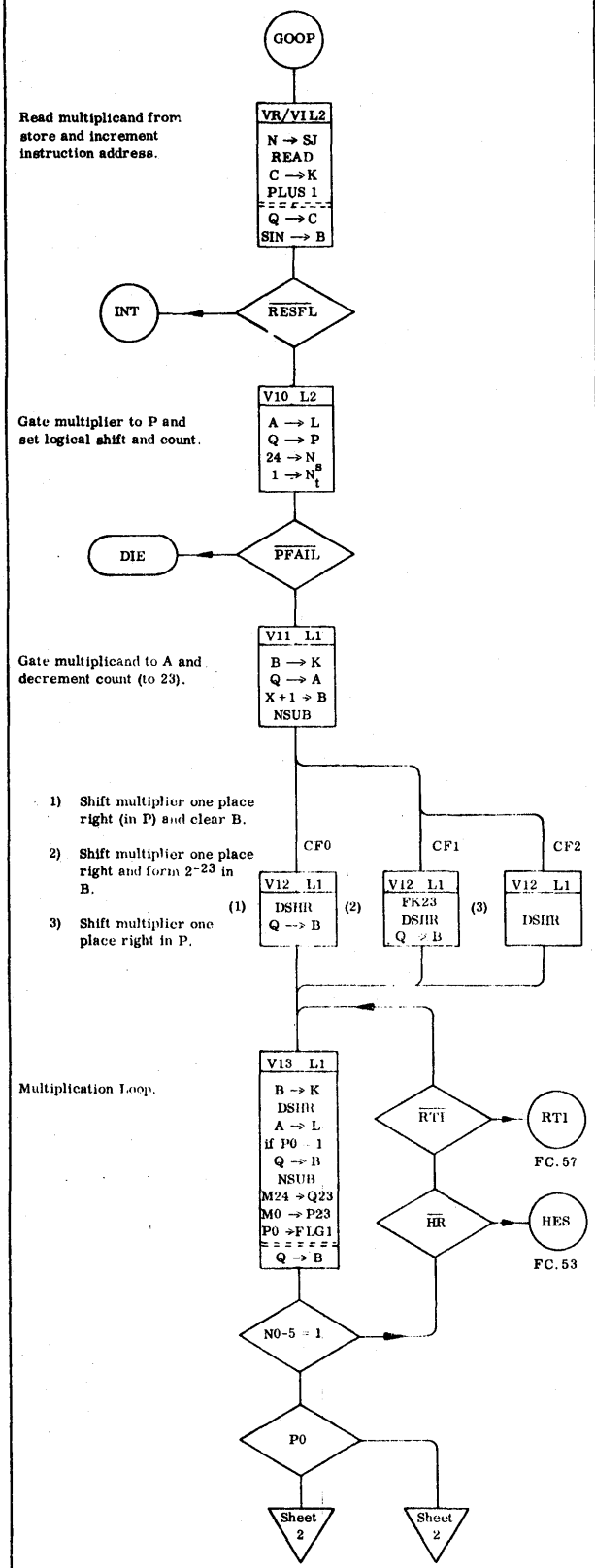
Logical mill operation on x and n.

Exit.

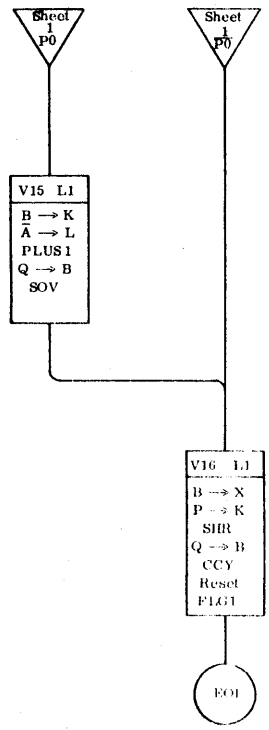
COMMENTS	VR & VI / SIGNAL	M.P.	CONDITIONS
	(EN-SAD)	2E11:3/93	
	(ESIN-B)	6D4:21/248	} $\overline{\text{HXOP}}$
	(READ)	2E4:12/162	
	ELS3-XJ	3F19:6/91	} HXOP
	EHX-B	3F14:18/87	
	(ECAX-K)	3E10:10/67	
	(PLUS1)	3D24:8/109	$\overline{\text{MAN}}$
	EQAX-C	3E17:12/85	$\overline{\text{RESFL}}$
	RESFL	2D7:6/32	DORLF & $\overline{\text{CPR}}$ & $\overline{\text{EXEC}}$
	EM-Q	3C14:23:167	
	$\overline{\text{GBKALL}}$	3F6:21/61	
	GALALL	3D30:3/70	
	EAND	2D18:25/95	CF0
	EOR	3B33:12/44	CF2
	ENEQV	3D20:17/107	CF1
	EVI	3A16:12/8	
VR & VI: The store is accessed at the N address and operand n is read to B. Operand x is in A from the Instruction Phase. VI increments the instruction address and returns it to C. GBKALL and GALALL prime B → K and A → L respectively.			
	VI		
	(EBQ-K)	3F7:23/62	
	(PCHECK)	3D15:17/112	$\overline{\text{HXOP}}$
	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3F7:24/62	
	(EBNP-K)	3E7:2/62	
	(EBRX-K)	3F7:4/62	
	(EBYZ-K)	3F7:25/62	
	(EAAQ-L)	3F33:25/72	
	(EAAQ-L*)	3F33:23/72	
	(EASX-L)	3F33:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	(EAR-L)	3F33:21/72	
	CCY	3F12:18/99	
	(NEQV)	3E21:12/75	CF2
	(AND)	3E21:6/75	CF0
	(OR)	3D3:11/11	CF1
	EQAZ-A	3F29:23/81	
	EQAZ-P	3F3:18/84	
V1: A and B are gated to L and K respectively and thus appear in the mill. A logical AND, OR or NONEQUIVALENCE operation is performed on the operands and the result is strobed to A, B and P. The result must be in B for writing to store, but is also placed in A and P for the sake of uniformity of the V1 beats. (The 023 and 117 must have a copy of the result of V1 in A and p in case of interrupt).	$\overline{\text{EQAJ-B}}$	3D13:21/79	
	$\overline{\text{EQKM-B}}$	3D13:22/79	
	$\overline{\text{EQNQ-B}}$	3D13:24/79	
	$\overline{\text{EQRZ-B}}$	3D13:23/79	
	EEB-SO	2F7:17/106	
	EVW	2B3:18/3	
	VW		
VW: The result is written to the store location held in N (or to an accumulator addressed by LS3 which would have been loaded from the mill in the Instruction Phase).	(EN-SAD)	2E11:3/93	} $\overline{\text{HXOP}}$
	(EN-SO)	3F21:9/75	
	(WRITE)	2E4:6/162	
	ELS3-XJ	3F19:6/91	} HXOP
	EBAZ-X	3F25:8/90	
	EOI	2A16:15/41	



COMMENTS	VR& / SIGNAL	MP	CONDITIONS
Also active at entry will be EEN-SAD, CG03, CF4:6, CF4-7, I034-7, I036:7, I035:7, etc.,			
	(EN-SAD)	6D4:21/248	$\overline{\text{INHPAUSE}}$
	(ESIN-B)	6D4:21/248	$\overline{\text{HXOP}}$
	(READ)	2E4:12/162	
	ELS3-XJ	3F19:6/19	
	EHX-B	3F14:18/87	HXOP
	(ECAX-K)	3E10:10/67	
	(PLUS 1)	3D24:8/109	$\overline{\text{MAN}}$
	EQAX-C	3E17:12/85	$\overline{\text{RESFL}}$ & $\overline{\text{EN-SAD}}$
VR/VI: The operand n is read from store location N to register B. The instruction address is updated by one and returned to C.	RESFL	3D7:6/32	DORLF & $\overline{\text{CPR}}$ & $\overline{\text{EVEC}}$
	GALALL	3D30:3/70	
	EVI	3A16:12/8	
	VI		
	(PCHECK)	3D15:17/112	$\overline{\text{HXOP}}$
	(EAAQ-L)	3F33:25/72	
	(EAAQ-L*)	3F33:23/72	
	(EAR-L)	3F33:21/72	
	(EASX-L)	3F33:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	EQAZ-A	3F29:23/81	
	EMFAN	3F28:17/104	I034
	EB-BJ	3E18:19/80	
	$\overline{\text{EQAJ-B}}$	3D13:21/79	I035:7
	$\overline{\text{EQKM-B}}$	3D13:22/79	I036:7
	$\overline{\text{EQNQ-B}}$	3D13:24/79	I037
	EQ-B	3D13:15/79	
	EEB-SO	2F7:17/106	
	EVW	2B5:18/3	
	VW		
VI: The A register (containing x loaded in the Instruction Phase) is gated to the mill and a selected portion of it is gated as follows: 034 : (Q0-5) ⟶ B_j 035 : (Q0-8) ⟶ A_j^j, B, P 036 : (Q0-11) ⟶ A, B, P to B partially. 037 : (Q0-14) ⟶ A, B, P to A and P totally. For the 034, the l.s. 6 bits of the mill are fanned to Q and one strobed to B_j. Carry is cleared in all cases. The required character is strobed to B to be written away in the next beat and is also placed in A and P. The latter is performed for the sake of uniformity of all VI beats; the 023 and 117 orders must have the result of VI in A and P in case of interrupt or hesitation.	(EN-SAD)	2E11:3/93	
	(EB-SO)	3F24:9/75	$\overline{\text{HXOP}}$
	(WRITE)	2E4:6/162	
	ELS3-XJ	3F19:6/91	
	EBAZ-X	3F25:8/90	HXOP
	EOI	2A16:10/11	
VW: The result of VI is written to the store location held in N (or to an accumulator addressed by LS3 which would have been loaded from the mill in the Instruction Phase).			



COMMENTS	VR/VI SIGNAL	M.P.	CONDITIONS
Also active at entry will be EVR, EVI, GCKALL, EQCALL, I040-2 and CF0, 1 or 2 as appropriate.			
	(EN-SAD)	2E11:3/93	
	(READ)	2E4:12/162	
	(ESIN-B)	6D4:21/248	
	RESFL	2D7:6/32	DORLF & $\overline{\text{CPR}}$ & $\overline{\text{EXEC}}$
	(ECAX-K)	3E10:10/67	
	(PLUS 1)	3D24:8/109	$\overline{\text{MAN}}$
	EQAX-C	3E17:12/85	$\overline{\text{RESFL}}$
	EV10	2A5:9/13	$\overline{\text{RESFL}}$
	GALALL	3D30:3/70	EV10
	EV33	3B20:20/33	RESFL
VR & VI: Q to C gating is inhibited if there is a reservation failure (RESFL).	V10		
	(EAAQ-L)	3F33:25/72	
	(EAAQ-L*)	3F33:23/72	
	(EAR-L)	3F33:21/72	
	(EASX-L)	3F33:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	EQAZ-P	3F3:18/84	
	FN24	3D29:13/113	
	FNT1	2D18:8/95	
	$\overline{\text{EV11}}$	2A6:16/14	
	$\overline{\text{GBKALL}}$	3F6:21/61	
V10: The multiplier (x) is available in A from the Instruction Phase and is gated to P. The count (N_s) is set to 24 and a logical shift specified (i.e. N_t = 1).	V11		
	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3F7:24/62	
	(EBNP-K)	3E7:2/62	
	(EBQ-K)	3F7:23/62	
	(EBRX-K)	3R7:4/62	
	(EBYZ-K)	3F7:25/62	
	EQAZ-A	3F29:23/81	
	EHX-B	3F14:18/87	
	NSUB	3F18:21/80	
V11: The multiplicand (n) is gated to A and the count decremented to 23 (NSUB). Register B is loaded with x* for the 042 instruction.	EV12	3B11:10/15	
	V12		
	$\overline{\text{EQAJ-B}}$	3D13:21/79	} I040:1
	$\overline{\text{EQKM-B}}$	3D13:22/79	
	$\overline{\text{EQNQ-B}}$	3D13:24/79	
	$\overline{\text{EQRZ-B}}$	3D13:23/79	
	EQ-B	3D13:15/79	
	DSHR	2C9:13/42	
	$\overline{\text{FK23}}$	3D5:6/69	I041
V12: 1) B is cleared to give a first partial product of zero. 2) B is forced to 2^{-23} to form the rounding fraction.	EV13	2A18:5/16	
	GBKALL	3F6:21/61	
	GALALL	3D30:3/70	(P0 & $\overline{\text{ENDHES}}$) (FLG1 & ENDHES)
	V13		
V13: The multiplicand (n) is added to the previous partial product in the mill if the l.s. multiplier bit (P0) is 1. For the first loop, n is added to the content of B which contains either zero (040), 2^{-24} (041) or x* (042). A double right shift is performed, the l.s. bit of the mill being gated to the m.s. bit of P. This loop is repeated 23 times (i.e. until the count is N0-5 equals 1). After all 23 cycles, B will hold the m.s. part of the final product. M24 is gated onto 023 (vacant as a result of the shifting operation) for input to B as the addition of the multiplicand and cumulative partial product may result in overflow into M24. The 'flag' bistable FLG1 is set if the l.s. multiplier bit (P0) is 1, to maintain a record of it during any subsequent hesitation. A hesitation break-point and RTI exit point are provided at the end of each cycle of the loop.	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3F7:24/62	
	(EBNP-K)	3E7:2/62	
	(EBQ-K)	3F7:23/62	
	(EBRX-K)	3F7:4/62	
	(EBYZ-K)	3F7:25/62	
	DSHR	2C9:13/42	
	(EAAQ-L)	3F33:25/72	} (P0 & $\overline{\text{ENDHES}}$)
	(EAAQ-L*)	3F33:23/72	
	(EAR-L)	3F33:21/72	} v (FLG 1 & ENDHES)
	(EASX-L)	3F33:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	EM24Q23	3D17:9/22	M24 = Q23
	SETFLG1	3C30:10/150	P0
	FLG 1	3C32:24/152	See Comments
	EV15	2A18:5/16	RTI & N0-5 = 1 & HR
	HESBKPT	2B15:25/47	
	EV17	2A10:3/21	$\overline{\text{N0-5 = 1}}$. RTI. $\overline{\text{HR}}$
	EV16	2A9:9/20	N0-5 = 1
	$\overline{\text{EV15}}$	2A8:9/19	
	$\overline{\text{GBKALL}}$	3F6:21/61	N0-5 = 1 & P0
	ENALALL	3D31:7/72	N0-5 = 1 & P0
	EENARX-L	3E33:20/102	EV15
	EPKALL	/66	EV15 EV16



Subtract multiplicand from final cumulative partial product.

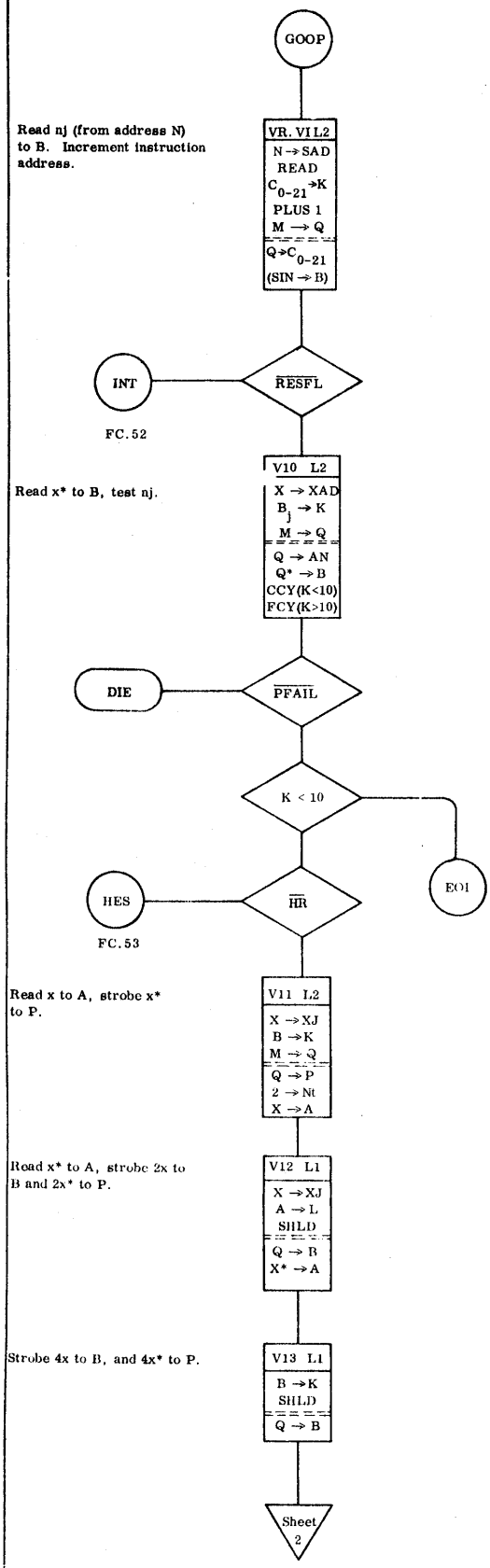
Write m.s. half of final product to X and clear carry and flag bistables.

Exit.

V15: Overflow is set if M23 ≠ M24. This beat occurs only for a negative multiplier.

V16: The l.s. half of the result is subject to a final right shift in the mill and is written to accumulator X + 1 in VQ of the subsequent Instruction Phase.

COMMENTS	V15 SIGNAL	MP	CONDITIONS
	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3F7:24/62	
	(EBNP-K)	3E7:2/62	
	(EBQ-K)	3F7:23/62	
	(EBRX-K)	3F7:4/62	
	(EBYZ-K)	3F7:25/62	
	(ENAAQ-L)	3C14:7/167	
	(ENARX-L)	3D31:5/73	
	(ENAYZ-L)	3D31:25/73	
	(PLUS 1)	3D24:8/109	
	$\overline{\text{EQAJ}}$-B	3D13:21/79	
	$\overline{\text{EQKM}}$-B	3D13:22/79	
	$\overline{\text{EQNQ}}$-B	3D13:24/79	
	$\overline{\text{EQRZ}}$-B	3D13:23/79	
	EQ-B	3D13:15/79	
	SOV	2D7:18/32	
	EV16	2A9:9/20	
	EPKALL	/66	
	V16		
	EBAZ-X	3F25:8/90	
	(EPAJ-K)	3E9:3/66	
	EPKQ-K)	3E9:5/66	
	(EPRX-K)	3F9:25/66	
	(EPYZ-K)	3F9:23/66	
	SHR	3F26:10/97	
	$\overline{\text{EQAJ}}$-B	3D13:21/79	
	$\overline{\text{EQKM}}$-B	3D13:22/79	
	$\overline{\text{EQNQ}}$-B	3D13:24/79	
	$\overline{\text{EQRZ}}$-B	3D13:23/79	
	EQ-B	3D13:15/79	
	CCY	3F12:18/99	
	RSTFLG1	3C31:10/150	
	EOI	2A16:15/41	



Read nj (from address N) to B. Increment instruction address.

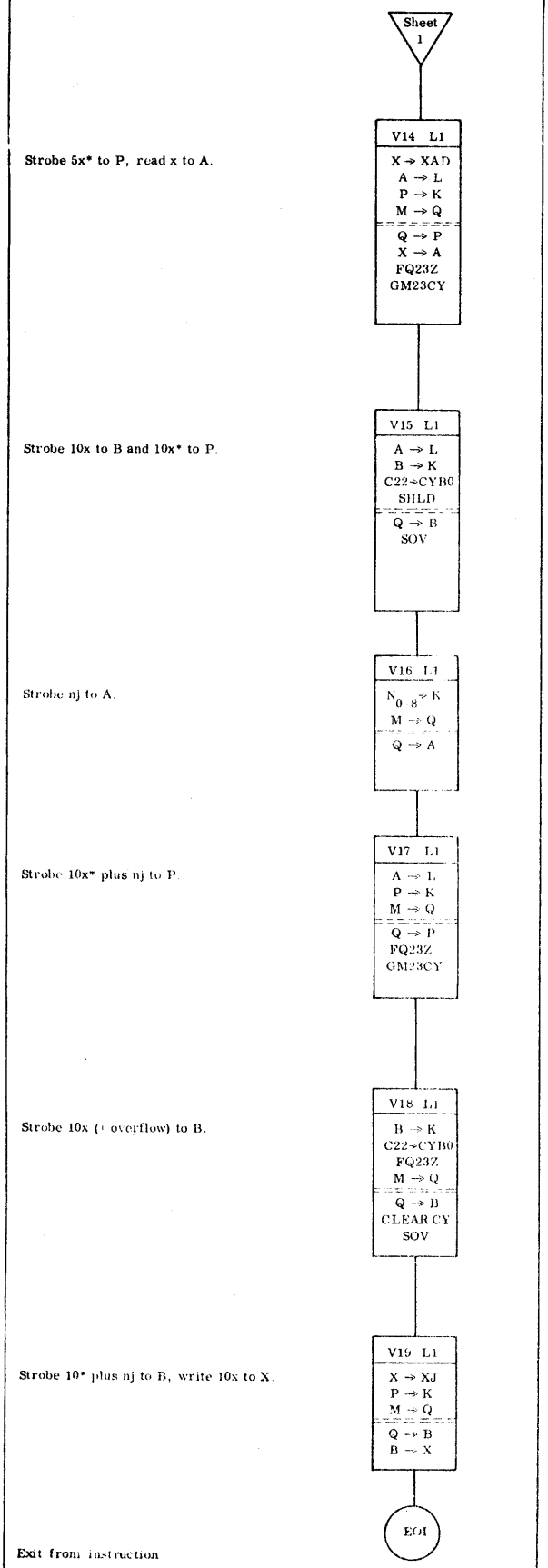
Read x* to B, test nj.

Read x to A, strobe x* to P.

Read x* to A, strobe 2x to B and 2x* to P.

Strobe 4x to B, and 4x* to P.

COMMENTS	VR.VI / SIGNAL	M.P.	CONDITIONS
Relevant signals active in previous beat: EVI, EVR, EESIN-B, I043.			
	(EN-SAD)	2E11:3/93	
	(ESIN-B)	6D4:21/248	
	(READ)	2E4:12/162	
	(ECAX-K)	3E10:10/67	
	(PLUS1)	3D24:8/109	
VR, VI: The character to be converted (nj) is read to B from store location N. The character is located in a specific character position of B. The current instruction address is incremented, and strobed to register C.	ELS3 → XJ	3F19: 6/91	HXOP
	EQAX-C	3E17:12-85	RESFL
	EHX-B	3F14:18/87	HXOP
	RESFL	2D7:6/32	DORLF. CPR. EXEC
	EV10	2A5:9/13	RESFL
	EEBJ-K	3D7:17/71	EV10
	V10		
	(PCHECK)	3D15:17/112	
	(EBJ-K)	3E21:17/75	
	ERX-XJ	3F20: 4/89	
	EHX*-B	3F18:18/80	
	EM-Q	3C14:23/167	
	PFAIL	6A6:21/214	PGEN = RB24
	DIE	3B33:25/44	PFAIL.PCHECK. INHPFL
V10: The character nj (in B) is gated onto bits 0-5 of K, where it is strobed into register A and N. Operand x* is read to B. Carry is cleared (CCY) or forced set (FCY) dependent upon the value of nj, i.e. the l.s. six bits of K.	EQAZ-A	3F29:23/81	
	EQ-N	3E1: 8/83	
	EQAQ-N	3E1: 2/83	
	EQRX-N	3E1: 7/83	
	EQYZ-N	3E1: 16/83	
	CCY	3F12:18/99	K <10
	FCY	3F15:17/106	K <10
	EOI	2A16:15/41	FCY
	EV11	2A6:16/14	K <10
	GBKALL	3F6:21/61	EV11
	V11		
	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3F7:24/62	
	(EBNP-K)	3E7:2/62	
	(EBQ-K)	3F7:23/62	
	(EBRX-K)	3F7:4/62	
	(EBYZ-K)	3F7:25/62	
If K ≥10, the character nj is non-numeric, and exit from the sequence is made via EOI. A numeric character (K < 10) results in entry to V11.	ERX-XJ	3F20:4/89	
	EM-Q	3C14:23/167	
	EQAZ-P	3F3:18/84	
	EHX-A	3D26:18/88	
	FNT2		
	EV12	3B11:10/15	
	GALALL	3D30:3/70	
V11: Operand x is read to A, and x* (B) strobed to P. Nt (N10-11) is forced to 2, thus any subsequent shifting operations will be of the arithmetic type.	V12		
	(EAAQ-L)	3F33:25/72	
	(EAR-L)	3F33:21/72	
	(EASX-L)	3F33:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	ERX-XJ	3F20:4/89	
	DSHL	3F27:20/105	
	EQ-B	3D13:15/79	
	EQAJ-B	3D13:21/79	
	EQKM-B	3D13:22/79	
	EQNQ-B	3D13:24/79	
	EQRZ-B	3D13:23/79	
	EHX*-A	3D28:8/108	
	EV13	2A18:5/16	
	GBKALL	3F6:21/61	
V12: Gate x (in A) to the mill, and shift left onto Q. Shift x* one place left in P. Strobe Q (2x) to B and read x* to A.	V13		
	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3F7:24/62	
	(EBNP-K)	3E7:2/62	
	(EBQ-K)	3F7:23/62	
	(EBRX-K)	3F7:4/62	
	(EBYZ-K)	3F7:25/62	
	DSHL	3F27:20/105	
	EQ-B	3D13:15/79	
	EQAJ-B	3D13:21/79	
	EQKM-B	3D13:22/79	
	EQNQ-B	3D13:24/79	
	EQRZ-B	3D13:23/79	
V13: The content of B (2x) is gated to the mill and shifted left onto Q. The content of P (2x*) is shifted left to give 4x*, and Q (4x*) is strobed to B.	EV14	2A7: 9/18	
	GALALL	3D30:3/70	
	EPKALL	/66	



V14: A (x*) and P (4x*) are added in the mill and the result (5x*) strobed to P. Any overflow from the mill operation (M23 = 1) is recorded in the carry bistable (GM23CY). The redundant sign bit (P23) is cleared by FQ23Z. Operand x is read to A.

V15: 5x is formed in the mill by addition of A (x) and B (4x). Any overflow from the previous operation (in C22) is added in. The mill output and P are shifted one place to the left giving 10x on Q and 10x* in P. 10x is strobed to B, and overflow is set if M23 ≠ M24 (SOV).

V16: The character nj (in N_{0-5}) is strobed to Register A.

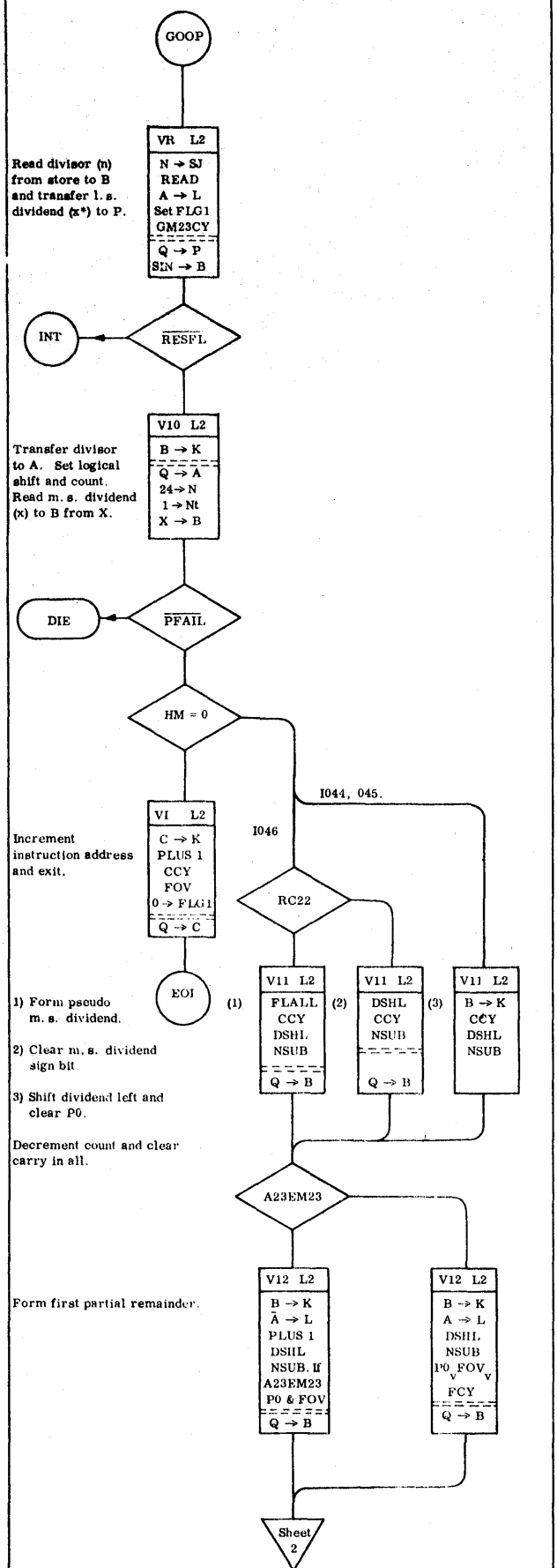
V17: 10x* (P) and (nj) are added in the mill, and the result strobed to P. FQ23Z clears P23 and any overflow (M23 ≠ M24) is recorded in C22 (GM23CY).

V18: Any overflow (C22) from the previous beat is added to 10x in the mill, and the result strobed to B. Carry is cleared (CCY) and overflow is set if M23 ≠ M24 (SOV).

V19: 10x (in B) is written to accumulator X, and 10x* + nj (in P) is transferred to Register B.

EOI: 10x* + nj is written to accumulator X + 1 in beat 0Q of the following Instruction Phase.

COMMENTS	V14 SIGNAL	MP	CONDITIONS
	(EAAQ-L)	3F33:25/72	
	(EAR-L)	3F33:21/72	
	(EASX-L)	3F33:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	(EPAJ-K)	3E9:3/66	
	(EPKQ-K)	3E9:5/66	
	(EPRX-K)	3F9:25/66	
	(EPYZ-K)	3F9:23/66	
	ERX-XJ	3F20:4/89	
	EM-Q	3C14:23/167	
	EQAZ-P	3F3:18/84	
	EHX-A	3D26:18/88	
	FQ23Z	3F22:15/101	
	GM23CY	3F11:10/105	
	EV15	2A8:9/19	
	GALALL	3D30:3/70	
	GBKALL	3F6:21/61	
	ECYB0	3F2:25/96	
	V15		
	(EAAQ-L)	3F33:25/72	
	(EAR-L)	3F33:21/72	
	(EASX-L)	3F33:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3F7:24/62	
	(EBNP-K)	3E7:2/62	
	(EBQ-K)	3F7:23/62	
	(EBRX-K)	3F7:4/62	
	(EBYZ-K)	3F7:25/62	
	(GC22)	2F10:25/112	
	DSHL	3F27:20/105	
	EQ-B	3D13:15/79	
	EQAJ-B	3D13:21/79	
	EQKM-B	3D13:22/79	
	EQNQ-B	3D13:24/79	
	EQRZ-B	3D13:23/79	
	SOV	2D7:18/32	
	EV16	2A9:9/20	
	V16		
	(ENAJ-K)	3D8:2/66	
	EM-Q	3C14:23/167	
	EQAZ-A	3F29:23/81	
	EV17	2A10:9/21	
	GALALL	3D30:3/70	
	EPKALL	/66	
	V17		
	(EAAQ-L)	3F33:25/72	
	(EAR-L)	3F33:21/72	
	(EASX-L)	3F33:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	(EPAJ-K)	3E9:3/66	
	(EPKQ-K)	3E9:5/66	
	(EPRX-K)	3F9:25/66	
	(EPYZ-K)	3F9:23/66	
	EM-Q	3C14:23/167	
	EQAZ-P	3F3:18/84	
	FQ23Z	3F22:25/101	
	GM23CY	3F11:10/105	
	EV18	3B1:22/23	
	GBKALL	3F6:21/61	
	ECYB0	3F2:25/96	
	V18		
	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3F7:24/62	
	(EBNP-K)	3E7:2/62	
	(EBQ-K)	3F7:23/62	
	(EBRX-K)	3F7:4/62	
	(EBYZ-K)	3F7:25/62	
	(GC22)	2F10:25/112	
	EM-Q	3C14:23/167	
	EQ-B	3D13:15/79	
	EQAJ-B	3D13:21/79	
	EQKM-B	3D13:22/79	
	EQNQ-B	3D13:24/79	
	EQRZ-B	3D13:23/79	
	CCY	3F12:18/99	
	SOV	2D7:18/32	
	FQ23Z	3E11:10/105	
	EV19	2A11:9/24	
	EPKALL	/66	
	V19		
	(EPAJ-K)	3E9:3/66	
	(EPKQ-K)	3E9:5/66	
	(EPRX-K)	3F9:25/66	
	(EPYZ-K)	3F9:23/66	
	EAX-XJ	3F20:4/89	
	EM-Q	3C14:23/167	
	EHAZ-X	3F25:8/90	
	EOI	2A16:15/41	



COMMENTS

Also active at entry will be EVR, GALALL, and I044-6. $I044_{v}I045_{v}I04C$ and I044:6 may be active as appropriate.

VR: x* is in A from the Instruction Phase and n is read from location N in store. Carry is set if the sign bit of the l. s. dividend (i. e. M23) is a 1. The FLG1 bistable is set.

V10: The divisor is transferred to A and Nt set to 1 to specify a logical shift. The count (Ns in N_{0-9}) is set to 24 and the m. s. dividend (x) read to B from accumulator X when it was stored in the Instruction Phase.

VI: Will be entered if the divisor is zero and overflow set. Where the divisor is non-zero, a test is performed to detect an 046 order (I046) with negative divisor.

V11: 1) If carry was set in VR (i. e. the dividend is negative) a pseudo m. s. dividend of all 1's must be set up; this puts -1 into B. A left shift then puts P23 (l. s. dividend sign bit) into B0 and sets P0 to zero. Carry is cleared.

2) If carry was not set (i. e. positive dividend) the m. s. dividend sign bit must be made zero (to equal that of the l. s. dividend). A double left shift puts the m. s. dividend B (with P23 in bit 0) and the l. s. dividend in P (with bit 0 zero). Carry is cleared.

3) Because of the double-length shift, bit 23 of the l. s. dividend appears in bit 0 of B (i. e. bit 0 of the m. s. dividend) and bit 0 of P is cleared. The m. s. bit of the dividend which was in B23 is last. Carry is cleared.

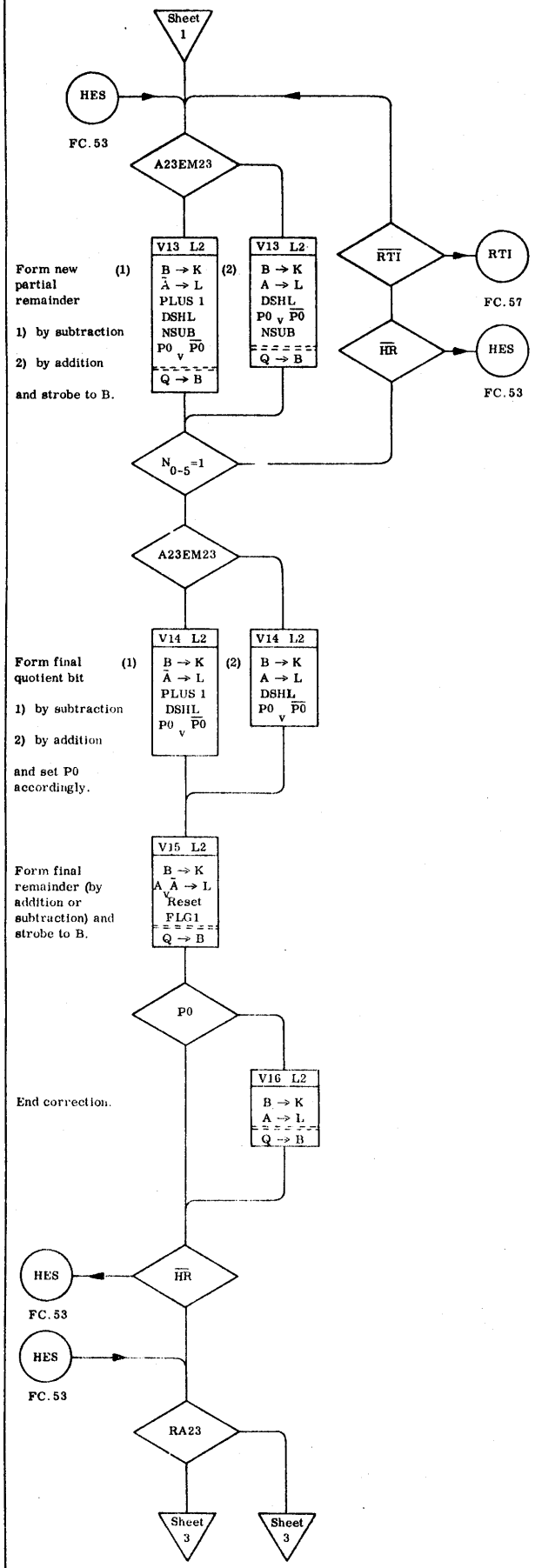
V12: The first partial remainder (PR) is formed either by addition or subtraction. The arithmetic operation to be performed is determined by comparison of the sign bits of the divisor (A23) and the dividend (M23). When these are equal M23EM23 is generated. The PR is shifted left and strobed to B.

1) The quotient bit (P0) is set if A23 ≠ M23 and overflow is forced. (0 & 044/6).

2) FCY is forced if A23 ≠ M23 & $\left[(045\ \&\ \overline{C23}_{v}\ M = 0\ \&\ P = 0\ \&\ 044/6)\right]$. ZRODVD is active if (P23 & M00217R & M22EM21), this will set carry if active or overflow if inactive. FOV is forced if A23 ≠ M23 & $\left[M \neq 0_{v} P \neq 0_{v} 045\right]$.

EV13	2A18:5/16	
$\overline{GBKALL}$	3F6:21/61	$\overline{P0}$ & ENDHES
GALALL	3D30:3/70	
ENALALL	3D31:7/72	$\overline{GALALL}$
EENARX-L	3E33:20/102	

VR / SIGNAL	M.P.	CONDITIONS
(EN-SAD)	2E11:3/93	
(ESIN-B)	6D4:21/248	$\overline{HXOP}$
(READ)	2E4:12/162	$\overline{HXOP}$
ELS3-XJ	3F19:6/91	HXOP
EHX-B	3F14:18/87	HXOP
RESFL	2D7:6/32	$\overline{DORLF}$ & $\overline{EXEC}$ & $\overline{CPR}$
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
(EQAZ-P)	3F3:18/84	
GM23CY	3F11:10/105	$\overline{RESFL}$
SETFLG1	3C30:10/152	$\overline{RESFL}$
EV33	3B20:20/33	$\overline{RESFL}$
$\overline{EV10}$	2A5:9/13	$\overline{RESFL}$
$\overline{GBKALL}$	3F6:21/61	EV10
V10		
(PCHECK)	3D15:17/112	
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3F7:4/62	
(EBYZ-K)	3F7:25/62	
EQAZ-A	3F29:23/81	
FN24	3D29:13/113	
FNT1	2D18:8/95	
ERX-XJ	3F20:4/89	
EHX-B	3F14:18/87	
EV1	3A16:12/8	$\overline{HM = 0}$
EV11	2A6:16/14	$\overline{HM = 0}$
FLALL	3F32:18/76	I046 & RC22 & $\overline{HM = 0}$
EENARX-L	3E33:20/102	
ENALALL	3D31:7/72	
V11		
(EAAQ-L)	3F33:25/72	I046 & RC22 & $\overline{HM = 0}$
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
(ENAAQ-L)	3C14:7/167	
(ENARX-L)	3D31:5/73	
(ENAYZ-L)	3D31:25/73	
CCY	3F12:18/99	
DSHL	3F27:20/105	
NSUB	3F18:21/80	
$\overline{EQAJ-B}$	3D13:21/79	I046
$\overline{EQKM-B}$	3D13:22/79	
$\overline{EQNQ-B}$	3D13:24/79	
$\overline{EQRZ-B}$	3D13:23/79	
EQ-B	3D13:15/79	
EV12	3B11:10/15	
$\overline{GBKALL}$	3F6:21/61	
GALALL	3D30:3/70	$\overline{A23EM23}$
V12AEM	3A6:7/17	A23EM23
ENALALL	3D31:7/72	
EENARX-L	3E33:20/102	V12AEM
VI		
(ECAX-K)	3E10:10/67	
(PLUS 1)	3D24:8/109	
EQAX-C	3F17:12/85	
CCY	3F12:18/99	
FOV	3F21:9/100	FLG1
ERX-XJ	3F20:4/89	$\overline{FLG1}$
EHX-B	3F14:18/87	$\overline{FLG1}$
RSTFLG1	3C31:10/150	
EOI	2A16:15/41	
V12		
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3F7:4/62	
(EBYZ-K)	3F7:25/62	
(EAAQ-L)	3F33:25/72	$\overline{A23FM23}$
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
(GALD)	3F33:24/72	
(ENAAQ-L)	3C14:7/167	A23EM23
(ENARX-L)	3D31:5/73	A23EM23
(ENAYZ-K)	3D31:25/73	A23EM23
DSHL	3F27:20/105	
(PLUS 1)	3D24:8/109	A23EM23 & $\overline{ENDHES}$
$\overline{EQAJ-B}$	3D13:21/79	
$\overline{EQKM-B}$	3D13:22/79	
$\overline{EQNQ-B}$	3D13:24/79	
$\overline{EQRZ-B}$	3D13:23/79	
EQ-B	3D13:15/79	
NSUB	3F18:21/80	
FCY	3F21:9/100	A23EM23 & GALD & $\overline{ZRODVD}$
FCY	3F15:17/106	A23EM23 & GALD & $\overline{ZRODVD}$
EEQ-P0	3F2:6/96	



COMMENTS

V13: The new partial remainder (PR) is formed by addition (or subtraction) and a left shift, and is strobed to B. A test is made on the count (prior to exit from the beat) and V13 is re-entered until such time as $N_8 = 1$. In each 'loop back', a hesitation break-point and a real-time interrupt break-point are provided. If either of these are utilised, the sequence is re-entered as shown once the hesitation has been dealt with. When the count has been reduced to 1, the signs of the previous PR and divisor are tested and V14 is entered.

V14: 1) PR sign ≡ divisor sign (A23EM23): the final quotient bit is formed by subtracting the divisor from the previous PR. P0 is set.

2) PR sign ≠ divisor sign (A23EM23): the final quotient bit is formed by addition. The final bit of the l. s. dividend is shifted out of P setting the quotient bit P0.

V15: The final remainder is formed (by addition if P0 = 0 or by subtraction if P0 = 1) and the FLG1 bistable is reset.

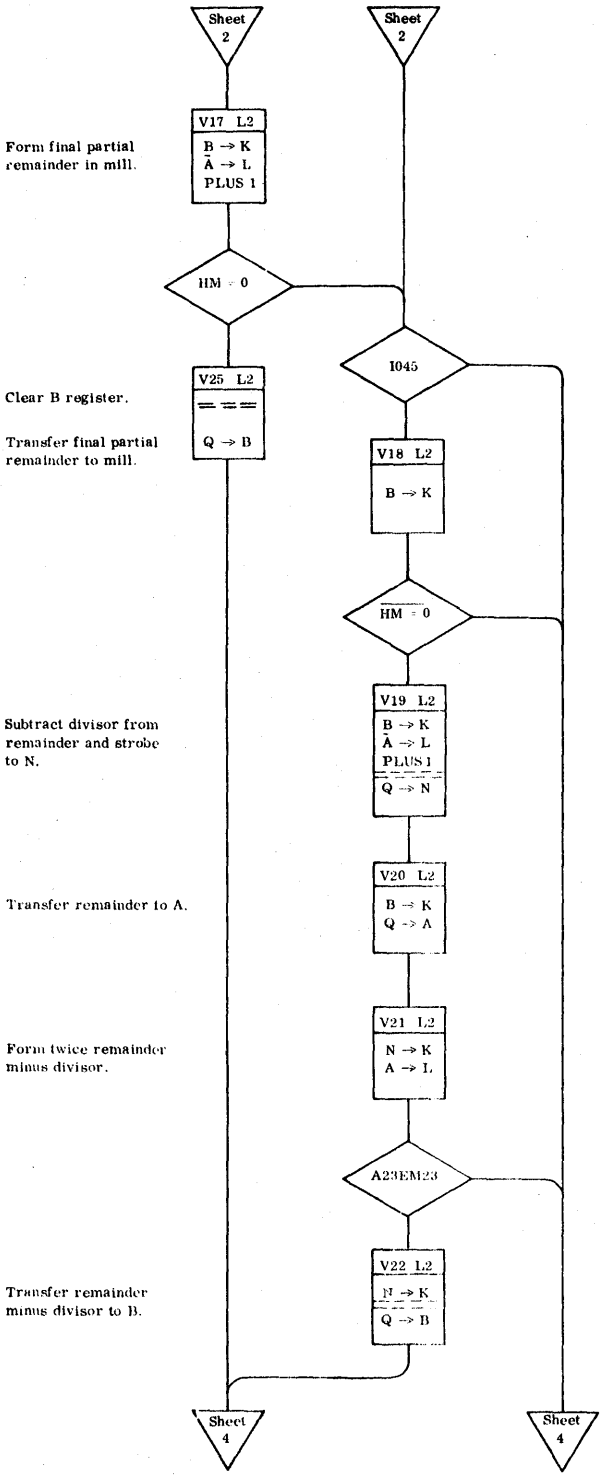
V16: Caters for end correction in the case where the final quotient bit is 0. A remainder is formed in B by the addition of the final partial remainder (in B from V15) and the divisor (in A). A hesitation break-point is provided prior to entry to the next beat. V16 will be bypassed if the quotient bit (RA23) is a 1.

V13 SIGNAL	M.P.	CONDITIONS
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3E7:4/62	
(EBYZ-K)	3F7:25/62	
(EAAQ-L)	3F33:25/72	$\overline{P0}$ & ENDHES
(EAAQ-L*)	3F33:23/72	$\overline{P0}$ & ENDHES
(EAR-L)	3F33:21/72	$\overline{P0}$ & ENDHES
(EASX-L)	3F33:7/72	$\overline{P0}$ & ENDHES
(EAY-L)	3F33:5/72	$\overline{P0}$ & ENDHES
(EAZ-L)	3F33:3/72	$\overline{P0}$ & ENDHES
(ENAAQ-L)	3C14:7/167	$\overline{GALALL}$
(ENARX-L)	3D31:5/73	$\overline{GALALL}$
(ENAYZ-L)	3D31:25/73	$\overline{GALALL}$
DSHL	3F27:20/105	
PLUS 1	3D24:8/109	
NSUB	3F18:21/80	
$\overline{EQAJ-B}$	3D13:21/79	
$\overline{EQKM-B}$	3D13:22/79	
$\overline{EQNQ-B}$	3D13:24/79	
$\overline{EQRZ-B}$	3D13:23/79	
EQ-B	3D13:15/79	
EEQ-P0	3F2:6/96	
EV14	2A7:9/18	$N_{0-5} = 1$
EV13	2A18:5/16	$N_{0-5} = 1$ & $\overline{HR}$ & $\overline{RTI}$
$\overline{GBKALL}$	3F6:21/61	
GALALL	3D30:3/70	A23EM23
ENALALL	3D31:7/73	A23EM23

V14		
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3F7:4/62	
(EBYZ-K)	3F7:25/62	
(EAAQ-L)	3F33:25/72	$\overline{A23EM23}$
(EAAQ-L*)	3F33:23/72	$\overline{A23EM23}$
(EAR-L)	3F33:21/72	$\overline{A23EM23}$
(EASX-L)	3F33:7/72	$\overline{A23EM23}$
(EAY-L)	3F33:5/72	$\overline{A23EM23}$
(EAZ-L)	3F33:3/72	$\overline{A23EM23}$
(ENAAQ-L)	3C14:7/167	A23EM23
(ENARX-L)	3D31:5/73	A23EM23
(ENAYZ-L)	3D31:25/73	A23EM23
(PLUS 1)	3D24:8/109	A23EM23 & ENDHES
DSHL	3F27:20/105	
EEQ-P0	3F2:6/96	
EV15	2A8:9/19	
GBKALL	3F6:21/61	
ENALALL	3D31:7/72	P0
EENARX-L	3E33:20/102	P0
GALALL	3D30:3/70	$\overline{P0}$

V15		
(EBAJ-K)		
(EBKM-K)		
(EBNP-K)		
(EBQ-K)		
(EBRX-K)		
(EBYZ-K)		
(EAAQ-L)	See V14	
(EAAQ-L*)	See V14	
(EAR-L)	See V14	P0
(EASX-L)	See V14	P0
(EAY-L)	See V14	P0
(EAZ-L)	See V14	P0
(ENAAQ-L)	See V14	$\overline{P0}$
(ENARX-L)	See V14	$\overline{P0}$
(ENAYZ-L)	See V14	$\overline{P0}$
$\overline{EQAJ-B}$	3D13:21/79	
$\overline{EQKM-B}$	3D13:22/79	
$\overline{EQNQ-B}$	3D13:24/79	
$\overline{EQRZ-B}$	3D13:23/79	
EQ-B	3D13:15/79	
RSTFLG1*	3D27:7/140	P0
EV16	2A9:9/20	P0
EV17	2A10:3/21	P0 & $\overline{HR}$ & RA23
EV18	3B12:22/23	P0 & $\overline{HR}$ & $\overline{RA23}$ & I045
EV24	3B16:10/28	P0 & $\overline{RA23}$ & $\overline{HR}$ & I044:6
$\overline{GBKALL}$	3F6:21/61	
GALALL	3D30:3/70	

V16		
(EBAJ-K)		
(EBKM-K)		
(EBNP-K)		
(EBQ-K)		
(EBRX-K)		
(EBYZ-K)	See V14	
(EAAQ-L)	See V14	
(EAAQ-L*)	See V14	
(EAR-L	See V14	
(EASX-L)	See V14	
(EAY-L)	See V14	
(EAZ-L)	See V14	
(PLUS 1)	3D24:8/109	P0
EV17	2A10:3/21	
$\overline{GBKALL}$	3F6:21/61	
EENARX-L	3E33:20/102	



COMMENTS

V17: The final partial remainder is formed by subtracting the divisor from the remainder. B still holds the remainder (from V16). A test is made on the FPR for zero (in the mill) to determine the next beat.

V25: The B register is cleared to give zero remainder.

V18: The FPR is fed to the mill and tested for zero.

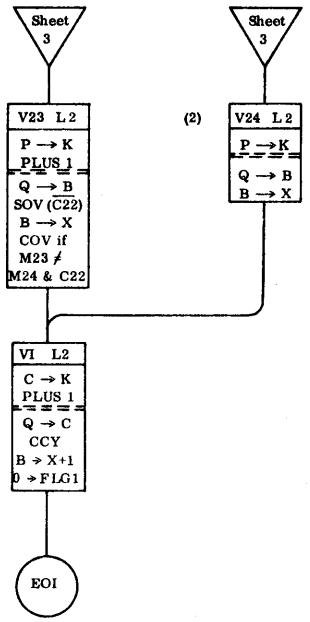
V19: The quantity 'remainder minus divisor' is formed from B + Ā and strobed to N.

V20: The remainder (in B from V16) is transferred to A.

V21: The quantity 'twice remainder plus divisor' is formed in the mill from N and A and mill bit 23 is compared with the sign bit of the remainder to determine the next beat.

V22: The quantity formed in V21 is transferred to B.

V17 / SIGNAL	MP	CONDITIONS
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3F7:2/26	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3F7:4/62	
(EBYZ-K)	3F7:25/62	
(ENAAQ-L)	3C14:7/167	
(ENARX-L)	3D31:5/73	
(ENAYZ-L)	3D31:25/73	
(PLUS 1)	3D24: /109	
EV25	3B17:21/29	HM = 0
EV18	3B12:22/23	I045 & HM = 0
EV24	3B16:10/28	HM = 0 &I1044.6
GBKALL	3F6:21/61	EV18
V25		
EQBIP	2D17:7/78	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
EQ-B	3D13:15/79	
EV23	2A13:8/9	
EPKALL	/66	
V18		
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3F7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3F7:4/62	
(EBYZ-K)	3F7:25/62	
EV19	2A11:9/24	HM = 0
GBKALL	3F6:21/61	EV19
ENALALL	3D31:7/7	
EENARX-L	3E33:20/102	
EV24	3B16:10/28	HM = 0
V19		
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3F7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3F7:4/62	
(EBYZ-K)	3F7:25/62	
(ENAAQ-L)	3C14:7/167	
(ENARX-L)	3D31:5/73	
ENAYZ-L)	3D31:25/73	
(PLUS 1)	3D24:3/109	
EQAQ-N	3E1:2/83	
EQRX-N	3E1:7/83	
EQYZ-N	3E1:16/83	
EQ-N	3E1:8/83	
EV20	3B13:18/25	
GBKALL	3F6:21/61	
V20		
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3F7:2/62	
(EBRX-K)	3F7:4/62	
(EBYZ-K)	3F7:25/62	
EQAZ-A	3F29:23/81	DVDIII
EV21	3B14:26/26	
ENKALL	3F8:7/61	
EENKQ-K	/61	
GALALL	3D30:3/70	
V21		
(ENAJ-K)	3D8:25/64	
(ENKQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/64	
(ENYZ-K)	3D8:10/64	
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
EV22	3B15:18/27	A23EM23
EV24	3B16:10/28	A23EM23
ENKALL	3E8:7/64	EV22
V22		
(ENAJ-K)	3D8:25/64	
(ENKQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/64	
(ENYZ-K)	3D8:10/64	
EQBIP	2D17:7/78	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
EQ-B	3D13:15/79	
EV23	2A13:8/9	
EPKALL	/66	



1) Write zero remainder to X and round quotient.

2) Write true remainder to X and transfer quotient to B.

Increment instruction address and transfer B to accumulator.

Exit.

COMMENTS

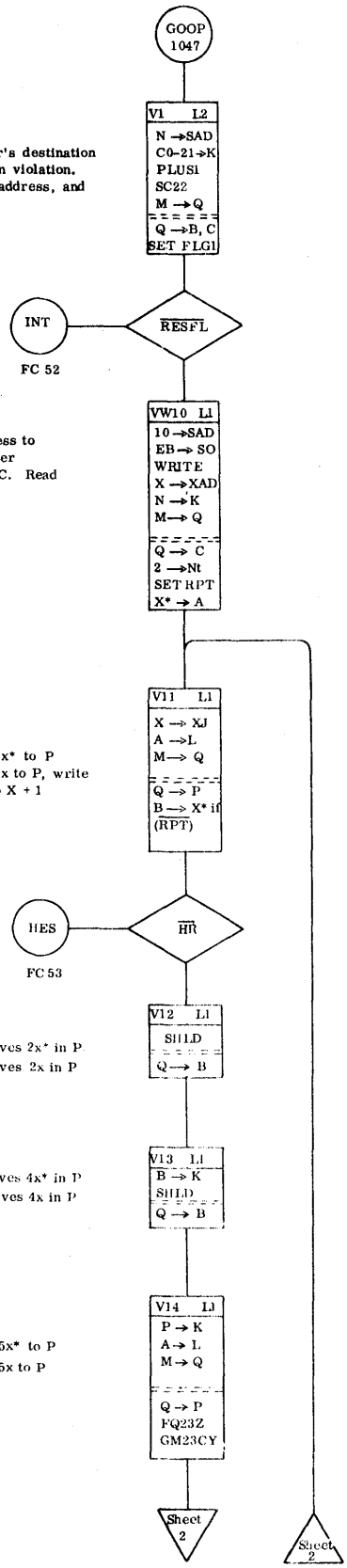
V23: The quotient in P is incremented by 1 and transferred to B. The remainder (in B) is transferred to accumulator X. Overflow is set if carry is clear (i.e. $\overline{RC22}$).

V24: The true remainder (FPR + divisor) held in B is written to accumulator X and the quotient held in P is transferred to register B.

VI: The instruction address is read from C, incremented and returned to C to give the address of the next instruction. Carry is cleared unconditionally.

Exit occurs at EOI, a break point being provided prior to entry to the Instruction Phase.

V23 SIGNAL	M.P.	CONDITIONS
(PLUS 1)	3D24:8/109	
$\overline{EQAJ-B}$	3D13:21/79	
$\overline{EQKM-B}$	3D13:22/79	
$\overline{EQNQ-B}$	3D13:24/79	
EQRZ-B	3D13:23/74	
SOV	2D7:18/32	RC22
EBAZ-X	3F25:8/90	
ERX-XJ	3F20:4/89	
EVI	2B2:18/4	
V24		
(EPAJ-K)	3E9:3/66	
(EPKQ-K)	3E9:5/66	
(EPRX-K)	3F9:25/66	
(EPYZ-K)	3F9:23/66	
$\overline{EQBIP}$	2D17:7/78	
$\overline{EQAJ-B}$	3D13:21/79	
$\overline{EQKM-B}$	3D13:22/79	
$\overline{EQNQ-B}$	3D13:24/79	
$\overline{EQRZ-B}$	3D13:23/79	
EQ-B	3D13:15/79	
EBAZ-X	3F25:8/90	
ERX-XJ	3F20:4/89	
EVI	2B2:18/4	
VI		
(ECAX-K)	3E10:10/67	
(PLUS 1)	3D24:8/109	
EQAX-C	3E17:12/85	
CCY	3F12:18/99	
EBAZ-X*	3F25:6/90	$\overline{FLG1}$
ERX-XJ	3F20:4/89	$\overline{FLG1}$
FOV	3F21:9/100	FLG1
RSTFLG1*	3D27:7/140	
EOI	2A16:15/41	



Test B.C.D. character's destination address for reservation violation. Increment instruction address, and set FLG1.

Write instruction address to location 10, and transfer destination address to C. Read x* to A, and set RPT.

(a) RPT: Strobe x* to P
(b) $\overline{RPT}$: Strobe x to P, write 10x* to X + 1

(a) RPT: Shift gives 2x* in P
(b) $\overline{RPT}$: Shift gives 2x in P

(a) RPT: Shift gives 4x* in P
(b) $\overline{RPT}$: Shift gives 4x in P

(a) RPT: Strobe 5x* to P
(b) $\overline{RPT}$: Strobe 5x to P

COMMENTS

Relevant signals active in previous beat: ESC22, EV1

V1:

The address into which the B.C.D. is to be written (N) is tested for reservation violation. The current instruction address (in C) is incremented by 1, and restored to C and B. The FLG1 bistable is set.

VW10:

The next instruction address is written to absolute location 10. The B.C.D. characters destination address is transferred to register C. Operand x*, the l.s. part of the binary fraction, is read to A. Nt (N10-11) is forced to 2 (FNT2) indicating that any subsequent shifting operation will be of the arithmetic type. The RPT (repeat) bistable is set to control the re-cycling of the conversion loop.

V11:

This beat is the first of the conversion loop, which comprises beats V11 to V16. At the end of the 1st cycle the RPT bistable is reset, thus RPT refers to the first and $\overline{RPT}$ to the second.

RPT: operand x* is transferred to register P
$\overline{RPT}$: operand x is transferred to register P, and 10x* (l.s. fraction is written to accumulator X + 1.

V12:

RPT: As a result of the arithmetic double left shift 2x* is formed in P, and x*22 (P22) is strobed to B0.

$\overline{RPT}$: The double left shift gives 2x in P and x22 in B0.

V13:

RPT: Both B (in the mill) and P are shifted left resulting in 4x* in A and x*21-22 in B0-1.

RPT: The double left shift gives 4x in P and x21-22 in B.

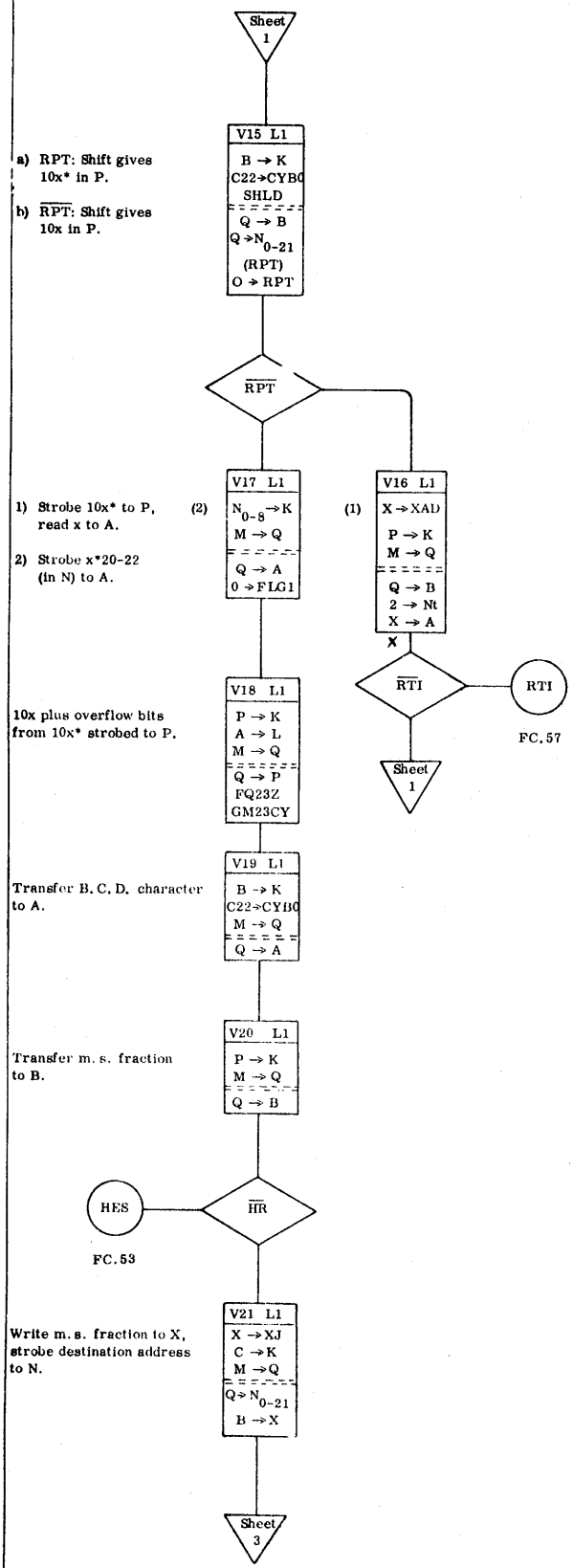
V14:

RPT: 5x* is formed in the mill, and strobed to register P.

$\overline{RPT}$: 5x is formed in the mill and strobed to P.

In either case the redundant sign bit in P23 is cleared (FQ23Z), and any overflow resulting from the mill operation (M23 ≠ 1) is recorded in the carry bistable (GM23CY).

V1 SIGNAL	M P	CONDITIONS
(EN-SAD)	2E11:3/93	
(ECAX-K)	3E10:10/67	
(PLUS1)	3D24:8/109	
(SC22)	3D3:22/11	
EM-Q	3C14:23/167	
EQBIP	2D17:7/78	
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
EQAX-C	3E17:4/85	$\overline{RESFL}$
EVW10	3A18:10/38	$\overline{RESFL}$
SETFLG1	3C30:10/150	
EEB-SO	2F7:17/106	
ENKALL	3F8:7/64	
VW10		
	3C32:24/152	
(FLG1)	3E21:9/75	
(EB-SO)	2E4 :6/162	
(WRITE)	3F10:9/112	
(FSAD10)		
(ENAJ-K)	3D8:25/64	
(ENKQ-K)	3D8:28/64	
(ENRX-K)	3D8:17/64	
(ENYZ-K)	3D8:10/64	
FRCE1	2F3:3/115	
FRCE3	2F3:6/115	
ERX-XJ	3F20:4/89	
EM-Q	3C14:23/167	
147NH		1047. $\overline{HES}$
EQCALL	3F17:2/85	147NH. VW10
EQAX-C	3E17:12/85	
EQY-C		
EQZ-C	3E17:16/85	
FNT2		
EHX*-A	3D28:8/10	
EV11	2A6:6/14	
GALALL	3D30:3/70	
V11		
(EAAQ-L)	3F33:25/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
(RPT)	3C28:23/14	
ERX-XJ	3F20:4/89	
EM-Q	3C14:23/167	
EQAZ-P	3F3:18/84	
EBAZ-X*	3F21:6/90	RPT
EV12	3B11:10/15	(1047. $\overline{HR}$) + (1047. FLG1. ENHNETH)
V12		
DSHL	3F27:20/10	
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
EV13	2A18:5/16	
GBKALL	3F6:21/61	
V13		
(EBAJ-K)	3F7 :26/62	
(EBKM-K)	3F7 :24/62	
(EBNP-K)	3F7 : 2/62	
(EBQ-K)	3F7 :23/62	
(EBRX-K)	3F7 : 4/62	
(EBYZ-K)	3F7 :25/62	
DSHL	3F27:20/105	
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
EV14	2A7:9/18	
EPKALL	2A7:9/66	
GALALL	3D30:3/70	
V14		
(EAAQ-L)	3F33:25/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
(EPAJ-K)	3F9:3/66	
(EPKQ-K)	3F9:5/66	
(EPRX-K)	3F9:25/66	
(EPYZ-K)	3F9:23/66	
EM-Q	3C14:23/167	
EQAZ-P	3F3:18/84	
FQ23Z		
GM23CY	3F11:10/105	
EV15	2A8:9/19	
GBKALL	3F6:21/61	
ECYB0	3F2:25/96	



V15: RPT: a further double left shift is performed, giving x*20-22 in B_{0-2} (plus any overflow in C22 from V14), and 10x* in P. The N Register is also loaded with x*20-22, but the character address in N_{22-23} is preserved (i.e. $Q \rightarrow N_{0-21}$ only). At the next clock RPT is cleared.

RPT: The effect of the double left shift is similar to the above except that B_{0-2} now held X_{20-22}, and P contains 10x (after the shift).

V16: 10x* in P, is transferred to register A, and operand x is again read to A. Nt is set to 2 (FNT2) and the conversion loop is recycled (from V11) for the second and final time.

V17: The overflow bits resulting from the multiplication of x* by 10, in N from V15, are strobed to A. FLG1 is reset at the next clock.

V18: The m.s. part of 10x (x*20-22) in A is added to 10x (in P), and the result (m.s. fraction) is gated to I. P23 is cleared (FQ23Z) and overflow (M23-1) is loaded into C22 (GM23CY).

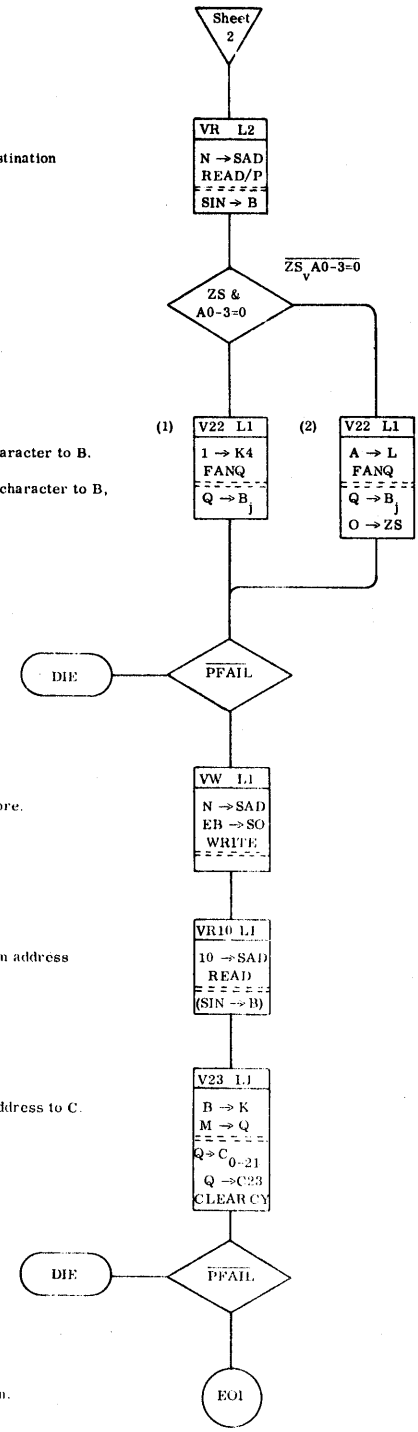
V19: The B.C.D. character (x20-22) in B_{0-2} is added to any overflow from the previous beat, the result being strobed to A.

V20: The m.s. fraction (10 + x* 20-22) is strobed to Register B.

V21:

The m.s. fraction in B is written to accumulator X. The B.C.D. character's destination (in C) is strobed to N0-21.

V15 / SIGNAL	M.P	CONDITIONS
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3E7:4/62	
(EBYZ-K)	3F7:25/62	
(GC22)	3F10:25/62	
DSHL	3F27:20/105	
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
EQ-N	3E1:8/83	RPT
EQAQ-N	3E1:7/83	
EQRX-N		
EV16	2A9:9/20	RPT
EPKALL	2A9:9/66	EV16
EV17	2A10:3/21	RPT
V16		
(EPAJ-K)	3E9:3/66	
(EPKQ-K)	3E9:5/66	
(EPRX-K)	3F9:25/66	
(EPYZ-K)	3F9:23/66	
EM-Q	3C14:23/16	
ERX-XJ	3F20:14/89	
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
FNT2		
EHX-A	3D26:18/88	
EV11	2A6:16/14	RTI
GALALL	3D30:3/70	EV11
V17		
(ENAJ-K)	3D8:25/64	
EM-Q	3C14:23/16	
EQAZ-A	3F29:23/81	
RSTFLG1	3C31:10/51	
EV18	3B12:22/23	
EPKALL		
GALALL	3D30:3/70	
V18		
(EPAJ-K)	3E9:3/66	
(EPKQ-K)	3E9:5/66	
(EPRX-K)	3F9:25/66	
(EPYZ-K)	3F9:23/66	
(EAAQ-L)	3F33:25/72	
(EAR-L)	3F33:21/72	
(EASZ-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
EM-Q	3C14:23/167	
EQAZ-P	3F3:18/84	
FQ23Z	3F22:25/101	
GM23CY	3F11:10/105	
EV19	2A11:9/24	
GBKALL	3F6:21/61	
ECYB0	3F2:25/96	
V19		
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3E7:4/62	
(EBYZ-K)	3F7:25/62	
(GC22)	3F10:25/11	
EM-Q	3C14:23/167	
EQAZ-A	3F29:23/81	
EV20	2B13:18/25	
EPKALL	3B13:18/66	
V20		
(EPAJ-K)	3E9:3/66	
(EPKQ-K)	3E9:5/66	
(EPRX-K)	3F9:23/66	
(EPYZ-K)	3F33:25/72	
EM-Q	3C14:23/16	
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13.23/79	
EV21	3B14:26/26	
V21		
(ECAX-K)	3E10:10/67	
ERX-XJ	3F20:4/89	
EM-Q	3C14:23/16	
EQ-N	3E1:8/83	
EQAQ-N	3F1:2/83	
EQRX-N	3E1:7/83	
EBAZ-X	3F25:8/90	
EV3	2A17:5/7	
EASIN-B	2E17:2/94	K<8. (HXOP). (SHXOP)



Read word from destination address.

1) Strobe space character to B.

2) Strobe B.C.D. character to B, clear ZS.

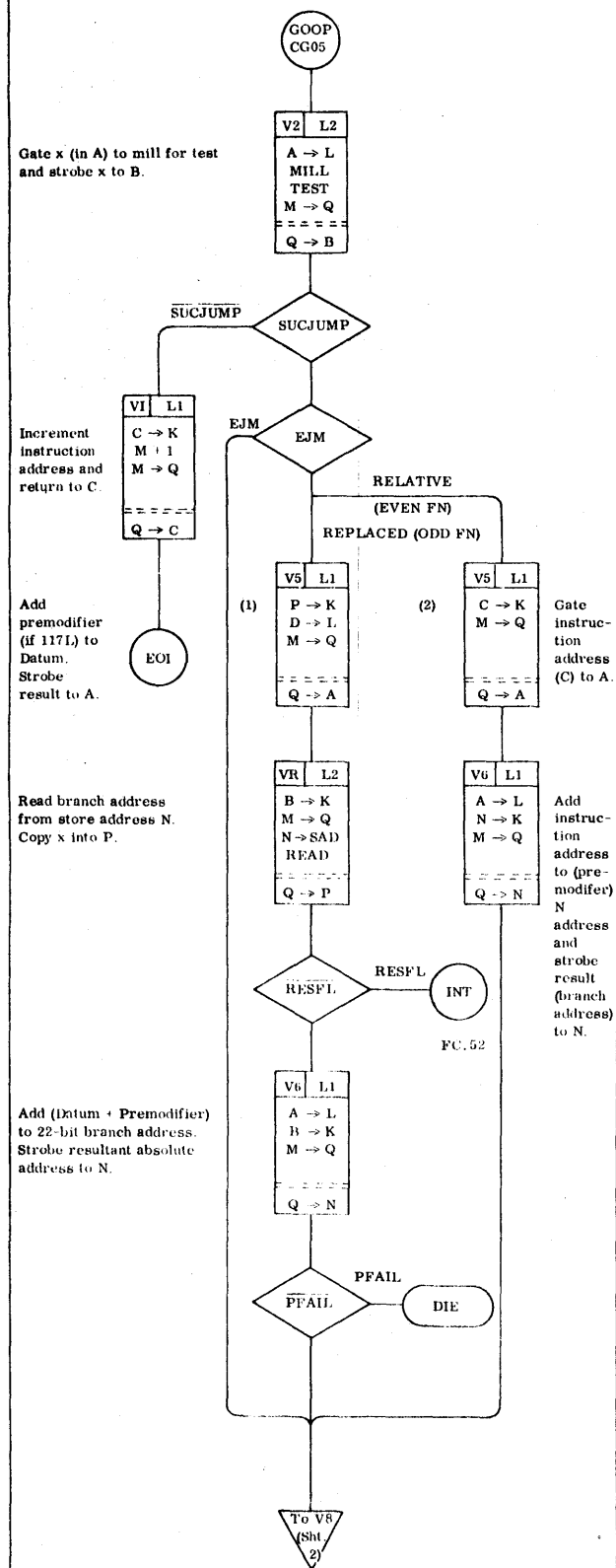
Write B.C.D. to store.

Read next instruction address from location 10.

Strobe instruction address to C.

Exit from instruction.

COMMENTS	VR / SIGNAL	M.P.	CONDITIONS
	(EN-SAD)	2E11:3/93	
	(READ)		
	(ESIN-B)	6D4:21/248	
	(PAUSE)		
VR: The word into which the B.C.D. character is to be inserted is read from store to B, on the read part of a Read Pause Write cycle.	ELS3-XJ	2F19:6/91	HXOP
	EHX-B	3F14:18/87	HXOP
	EV22	3B15:18/27	
	GALALL	3D30:3/70	$\overline{ZS_V A0\text{-}3\ 0}$
	V22		
	(PCHECK)	3D15:17/112	
	(FK4)	3D 5:26/69	ZS. A0-3 = 0
	(EAAQ-L)	3F33:23/72	
	(EAR-L)	3F33:21/72	
	(EASX-L)	3F33:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
V22:	PFAIL	6A6:21/21	RB24 = PGEN
	DIE	3B33:25/44	PCHECK. PFAIL $\overline{INHPFL}$
1) The ZS bistable has been previously set, and the B.C.D. character (A0-3) is zero. A space character (010000) if formed by forcing K4, and is strobed into a particular character position of B, as specified by the character address in N22-23.	EMFAN	3F28:17/107	
	EQ-BJ	3E18:19/80	
	EQ-B	3D13:15/79	
	GQ22ZS	3D23:25/103	A0-3 ≠ 0
2) The B.C.D. character (in the l.s. bits of A) is fanned onto Q to be strobed into a particular character position of B. The ZS bistable is cleared.	EVW	2B3:18/3	
	EEB-SO	2F7:17/106	$\overline{HXOP}$
	VW		
	EHX-B	3F14:18/87	HXOP
	(EN-SAD)	2E11: 3/93	
	(EB-SO)	3E21: 9/75	
VW: The word in B (containing the B.C.D. or space character) is written to the destination address N.	(WRITE)	2E 4: 6/162	
	ELS3-XJ	3F19:6/91	HXOP
	EVR10	3A14:22/39	$\overline{HXOP}$
	EESIN-B	2E17:2/94	
	VR10		
VR10: The next instruction address (dumped in VW10) is retrieved from store location 10.	(FSAD10)		
	(ESIN-B)		
	(READ)		
	FRCE1		
	FRCE3		
	EV23	2A13:8/9	
	GBKALL	3F6:21/61	
V23: The next instruction address is strobed to C_{0-21} with overflow (also dumped in VW10 and retrieved in VR10) restored to C23. The carry bistable is cleared.	V23		
	(PCHECK)		
	(EBAJ-K)		
	(EBKM-K)		
	(LBNP-K)		
	(EBQ-K)		
	(EBRX-K)		
	(EBYZ-K)		
	PFAIL		RB24 = PGEN
	DIE		PCHECK. PFAIL $\overline{INHPFL}$
	EM-Q		
	EQAX-C		
	EQZ-C		
	CCY		
	EOI		



Gate x (in A) to mill for test and strobe x to B.

Increment instruction address and return to C.

Add premodifier (if 117L) to Datum. Strobe result to A.

Read branch address from store address N. Copy x into P.

Add (Datum + Premodifier) to 22-bit branch address. Strobe resultant absolute address to N.

Gate instruction address (C) to A.

Add instruction address to (premodifer) N address and strobe result (branch address) to N.

COMMENTS

Relevant signals active in previous beat:
GOOP, EV2, GALALL.

V2: Mill Tests according to instructions being carried out, as follows:-

050/1 Instructions test to determine whether x = 0
052/3 " " " " " x ≠ 0
054/5 " " " " " x > 0 (+ve)
056/7 " " " " " x < 0 (-ve)

VI: is entered if the jump is unsuccessful ($\overline{\text{SUCJUMP}}$).

V5 and V6 are only entered if Extended Jump Mode (EJM) is specified, otherwise V8 is entered.
EJM allows jumps > 32K words.
$\overline{\text{EJM}}$ " " ≯ 32K " - even instructions only.

In EJM, jumps may be either RELATIVE or REPLACED.

V5:

1) If previous 117 instruction (117L), premodifier is in P. This is added to datum and result strobed to A. See conditions for EV5 (in V2 below).

V6. (RELATIVE)

The branch address is formed by adding the current instruction address (now in A) to the relative N address, which may have been premodified in the instruction phase. In 'negative jumps', sign extension is carried out in VDEC of the instruction phase.

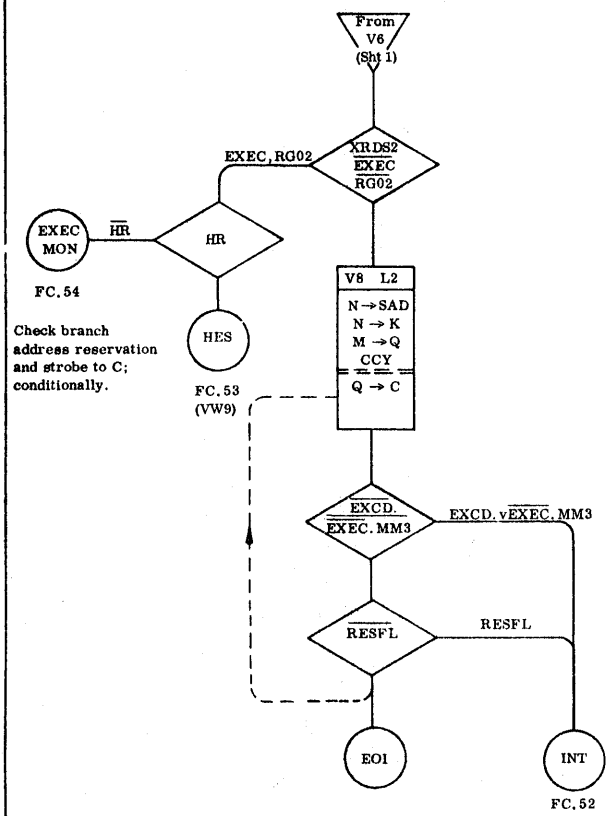
VR: (REPLACED)

x (in B) copied into P.
Store location of branch address was datumised and placed in N register in instruction phase. In VR the store is addressed from N and this part of the branch address is read out to B.

V6: (REPLACED)

Datum or (Datum + Premodifier) was placed in A in V5. Remainder of branch address is now in B. The contents of A and B are added to form the complete branch address which is strobed to N.

V2 / SIGNAL	M.P	CONDITIONS
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
SUCJUMP	3E23:20/111	I050:1. HM 0
SUCJUMP1	3F23:2/111	I052:3. HM 0
SUCJUMP2	3E23:24/111	I054:5. M23
EM-Q	3C14:23/167	I056:7. M23
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
XRDS	2A12:8/30	
EV1	3A16:12/8	$\overline{\text{SUCJUMP}}$ SUCJUMP1. XRDS.
EV5		EJ. ($\overline{\text{I076:7}}_{\text{v}}$ $\overline{\text{FPUBUSY}}_{\text{v}}$ $\overline{\text{FPU}}$) XRDS. EJ.
XRDS2	3A16:21/8	$\overline{\text{SUCJUMP1}}$. ($\overline{\text{I076:7}}$ v $\overline{\text{FPUBUSY}}$) XRDS2. ($\overline{\text{EXEC}}$ v $\overline{\text{RG02}}$)
EV8	3A21:12/11	F0
GDLA	3F31:18/74	
VI		
(ECAX-K)	3E10:10/67	
(PLUS 1)	3D24:8/109	
EM-Q	3C14:23/167	
EQAX-C	3E17:12/85	$\overline{\text{RESFL}}$
EOI	2A16:15/41	
V5		
(ECAX-K)	3E10:10/67	$\overline{\text{F0}}$
(EPAJ-K)	3E9:3/66	
(EPKQ-K)	3E9:5/66	117L.REPL
(EPRX-K)	3E9:25/66	
ED:L1		GDLA (V2)
ED:L2		
EM-Q	3C14:23/167	
EQAZ-A	3F29:23/81	
EV6	3A20:21/10	$\overline{\text{REPL}}$
EVR	2A17:5/7	F0
GALALL	3D30:3/70	EV6
EESIN B	2E17:2/94	EVR. $\overline{\text{HXOP}}$
VR		
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3F7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3E7:4/62	
(EBYZ-K)	3F7:25/62	
EM-Q	3C14:23/167	
EQAZ-P	3F29:23/81	
ELS3-XJ	3E19:6/91	HXOP
EHX-B	3F14:18/87	
(EN-SAD)	2L11:3/93	$\overline{\text{HXOP}}$
RESFL	2D7:16/32	DORLF. $\overline{\text{CPR}}$.
	5D1:20/284	$\overline{\text{EXEC}}$
RI	6D4:21/248	$\overline{\text{HXOP}}$
(ESIN-B)		
EV6	3A20:21/10	$\overline{\text{RESFL}}$
GALALL	3D30:3/70	
V6		
(PCHECK)	3D15:17/112	
DIE	3B33:25/44	PFAIL
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
(ENKQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/61	
EM-Q	3C14:23/167	
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3F7:2/62	
(EBRX-K)	3E7:4/62	
(EBQ-K)	3F7:23/62	
EQ-N	3E1:8/83	
EQYZ-N	3E1:16/83	
EQRX-N	3E1:7/83	
EQAQ-N	3E1:2/83	
EV8	3A21:12/11	$\overline{\text{XRDS2}}$. ($\overline{\text{EXEC}}$ v $\overline{\text{RG02}}$)
HESBKPT	2B15:25/47	XRDS2. EXEC RG02
EJ10	2A5:9/13	$\overline{\text{XRDS2}}$. EXEC RG02. $\overline{\text{HR}}$



If Executive Trace has been specified by a 125E instruction, a special Executive Monitoring routine is entered prior to V8. A hesitation break point occurs at the start of this routine.

V8: N → SAD is provided to initiate reservation check.

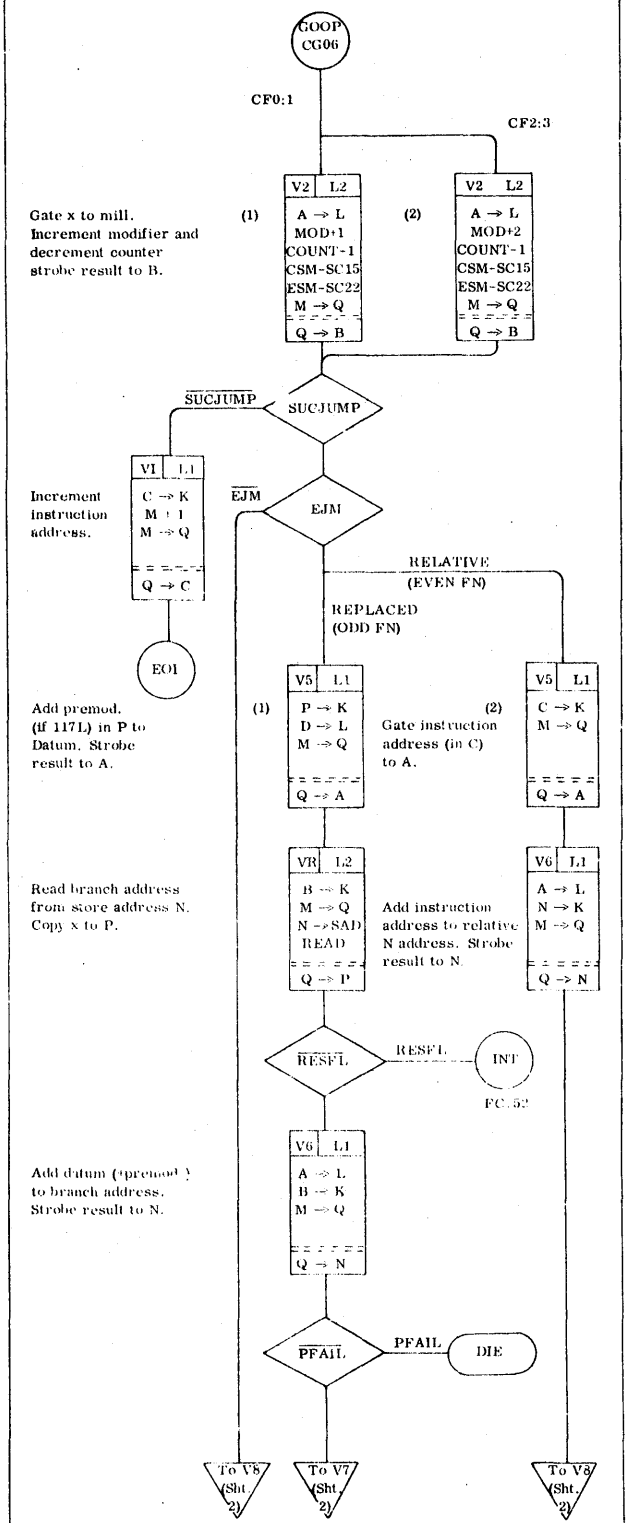
EOI if $\overline{EXCD}$. $\overline{EXEC}$. MM3

EXCD = Extracode and is only relevant in Group 7 instructions. If Monitor Mode 3 is specified in normal mode or if a RESFL occurs, the interrupt sequence is entered after V8.

The branch address is only strobed to C if the conditions for EOI are present, as indicated by the broken line. It should be remembered that the conditions are present in V8 and that (as mentioned in the format conventions) the strobe terminating any beat followed by 'decision diamonds' occurs after the decision diamonds.

Note that if a RESFL occurs, the interrupt sequence is entered at V33, but for mon. mode 3 the entry point is V36. See signal columns.

V8 SIGNAL	M.P.	CONDITIONS
(EN-SAD)	2E11: 3/93	
RESFL	2D 7: 6/32	DORLF. $\overline{CPR}$. $\overline{EXEC}$
(ENAJ-K)	3D 8:25/64	
(ENKQ-K)	3D 8:23/64	
(ENRX-K)	3D 8:17/64	
EM-Q	3C14:23/167	
EQAX-C	3E17:12/85	EOI
EOI	2A16:15/41	RESFL. $\overline{EXCD}$ $\overline{EXEC}$. MM3
EV33	3B20:20/33	RESFL
EV36	3A22:18/35	RG00. RG01 $\overline{EXEC}$. $\overline{PM}$ $\overline{RESFL}$
CCY	3F12:18/99	



COMMENTS

Relevant signals active in previous beat:
GOOP, CG06, GALALL, ESC15, EV2.

V2: Subtraction (from count) is performed by forcing K to 'all ones'. 'PLUS 1' adds 1 to modifier, FK1 adds 2 to modifier.

CSM:

1) Add 1 to the modifier (bits 0-14).
   Subtract 1 from the count (bits 15-23). SC15.
2) Add 2 to the modifier (bits 0-14).
   Subtract 1 from the count (bits 15-23). SC15.

ESM:

1) Add 1 to the modifier (bits 0-21). SC22.
2) Add 2 to the modifier (bits 0-21). SC22.

Note that in ESM the 22-bit address leaves no room for a 'count portion' and the operations therefore affect only the modifier. If count required in ESM, 066/7 instruction follows.

SUCJUMP is generated if test on count (≠0) successful.
I060-3 in CSM: SUCJUMP if M15-23 / 0.
I060-5 in CSM (i.e. ESM): there is no count portion and SUCJUMP is made unconditionally. If a count is required with these instructions, the next instruction is made an 066/7.

VI is entered if jump is unsuccessful.
V5 and V6 are only entered if Extended Jump Mode (EJM) is specified, otherwise V8 is entered.
EJM allows jumps > 32K words.
$\overline{\text{EJM}}$ allows jumps ≯ 32K words - even instructions only.

In EJM, jumps may be either RELATIVE or REPLACED.

V5:

1) If previous 117 instruction (117L), premodifier is in P. This is added to datum and result strobed to A. See conditions for EV5 (in V2 table below).

V6: (RELATIVE)

The branch address is formed by adding the current instruction address (now in A) to the relative N address, which may have been premodified in the Instruction Phase.

VR: (REPLACED)

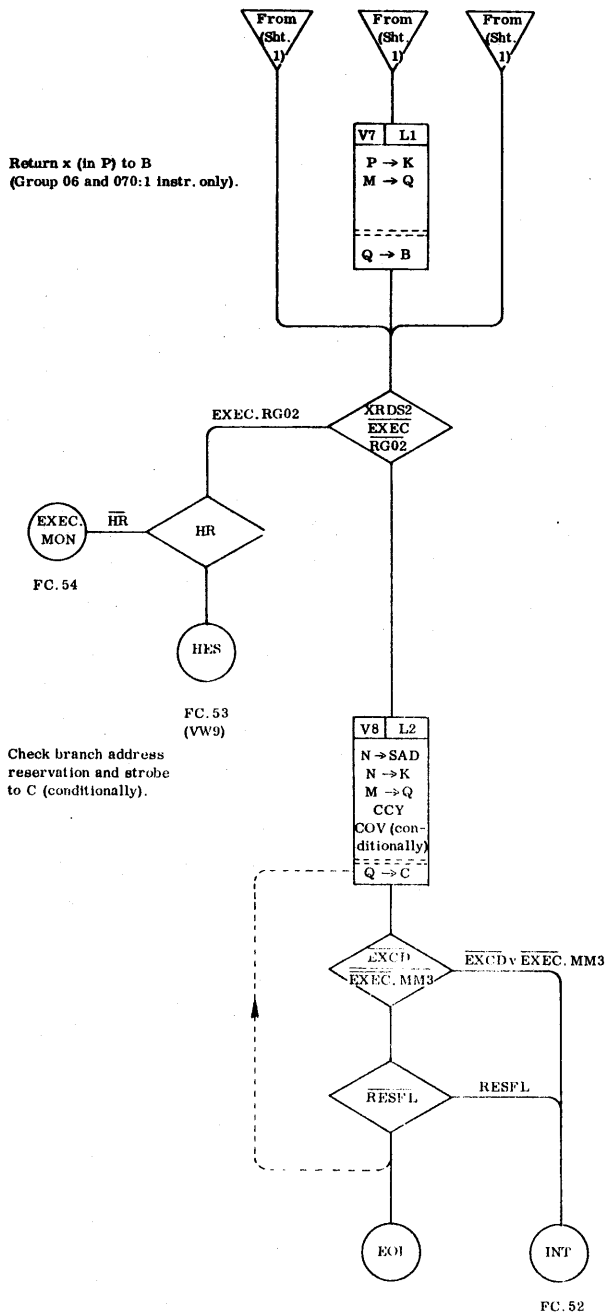
x (in B) copied into P.
Store location of branch address was datumised and placed in N Register in instruction phase. In VR, the store is addressed from N and this part of the branch address is read out to B.

V6: (REPLACED)

Datum or (Datum + Premodifier) was placed in A in V5. Remainder of branch address is now in B. The contents of A and B are added to form the complete branch address which is strobed to N.

EV8	3A21:12/11	XRDS2. ($\overline{\text{EXEC}}_V$ RG02)
HESBKPT	2B15:25/47	XRDS2. EXEC RG02)
EV10	2B 1:13/50	XRDS2. EXEC RG02. $\overline{\text{HR}}$
EENKQ-K	3E 1:16/83	EV8
EPKALL	3E 1:16/66	EV7. JUMP
EV7	3A21:21/11	REPL

V2 SIGNAL	M P	CONDITIONS
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3F33:23/72	
(EAR-L)	2F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
(FK15-21)	3D5:12/69	CSM. CF0:7. (EV2)
(FK22)	3E5:8/69	F2. CSM
(FK23)	3E5:16/69	F2. CSM
(FK1)	3D5:8/68	CF2:3
(PLUS 1)	3D24:8/109	I060:1
(SC15)	3D15:6/110	CSM
(SC22)	3D3:22/112	CSM
EM-Q	3C14:23/167	
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
XRDS	2D12:8/30	
		CSM. $\overline{\text{CF0-5}}_V$ CSM. I060-3
SUCJUMP/	3E23:20/111	$\overline{\text{M1523ZR}}_V$
1/2	3F23:2/111	CSM. I064:5
	3E23:24/111	$\overline{\text{HMDZR}}$ SUCJUMP1.
XRDS2	3A16:21/8	XRDS. $\overline{\text{EJ}}$. ($\overline{\text{I076:7}}_V$ $\overline{\text{FPUBUSY}}$)
EVI	3A16:23/8	$\overline{\text{SUCJUMP}}$ XRDS. SUCJUMP1.
EV5	2B13:3/9	EJ. $\overline{\text{I076:7}}_V$ $\overline{\text{FPU}}_V$ FPUBUSY)
EV8	3A21:12/11	XRDS2. ($\overline{\text{EXEC}}_V$ RG02)
GDLA	3F31:18/74	F0
VI		
ECAX-K	3E10:10/67	
(PLUS 1)	3D24:8/109	
EM-Q	3C14:23/167	
EQAX-C	2E17:12/85	$\overline{\text{RESFL}}$
CCY	3F12:18/99	
EOI	2A16:15/41	
V5		
(ECAX-K)	3E10:10/67	F0
(EPAJ-K)	3E9:3/66	117L. REPL
(EPKQ-K)	3E9:5/66	
(EPRX-K)	3E9:25/66	
ED-L:1	3E21:25/75	F0 (V2)
ED-L:2	3C21:22/75	
EM-Q	3C14:23/167	
EQAZ-A	3F29:23/81	
EV6	2A20:21/10	$\overline{\text{REPL}}$
EVR	2A17:5/7	F0
GALALL	3D30:3/70	EV6
EESIN-B	2E17:2/94	EVR. $\overline{\text{HXOP}}$
VR		
(EBAJ-K)	3F7:26/62	
(EBKM-K)	2F7:24/62	
(EBNP-K)	3F7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3E7:4/62	
(EBYZ-K)	3F7:25/62	
EM-Q	3C14:23/167	
EQAZ-P	3F29:23/81	
ELS3-X1	3F19:6/91	HXOP
EBX-B	3F14:18/87	
(EN SAD)	2E11:3/93	$\overline{\text{HXOP}}$
RESFL	2D7:6/32	DORLF. $\overline{\text{CPR}}$.
	5E1:20/281	$\overline{\text{EXEC}}$
RI		$\overline{\text{HXOP}}$
(ESIN B)	6D4:21/284	
EV6	3A20:21/10	$\overline{\text{RESFL}}$
GALALL	3D30:3/70	
V6		
(PCHECK)	3D15:17/112	
DIE	3B33:25/44	PFAIL
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
(ENKQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/64	
EM-Q	3C14:23/167	
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBRX-K)	3E7:4/62	
(EBQ-K)	3F7:23/62	
EBX-N	3E1:6/83	
EQYZ-N	3D6:26/83	
EQRX-N	3E1:7/83	
EQAQ-N	3E1:2/83	
XRDS2	3A16:21/8	$\overline{\text{EV7}}$



Return x (in P) to B (Group 06 and 070:1 instr. only).

Check branch address reservation and strobe to C (conditionally).

1) Write B to X in VQ of Inst. Phase following.

2) Set ZS if IRQ 22. GQ22ZS.

COMMENTS	V7 SIGNAL	M.P	CONDITIONS
V7: X is returned to B in order that it may be written directly to acc. X in VQ of the Inst. Phase following.	(EPAJ-K)	3E 9: 3/66	
	(EPKQ-K)	3E 9: 5/66	
	(EPRX-K)	3F 9: 5/66	
	(EPYZ-K)	3F 9:23/66	
	EM-Q	3C14:23/167	
	EQ-B	3D13:15/79	
	EQAJ-B	3D13:21/79	
	EQKM-B	3D13:22/79	
	EQNQ-B	3D13:24/79	
	EQRZ-B	3D13:23/79	
	XRDS2	3A16:21/8	
	EV8	3A21:12/11	XRDS2. (EXEC v RG02)
	hESBKPT	2B15:25/47	XRDS2. EXEC. RG02
	EV10	2B 1:13/50	XRDS2. EXEC. RG02. HR
	EGNKQ-K		EV8
If Executive Trace has been specified by a 125E instruction, a special Executive Monitoring routine is entered in the beat immediately before V8. A hes. break-point occurs at the start of this routine.	V8		
	(EN-SAD)	2E11: 3/93	
	RESFL	2D 7: 6/32	DORLF. CPR. EXEC
	(ENAJ-K)	3D 8:25/64	
	(ENKQ-K)	3D 8:23/64	
	(ENRX-K)	3D 8:17/64	
	EM-Q	3C14:23/167	
	EQAX-C	3E17:12/85	RESFL. EXCD
	EOI	2A16:15/41	EXEC. MM3
	EV33	3B20:20/33	RESFL
V8: N → SAD is provided to initiate reservation check.	EV36	3A22:18/35	RG00. RG01 EXEC. PM. RESFL
	COV	3E16:25/100	EOI. (1070:1 v 1074:5. XD2 v D4)
	CCY	3F12:18/99	EOI
	GQ22ZS	3D23:25/103	EOI. 1072:3
	FOV	3F21: 9/100	EOI. (1074:5 XD7 v 1072:3. RN23)

EOI if EXCD. EXEC. MM3

EXCD - Extracode and is only relevant in Group 07 instructions. If Monitor Mode 3 is specified by the G register or if a RESFL occurs the interrupt sequence is entered in V8.

The branch address is only strobed to C if the conditions for EOI are present as indicated by the broken line. It should be remembered that the conditions are present in V8 and that (as mentioned in the format conventions) the strobe terminating any beat followed by 'decision boxes' occurs after the decision boxes.

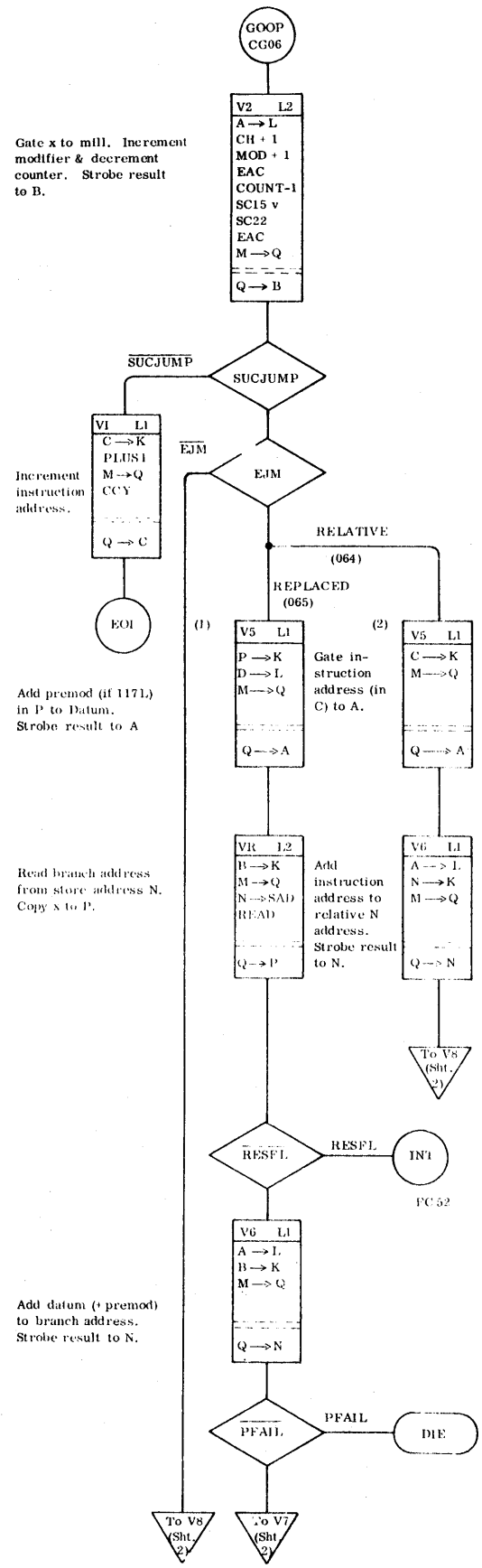
In 070/1 instr, OV is cleared since a record is maintained in the link.

Note that, if a RESFL occurs, the interrupt sequence is entered at V33, but for Monitor Mode 3 the entry point is V36. See signal columns.

In 072:3 instructions, the Zero Suppression bistables takes up the state of the ZS bit (Q22) at the ultimate strobe of V8.

In 070-1 instructions, OV is cleared since a record is maintained in the link.

In 074-5 instructions, OV is cleared if X = 2 or 4 and forced if X = 7. (See conditions on Sheet 1)



COMMENTS

RELEVANT SIGNALS ACTIVE IN PREVIOUS BEAT GOOP, CG06, GALALL, ESC15 (CSM), ESC22 (ESM).

064/5 instructions are used with character counter/modifier formats.

V2

CSM & ESM:

Character address (bits 22 & 23) incremented by 1. If CH = 3, overflow occurs and is fed back to M0. EAC (End Around Carry) makes CYB0.

CSM only:

Count decremented by 1 (FK 15-21).
Carry suppressed between bits 14 & 15.

ESM only:

There is no count component. If count required in ESM, this is dealt with by 066/7 instructions.
Carry suppressed between bits 21 & 22.

SUCJUMP is generated if test on count ($\neq 0$) is successful.
I064-5 in CSM: SUCJUMP if M15-23 $\neq 0$
I064-5 in $\overline{CSM}$ (i.e. ESM: there is no count portion and SUCJUMP is made unconditionally.

VI is entered if jump is unsuccessful.
V5 & V6 are only entered if Extended Jump Mode (EJM) is specified, otherwise V8 is entered.
EJM allows jumps > 32K words
EJM allows jumps $\not>$ 32K words - even instructions only.
In EJM, jumps may be RELATIVE or REPLACED.

V5

(1) If previous 117 instruction (117L), premodifier is in P. This is added to datum and result strobed to A. See conditions for EV5 (in V2 table below).

V6 (RELATIVE)

The branch address is formed by adding the current instruction address (now in A) to the relative N address, which may have been premodified in the instruction phase. In 'negative jumps', sign extension is carried out in VDEC of the instruction phase.

VR (REPLACED)

x (in B) copied into P.
Store location of branch address was datumised and placed in N register in instruction phase. In VR, the store is addressed from N and this part of the branch address is read out to B.

V6 (REPLACED)

Datum or (Datum + Premodifier) was placed in A in V5. Remainder of branch address is now in B. The contents of A & B are added to form the complete branch address which is strobed to N.

XRDS2	3A16:21/8	$\overline{EV7}$
EV8	3A21:12/11	XRDS2. ($\overline{EXEC}$. RG02)
HESBKPT	2B15:25/47	XRDS2. EXEC. RG02
EV10	2B 1:13/50	XRDS2. EXEC. RG02 $\overline{HR}$
EENKQ-K	3E 1:16/83	EV8
EPKALL	3E 1:16/66	EV7. JUMP
EV7	3A21:12/11	REPL

V2 SIGNAL	MP	CONDITIONS
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33: 7/72	
(EAY-L)	3F33: 5/72	
(EAZ-L)	3F33: 3/72	
(EAC)	3D13:16/79	
(CYB0)	6D26: 3/199	EAC. H122. H123. HK22
FK22	3E 5: 8/69	CF4:5
FK15-21	3D 5:12/69	$\overline{CF6:7}$. CSM
(SC15)	3D15: 6/112	CG06. $\overline{CSM}$
(SC22)	3D 3:22/112	CG06. $\overline{CSM}$ v I064-5. CSM
EM-Q	3C14:23/167	
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
XRDS	2A12: 8/30	
SUCJUMP/1/2	3E23:20/111	$\overline{CSM}$. CF0-5 v CSM. I064-5 $\overline{HMDZR}$
	3F23: 2/111	
	3E23:24/111	
XRDS2	3A16:21/8	SUCJUMP1.XRDS EJ. $\overline{(1076:7}$ v $\overline{FPUBUSY}$
EV1	3A16:12/8	XRDS. $\overline{SUCJUMP}$ XRDS. SUCJUMP1
EV5	2B13:3/9	EJ. (1076:7 v $\overline{FPU}$ v $\overline{FPUBUSY}$)
EV8	3A21:12/11	XRDS2. EXEC $\overline{RG02}$
GDLA	3F31:18/74	F0
V1		
ECAX-K	3E10:10/67	
(PLUS 1)	3D24: 8/109	
EM-Q	3C14:23/167	
EQAX-C	3E17:12/85	$\overline{RESFL}$
CCY	3F12:18/99	
EOI	2A16:15/41	
V5		
(ECAX-K)	3E10:10/67	F0
(EPAJ-K)	3E 9: 3/66	I117L. REPL
(EPKQ-K)	3E 9: 5/66	
(EPRX-K)	3E 9:25/66	
(ED-L-1)	3E21:25/75	F0 (V_2)
(ED 1-2)	3C21:22/75	
EM-Q	3C14:23/167	
EQAZ-A	3E29:25/81	
EV6	3A20:21/10	$\overline{REPL}$
EVR	2A17: 5/7	F0
GALALL	3D30: 3/70	EV6
EESIN-B	2E17: 2/94	
VR		
(EBAJ-K)	3F 7:26/62	
(EBKM-K)	3F 7:21/62	
(EBNP-K)	3E 7: 2/62	
(EBQ-K)	3F 7:23/62	
(EBRX-K)	3E 7: 4/62	
(EBYZ-K)	3F 7:25/62	
EM-Q	3C14:23/167	
EQAZ-P	3F29:23/81	
ELS3-X1	3F19: 6/91	HXOP
EHX-B	3F14:18/87	
(EN-SAD)	3E11: 3/93	$\overline{HXOP}$
RESFL	2D 7: 6/32	DORLF. $\overline{CPR}$. $\overline{EXEC}$
RI	5E 1:20/284	$\overline{HXOP}$
(ESIN-B)	6D 4:21/248	
EV6	3A20:21/10	$\overline{RESFL}$
GALALL	3D30: 3/70	
V6		
(PCHECK)	3D15:17, 11:2	
DIE	3H33:25/44	PFAIL
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33: 7/72	
(EAY-L)	3F33: 5/72	
(EAZ-L)	3F33: 3/72	
(ENKQ-K)	3D 8:23/64	
(ENRX-K)	3D 8:17/64	
EM-Q	3C14:23/167	
(EBAJ-K)	3F 7:26/62	
(EBKM-K)	3F 7:24/62	
(EBNP-K)	3E 7: 2/62	
(EBRX-K)	3E 7: 4/62	
(EBQ-K)	3F 7:23/62	
EQ-N	3E 1: 6/83	
EQYZ-N	6D 6:26/83	
EQRX-N	3E 1: 7/83	

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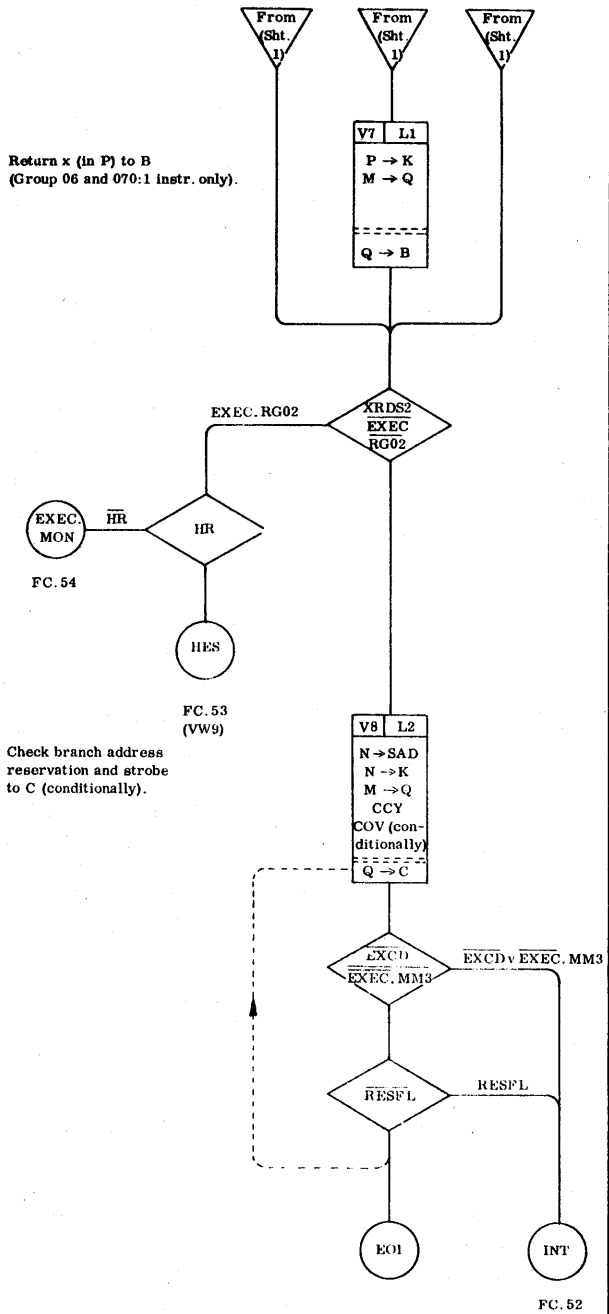
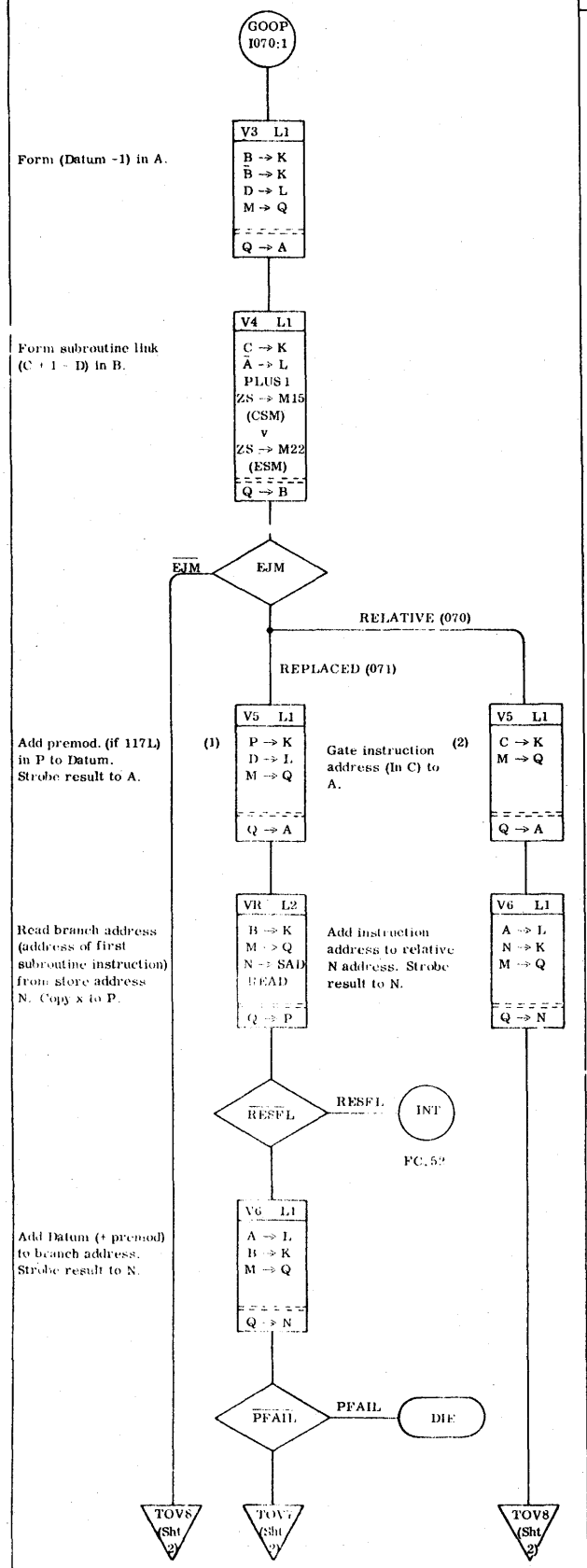


COMMENTS	V7 SIGNAL	M.P	CONDITIONS
V7: X is returned to B in order that it may be written directly to acc. X in VQ of the Inst. Phase following.	(EPAJ-K)	3E 9: 3/66	
	(EPKQ-K)	3E 9: 5/66	
	(EPRX-K)	3F 9: 5/66	
	(EPYZ-K)	3F 9:23/66	
	EM-Q	3C14:23/167	
	EQ-B	3D13:15/79	
	EQAJ-B	3D13:21/79	
	EQKM-B	3D13:22/79	
	EQNQ-B	3D13:24/79	
	EQRZ-B	3D13:23/79	
	XRDS2	3A16:21/8	
	EV8	3A21:12/11	XRDS2. (EXEC v RG02)
	hESBKPT	2B15:25/47	XRDS2. EXEC. RG02
	EV10	2B 1:13/50	XRDS2. EXEC. RG02. HR
	EGNKQ-K		EV8
If Executive Trace has been specified by a 125E instruction, a special Executive Monitoring routine is entered in the beat immediately before V8. A hes. break-point occurs at the start of this routine.	V8		
	(EN-SAD)	2E11: 3/93	
	RESFL	2D 7: 6/32	DORLF. CPR. EXEC
	(ENAJ-K)	3D 8:25/64	
	(ENKQ-K)	3D 8:23/64	
	(ENRX-K)	3D 8:17/64	
	EM-Q	3C14:23/167	
	EQAX-C	3E17:12/85	RESFL. EXCD
	EOI	2A16:15/41	EXEC. MM3
	EV33	3B20:20/33	RESFL
V8: N → SAD is provided to initiate reservation check.	EV36	3A22:18/35	RG00. RG01 EXEC. PM. RESFL
	COV	3E16:25/100	EOI. (1070:1 v (1074:5. XD_2 v D4)
	CCY	3F12:18/99	EOI
	GQ22ZS	3D23:25/103	EOI. 1072:3
	FOV	3F21: 9/100	EOI. (1074:5 XD7 v1072:3. RN23)
EOI if EXCD. EXEC. MM3			
EXCD = Extracode and is only relevant in Group 07 instructions. If Monitor Mode 3 is specified by the G register or if a RESFL occurs the interrupt sequence is entered in V8.			
The branch address is only strobed to C if the conditions for EOI are present as indicated by the broken line. It should be remembered that the conditions are present in V8 and that (as mentioned in the format conventions) the strobe terminating any beat followed by 'decision boxes' occurs after the decision boxes.			
In 070/1 instr, OV is cleared since a record is maintained in the link.			
Note that, if a RESFL occurs, the interrupt sequence is entered at V33, but for Monitor Mode 3 the entry point is V36. See signal columns.			
In 072:3 instructions, the Zero Suppression bistables takes up the state of the ZS bit (Q22) at the ultimate strobe of V8.			
In 070-1 instructions, OV is cleared since a record is maintained in the link.			
In 074-5 instructions, OV is cleared if X = 2 or 4 and forced if X = 7. (See conditions on Sheet 1)			



COMMENTS

Relevant signals active in previous beat:
GOOP, EV3, ¬BKALL, GDLA, PNBAZ, K.

070/1 instructions provide entry to a subroutine. The first operation required is to store the (relative) next instruction address so that this may be made available on exit from the subroutine. In V3, 1 is subtracted from Datum and in V4 the result of this operation is subtracted from the instruction address (in C). Thus: C - (D -1) = C + 1 - D.

V3: 1 is subtracted from Datum by gating B and B̄ to K and D to L. Thus K = 'all ones' and L = Datum.

Note that EV4 is not made. V3 makes V4 direct (0066).

V4: The result of the operation in V3 is subtracted from C. The state of the zero suppression bistable (ZS) is forced onto the Q highway, necessary gating in the data flow being initiated by GZSM15 (CSM) or GZSM22 (ESM).

All C except bit 22 ('carry') is gated to the mill. This includes the overflow bit (23). Thus, at the strobe setting:

	OV		CLEAR	ZS	Rel. next inst. addr.	
V5, B =	23	22	16	15	14	0 (CSM)
	OV	ZS	Relative next inst. addr.			
OR	23	22	21			0 (ESM)

In 070/1 instructions, SUCJUMP is forced unconditionally, since no test is required.

V5 and V6 are only entered if Extended Jump Mode (EJM) is specified. Otherwise, V8 is entered.
EJM allows jumps > 32K words.
$\overline{\text{EJM}}$ allows jumps ≯ 32K words - even instructions only.

In EJM, jumps may be either RELATIVE or REPLACED.

V5:

1) If previous 117 instruction (117L), premodifier is in P. This is added to datum and result strobed to A (see conditions for EV5 in V2 table below).

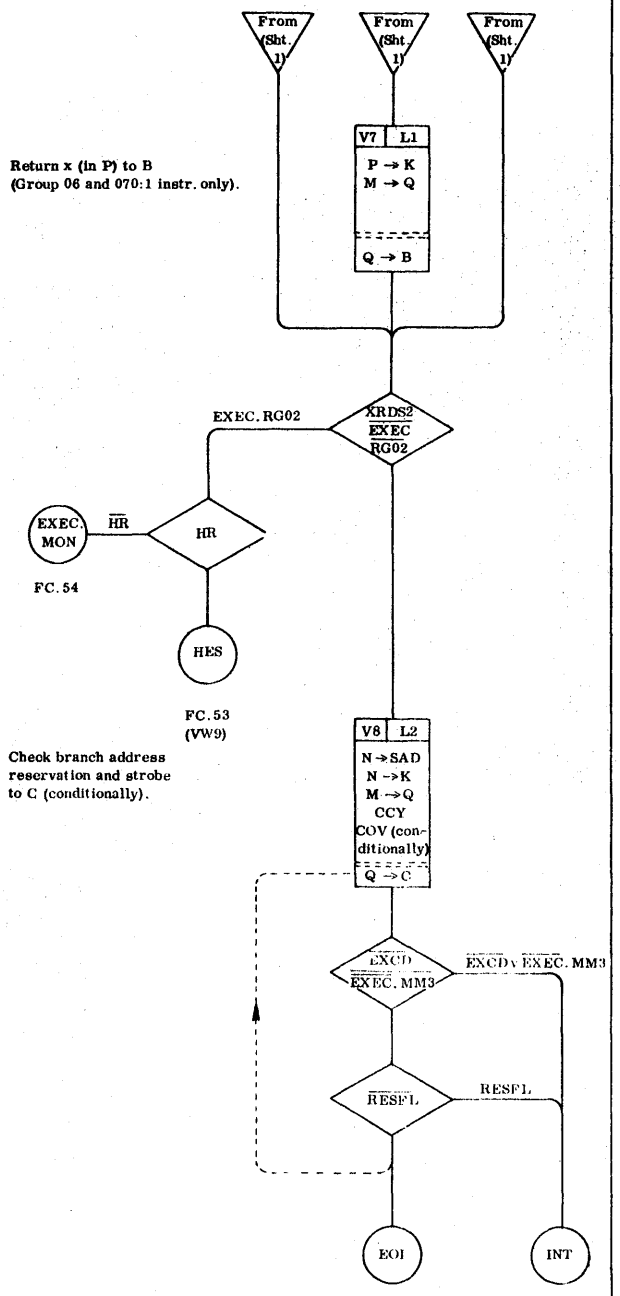
V6 & VR: The branch address is the address of the first subroutine instruction.

V6 (RELATIVE)
The branch address is formed by adding the current instruction address (now in A) to the relative N address, which may have been premodified in the Instruction Phase. In 'negative jumps', sign extension is carried out in VDEC of the Instruction Phase.

VR (REPLACED)
x (in B) copied into P.
Store location of branch address was datumised and placed in N register in Instruction Phase. In VR store is addressed from N and this part of the branch address is read out to B.

V6 (REPLACED)
Datum or (Datum + Premodifier) was placed in A in V5. Remainder of branch address is now in B. The contents of A and B are added to form the complete branch address which is strobed to N.

V3 SIGNAL	M.P	CONDITIONS
ED-L-1	3E21:23/75	CPR $\overline{\text{EXEC}}$
ED-L-2	3E21:22/75	
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3F7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3F7:4/62	
(EBYZ-K)	3F7:25/62	
ENBAZ-K	3D3:9/112	
EM-Q	3C14:23/117	
EQAZ-A	3F29:23/81	
EENARXL	3E33:20/102	
V4		
ECAX-K	3E10:10/67	
ECZ-K	3F10:19/67	
ENAAQ-L	3C14:7/167	
ENARX-L	3D31:5/73	
EZS-Q15	3F22:13/101	CSMNEJ
EZS-Q22	3E16:13/100	$\overline{\text{CSMNEJ}}$
(PLUS1)	3D24:8/109	
$\overline{\text{EQ-3}}$	3D13:15/79	
$\overline{\text{EQAJ-B}}$	3D13:21/79	
$\overline{\text{EQKM-B}}$	3D13:22/79	
$\overline{\text{EQNQ-B}}$	3D13:24/79	
$\overline{\text{EQRZ-B}}$	3D13:23/79	
SUCJUMP	3E23:20/111	
SUCJUMP_1	3F23:2/111	
SUCJUMP_2	3E23:24/111	
XRDS	2A12:8/30	
EJ	2D11:16/142	RG5
		SUCJUMP_1.
XRDS_2	3A16:21/8	XRDS. $\overline{\text{EJ}}$. 1076:7v $\overline{\text{FPUBUSY}}$
		XRDS. SUCJUMP_1.
EV_5	2B13:3/9	$\overline{\text{EJ}}$. 1076:7v $\overline{\text{FPU}}$ v FPUBUSY
GDLA	3F31:18/74	F0
EV8	3A21:12/11	XRDS_2. $\overline{\text{EXEC}}$ RG02.
V5		
(ECAX-K)	3E10:10/67	F0
(EPAJ-K)	3E9:3/66	
(EPKQ-K)	3E9:5/66	117L, PEPL
(EPRX-K)	3F9:25/66	
ED-L-1	3E21:23/75	F0 (V1)
ED-L-2	3E21:22/75	
EM-Q	3C14:23/117	
EQAZ-A	3F29:23/81	
EV6	3A20:21/10	RLPL
EVR	2A17:5/7	F0
GALALL	3D30:3/70	EV6
EESEN-B	3E17:2/94	
VR		
(EBAJ-K)	3F2:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3E7:4/62	
(EBYZ-K)	3F7:25/62	
EM-Q	3C14:23/117	
EQAZ-P	3F29:23/81	
ELS_3-N4	3E19:6/91	HXOP
EHX-B	3F14:18/75	
(EN-SAD)	2E11:3/99	HXOP
RESFL	2D7:16/59	DORLF, CPR, $\overline{\text{EXEC}}$
RI	5D1:20/284	HXOP
(ESEN-B)	6D1:21/248	
EV6	3A20:21/10	$\overline{\text{RESTL}}$
GALALL	3D30:3/70	
V6		
(PCHECK)	3D15:17/112	
DIE	3B33:25/11	PFAIL
(EAAQ-L)	3F33:25/72	
(EAAO-L*)	3F33:23/72	
(EAB-L)	3F33:21/72	
(EASN-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
(ENKQ-L)	3D3:23/61	
(ENRX-K)	3D3:17/61	
EM-Q	3C14:23/67	
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3F7:2/62	
(EBRX-K)	3E7:4/62	
(EBQ-K)	3F7:23/62	
EQ-N	3E1:8/83	
EQAZ-N	3E1:16/83	
EQR-N	3E1:7/83	
EQA-N	3E1:2/83	
XRDS2	3A16:21/6	EV7
EV5	3A21:12/11	XRDS_2. $\overline{\text{EXEC}}$.
BESBKPT	2B15:25/47	RG02
EV10	2A5:9/13	XRDS_2. $\overline{\text{EXEC}}$. RG02. HR.
ELNEQ-K	3L1:16/83	EV8
EPKALL	Sht. 66	EV7. JUMP
EV7	3A21:12/11	RLPL



1) Write B to X in VQ of Inst. Phase following.

2) Set ZS if BQ 22. GQ22ZS.

V7: X is returned to B in order that it may be written directly to acc. X in VQ of the Inst. Phase following.

If Executive Trace has been specified by a 125E instruction, a special Executive Monitoring routine is entered in the beat immediately before V8. A hes. break-point occurs at the start of this routine.

V8: N → SAD is provided to initiate reservation check.

EOI if $\overline{EXCD}$. $\overline{EXEC}$. MM3

EXCD - Extracode and is only relevant in Group 07 instructions. If Monitor Mode 3 is specified by the G register or if a RESFL occurs the interrupt sequence is entered in V8.

The branch address is only strobed to C if the conditions for EOI are present as indicated by the broken line. It should be remembered that the conditions are present in V8 and that (as mentioned in the format conventions) the strobe terminating any beat followed by 'decision boxes' occurs after the decision boxes.

In 070/1 instr, OV is cleared since a record is maintained in the link.

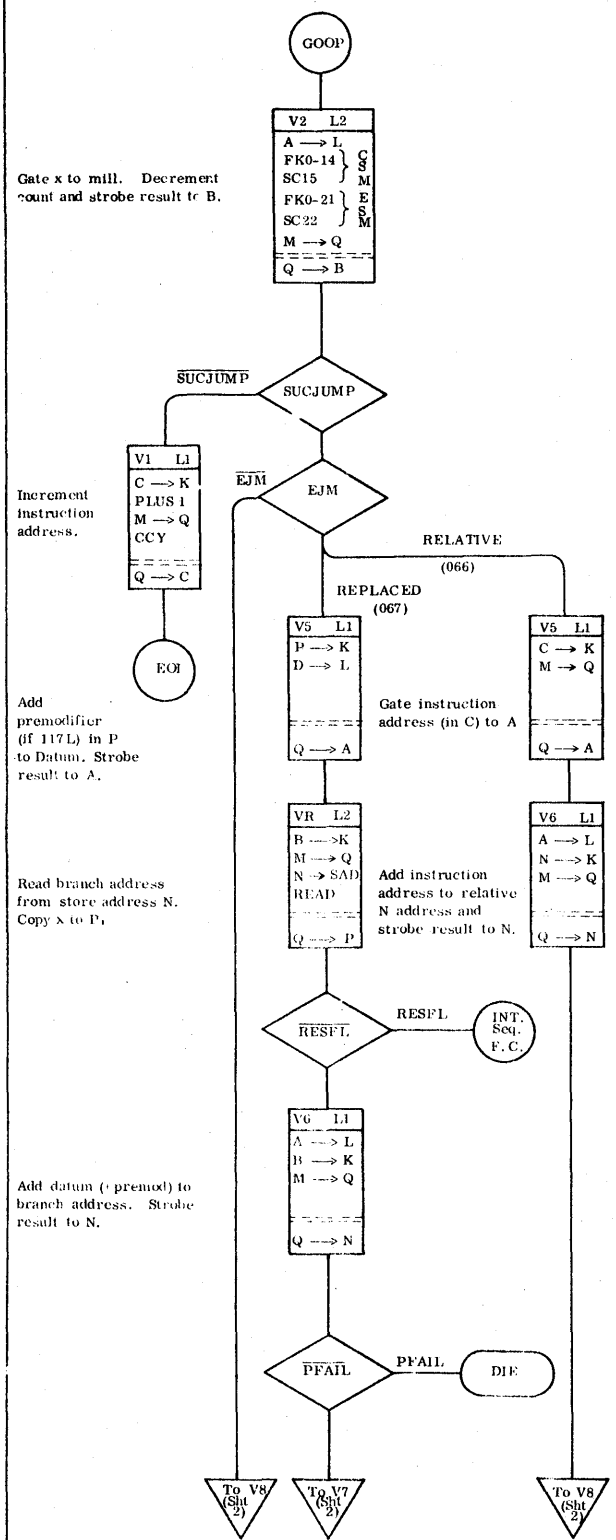
Note that, if a RESFL occurs, the interrupt sequence is entered at V33, but for Monitor Mode 3 the entry point is V36. See signal columns.

In 072:3 instructions, the Zero Suppression bistables takes up the state of the ZS bit (Q22) at the ultimate strobe of V8.

In 070-1 instructions, OV is cleared since a record is maintained in the link.

In 074-5 instructions, OV is cleared if X = 2 or 4 and forced if X = 7. (See conditions on Sheet 1)

COMMENTS	V7 / SIGNAL	M.P.	CONDITIONS
	(EPAJ-K)	3E 9: 3/66	
	(EPKQ-K)	3E 9: 5/66	
	(EPRX-K)	3F 9: 5/66	
	(EPYZ-K)	3F 9:23/66	
	EM-Q	3C14:23/167	
	EQ-B	3D13:15/79	
	EQAJ-B	3D13:21/79	
	EQKM-B	3D13:22/79	
	EQNQ-B	3D13:24/79	
	EQRZ-B	3D13:23/79	
	XRDS2	3A16:21/8	
	EV8	3A21:12/11	XRDS2. ($\overline{EXEC}$ v RG02)
	hESBKPT	2B15:25/47	XRDS2. EXEC. RG02
	EV10	2B 1:13/50	XRDS2. EXEC. RG02. $\overline{HR}$
	EGNKQ-K		EV8
	V8		
	(EN-SAD)	2E11: 3/93	
	RESFL	2D 7: 6/32	DORLF. $\overline{CPR}$. $\overline{EXEC}$
	(ENAJ-K)	3D 8:25/64	
	(ENKQ-K)	3D 8:23/64	
	(ENRX-K)	3D 8:17/64	
	EM-Q	3C14:23/167	
	EQAX-C	3E17:12/85	$\overline{RESFL}$. $\overline{EXCD}$
	EOI	2A16:15/41	$\overline{EXEC}$. $\overline{MM3}$
	EV33	3B20:20/33	RESFL
	EV36	3A22:18/35	RG00. RG01 $\overline{EXEC}$. $\overline{PM}$. $\overline{RESFL}$
	COV	3E16:25/100	EOI. (1070:1 v I074:5. XD_2v D4)
	CCY	3F12:16/99	EOI
	GQ22ZS	3D23:25/103	EOI. 1072:3
	FOV	3F21: 9/100	EOI. (1074:5 XD7 v1072:3. RN23)



COMMENTS

RELEVANT SIGNALS ACTIVE IN PREVIOUS BEAT:
EV2, V2066:7, GALALL, ESC15 (CSM), ESC22 (ESM)
GOOP

The 066/7 instructions branch to N if $x_c \neq 0$. These instructions contain either a 15 bit counter (CSM) or a 22 bit counter (ESM), but no modifier. Their main application is in ESM, when they provide the counter to be used in conjunction with the previous instruction's 22-bit modifier.

V2

The count is decremented by 1, the necessary bits of the K highway being forced to '1' at the same time as x (in A) is gated to the L highway.

CSM: Force K bits 0-14 and suppress carry between bits 14 & 15.
ESM: Force K bits 0-14 and suppress carry between bits 21 & 22.

SUCJUMP if count ≠ 0, bits 0-14 being tested in CSM and 0-21 in ESM. V1 is entered if jump is unsuccessful.

V5 and V6 are only entered if Extended Jump Mode (EJM) is specified, otherwise V8 is entered.
EJM allows jumps >32K words.
EJM " " ≯32K " - even instruction only.

V5

(1) If previous 117 instruction (1117L), premodifier is in P. This is added to datum and result strobed to A. See conditions for EV5 (in V2 table below).

V6 (RELATIVE)

The branch address is formed by adding the current instruction address (now in A) to the relative N address, which may have been premodified in the instruction phase. In 'negative jumps', sign extension is carried out in VDEC of the instruction phase.

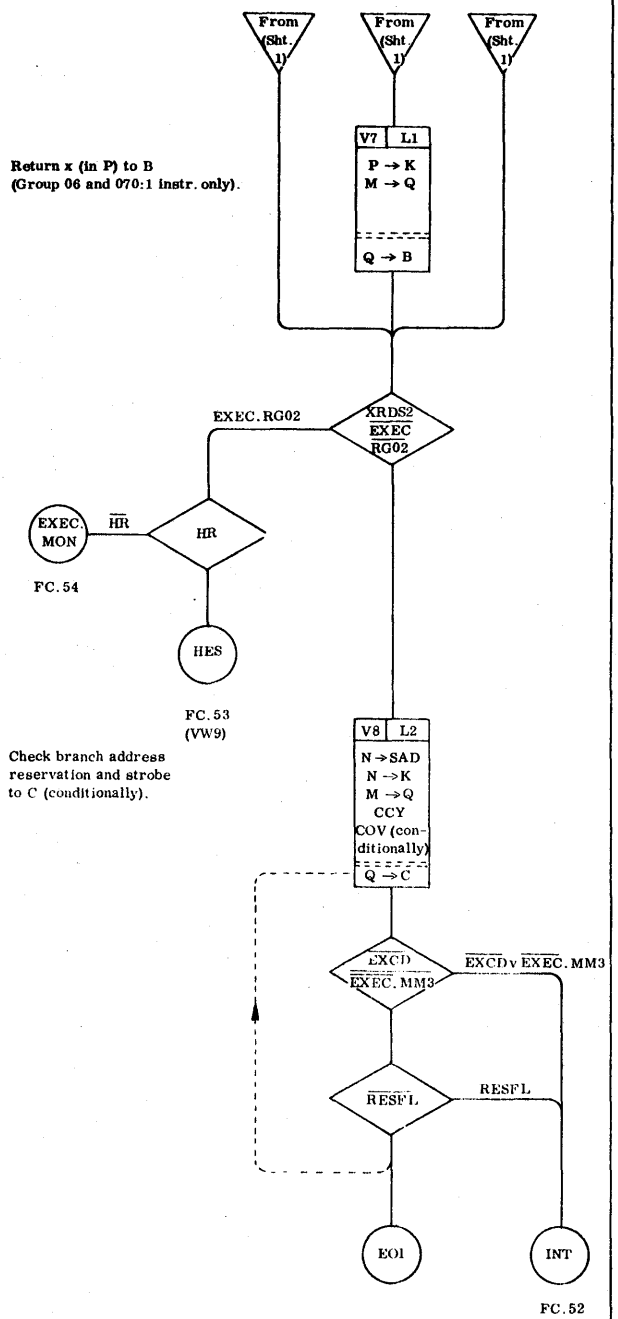
VR (REPLACED)

x (in B) copied into P.
Store location of branch address was datumised and placed in N register in instruction phase. In VR, the store is addressed from N and this part of the branch address is read out to B.

V6 (REPLACED)

Datum or (Datum + Premodifier) was placed in A in V5. Remainder of branch address is now in B. The contents of A & B are added to form the complete branch address which is strobed to N.

V2 / SIGNAL	M.P.	CONDITIONS
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/27	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
(FK0-714)	3D5:16/68	CG06. CF0:7
(FK1 to FK6)		
(FK15-21)	3D5:12/69	CSM. V2066:7.
(SC15)	3D15:6/112	CG06. CSM
(SC22)	3D3:22/112	CG06. CSM
EM-Q	3C14:23/167	
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
SUCJUMP1	3E23:20/111	M0014ZR$_V$
SUCJUMP2	3F23:2/111	M1521ZR. $\overline{CSM}$
SUCJUMP	3E23:24/111	
XRDS	2A12:8/30	
XRDS2	3A16:21/8	$\overline{SUCJUM1}$.$\overline{XRDS}$ EJ. (1076:7$_V$ $\overline{FPU}$ $_V\overline{FPUBUSY}$)
EV1	3A16:12/8	XRDS.SUCJUMP
V2		
EV5	2B13:3/9	XRDS. SUCJUMP1 EJ.(1076:7$_V$ FPU $_V$FPUBUSY)
EV8	3A21:12/11	XRDS2. $\overline{EXEC}$. $\overline{RG02}$
GDLA	3F31:18/71	F0
V1		
ECAX-K	3E10:10/67	
(PLUS1)	3D21:8/107	
EM-Q	3C14:23/167	
EQAX-C	3E17:12/85	RESFL
CCY	3F12:18/99	
EOI	2A16:15/11	
V5		
(ECAX-K)	3E10:10/67	$\overline{F0}$
(EPAJ-K)	3E9:3/66	
(EPKQ-K)	3E9:5/66	1117L. REPL
(EPRX-K)	3E9:25/66	
(ED-L:1)	3E21:25/75	F0 (V2)
(ED-L:2)	3E21:22/75	
EM-Q	3C14:23/167	
EQAZ-A	3E29:23/81	
EV6	3A20:21/10	$\overline{REPL}$
EVR	2A17:5/9	F0
GALALL	3D20:3/20	EV6
EESIN-B	2E17:2/94	
VR		
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3E7:4/62	
(EBYZ-K)	3F7:25/62	
EM-Q	3C14:23/62	
EQAZ-P	3D29:23/167	
EISS-NJ	3F19:6/91	HXOP
EHN-B	2E14:18/87	
(EN-SAD)	2E11:3/93	HXOP
RESFL	2D7:6/82	$\overline{EXEC}$.$\overline{HR}$.$\overline{EXEC}$
RI	5E1:20/284	HXOP
(ESIN-B)	6D1:21/248	
EV6	3A20:21/10	$\overline{RESFL}$
GALALL	3D20:3/20	
V6		
(PCHECK)	3D15:17/112	
DIE	3B33:25/44	PFAIL
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
(ENKQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/64	
EM-Q	3C14:23/167	
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBRX-K)	3E7:4/62	
(EBQ-K)	3F7:23/62	
EQ-N	3E1:28/83	
EBYZ-K	3F7:25/62	
EQRX-N	3E1:7/83	
XRDS2	3A16:21/8	$\overline{EV7}$
EV8	3A21:12/11	$\overline{XRDS2}$. ($\overline{EXEC}$ $_V$ $\overline{RG02}$)
RESPT	2B15:25/47	XRDS2. EXEC. RG02
EV10	2B1:13/50	XRDS1. EXEC. RG02. $\overline{HR}$
EENKQ-K	Sht. 64	EV8
EPKALL	Sht. 66	EV7. JUMP
EV7	3A21:12/11	REPL



1) Write B to X in VQ of Inst. Phase following.

2) Set ZS if HQ 22. GQ22ZS.

V7: X is returned to B in order that it may be written directly to acc. X in VQ of the Inst. Phase following.

If Executive Trace has been specified by a 125E instruction, a special Executive Monitoring routine is entered in the beat immediately before V8. A hes. break-point occurs at the start of this routine.

V8: N → SAD is provided to initiate reservation check.

EOI if $\overline{EXCD}$. $\overline{EXEC}$. MM3

EXCD = Extracode and is only relevant in Group 07 instructions. If Monitor Mode 3 is specified by the G register or if a RESFL occurs the interrupt sequence is entered in V8.

The branch address is only strobed to C if the conditions for EOI are present as indicated by the broken line. It should be remembered that the conditions are present in V8 and that (as mentioned in the format conventions) the strobe terminating any beat followed by 'decision boxes' occurs after the decision boxes.

In 070/1 instr, OV is cleared since a record is maintained in the link.

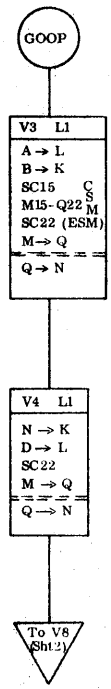
Note that, if a RESFL occurs, the interrupt sequence is entered at V33, but for Monitor Mode 3 the entry point is V36. See signal columns.

In 072:3 instructions, the Zero Suppression bistables takes up the state of the ZS bit (Q22) at the ultimate strobe of V8.

In 070-1 instructions, OV is cleared since a record is maintained in the link.

In 074-5 instructions, OV is cleared if X = 2 or 4 and forced if X = 7. (See conditions on Sheet 1)

COMMENTS	V7 SIGNAL	MP	CONDITIONS
	(EPAJ-K)	3E 9: 3/66	
	(EPKQ-K)	3E 9: 5/66	
	(EPRX-K)	3F 9: 5/66	
	(EPYZ-K)	3F 9:23/66	
	EM-Q	3C14:23/A67	
	EQ-B	3D13:15/79	
	EQAJ-B	3D13:21/79	
	EQKM-B	3D13:22/79	
	EQNQ-B	3D13:24/79	
	EQRZ-B	3D13:23/79	
	XRDS2	3A16:21/8	
	EV8	3A21:12/11	XRDS2. (EXEC v RG02)
	hESBKPT	2B15:25/47	XRDS2. EXEC. RG02
	EV10	2B 1:13/50	XRDS2. EXEC. RG02. HR
	EGNKQ-K		EV8
	V8		
	(EN-SAD)	2E11: 3/93	
	RESFL	2D 7: 6/32	DOR1.F. CPR. EXEC
	(ENAJ-K)	3D 8:25/64	
	(ENKQ-K)	3D 8:23/64	
	(ENRX-K)	3D 8:17/64	
	EM-Q	3C14:23/A67	
	EQAX-C	3E17:12/85	RESFL. EXCD
	EOI	2A16:15/41	EXEC. MM3
	EV33	3B20:20/33	RESFL
	EV36	3A22:18/35	RG00. RG01 EXEC. PM. RESFL
	COV	3E16:25/100	EOI. (1070:1 v 1074:5. XD2 v D4)
	CCY	3F12:18/99	EOI
	GQ22ZS	3D23:25/103	EOI. 1072:3
	FOV	3F21: 9/100	EOI. (1074:5 XD7 v 1072:3. RN23)



Transfer link (in A) to N.

Datumise relative next instruction address and return to N.

COMMENTS

Relevant signals active in previous beat:
GOOP, I072:3, EXITV3, GALALL, (EXITV3. $CSM_V EJM$), ESC15 ($\overline{EJ}$. CSM), ESC22 ($\overline{CSM}_V EJM$), GBKALL.

The 072:3 instructions provide exit from subroutine.

V3: The link (relative address of next instruction in the object program) is added to the relative N address of the 072:3 instruction and the result is strobed to N.

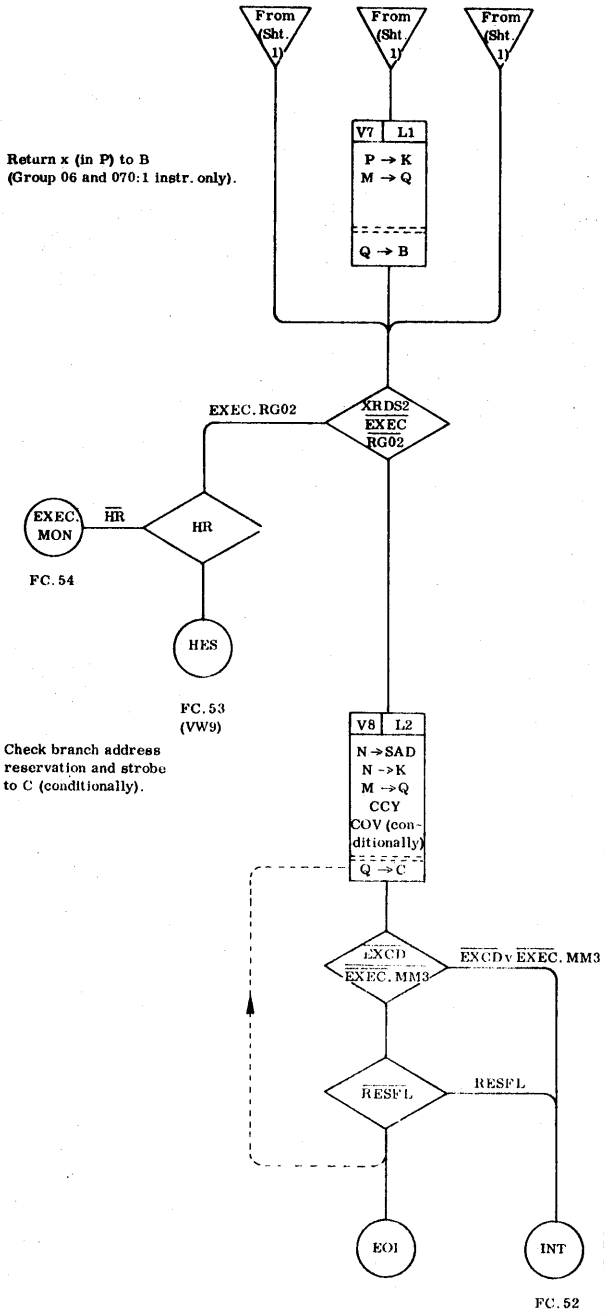
Carry is suppressed between mill slices 14 & 15 (CSM) or 21 & 22 (ESM).

The link includes a record of zero suppression (ZS) in bit 15 (CSM) or bit 22 (ESM) and of overflow in bit 23. If ZS = bit 15, it is transferred to bit 22 on exit from the mill in order to allow the formation of a 22-bit address.

V4: The relative address of the next instruction in the object program is datumised and returned to N.

Carry is suppressed between mill 21 & 22 to protect the ZS and overflow bits included in the link.

V3 / SIGNAL	M.P.	CONDITIONS
EASX-L	3F33:7/72	GALALL (EV3)
EAY-L	3F33:5/72	GALALL (EV3)
(EAAQ-L)	3F33:25/72	EXIT V3 (EV3)
(EAAQ-L*)	3F33:23/72	EXIT V3 (EV3)
(EAR-L)	3F33:21/72	EXIT V3 (EV3)
(EAZ-L)	3F33:3/72	EXIT V3 (EV3)
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3F7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3E7:4/62	
(EBYZ-K)	3F7:25/62	
SC15	3D15:6/112	ESC15 (EV3)
SC22	3D3:22/112	ESC22 (EV3)
CSMNEJ	3E26:3/22	CSM. $\overline{EJ}$
GM15Q22	3F22:12/101	CSMNEJ
EM-Q	3C14:23/167	
EQ-N	3E1:8/83	
EQAQ-N	3E1:2/83	
EQRX-N	3E1:7/83	
EQYZ-N	6D6.26/83	
GDLA	3F31:18/74	
EENKQ-K	3E1:16/83	
ESC22	3E4:26/98	
V4		
ENAJ-K	3D8:25/64	CSM. $\overline{EJM}$
ENKQ-K	3D8:23/64	CSM. $\overline{EJM}$
ENYZ-K	3D8:10/64	CSM. $\overline{EJM}$
ENRX-K	3D8:17/64	$ESM_V EJM$
ED-L:1	3E21:25/75	$\overline{CPR. EXEC}$
ED-L:2	3C21:22/75	$\overline{CPR. EXEC}$
SC22	3D3:22/112	
EM-Q	3C14:23/167	
EQ-N	3E1:8/83	
EQAQ-N	3E1:2/83	
EQRX-N	3E1:7/83	
EQYZ-N	6D6:26/83	
EV8	3A21:12/11	$\overline{EXEC}_V \overline{RG02}$ XRDS2
EJ	2D11:16/142	RG5
XRDS2	3A16:21/8	
HESBKPT	2B15:25/47	XRDS2. EXEC. RG02
EV10	2B1:13/50	XRDS2. EXEC. RG02. $\overline{HR}$



1) Write B to X in VQ of Inst. Phase following.

2) Set ZS if BQ 22. GQ22ZS.

V7: X is returned to B in order that it may be written directly to acc. X in VQ of the Inst. Phase following.

If Executive Trace has been specified by a 125E instruction, a special Executive Monitoring routine is entered in the beat immediately before V8. A hes. break-point occurs at the start of this routine.

V8: N → SAD is provided to initiate reservation check.

EOI if $\overline{EXCD}$. $\overline{EXEC}$. MM3

EXCD - Extracode and is only relevant in Group 07 instructions. If Monitor Mode 3 is specified by the G register or if a RESFL occurs the interrupt sequence is entered in V8.

The branch address is only strobed to C if the conditions for EOI are present as indicated by the broken line. It should be remembered that the conditions are present in V8 and that (as mentioned in the format ecoventions) the strobe terminating any beat followed by 'decision boxes' occurs after the decision boxes.

In 070/1 instr, OV is cleared since a record is maintained in the link.

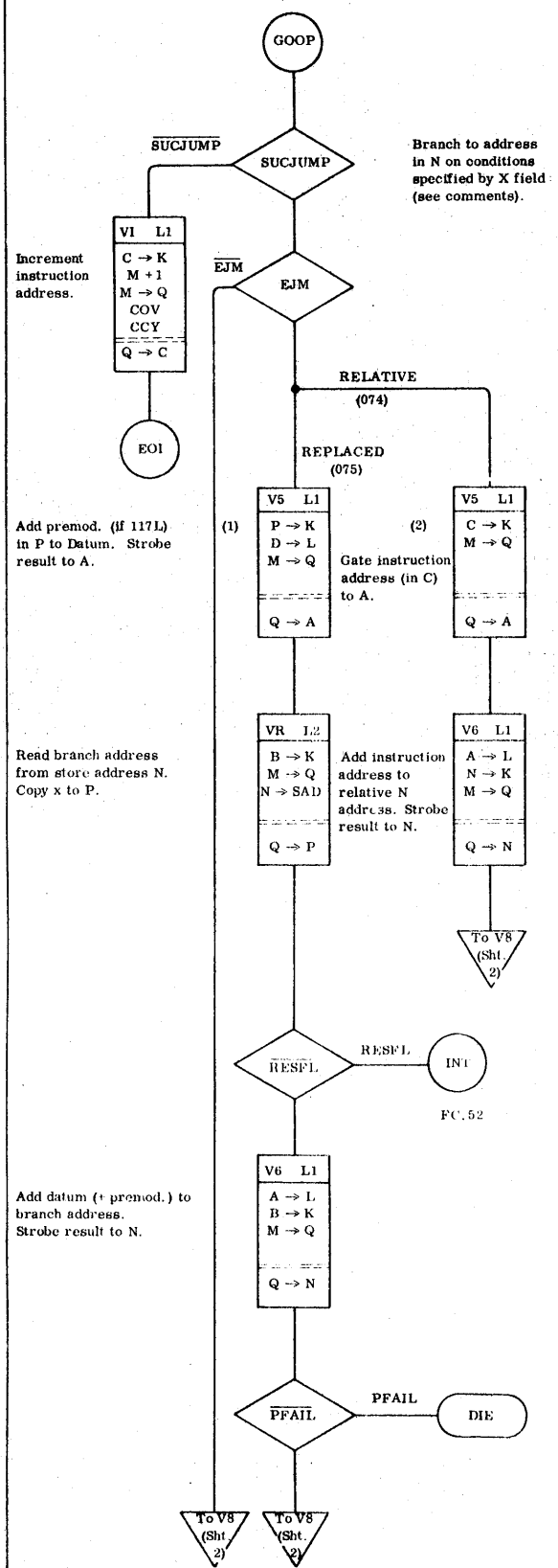
Note that, if a RESFL occurs, the interrupt sequence is entered at V33, but for Monitor Mode 3 the entry point is V36. See signal columns.

In 072:3 instructions, the Zero Suppression bistables takes up the state of the ZS bit (Q22) at the ultimate strobe of V8.

In 070-1 instructions, OV is cleared since a record is maintained in the link.

In 074-5 instructions, OV is cleared if X = 2 or 4 and forced if X = 7. (See conditions on Sheet 1)

COMMENTS	V7 / SIGNAL	M.P.	CONDITIONS
	(EPAJ-K)	3E 9: 3/66	
	(EPKQ-K)	3E 9: 5/66	
	(EPRX-K)	3F 9: 5/66	
	(EPYZ-K)	3F 9:23/66	
	EM-Q	3C14:23/167	
	EQ-B	3D13:15/79	
	EQAJ-B	3D13:21/79	
	EQKM-B	3D13:22/79	
	EQNQ-B	3D13:24/79	
	EQRZ-B	3D13:23/79	
	XRDS2	3A16:21/8	
	EV8	3A21:12/11	XRDS2. ($\overline{EXEC}$ v $\overline{RG02}$)
	hESBKPT	2B15:25/47	XRDS2. EXEC. RG02
	EV10	2B 1:13/50	XRDS2. EXEC. RG02. $\overline{HR}$
	EGNKQ-K		EV8
	V8		
	(EN-SAD)	2E11: 3/93	
	RESFL	2D 7: 6/32	DORLF. $\overline{CPR}$. $\overline{EXEC}$
	(ENAJ-K)	3D 8:25/64	
	(ENKQ-K)	3D 8:23/64	
	(ENRX-K)	3D 8:17/64	
	EM-Q	3C14:23/167	
	EQAX-C	3E17:12/85	$\overline{RESFL}$. $\overline{EXCD}$
	EOI	2A16:15/41	$\overline{EXEC}$. $\overline{MM3}$
	EV33	3B20:20/33	RESFL
	EV36	3A22:18/35	RG00. RG01 $\overline{EXEC}$. $\overline{PM}$. $\overline{RESFL}$
	COV	3E16:25/100	EOI. (I070:1 v I074:5. XD_2 v D4)
	CCY	3F12:18/99	EOI
	GQ22ZS	3D23:25/103	EOI. 1072:3
	FOV	3F21: 9/100	EOI. (I074:5 XD7 v I072:3. RN23)



COMMENTS

Relevant signals active in previous beat:
See signal tables below.

074-077 instructions branch to an address in N under conditions specified by the value of x.

These instructions are entered on GOOP becoming active at the end of the Instruction Phase. Other conditions for entry will have been activated earlier in the Instruction Phase. SUCJUMP is made active as soon as the X field of the instruction is decoded (i.e. on the X Register being loaded) in VDEC, XD0, XD1:2 etc., are decodes of the X field and are interpreted as follows:-

XD0 is active when x = 0.
XD1:2 is active when x = 1 or 2.

SUCJUMP allows a jump to the address in N if:

x = 0 (unconditionally)
x = 1 (if overflow set)
x = 2 (if overflow set - clear overflow)
x = 3 (if overflow clear)
x = 4 (if overflow clear - if not, clear overflow).
x = 5 (if carry set)
x = 6 (if carry clear)
x = 7 (if overflow clear - set overflow).

VI is entered if jump is unsuccessful. V5 and V6 are only entered if Extended Jump Mode (EJM). Otherwise, V8 is entered. EJM allows jumps >32K words. $\overline{\text{EJM}}$ allows jumps ≯32K words. In EJM, jumps may be either relative or replaced.

V5 (REPLACED)

1) If previous 117 instruction (117L active), premodifier is in P. This is added to Datum and result strobed to A. See conditions for EV5 (in table 2 below).

V6 (RELATIVE)

The branch address is formed by adding the current instruction address (now in A) to the relative N address, which may have been premodified in the Instruction Phase. In 'negative jumps', sign extension is carried out in VDEC of the Instruction Phase.

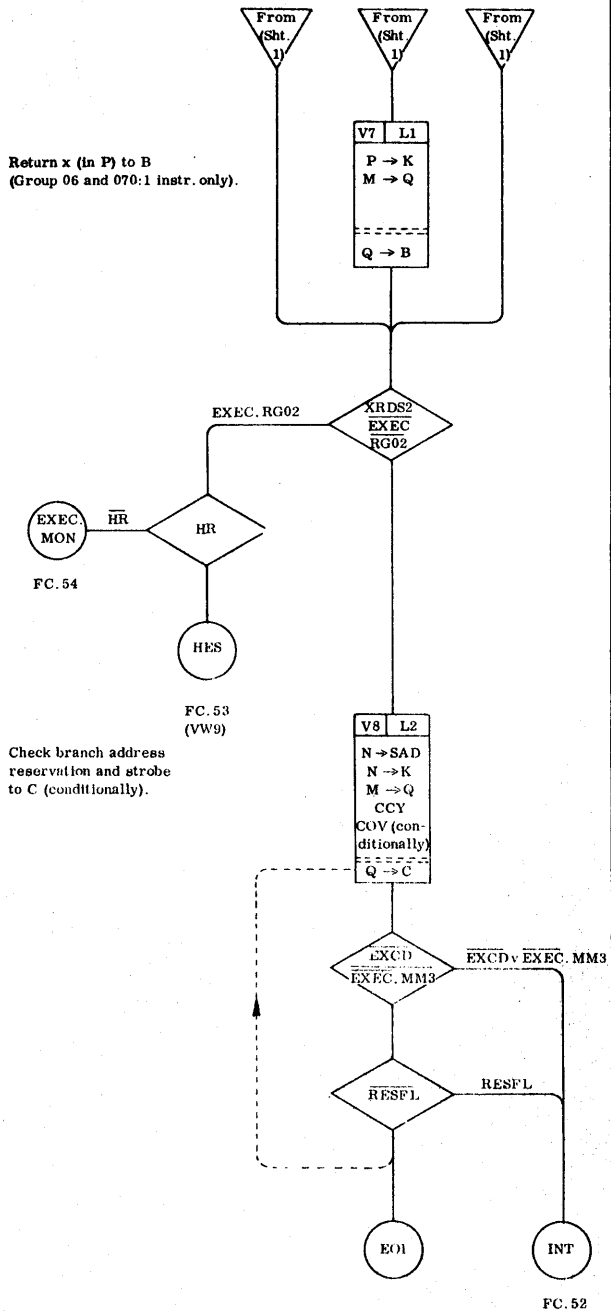
VR (REPLACED)

x (in B) copied into P.
Store location of branch address was datumised and placed in N Register in Instruction Phase. In VR, the store is addressed from N and this part of the branch address is read out to B.

V5 (REPLACED)

Datum or (Datum + Premodifier) was placed in A in V5. Remainder of branch address is now in B. The contents of A and B are added to form the complete branch address which is strobed to N.

INST PHASE / SIGNAL	MP	CONDITIONS
SUCJUMP1	3F23:2/111	$\overline{XD0}_V$
SUCJUMP2	3E23:24/111	$\overline{XD1{:}2\ RC23}_V$
SUCJUMP	3E23:20/111	$\overline{XD347}$
		$\overline{C2311}_V$
		$\overline{X16.RC22}_V$
		$\overline{X16.RC22}$
C23117	Sheet 111	RC23
GOOP	2B13:20/9	
XRDS	2A12:8/30	
XRDS2	3A16:21/8	SUCJUMP1. XRDS
		$\overline{EJ.(I076{:}7}_V$
		$\overline{FPUBUSY)}$
EV1	2B2:18/4	$\overline{SUCJUMP}$
EV5	2B13:3/9	XRDS. SUCJUMP1.
		$\overline{EJ.(I076{:}7}_V$
		$\overline{FPU}_V$
		$\overline{FPUBUSY}$
EV8	3A21:12/11	XRDS2. $(\overline{EXEC}_V \overline{RG02})$
GDLA	3F31:18/74	F0
VI		
ECAX-K	3E10:10/67	
(PLUS 1)	3D24:8/109	
EM-Q	3C14:23/167	
EQAX-C	3E17:12/85	$\overline{RESFL}$
		$\overline{VI.XD7}_V$
COV	3E16:25/100	EOI.
		$(XD2_V XD4)$
CCY	3F12:18/99	
EOI	2A16:15/41	
V5		
(ECAX-K)	3E10:10/67	$\overline{F0}$
(EPAJ-K)	3E9:3/66	117L.REPL
(EPKQ-K)	3E9:5/66	
(EPRX-K)	3E9:5/66	
ED-L:1	3E21:25/75	F0
ED-L:2	3E21:22/75	
EM-Q	3C14:23/167	
EQAZ-A	3F29:23/81	
EV6	3A20:21/10	$\overline{REPL}$
EVR	2A17:5/7	F0
GALALL	3D30:3/70	EV6
ESIN-B	2E17:2/94	
VR		
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3F7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3F7:4/62	
(EBYZ-K)	3F7:25/62	
EM-Q	3C14:23/167	
EQAZ-P	3F3:18/84	
ELS3-XJ	3F19:6/91	HXOP
EHX-B	3F14:18/87	
(EN-SAD)	2E11:3/93	HXOP
RESFL	2D7:6/32	$\overline{DORLF.CPR}$
		$\overline{EXEC}$
RI	5D1:12/276	HXOP
(ESIN-B)	6D4:21/248	
EV6	3A20:21/10	$\overline{RESFL}$
GALALL	3D30:3/70	
V6		
(PCHECK)	3D15:17/112	
DIE	3B33:25/41	PFAIL
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
(ENKQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/64	
EM-Q	3C14:23/67	
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3F7:2/62	
(EBR'-K)	3F7:4/62	
(EBQ-K)	3F7:23/62	
EQ-N	3E1:8/83	
EQYZ-N	3E1:16/83	
EQRX-N	3E1:7/83	
EQAQ-N	3E1:2/83	
XRDS2	3A16:21/8	$\overline{EV7}$
EV8	3A21:12/11	XRDS2. $\overline{EXEC}$. RG02
HESBKPT	2B15:25/47	
EV10	2A5:9/13	XRDS2. EXEC. RG02. $\overline{HR}$
$\overline{EENKQ-K}$	Sheet 64	EV8



1) Write B to X in VQ of Inst. Phase following.

2) Set ZS if HQ 22. GQ22ZS.

COMMENTS	V7 SIGNAL	M.P	CONDITIONS
	(EPAJ-K)	3E 9: 3/66	
	(EPKQ-K)	3E 9: 5/66	
	(EPRX-K)	3F 9: 5/66	
	(EPYZ-K)	3F 9:23/66	
V7: X is returned to B in order that it may be written directly to acc. X in VQ of the Inst. Phase following.	EM-Q	3C14:23/167	
	EQ-B	3D13:15/79	
	EQAJ-B	3D13:21/79	
	EQKM-B	3D13:22/79	
	EQNQ-B	3D13:24/79	
	EQRZ-B	3D13:23/79	
	XRDS2	3A16:21/8	
	EV8	3A21:12/11	XRDS2. (EXEC v RG02)
	hESBKPT	2B15:25/47	XRDS2. EXEC. RG02
	EV10	2B 1:13/50	XRDS2. EXEC. RG02. HR
	EGNKQ-K		EV8
If Executive Trace has been specified by a 125E instruction, a special Executive Monitoring routine is entered in the beat immediately before V8. A hes. break-point occurs at the start of this routine.	V8		
	(EN-SAD)	2E11: 3/93	
	RESFL	2D 7: 6/32	DORLF. CPR. EXEC
	(ENAJ-K)	3D 8:25/64	
	(ENKQ-K)	3D 8:23/64	
	(ENRX-K)	3D 8:17/64	
	EM-Q	3C14:23/167	
	EQAX-C	3E17:12/85	RESFL. EXCD
	EOI	2A16:15/41	EXEC. MM3
	EV33	3B20:20/33	RESFL
V8: N → SAD is provided to initiate reservation check.	EV36	3A22:18/35	RG00. RG01 EXEC. PM. RESFL
	COV	3E16:25/100	EOI. (1070:1 v 1074:5. XD2 v D4)
	CCY	3F12:18/99	EOI
	GQ22ZS	3D23:25/103	EOI. 1072:3
	FOV	3F21: 9/100	EOI. (1074:5 XD7 v 1072:3. RN23)

EOI if EXCD. EXEC. MM3

EXCD = Extracode and is only relevant in Group 07 instructions. If Monitor Mode 3 is specified by the G register or if a RESFL occurs the interrupt sequence is entered in V8.

The branch address is only strobed to C if the conditions for EOI are present as indicated by the broken line. It should be remembered that the conditions are present in V8 and that (as mentioned in the format conventions) the strobe terminating any beat followed by 'decision boxes' occurs after the decision boxes.

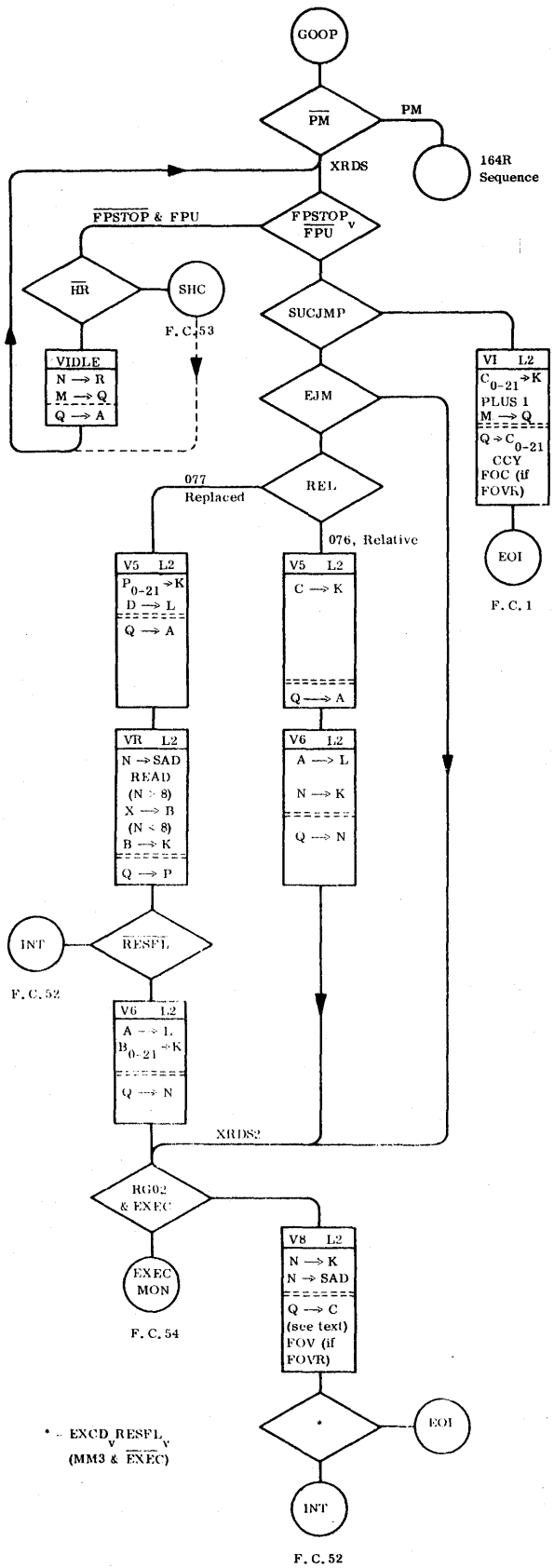
In 070/1 instr, OV is cleared since a record is maintained in the link.

Note that, if a RESFL occurs, the interrupt sequence is entered at V33, but for Monitor Mode 3 the entry point is V36. See signal columns.

In 072:3 instructions, the Zero Suppression bistables takes up the state of the ZS bit (Q22) at the ultimate strobe of V8.

In 070-1 instructions, OV is cleared since a record is maintained in the link.

In 074-5 instructions, OV is cleared if X = 2 or 4 and forced if X = 7. (See conditions on Sheet 1)



COMMENTS

The 076/7 instructions are used to branch to N on the following conditions:

X = 0	branch if a = 0
X = 1	branch if a ≠ 0
X = 2	branch if a ⩾ 0
X = 3	branch if a < 0
X = 4	branch if FOV clear
X = 5	branch if FOV set
X = 6, 7	undefined.

The 076 is used for relative jump address, the 007 for replaced jump addresses.

Where 'a' is the content of the F. P. accumulator.

If the machine is in Priority mode, exit is made to the 164R sequence immediately after the Instruction Phase.

It should be noted that the 076/7 instructions may be used even if the hardware F. P. U. option is not fitted - in this case, the instruction is treated as an extracode and causes a voluntary interrupt to enter Executive upon termination of this sequence.

Where a hardware F. P. U. is fitted, but if not free to engage in a transfer of information, a waiting loop (VIDLE) is entered and cycled until the F. P. U. is free, at which time the main sequence is re-entered. A hesitation break point is provided in each cycle of the loop.

If the F. P. U. is not busy, or where no such unit is fitted, the sequence is entered directly from GOOP. A test is made on the X field and the content of the F. P. U. accumulator or overflow (FOVR) as appropriate.

A successful jump (SUCJMP) is defined as:-

X	a
0	0
1	≠ 0
2	⩾ 0
3	< 0
4	FOVR clear
5	FOVR set

Note:

SUCJMP is forced if $\overline{FPU}$.

1. Relative jumps (076)

The absolute instruction address is formed from the control address in C (strobed to A) plus the relative N address (in N). The result is strobed to N.

2. Replaced jumps (077)

The (premodified) address is datumised and strobed to A. The branch address is then read from store address N (or X) and is copied to P. The (22 bit) branch address is datumised (and premodified if required) and strobed to N.

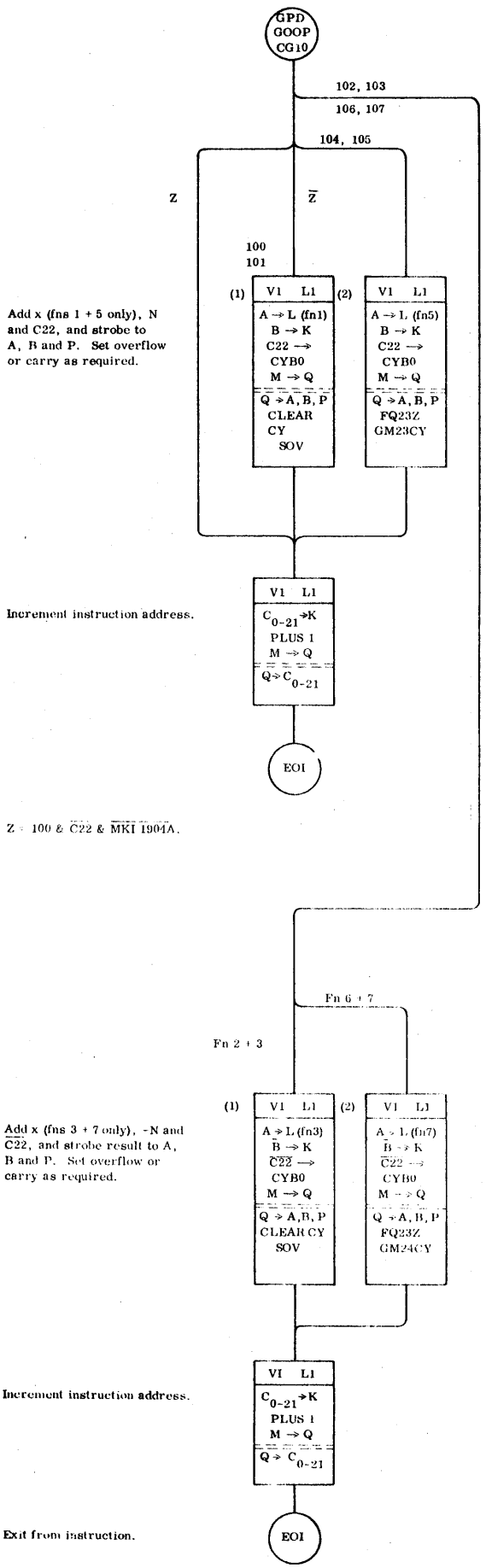
3. EJM

Entry is made directly to V8.

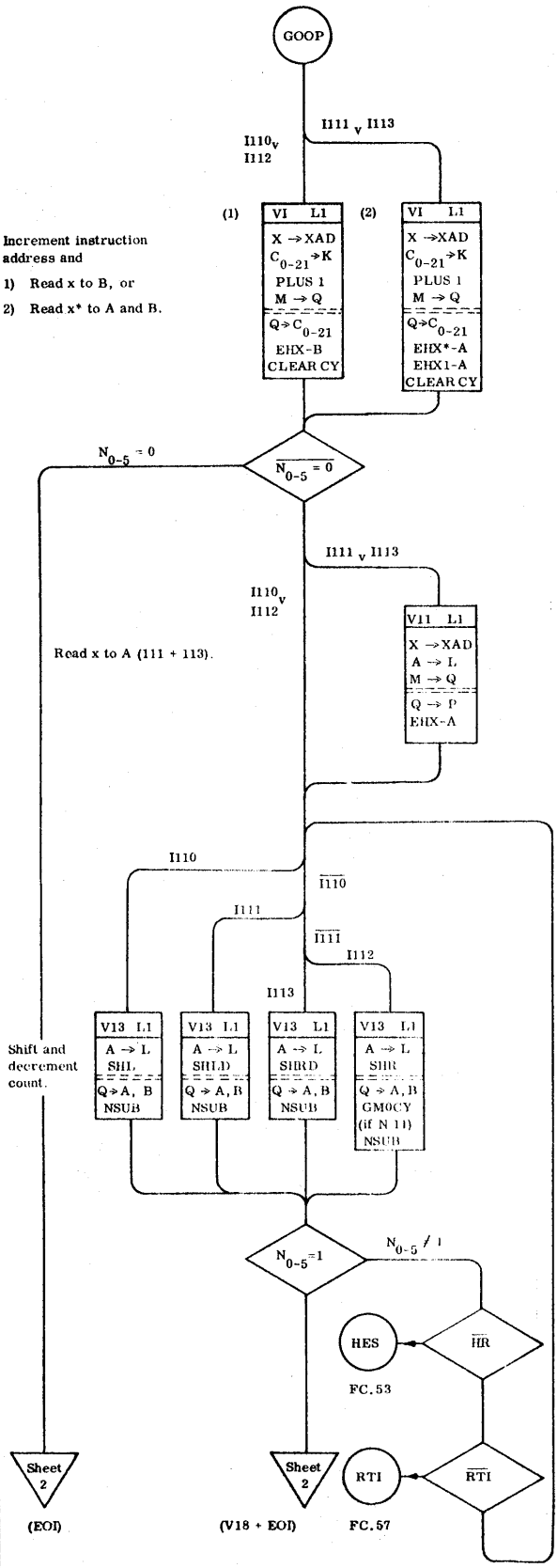
V8 tests the branch address for reservation failure. The address is transferred to C if EXCD & $\overline{RESFL}$ & ($\overline{MM3}$ v EXEC) and the Instruction Phase is entered. If reservation failure has occurred, the Interrupt Sequence is entered.

Overflow is set if the exponent has overflowed, and carry is cleared.

VIDLE SIGNAL	M.P.	CONDITIONS
(ENAJ-K)	3D8:25/64	
(EMKQ-K)	3D8:28/64	
(ENRX-K)	3D8:27/64	
(ENYZ-K)	3D8:10/64	
EQAZ-A	3F29:23/81	
EVIDLE	3A12:2/40	
EV5	2B13:3/9	
EVI	2B2:18/4	
GDLA	3F31:18/74	EV5 & F0
V8		
(ENKQ-K)	3E9:5/66	
(ENRX-K)	3F9:25/66	
(EN-SAD)	2E11:3/93	
CCY	3F12:18/99	EOI
EQAX-C	3E17:4/85	EOI
FOV		
EOI	2A16:15/41	$\overline{EXCD}$ & $\overline{RSFL}$ & EXEC $\overline{MM3}$) v EXCD $\overline{RESFL}$
INT	3C27:23/147	v (MM3 & EXEC)
VI		
(EXAX-K)	3E10:10/67	
(PLUS 1)	3D24:8/109	
EQAX-C	3E17:4/85	$\overline{RESFL}$
CCY	3F12:18/99	
EOI	2A16:15/41	
V5		
(ECAX-K)	3E10:10/67	F0
(EPAJ-K)	3E9:3/66	D17L4
(EPKQ-K)	3E9:5/66	REPL
(EPRX-K)	3E9:25/66	
EQAZ-A	3F29:23/81	
EVR	2A17:5/7	F0
EV6	3A20:21/10	$\overline{REPL}$
GBKALL	3F6:21/61	EVR
EESIN-B	2E17:2/94	$\overline{HXOP}$
GALALL	3D30:3/70	EV6
VR		
(EN-SAD)	2E11:3/93	
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3F7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3F7:4/62	
(EBYZ-K)	3F7:25/62	
EHX-B	3F14:18/87	K > 8
(ESIN-B)	6D4:21/248	$\overline{HXOP}$
EQAZ-P	3F3:18/81	
V6		
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3D33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3F7:4/62	
EQ-N	3E1:8/83	
EQAQ-N	3E1:2/83	
EQRX-N	3E1:6/83	
EQYZ-N	3E1:9/83	
XRDS2	3A16:21/8	V6 & $\overline{EV7}$
EV8	3A21:12/11	$\overline{XRDS2}$ & ($\overline{EXEC}$ v $\overline{RG02}$
EV10	2A5:9/13	RG02 & EXEC & XRDS2 & $\overline{HR}$



COMMENTS	V1 / SIGNAL	MP	CONDITIONS
Relevant signals active in previous beat: GPD, EV1, GALALL (odd fns only), GBKALL (fns 0, 1, 4, 5), PNBAZ-K (fns 2, 3, 6, 7), ECYB0 (fns 0, 1, 4, 5), EENC22 (fns 2, 3, 6, 7).	(EAAQ-L)	3F33:23/72	
	(EAR-L)	3F33:21/72	GALALL (made
	(EASX-L)	3F33: 7/72	by CG10. F0)
	(EAY-L)	3F33: 5/72	
	(EAZ-L)	3F33: 3/72	
	(EBAJ-K)	3F 2:26/62	
	(EBKM-K)	3F 7:24/62	GBKALL (made
F1: F1 is bit 1 of the function register and distinguishes fns 0, 1, 4 and 5 from fns 2, 3, 6, 7.	(EBNP-K)	3F 7: 2/62	by CG10. $\overline{F1}$)
	(EBQ-K)	3F 7:23/62	
	(EBRX-K)	3F 7: 4/62	
Note that Group 10 instructions are literals where N (22-bits in B) is interpreted as an operand, and not as an address.	(EBYZ-K)	3F 7:25/62	
	(ENBAZ-K)	3D 3: 9/112	PNBAZ-K (made by CG0:10. F1)
	(GC22)	2F10:25/112	See comments
	(GNC22)	3D 3:17/112	See comments
	EM-Q	3C14:23/67	
	EQAZ-A	3F29:23/81	
V1: Fn 0 + 1 (1) operate on a s.l. operand, or the m.s. word of a d.c. operand (sets overflow).	EQ-B	3D13:15/79	
	EQAJ-B	3D13:21/79	
Fn 4 + 5 (2) operate on the l.s. word of a d.l. operand. The A → L gating (x in A) is only required for fns 1 and 5.	EQFM-B	3D13:22/79	
	EQNQ-B	3D13:24/79	
	EQRZ-B	3D13:23/79	
	EQAZ-P	3F 3:18/84	
1) CCY clears carry from a previous instruction in C22. Overflow can only occur for fn 1, and is set in C23 by SOV if M23 ≠ M24.	CCY	3F12:18/99	$\overline{F2}$
	SOV	2D 7:18/32	$\overline{F2}$
2) The redundant sign bit in bit 23 of A, B and P is cleared by FQ23Z. Carry is set from bit 23 of the mill output by GM23CY (fn 5 only).	FQ23Z	3F22:25/101	F2
	GM23CY	3F11:10/105	CF 4:5
	GM24CY	2D 7: 9/32	CF 6:7
	EVI	3A16:12/8	
	VI		
VI: The current instruction address is incremented in the mill (PLUS 1 forces data flow CYB0), and restored to C (bits 0-21).	(ECAX-K)	3E10:10/67	
	(PLUS 1)	3D24: 8/109	
	EM-Q	3C14:23/67	
	EQAX C	3E17: 4/85	
	EOI	2A16:15/41	
	EBAZ-X	3F25: 8/91	$\overline{ENDHES}$
EOI: The result (in B) is written to accumulator X in beat VQ of the following Instruction Phase.			
V1: The $\bar{A}$ → L gating is only required for fns 3 and 7.			
1) Carry is cleared from C22 by CCY, and overflow is set in C23 by SOV, if M23 ≠ M24 (fn 3 only).			
2) The redundant sign bit is cleared from A, B and P (FQ23Z) and carry is set by GM24CY for fns 6 and 7, gating $\overline{M24}$ to carry.			
VI: See above.			
EOI: See above.			



Relevant signals active in previous beat:
EVI

VI: The current instruction address is incremented in the mill (PLUS 1), and strobed to C_{0-21}. Carry is cleared from C22 (CCY).

1) For the single length shifts (110, 112) the operand K is read to B.

2) For double length shifts (111, 113) x* is read to A and B.

A test is performed on the count (in N_{0-5}) which, if zero, results in exit from the instruction via EOI. A non-zero count results in entry to V11 or V13 dependent on the instruction.

V11: For the 111, 113 instruction only, V11 is entered. Operand x* (in A) is strobed to register P and x is read to A. This gives the double length operand x: in A and P.

V13: Beat V13 comprises the shift loop, the actual type of shift to be performed being defined by the instruction and the value of Nt (N_{10-11}). For the 112 instruction only, with Nt = 2 + 3 (arithmetic or special types), the l. s. bit of x (M0) is recorded in the carry bistable (GM0CY).

The total number of shift operation to be performed is specified by the count as N_{0-5} (the count can be considered as occupying bits 0-9 of N, the m. s. 4 bits being clear). V13 is cycled continuously until the count, which is reduced by 1 for each cycle, is zero. Note that $N_{0-5} = 1$ primed the next beat, as the count will reduce to zero at the clock ending V13.

VI / SIGNAL	M.P.	CONDITIONS
(ECAX-K)	3E10:10/67	
(PLUS 1)	3D24: 8/109	
ERX-XJ	3F20: 4/89	
EHX-B	3F14:18/87	I110:2
EHX*-A	3D28: 8/108	I111:3
EHX*-B	3F18:18/80	I111:3
EQAX-C	3E17:12/85	
EM-Q	3C14:23/167	
CCY	3F12:18/99	
EV11	2A 6:16/4	I111:3. $\overline{N0-5=0}$
GALALL	3D30: 3/70	(I110:3. EV13) + (I111:3. EV11)
EV13	2A18: 5/16	VI. I110:2. $\overline{N0-5 = 0}$
EOI	2A16:15/41	VI. I110:3. N0-5 = 0
V11		
(EAAQ-L)	3F33:25/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33: 7/72	
(EAY-L)	3F33: 5/72	
(EAZ-L)	3F33: 3/72	
ERX-XJ	3F20: 4/89	
EM-Q	3C14:23/167	
EQAZ-P	3F 3:18/84	
EHX-A	3D26:18/88	
EV13	2A18: 5/16	I11:3. V11
GALALL	3D30: 3/70	I110-3. EV13
V13		
(EAAQ-L)	3F33:25/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33: 7/72	
(EAY-L)	3F33: 5/72	
(EAZ-L)	3F33: 3/72	
SHL	3D33: 8/102	I110
DSHL	3F27:20/105	I111
SHR	3F26:10/97	I112
DSHR	2C 9:13/42	I113
EQ-B	3D13:15/79	
$\overline{\text{EQAJ-B}}$	3D13:21/79	
$\overline{\text{EQKM-B}}$	3D13:22/79	
$\overline{\text{EQNQ-P}}$	3D13:24/79	
$\overline{\text{EQRZ-B}}$	3D13:23/79	
EQAZ-A	3F29:23/81	
GM0CY	3E11:13/114	I112. N11
NSUB	3F18:21/80	
EV18	3B12:22/23	N0-5=1.(I111:3+ I112. N11)
$\overline{\text{EPKALL}}$	Page 66	I111:3
$\overline{\text{GBKALL}}$	3F 6:21/61	I112. N11
ECYB0	3F 2:25/96	I112. N11
EOI	2A16:15/41	N0-5 1. (I110+ I112. $\overline{\text{N11}}$)
EV13	2A18: 5/16	V13. $\overline{\text{N0-5=1}}$ I110-3. $\overline{\text{HR. RTI}}$
GALALL	3D30: 3/70	EV13. I110-3

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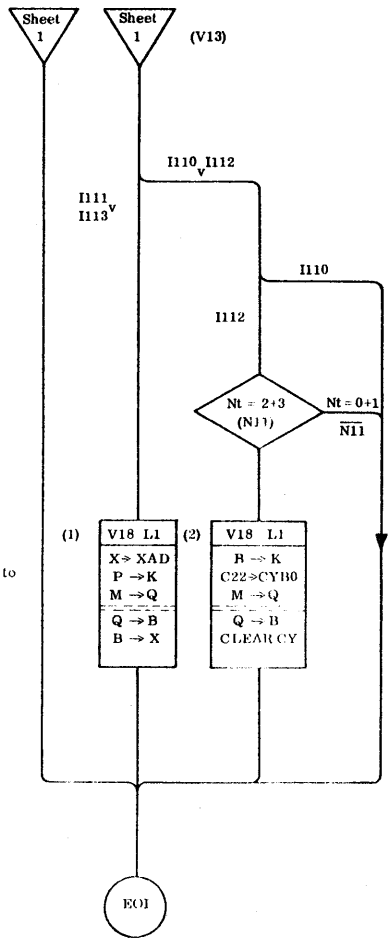
ICL | 1904A MK II 1904S 1903T | 110-113 INSTRUCTIONS (GOOP-V13) | FC 29 SHEET 1 OF 2



1) Write x* to X.

2) Add C22 to x, strobe to B.

Exit

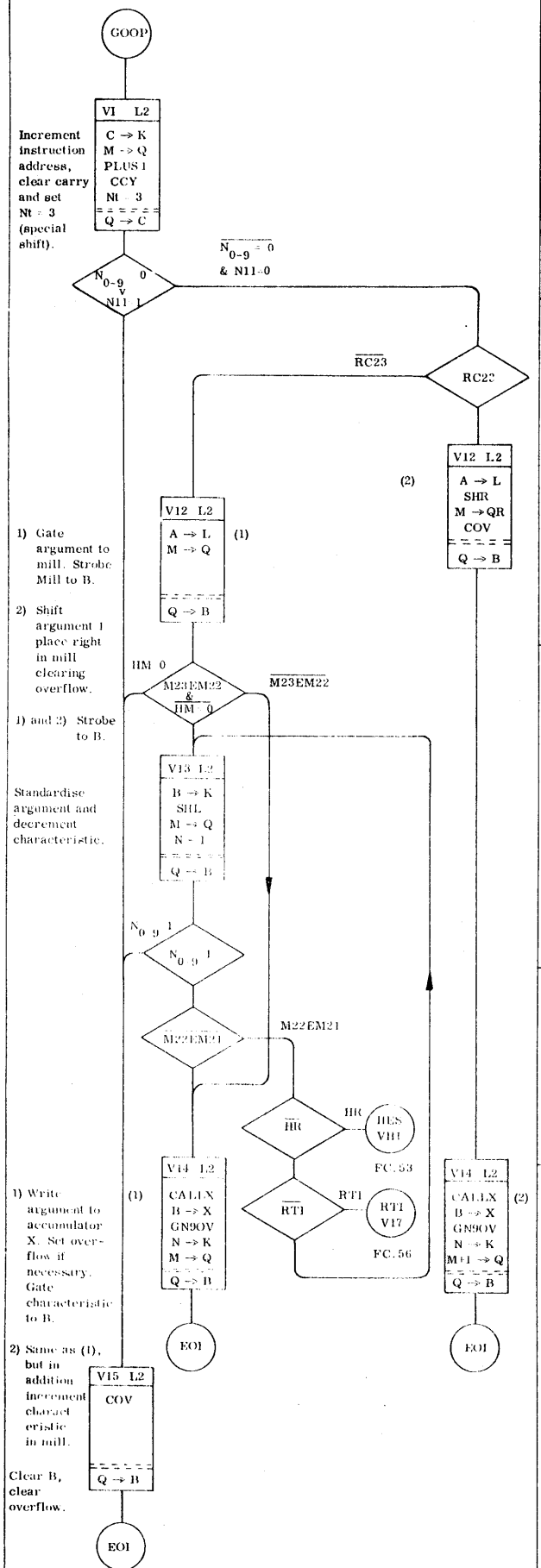
V18:

1) Double length - the new value of x (in B) is written to X, and the new value of x* is transferred from P to B.

2) 112 with Nt = 2 + 3 only - C22 (set in V13) is added to the new value of x (in B) and the result strobed to B. Carry is cleared by CCY.

EOI: The new value of x is written to X for the 110, 112 instructions, while for the 111, 113 instruction X + 1 is loaded with the new value of x*.

COMMENTS	V18 SIGNAL	MP	CONDITIONS
	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3F7:24/62	
	(EBNP-K)	3E7:2/62	GBKALL
	(EBQ-K)	3F7:23/62	
	(EBRX-K)	3E7:4/62	
	(EBYZ-K)	3F7:25/62	
	(EPAJ-K)	3E9:3/66	
	(EPKQ-K)	3E9:5/66	EPKALL
	(EPRX-K)	3F9:25/66	
	(EPYZ-K)	3F9:23/66	
	(GC22)	2F10:25/112	ECYB0
	ERX-XI	3F20:4/89	
	EM-Q	3C14:23/167	
	$\overline{EQ-B}$	3D13:15/79	
	$\overline{EQAJ-B}$	3D13:21/79	
	$\overline{EQKM-B}$	3D13:22/79	I111:3 + (I112. N11)
	$\overline{EQNQ-B}$	3D13:24/79	
	$\overline{EQRZ-B}$	3D13:23/79	
	CCY	3F12:18/99	I112. N11



COMMENTS

Relevant signals active in previous beat:
GOOP, I114:5, EVI.

VI: Increment instruction address, clear carry and set Nt = 3.
$C_{0-21} \rightarrow K$.
Add 1 to M0 (data flow CYB0).

Force $\overline{C22}$ (Clear any carry from previous instructions).

Force Nt (N10 & N11) to 3 for 'special' shift.

EV12 made if characteristic +ve (N11) and not zero ($N_{0-9} \neq 0$).
EV15 made if characteristic -ve (N11) or zero ($N_{0-9} = 0$).

Argument (in A) → L.

V12 (2)

If C_{23} is set (indicating argument overflow), the overflow is cleared by doing a special right shift of the argument (Nt = 3). This is compensated for by incrementing the characteristic in the next beat (V14 (2)).

V12 (1)

If $\overline{RC23}$ (no overflow); the argument is simply gated through the mill and strobed to B.

EV13 made if M23 ≡ M22 (i.e. argument has still to be standardised) and OV not set.

EV14 for V14 (2) made if OV not set and argument already standardised.

EV15 made if OV not set and argument = 0
N_{0-8} is gated to the K highway.

Argument standardised by repeatedly shifting left one place. Characteristic (N_{0-8}) decremented by 1 at each shift.

Hesitation break-point and Real Time Interrupt at each cycle of the loop.

Loop cycled until argument is standardised or characteristic = 0.

Note that N_{0-9} is gated (to conform with other instructions) but only N_{0-8} is used.
EV17 is entry to 'Real Time Interrupt' Sequence.
EV14: if $N_{0-9} = 1$ is active before the final strobe of V13, a zero character is indicated since on the final strobe N_{0-9} would (due to NSUB1) be made 0.
M22EM21 indicates argument in standard form.
EV15: Enter if $N_{0-9} = 1$.
Hesitation break-point (intra order type 3) entered if argument non standard (and non zero).

V14 (1)

$N_9 = 1$ indicates characteristic overflow, so set C_{23} (see WGHN01/361).
Argument written to accumulator X (from B).
Characteristic → B.

V14 (2)

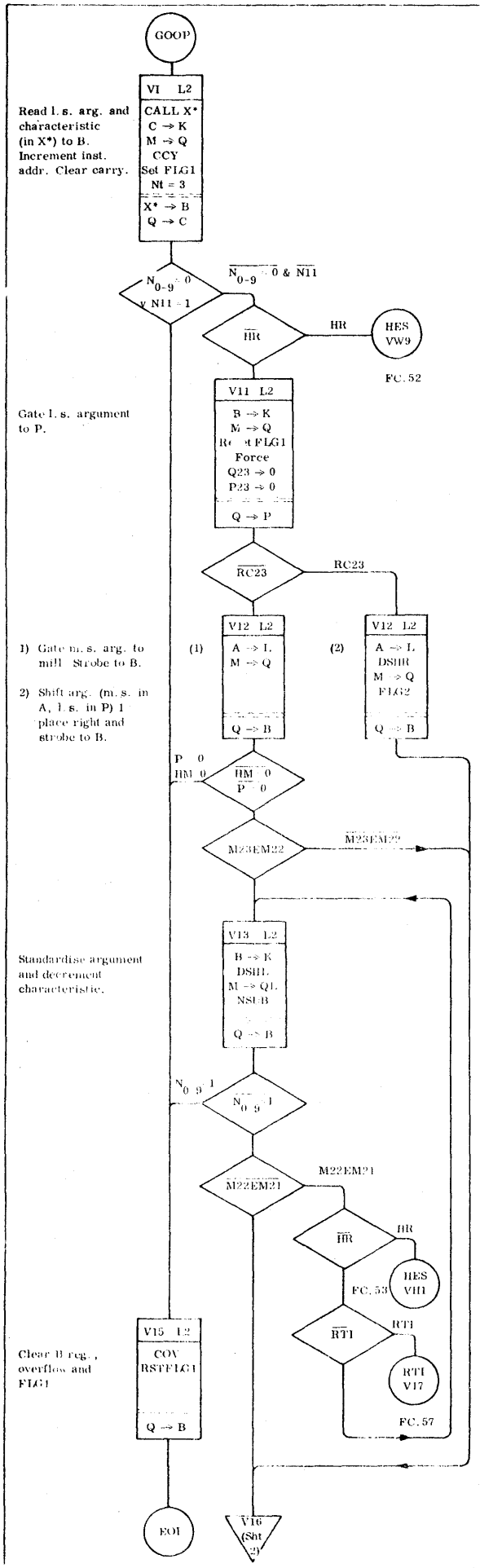
As for V14 (1), but characteristic is incremented by 1 in mill before being strobed to B.

EOI. In VQ of Instruction Phase following, characteristic is written to X + 1 or zero is written to X and X + 1.

V15: B is cleared by gating Q (all noughts) to B.
Overflow (C_{23}) is cleared.

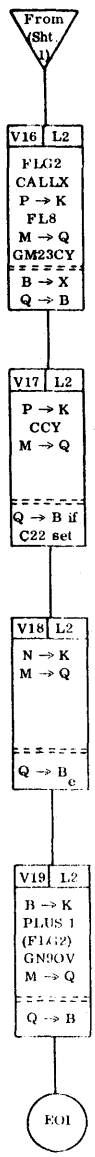
EOI: Comments as for EOI in V14.

V1 SIGNAL	M P	CONDITIONS
ECAX-K	3E10:10/67	
(PLUS 1)	3D24:8/109	
EM-Q	3C14:23/167	
EQAX-C	3E17:12/85	$\overline{RESFL}$
CCY	3F12:18/99	
FNT3	2D7:23/32	
EV12	3B11:10/15	$N_{0-9} = 0$ & $\overline{N_{11}}$
EV15	2A8:9/19	$N_{11} = 1$ v $N_{0-9} = 0$
GALALL	3D30:3/70	
V12		
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
SHR	3F26:10/97	RC23
EM-QR	6C33:7/248	SHR
COV	3E16:25/100	DNT3
EM-Q	3C14:23/167	SHR
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
EV13	2A18:5/16	M23EM22. HM=0
EV14	2A7:9/18	$\overline{M23EM22}$ v RC23
EV15	2A8:9/19	$\overline{RC23}$. HM=0
V13		
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3E7:4/62	
(EBYZ-K)	3F7:25/62	
SHL	3D33:8/102	
EM-Q	3C14:23/167	
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
NSUB	3F18:21/80	
EV14	2A7:9/18	$N_{0-9} = 1$. $\overline{M22EM21}$
EV13	2A18:5/16	$N_{0-9} = 1$. {M22EM21 / RTI.HR}
EV15	2A8:9/19	$N_{0-9} = 1$
HESBKPT	2B15:24/47	$N_{0-9} = 1$. M22EM21
EV14	2A16:3/21	$N_{0-9} = 1$. {M22EM21 / HR}
HES6	2C13:12/46	
V14		
GN9OV	3D23:12/103	
LRX-XJ	3E20:1/75	
EBAZ-X	3F25:8/90	
(ENAJ-K)	3D8:25/61	
(PLUS 1)	3D24:8/109	
EM-Q	3C14:23/167	
EQ-B	3D13:15/79	
EQKM-B	3D13:22/79	
EQAJ-B	3D13:21/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
EOI	2A16:15/11	$\overline{EV15}$
V15		
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
COV	3E16:25/100	
EOI	2A16:15/11	



COMMENTS
Relevant signals active in previous beat: GOOP, I114:5, EVI, SETFLG.
VI: Force $\overline{C22}$ (clear any carry from previous instructions). Force Nt (N10 & N11) tp 3 for 'special' shift. Set FLG1.
If characteristic negative or zero, next beat is V15. If characteristic positive, enter hes. break-point No. 3 at VW9. If no further hes. requests, next beat is V11.
V11: Reset FLG1 (this has indicated the path selected). Clear Q23 which clears P23 when Q → P.
$FDEC_1$ is made by I115.
Set V12 1) if overflow clear.
2) if overflow set.
V12:
(2) m. s. arg. is in A, l. s. in P. Nt = 3 still set, so this is special shift which clears OV.
V15: Entered if l. s. and m. s. arg. = 0.
V13: Entered if arg. non-standard (M23 ≠ M22)
V16: Entered if arg. standard (M23 / M22)
V13: Argument standardised by repeatedly shifting left 1 place. Note that P (containing l. s. portion) uses 'internal' shift and P → K is not required. Characteristic (in N_{0-8}) is decremented by 1 at each cycle.
If characteristic = 0, exit to V15 (note that N_{0-9} is gated to conform with other instructions) but only N_{0-8} is used.
At conclusion of each V13 beat, if test shows non-standard arg. (M22EM21) and char. ≠ 0 ($\overline{N_{0-9}}$ = 1), enter HESBKPT type 3. Then, if $\overline{HR}$, enter RTI (if required), afterwards returning to recycle V13. If arg. standardised and char. ≠ 0, enter V16. Note that if N_{0-9} = 1 is active before the final strobe of V13, a zero char. is indicated, since on final strobe N_{0-9} would (due to NSUB) be made 0.
V15: Q → B 'clears' B since Q is 'all noughts'. FLG1 is reset.

VI SIGNAL	MP	CONDITIONS
ERX-XJ	3E20:4/89	
EHX*-B	3F18,18/80	
ECAX-K	3E10:10/67	
(PLUS 1)	3D24:8/109	
EM-Q	3C14:22/167	
EQAX-C	3E17:12/86	
CCY	3F12:18/99	
FNT3	2D7:23/37	
(FLG 1)	3C32:34/152	
HESBKPT	2B15:25/47	$\overline{N0-9}$ 0. $\overline{N11}$
EV11	2A6:16/14	$\overline{HR}$
EV15	2A8:9/19	N0-9 0, N11
GBKALL	3E6:21/61	
V11		
RSTFLG1	3C31:10/150	
FQ23Z	3F22:25/101	
EM-Q	3C14:23/167	
EQAZ-P	3F3:18/84	
FDEC1	2E13:9/48	
EV12	3B11:10/15	FDEC1
GALALL	3D30:3/70	
V12		
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F3:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
EM-Q	3C14:23/167	
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
DSHR	2C9:13/42	RC 23
EPKALL	Page 66	EV16
EV16	2A9:9/20	RC 23 v M23EM22
EV13	2A18:5/16	HM 0 P 0. M23EM22. $\overline{RC23}$
EV15	2A8:9/19	P 0. RC23. HM 0
GBKALL	3E6:21/61	
V13		
(EBAJ-K)	3E7:26/67	
(EBKM-K)	3E7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3E7:23/62	
(EBRN-K)	3E7:4/62	
(EBYZ-K)	3E7:25/62	
EM-Q	3C14:23/167	
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
I115:190	Page 79	
NSUB	3E15:21/80	
EV15	2A8:9/19	N0-9 1
HESBKPT	2B15:25/47	$\overline{N0-9}$ 1 M22EM21
EV13	2A18:5/16	$\overline{N0-9}$ 1. $\overline{RTI}$. M22EM21. $\overline{HR}$
EV17	2A10:3/21	$\overline{N0-9}$ 1. $\overline{HR}$ M22EM21. RTI
EV16	2A9:9/20	$\overline{N0-9}$ 1 M22EM21
EFL08	3E11:25/111	
VI		
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
COV	3E16:25/100	
RSTFLG1	3C31:10/150	
EOI	2A16:15/41	



V16: Force bit 8 of L to 1. Since P → K (EPKALL) made by EV16. FL08 adds 1 to bit 8 of l. s. argument. If this bit is already 1, CY will add 1 to bit 9. L, S. argument is now rounded at bit 9 and thus consists of bits 9-22 of l. s. word. If this operation results in overflow, it is registered in C_{22} (GM23CY).

(Characteristic is in N).

V16 SIGNAL	M P	CONDITIONS
(FLG2)	3C32:23/152	V12
ERX-X)	3F20:4/89	
EBAZ-X	3F25:8/90	
FL08	3D15:9/112	
(EPYZ-K)	3F9:23/66	
EM-Q	3C14:23/167	
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
GM23CY	3F11:10/105	
EV17	2A10:3/21	
EPKALL	Page 66	

V17: Unrounded l. s. argument (in P) → B. Since $P_{0-8} = 0$ the characteristic in B is cleared.

If carry set in V16, clear it and replace rounded with unrounded from P for the special case where rounding clears the l. s. word.

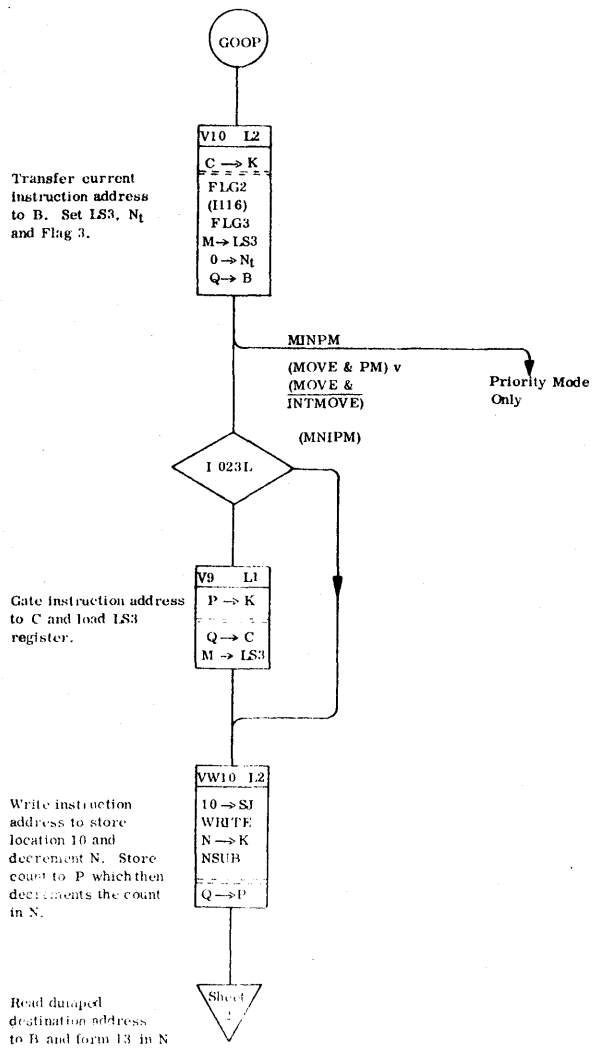
V17		
(EPAJ-K)	3E9:3/66	
(EPKQ-K)	3F9:5/66	
(EPRX-K)	3F9:25/66	
(EPYZ-K)	3F9:23/66	
EM-Q	3C14:23/167	
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
CCY	3F12:18/99	
EV18*	3B17:12/29	
EV18	3B12:22/23	EV18*
GNKIP	3D9:10/63	
ENKALL	3F8:7/64	

V18: $N_{0-8} \rightarrow K$ $Q_{0-8} \rightarrow K$ At the end of this beat the (unrounded) l. s. argument and the characteristic are in B.

V18		
(ENAJ-K)	3D8:25/64	
(ENKQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/64	
(ENYZ-K)	3D8:10/64	
EM-Q	3C14:23/167	
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EV19	2A11:9/24	
GBKALL	3F6:21/61	

V19: Set overflow if characteristic overflows ($N_9 = 1$). Reset FLG2.

V19		
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:21/62	
(EBNP-K)	3F7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3F7:4/62	
(EBYZ-K)	3F7:25/62	
(PLUS1)	3D24:8/103	FLG2
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
GN9OV	3D23:12/103	
FLG2	3C32:25/152	
EOI	2A16:15/41	



COMMENTS

The INTMOVE bistable will be set at entry if the order has been previously interrupted and will remain set until the end of the sequence. I023L will also be set if the previous order was an 023 (OBEY) instruction. If the 116/126 order is given while the processor is in Priority Mode, PM is set. Also active at entry time will be MOVE, I126 I116, and EV10. MINPM = interrupted 116/126 & $\overline{PM}$; MNIPM = interrupted (116/126 and PM.) v (MOVE $\overline{INTMOVE}$).

V10:

The current instruction address will be in C from the Instruction Phase. N_t is forced to 0 to specify a cyclic shift FLG3 is set FLG2 is also set if 116.

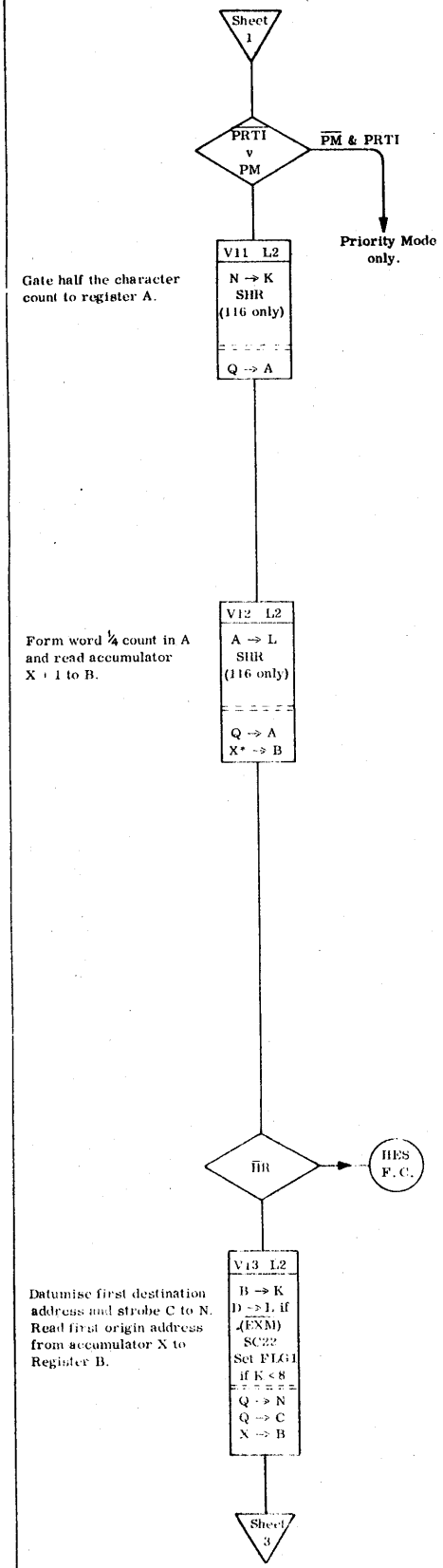
V9:

If INTMOVE is not set or if the processor is in Priority Mode, and I023L is set, V9 is entered. The instruction address will have been gated to P in the final beat of the 023 instruction in this case and this is now transferred to C, LS3 being loaded from the l. s. 3 bits of the address. This beat is omitted if an 023 was not the last order.

VW10:

The instruction address (in B from the Instruction Phase if I023L or in B from V10 if $\overline{I023L}$) is dumped to store location 10 and the word or character count in N0 - 9 is decremented by 1 and transferred to P.

V10 / SIGNAL	MP	CONDITIONS
(ECAX-K)	3E10:10/67	
(ECY-K)	3F10:25/67	
(ECZ-K)	3F10:19/67	
$\overline{EQAJ-B}$	3D13:21/79	
$\overline{EQKM-B}$	3D13:22/79	
$\overline{EQNQ-B}$	3D13:24/79	
$\overline{EQRZ-B}$	3D13:23/79	
EQ-B	3D13:15/79	
EM-LS3	3E19:3/91	
FNT0	3D17:4/22	
EVW10	3A18:10/38	$I\ 023L_v$(INTMV & $\overline{PM}$)
EV9	2A4:9/12	I 023L & (PM_v $\overline{INTMOVE}$)
$\overline{EEB-SO}$	2F7:17/160	EVW10
$\overline{EPKALL}$	Page 66	EV9
VW10		
(FSAD10)	2F10:9/112	
FRCE1	2F3:3/115	
FRCE3	2F3:6/115	
(EB-SO)	3E21:9/75	
$\overline{(FK1)}$	3D5:8/68	MINPM
$\overline{(FK2)}$	3D5:24/68	MINPM
$\overline{(FK3)}$	3D5:22/68	MINPM
$\overline{EQAQ-N}$	3E1:2/83	MINPM
EQRX-N	3E1:7/83	MINPM
EQYZ-N	3E1:16/83	MINPM
EQ-N	3E1:8/83	MINPM
EQAZ-A	3F29:23/81	MINPM
(ENAJ-K)	3D8:25/61	MNIPM
EQAZ-P	3F3:18/84	MNIPM
NSUB	3F18:21/80	MNIPM
EV11	2A6:16/14	
EESIN-B	2E17:2/94	MOVE & INTMOVE & $\overline{PM}$
EEC-SAD	2F6:18/92	$\overline{INTMOVE}$ & $\overline{PM}$ & PRTI & $\overline{HXIN}$
V9		
(EPAJ-K)	3E9:3/66	
(EPKQ-K)	3E9:5/66	
(EPRX-K)	3E9:25/66	
(EPYZ-K)	3E9:23/66	
EQAX-C	3E17:12/85	
EM-LS3	3E19:3/91	
EVW10	3A18:10/38	
EEB-SO	2F7:17/106	
V11		
(EN-SAD)	2E11:3/93	MINPM
(READ)	2E14:12/162	MINPM
(ESIN-B)	6D1:21/248	See Comments
(EC-SAD)	3C14:8/116	See Comments
ELS3-XJ	3F19:6/91	$\overline{INTMOVE}$ & PRTI & $\overline{HXIN}$
LHX-B	3F14:18/87	$\overline{INTMOVE}$ & PRTI & $\overline{HXIN}$
NSUB	3F18:21/80	MINPM
SHR	3E20:10/97	MNIPM & I 126
(ENAJ-K)	3D8:25/61	MNIPM
EQAZ-A	3F29:23/81	MNIPM
EV12	3B11:10/15	
EESIN-B	2E17:2/94	MINPM
EEB-SO	2F7:17/106	MNIPM & PRTI
ESC22	3E4:26/98	MINPM
GD1A	3F31:18/74	MINPM
$\overline{GBKALL}$	3F6:21/61	MINPM
GALALL	3D30:3/70	MNIPM



Gate half the character count to register A.

Form word ¼ count in A and read accumulator X + 1 to B.

Datumise first destination address and strobe C to N. Read first origin address from accumulator X to Register B.

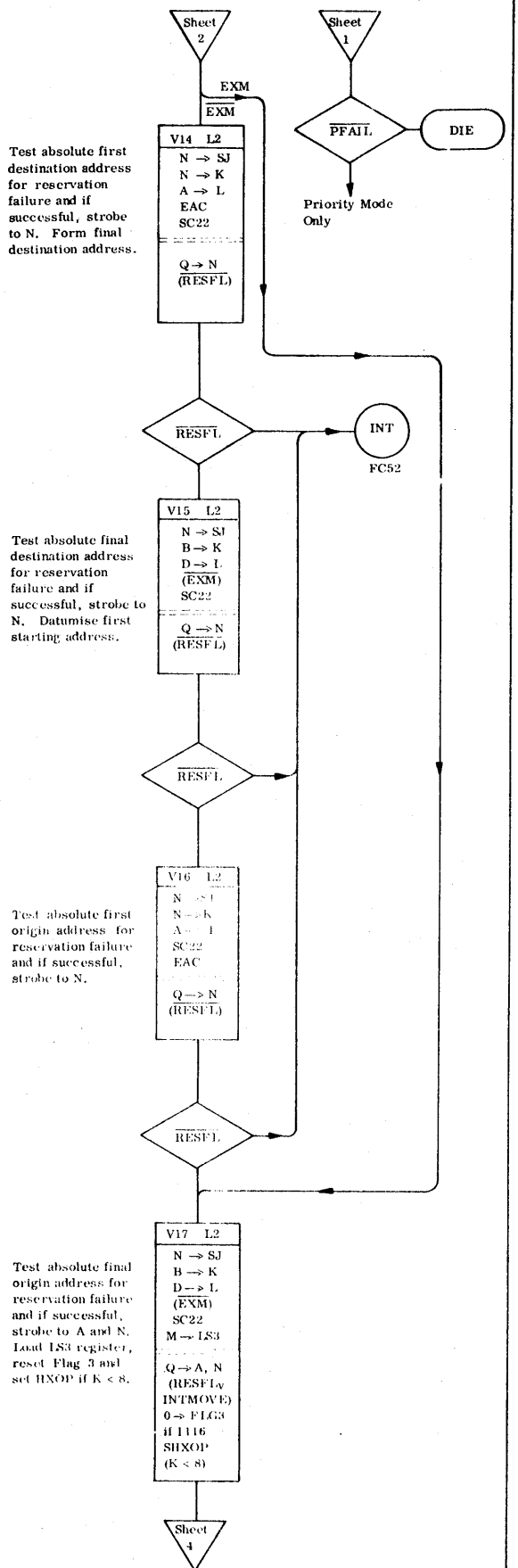
PRTI will be set if Real Time Interrupts are permitted.

V11: If RTI's are not permitted or if the processor is in PM, the character count is gated from N and shifted one place right (for the 116 only) to give ½ the character count in A.

V12: The ¼ or character count is formed from half the count (in V11) by a further right shift. In the case of PM & PRTI, address 11 is forced, the instruction accessed in V11 is dumped there and accumulator X + 1 is read to B to give the first destination address.

V13: The first destination address accessed in V12 is datumised (if the processor is not in Executive Mode) and FLAG1 is set if the address is less than 8 (i. e. K > 8). The datumised address (undatumised in EXM) is then placed in N and C. Accumulator X is read to give the first origin address in B.

COMMENTS	V12 SIGNAL	M P	CONDITIONS
	(EN-SAD)	2E11:3/93	
	(READ)	2E4:12/162	MINPM
	(ESIN-B)	6D4:21/248	
	FSAD11	3F7:3/62	MNIPM
	(WRITE)	2E4:6/162	MNIPM &
	(EB-SO)	3E21:9/75	PRTI
	NSUB	3F18:21/80	MINPM
	(SC22)	3D3:22/112	
	(ED-L:1)	3E21:25/75	EXEC & $\overline{\text{CPR}}$
	(ED-L:2)	3E21:22/75	& MINPM
	SETFLG1	3C30:10/150	MINPM & K < 8
	(EBAJ-K)	3F7:26/62	
	(EBNP-K)	3E7:2/62	
	(EBQ-K)	3F7:23/62	
	(EBKX-K)	3E7:4/62	MINPM
	(EBYZ-K)	3F7:25/62	
	EQCALL	3E17:9/85	
	EQAX-C	3E17:12/85	
	EQZ-C	3E17:16/85	
	EBX*-B	3F18:18/80	MNIPM
	SHR	3F26:10/97	MNIPM & H26
	(EAAQ-L)	3F33:25/72	
	(EAAQ-L*)	3F33:23/72	
	(EAR-L)	3F33:21/72	
	(EASX-L)	3F33:7/72	MNIPM
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	EQAZ-A	3F29:23/81	
	(PCHECK)	3D15:17/112	
	EV13	2A18:5/16	
	EESIN-B	2E17:2/94	MINPM
	GDLA	3F31:18/74	MNIPM
	ESC22	3E4:26/98	
	GBKALL	3F6:21/61	MINPM
	V13		
	(EN-SAD)	2E11:3/93	
	(READ)	2E4:12/162	MINPM
	(ESIN-B)	6D4:21/248	
	(FLG1)	3C30:24/152	MINPM & K < 8
	(ED-L:1)	3E21:25/75	MINPM &
	(ED-L:2)	3E21:22/75	CPR & $\overline{\text{EXEC}}$
	(SC22)	3D3:22/112	MNIPM
	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3E7:24/62	
	(EBNP-K)	3E7:2/62	See
	(EBQ-K)	3F7:23/62	Comments
	(EBKX-K)	3E7:4/62	
	(EBYZ-K)	3F7:25/62	
	EQAQ-N	3E17:3/83	
	EQRS-N	3E17:7/83	
	EQYZ-N	3E17:16/83	See FLG1
	EQ-N	3E17:5/83	
	EQCALL	3E17:9/85	
	EQAX-C	3E17:12/85	
	EQZ-C	3E17:16/85	MNIPM
	EQAZ-P	3E3:18/81	MINPM
	EBX-B	3F14:18/80	MNIPM
	SETFLG1	3C30:10/150	MNIPM & K < 8
	EV11	2A7:9/16	$\overline{\text{EXEC}}$ & (EXECABOVE Page 61)
	EV17	2A10:3/24	EXEC & MINPM
	ENKALL	3E8:7/64	MNIPM &
	EENKQ-K	Page 61	LV14
	GALALL	3D30:3/70	
	ESC22	3E4:26/98	EV14 & MNIPM



Test absolute first destination address for reservation failure and if successful, strobe to N. Form final destination address.

Test absolute final destination address for reservation failure and if successful, strobe to N. Datumise first starting address.

Test absolute first origin address for reservation failure and if successful, strobe to N.

Test absolute final origin address for reservation failure and if successful, strobe to A and N. Load LS3 register, reset Flag 3 and set HXOP if K < 8.

COMMENTS

V14:

If the processor is not in Executive Mode, the first destination address is tested for a reservation failure. If this does not occur, the address is strobed to N. Should a reservation failure be found, entry is made to the interrupt sequence. The count is added to the first destination address to give the final destination address.

V15:

The final destination address formed in V14 is tested for reservation failure and the first starting address is datumised and strobed to N if no reservation failure has occurred.

V16:

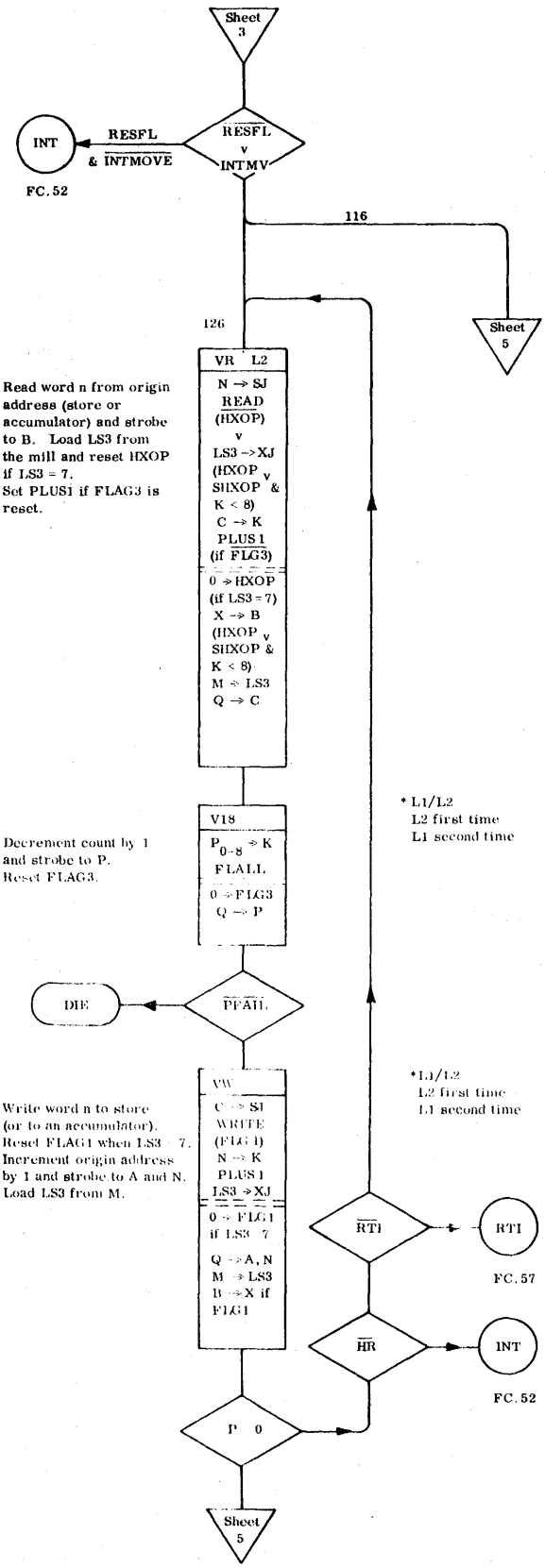
The first origin address formed in V15 is tested for reservation failure and if none occurs, the count is added to it to give the final origin address in N.

V17:

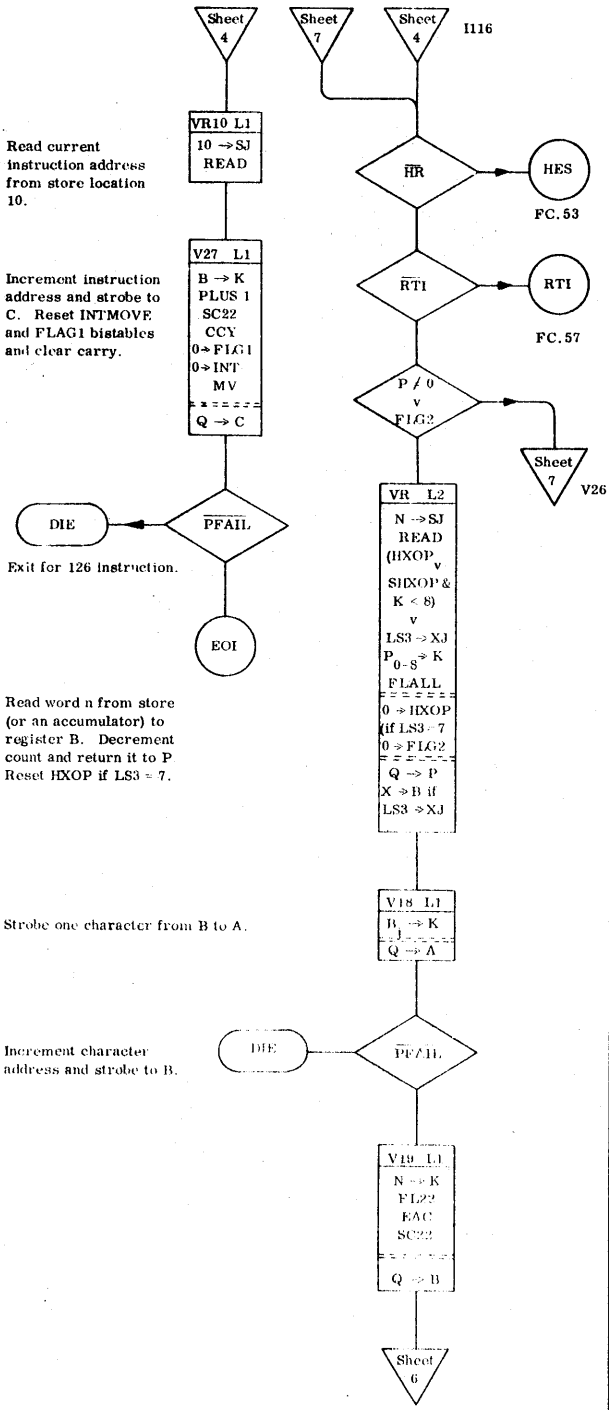
The final origin address formed in V16 is tested for reservation failure. If entry was from V13 (EXM) the first origin address is strobed to A and N. If entry was from V13 (INTMOVE), the first origin address is datumised and strobed to A and N. Flag 3 is reset and HXOP set if the address is less than 8 (i.e K < 8).

V14 / SIGNAL	MP	CONDITIONS
V14		
(EN-SAD)	2E11:3/93	MNIPM
(ENAJ-K)	3D8:25/64	
(ENKQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/64	
(ENYZ-K)	3D8:10/64	
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
EAC	3D13:16/79	
(SC22)	3D3:22/112	
RESFL	2D7:6/32	DORLF & $\overline{CPR}$ & $\overline{EXEC}$
EAZ-L	3F33:3/72	
$\overline{EQAQ}$-N	3E1:2/83	$\overline{RESFL}$ & MNIPM
EQRX-N	3E1:7/83	
EQYZ-N	3E1:16/83	
EQ-N	3E1:8/83	
EV13	2A18:5/16	MNIPM & CSM & EV13
BKGWT	Page 62	
V15		
$\overline{GBKALL}$	3F6:21/61	$\overline{CSM}$ & MNIPM
ESC22	3E4:26/98	MNIPM
GDLA	3F31:18/74	
V15		
(EN-SAD)	2E11:3/93	See Comments
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3F7:4/62	
(EBYZ-K)	3F7:25/62	
(ED-L:1)	3E21:25/75	MNIPM & $\overline{CPR}$ & $\overline{EXEC}$
(ED-L:2)	3E21:22/75	
(SC22)	3D3:22/112	MNIPM
EQAQ-N	3E1:2/83	MNIPM & $\overline{RESFL}$
EQRX-N	3E1:7/83	
EQYZ-N	3E1:16/83	
EQ-N	3E1:8/83	
EV16	2A9:9/20	MNIPM
ENKALL	3F8:7/64	
EENKQB	Page 64	
GALALL	3D10:3/70	
ESC22	3E4:26/98	
V16		
(EN-SAD)	2E11:3/93	EV17 & $\overline{CSM}$
(ENAJ-K)	3D8:25/64	
(ENKQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/64	
(ENYZ-K)	3D8:10/64	
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
(SC22)	3D3:22/112	
EAC	3D13:16/79	
$\overline{EQAQ}$-N	3E1:2/83	
EQRX-N	3E1:7/83	
EQYZ-N	3E1:16/83	
EQ-N	3E1:8/83	
EV17	2A10:3/21	$\overline{RESFL}$
$\overline{GBKALL}$	3F6:21/61	EV17 & $\overline{CSM}$
GDLA	3F31:18/74	
ESC22	3E4:26/98	
V17		
(EN-SAD)	2E11:3/93	$\overline{CSM}$
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3E7:4/62	
(EBYZ-K)	3F7:25/62	
(ED-L:1)	3E21:25/75	$\overline{CPR}$ & $\overline{EXEC}$
(ED-L:2)	3E21:22/75	
(SC22)	3D3:22/112	
EQAQ-A	3F29:23/81	$RESFL_V$
$\overline{EQAQ}$-N	3E1:2/83	
EQRX-N	3E1:7/83	INTMOVE
EQYZ-N	3E1:8/83	
EQ-N	3E1:8/83	
RESFL	2D7:6/32	DORLF & $\overline{CPR}$ & $\overline{EXEC}$
EM-LS3	3E19:3/91	
SHXOP	2E17:21/94	

EVR	2A17:5/7	$\overline{RESFL}$
EESIN-B	2E17:2/94	
FLALL	3F32:18/76	I116
EENARX-L	3E33:20/102	



COMMENTS	VR / SIGNAL	MP	CONDITIONS
	(EN-SAD)	2E11:3/93	
	(ESIN-B)	6D4:21/248	$\overline{HXOP}$ v(SHXOP & $\overline{K<8}$)
	(READ)	2E4:12/162	
	E1S3-XJ	2F19:6/91	HXOP
	EHX-B	3F14:18/87	
	(EC'AX-K)	3E10:10/67	
	(PLUS 1)	3D24:8/109	$\overline{FLG3}$
	EQCALL	3E17:9/85	
	EQAX-C	3E17:12/85	$\overline{RESFL}$
	EQZ-C	3E17:16/85	
The sequence branches at this point, and dependent upon whether a 116 or 126 instruction is being serviced, VR (Sheet 5) or VR (Sheet 4) is entered.	RESFL	2D7:6/32	DORLF & $\overline{CPR}$ $\overline{EXEC}$
	EM-LS3	3E19:3/91	
	EV18	3B12:23/23	
	FLALL	3F32:18/76	1126
	EENARX-L	3E33:20/102	
VR: (I126) - The first word to be transferred is read to B from the first origin address (in N). On the first cycle of the loop, the first destination address is gated via the mill to set LS3 and then strobed to B. On the second (and subsequent) cycles, the destination address is incremented (as FLAG3 is reset by this time) and HXOP is reset when LS3 = 7.	V18		
	(EPAJ-K)	3E9:3/66	
	(EAAQ-L)	3F33:25/72	
	(EAAQ-L*)	3F33:23/72	
	(EAR-L)	3F33:21/72	
	(EASX-L)	3F33:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	1126
	(ENAAQ-L)	3C14:7/167	
	(ENARX-L)	3D31:5/73	
	(ENAYZ-L)	3D31:25/73	
	EQAZ-P	3F3:18/84	
	(PCHECK)	3D15:17/112	
	EVW	2B3:18/3	
	EEC-SAD	2F6:18/92	$\overline{HXOP}$
	EEB-SO	2F7:17/106	$\overline{FLG1}$
	ENKALL	3F8:7/64	
	EENKQ-K	Page 64	
	VW		
	EC-SAD)	3C14:8/167	$\overline{HXOP}$
	(WRITE)	2E4:6/162	$\overline{FLG1}$
	(EB-SO)	3E21:9/75	
	E1S3-XJ	2F19:6/91	HXOP
	EBAZ-X	3F25:8/90	
	(ENAJ-K)	3D8:25/61	
	(ENKQ-K)	3D8:23/61	
	(ENRX-K)	3D8:17/61	
	(ENYZ-K)	3D8:10/61	
	(PLUS 1)	3D24:8/109	
	(EQAZ-A)	3F29:23/81	
	EQAQ-N	3E1:2/83	
	EQRX-N	3E1:7/83	
	EQYZ-N	3E1:16/83	
	EQ N	3E1:8/83	
	EM-LS3	3E19:3/91	
	RST FLG1	3C31:10/150	LS3 = 7
VW: The origin word is written to the destination address in C (for the store) or LS3 (for an accumulator). The origin address in N is incremented in the mill by PLUS 1 and strobed to A and N. When LS3 = 7, FLAG1 is reset. LS3 is reloaded from mill bits 0-2. The count is tested and if not equal to zero (i.e. P ≠ 0) the three beats (VR-VW) are repeated when P = 0, VR10 is entered. Each loop contained a hesitation break-point and a real time interrupt break-point.	EVR	2A17:5/7	$\overline{P0}$ & $\overline{HR}$ & $\overline{RTI}$
	EVR10	3A14:22/39	P = 0



Read current instruction address from store location 10.

Increment instruction address and strobe to C. Reset INTMOVE and FLAG1 bistables and clear carry.

Exit for 126 instruction.

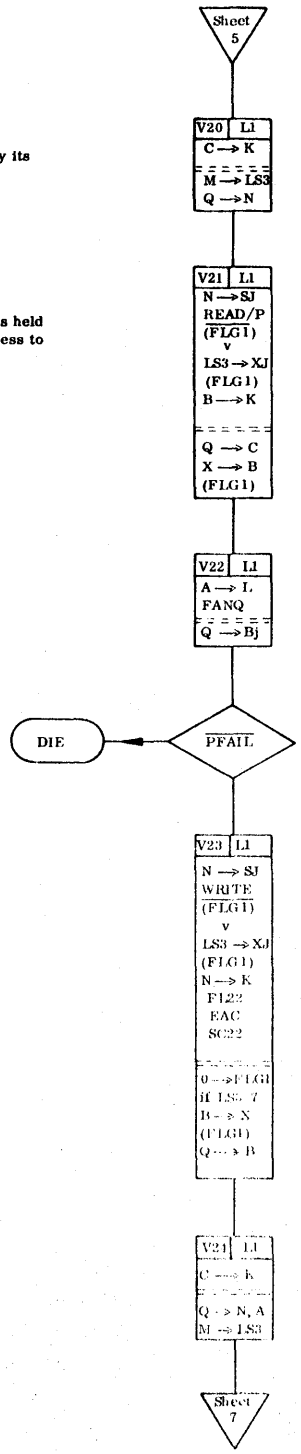
Read word n from store (or an accumulator) to register B. Decrement count and return it to P. Reset HXOP if LS3 = 7.

Strobe one character from B to A.

Increment character address and strobe to B.

COMMENTS
VR10: The current instruction address (and overflow) are retrieved from store location 10 and read to B.
V27: The instruction address read in VR10 is incremented and strobed to C, the INTMOVE and FLG1 bistables being reset (if not already reset). Carry is cleared and exit is made from the 126 sequence to the Instruction Phase for the next order.
VR: For the 116 instruction, the word n is read to B from the address held in N (or LS3). The count (in P_{0-8}) is decremented and HXOP reset if LS3 = 7, (i.e. if the origin address is not held in an accumulator). The FLAG2 bistable is reset.
V18: The character of the origin word read in VR (as designated by N_{22-23}) is strobed to bits 0-5 of A.
V19: Character address is incremented and strobed to B so that the next most significant character position will be selected in V22.

VR10 SIGNAL	MP	CONDITIONS
(FSAD10)	2F10:9/112	
FRCE1	2F3:3/115	
FRCE3	2F3:6/115	
(READ)	2E4:12/162	
(ESIN-B)	6D4:21/248	
EV27	3B18:12/29	
ESC22	3E4:26/98	
GBKALL	3F6:21/62	
V27		
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3E7:4/62	
(EBYZ-K)	3F7:25/62	
(PLUS 1)	3D24:8/109	
(SC22)	3D3:22/112	
CCY	3F12:18/99	
EQAX-C	3E17:12/85	
EQZ-C	3E17:16/85	
RSTFLG1	3C31:10/150	
(PCHECK)	3D15:17/112	
EOI	2A16:15/41	
VR		
(EN-SAD)	2E11:3/93	$\overline{HXOP}$ v (SHXOP & K < 8)
(READ)	2E4:12/162	
(ESIN-B)	6D4:21/248	
ELS3-XJ	2F19:6/91	HXOP v SHXOP & K < 8
EHX-B	3F14:18/87	
(EPAJ-K)	3E9:3/66	
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
(ENAAQ-L)	3C14:7/16	
(ENARX-L)	3D31:5/73	
(ENAYZ-L)	3D31:25/73	
EQAZ-P)	3F3:18/84	
EV18	3B12:22/23	
EEBJ-K	3D7:17/71	
V18		
(EBL-K)	3E21:17/70	
EQAZ-A	3F29:23/81	
EV19	2A11:9/24	
ENEALL	3F8:7/64	
ELSEQ-K	Page 64	
ESC22	3E4:26/98	
V19		
(ENAJ-K)	3D8:25/64	
(ENQQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/64	
(ENYZ-K)	3D8:10/64	
FL22	3F25:2/90	
(EAC)	3D13:16/79	
(SC22)	3D3:22/112	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
EQ-B	3D13:15/79	
EV20	2B13:18/25	
GCKALL		



Gate destination address to N and copy its l. s. 3 bits to LS3.

Read store (or accumulator) at address held in N (MLS3) and store this origin address to C.

Gate on character to B

Write the character selected in V22 to store (or to an accumulator). Increment destination address and strobe to B. Reset Flag 1 if LS3 = 7.

Gate origin address to N and A and load LS3.

COMMENTS

V20: The destination address in C is gated via the mill (setting LS3) to N.

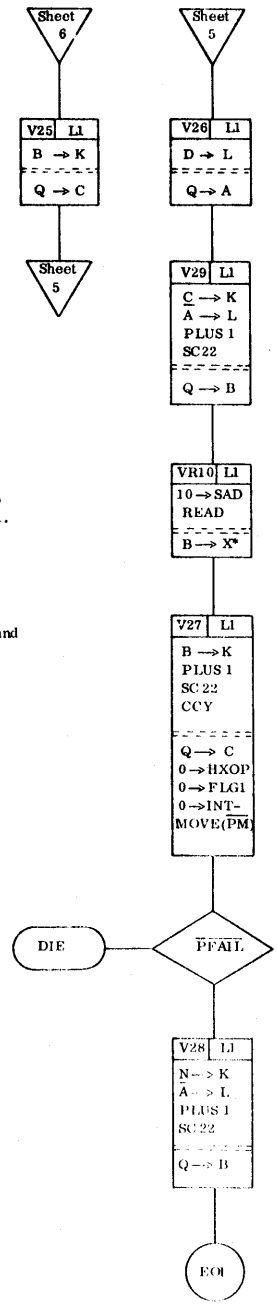
V21: A read/pause (or accumulator) cycle is initiated and the origin address in B is strobed to C, leaving the former register clear for the word from the destination address.

V22: The character placed in A in V18 is fanned onto the Q highway and is then strobed into one character position of B.

V23: The character copied into B in V22 is written to store (or to an accumulator). The destination address in N22 - 23 is incremented and strobed to B. Flag 1 is reset if LS3 = 7.

V24: The origin address (in C) is gated via the mill, setting LS3, to A and N.

V20 / SIGNAL	M.P.	CONDITIONS
(ECAX-K)	3E10:10/67	
(ECY-K)	3F10:25/67	
(ECZ-K)	3F10:19/67	
$\overline{\text{EQAQ-N}}$	3E1:2/83	
EQRX-N	3E1:7/83	
EQYZ-N	3E1:16/83	
EQ-N	3E1:8/83	
EM-LS3	3E19:3/91	
EV21	3B14:26/26	
$\overline{\text{EESIN-B}}$	2E17:2/94	$\overline{\text{FLG1}}$
$\overline{\text{GBKALL}}$	3F6:21/61	
V21		
(EN-SAD)	2E11:3/93	$\overline{\text{FLG1}}$
(READ)	2E4:12/162	
(ESIN-B)	6D4:21/284	$\overline{\text{FLG1}}$
(PAUSE)	2E10:7/143	$\overline{\text{FLG1}}$
ELS3-XJ	3F19:6/91	
EHX-B	3F14:18/87	
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3E21:15/62	
(EBNP-K)	3F7:24/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3E7:4/62	
(EBYZ-K)	3F7:25/62	
EQCALL	3F17:2/85	
EQAX-C	3E17:12/85	
EQZ-C	3E17:16/85	
EV22	3B14:25/27	
GALALL	3D30:3/70	
V22		
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
EMFAN	3F28:17/107	
EQ-BJ	3E18:19/80	
(PCHECK)	3D15:17/112	
EV23	2A13:8/9	
EEB-SO	2F7:17/106	$\overline{\text{FLG1}}$
ENKALL	3F8:7/64	
ESC22	3E4:25/98	
V23		
(EN-SAD)	2E11:3/93	$\overline{\text{FLG1}}$
(WRITE)	2E3:6/162	
(EB-SO)	3E21:9/75	
ELS3-XJ	3F19:6/91	$\overline{\text{FLG1}}$
EBAZ-X	3F20:8/90	
(ENAJ-K)	3D8:25/61	
(ENKQ-K)	3D8:23/61	
(ENRX-K)	3D8:17/64	
(ENYZ-K)	3D8:10/61	
(F122)	3F25:2/50	
(EAC)	3D13:16/79	
(SC22)	3D3:22/112	
$\overline{\text{EQBJP}}$	2D17:7/48	
$\overline{\text{EQAJ-B}}$	3D13:21/79	
$\overline{\text{EQRM-B}}$	3D13:22/79	
$\overline{\text{EQNQ-B}}$	3D13:24/79	
$\overline{\text{EQBZ-B}}$	3D13:23/79	
EQ-B	3D13:15/79	
RSTFLG1	3C31:D/150	
EV24	3B16:10/28	
V24		
(ECAX-K)	3E10:10/67	
(ECY-K)	3F10:25/67	
(ECZ-K)	3F10:19/67	
$\overline{\text{EQAQ-N}}$	3E1:2/83	
EQRX-N	3E1:7/83	
EQYZ-N	3E1:16/83	
EQ-N	3E1:8/83	
EQAZ-A	3F29:23/81	
EM-LS3	3E19:3/91	
EV25	3B17:21/29	
$\overline{\text{GBKALL}}$	3F6:21/61	



Gate destination address to C and return to VR (sheet 5).

Gate datum to A register.

Subtract datum from destination address (in C) and strobe the absolute address to B.

Read (dumped) current instruction address from store location 10. I mp absolute address formed in V29 to X + 1.

Increment current instruction address and strobe to C. Reset HXOP, FLAG1 and INTMOVE ($\overline{PM}$) bistables.

Transfer final origin (plus ¼) address to B.

Exit to Instruction Phase.

V25: The destination address (together with its incremented character address) is strobed from B to C. The loop is then recycled by entry to VR (sheet 5) until P = 0 or FLG1 is reset.

V26: The datum is copied into the A register for subtraction in the next beat.

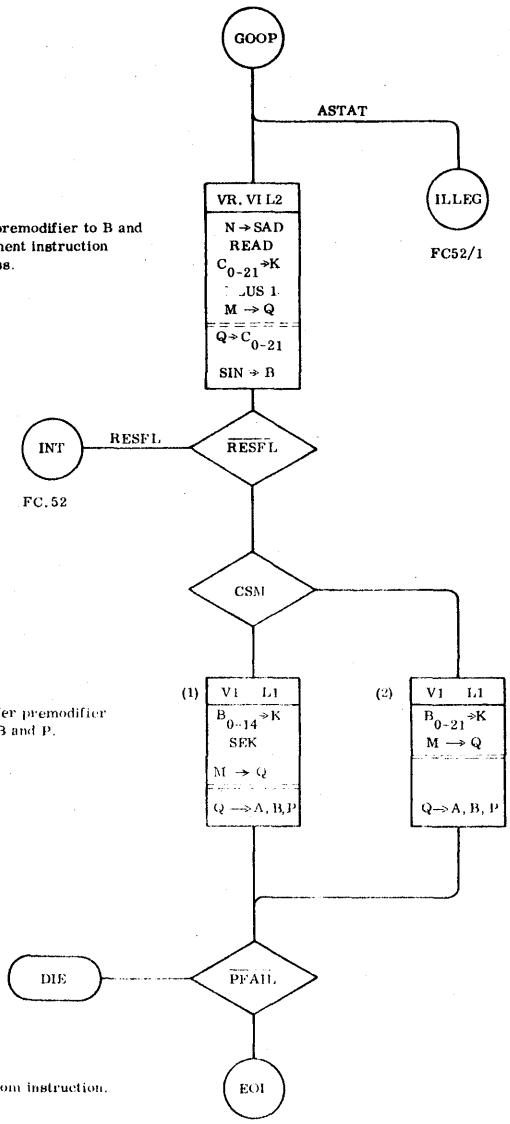
V29: The absolute destination address is formed by gating the inverse of the datum ($\overline{A}$) to the mill along with the datumised address and PLUS 1. The result of the subtraction is placed in register B.

VR10: The current instruction address is read from its dump location in store location 10. During this read store cycle, the absolute address formed in V29 is dumped to X + 1.

V27: The current instruction address (in B from VR10) is incremented and placed in C. HXOP, FLG1 and INTMOVE (if $\overline{PM}$) are all reset.

V28: The N register now contains the last origin address + ¼ - i.e. what would have been the next origin address if the transfer has been one word longer. The datum (in A from V26) is subtracted from the datumised address to give the absolute address which is strobed to accumulator X in the next Instruction Phase.

COMMENTS	V25 SIGNAL	M.P.	CONDITIONS
	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3F7:24/62	
	(EBNP-K)	3E7:2/62	
	(EBQ-K)	3F7:23/62	
	(EBRX-K)	3E7:4/62	
	(EBYZ-K)	3F7:25/62	
	EQCALL	3F17:2/85	
	EQAX-C	3F17:12/85	
	EQZ-C	3E17:16/85	
	EVR	2A17:5,7	$\overline{HR}$ & $\overline{RT}$ & ($\overline{P=0}$ v FLG2)
	EV26	3A23:21/37	P=0 v $\overline{FLG2}$
	GDLA	3F31:18/74	EV26
	EESIN-B	2E17:2/97	EVR & $\overline{HXOP}$
	V26		
	ECY-K	3F10:25/67	
	(ED-L:1)	3E21:25/75	CPR & EXEC
	(ED-L:2)	3E21:22/75	
	EQAZ-A	3F29:23/81	
	EV29		
	FLAX	3D29:25/113	
	ESC22	3E4:25/98	
	VR10		
	(FSAD10)	2F10:9/112	
	(ESIN-B)	6D4:21/248	
	(READ)	2E4:12/162	
	EBAZ-X*	2F25:6/90	
	EV27	3B18:12/29	
	GBKALL	3F6:21/61	
	ESC22	3E4:25/98	
	V27		
	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3F7:24/62	
	(EBNP-K)	3E7:2/62	
	(EBQ-K)	3F7:23/62	
	(EBRX-K)	3E7:7/62	
	(EBYZ-K)	3F7:25/62	
	(PLUS 1)	3D24:8/109	
	(SC22)	3D3:22/112	
	CCY	3F12:18/99	
	EQAX-C	3E17:12/85	
	EQZ-C	3E17:16/85	
	RSTFLG1	3C31:10/150	
	EV28	2C11:17/43	
	ESC22	3E4:25/98	
	ENKALL	3F8:7/64	1 1 16
	$\overline{ENALALL}$	3D31:7/73	
	EENARX-L	3E33:20/102	
	V28		
	(ENAJ-K)	3D8:25/64	1 1 16
	(ENKQ-K)	3D8:23/67	
	(ENRX-K)	3D8:17/65	
	(ENYZ-K)	3D8:10/67	
	(ENAAQ-L)	3C11:7/165	
	(ENARX-L)	3D31:25/73	
	(ENAYZ-L)	3D31:25/73	
	(PLUS 1)	3D27:8/109	
	(SC22)	3D3:22/112	
	$\overline{EQAJ-B}$	3D13:21/79	
	$\overline{EQKM-B}$	3D13:22/79	
	$\overline{EQNQ-B}$	3D13:24/79	
	$\overline{EQYZ-B}$	3D13:23/79	
	EQ-B	3D18:15/79	
	EOI	2A16:15/41	
	V29		
	(ECAX-K)	3E10:10/67	
	(ECY-K)	3F10:25/67	
	(ECZ-K)	3F10:19/67	
	(EAAQ-L)	3F33:25/72	
	(EAAQ-L*)	3F33:23/72	
	(EAR-L)	3F33:21/72	
	(EASX-L)	3F33:7/72	
	(PLUS 1)	3D24:8/109	
	(SC22)	3D3:22/112	
	EQBIP	2D17:7/78	
	$\overline{EQAJ-B}$	3D13:21/79	
	$\overline{EQKM-B}$	3D13:22/79	
	$\overline{EQNQ-B}$	3D13:24/79	
	$\overline{EQRZ-B}$	3D13:23/79	
	EQ-B	3D13:15/79	
	EVR10	3A14:22/39	
	EESIN-B	2E17:2/94	



Read premodifier to B and increment instruction address.

Transfer premodifier to A, B and P.

Exit from instruction.

COMMENTS

Relevant signals active in previous beat:
GPA, EVR, EVI, EESIN-B, I117.

VR. VI: The premodifier (n), which may be 15 or 22 bits, depending on the current store mode, is read to B from store. The current instruction address is incremented in the mill (PLUS 1 forces data flow CYB0) and restored to C (bits 0-21).

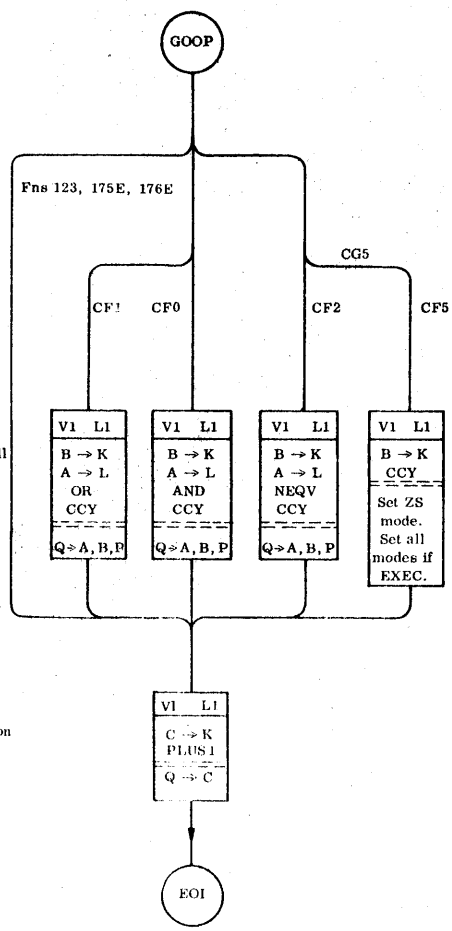
V1:

1) In CSM the premod. is 15-bits (in B_{0-14}) and must be expanded to 22 bits by extending the sign bit (B14) the required number of places (SEK). This is accomplished when the premod. is gated onto K, as SEK makes K_{15-21} all 1's if B14 = 1.

2) The 22-bit premodifier in ESM is transferred directly to the A, B and P registers.

EOI: The A bistable is set (ASTAT) to ensure that the second of two successive 117 instructions goes illegal. An involuntary entry to Executive is then made (via the interrupt sequence) at GOOP if the next instruction is a 117.

VR.VI / SIGNAL	MP	CONDITIONS
(EN-SAD)	2E11:3/93	
(ESIN-B)	6D4:21/248	
(READ)	2E4:12/162	
(ECAX-K)	3E10:10/67	
(PLUS 1)	3D24:8/109	
ELS3-XJ	3F19:6/91	HXOP
EM-Q	3C14:23/167	
EQAX-C	3E17:12/85	$\overline{\text{RESFL}}$
EHX-B	3F14:18/87	HXOP
RESFL	2D7:6/32	DORLF. $\overline{\text{CPR}}$. $\overline{\text{EXEC}}$
EVI	3A16:12/8	$\overline{\text{RESFL}}$
VI	3B28:21/52	EVI
V1		
(PCHECK)	3D15:17/112	
EBAJ-K	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3E7:4/62	$\overline{\text{CSM}}$
(SEK)	3E23:6/111	CSM. HB14*
PFAIL	6A6:21/21	PGEN = RB24
DIE	3B33:25/44	PFAIL. PCHECK $\overline{\text{INHPFL}}$.
EM-Q	3C14:23/167	
EQAZ-A	3F29:23/81	
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
EQAZ-P	3F3:18/84	
EOI	2A16:15/41	

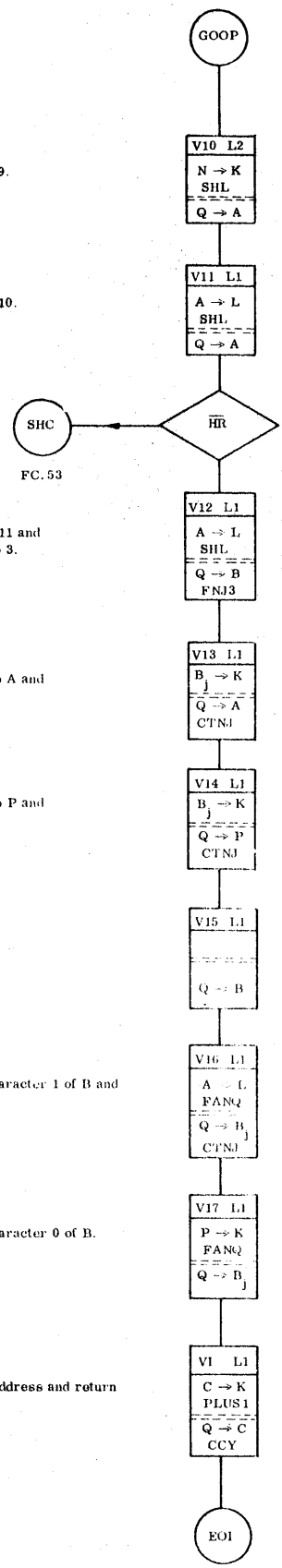


Gate operands to mill and perform logical operation.

Increment instruction address.

Exit.

COMMENTS	VI SIGNAL	M.P.	CONDITIONS
Also active at entry will be: **GPD, EV1, I120-2 or I125, GBKALL., GALALL., ($\overline{I125}$), EOR_V, $EAND_V$ ENEQV, and LITERAL.**			
	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3F7:24/62	
	(EBNP-K)	3E7:2/62	
	(EBQ-K)	3F7:23/62	
	(EBRX-K)	3E7:4/62	
	(EBYZ-K)	3F7:25/62	
	(EAAQ-L)	3F33:25/72	I120-2
	(EAAQ-L)	3F33:23/72	
	(EAAQ-L*)	3F33:23/72	
	(EAR-L)	3F33:21/72	
	(EASX-L)	3F33:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	(AND)	3E21:6/75	CF0
	(OR)	3D3:11/112	CF1
	(NEQV)	3E21:12/75	CF2
	(ZS)	2C6:23/153	I 125
	EDFG	3F16:12/86	I125 & EXEC
	CCY	3F12:18/99	
	EQAZ-A	3F29:23/81	
	EQAZ-P	3F3:18/84	
	V1		
V1: As these instructions are literals, the operand N will be in B from the Instruction Phase and A will hold x. N and x are gated to the mill for a logical AND, OR, or NONEQUIVALENCE operation and the result is strobed to registers A, B and P. For the 125, the ZS bistable is set from Q0 in normal mode and the G register (bits 3-5) is loaded from Q_{3-5} in Executive mode. Carry is cleared in both cases.	$\overline{EQAJ-B}$	3D13:21/79	
	$\overline{EQKM-B}$	3D13:22/79	
	$\overline{EQNQ-B}$	3D13:24/79	
	$\overline{EQRZ-B}$	3D13:22/79	
	EQ-B	3D13:15/79	
	EVI	3A16:12/8	
	VI		
VI: The instruction address is incremented by one and returned to C.	(ECAX-X)	3E10:10/67	
	(PLUS 1)	3D24:8/109	$\overline{MAN}$
	EQAX-C	3E17:12/85	
	EOI	2A16:15/41	
EOI: In beat V0 of the Instruction Phase, the content of B is written to accumulator X.			



Gate count to A, bits 1-9.

Gate count to A, bits 2-10.

Gate count to B, bits 3-11 and force character count to 3.

Gate character 3 of B to A and decrement count to 2.

Gate character 2 of B to P and decrement count to 1.

Clear B.

Gate bits 0-5 of A to character 1 of B and decrement count to 0.

Gate bits 0-5 of P to character 0 of B.

Increment instruction address and return to C.

Exit.

COMMENTS	V10 / SIGNAL	M.P.	CONDITIONS
Also active at entry will be I124 and EV10.			
	(ENAJ-K)	3D8:25/64	
	SHL	3D33:8/102	
	EQAZ-A	3F29:23/81	
	GALALL	3D30:3/70	
	EV11	2A6:16/14	
	V11		
V10: The count (x_c) is in N (bits 0 to 8) from the Instruction Phase and is shifted one place left into A, bits 1 to 9.	(EAAQ-L)	3F33:25/72	
	(EAAQ-L*)	3F33:23/72	
	(EAR-L)	3F33:21/72	
	(EASX-L)	3F33:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	SHL	3D33:8/102	
	EQAZ-A	3F29:23/81	
V11: The count is again shifted one place left and returned to A, bits 2 to 10.	HESBKPT	2B15:25/47	
	EVH2	2C14:13/45	HR & $\overline{\text{HES3}}$
	EV12	3B11:10/15	$\overline{\text{EVH2}}$
	GALALL	3D30:3/70	EV12
	V12		
A hesitation break-point is now allowed.			
	(EAAQ-L)	3F33:25/72	
	(EAAQ-L*)	3F33:23/72	
	(EAR-L)	3F33:21/72	
	(EASX-L)	3F33:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	SHL	3D33:8/102	
	EQAJ-B	3D13:21/79	
	EQKM-B	3D13:22/79	
	EQNQ-B	3D12:24/79	
	EQRZ-B	2D13:23/79	
	EQ-B	3D13:15/79	
V12: A third shift left of one place occurs putting the count in B, bits 3 to 11. The character registers NCH (bits 22 & 23 of N) is forced to 3.	FNJ3	3D18:5/140	
	EEBJ-K	3D7:17/71	
	EV13	2A18:5/16	
	V13		
V13: The l.s. character (3) of B (bits 0-5) is placed in the l.s. 6 bits of A and NCH again decremented by 1.			
	(EBJ-K)	3E21:17/75	
	EQAZ-A	3F29:23/81	
	CTNJ	3D14:8/104	
	EEBJ-K	3D7:17/71	
	EV14	2A7:9/18	
	V14		
V14: Character 2 of B (bits 6-11) is placed in the l.s. 6 bits of P and NCH again decremented by 1.			
	(EBJ-K)	3E21:17/75	
	EQAZ-P	3F3:18/84	
	CTNJ	3D14:8/104	
	EV15	2A8:9/19	
	V15		
V15: B is cleared to ensure that bits 0-14 (x_m) will be zero.			
	EQAJ-B	3D13:21/79	
	EQKM-B	3D13:22/79	
	EQNQ-B	3D13:24/79	
	EQRZ-B	3D13:23/79	
	EQ-B	3D13:15/79	
	GALALL	3D30:3/70	
	EV16	2A9:9/20	
	V16		
V16: Count bits 0-2 are now in bits 3-5 of A. Bits 0-5 of A are therefore strobed to character 1 of B. This puts count bits 0-2 in B15-17. NCH is decremented to zero.			
	(EAAQ-L)	3F33:25/72	
	(EAAQ-L*)	3F33:23/72	
	(EAR-L)	3F33:21/72	
	(EASX-L)	3F33:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	EMFAN	3F28:14/107	
	EQ-BJ	3E18:19/80	
	CTNJ	3D14:8/104	
V17: Count bits 3-8 (in P_{0-5}) are fanned to Q and strobed to character position 0 (bits 18-23) of B. At this time, B_{15-23} holds the count x_c abd B_{0-14} is all zero (x_m).	EPKALL	Page 66	
	EV17	2A10:3/21	
	V17		
VI: The instruction address is incremented by 1 and returned to C.			
	(EPAJ-K)	3E9:3/66	
	(EPKQ-K)	3E9:5/66	
	(EPRX-K)	3E9:5/66	
	(EPYZ-K)	3E9:23/66	
	EMFAN	3F28:17/107	
	EQ-BJ	3E18:19/80	
	EVI	3A16:12/8	
	VI		
The content of register B is strobed to accumulator X in VQ of the Instruction Phase.	(EXAX-K)	3E10:10/67	
	(PLUS 1)	3D24:8/109	
	$\overline{\text{EQAX-C}}$	3E17:4/85	
	CCY	3F12:18/99	
	EOI	2A16:15/41	

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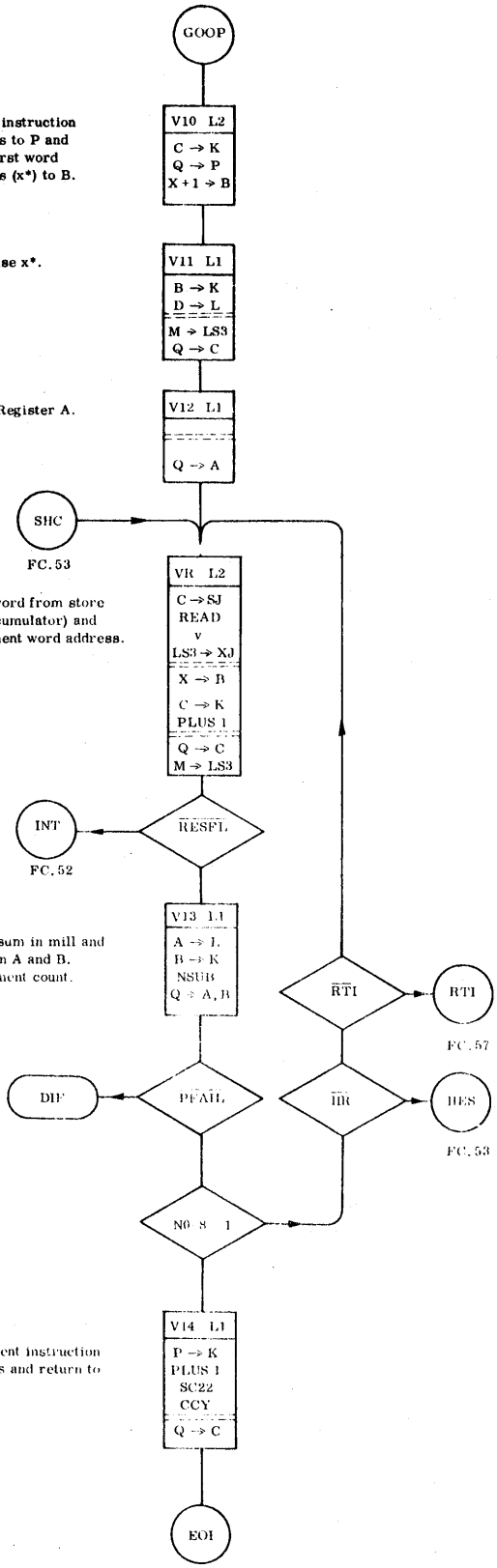
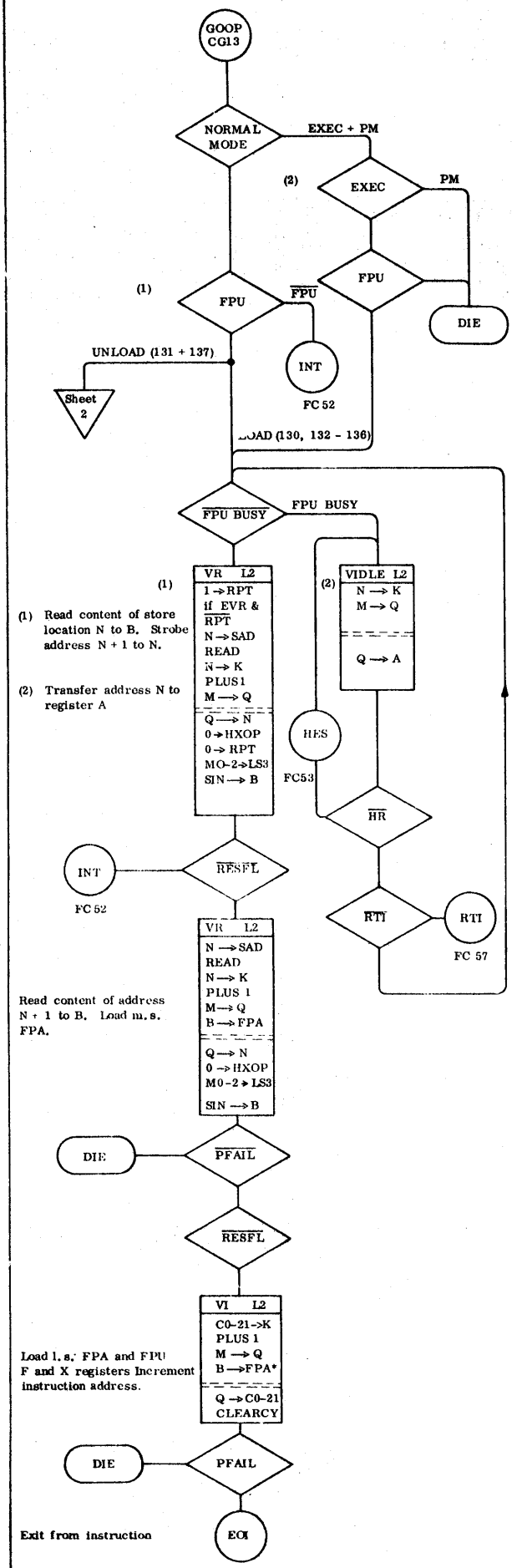


COMMENTS
Also active at entry will be: GCKALL, EV10, FOV (if RN23), ECKALL, MVSUM (if OV set), I127 and I127INT.
V10: V11I127 is active only while EV11 is active (i.e. during V10).
VR: If the address is <8, an accumulator is read, otherwise a store location is accessed. EM-LS3 loads Register LS3 from the mill (bits 0-2) to give the accumulator address (if needed).
V13: NSUB is active to decrement Ns (N_{0-9}) by 1.
If RTI is active, it will inhibit certain types of hesitation request.
HESBKPT is also active at exit and hesitations are allowed. If there are more (or after they have been serviced), the Instruction Phase is entered, at EOI.

VIO / SIGNAL	MP	CONDITIONS
(ECAX-K)	3E10:10/67	
(ECY-K)	3F10:25/67	
(ECZ-K)	3F10:19/67	
EQAZ-P	3F3:18/84	
EHX*-B	3F18:16/80	
EV11	2A6:16/14	
V11I127	Sheet 74	
EEBKM-K	Sheet 62	
GD1A	3F31:18/74	
V12		
EQAZ-A	3F29:23/81	
HXOP	3C26:23/160	K<8
EVR	2A17:5/7	
EEC-SAD	2F6:18/92	
GCKALL	Sheet 67	
EESIN-B	2E17:2/94	$\overline{\text{HXOP}}$
V11		
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3E7:4/62	$\overline{\text{CSM}}$
(EBYZ-K)	3F7:25/62	
(ED-L:1)	3E1:25/75	$\overline{\text{EXEC}}$ & $\overline{\text{CPR}}$
(ED-L:2)	3E21:22/75	
EQAZ-C	Sheet 85	
EMLS3	3E19:4/91	
SHXOP	2E17:21/94	M<8
EV12	3B11:10/15	
VR		
(EC-SAD)	3C14:8/67	
(READ)	2E4:12/162	
(ESIN-B)	6D4:21/248	$\overline{\text{HXOP}}$
RESFL	2D7:6/32	IORLF & $\overline{\text{CPR}}$
EMLS3	3E19:4/91	& $\overline{\text{EXEC}}$
ELS3-XJ	3F19:6/91	IXOP
EHX-B	3E14:6/87	
(ECAX-K)	3E10:10/67	
(ECY-K)	3F10:25/67	
(ECZ-K)	3F10:19/67	
(PLUS 1)	3D24:8/109	
EQCALL	3F17:2/85	$\overline{\text{RESFL}}$
EQAX-C	3E17:12/85	
EQZ-C	3E17:16/85	
(HXOP)	3C26:23/10	M<8
EV13	2A18:5/16	$\overline{\text{RESFL}}$
GALALL	3D30:3/10	EV13
GBKALL	3F6:21/61	
EEBKM-K	Sheet 62	
EV33	3B20:20/33	RESFL
V13		
(PCHECK)	3D15:17/12	
(EAAQ-L)	3F35:25/72	
(EAAQ-L')	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3E7:4/62	
(EBYZ-K)	3F7:25/62	
NSUB	3F18:21/80	
EQAZ-A	3F29:23/81	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:21/79	
EQRZ-B	3D13:23/79	
EQ-B	3D13:15/79	
EPKALL	Page 66	EV14
ESC22	3E4:25/98	
EV14	2A7:9/18	$N_{0-8} = 1$
HESBKPT	2B15:25/17	$\overline{N_{0-8}} = 1$
EVR	2A17:5/7	$\overline{N_{0-8}} = 1$ & $\overline{\text{HR}}$ & $\overline{\text{RTI}}$
EVH1	2C14:12/45	HESBKPT & HR & HES3
EVL2	2C14:13/45	HESBKPT & HR & $\overline{\text{HES3}}$
EV17	2A10:3/21	RTI & $\overline{\text{HR}}$
V14		
(EPAJ-K)	3E9:3/66	
(EPKQ-K)	3E9:5/66	
(EPRX-K)	3E9:25/66	
(EPYZ-K)	3E9:23/66	
(PLUS 1)	3D24:8/109	$\overline{\text{MAN}}$
(SC22)	3D3:22/112	
EQCALL	3F17:2/85	
EQAX-C	3E17:12/85	
EQZ-C	3E17:16/85	
C → J	3F12:16/99	
EOI	2A16:15/41	

ISSUE	1 Nov. 72								
ICL	1904A MK II 1904S 1903T	127 INSTRUCTION (GOOP-EOI)						FC 36 SHEET 1 OF 1	



(1) Read content of store location N to B. Strobe address N + 1 to N.

(2) Transfer address N to register A

Read content of address N + 1 to B. Load m.s. FPA.

Load l.s. FPA and FPU F and X registers Increment instruction address.

Exit from instruction

COMMENTS

Relevant signals active in previous beat: EVR (BUSY), EVIDLE (BUSY), EESIN-B (EVR), ENKALL, EV30 (131 + 137)

(1) If a group 13 instruction is given in normal mode, and a hardware F.P.U. is not fitted the instruction is treated as an extracode. EV34 is forced (for entry to the interrupt sequence) by EXCD. GOOP. EXEC.

Similarly, in Priority mode, EV34 is forced under the same conditions

VIDLE:

The address N is transferred to the A register since the N register is required if subsequent entry is made to the hesitation sequence. VIDLE is cycled repeateadly until either the F.P.U. is free or a RTI occurs.

VR

A second 'READ' beat is produced when RPT initiates EVR during the first 'READ' beat. RPT is resct (by $\overline{FPT}$) at the end of the first 'READ' beat. Since LUFPUB is conditional on $\overline{RPT}$, this ensures that the load FPU operation is not started until the beat following the reading from store of the first (m.s.) word of the operand.

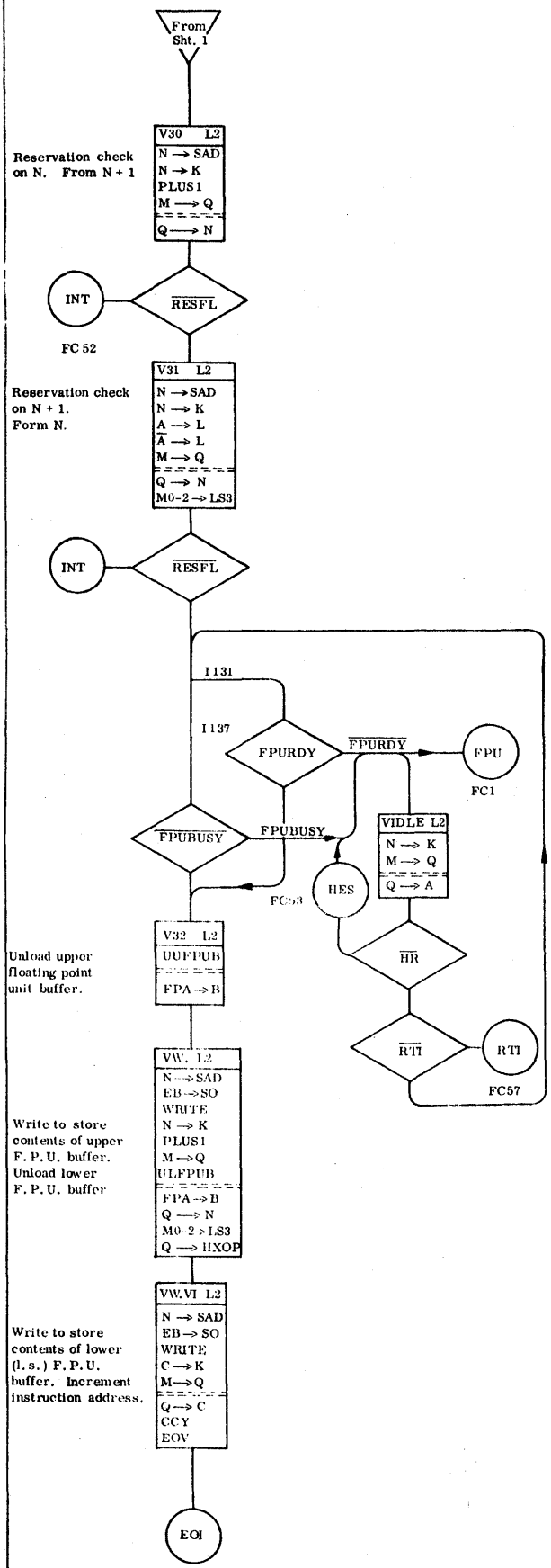
VR

LUFPUB (load upper F.P.U. buffer) produces the strobe in the F.P.U. which loads the m.s. part of the operand from the B register to the F.P.U. Input Buffer.

VI

LLFPUB (load lower F.P.U. buffer) produces the strobe in the F.P.U. which loads the l.s. part of the operand from the B register to the F.P.U. input buffer and starts the F.P.U. clock.

VIDLE SIGNAL	MP	CONDITIONS
(ENAJ-K)	3D8:25/64	
(ENKQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/64	
(ENYZ-K)	3D8:10/64	
EM-Q	3C14:23/167	
EQAZ-A	Sheet 85	
$\overline{EVR}$	2A17:5/7	VRIP
$\overline{VRIP}$	2A14:19/5	I1302-6. $\overline{RTI}$. $\overline{HR}$. $\overline{FPUBUSY}$
EESIN-B	2E17:2/94	EVR. ($\overline{HXOP}$. $\overline{SHXOP}$. K < 8)
ENKALL	Sheet 64	EVR+ EVIDLE
EVIDLE	3A12:2/40	VIDLE. I1302-6. $\overline{FPUBUSY}$. $\overline{RTI}$. $\overline{HR}$
VR		
(ESIN-B)	6D4:21/248	
(EN-SAD)	2E11:3/93	
(READ)	2E19:12/162	
(ENAJ-K)	3D8:25/64	
(ENKQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/64	
(ENYZ-K)	3D8:10/64	
(PLUS 1)	3D24:8/109	
EM-Q	3C14:23/167	
ELS3-XJ	3F19:6/91	HXOP
EHX-B	3E14:6/87	HXOP
EM-LS3	3E19:4/91	
LUFPUB	2E7:2/32	$\overline{RPT}$
EQ-N	3E1:8/83	
EQAQ-N	3E1:2/83	$\overline{RESFL}$
EQRX-N	3E1:6/83	
EQYZ-N	3E1:16/83	
(PCHECK)	3D15:17/112	(VR. RPT)
PFAIL	6A6:21/214	PGEN - RB24
DIE	3B33:25/44	PCHECK. PFAIL. $\overline{INHPFL}$
RESFL	2D7:6/32	DORLF. $\overline{CPR}$. EXEC
EVR	2A17:5/7	RPT. $\overline{RESFL}$
EESIN-B	2E17:2/94	EVR. $\overline{HXOP}$. $\overline{SHXOP}$. K < 8)
$\overline{ENKALL}$	3F8:7/64	EVR
EVI	3A16:12/8	VR. $\overline{RPT}$. $\overline{RESFL}$
VI		
(PCHECK)	3D15:17/112	(VR. $\overline{RPT}$)
(ECAX-K)	3E10:10/67	
(PLUS 1)	3D24:8/109	
PFAIL	6A6:21/214	PGEN - RB24
DIE	3B33:25/44	PCHECK. PFAIL. $\overline{INHPFL}$.
EM-Q	3C14:23/167	
LLFPUB	2E7:22/32	$\overline{VW}$.
EQAX-C	3E17:12/85	$\overline{RESFL}$
CCY	3F12:18/99	
EOI	2A16:15/41	



COMMENTS

V30

A reservation check is carried out on the address in N, which is the destination of the m. s. part of the double length operand to be received from the F. P. U. This address is then incremented by 1 and returned to N.

V31

A reservation check is carried out on N + 1. This address is now decremented by 1, again forming N, and returned to the N register.

If a 131 instruction, the F. P. U. carries out its 'Floating to Fixed' conversion and on completion of this operation initiates "FPURDY". The instruction now re-enters the main micro-program and completes the final three beats of the sequence.

VIDLE

See Sheet 1.

V32

The m. s. word of the double length operand is transferred from the F. P. U. to the B register.

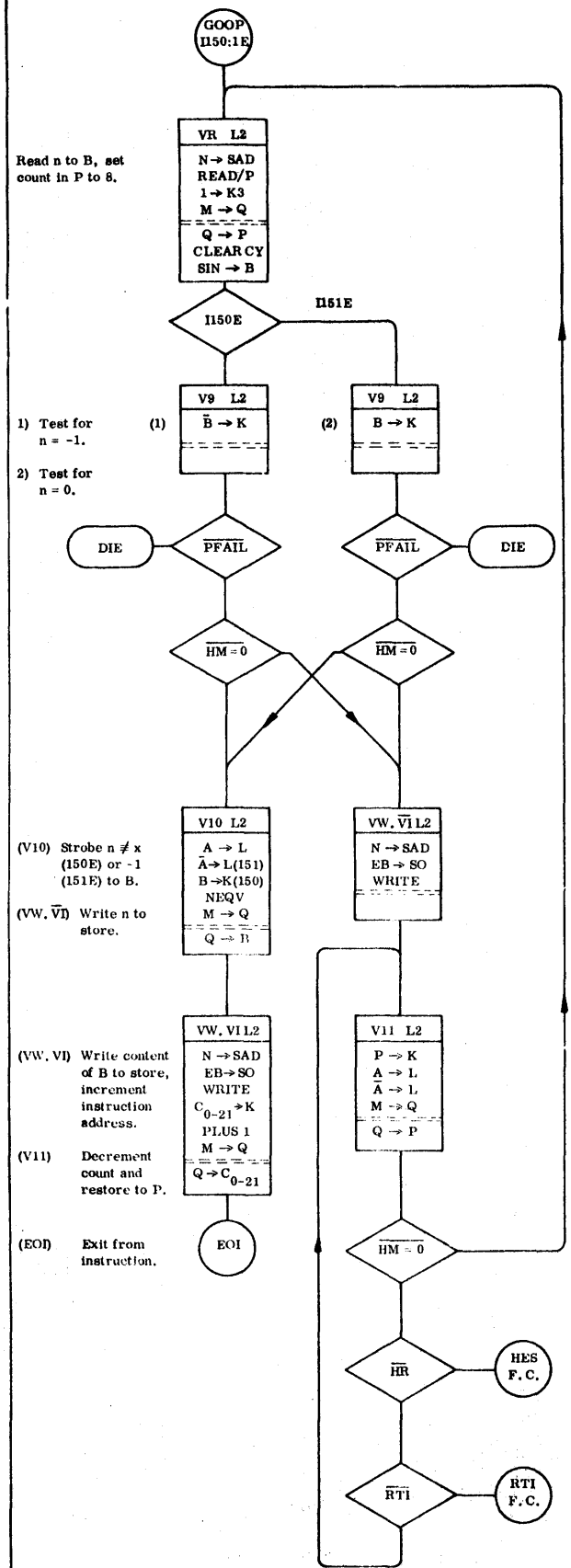
VW, VI

The store is addressed from the N register, the m. s. word of the double length operand is written to store, the N register's contents are incremented by 1 and the l. s. word of the operand gated from the F. P. U.

VW, VI

The store is addressed from the N register and the l. s. word of the double length operand written to store. The current instruction address is incremented, carry is cleared and, if B23 is set (indicating exponent overflow), the overflow bistable is force set.

V30 SIGNAL	M.P.	CONDITIONS
(EN-SAD)	2E11:3/93	
(ENAJ-K)	3D8:25/64	
(ENKQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/64	
(ENYZ-K)	3D8:10/64	
(PLUS 1)	3D24:8/109	
EM-Q	3C14:23/167	
EQ-N	3E1:8/83	} $\overline{\text{RESFL}}$
EQAQ-N	3E1:2/83	
EQRX-N	3E1:6/83	
EQYZ-N	3E1:16/83	
RESFL	2D7:6/32	DORLF. $\overline{\text{CPR}}$. $\overline{\text{EXEC}}$
EV31	3B19:2/31	$\overline{\text{RESFL}}$
ENKALL	Sheet 64	
FLALL	2E32:6/76	
EENARXL	3E33:19/102	
V31		
(EN-SAD)	2E11:3/93	
(ENAJ-K)	3D8:25/64	
(ENKQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/64	
(ENYZ-K)	3D8:10/64	
(EAAQ-L)	3F33:25/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
(ENAAQ-L)	3C14:7/167	
(ENAYZ-L)	3D31:25/73	
(ENARX-L)	3D31:5/73	
EM-Q	3C14:23/167	
EQ-N	3E1:8/83	
EQAQ-N	3E1:2/83	} $\overline{\text{RESFL}}$
EQRX-N	3E1:6/83	
EQYZ-N	3E1:16/83	
EM-LS3	3E19:4/91	
RESFL	2D7:6/32	DORLF. $\overline{\text{CPR}}$. $\overline{\text{EXEC}}$
EV32	Sheet 32	$\overline{\text{RESFL}}$. (131 FPURDY) + (137. FPUBUSY)
EVIDLE	3A12:2/40	(131. $\overline{\text{FPURDY}}$) + (137. FPUBSY)
ENKALL	Sheet 64	VIDLE
VIDLE		
(ENAJ-K)	3D8:25/64	
(ENKQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/64	
(ENYZ-K)	3D8:10/64	
EM-Q	3C14:13/167	
EQAZ-A	3F29:23/81	
V32		
EV32	Sheet 32	$\overline{\text{HR}}$. $\overline{\text{RTI}}$. [(130. FPURDY) + (137. $\overline{\text{FPUBUSY}}$)]
EVIDLE	3A12:2/40	$\overline{\text{HR}}$. $\overline{\text{RTI}}$. [(130. $\overline{\text{FPURDY}}$) + (137. FPUBUSY)]
ENKALL	Sheet 64	EVIDLE
V32		
UUFPUB	2E7:7/32	
EVW	2B3:18/3	
EEB-SO	2F7:17/106	HXOP
ENKALL	Sheet 64	
VW		
(EN-SAD)	2E11:3/93	
(EB-SO)	3E21:9/75	
(WRITE)	2E4:6/162	
(ENAJ-K)	3D8:25/64	
(ENKQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/64	
(ENYZ-K)	3D8:10/64	
(PLUS 1)	3D24:8/109	
EM-Q	3C14:23/167	
ELS3-XI	3F19:6/91	HXOP
EM-LS3	2E19:4/91	HXOP
EQ-N	3E1:8/83	
EQAQ-N	3E1:2/83	
EQRX-N	3E1:6/83	
EQYZ-N	3E1:16/83	
ULFPUB	2E7:23/32	$\overline{\text{VI}}$
EVW	2B3:18/3	$\overline{\text{VI}}$
EEB-SO	2F7:17/106	$\overline{\text{HXOP}}$
EVI	3A16:12/8	$\overline{\text{VI}}$
VW, VI		
(EN-SAD)	2E11:3/93	
(EB-SO)	3E21:9/75	
(WRITE)	2E4:6/162	
(FCAX-K)	3E10:10/67	
EI-Q	3C14:23/167	
EQAX-C	3E17:12/85	
FOV	3F21:9/100	RB23
CCY	3F12:18/99	
EOI	2A16:15/41	



COMMENTS

Relevant signals active in previous beat:
EVR, EESIN-B ($\overline{HXOP}$).

VR: The operand n is read to B from store. The K highway is forced to 8 (FK3), and this constant is strobed to P as a loop count. The carry bistable is cleared (CCY).

V9: Operand n is gated to the mill for testing purposes. For 150E the test is for n = -1, while for the 151E the test if for n = 0. Note the mill output will be zero if n = -1 (150E) or n = 0 (151E).

V10: 150E: The operand n ≠ x (x in A) is forced in the mill and strobed to B.

151E: The integer -1, forced in the mill (A and $\bar{A}$) is strobed to B.

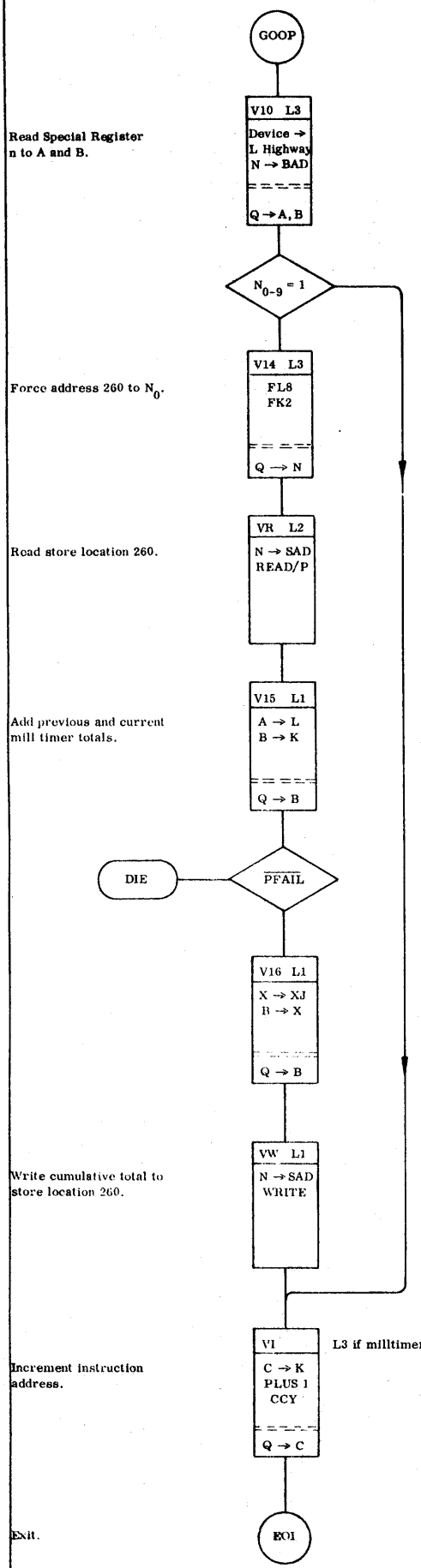
VW, VI: The content of B is written to store location N. The current instruction address is incremented (PLUS 1) and restored to C_{0-21}.

VW, $\overline{VI}$: When n = -1 (150E) or n ≠ 0 (151E) this beat is entered instead of V10, and operand n is returned to store.

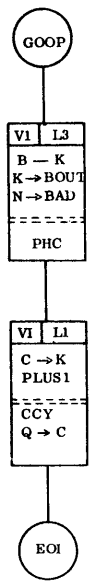
V11: The count in P is decremented in the mill, and the new value is tested prior to entry to the next beat.

V11 is looped a total of 8 times, until the count is zero, at which stage the instruction is repeated from VR.

VR SIGNAL	MP	CONDITIONS
(EN-SAD)	2E11:3/93	
(ESIN-B)	6D4:21/248	
(READ)	2E14:12/162	
(PAUSE)	2E10:6/276	
(FK3)	3D5:22/68	
ELS3-XJ	3F19:6/91	HXOP
EHX-B	3E14:6/87	HXOP
EM-Q	3C14:23/167	
EQAZ-P	3F3:18/84	
CCY	3F12:18/99	
EV9	2A4:9/12	
GBKALL	3F6:21/61	I151-4E
PNBAZ-K	2F17:24/94	I150E
V9		
(PCHECK)	3D15:17/112	
(EBAJ-K)	3F7:26/62	GBKALL
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3E7:4/62	
(EBYZ-K)	3F7:25/62	
(ENBAZ-K)	3D9:9/112	PNBAZ-K
PFAIL	6A6:21/214	PGEN ≠ RB24
DIE	3B33:25/44	PCHECK. PFAIL. $\overline{INHPFL}$
EV10	2A5:9/13	(I150E. $\overline{HM=0}$) + (I151E. HM=0)
GALALL	3D30:3/70	EV10
ENALALL	3D31:7/93	EV10. I151E
EENARXL	3E33:19/102	ENALALL
GBKALL	3F6:21/61	EV10. I150E
ENEQV	3D20:17/2	EV10. I150:1E
EVW	2B3:18/3	(I150E. $\overline{HM=0}$) + (I151E. $\overline{HM=0}$)
EEB-SO	2F7:17/106	EVW. $\overline{HXOP}$
V10		
(EAAQ-L)	3F33:25/72	GALALL
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
(ENAAQ-L)	3C14:7/167	ENALALL/ EENARXL
(ENARX-L)	3D31:5/73	
(ENAYZ-L)	3D31:25/73	
(EBAJ-K)	3F7:26/62	GBKALL
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3E7:4/62	
(EBYZ-K)	3F7:25/62	
(NEQV)	3E21:12/75	
EM-Q	3C19:23/167	
EQ-B	3D13:15/79	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
EVW	2B2:18/3	
EEB-SO	2F7:17/106	EVW. $\overline{HXOP}$
EVI	3A16:12/8	
VW, VI		
(EN-SAD)	2E11:3/93	
(EB-SO)	3E21:9/75	
(WRITE)	2E4:6/162	
(ECAX-K)	3E10:10/67	
(PLUS 1)	3D24:8/109	
ELS3-XJ	3F19:6/91	HXOP
EBAZ-X	3F25:8/90	HXOP
EM-Q	3C14:23/167	
EQAN-C	3E17:12/85	
EOI	2A16:15/41	
VW, $\overline{VI}$		
(EN-SAD)	2E11:3/93	
(EB-SO)	3E21:9/75	
(WRITE)	2E4:6/162	
EV11	2A6:16/14	
EPKALL	Page 66	
FLALL	2E32:6/76	
EENARXL	3E33:19/102	FLALL
V11		
(EAAQ-L)	3F33:25/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
(ENAAQ-L)	3C14:7/167	
(ENARX-L)	3D31:5/73	
(ENAYZ-L)	3D31:25/73	
(EPAJ-K)	3E9:3/66	
(EPKQ-K)	3E9:5/66	
(EPRX-K)	3E9:25/66	
(EPYZ-K)	3E9:23/66	
EM-Q	3C14:23/167	
EQ-P	3F3:18/84	
EOI	2A17:5/7	$\overline{HM=0}$
EESIN-B	2E17:7/44	EVR. $\overline{HXOP}$
EV11	2A6:16/14	$\overline{HM=0}$. $\overline{HR}$. $\overline{RTI}$
EPKALL	Page 66	EV11
FLALL	2E32:6/76	EV11
EENARXL	3E33:19/102	FLALL



COMMENTS	VIO / SIGNAL	MP	CONDITIONS
The device to be read is selected by the decode of the instruction's N-field which produces ND1, ND2, ND3, ND64, ND65 or ND129. These allow the contents of one of the special registers to be read.	GO1US	3D19:20/162	
	ETIM-L	2D16:21/60	ND1
	ETYP	3D16:16/	ND2, ND3
	E64-L	3D10:12/77	ND64
	E65-L	3D10:6/77	ND65
	ESP129	3D10:20/77	ND129
V10: The selected special register is addressed by N and its contents read to the L highway and strobed via the mill to A and B.	EQAZ-A	3F29:23/81	
	EQAJ-B	3D13:21/79	
	EQKM-B	3D13:22/79	
	EQNQ-B	3D13:24/79	
	EQRX-B	3E1:6/83	
	EQYZ-B	3E1:9/83	
	EQ-B	3D13:15/79	
	EN-BAD	3E28:20/108	
	EV14	2A7:9/18	$N_{0-9}=1$
	EFL08	3E11:25/114	
$N_{0-9}=1$ (and ND1) is active if the milltimer special register is to be read.	EVI	3A16:12/8	$\overline{N_{0-9}=1}$
	EBAZ-X	3F25:8/90	EV14
	V14		
V14: Address 260 (i.e. 256+4N) is forced to N by gating 256 to L and 4 to K and adding these in the mill. The sum (260) is then strobed to N. Milltimer register is cleared.	(FL08)	3D15:7/112	
	(FK2)	3D5:24/68	
	EQAQ-N	3E1:2/83	
	EQRX-N	3E1:6/83	
	EQYZ-N	3E1:16/83	
	EQ-N	3E1:8/83	
	EVR	2A17:5/7	
	EESIB-B	2E17:2/94	
	VR		
VR: The store is accessed at the address in N (260) and the previous milltimer total read to B, the store location being cleared by the PAUSE part of the beat.	(EN-SAD)	2E11:3/93	
	(ESIN-B)	6D4:21/248	
	(READ)	2E14:12/162	
	(PAUSE)	2E10:6/276	
	EV16	2A9:9/20	
	GALALL	3D30:3/70	
	GBKALL	3F6:21/61	
	EEBKM-K	Sheet 62	
V15: The previous and current milltimer totals are added (A → L and B → K respectively) in the mill and strobed to B.	V16		
	(EAAQ-L)	3F33:25/72	
	(EAAQ-L*)	3F33:23/72	
	(EAR-L)	3F33:21/72	
	(EASX-L)	3F33:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3F7:24/62	
	(EBNQ-K)	Sheet 62	
	(EBRX-K)	3E7:4/62	
	(EBYZ-K)	3F7:25/62	
	EQAJ-B	3D13:21/79	
	EQKM-B	3D13:22/79	
	EQNQ-B	3D13:24/79	
	EQRZ-B	3D13:23/79	
	EQ-B	3D13:15/79	
V16: Milltimer total written to X.	EVW	2B3:18/3	
	EEB-SO	2F7:17/106	
	VW		
	(EN-SAD)	2E11:3/93	
	(EB-SO)	3E21:9/75	
	(WRITE)	2E4:6/162	
	EVI	3A16:12/8	
VW: The new cumulative total formed in B in V16 is written to the address in N (still 260 from V14).	VI		
	(ECAX-K)	3E10:10/67	
	(PLUS 1)	3D24:3/109	
	EQAX-C	3E17:12/85	
	CCY	3F12:18/99	
	EOI	2A16:15/41	
VI: The instruction address is incremented and returned to C. Carry is cleared and during the subsequent Instruction Phase, the content of the special register read in V10 is copied from B to accumulator X if the order did not specify a milltimer-read operation.	ERX-XJ	3F20:4/89	

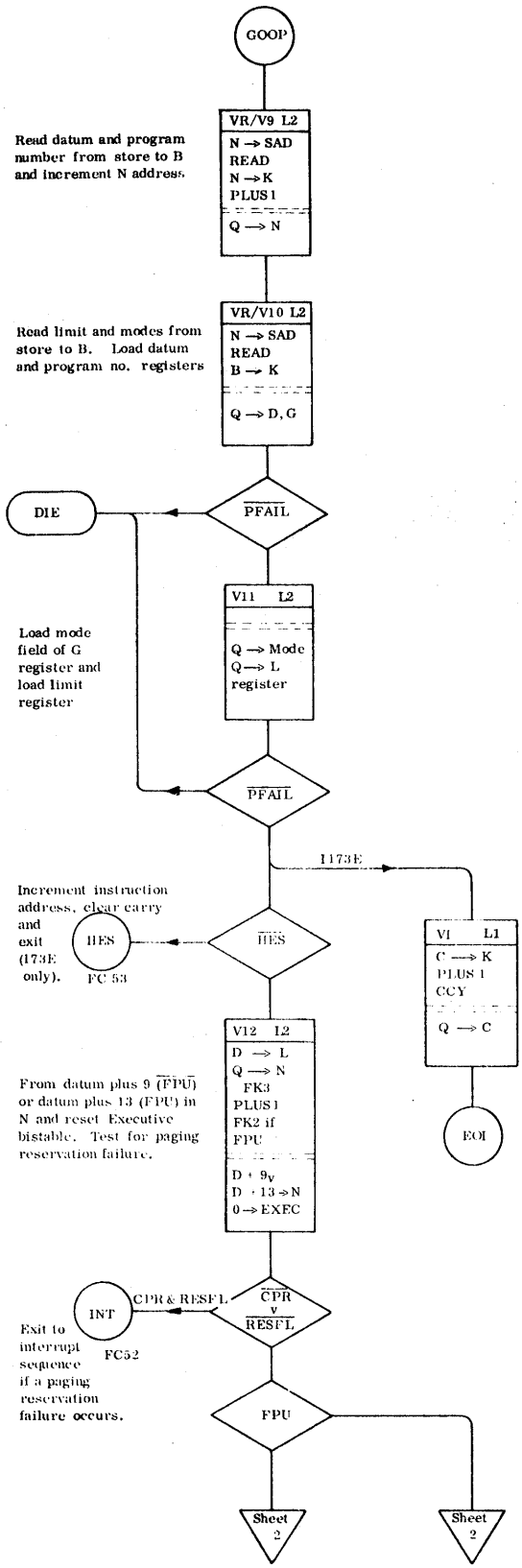


Address device via BAD from N and strobe the control code (x, in B) to it.

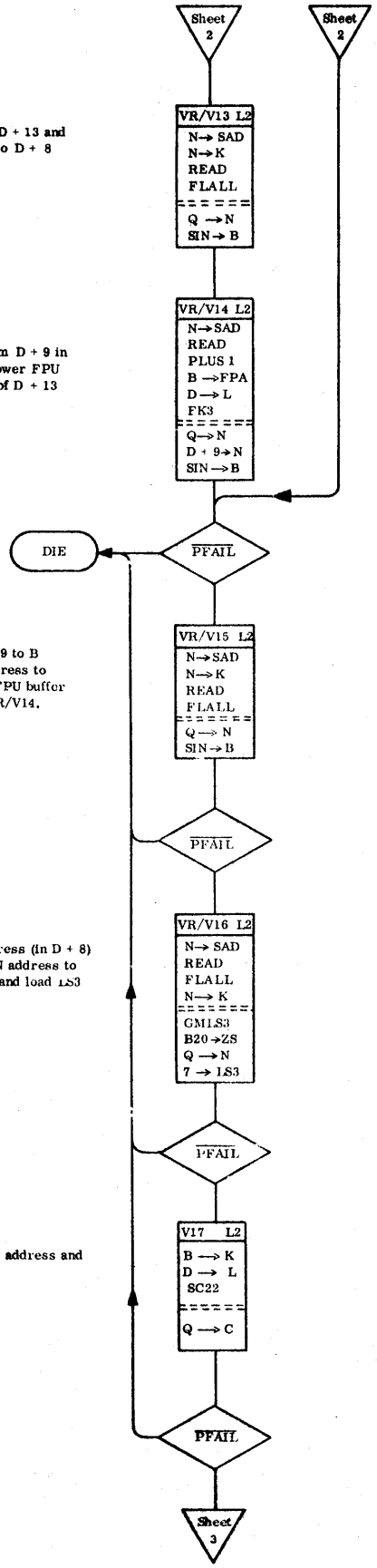
Increment instruction address and clear carry.

Exit.

COMMENTS	V1 / SIGNAL	M.P.	CONDITIONS
When a 171E order has been specified, VMOD of the Instruction Phase will load the content of accumulator X (x) to B (note, Q → B gating is inhibited in VMOD for a 171E order). Also active at GOOP time are I171E, GPD, EV1, GBKALL, EEBKM-K and GO1US.	EN-BAD	3E28:20/108	
	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3F7:24/62	
	(EBNP-K)	3E7:2/62	
	(EBQ-K)	3F7:23/62	
	(EBRX-K)	3E7:4/62	
	(EBYZ-K)	3F7:25/62	
	(PHC)	2F9:6/265	
	EV1	3A16:12/8	
V1:	VI		
The device is addressed from N_{0-5} and the content of accumulator X (the control code, in B from the Instruction Phase) is gated onto K. Data on K automatically appears at the BOUT gates which are opened in this case by K → BOUT. The control code is then loaded into the device's register.	(ECAX-K)	3E10:10/67	
	(PLUS1)	3D24:8/109	
	EQAX-C	3E17:12/85	
	EOI	2A16:15/21	
V1:			
The instruction address (in C) is incremented and returned to C. Carry is cleared and exit is made via EOI to the next Instruction Phase.			



COMMENTS	VR/V9 SIGNAL	MP	CONDITIONS
VR/V9: The datum and program number are held in the store location N loaded in the previous Instruction Phase. These are read to B and the address register is incremented (PLUS 1) to N + 1.	(EN-SAD)	2E11:3/93	
	(READ)	2E4:12/16	
	(ESIN-B)	6D4:21/248	
	(ENAJ-K)	3D8:25/64	
	(ENKQ-K)	3D8:23/64	
	(ENRX-K)	3D8:17/64	
	(ENYZ-K)	3D8:10/64	
	(PLUS 1)	3D24:8/109	
	EQNIP	3D2:26/82	
	$\overline{\text{EQAQ-N}}$	3E1:2/83	
	$\overline{\text{EQRX-N}}$	3E1:6/83	
	EQYZ-N	3E1:16/83	
	EQ-N	3E1:8/83	
	EVR	2A17:5/7	
	EV10	2B5:9/13	
	EESIN-B	2E17:2/94	
VR/V10: The limit and the machine modes are read from N + 1. During the store cycle, the datum read in VR/V9 is strobed to the datum register and the program number is placed in bits 6 to 9 of the C register.	VR/V10		
	(EN-SAD)	2E11:3/93	
	(READ)	2E4:12/16	
	(ESIN-B)	6D4:21/248	
	(PCHECK)	3D15:17/112	
	$\overline{\text{EQ-D}}$	3D28:26/108	
	EV11	2A6:16/14	
V11: The limit read in VR/V10 is transferred from B to the limit register and the machine modes are loaded into bits 0 to 5 of the G register.	V11		
	$\overline{\text{EDFG}}$	3F16:8/86	
	$\overline{\text{EQ-L}}$	3F16:22/86	
	EV12	3B11:10/15	1172E& ($\overline{\text{HR}}_V$ ENHNEIB)
	EVI	3A16:12/8	1173E
	GDLB	3D32:25/75	EVI 12
V12: The 172E order continues at V12. In this beat, D + 9 is formed in N (D + 13 if the floating point unit is fitted) and the EXEC bistable is reset. A paging reservation failure check is carried out and if this occurs, entry is made to V21 of the interrupt sequence.	V12		
	(ED-L:1)	3E21:15/75	$\overline{\text{CPR}}$
	(ED-L:2)	3E21:22/75	
	(PLUS 1)	3D24:8/109	
	$\overline{\text{(FK2)}}$	3D5:24/68	FPU
	(FK3)	3D5:22/68	
	EQNIP	3D2:26/82	
	$\overline{\text{EQAQ-N}}$	3E1:2/83	
	$\overline{\text{EQRX-N}}$	3E1:6/83	
	EQYZ-N	3E1:16/83	
	EQ-N	3E1:8/83	
	RESFL	2D7:6/32	DORLF
	EVR	2A17:5/7	
	EV13	2A18:5/16	FPU
	EV15	2A8:9/19	FPU
	EESIN-B	2E17:2/91	
	ENKALL	Sheet 61	
The sequence now divides, taking one of two branches dependant upon whether or not the hardware floating point unit (FPU) option is fitted.	VI		
	(ECAX-K)	3E10:10/67	
	(PLUS 1)	3D24:8/109	
	EQAX-C	3E17:12/85	
	EOI	2A16:15/41	



Read the content of D + 13 and decrement address to D + 8

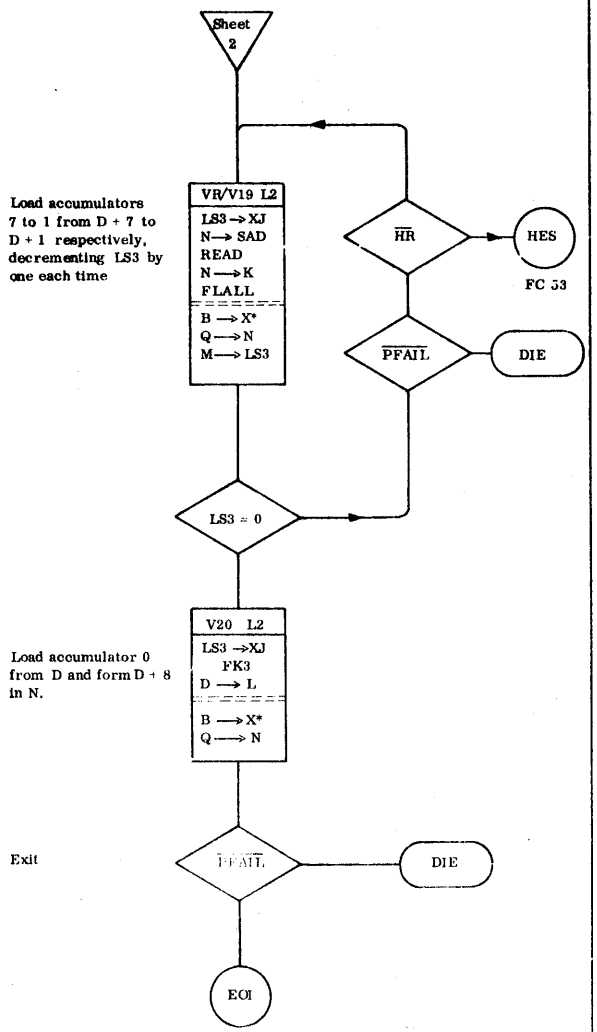
Read D + 12 and form D + 9 in register N. Load lower FPU buffer from content of D + 13 read in VR/V13.

Read content of D + 9 to B and decrement N address to D + 8. Load upper FPU buffer from data read in VR/V14.

Read instruction address (in D + 8) to B and decrement N address to D + 7. Set 25 mode and load LS3 register from mill.

Datumise instruction address and strobe to C.

COMMENTS	VR/V13 SIGNAL	M.P.	CONDITIONS
	(EN-SAD)	2E11: 3/93	
	(READ)	2E 4:12/16	
	(ESIN-B)	6D 4:21/248	
	NSUB	3F18:21/80	
	EVR	2A17: 5/7	
	EV14	2A 7: 9/18	
	GDLA	3F31:18/74	
	VR/V14		
VR/V13: The content of the store address held in N (D + 13 formed in V12) is read to B. This data is in face, the required content of the l.s. FPU buffer, N is decremented (by NSUB) to D + 12.	(EN-SAD)	2E11:3/93	
	(READ)	2E 4:12/16	
	(ESIN-B)	6D 4:21/248	
	(PCHECK)	3D28:26/108	
	NSUB	3F18:21/80	
	LLFPUB	2E 7:22/32	
	$\overline{FK3}$	3D 5:22/68	
	(PLUS1)	3D24: 8/109	
VR/V14: The content of D + 12 (the required content of the m.s. FPU buffer) is read to B. During the store cycle, the l.s. FPU buffer is loaded from the data in B (from VR/V13).	$\overline{EQAQ-N}$	3E 1: 2/83	
	$\overline{EQRX-N}$	3E 1: 6/83	
	EQYZ-N	3E 1:16/83	
	EQ-N	3E 1: 8/83	
	(ED-L:1)	3E21:25/75	
	(ED-L:2)	3E21:22/75	$\overline{CPR}$ & $\overline{EXEC}$
	EVR		
	EV15		
	ENKALL		
	VR/V15		
	(EN-SAD)	2E11: 3/93	
	(READ)	2E 4:12/16	
	(ESIN-B)	6D 4:21/248	
	(PCHECK)	3D28:26/108	
	NSUB	3F18:21/80	
VR/V15: The content of D + 9 is read from store. This word contains the ZS and A bistable modes. The address is then decremented to D + 8. During the store cycle, the m.s. FPU buffer is loaded from the content of B (loaded in VR/V14).	LUFPUB	2E 7: 2/32	
	EV16	2A 9/ 9/20	
	EVR	2A17: 5/7	
	EESIN-B	2E17: 2/94	
	ENKALL	Sheet 64	
	EENKQ-K	Sheet 64	
	VR/V16		
	(EN-SAD)	2E11:3/93	
	(READ)	2E4:12/16	
	(ESIN-B)	6D4:21/248	
	(PCHECK)	3D28:26/108	
	NSUB	3F18:21/80	
	$\overline{EM-LS3}$	3E19:4/91	
	(ENAJ-K)	3F7:24/62	
	(ENKQ-K)	3D8:23/64	
	(ENRX-K)	3D8:17/64	
	(ENYZ-K)	3D8:10/64	
VR/V16: The store is accessed at D + 8 to read out the instruction address. N is again decremented to give D + 7. During the store cycle, the ZS bistable is set (or reset) according to bit 20 of the word read to B in VR/V15. N is also gated via the mill back to N. This means that the l.s. 3 bits of the mill will contain the constant 7. These bits are copied into the LS3 register, forcing it to 7 to provide the count for VR/V19 (sheet 3).	$\overline{EQAQ-N}$	3E1:2/83	
	$\overline{EQRX-N}$	3E1:6/83	
	EQYZ-N	3E1:16/83	
	EQ-N	3E1:8/83	
	EV17	2A10:3/21	
	GDLA	3F31:18/74	
	GBKALL	3F6:21/61	
	EEBKM-K	Sheet 62	
	V17		
	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3F7:24/62	
	(EBNP-K)	3F7:2/62	
	(EBQ-K)	3F7:23/162	
	(EBRX-K)	3E7:4/62	
	(EBYZ-K)	3F7:25/62	
	(ED-L:1)	3E21:25/75	
	(ED-L:2)	3E21:22/75	
	EQCALL	3F17:2/85	
	EQAX-C	3E17:12/85	
V17: The instruction address read in VR/V16 is datumised and strobed to C.	EQZ-C	3E17:16/85	
	EVR	2A17:5/7	
	EV19	2A11:9/24	
	ENKALL	Sheet 64	
	EENKQ-K	Sheet 64	

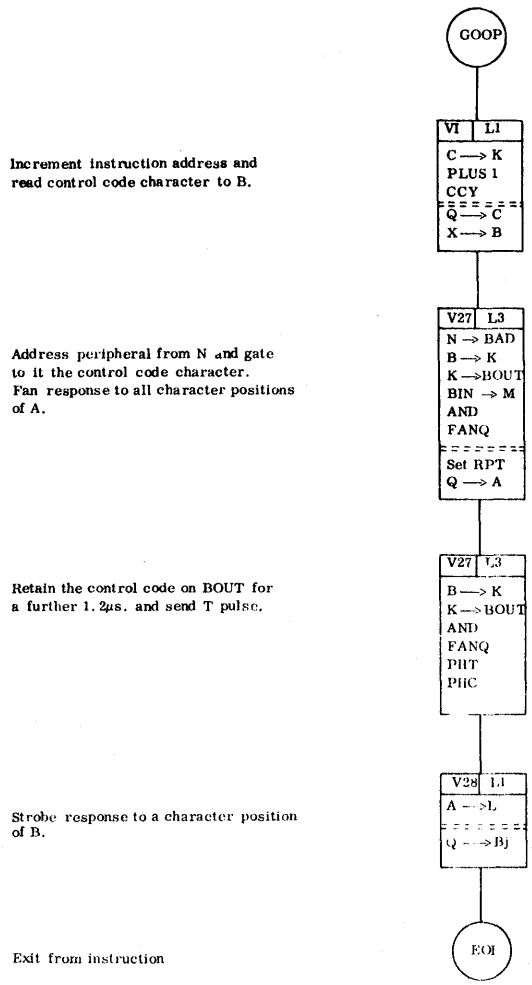


COMMENTS

VR/V19: The m.s. 7 hardware accumulators are reloaded from store locations D + 7 to D + 1, one accumulator being reloaded for each cycle of the loop. Each time VR/V19 is cycled, the address is decremented and returned to N via the mill. This allows LS3 to be reloaded for each cycle from the mill, decrementing its count by one each time. When this count equals zero, the m.s. 7 accumulators have all been loaded and entry is made to V20.

V20: The l.s. accumulator (0) is loaded from store address D. Bit 3 of K is forced to 1 and this is gated via the mill and Q to N. The datum is simultaneously gated to L and thus D + 8 appears on Q. This is then gated into N to give the address of the dumped instruction preparatory to the Instruction Phase which is entered at EOI.

VR/V19 SIGNAL	MP	CONDITIONS
FLALL	2E11: 3/93	
(EN-SAD)	2E 4:12/16	
(READ)	6D 4:21/248	
(ESIN-B)	3F18:21/80	
$\overline{EM-LS3}$	3E19: 4/91	
EBAZ-X	3F25: 8/90	
EBAZ-X*	3D 8:25/64	
(ENAJ-K)		
(ENKQ-K)	3D 8:23/64	
(ENRX-K)	3D 8:17/64	
(ENYZ-K)	3D 8:10 64	
$\overline{EQAQ-N}$	3E 1: 2/83	
$\overline{EQRX-N}$	3E 1: 6/83	
EQYZ-N	3E 1:16/83	
EQ-N	3E 1: 8/83	
ELS3-XJ		
EV20	3B13:18/25	FEOI & (ENHNEBI
EVR	2A17: 5/7	$\sqrt{\overline{LS3 = 0}}$ & $\overline{HR}$)
EV20	3B13:18/25	FEOI & LS3 = 0
GDLA	3F31:18/74	FEDI
V20		
(EN-SAD)	2E11: 3/93	
(READ)	2E 4:12/16	
(ESIN-B)	6D4:21/248	
(PCHECK)	3D15:17/112	
EBAZ-X	3F25: 8/90	
(FK3)	3D 5:22/68	FEOI
(ED-L:1)	3E21:25/75	$\overline{CPR}$ & $\overline{EXEC}$
(ED-L:2)	3E21:22/75	
$\overline{EQAQ-N}$	3E 1:2/83	
$\overline{EQRX-N}$	3E 1: 6/83	
EQYZ-N	3E 1:16/83	
EQ-N	3E 1: 8/83	
EOI	2A16:15/41	



Increment instruction address and read control code character to B.

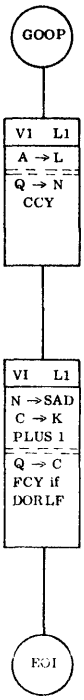
Address peripheral from N and gate to it the control code character. Fan response to all character positions of A.

Retain the control code on BOUT for a further 1.2μs. and send T pulse.

Strobe response to a character position of B.

Exit from instruction

COMMENTS	V1 / SIGNAL	M.P	CONDITIONS
Also active at entry will be I174E, EXEC, EVI.			
	(ECAX-K)	3E10:10/67	
	(PLUS 1)	3D24:8/109	
	CCY	3F12:18/99	
	EHX-B	3E14:6/87	
V1: The instruction address is incremented and returned to C. Accumulator X holds the control code character (bits 0-5) which is gated to B.	EV27	3B18:12/29	
	GBKALL	3F6:21/61	
	EEHKM-K	Sheet 62	
	EAND	2D18:25/95	
	V27		
V27 (& $\overline{\text{RPT}}$): The peripheral is addressed from N (loaded during the Instruction Phase) and the control code in B is strobed to it over the BOUT highway. The beat is 'stretched' to 1.2μs to allow time for the peripheral response to be received. This response is then formed to all character positions of A and the RPT bistable is set. AND is set to prevent the control code being OR'ed with the response onto the M highway - as L is all zeroes, the mill output will be all zeroes with AND active.	EN-BAD	3E28:20/108	
	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3F7:24/62	
	(EBNP-K)	3E7:2/62	
	(EBQ-K)	3F7:23/62	
	(EBRX-K)	3E7:4/62	
	(EBY-K)	Sheet 62	
	(EBZ-K)	Sheet 62	
	EBIN-M	3E25:6/90	
	(AND)	3E21:6/75	
	EMFAN	3F28:17/107	
	(RPT)	3C28:23/149	
	EQAZ-A	3F29:23/81	
	NR74v27	3D3:16/48	$\overline{\text{RPT}}$ & V27
V27 (&RPT): V27 is repeated to hold the control code on BOUT for a further 1.2μs and the T pulse (PHT) is sent to the peripheral.	EV27	3B18:12/29	NR74v27
	EV28	2B12:20/30	V27&RPT
	GALALL	3D30:3/70	EV28
	EEASX-L	Sheet 72	
	V28		
V28: The response received from the peripheral in V27 is gated to a selected character position of B. This will be the l.s. position (NCH - 3,) set in the Instruction Phase unless the order has been modified in w'ich case the character position will be determined by the top two bits of the modifier. The word containing this response character is written to accumulator X in the subsequent Instruction Phase.	(EAAQ-L)	3F33:25/72	
	(EAAQ-L*)	3F33:23/72	
	(EAR-L)	3F33:21/72	
	(EASX-L)	3F33:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	EQ-BJ	3E18:11/80	
	EOI	2A16:15/41	



Transfer x to register N and clear carry.

Increment instruction address and strobe to C. Force carry if datum or limit failure occurs.

Exit.

COMMENTS

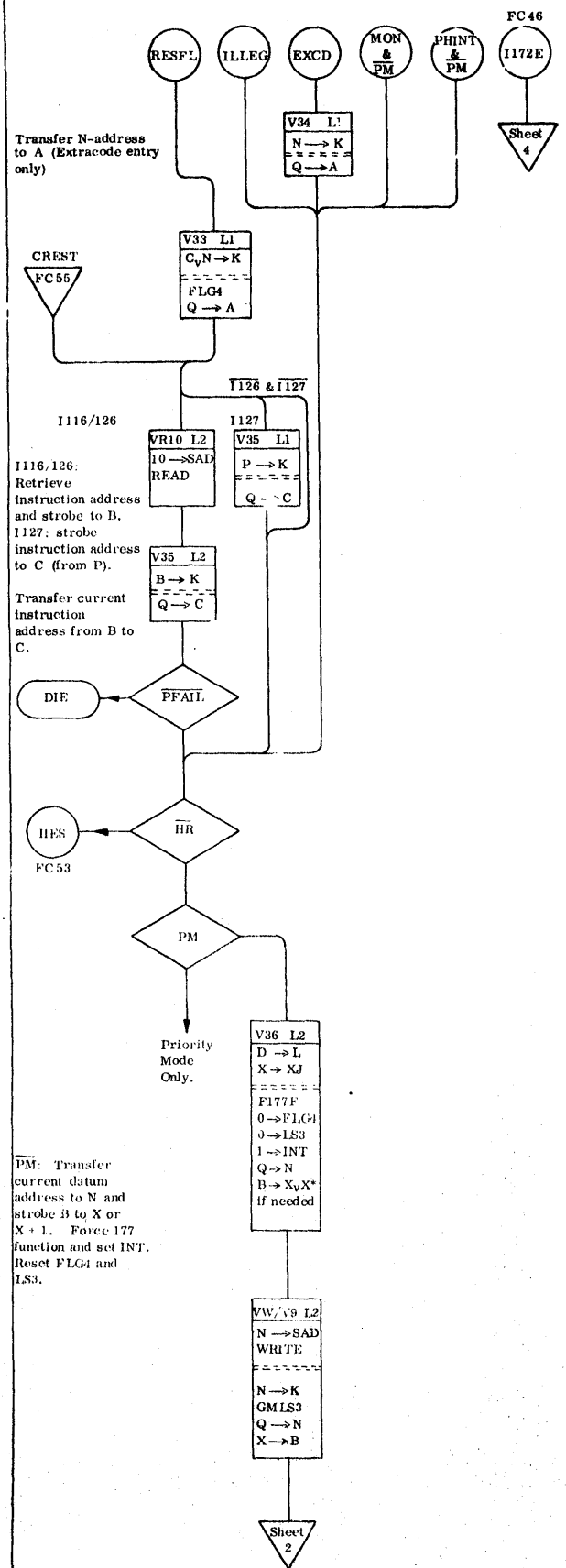
Also active at entry are I177E, GPD, EV1 and GALALL.

V1: The content of A (x, loaded in the Instruction Phase) is gated to the N register and carry is cleared.

VI: The content of N (x, from V1) is placed on the SAD highway and a reservation check made. If reservation failure occurs (DORLF) carry is forced set. The instruction address is incremented and the new address returned to C.

Exit is then made to the Instruction Phase.

V1 SIGNAL	MP	CONDITIONS
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
EQNIP	3D2:26/82	
$\overline{\text{EQAQ-N}}$	3E1:2/83	
$\overline{\text{EQRX-N}}$	3E1:6/83	
EQYZ-N	3E1:16/83	
EQ-N	3E1:8/83	
CCY	3F12:18/99	
EVI	3A16:12/8	
VI		
(EN-SAD)	2F11:3/93	
(ECAX-K)	3E10:10/67	
(PLUS1)	3D24:8/109	
(EQAX-C)	3E17:12/85	
FCY	3F15:17/106	DORLF
EOI	2A16:15/41	



COMMENTS

There are 7 entry points to the Interrupt Sequence:

Reservation failure: RESFL
CREST sequence: CREST (from VFC12)
Illegal order: ILLEG (GOOP & ASTAT & J117 & $\overline{\text{EXEC}}$)
172E sequence: I172E
Extracode: EXCD
Monitoring: MON ($\overline{\text{PM}}$)
Peripheral interrupt: (PIINT ($\overline{\text{PM}}$))

V34:

An EXCD interrupt requires the transfer of the N address to A to be written to store (or to an accumulator) in V11.

V33:

If entry was due to RESFL, the failed address is transferred to A from either C or N.

VR10/V34:

The instruction address (dumped in location 10 on entry to the 116/126 ((MOVE) order) is retrived and strobed to B.

V35:

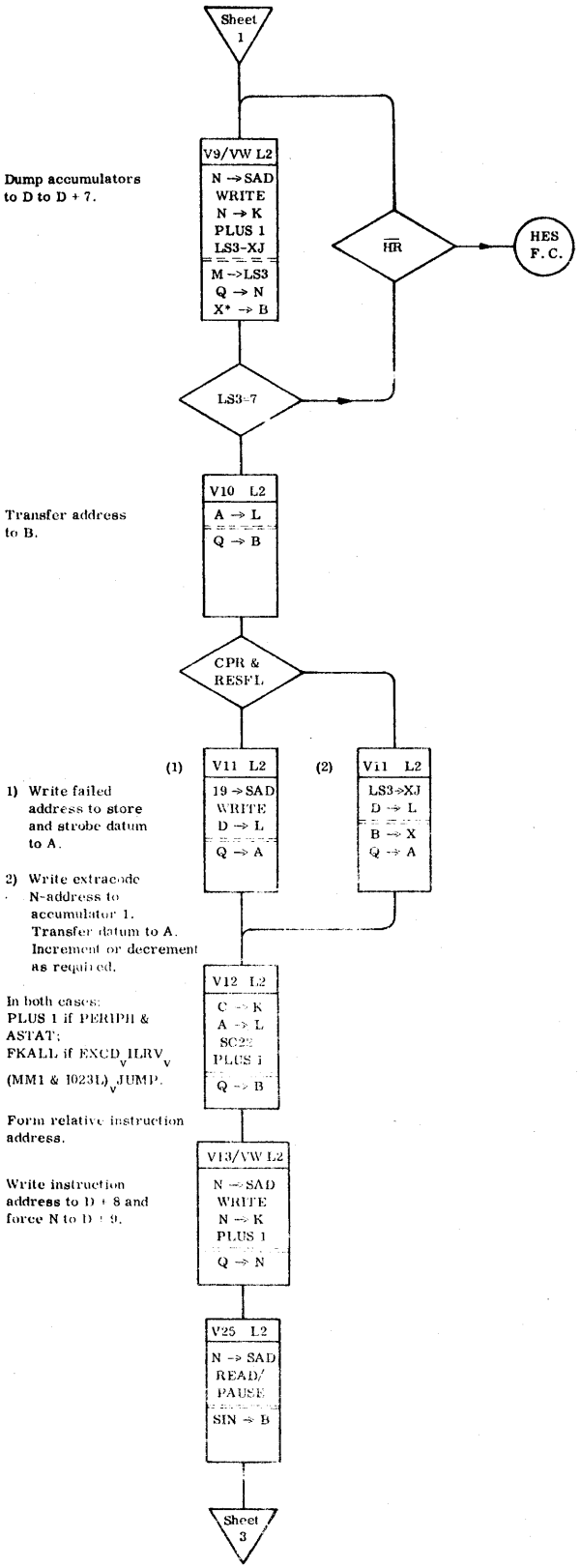
This beat is entered if the RESFL occurs in the loop of a 127 order. The current instruction address is then in P and is transferred to C to be incremented in V12. If the interrupted was a 116/1267, the same action occurs with the exception that the address is held in B rather than in P.

V36& $\overline{\text{PM}}$:

The datum for the interrupted program is transferred to N and the LS3 register is loaded from the mill. The accumulator address highway (XJ) is cleared and thus X0 is read to B. A 177 function is forced (F177F) to clean the function register and FLG4 is reset. INT is then set to indicate that the interrupt sequence proper is underway.

VW/V9:

V33 SIGNAL	M.P.	CONDITIONS
(EC-SAD)	3C14:8/167	(EC-SAD)
(EN-SAD)	2E11:3/93	(EN-SAD)
(WRITE)	2E4:6/162	
(EB-SO)	3E21:9/75	
RESFL	2D7:6/32	DORLF & $\overline{\text{CPR}}$ & $\overline{\text{EXEC}}$
ECAX-K	3E10:10/67	EC-SAD
ECY-K	3F10:25/67	
ECZ-K	3F10:19/67	
ENAJ-K	3D8:25/64	EN-SAD
ENKQ-K	3D8:23/64	
ENRX-K	3D8:17/64	
ENYZ-K	3D8:10/64	
EQAZ-A	3F29:23/81	
(FLG4)	2C8:24/156	
EVR10	3A14:22/39	MOVE
EV34	2B12:3/30	
EV35	2B21:12/34	$\overline{\text{MVSUM}}$
GDLA	3F31:18/74	EV36
EESIN-B	2E17:2/94	EVR10
V34		
(FSAD10)	2F10:9/112	I116, I126
FRCE1	2F3:3/115	
FRCE3	2F3:6/115	
(READ)	2E4:12/162	
(ESIN-B)	6D4:21/248	
RESFL	2D7:6/32	DORLF & $\overline{\text{CPR}}$ & $\overline{\text{EXEC}}$
ENAJ-K	3D8:25/64	EXCD
ENKQ-K	3D8:23/64	
ENRX-K	3D8:17/64	
ENYZ-K	3D8:10/64	
EQAZ-A	3F29:23/81	
EV35	2B21:12/34	MOVE
GBKALL	3F6:21/61	
V35		
(EBAJ-K)	3F7:26/62	MOVE
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3E7:4/62	
(EBYZ-K)	3F7:25/62	
EQCALL	3F17:2/78	
EQAX-C	3E17:12/85	
EQZ-C	3E17:16/85	
(EPAJ-K)	3E9:3/66	I127
(EPKQ-K)	3E9:5/66	
(EPRX-K)	3F9:25/66	
(EPYZ-K)	3F9:23/66	
(PCHECK)	3D15:17/112	
EV36	3A22:18/35	
GDLA	3F31:18/74	
V36		
(ED-L:1)	3E21:25/75	CPR & $\overline{\text{EXEC}}$
(ED-L:2)	3E21:22/75	
EQNIP	3D2:26/82	$\overline{\text{PM}}$
EQAQ-N	3E1:2/83	
EQRX-N	3E1:7/83	
EQYZ-N	3E1:16/83	
EQ-N	3E1:8/83	
F177F	3D14:25/104	
(INT)	2C27:23/147	
EM-LS3	3E19:3/91	
F164F	3D17:16/22	PM
GOOP	2B13:20/9	
EVW	2B3:16/3	$\overline{\text{PM}}$
EV9	2A4:9/12	
ENKALL	3E8:7/64	
EEB-SO	2F7:17/106	



Dump accumulators to D to D + 7.

Transfer address to B.

1) Write failed address to store and strobe datum to A.

2) Write extracode N-address to accumulator 1. Transfer datum to A. Increment or decrement as required.

In both cases: PLUS 1 if PERIPH & ASTAT; FKALL if $EXCD_V$ $ILRV_V$ (MM1 & 1023L)$_V$ JUMP.

Form relative instruction address.

Write instruction address to D + 8 and force N to D + 9.

COMMENTS

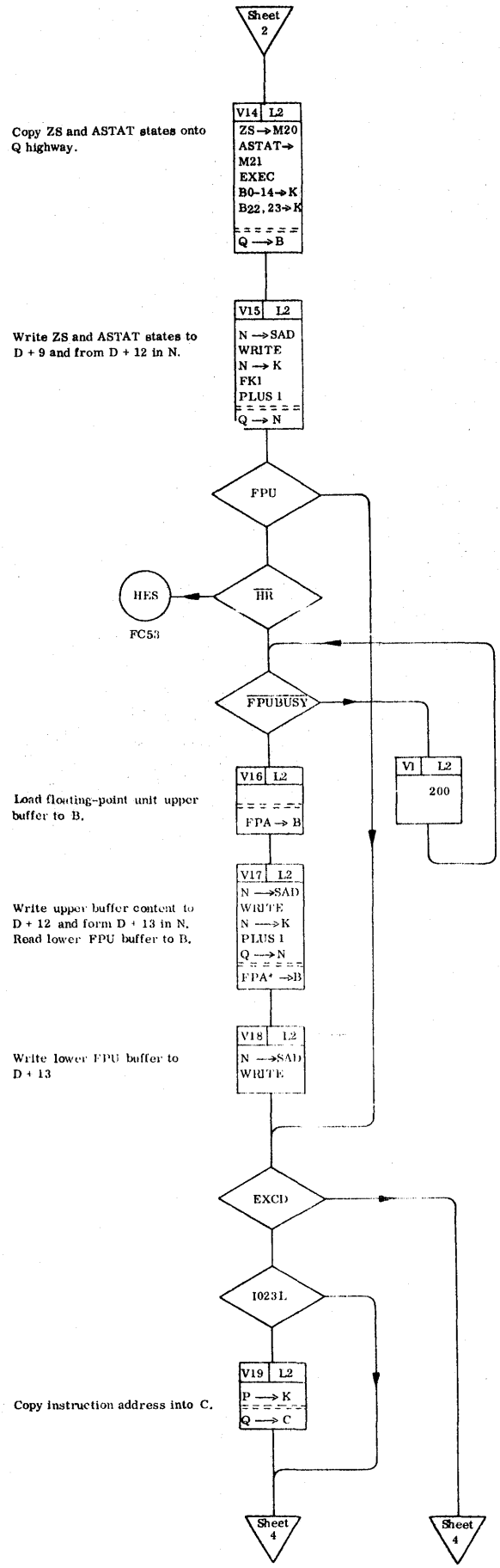
V9/VW: The accumulators 0 to 7 are dumped to store locations D to D + 7. LS3 is incremented for each cycle and a hesitation break-point is provided. When LS3-7 (i.e. all the accumulators have been dumped) V10 is entered.

V10: A contains the failed address (for RESFL entry) or the N address (for EXCD entry) and this is copied into B to be written to store or an accumulator in V11.

V11: For a paging failure entry (CPR & RESFL), the failed address is written to store location 19. Otherwise, accumulator 0 is addressed from LS3 and the extracode N address (or the current instruction address) is dumped to Accumulator 1.

In both cases, the datum is copied into Register A.

V9/VW SIGNAL	MP	CONDITIONS
(EN-SAD)	2E11:3/93	
(WRITE)	2E4:6/162	
(EB SO)	3E21:9/75	
RESFL	2D7:6/32	DORLF & $\overline{CPR}$ & $\overline{EXEC}$
(ENAJ-K)	3D8:25/64	
(ENKQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/64	
(ENYZ-K)	3D8:10/64	
(PLUS 1)	3D24:8/109	
EQNIP	3D2:26/82	
EQAQ-N	3E1:2/83	
EQRX-N	3E1:7/83	
EQYZ-N	3E1:16/83	
EQ-N	3E1:8/83	
EM-LS3	2E19:3/91	
EHX*-B	3F18:18/80	
ELS3-XJ	3F19:6/91	
EVW	2B3:18/3	$\overline{HR}$ & $\overline{LS3 = 7}$
EV9	2A4:9/12	
EV10	2A5:9/13	LS3 = 7
GALALL	3D30:3/70	
V10		
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3D33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
EQ-B	3D13:15/79	
EV11	2A6:16/11	
GDLA	3F31:18/74	
FKALL	5A6:9/60	$ILLRV64_V$
PNBAZ-K	2F17:24/94	$EXCD64_V$
GBKALL	3F6:21/61	
EEB-SO	2F7:17/106	CPR & RESFL
V11		
(FSAD19)	2F3:21/115	
(WRITE)	2E4:6/162	CPR & RESFL
(EB-SO)	2E21:9/75	
(ED-L:1)	3E21:25/75	
(ED-L:2)	5E21:22/75	
EQAZ-A	3F29:23/81	
ELS3-XJ	3F19:6/91	
EBAZ-X*	3F2:6/90	
(PLUS 1)	3D24:8/109	ASTAT & FKALL
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3F7:2/62	
(EBQ-K)	3F7:23/62	$ILLRV64_V$
(EBRX-K)	3F7:4/62	$EXCD64_V$
(EBYZ-K)	3F7:25/62	
(ENBAZ-K)	3D3:9/112	
EA12	3B11:10/15	
GCKALL	/67	
EENARX-L	3E33:10/102	
ESC22	3E4:25/98	
V12		
(ECAX-K)	3E10:10/67	
(ECY-K)	3F10:25/67	
(ECZ-K)	3F10:19/67	
(ENARX-L)	3D31:5/73	
(SC22)	3D3:22/112	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
EQ-B	3D13:15/79	
(PLUS 1)	3D24:8/109	
EV13	2A18:5/16	
EVW	2B3:18/3	
EEB-SO	2F7:17/106	
ENKALL	3F8:7/61	
V25		
(EN-SAD)	2E11:3/93	
(READ)	2E4:12/162	
(PAUSE)	2E10:7/143	
EV14	2A7:9/18	
V13/VW		
(EN-SAD)	2E11:3/93	
(WRITE)	2E4:6/162	
(EB-SO)	2E21:9/75	
RESFL	2D7:6/32	DORLF & $\overline{CPR}$ & $\overline{EXEC}$
(ENAJ-K)	3D8:25/64	
(ENKQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/64	
(ENYZ-K)	3D8:10/64	
(PLUS 1)	3D24:8/109	
EQAQ-N	3E1:2/83	
EQRX-N	3E1:7/83	
EQYZ-N	3E1:10/83	
EQ-N	3E1:8/83	
EV25	3B19:21/29	
EEN-SAD	/93	



V14: The state of the ZS bistable is copied into M20 and, if entry to the sequence was of the MON or ILLEG type, the state of the A bistable (ASTAT) is copied to Q21. The Q highway is then loaded to register B.

V15: B (containing the ASTAT and/or ZS states) is written to D + 9. The address D + 9 is incremented by 3 to give D + 12.

V16: If the FPU facility is fitted, its upper buffer is loaded to B.

V17/VW: The content of the FPU upper buffer is written from B to D + 12. D + 13 is formed in N (D + 13 & PLUS1). The lower FPU buffer is strobed to B for V18/VW.

V18/VW: The content of the lower FPU buffer is written from B to D + 13.

V19: This beat is entered if EXCD & I023L are set. The instruction address (in P from the Instruction Phase) is then copied to register C.

V14 / SIGNAL	M.P.	CONDITIONS
EZSQ20	2E 7:11/32	
EAS-Q21	2F 2:15/142	MON64, ILLEG64
EXEC	2C 1:25/144	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
EQ-B	3D13:15/79	
EV15	2A 8: 9/19	
GNKIP	3D 9:10/63	
ENKALL	3F 8: 7/64	
EEB-SO	2F 7:17/106	
EENKQ-K	Page 64	
V15		
(EN-SAD)	2E11: 3/93	
(WRITE)	2E 4: 6/162	
(EB-SO)	3E21: 9/25	
RESFL	2D 7: 6/32	DORLF & $\overline{QR4}$ EXEC.
(ENAJ-K)	3D 8:25/64	
(ENKQ-K)	3D 8:23/64	
(ENRX-K)	3D 8:17/64	
(ENYZ-K)	3D 8:10/64	
(FK1)	3D 5: 8/68	
(PLUS1)	3D24: 8/109	
EQ-N	3E 1: 8/83	
(EQNIP)	3D 2:26/82	
EV16	2A 9: 9/20	FPU & HR & $\overline{\text{FPUBUSY}}$
EV19	2A11: 9/24	EXCD64 & $\overline{\text{FPU}}$ & I023L
EVIDLE	3A12: 2/40	See Comments
EV20	3B13:18/25	FPU & EXCD64 & I023L
EVR	2A17: 5/7	
EV21	3B14:26/26	$\overline{\text{FPU}}$ & EXCD64
EPKALL	Page 66	EV19
EEC-SAD	2F 6:18/92	EV20
V16		
UUFPUB	2F 7: 7/32	
EV17	2A10:3/21	
EVW	2B 3:18/3	
GNKIP	3D 9:10/63	
ENKALL	3F 8: 7/64	
EENKQ-K	Page 64	
EEB-SO	2F 7:17/106	
V18/VW		
(EN-SAD)	2E11: 3/93	
(WRITE)	2E 4: 6/162	
(EB-SO)	3E21: 9/75	
RESFL	2D 7: 6/32	DORLF & $\overline{CPR}$ & $\overline{EXEC}$
EV19	2A11: 9/24	I023L & EXCD64
EV20	3B13:18/25	EXCD64 & I023L
EVR	2A17: 5/7	
EV21	3B14:26/26	$\overline{EXCD64}$
EPKALL	Page 66	EV19
EEC-SAD	2F 6:18/92	EV20
V17/VW		
(EN-SAD)	2E11: 3/93	
(WRITE)	2E 4: 6/162	
(EB-SO)	3E21: 9/75	
RESFL	2D 7: 6/32	DORLF & $\overline{CPR}$ & $\overline{EXEC}$
(ENAJ-K)	3D 8:25/64	
(ENKQ-K)	3D 8:23/64	
(ENRX-K)	3D 8:17/64	
(ENYZ-K)	3D 8:10/64	
(PLUS 1)	3D24: 8/109	
EQAQ-N	3E 1: 2/83	
EQRX-N	3E 1: 7/83	
EQYZ-N	3E 1:16/83	
EQ-N	3E 1: 8/83	
ULFPUB	2F 7: 7/32	
EV18	3B12:22:23	
EVW	2B 3:18/3	
EEB-SO	2F 7:17/106	
V19		
(EPAJ-K)	3E 9: 3/66	
(EPKQ-K)	3E 9: 5/66	
(EPRX-K)	3F 9:25/66	
(EPYZ-K)	3F 9:23/66	
EQCALL	3F17: 2/85	
EQAX-C	3E17:12/85	
EQZ-C	3E17:16/85	
EV20	3B13:18/25	
EV.(	2A17: 5/7	
EE.-SAD	2F 6:18/92	
EESIN-B	2E17: 2/94	

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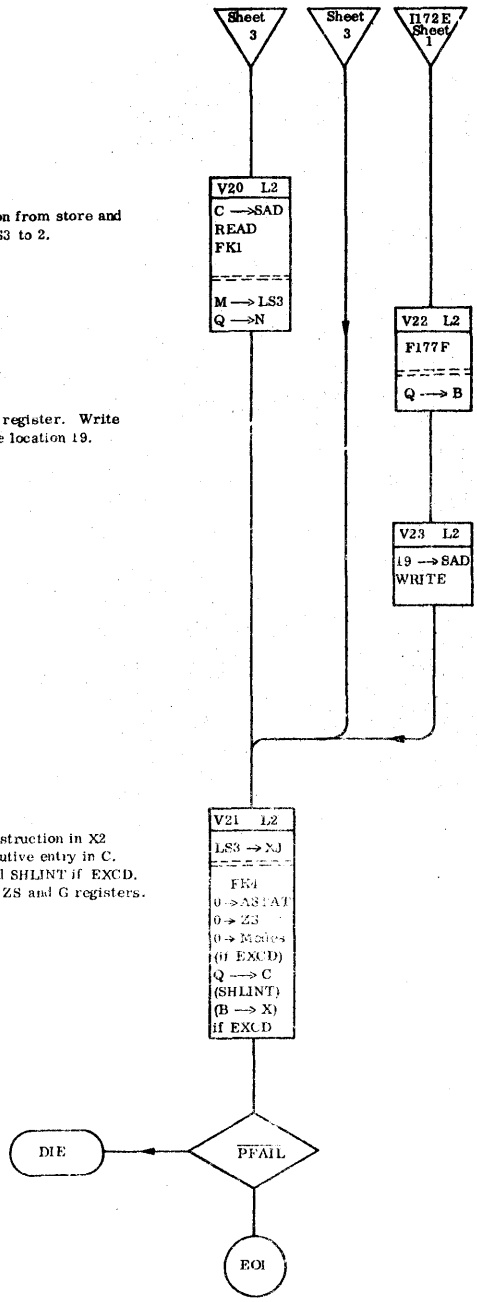
ICL | 1904A MKII 1904S,1903T | INTERRUPT SEQUENCE (V14 – V19) | FC52 SHEET 3 OF 4



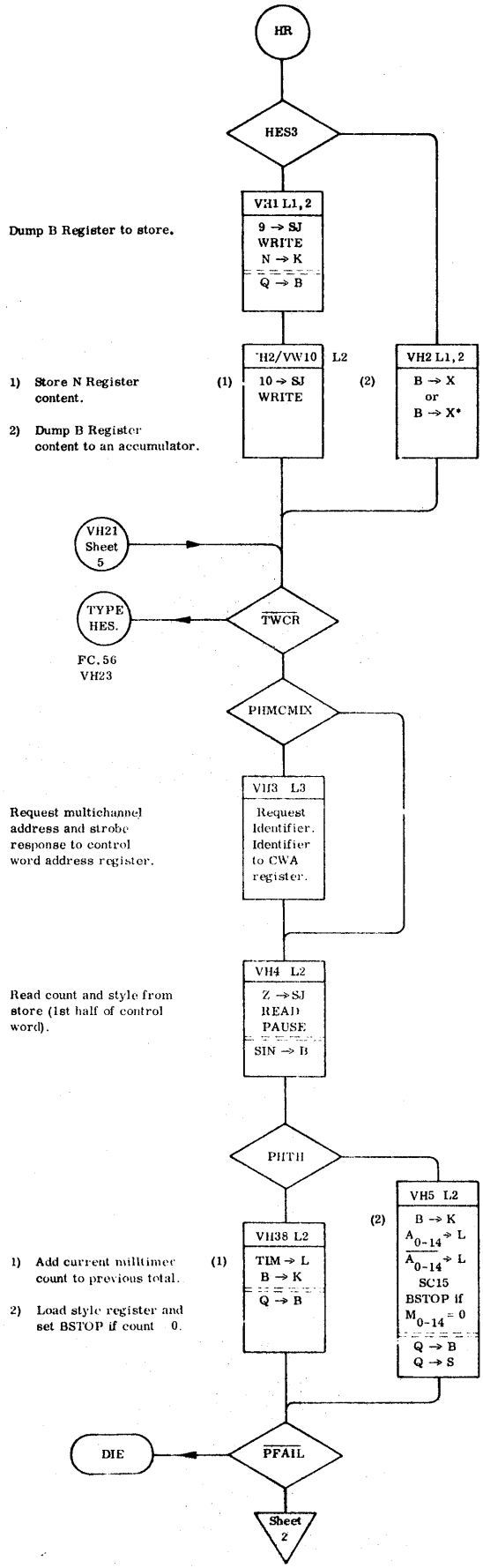
Read instruction from store and force N and LS3 to 2.

Clear function register. Write Datum to store location 19.

Dump EXCD instruction in X2 and form Executive entry in C. Set PLUS 1 and SHLINT if EXCD. Reset ASTAT, ZS and G registers.

Exit

COMMENTS	V20/VR SIGNAL	M.P.	CONDITIONS
	(EC-SAD)	3C14:8/167	
	(READ)	2E4:12/162	
	(ESIN-B)	6D4:21/248	
	(FK1)	3D5:8/68	
	EM-LS3	3E19:3/91	
	EQAQ-N	3E1:2/83	
	EQRX-N	3E1:7/83	
	EQYZ-N	3E1:16/83	
	EQ-N	3E1:8/83	
	EV21	3B14:26/26	
	V22		
V20; The address loaded in V19 is read to obtain the instruction from store and N and LS3 are forced to 2.			
	EQAJ-B	3D13:21/79	
	EQKM-B	3D13:22/79	
	EQNQ-B	3D13:24/79	
	EQRZ-B	3D13:23/79	
	EQ-B	3D13:15/79	
V22: If the sequence is entered from a 172E order (with a paging failure), the datum for the failed address is transferred to B and a 177 function is forced to test the datum.	F177F	3D14:25/104	
	EV23	2A13:8/9	
	EEB-SO	2F7:17/106	
	V23		
	(FSAD19)	Page 115	
	(WRITE)	2E4:6/162	
	(EB-SO)	3 E21:9/75	
V23/VW: The datum is written to store address 19.	RESFL	2D7:6/32	DORLF & $\overline{\text{CPR}}$ & $\overline{\text{EXEC}}$
	EV21	3B14:26/26	
	V21		
	(FK4)	3D5:26/172	
	EQCALL	3F17:12/75	
	EQAX-C	3E17:12/75	
	EQZ-C	3E17:16/75	
	(PLUS1)	3D24:8/109	INT
	ELS3-XJ	3F19:6/91	FLG1 & CHMV106
V21: The EXCD instruction is written to accumulator 2 (LS3 forced to 2 in V20) and the Executive entry address is formed in C. This is 16 for involuntary entries and 32 for voluntary entries. SHIJNT (shift left n → Q) is active to give 32.	EBAZ-X	3F25:8/90	EXCD
	RESETG	3F16:13/86	
	(SHLINT)	2D3:21/48	EXCD
	(PCHECK)	3D15:17/112	I172E
	EOI	2A16:15/41	
The A and ZS bistables are now reset as in the mode-field of the G register (by RESETG).			
The sequence exits at EOI.			



COMMENTS

A hesitation request (HR) will be allowed when HESBKPT is active. EIHES will also be active if the break-point is of the end of order type.

VH1: Type 3 hesitations require dumping of the B register to store: for other types it is dumped to an accumulator (in VH2).

VH2 & VW10: For type 3 hesitations, the N register is written to store (VW10). VH2 gates B to an accumulator for other types of hesitation as described above, the selection of X or X + 1 being decided as follows:-

B → X if: ENDHES & EOI & (CG00 v CG10 v I02N3:6 v IH0:2 v I170: 4E v I12N356) v (I114:5 & V15).

B → X + 1 if: ENDHES & EOI & (I040:3 v I111:3 v I114:5).

PHMCMIX is active when the hesitation request is from a multichannel device.

VH3: In this case, a request is sent to the device for the 'address' of the requesting mechanism. The reply to this request is gated into the control word address register in the Distributor Plane by STR510.

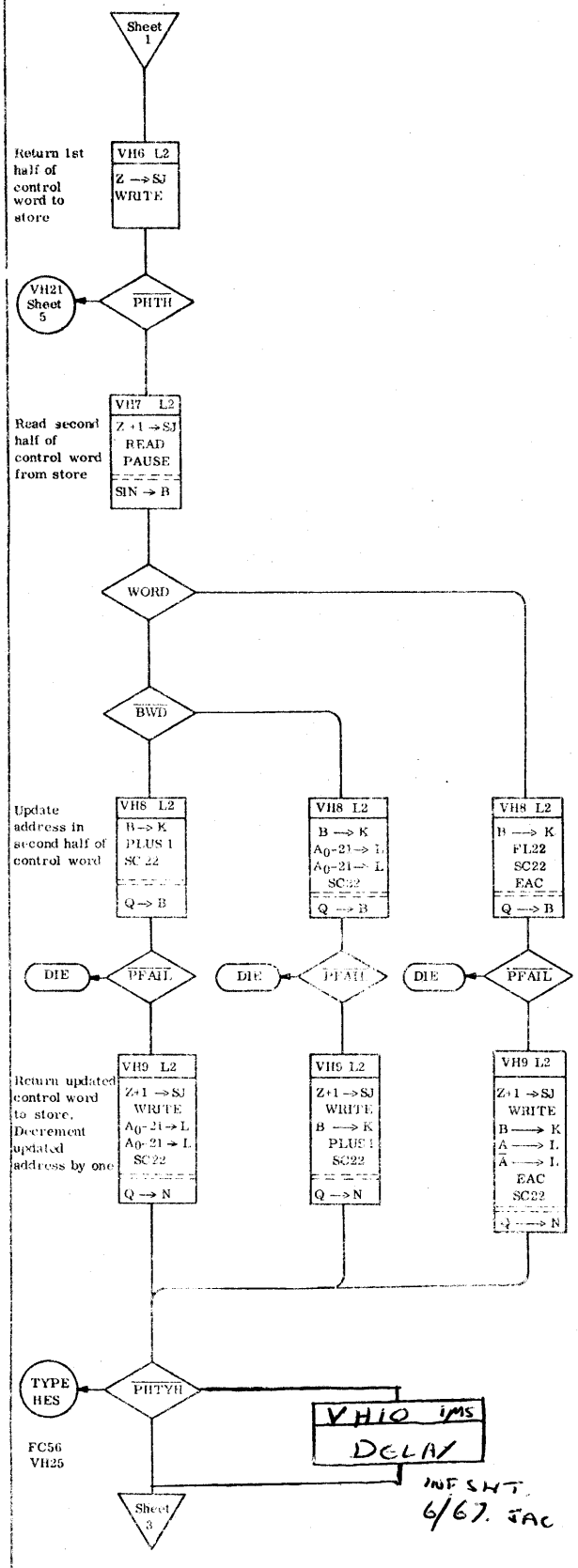
VH4: The style and count are read from store. This information is contained in the first control word.

PHTH: indicated that the hesitation request is from the milltimer.

VH38: For milltimer requests the content of the timer register is gated to Register B.

VH5: For all other requests one is subtracted from the count field and the style register is loaded. If the count equals zero, BSTOP is set for use in VH12 (q.v).

VH1 SIGNAL	MP	CONDITIONS
(FSAD9)	2F10:6/112	
FRCE0	2F3:8/115	
FRCE3	2F3:6/115	
(EB-SO)	3E21:9/75	
(WRITE)	2E4:6/162	DORLE & $\overline{\text{CPR}}$
RESFL	2D7:6/32	& $\overline{\text{EXEC}}$
(ENAJ-K)	3D8:25/64	
(ENKQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/64	
(ENYZ-K)	3D8:10/64	
(EQAJ-B)	3D13:21/79	
(EQKM-B)	3D13:22/79	
(EQNQ-B)	3D13:24/79	
EQRZ-B	3D13:23/74	
EQ-B	3D13:15/79	
EEB-SO	2F7:17/106	
EVW10	3A18:10/38	HES3
$\overline{\text{EVH2}}$	2C14:13/45	
$\overline{\text{GHESPR}}$	2E1:9/140	EVH2
VH2 & VW10		
(FSAD10)	2F10:9/112	} HES3
FRCE3	2F3:6/115	
FRCE1	2F3:3/115	
(EB-SO)	3E21:9/75	
(WRITE)	2E4:6/162	DORLF & $\overline{\text{CPR}}$ & $\overline{\text{EXEC}}$
(EBAZ-X)	3F25:8/90	} See Comments
(EBAZ-X*)	3F25:6/90	
EESIN-B	2E17:2/94	
EVH3	2A1:25/45	PHMCMIX
EVH4	2C9:4/42	$\overline{\text{TWCR}}$ & PHMCMIX
EVH23	2D9:22/42	TWCR
VH3		
$\overline{\text{(PHNO)}}$	2F9:8/265	
STR510	5A4:6/269	
EESIN-B	2E17:2/94	
EVH4	2C9:4/42	
V4		
(ECW-SAD)	2F3:25/115	
(READ)	2E4:12/162	
(PAUSE)	2E10:7/143	
(ESIN-B)	6D4:21/248	
$\overline{\text{GBKALL}}$	3F6:21/61	
EVH5	3B32:17/59	PHTH
EVH38	3B32:4/59	PHTH
VH5		
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3E7:4/62	
(EBYZ-K)	3F7:25/62	
EQAJ-B)	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
EQ-B	3D13:15/79	
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3F33:23/72	
(ENAAQ-L)	3C14:7/167	
(SC15)	3D15:6/112	
(OUT)	3C17:6/266	} S register bits
(BWD)	2C15:9/266	
(WORD)	3C17:12/266	
(MCHAN)	3C17:27/266	
(RCHG)	3C17:22/266	
(SG)	3C14:11/167	
WDFWD	2E15:19/141	WORD & FWD
CHF	2E15:15/141	$\overline{\text{WORD}}$ & $\overline{\text{FWD}}$
WDIN	2D11:24/142	WORD & $\overline{\text{OUT}}$
VH5		
WDOUT	2F16:16/60	WORD & OUT
(BSTOP)	2C5:22/157	M0014ZR
(PCHECK)	3D15:17/112	
EEB-SO	2F7:17/106	
EVH6	3B32:10/59	
VH38		
ETIM-L	2D16:21/60	
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3E7:4/62	
EQBIP	2D17:7/78	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
EEB-SO	2F7:17/106	
EVH6	3B32:10/59	



COMMENTS	VH6 SIGNAL	M.P.	CONDITIONS
	(ECW-SAD)	2F3:25/115	
	(EB-SO)	2E21:9/75	
	(WRITE)	2E4:6/162	
	EESIN-B	2E17:2/94	PHTH
	EVH7	3A32:9/59	
	VH7		
	(ECW-SAD)	2F3:25/115	
	ERCE0	2F3:8/115	
	(ESIN-B)	6D4:21/248	
	(READ)	2E4:12/162	
	(PAUSE)	2E10:7/143	$\overline{\text{INHPAUS}}$
PHTH is active for a milltimer hesitation request (from the Data Flow plane) if no peripheral hesitation requests are waiting.	FLAX	3D29:25/113	WORD & BWD
	$\overline{\text{EENARX-L}}$	3E33:9/102	
	$\overline{\text{GBKALL}}$	3F6:21/61	
	ESC22	3E4:25/98	
	VH8		
	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3F7:24/62	
	(EBNP-K)	3E7:2/62	
	(EBQ-K)	3F7:23/62	
	(EBRX-K)	3E7:4/62	
	(EBYZ-K)	3F7:25/62	
	EQBIP	2D17:7/78	
	EQAJ-B	3D13:21/79	
	EQKM-B	3D13:22/79	
	EQNQ-B	3D13:24/79	
	EQRZ-B	3D13:23/79	
WORD and BWD are activated by style register bits 21 and 22 respectively.	EQ-B	3D13:15/79	
	(SC22)	3D3:22/112	
	(PLUS 1)	3D24:8/109	WDFWD
	(EAC)	3D13:16/79	CHF
	(ENAAQ-L)	3C14:7/167	
	(ENARX-L)	3D31:5/73	
	(EAAQ-L)	3F33:25/72	WORD & BWD
	(EAAQ-L*)	3F33:23/72	
	(EASX-L)	3F33:7/72	
	(EAR-L)	3F33:21/72	
	(PCHECK)	3D15:17/112	
	VH8		
VH8 & VH9: The address field of the second half of the control word must be updated for possible use in the next cycle of the Slow Hesitation sequence. The original address is needed for the present cycle however and so the updated address is decremented by one for use later in this sequence.	FLAX	3D29:25/113	$\overline{\text{BWD}}$
	EENARXL	3E33:19/102	$\overline{\text{BWD}}$
	FLALL	3F32:18/76	$\overline{\text{WORD}}$ & $\overline{\text{BWD}}$
	$\overline{\text{EEB-SO}}$	2F7:17/106	
	$\overline{\text{GBKALL}}$	3F6:21/61	
	ESC22	3E4:25/98	
	VH9		
	FRCE0	2F3:8/115	
	(ECW-SAD)	2F3:25/115	
	(EB-SO)	2E21:9/75	
	WRITE	2E4:6/162	DORLF & $\overline{\text{CPR}}$ & $\overline{\text{EXEC}}$
	RESFL	2D7:6/32	
	(ENAAQ-L)	3C14:7/167	
	(ENARX-L)	3D31:5/23	$\overline{\text{BWD}}$
	(ENAYZ-L)	3D31:25/73	
	(ENARX-L)	3D31:9/73	
	(EAAQ-L)	3F33:25/72	$\overline{\text{WDFWD}}$
	(EAAQ-L*)	3F33:23/72	
	(EAR-L)	3F33:21/72	
	VH9		
	(EAY-L)	3F33:5/72	
	(EAZ-L)	2F33:3/72	$\overline{\text{WDFWD}}$
	(EASX-L)	3F33:7/72	
	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3F7:24/62	
	(EBNP-K)	3E7:2/62	
	(EBQ-K)	3F7:23/62	
	(EBRX-K)	3E7:4/62	
	(EBYZ-K)	3F7:25/62	
	(SC22)	3D3:22/112	
	(PLUS 1)	3D24:8/109	WDBWD
	(EAC)	3D13:16/79	CHF
	(EQAQ-N)	3E1:2/83	
	EQRX-N	3E1:7/83	
	EQYZ-N	3E1:16/83	
	EQ-N	3E1:8/83	
PHTYH indicates a typewriter hesitation request and is made in the Data Flow.	EESIN-B	2E17:2/94	PHTYH
	EVH25	3A33:4/59	PHTYH
	EVH11	2B14:6/44	$\overline{\text{PHMC MIX}}$ & $\overline{\text{PHTYH}}$ & $\overline{\text{WDIN}}$
	EVH12	2B14:25/44	$\overline{\text{PHMC MIX}}$ & $\overline{\text{WDIN}}$
	EVH9	2A7:5/13	PHMC MIX

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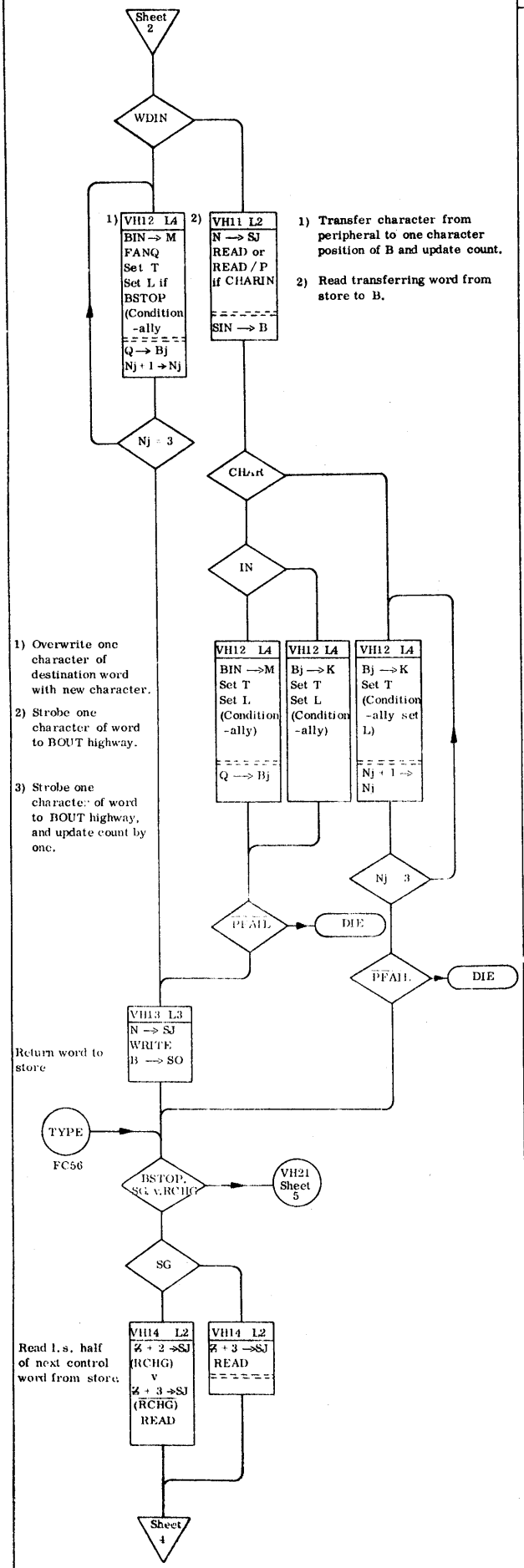
ICL | 1904A MK II 1904S 1903T | SLOW HESITATION SEQUENCE (VH6-VH10) | FC53 SHEET 2 OF 5



1) Transfer character from peripheral to one character position of B and update count.

2) Read transferring word from store to B.

COMMENTS

VH12: For an inwards word transfer (WDIN), the word is transferred to B one character at a time, the count being updated by 1 for each loop. When the count equals 3, the complete word is written to store (VH13).

VH11: For any other type of transfer, the transferring word is read from store to B. The store cycle is a read for character or outward transfer, and a read/pause for an inward or word transfer.

VH12: For an inwards character transfer, the character is read from the BIN highway to one character position of the word accessed in VH11. L is set if BSTOP & $\overline{SG}$ & $\overline{RCHG}$.

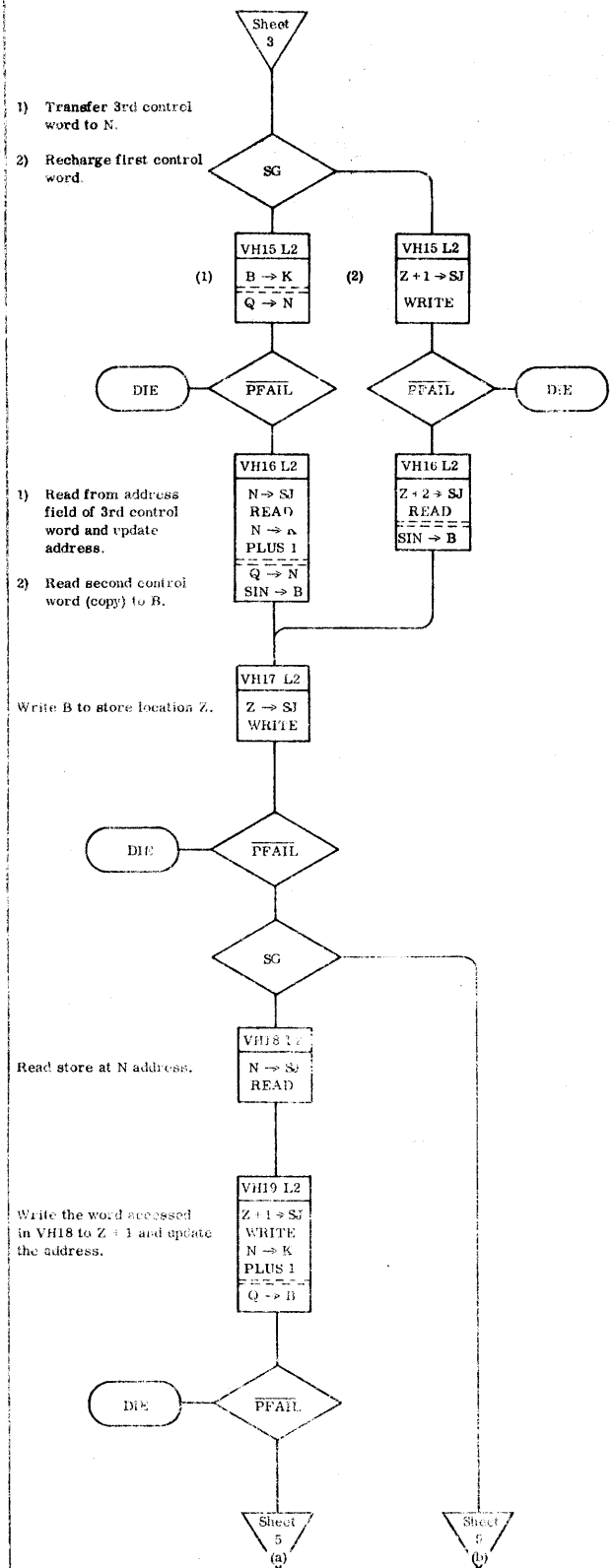
If an outwards character transfer is to occur, the character is placed at the entry to the BOUT highway (on K) ready for transfer at the exit strobe.

An outward word transfer is accomplished by four cycles similar to that for an outward character transfer, but the character count must be updated by 1 for each loop until Nj = 3.

VH13: Returns the transferring word to store.

VH14: Reads the control word from store. If scatter-gather and recharge are required, Z + 3 is read.

VH11 SIGNAL	:4 P.	CONDITIONS
(EN-SAD)	2E11:3/93	
(ESIN-B)	6D4:21/248	
(READ)	2E4:12/162	
(PAUSE)	2E10:7/143	$\overline{WORD}$ & $\overline{OUT}$ & INITPAUS
EVH12	2B14:25/106	
EEBJ-K	3D7:17/71	OUT
VH12		
(PCHECK)	3D15:7/112	
EBIN-M	3E25:6/90	$\overline{OUT}$
EQ-BJ	3E18:11/80	
EMFAN	3F28:17/107	WORD & $\overline{OUT}$
CTNJUP	3D14:6/104	WORD
(TPRIME)	2F9:23/265	
(PHL)	2F9:4/265	$\overline{SG}$ & BSTOP & $\overline{RCHG}$
HESXRDS	2D9:3/42	WORD & OUT
(EBJ-F)	3E21:17/75	OUT
EEB-SO	2F7:17/106	EVH13
GO1US	3D19:20/162	EVH13
EVH12	2B14:25/44	$\overline{NJ = 3}$ & WORD
EVH21	2C11:17/43	WDOUT & $\overline{BSTOP}$
EVR10	3A14:22/39	EVH21 & $\overline{HR}$ & HES3
EVH13	3B32:24/59	$\overline{WDOUT}$
EVH14	2A20:7/10	HESX & RDS & BSTOP
VH13		
(EN-SAD)	2E11:3/93	
(EB-SO)	2E21:9/75	
(WRITE)	2E4:6/162	
HESXRDS	2D9:3/42	
EESIN-B	2E17:2/94	EVH14
EVH14	3A20:7/10	SG v RCHG
EVH21	2C11:17/43	$\overline{SG}$ & $\overline{RCHG}$
VH14		
(ECW-SAD)	2F3:25/115	
FRCE0	2F3:8/115	($\overline{RCHG}$ & SG) v
FRCE1	2F3:3/115	($\overline{SG}$ & RCHG)
(READ)	2E4:12/162	
(EBJ-K)	3E21:17/75	
(ESIN-B)	6D4:21/248	
EQN1P	3D2:26/82	SG
$\overline{GBKALL}$	3F6:21/61	
EEB-SO	2F7:17/106	RCHG & $\overline{SG}$



VH15: For SG, the third control word holds a link address and must be transferred to N.

For RCHG, the first control word is recharged from a copy of itself held in Z + 3.

VH16: For SG, the address accessed in VH15 is entered and this address updated by 1.

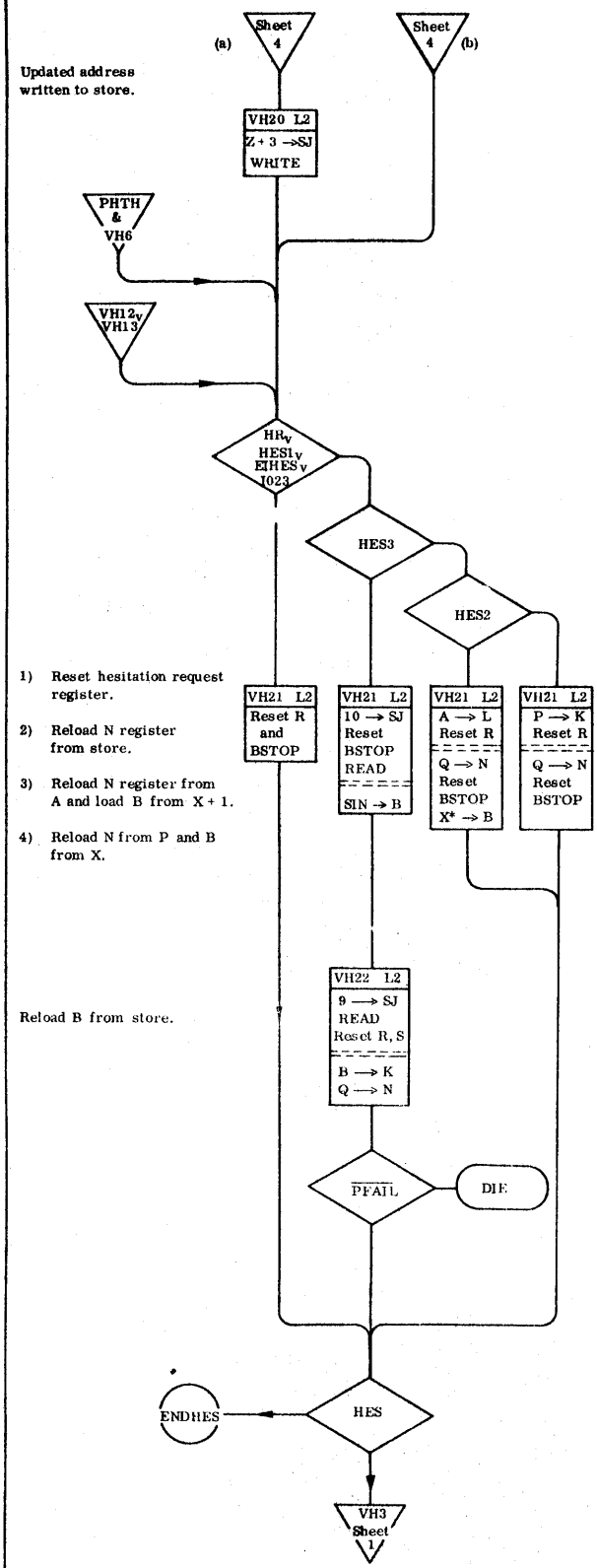
For RCHG the copy of the second control word held in Z + 2 is read to B.

VH17: The content of B is written to Z. For SG this will be the word read in VH16 and for RCHG it will be the copy of the second control word. Thus at this beat (for RCHG), both the control words have been recharged from their copies held in Z + 2 and Z + 3.

VH18: (SG only) the store is accessed at the address in N and the word read to B.

VH19: This word is written to Z + 1 and the address updated by 1.

VH15 SIGNAL	M.P.	CONDITIONS
(PCHECK)	3D15:7/112	
(EN-SAD)	2E11:2/93	$\overline{SG}$
FRCE0	2F3:8/115	$\overline{SG}$
(READ)	2E4:12/162	
(CB-SO)		
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3EF:4/62	SG
(EBYZ-K)	3F7:25/62	
EQAQ-N	3E1:2/83	
EQRX-N	3E1:7/83	
EQYZ-N	6D6:26/83	
EQ-N	3E1:8/83	
EESIN-B	2E17:2/94	
GNKIP	3D9:10/63	
ENKALL	3F8:7/64	
VH16		
(PCHECK)	3D15:7/112	
(ECW-SAD)	2F3:25/115	$\overline{SG}$
FRCE1	2F3:3/115	$\overline{SG}$
(ESIN-B)	6D4:21/248	
(READ)	2E4:12/162	
RESFL	2D7:6/32	DORLF & $\overline{CPR}$ & $\overline{EXEC}$
(EN-SAD)	2E11:3/93	
(ENAJ-K)	3D8:25/64	
(ENKQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/64	
(ENYZ-K)	3D8:10/64	
PLUS 1	3D24:8/109	
EQNIP	3D2:26/82	
EQAQ-N	3E1:2/83	
EQRX-N	3E1:7/83	
EQYZ-N	6D6:26/83	
EQ-N	3E1:8/83	
EEB-SO	2F7:17/106	
VH17		
(PCHECK)	3D15:7/112	
(ECW-SAD)	2F3:25/115	
(EB-SO)	3E21:9/75	
(WRITE)	2E4:6/162	
EVH21	2C11:17/43	$\overline{SG}$
EVH10	3A14:22/39	$\overline{SG}$
EESIN-B	2E17:2/91	EVH21 & $\overline{HR}$ & HES3
		EVH18
VH18		
(EN-SAD)	2E11:3/93	
(ESIN-B)	6D4:21/248	
(READ)	2E4:12/162	
GNKIP	3D9:10/63	
ENKALL	3F8:7/64	
VH19		
(PCHECK)	3D15:7/112	
(ECW-SAD)	2F3:25/115	
(EB-SO)	3E21:9/75	
FRCE0	2F3:8/115	
FRCE1	2F3:3/115	
(READ)	2E4:12/162	
(ENAJ-K)	3D8:25/64	
(ENKQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/64	
(ENYZ-K)	3D8:10/64	
EQBIP	2D17:7/78	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
EQ-B	3D13:15/79	
(PLUS 1)	3D24:8/109	



COMMENTS	VH20 / SIGNAL	M.P.	CONDITIONS
	VH20		
	(ECW-SAD)	2F3:25/115	
	FRCE0	2F3:8/115	
	FRCE1	2F3:3/115	
	(EB-SO)	3E21:9/75	
VH20: Is the final beat of the scatter-gather sequence.	(WRITE)	2E4:6/162	
	GALALL	3D30:3/70	EVH21 & HES2
	EVH21	2C11:17/43	$\overline{\text{RESFL}}$
	EVR10	3A14:22/39	EVH21 & HR & HES3
			EVH21 & I023
	EESIN-B	2E17:2/94	EVH21
	VH21		
	(FSAD10)	2F10:9/112	
	FRCE1	2F3:3/115	
	FRCE3	2F3:6/115	
	(VR10)	3A27:12/51	HES3 & $\overline{\text{HR}}$
	(ESIN-B)	6D4:21/148	
	(READ)	2E4:12/162	
	(EPAJ-K)	3E9:3/66	} I023
	(EPKQ-K)	3E9:5/66	
	(EPRX-K)	3F9:25/66	
	(EPYZ-K)	3F9:23/66	
	(EAAQ-L)	3F33:25/72	} HES2
	(EAAQ-L*)	3F33:23/72	
	(EASX-L)	3F33:7/72	
	(EAR-L)	3F33:21/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	EHX-B	3F14:18/87	I047
	EHX*B	3F18:18/80	HES2
	EQNIP	3D2:26/82	} I023_{V}HES2
VH21: The B and N registers are reloaded from a copy of their content at the time of entry to the hesitation sequence. The hesitation priority-race bistables are set by GHESPR.	EQAQ-N	3E1:2/83	
	EQRX-N	3E1:7/83	
	EQYZ-N	3E1:16/83	
	EQ-N	3E1:8/83	
	VH21		
	$\overline{\text{GHESPR}}$	2E1:9/140	I023_{V}HES21
	$\overline{\text{GBKALL}}$	3F6:21/61	EVH22
	EVH22	3A32:4/59	VR10
	ENDHES	2C13:25/46	$\overline{\text{VR10}}$ & $\overline{\text{HES}}$
VH22: For certain orders, B is written to store (rather than an accumulator) at the time of the hesitation and this is re-loaded in VH22.	**VH22**		
	(PCHECK)	3D15:17/112	
	(FSAD9)	2F10:6/112	
	FRCE3	2F3:6/115	
	FRCE0	2F3:8/115	
	(ESIN-B)	6D4:21/248	
	(READ)	2E4:12/162	
	$\overline{\text{EQNIP}}$	3D2:26/82	
	$\overline{\text{EQAQ-N}}$	3E1:2/83	
	EQRX-N	3E1:7/83	
	EQYZ-N	3E1:16/83	
	EQ-N	3E1:8/83	
	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3F7:24/62	
	(EBNP-K)	3F7:2/62	
	(EBQ-K)	3F7:23/62	
	(EBRX-K)	3F7:4/62	
	(EBYZ-K)	3F7:25/62	
	GHESPR	2E1:9/140	
	EVH3	2A1:25/45	HES & $\overline{\text{TWCR}}$
HES: If another hesitation request is outstanding, the sequence is re-entered at VH3. Otherwise exit occurs and the bistable ENDHES is set.	ENDHES	2C13:25/46	$\overline{\text{HR}}$

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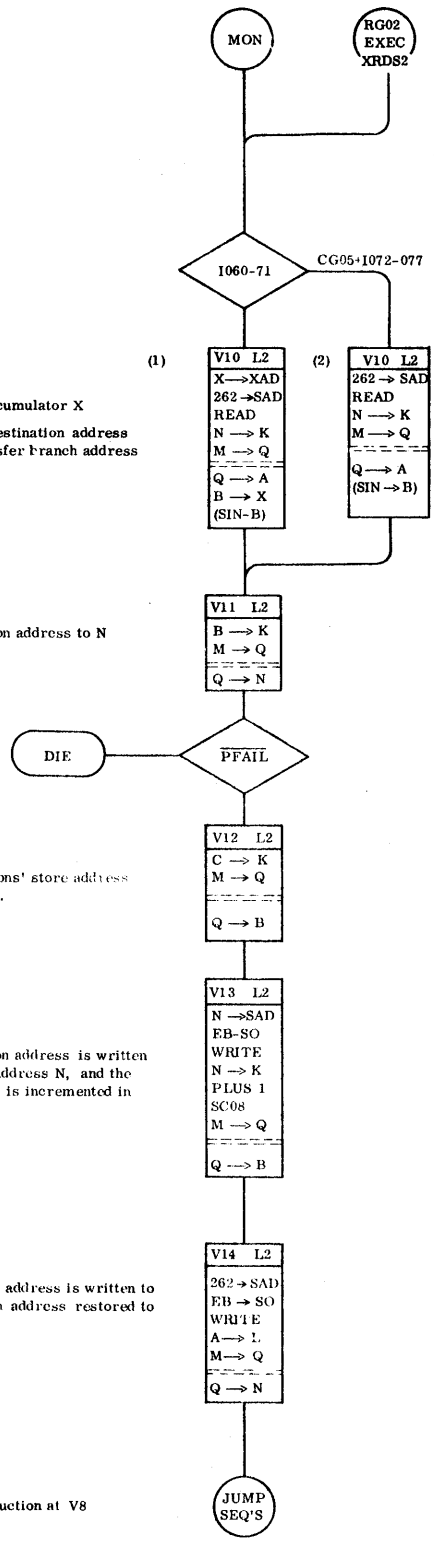


(1) Write B to accumulator X

(1) and (2) Read destination address from 262, transfer branch address to A.

Transfer destination address to N

The jump instructions' store address is transferred to B.

The jump instruction address is written to the destination address N, and the destination address is incremented in the mill.

The new destination address is written to 262, and the branch address restored to registerN.

Entry to jump instruction at V8

COMMENTS	V10 / SIGNAL	M.P.	CONDITIONS
Relevant signals active in previous beat: EV10, EESIN-B, ENKALL.	V10		
	(FSAD 262)	2F10:15/112	
	(ESIN-B)	6D4:21/248	
	(READ)	2E4:12/162	
	(ENAJ-K)	3D8:25/64	
	(ENKQ-K)	3D8:23/64	
	(ENRX-K)	3D8:17/64	
	(ENYZ-K)	3D8:10/64	
	EM-Q	3C14:23/167	
	ERX-XJ	3F20:4/R	
	EBAZ-X	3F25:8/90	CG06+1070:1
	EQAZ-A	3F29:23/81	
	EV11	2A6:16/14	
	GBKALL	3F6:21/61	
	V11		
	(PCHECK)	3D15:17/112	
	(EBAJ-K)	3F7:26/62	
	(EBKM-K)	3F7:24/62	
	(EBNP-K)	3E7:2/62	
	(EBQ-K)	3F7:23/62	
	(EBRX-K)	3E7:4/62	
	(EBYZ-K)	3F7:25/62	
	PFAIL	6A6:21/214	PGEN = RB24
	DIE	3B33:25/44	PFAIL. PCHECK INHPFL
	EM-Q	3C14:23/107	
	EQNIP	3D2:26/82	
	EQ-N	3E1:8/83	
	EQAQ-N	3E1:2/83	
	EQRX-N	3E1:7/83	
	EQYZ-N	3E1:16/83	
	EV12	3B11:10/15	
	V12		
	(ECAX-K)	3E10:10/67	
	(ECY-K)	3F10 25/67	
	(ECZ-K)	3F10:19/67	
	EM-Q	3C14:23/167	
	EQ-B	3D13:15/79	
	EQAJ-B	3D13:21/79	
	EQKM-B	3D13:22/79	
	EQNQ-B	3D13:24/79	
	EQRZ-B	3D13:23/79	
	EV13	2A18:5/16	
	EEB-SO	2F7:17/106	
	ENKALL	3F8:7/64	
	ESC08	3A6:24/17	
	V13		
	(EN-SAD)	2E11:3/93	
	(EB-SO)	3E21:9/75	
	(WRITE)	2E4:6/162	
	(ENAJ-K)	3D8:25/64	
	(ENKQ-K)	3D8:23/64	
	(ENRX-K)	3D8:17/64	
	(ENYZ-K)	3D8:10/64	
	(PLUS1)	3D24:8/109	
	(SC08)	2F10:22/112	
	EM-Q	3C14:23/167	
	EQ-B	3D13:15/79	
	EQAJ-B	3D13:21/79	
	EQKM-B	3D13:22/79	
	EQRZ-B	3D13:23/79	
	EV14	2A7:9/18	
	EEB-SO	2F7:17/106	
	GALALL	3D30:3/70	
	V14		
	(FSAD 262)	2F10:15/112	
	(EB SO)	3E21:9/75	
	(WRITE)	2E4:6/162	
	(EAAQ-L)	3F33:25/72	
	(EAR-L)	3F33:21/72	
	(EASX-L)	3F33:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	EM-Q	3C14:23/167	
	EQ-N	3E1:8/83	
	EQAQ-N	3E1:2/83	
	EQRX-N	3E1:7/83	
	EQYZ-N	3E1:16/83	
	EV8	3A21:12/11	

V10:

(1) The updated operand x, in B, is returned to accumulator X.

(1) & (2) The address in store, into which the store address of the successful jump instruction is to be stored, is read to B from absolute store location 262. The branch address (in register N from the jump instruction) is transferred to register A, leaving register N available for subsequent operations.

V11:

The destination address (in B, from 262) is transferred to N.

V12:

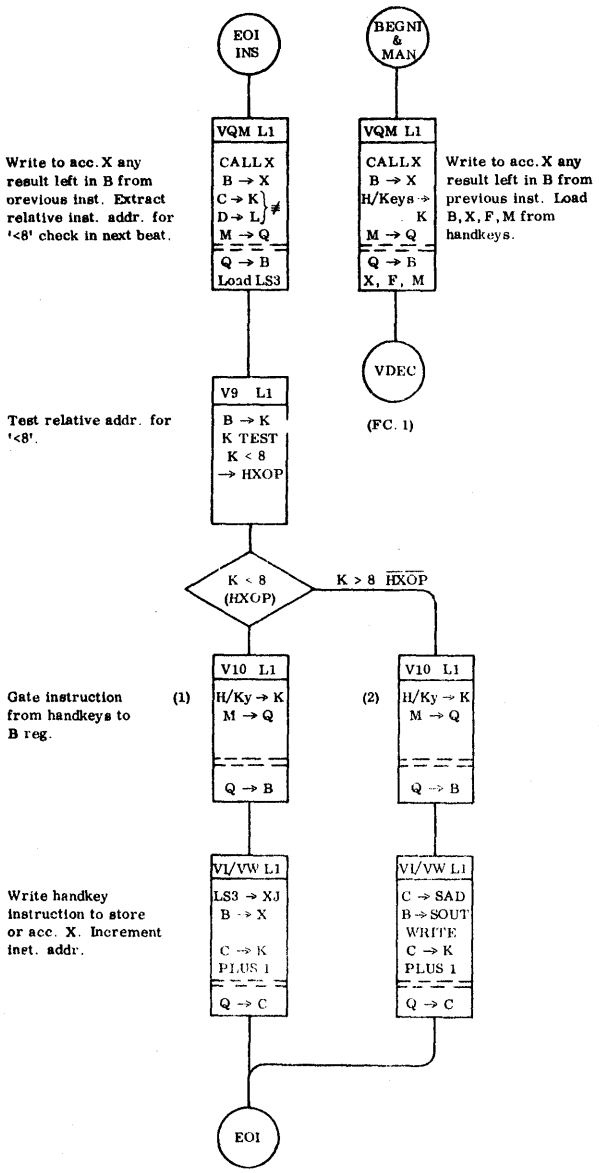
The address of the jump instruction (in C) is transferred to B.

V13:

The jump instruction address is written to store at the destination address N. The destination address is incremented in the mill (PLUS 1) and restored to register N so as to be available for monitoring of the next successful jump.

V14:

The updated destination address is written to 262, and the branch address (in A from V10) is restored to register N



COMMENTS

Relevant signals active in previous beat: MAN, INS,
EVQM if $\overline{HR}$ $\overline{RTI}$ $\overline{INTR}$ $\overline{I117}$ $\overline{I023}$
GDLA if INS
GCKALL if INS
ENEQV if INS

VQM:

Prime F Register (MAN only)
Prime F Register with *177 (Insert only). *117 effectively overwrites any previous instruction code. VDEC is not produced in INSERT. Thus, F177 is not decoded and therefore not acted upon in INSERT.
Address acc. from X Register and write B to X if required. Note that EBAZ - X or EBAZ - X* is made if previous instruction requires this action. The conditions for the production of these signals are decoded from the relevant instructions and appear on logic diagram WGH08/0095.

If MAN:

a) Load instruction set up on handkeys to K highway.

b) Load X, F and M registers.

c) VDEC in the Instruction Phase (FC. 1) is entered on completion of VQM.

If INSERT:

C to K
Datum to L
Instr. Addr. ≠ Datum

} The difference between the absolute address (in C) and Datum is the Relative Addr. which we wish to check for <8 in the next beat.

V9 is entered on completion of VQM.

V9: K < 8 generated in data flow if instr. address < 8.
HXOP = Accumulator operation.

V10: Both (1) and (2) load the instruction set up on h/keys to the B Register.

(1) Initiates signals for accumulator operation.

(2) Initiates signals for store operation.

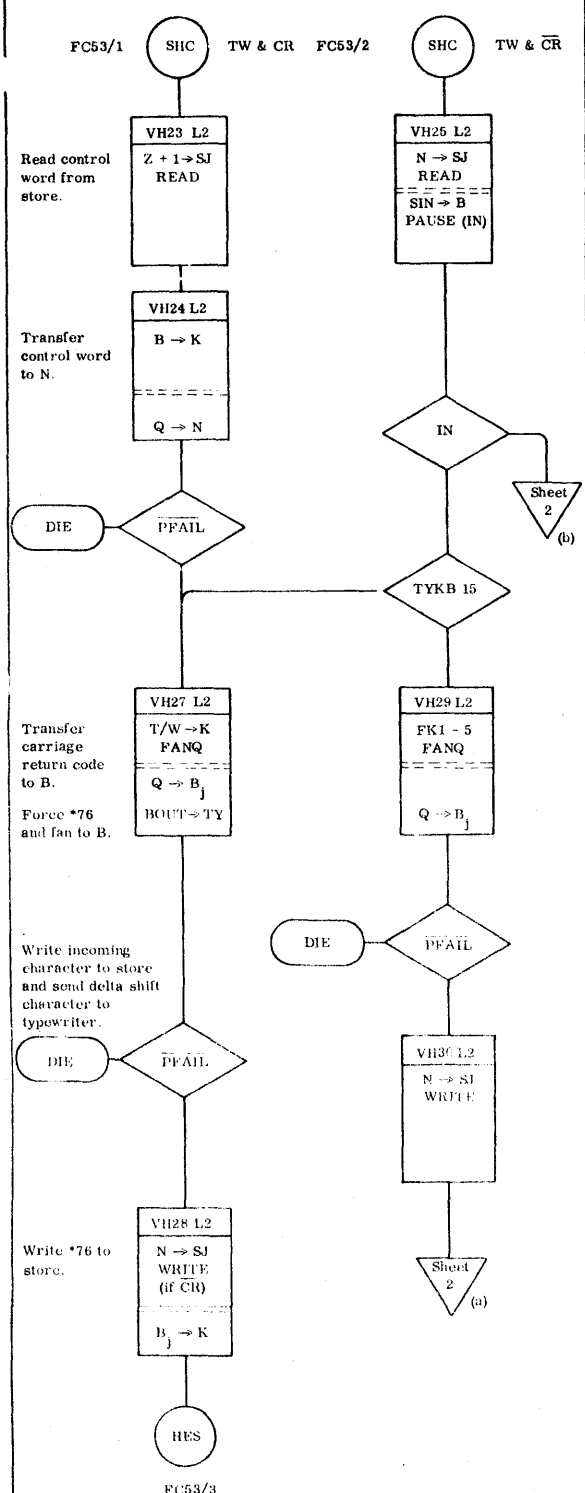
VI/VW:

(1) Accumulator addressed from LS3 reg. and B → X.

(2) Store addressed from C Register and B written to store.

Instruction address (in C reg.) incremented in mill and returned to C.

VQM SIGNAL	MP	CONDITIONS
GXFM	2D16:7/60	MAN
F177F	3D14:25/104	INS
ERX-XJ	3F20:4/89	
EBAZ-X	3F25:8/90	EBAZ-X*
EBAZ-X*	3F25:6/90	EBAZ-X
EHS1-K	6D4:16/248	MAN
EHS2-K	2C2:9/141	MAN
EM-Q	3C14:23/167	
EQ-BIP	2D17:7/78	
EQ-B	3D13:15/79	
$\overline{EQAJ-B}$	3D13:21/79	
$\overline{EQKM-B}$	3D13:22/79	
$\overline{EQNQ-B}$	3D13:24/79	
$\overline{EQRZ-B}$	3D13:23/79	
(ECAX-K)	3E10:10/67	
(ECY-K)	3F10:25/67	
(ECZ-K)	3F10:19/67	INS
(ED-L:1)	3E21:25/75	
(ED-L:2)	3E21:22/75	
(NEQV)	3E21:12/75	
EM-LS3	3E19:3/91	
$\overline{EV9}$	2A4:9/12	INS
$\overline{GBKALL}$	3F6:21/61	
EVDEC	3A11:12/2	MAN
V9		
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3F7:24/62	
(EBNP-K)	3E7:2/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3E7:4/62	
(EBYZ-K)	3F7:25/62	
K < 8	6A16:20/179	If addr. < 8
SHXOP	2E17:21/94	INS
(HXOP)	3C26:23/160	SHXOP. K < 8
EV10	2A5:9/13	INS
V10		
(EHS1:K*)	2E2:6/141	INS
(EHS2:K)	2E2:9/141	INS
$\overline{EM-Q}$	3C14:23/167	
$\overline{EQ-BIP}$	2D17:7/78	
$\overline{EQ-B}$	3D13:15/79	
$\overline{EQAJ-B}$	3D13:27/79	
$\overline{EQKM-B}$	3D13:22/79	
$\overline{EQNQ-B}$	3D13:24/79	
$\overline{EQRZ-B}$	3D13:23/79	
EVW	3B3:18/3	INS
EVI	3A16:12/13	INS
EEC-SAD	2F6:18/92	INS. $\overline{HXOP}$
EEB-SO	2F7:17/106	$\overline{HXOP}$
VI/VW		
EC-SAD	3E10:9/167	$\overline{HXOP}$
EB-SO	3E21:9/75	
WI	C5D1:21/285	
LR	C5D1:22/285	
ELS3-XJ	3F19:6/91	HXOP
EBAZ-X	3F25:8/90	HXOP
(ECAX-K)	3E10:10/67	
(PLUS 1)	3D24:8/109	
EM-Q	3C14:23/167	
EQAX-C	3E17:12/85	$\overline{RESFL}$
EOI	2A16:15/41	



VH23: The m.s. half of the control word is read from store to B.

VH25: Data read for outward. Data dest. access for inward word containing the *77 or *76/*32 is made available in B. Entry will be made to VH31 if the transfer is outwards (i.e. $\overline{IN}$). DELTA is set for an inwards transfer (if not already set).

VH24: The address parts of the control word are transferred to Register N.

TYKB 15 indicates that the operator's key pressed is in delta shift if bit 15 of the mill equals 1.

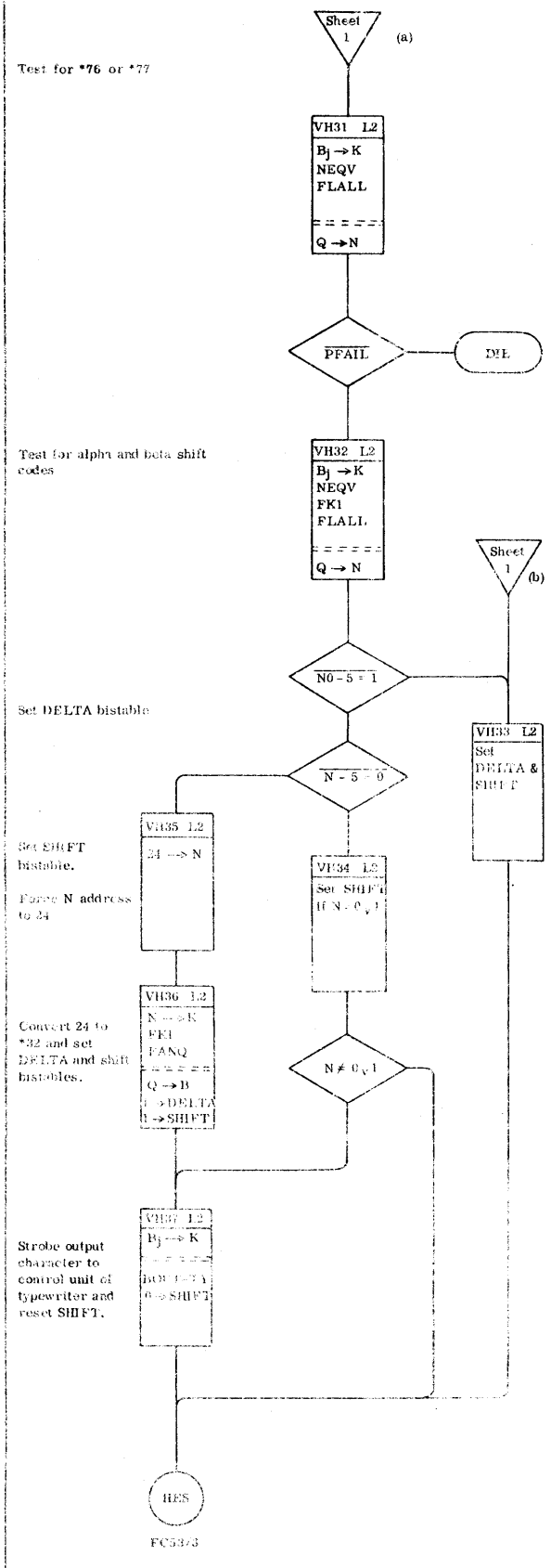
VH27: The carriage return code is written into the destination word.

VH29: Bits 1 to 5 of K are forced to all 1's to give *76. This is then fanned to all character positions of B.

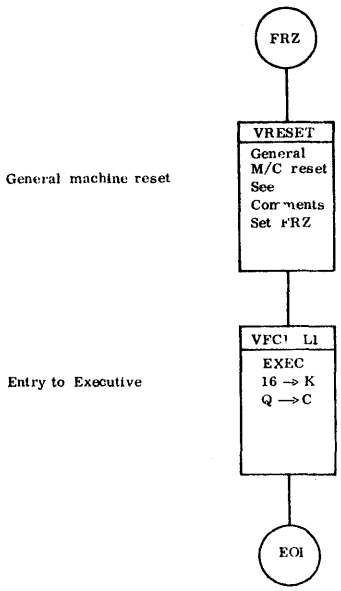
VH30: *76 is written to store.

VH28: Exit will occur after VH28 via VH21 of the SHC sequence.

VH23 SIGNAL	MP	CONDITIONS
(ECW-SAD)	2F3:25/115	
FRCE0	2F3:8/115	
(ESIN-B)	6D4:21/248	
(READ)	2E4:12/162	
RESFL	2D7:6/32	DORLF & $\overline{EXEC}$ & $\overline{CPR}$
GBKALL	3F6:21/61	
VH24		
(PCHECK)	3D15:17/112	
$\overline{EQNIP}$	3D2:26/82	
$\overline{EQAQ-N}$	3E1:2/83	
EQRX-N	3E1:7/83	
EQYZ-N	3E1:16/83	
EQ-N	3E1:8/83	
EBAJ-K	3F7:26/62	
EBKM-K	3F7:24/62	
EBNP-K	3E7:2/62	
EBQ-K	3F7:25/62	
EBRX-K	3E7:4/62	
EFYZ-K	3F3:25/62	
EVH27	2A1:13/75	
VH27		
EMFAN	3F28:17/107	
EQ-BJ	3E18:9/80	
EQ-B	3E13:15/79	
BOUT-TY	2D8:7/252	TYES & $\overline{PHC}$
(DELTA)	2E8:13/252	$\overline{TYOUT}$
EEB-SO	2F7:17/106	
VH28		
(EN-SAD)	2E11:3/93	
(EB-SO)	3E21:9/75	$\overline{CR}$
(WRITE)	2E4:6/162	
EBJ-K	3E21:17/75	
HESXRDS	2D9:3/42	
EVH21	2C11:17/43	BSTOP
EVR10	3E14:22/39	EVH21 & HES3 & $\overline{HR}$
VH25		
(EN-SAD)	2E11:3/93	
(ESIN-B)	6D4:21/248	
(READ)	2E4:12/162	
(PAUSE)	2E10:7/173	$\overline{OUT}$
RESFL	2D7:6/32	DORLF & $\overline{EXEC}$ & $\overline{CPR}$
EVH27	2A1:13/75	$\overline{OUT}$ & $\overline{DELTA}$
EVH29	3C14:15/167	$\overline{OUT}$ & $\overline{DELTA}$
EVH31	3A33:21/59	OUT
FLALL	3F32:18/76	
EENARX-L		EVH31
EEBJ-K	3D7:17/71	
ENEQV	3D20:17/107	
VH29		
($\overline{FK1}$)	3D5:8/68	
($\overline{FK2}$)	3D5:24/68	
($\overline{FK3}$)	3D5:22/68	
($\overline{FK4}$)	3D5:26/69	
($\overline{FK5}$)	3D5:4/69	
EMFAN	3F28:17/107	
EQ-BJ	3E18:19/80	
EQ-B	3D13:15/79	
(PCHECK)	3D15:17/112	
EEB-SO	2F7:7/106	
VH30		
(EN-SAD)	3E11:3/93	
(WRITE)	2E7:6/162	
(EB-SO)	2E21:9/75	
RESFL	2D9:6/32	DORLF & $\overline{EXEC}$ & $\overline{CPR}$
HESXRDS	2D9:3/42	
EVH21	2C11:17/43	$\overline{BSTOP}$
EVR10	3A14:22/39	EVH21 & HES3 & $\overline{HR}$
FLALL	3F32:18/96	



COMMENTS	VH31 SIGNAL	M.P.	CONDITIONS
	VH31		
VH31:	(EBJ-K)	3E21:17/75	
	(EAAQ-L)	3F23:25/72	
A test is made for *76 and *77 (NEWLINE code).	(EAAQ-L*)	3F33:23/72	
	(EAR-L)	3F33:21/72	
	(EASX-L)	3F23:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	(ENAAQ-L)	3C14:7/107	
	(ENARX-L)	3D31:5/73	
	(ENAYZ-L)	3D31:75/73	
	(NEQV)	3E21:12/75	
	(EQ-N)	3E1:8/83	
	(EQAQ-N)	3E1:2/83	
	(EQRX-N)	3E1:7/83	
	FLALL	3F32:18/76	
	EENARX-L	3E33:20/102	
	ENEQV	3D20:17/107	
	EEBJ-K	3D7:17/71	
	VH32		
VH32:	(EBJ-K)	3E21:17/75	
	(ENAAQ-L)	3C14:7/107	
A test is made for *74 and *75 (alpha or beta shift code) and, if detected, exit is made via VH34 and VH21 of the SHC	(ENARX-L)	3D31:5/73	
	(ENAYZ-L)	3D31:25/73	
	(EAAQ-L)	3F33:25/72	
	(EAAQ-L*)	3F33:23/72	
	(EAR-L)	3F33:21/72	
	(EASX-L)	3F33:7/72	
	(EAY-L)	3F33:5/72	
	(EAZ-L)	3F33:3/72	
	(FK1)	3D5:8/68	
	(NEQV)	3E21:12/72	
	EQ-N	3E1:8/83	
	EQAQ-N	3E1:2/83	
	EQRX-N	3E1:7/83	
	EVH33	3A33:8/59	N0 - 5 = 1
	EVH34	3B33:13/44	N0 - 5 = 1 & N0 - 5 = 0
	EVH35	3A32:21/59	N0 - 5 = 0
VH33:	VH33		
DELTA is set to indicate that the following character is in delta shift code. SHIFT is also set to prevent printing action.	TYK15	2E8:5/252	
	(SHIFT)	2E8:20/252	
	(DELTA)	2E8:13/252	
VH34:	EVH21	2C11:17/43	BSTOP
SHIFT is set to prevent printing of the alpha or beta shift codes.	EVR10	3A14:22/39	EVH21 & HES3 & IIR
VH35:	VH34		
N is forced to 24 preparatory to the formation of *32 in VH36.	(SHIFT)	2E8:20/252	
VH36:	EVH37	2B1:12/50	N0 - 5 = 0 & N0 - 5 = 1
SHIFT is made active to ensure that there is no typewriter printing action at this stage.	EVH21	2C11:17/43	BSTOP
	EVR10	3A14:22/39	EVH21 & HES3 & IIR
	VH35		
VH37 (from VH36)	FH24	3D39:1/113	
BOUT-TY gates DELTA and *32 (on the BOUT highway) to set NL (newline), and also resets the IIR bistable.	VH36		
	(ENAAQ-K)	2D8:29/67	
*32 (L.s. 6 bits of K) is strobed to the 6-bit control buffer register of the typewriter which can then proceed with the carriage return/new line operation. The sequence exits via VH21 of the SHC sequence as both SG and RCHG bits will be zero.	(FK1)	3D5:8/68	
	EMFAN	3F28:9/107	
	EQBIP	2D17:7/78	
	EQAJ-B	3D13:21/79	
	EQKM-B	3D13:22/79	
	EQNQ-B	3D13:24/79	
	EQRZ-B	3D13:23/79	
	EQ-B	3D13:15/79	
	(DELTA)	2E8:13/252	
VH37: (from VH34)	EVH37	2B1:12/50	
	EEBJ-K	3D7:17/71	
as above but for *32 read "character read from typewriter".	VH37		
	(EBJ-K)	3E21:17/75	
	BOUT-TY	2D8:7/252	TYES & PHC
	EVH21	2C11:17/43	BSTOP
	EVR10	3A14:22/39	EVH21 & HES3 & IIR



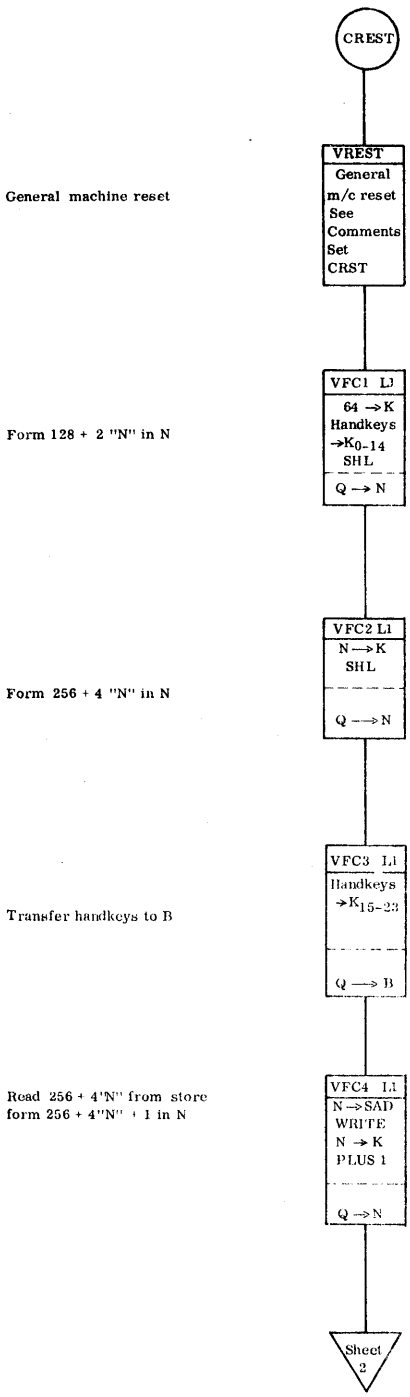
COMMENTS	VRESET / SIGNAL	MP	CONDITIONS
	Various bistables are reset in this beat - see Comments.		
	(FRZ)	2E10:12/143	
	VFC1		
Operation of the FREEZE key generates KFRZ, setting the FRZ bistable. Various registers and bistables in the system are reset and an entry is made to Executive at store location 16. The activity in the machine is as follows:	(FK4) (EXEC) EQCALL EQAX-C EQZ-C	3D5:26/69 2C1:23/144 3A17:2/85 3E17:12/85 3E17:16/85	$\overline{PM}$

VRESET:

RESETS: EXEC, RTINT, EIHES, I117L, I023L, INT, HES, PM, INTMOVE, RP1, ASTAT, FLG1, FLG2, FLG3, FLG4, ZS, ZSINT, BSTOP, DUMMYOV, HXIN, HXOP, FORCRT1, RTI bistables; data flow registers P, D and G; I174PAC, MILLRDY and real time clock; store control bistables, SHC, C, L, No, T, A and B bistables and SR64/65; PIF control and status bistables; typewriter control bistables.

VFC1: At the start of this beat the machine clock is restarted. EXEC is set and entry made to Executive at address 16.

The FREEZE sequence is used where it is required to place the machine in a suitable condition for restarting after a fault has been detected.



COMMENTS

Operation of the CREST key generates KCRST, setting the CRST bistable. Various registers and bistables in the system are reset, these being:

VRESET:

Resets: EXEC, RTINT, EIHES, I117L, ZS, I023L, INT, HES, PM, INTMOVE, RPT, ASTAT, FLG1, FLG2, FLG3, FLG4, ZSINT, BSTOP, DUMMYOV, HXIN, HXOP, FORCRTI and RTI bistables; data flow registers P, D and G; I174PAC, MILLRDY and real time clock; store control bistables, SHC, C, L, No, T, A and R bistables and SR64/65; PIF control and status bistables; typewriter control bistables.

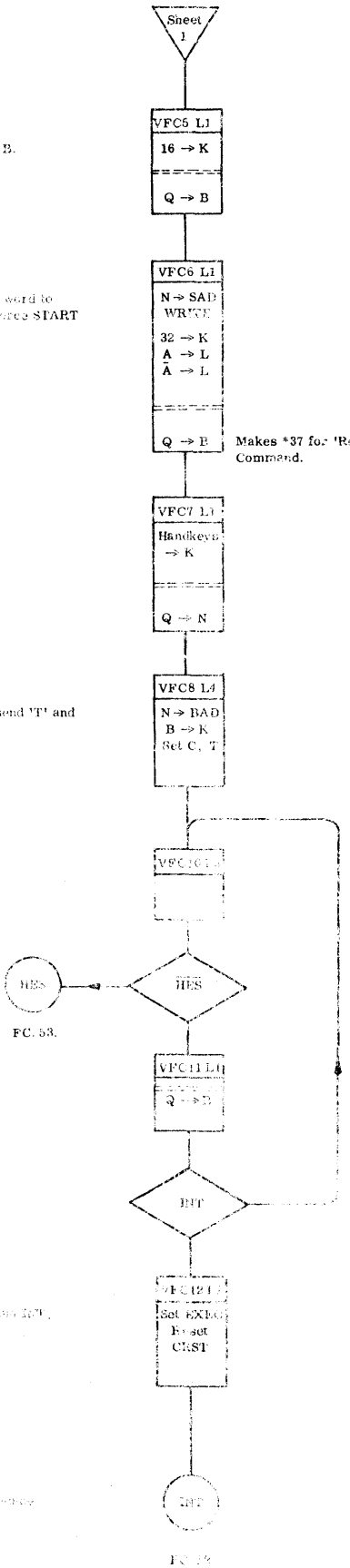
VFC1: The address set up on the handkeys ("N") is gated to the mill along with the constant 64. The mill output is then shifted one place left, effectively multiplying the mill output by 2 to give 128 + 2"N", which is strobed via Q to N.

VFC2: The content of N is again shifted left one place to give 256 + 4N.

VFC3: The style field of the instruction on the handkeys is strobed to bits 15 to 23 of B and bits 0 to 14 are cleared.

VFC4: The style field in B15 to 23 is written to address 256 + 4"N" in store to form part of the first control word. 256 + 4"N" + 1 is then formed in N to give the address for the second control word.

VRESET / SIGNAL	M.P.	CONDITIONS
Various bistables are reset in this beat - see Comments (CRST).		
EVFC1		
VFC1		
(FK6)	3E5:2/69	
SHL	3D33:8/102	
EQNIP	3D2:26/82	
EQAQ-N	3E1:2/83	
EQRX-N	3E1:7/83	
EQYZ-N	3E1:16/83	
EVFC2	3A26:18/49	
GNKIP	3D9:10/63	
ENKALL	3F8:7/64	
ENKQ-K	Sheet 64	
VFC2		
(ENAJ-K)	3D8:25/64	
(ENKQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/64	
(ENYZ-K)	3D8:10/64	
SHL	3D33:8/102	
EQNIP	3D2:26/82	
EQAQ-N	3E1:2/83	
EQRX-N	3E1:7/83	
EQYZ-N	3E1:16/83	
VFC3		
EQBIP	2D17:7/78	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D12:23/79	
EQ-B	3D13:15/79	
EEB-SO	2F7:17/106	
ENKALL	3F8:7/64	
EENKQ-K	Sheet 64	
VFC4		
(EN-SAD)	2E11:3/93	
(EB-SO)	5E21:9/75	
(WRITE)	2E4:6/162	
(ENAJ-K)	3D8:25/64	
(ENKQ-K)	3D8:23/64	
(ENRX-K)	3D8:17/64	
(ENYZ-K)	3D8:10/64	
(PLUS 1)	3D24:8/109	
EQNIP	3D2:26/82	
EQAQ-N	3E1:2/83	
EQRX-N	3E1:7/83	
EQYZ-N	3E1:16/83	



VFC5: *20 (≡16) is formed in Register B by forcing the K highway (bit 4) to 1. This will form in B the first store address for the incoming bootstrap. Bits 0-14 of B are cleared.

VFC6: The address (16) formed in VFC5 is written to 256 + 4N + 1 and the constant 31 (*37) is formed in B. This is the START code for the input peripheral.

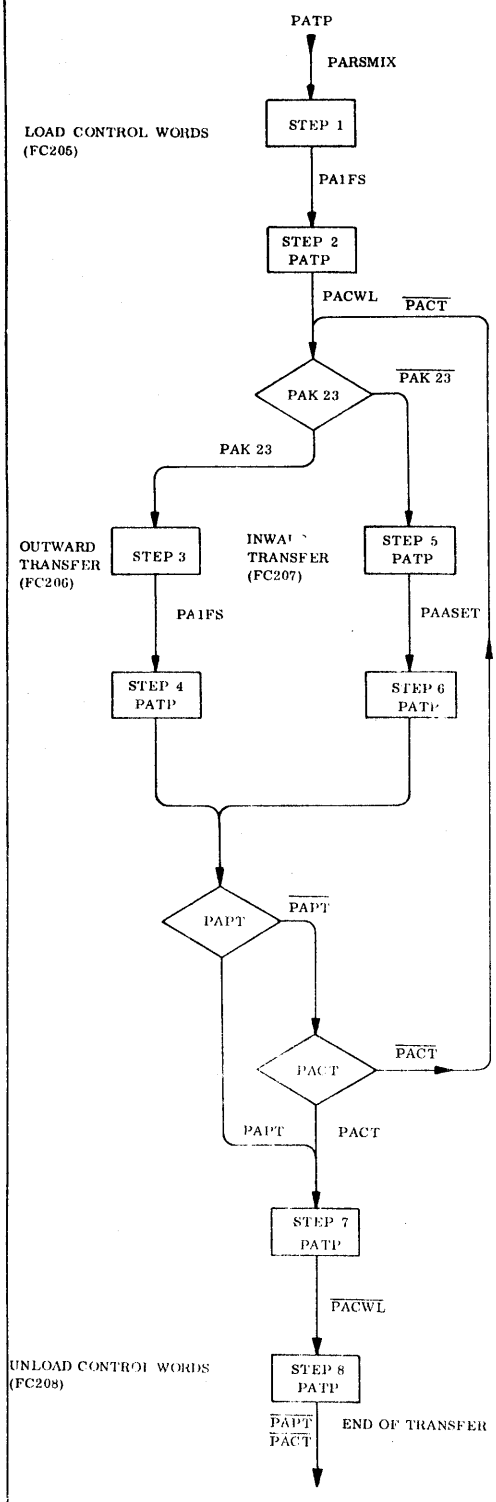
VFC7: The control word from the handkeys is again strobed to Register N, giving the peripheral address 'N' in the l. s. 6 bits of that register.

VFC8: The input device is addressed via the BAD lines from Register N, raising the peripheral's A line, and the C line is raised. This means that information on the Do lines will be treated as a control code rather than data.

VFC11: The B Register is cleared as the peripheral will have responded to the control code by this time. If the device has not generated an interrupt by this time, VFC10 and VFC11 are cycled to form a waiting loop. Entry is made to VFC12 when the device interrupts.

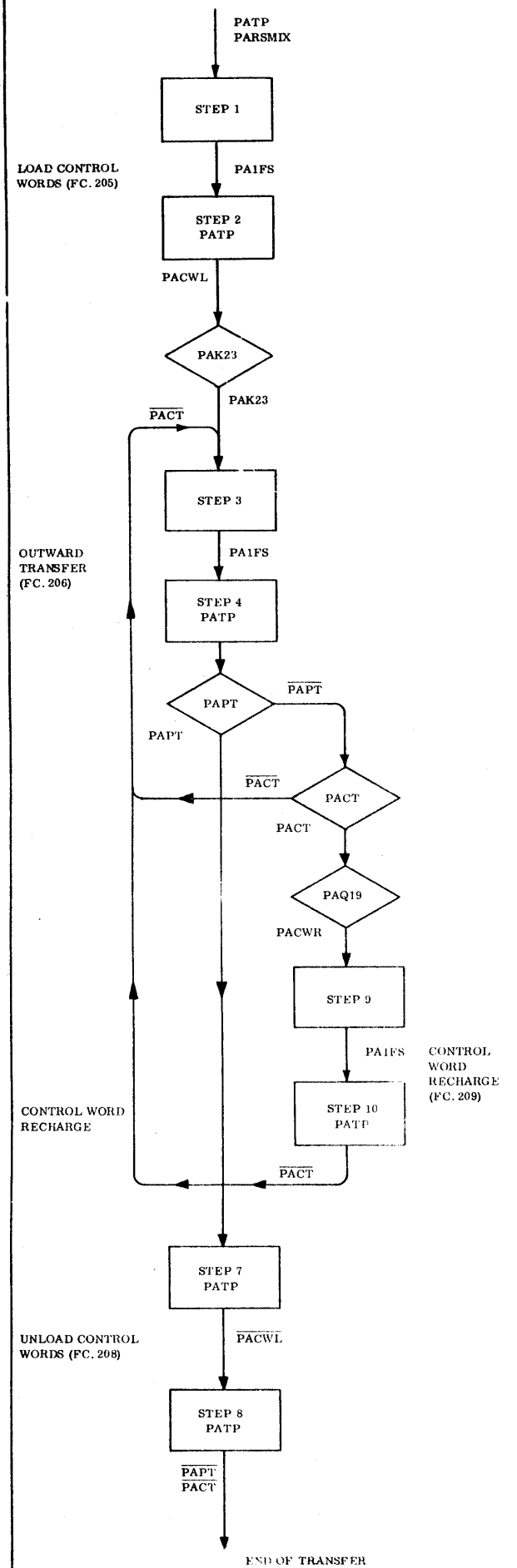
VFC12: An entry to Executive is now required and the EXEC bistable is set to accomplish this. CRST is reset and INT is set. The sequence then enters the interrupt sequence at V21 (FC52).

VFC5 SIGNAL	M.P.	CONDITIONS
(FK4)	3D5:26/69	
EQBIP	2D17:7/78	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
EQ-B	3D13:15/79	
EEB-SO	2F7:17/106	
FLALL	3F32:18/76	
EENARX-L	3E33:20/102	
VFC6		
(EH-SO)	3E21:9/75	
(WRITE)	2E4:6/162	
(FK5)	3D5:4/69	
(EAAQ-L)	3F33:25/72	
(EAAQ-L*)	3F33:23/72	
(EAR-L)	3F33:21/72	
(EASX-L)	3F33:7/72	
(EAY-L)	3F33:5/72	
(EAZ-L)	3F33:3/72	
(ENAAQ-L)	3C14:7/167	
(ENAIX-L)	3D31:5/73	
(ENAYZ-L)	3D31:25/73	
EQBIP	2D17:7/78	
EQAJ-B	3D31:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
EQ-B	3D13:15/79	
GBKALL	3F6:21/61	
VFC7		
EQNIP	3D2:26/82	
EQAQ-N	3E1:2/83	
EQRX-N	3E1:7/83	
EQ-N	2E1:8/83	
GBKALL	3F6:21/61	
EVFC8		
GODELAY		
GOST2	3D21:21/163	
GDLA	3F31:18/74	
VFC8		
EN-BAD	3E28:20/108	
(PEC)	2F9:6/265	
(PHT)	2F9:2/265	
(EBAJ-K)	3F7:26/62	
(EBKM-K)	3E21:15/62	
(EBNP-K)	3F17:24/62	
(EBQ-K)	3F7:23/62	
(EBRX-K)	3E7:4/62	
(EBYZ-K)	3E7:25/26	
EVFC10	2B/:13/50	
GOTUS	3D19:20/162	
VFC		
EVFC11		
VFC11		
[illegible]	2D17:7/78	
EQAJ-B	3D13:21/79	
EQKM-B	3D13:22/79	
EQNQ-B	3D13:24/79	
EQRZ-B	3D13:23/79	
EQ-B	3D13:15/79	
EVFC12	3B23:8/17	
VFC12		
(PXEC)	2C1:27/164	PM
GINT1	3C27:23/147	
SV21	3B14:26/26	



SIGNAL	COMMENTS
PATP	Priorities are strobed at PATP locations on the chart to allow time-sharing between peripherals and between data buffers.
PARSMIX	The R line of the priority peripheral is active and the R stat is set. STEP 1 is entered.
STEP 1	Load control word 1 (CW1)
PA1FS	1FS Stat set. Allows entry to STEP 2
STEP 2	Load control word 0 (CW0)
PACWL	CWL Stat set. Allows entry to Step 3 or 5
$\overline{\text{PACT}}$	Permits transfer of the next word.
$\overline{\text{PAK 23}}$	Style bit 23 = 0 Inward Transfer
PAK23	Style bit 23 = 1 Outward Transfer
	Outward Transfer
STEP 3	Read data from store into data buffer. Update CW1.
PA1FS	1FS Stat set. Allows entry to Step 4.
STEP 4	Update CW0
	Inward Transfer
STEP 5	CW0 Updated. Word transferred from peripheral to data buffer.
PAASET	A stat set. Allows entry to Step 6.
STEP 6	Store write cycle initiated. Data word transferred to store. CW1 Updated.
PAPT	If peripheral terminates the transfer, entry is made direct to Steps 7 and 8.
PACT	CT stat sets when one block of data words have been transferred. Allows entry to Steps 7 and 8.
STEP 7	Unload CW1
$\overline{\text{PACWL}}$	CWL Stat unset. Allows entry to Step 8.
STEP 8	Unload CW0
$\overline{\text{PATP}}$	PT stat unset } Allows entry to Step 1
$\overline{\text{PACT}}$	CT stat unset } For next block transfer.

SIGNAL	M.P	E.D REF WGHOJFN
PATP	1B20:25	13 OT
PARSMIX	1C21:9	25 QI
PA1FS	1A17:15	2 VN
PACWL	1D13:16	10 IF
PACT	1D12:16	10 VF
PAK23	1A16:20	84 VP
PAASET	1E28:16	21 IP
PAPT	1D11:16	10 IP
$\overline{\text{PACT}}$	1D12:12	10 TD
$\overline{\text{PAK23}}$	1A4:12	81 SR
$\overline{\text{PACWL}}$	1D13:12	10 GD
$\overline{\text{PAPT}}$	1D11:12	10 GN



SIGNAL	COMMENTS
PAPT	Priorities are strobed at PATP locations on the chart to allow time sharing to take place between peripherals and between data buffers.
PARSMIX	The R line of the priority peripheral is active and the R stat. is set. STEP 1 is entered.
STEP 1	Load control word 1 (CW1).
PA1FS	1FS stat. set. Allows entry to STEP 2.
STEP 2	Load control word 0.
PACWL	CWL stat. set - allows entry to STEP 3.
PAK23	Style bit 23 = 1. Outward transfer.
$\overline{\text{PACT}}$	Permits transfer of the next word.
STEP 3	Read data from store into data buffer. Update CW1.
PA1FS	1FS stat. set. Allows entry to STEP 4.
STEP 4	Update CW0.
$\overline{\text{PAPT}}$	The peripheral has not terminated the transfer as sufficient repetitions of the data block have not yet been made.
PAPT	Peripheral terminates. Enter STEP 7.
$\overline{\text{PACT}}$	When the CT stat. is in the unset state at the end of a STEP 3, 4 sequence, the sequence is re-entered because a complete block has not yet been transferred to the peripheral, but when the stat. unsets at the end of a STEP 9, 10 sequence, entry to the STEP 3, 4 sequence is made to initiate a repeat transfer of the previous block.
PACT	Count terminates. End of block. Enter CWR routine.
$\overline{\text{PACWR}}$	Style bit 19 = 0. Transfer not CWR mode.
PACWR	Style bit 19 = 1. Transfer is CWR mode. Enables entry to STEP 9.
STEP 9	CW1 is replaced by CW3.
PA1FS	1FS stat. set. Allows entry to STEP 10.
STEP 10	CW0 is replaced by CW2.
$\overline{\text{PACT}}$	CT stat. unset. Allows entry to STEP 3. Repeat the block transfer.
STEP 7	Unload CW1.
$\overline{\text{PACWL}}$	CWL stat. unset. Allows entry to STEP 8.
STEP 8	Unload CW0.
$\overline{\text{PAPT}}$ $\overline{\text{PACT}}$	PT stat. unset.) Allows entry to STEP 1 CT stat. unset.) for next block transfer.

SIGNAL	M.P.	E.D. REF. WCHØ3FN
PARSMIX	1C21:9	25 QI
PA1FS	1A17:15	2 VN
PACWL	1D13:16	10 IF
PAK23	1A16:20	84 VP
PACT	1D12:16	10 VF
PAPT	1D11:16	10 IP
$\overline{\text{PACWR}}$	1A21:16	120 TP
$\overline{\text{PACT}}$	1D12:12	10 TD
$\overline{\text{PAPT}}$	1D11:12	10 GN
$\overline{\text{PACWL}}$	1D13:12	10 GD

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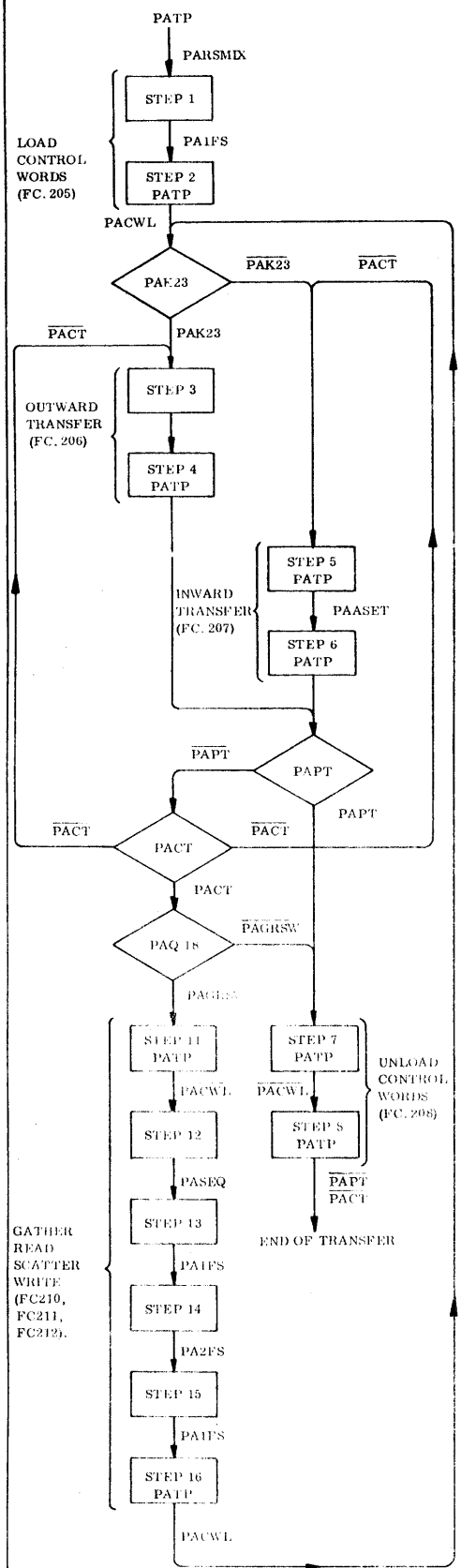
ICL	1904 A/S 1903T	P.A.C. OUTWARD TRANSFER WITH C.W.R.	FC 201



FUNCTION	COMMENTS
PATP	Priorities are strobed at PATP locations on the chart to allow time sharing to take place.
PARSMIX	Priority peripheral has raised its R line. Allow entry to STEP 1.
STEP 1	Load Control Word 1 (CW1).
PA1FS	1FS stat. set. Allows entry to STEP 2.
STEP 2	Load Control Word 0 (CW0).
PACWL	CWL stat. set. Allows entry to STEPS 3 or 5.
$\overline{\text{PAK23}}$	Style bit 23 = 0. Inward Transfer.
PAK 23	Style bit 23 = 1. Outward Transfer.
$\overline{\text{PACT}}$	Permits transfer of next word.
	OUTWARD TRANSFER
STEP 3	Read data from store into data buffer. Update CW1.
PA1FS	1FS stat. set. Allows entry to STEP 4.
STEP 4	Update CW0.
	INWARD TRANSFER
STEP 5	Update CW0. Word transferred from peripheral to data buffer.
PAASET	A stat. set. Allows entry to STEP 6.
STEP 6	Store write cycle initiated. Data word transferred to store. Update CW1.
$\overline{\text{PAPT}}$	Peripheral terminate has not occurred.
PAPT	Peripheral terminate has occurred. Allows entry to STEP 7.
$\overline{\text{PACT}}$	Count terminate has not occurred. Transfer continues.
PACT	Count terminated. Enter GRSW step sequence unless transfer is completed i.e. unless PAQ 18 has been changed to an '0' bit.
$\overline{\text{PAGRSW}}$	Style bit 18 = 0. Not GRSW Mode.
PAGRSW	Style bit 18 = 1. GRSW Mode. Allows entry to STEP 11.
STEP 11	Contents of CW3 transferred to CW1 buffer.
$\overline{\text{PACWL}}$	CWL stat. unset. Allows entry to STEP 12.
STEP 12	CW1 addresses store. Data transferred from store to data buffer. CW1 updated.
PASEQ	SEQ stat. set. Allows entry to STEP 13.
STEP 13	Data transferred from data buffer to CW0 buffer.
$\overline{\text{PA1FS}}$	1FS stat. unset. Allows entry to STEP 14.
STEP 14	CW1 addresses store. Data transferred from store to data buffer. CW1 updated.
PA2FS	2FS stat. set. Allows entry to STEP 15.
STEP 15	Address in CW1 buffer written to store at address CW3.
PA1FS	1FS stat. set. Allows entry to STEP 16.
STEP 16	Data transferred from data buffer to CW1 buffer. CWL stat. is now set which allows another transfer to take place.
STEP 7	Unload CW1.
$\overline{\text{PACWL}}$	CWL stat. unset. Allows entry to STEP 8.
STEP 8	Unload CW0.
$\overline{\text{PAPT}}$	PT stat. unset } Allows entry to STEP 1
$\overline{\text{PACT}}$	CT stat. unset } for next block transfer.

SIGNAL	MP	E D REF WGHO3EN
PARSMIX	1C21:9	25 Q1
PA1FS	1A17:15	2 VN
PACWL	1D13:16	10 IF
$\overline{\text{PAK23}}$	1A16:20	84 VP
PAK23	1A4:12	81 SR
$\overline{\text{PACT}}$	1D12:16	10 VF
PACT	1D12:12	10 TD
$\overline{\text{PAPT}}$	1D11:12	10 GN
PAASET	1E28:16	21 IP
PAPT	1D11:16	10 IR
$\overline{\text{PAGRSW}}$	1B21:12	120 GD
PAGRSW	1B21:16	120 IF
$\overline{\text{PACWL}}$	1D13:12	10 GD
PA1FS	1A17:13	2 UN
PASEQ	1A17:6	2 OU
PA2FS	1A17:7	2 NR
PATP	1B20:25	13 OT

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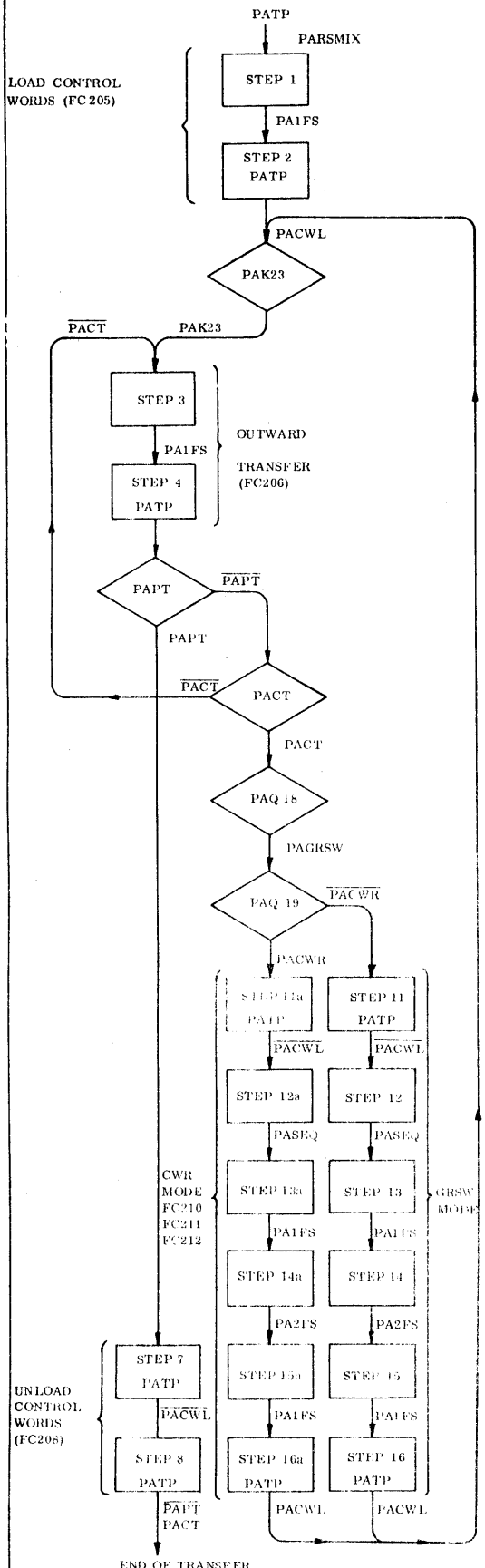
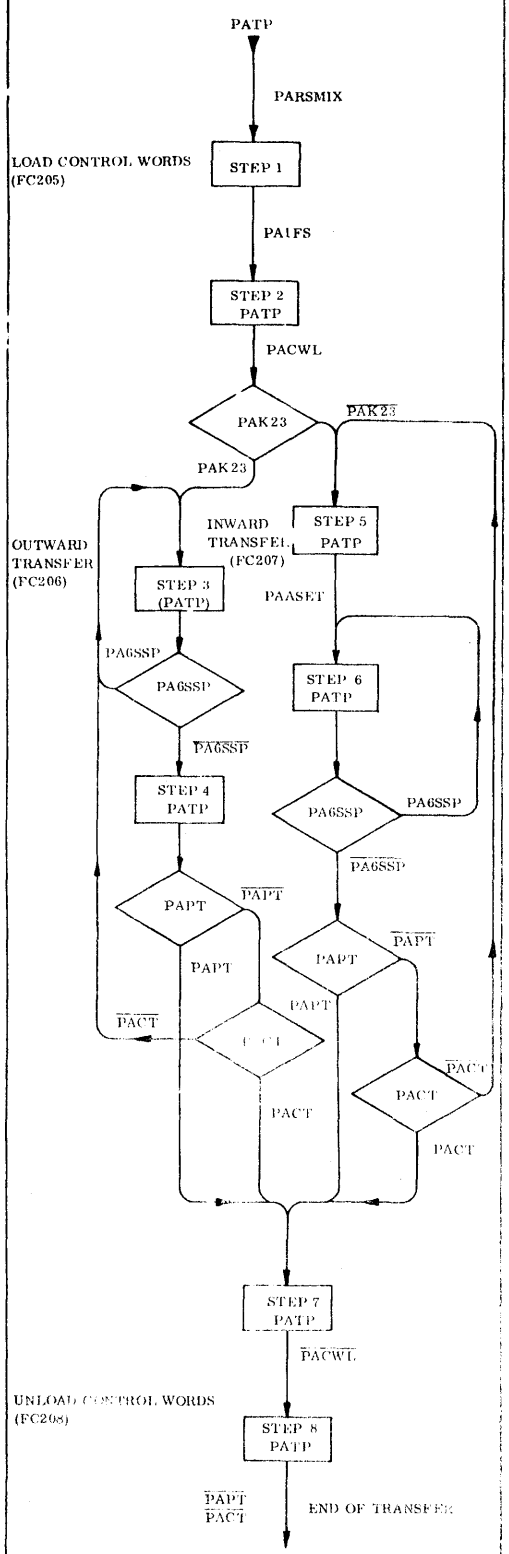
ICL	1904A/S 1903T	P.A.C. INWARD/OUTWARD TRANSFER WITH G.R.S.W.	FC202



SIGNAL	COMMENTS
PATP	Priorities are strobed at PATP locations to allow time sharing to take place.
PARSMIX	Priority peripheral has raised its R line. Allows entry to STEP1
STEP 1	Load Control word 1 (CW1)
PA1FS	1FS stat set. Allows entry to STEP 2
STEP 2	Load control word 0 (CW0)
PACWL	CWL stat set. Allows entry to STEP 3.
PAK23	Style bit 23 = 1 Outward Transfer.
$\overline{\text{PACT}}$	Permits transfer of next word
STEP 3	Read data from store into data buffer. Update CW1
PA1FS	1FS stat set. Allows entry to STEP 4
STEP 4	Update CW0.
$\overline{\text{PAPT}}$	Peripheral has not terminated. Continue the transfer.
PAPT	Peripheral has terminated. The transfer is completed. Enter STEP 7.
$\overline{\text{PACT}}$	The count has not terminated. Enter STEP 3 and transfer the next data word.
PACT	The count has terminated. Continue transfer according to the state of style bit 19 (PAQ19) of the current control word CW0 as follows
PAQ19 (PACWR)	1) If PAQ19 = 0 More data is required to complete a block Continue the transfer in GRSW mode. 2) If PAQ19 = 1 Recharge the control words and repeat the block transfer to the peripheral.
PAQ18 (PAGRSW)	Bit 18 = 1. Enables entry to STEPS 11 to 16.
STEP 11	Address store at location 256 + 4N + 3 (CW3) and transfers word to CW1 buffer
STEP 11a	Address store at location 256 + 4N + 2 (CW2) and transfers word to CW1 buffer
$\overline{\text{PACWL}}$	Control words unloaded. Allows entry to STEP 12 or 12a
STEP 12	Address store from CW1. Read R + 2 into data buffer. Update CW1 to give address of R + 3.
STEP 12a	Address store from CW1 Read R into data buffer. Update CW1 to give address of R + 1.
PASEQ	SEQ stat set allows entry to STEP 13 or 13a
STEP 13	Transfer item R + 2 from data buffer to CW0 buffer
STEP 13a	Transfer item R from data buffer to CW0 buffer.
PA1FS	1FS Stat set. Allows entry into STEP 14 or 14a
STEP 14	Address store from CW1. Read item R + 3 to data buffer. Update CW1 to give address of item R + 4. Unset 1FS stat.
STEP 14a	Address store from CW1. Read item R + 1 to data buffer. Update CW1 to give address of R + 2. Unset 1FS stat.
PA2FS	2FS stat set. Allows entry to STEP 15 or 15a
STEP 15	Address store from R - encode and write address of R + 4 in location 256 + 4N + 3 (CW3)
STEP 15a	Address store from R-encode and write address of R + 2 in location 256 + 4N + 3 (CW3)
PA1FS	1FS stat set. Allows entry to STEP 16 or 16a
STEP 16	Transfer item R + 3 from data buffer to CW1 buffer.
STEP 16a	Transfer item R + 1 from data buffer to CW1 buffer.
PACWL	Control words loaded - allows entry to STEP 3.
STEP 7	Unload CW1
$\overline{\text{PACWL}}$	CWL stat unset. Allows entry to STEP 8
STEP 8	Unload CW0
$\overline{\text{PAPT}}$	PT stat unset) Allows entry to STEP 1
$\overline{\text{PACT}}$	CT stat unset) for next block transfer.

SIGNAL	M.P.	E.D REF WGH03 FN
PATP	1B20:25	13 OT
PARSMIX	1C21: 9	25 QI
PA1FS	1A17:15	2 VN
PACWL	1D13:16	10 IF
PAK23	1A16:20	84 VP
PACT	1D12:16	10 VF
PAPT	1D11:16	10 IP
PAGRSW	1B21:16	120 IF
PACWR	1A21:16	120 IP
PASEQ	1A17: 6	2 OU
PA2FS	1A17: 7	2 NR
$\overline{\text{PACT}}$	1D12:12	10 TD
$\overline{\text{PACWL}}$	1D13:12	10 GD
$\overline{\text{PAPT}}$	1D11:12	10 GN



SIGNAL	COMMENTS
PATP	Priorities are strobed where PATP occurs on the flow chart to allow time sharing between peripherals and between data buffers.
PARSMIX	The R line of peripheral 24 is active and the R stat is set. STEP 1 is entered.
STEP 1	Load control word 1 (CW1)
PA1FS	1FS stat set. Allows entry to STEP 2.
STEP 2	Load control word 0 (CW0)
PACWL	CWL stat set indicating that the control words are loaded. Allows entry to STEP 3 or 5.
PAK23	Style bit 23 is a 1 bit indicating an outward transfer.
$\overline{\text{PAK23}}$	Style bit 23 is an 0 bit, indicating an inward transfer.
	NOTE:- When a transfer commences, if the count word is not a complete multiple of 8, then normal transfer procedure is followed until the count word becomes a direct multiple of eight and thereafter the transfer proceeds as indicated below.
	OUTWARD TRANSFER
STEP 3	Data transferred from store to the peripheral.
PA6SSP	Inhibits the 1FS stat when less than eight words have been transferred.
$\overline{\text{PA6SSP}}$	Enables entry to STEP 4 every eight word.
STEP 4	Updates the count word by eight.
	INWARD TRANSFER
STEP 5	Control word CW0 updated.
PAASET	A stat set. Allows entry to STEP 6.
STEP 6	Data word transferred from peripheral to store.
PA6SSP	Inhibits entry to SP5 which causes STEP 6 to be re-entered when data has been received from peripheral
$\overline{\text{PA6SSP}}$	Occurs after each eight word transfer. Allows entry to STEP 5 which updates the count by eight.
$\overline{\text{PAPT}}$	PT stat unset. Transfer is not peripheral terminated.
PAPT	PT stat set. Transfer is terminated. Allows entry to STEP 7.
$\overline{\text{PACT}}$	CT stat unset. Transfer is not count terminated. Enter STEPS 3 and 4 for transfer of next eight words.
PACT	CT stat set. Transfer is terminated. Allows entry to STEP 7.
STEP 7	Unload CWL.
$\overline{\text{PACWL}}$	CWL stat unset. Allows entry to STEP 8.
STEP 8	Unload CW0.
$\overline{\text{PAPT}}$ $\overline{\text{PACT}}$	PT stat unset) Allows entry to STEP 1 CT stat unset) for next block transfer.

SIGNAL	MP	E.D REF WGH03 FN
PATP	1B20:25	13 OT
PARSMIX	1C21:9	25 QI
PA1FS	1A17:15	2 VN
PACWL	1D13:16	10 IF
$\overline{\text{PACWL}}$	1D13:12	10 GD
PAK23	1A16:20	84 VP
$\overline{\text{PAK23}}$	1A4:12	81 SR
PAASET	1E28:16	21 IP
PAPT	1D11:16	10 IP
$\overline{\text{PAPT}}$	1D11:12	10 GN
PACT	1D12:16	10 VF
$\overline{\text{PACT}}$	1D12:12	10 TD
PA6SSP	1E27:24	65 RS

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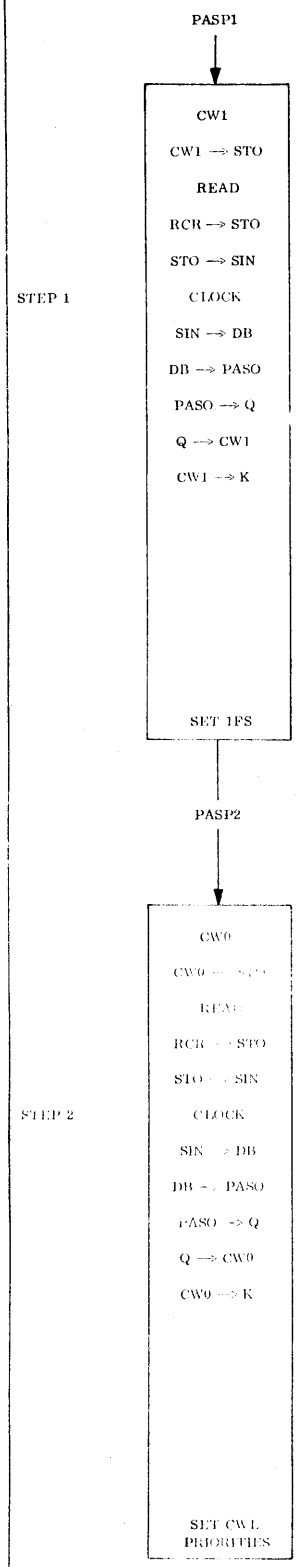
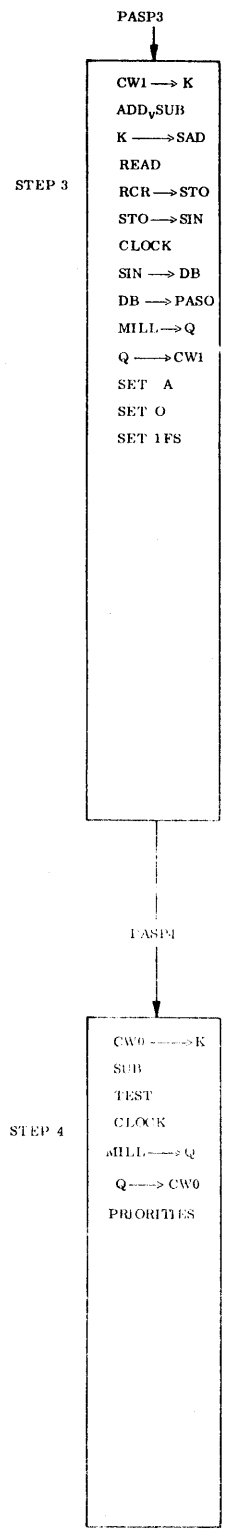
ICL	1904A/S 1903T	P.A.C. INWARD/OUTWARD TRANSFER - HIGH SPEED PERIPHERAL	FC204



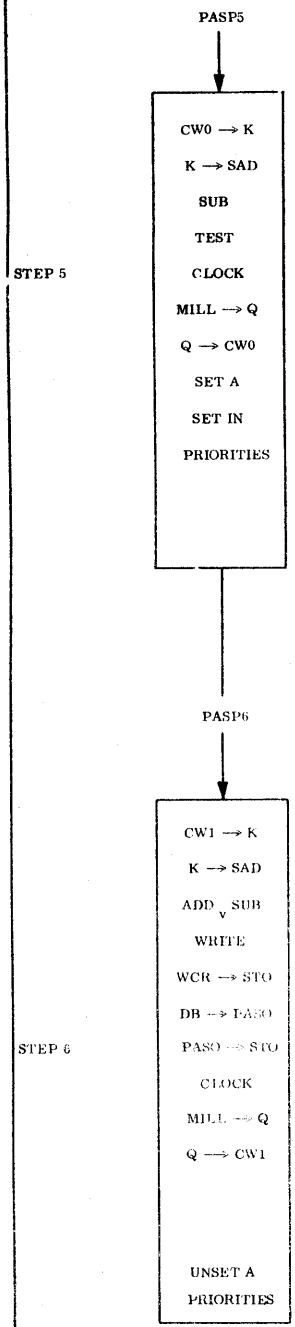
FUNCTION	SIGNAL	COMMENTS
STEP 1	PASP1	STEP 1 is active. CW1 is to be read from store and loaded into the CW buffer.
CW1	PARE00	Inserts a 1-bit in the l.s. bit position of the encoder address. Enables the encoder to produce store address 256 + 4N + 1, i.e. CW1.
CW1 → STO	PACW-SAD	Encoder addresses store on the SAD highway.
READ	PARD	Initiates a store access request by setting the RCR stat.
RCR → STO	PARCR	To store. Requests store access.
STO → SIN	PADA	Signal from store to indicate that control word CW1 is available on the SIN highway.
CLOCK	PADA	Starts the clock pulses.
SIN → DB	PADA	Initiates the GSIN signal which gates CW1 into the data buffer (e.g. PA0GSIN for data buffer 0).
DB → PASO	$\overline{\text{PAK-SO}}$	Enables the GSO signal (e.g. PA0GSIN) which transfers CW1 from the data buffer to the PASO highway for parity checking and for transfer to the Q highway.
PASO → Q	PASO-Q	Transfers CW1 from the PASO highway to the Q highway.
Q → CW1	PAQ-CW1	Transfers CW1 from the Q highway to the control word buffer.
CW1 → K	PACW1-K	Transfers CW1 to the K highway for display only.
SET 1FS	PASP1	1FS stat. set. STEP 1 ends, STEP 2 commences.
STEP 2	PASP2	STEP 2 is active. CW0 is to be read from store and loaded into the CW0 buffer.
CW0	$\overline{\text{PARE00}}$	Inhibits the 1-bit in the l.s. bit position of the encoder address. The encoder now produces store address 256 + 4N + 0, i.e. CW0.
CW0 → STO	PACW-SAD	Encoder addresses store on the SAD highway.
READ	PARD	Initiates request for a store access by setting the RCR stat.
RCR → STO	PARCR	To store. Requests store access.
STO → SIN	PADA	Signal from store to indicate that control word CW0 is available on the SIN highway.
CLOCK	PADA	Starts the clock pulses.
SIN → DB	PADA	Initiates the GSIN signal (e.g. PA0GSIN) which transfers CW0 into the data buffer.
DB → PASO	$\overline{\text{PAK-SO}}$	Enables the GSO signal (e.g. PA0GSO) which transfers CW0 from the data buffer to the PASO highway for parity checking and for transfer to the Q highway.
PASO → Q	PASO-Q	Transfers CW0 from the PASO highway to the Q highway.
Q → CW0	PAQ-CW0	Transfers CW0 from the Q highway to the CW0 buffer.
CW0 → K	PACW0-K	Transfers CW0 to the K highway for display only.
SET CWL	PASCWL	Sets CWL stat. to indicate that control words are loaded. Enables entry to next step.
PRIORITIES	$\overline{\text{PASKP}}$	PATP strobes priorities.

STEP1 / SIGNAL	MP	ED REF WGHO3FN
STEP 1 enabling signals		
$\overline{\text{PACWL}}$	1D13:12	10 GD
$\overline{\text{PARSMIN}}$	1C21:9	25 QJ
$\overline{\text{PA1FS}}$	1A17:13	2 UN
$\overline{\text{PACT}}$	1D12:12	10 TD
$\overline{\text{PAPT}}$	1D11:12	10 GN
Enter STEP 1		
PASP1	1A16:24	1 FA
PARE00	1B16:8	1 QT
PACW-SAD	1B17:6	2 GL
PARD	1C17:10	2 OE
PARCR	1B19:22/24	11 WQ
PADA	1C19:11	12 EA
$\overline{\text{PAK-SO}}$	1B17:10	2 EJ
PASO-Q	1B17:4	2 PJ
PAQ-CW1	1C17:2	2 HD
PACW1-K	1B17:15	2 WM
STEP 2		
STEP 2 enabling signals		
$\overline{\text{PACWL}}$	1D13:12	10 GD
$\overline{\text{PARSMIN}}$	1C21:9	25 QJ
$\overline{\text{PA1FS}}$	1A17:15	2 VN
$\overline{\text{PACT}}$	1D12:12	10 TD
$\overline{\text{PAPT}}$	1D11:12	10 GN
Enter STEP 2		
PASP2	1B16:4	1 FC
PARE00	1B16:8	1 QT
PACW-SAD	1B17:6	2 GL
PARD	1C17:10	2 OE
PARCR	1B19:22/24	11 WQ
PADA	1C19:11	12 EA
$\overline{\text{PAK-SO}}$	1B17:10	2 EJ
PASO-Q	1B17:4	2 PJ
PAQ-CW0	1C17:3	2 HB
PACW0-K	1B17:19	2 VL
PASCWL	1C17:7	2 JE
PASKP	1B16:6	1 QP



FUNCTION	SIGNAL	COMMENTS
STEP 3	PASP3	STEP 3 is active. CW1 is to be updated and data is to be read from store and transferred to the data buffer.
CW1 ⟶ K	PACW1-K	Transfers CW1, from the control word buffer to the K highway for addressing of store and updating in the mill.
ADDvSUB	{ PAADD / PASUB	Updates CW1. Adds 1 for forward addressing Updates CW1 Subtracts 1 for backward addressing.
K ⟶ SAD	PAK-SAD	CW1 addresses store via the K and SAD highways
READ	PARD	Initiates a store access request by setting the RCR stat.
RCR ⟶ STO	PARCR	To store. Requests a store access.
STO ⟶ SIN	PADA	Signal from store to indicate that the requested data is available on the SIN highway.
CLOCK	PADA	Starts the clock pulses.
SIN ⟶ DB	PADA	Initiates the GSIN signal (e.g. PA0GSIN) which gates the data into the data buffer.
DB ⟶ PASO	$\overline{\text{PAK-SO}}$	Enables the GSO signal which gates the data from the data buffer to the PASO highway where parity is checked.
MILL ⟶ Q	$\overline{\text{PASO-Q}}$	Connects the mill output to the Q highway
Q ⟶ CW1	PAQ-CW1	CW1 (updated) is returned to the CW buffer from the Q highway.
SET A	PASETA	Sets the A stat in the active peripheral channel. Prohibits use of the data buffer by other peripheral channels connected to the buffer until the transfer of data to the selected peripheral has ended. Also activates the peripheral interface A line.
SET O	PASETO	Switches the DBO stat for outward transfer which activates the interface T line and initiates the data character gating pulses. (e.g. PA0CH0 for data buffer 0, first character).
SET 1FS	PASP3	1F3 stat sets. STEP 3 ends STEP4 commences.
STEP 4	PASP4	STEP 4 is active. The count word (CW0) is to be updated and the count tested for zero content.
CW0 ⟶ K	PACW0-K	Transfers CW0 from the control word buffer to the mill for updating.
SUB	PAUSB	Decrements the count word by one for each data word received from store.
TEST	PAGMT	Initiates the mill test. Sets the CT stat when the word count is zero.
CLOCK	PAGMT	starts the clock pulses.
MILL ⟶ Q	$\overline{\text{PASO-Q}}$	Connects the mill output to the Q highway
Q ⟶ CW0	PAQ-CW0	CW0 (updated) is returned to the CW buffer from the Q highway.
PRIORITIES	$\overline{\text{PASKP}}$	PATP strobes priorities.

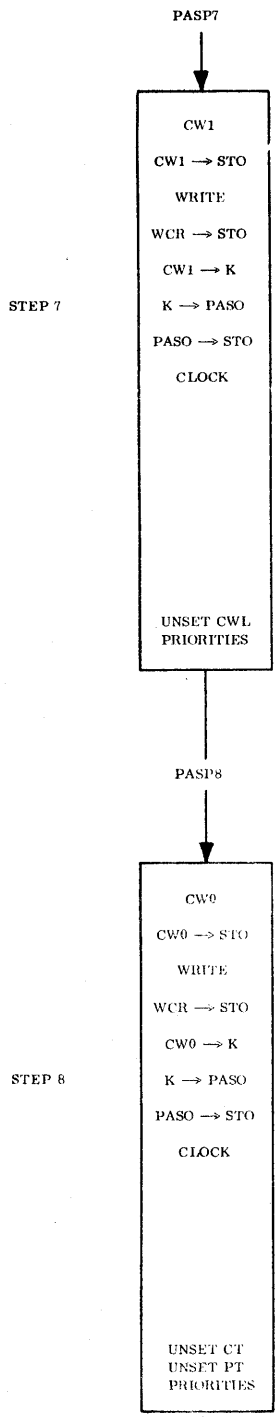
STEP3 / SIGNAL	M P	E D REF WGH03FN
STEP 3 enabling signals		
PACWL	1D13:16	10 IF
$\overline{\text{PAK23}}$	1C12: 4	84 VP
$\overline{\text{PA1FS}}$	1A17:13	2 UN
$\overline{\text{PAPT}}$	1D11:12	10 GN
$\overline{\text{PACT}}$	1D12:12	10 TD
Enter STEP 3		
PASP 3	1A16:2	1 HF
PACW1-K	1B17:15	2 WM
PAADD	1A17:18	2 KO
PASUB	1A17:22	2 JN
PAK-SAD	1B17:12	2 HM
PARD	1C17:10	2 OE
STEP 3		
PARCR	1B19:22/24	11 WQ
PADA	1C19:11	12 EA
$\overline{\text{PAK-SO}}$	1B17:10	2 EJ
$\overline{\text{PASO-Q}}$	1A17:26	2 PH
PAQ-CW1	1C17:2	2 HD
PASETA	1B17:24	2 LJ
PASETO	1B17:25	2 RK
STEP 4		
STEP 4 enabling signals		
PACWL	1D13:16	10 IF
PAK23	1A16:20	84 VP
PA1FS	1A17:15	2 VN
$\overline{\text{PAPT}}$	1D11:12	10 GN
$\overline{\text{PACT}}$	1D12:12	10 TD
Enter STEP 4		
PASP4	1A16:18	1 FG
PACW0-K	1B17:19	2 VL
PASUB	1A17:22	2 JN
PAGMT	1B17:26	2 RA
$\overline{\text{PASO-Q}}$	1A17:26	2 PH
PAQ-CW0	1C17: 3	2 HB
$\overline{\text{PASKP}}$	1B16: 6	1 QP



FUNCTION	SIGNAL	COMMENTS
STEP 5	PASP5	STEP 5 is active. The count portion of CW0 is to be updated and at the end of the step transfer of the data word from the peripheral to the data buffer will commence.
CW0 → K	PACW0-K	Transfers CW0 to the K highway and to the mill.
K → SAD	PAK-SAD	Transfers CW0 from the K highway to the SAD highway. This is an unproductive transfer.
SUB	PASUB	CW0 is decremented by one for each data word transferred.
TEST	PAGMT	Initiates the mill test. Sets the CT stat. when the word count is reduced to zero.
CLOCK	PAGMT	Starts the clock pulses.
MILL → Q	$\overline{\text{PASO-Q}}$	Connects the mill output to the Q highway.
Q → CW0	PAQ-CW0	CW0 (updated) is returned to the CW buffer from the Q highway.
SETA	PASETA	Sets the A stat. in the selected peripheral channel. Prohibits use of the data buffer by other peripheral channels connected to the buffer until a word of data has been transferred to PAC from the peripheral and written away to store. Also activates the interface A line to the peripheral.
SET IN	PASETIN	Switches the DBO stat. for inward transfer which activates the interface T line to the peripheral and initiates the data character gating pulses (e.g. PA0TIN0 for data buffer 0, first character).
PRIORITIES	$\overline{\text{PASKP}}$	PATP strobes priorities at the end of the step and PAC may now service another data buffer. The A stat. associated with the current transfer remains set therefore STEP 6 of this transfer must be entered when PAC resumes control of the buffer.
	PAASET	The A stat. in the selected peripheral channel is still set and the peripheral R stat. sets when the fourth data character is being gated into the data buffer therefore STEP 6 is entered.
STEP 6	PASP6	Data is to be written from the data buffer into store and CW1 is to be updated.
CW1 → K	PACW1-K	Transfers CW1 to the K highway and to the mill.
K → SAD	PAK-SAD	CW1 addresses store via the K and SAD highways.
ADD v SUB	PAADD PASUB	Updates CW1. Adds one if forward addressing. Updates CW1. Subtracts one if backward addressing.
WRITE	PARVW	Sets the write store request stat. WCR.
WCR → STO	PAWCR	To store. Requests a store access.
DB → PASO	$\overline{\text{PAK-SO}}$	Enables GSO (e.g. PA0GSO) which gates the data from the data buffer to the PASO highway.
PASO → STO	PAOCC	Signal from store. Gates data into store.
CLOCK	PAOCC	Starts the clock pulses.
MILL → Q	$\overline{\text{PASO-Q}}$	Connects the mill output to the Q highway.
Q → CW1	PAQ-CW1	CW1 (updated) is returned to the CW buffer from the Q highway.
UNSET A	PARSETA	Unsets the A stat. The data buffer is now available to other peripheral channels.
PRIORITIES	$\overline{\text{PASKP}}$	PATP strobes priorities.

STEP 5 SIGNAL	M.P.	CONDITION
STEP 5 enabling signals		
$\overline{\text{PAK23}}$ $\overline{\text{PAASET}}$ $\overline{\text{PAPT}}$ $\overline{\text{PACWL}}$ $\overline{\text{PACT}}$ $\overline{\text{PA6SSP}}$	REFER TO COL. 4	R stat. set by Peripheral
Enter STEP 5		E.D. REF. WGHØ3FN
PASP5	1B16:25	1 FI
PACW0-K	1B17:19	2 VL
PAK-SAD	1B17:12	2 HM
PASUB	1A17:22	2 JN
$\overline{\text{PAGMT}}$	1B17:26	2 RA
$\overline{\text{PASO-Q}}$	1A17:26	2 PH
PAQ-CW0	1C17:3	2 HB
PASETA	1B17:24	2 LJ
$\overline{\text{PASETIN}}$	1B17:20	2 IF
$\overline{\text{PASKP}}$	1B16:6	1 QP
$\overline{\text{PAK23}}$	1A16:20	84 VP
$\overline{\text{PAASET}}$	1E28:12	21 GN
$\overline{\text{PAPT}}$	1D11:12	10 GN
$\overline{\text{PACWL}}$	1D13:16	10 IF
$\overline{\text{PACT}}$	1D12:12	10 TD
$\overline{\text{PA6SSP}}$	1E27:24	65 RS

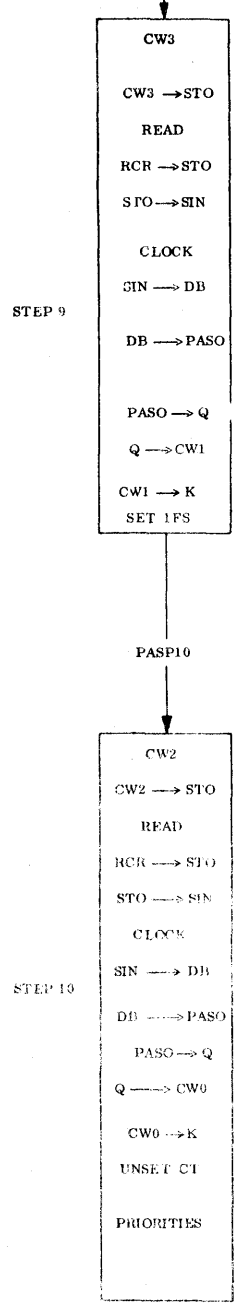
STEP 6 SIGNAL	M.P.	CONDITION
STEP 6 enabling signals		
$\overline{\text{PAK23}}$ PAASET PACWL	REFER TO COL. 10	R stat. set by Data Buffer control
Enter STEP 6		E.D. REF. WGHØ3FN
PASP6	1A16:4	1 FK
PACW1-K	1B17:15	2 WM
PAK-SAD	1B17:12	2 HM
PAADD	1A17:18	2 KO
PASUB	1A17:22	2 JN
PARVW	1C17:4	2 SC
PAWCR	1B19:21	11 WS
$\overline{\text{PAK-SO}}$	1B17:10	2 EI
PAOCC	1C19:7	12 JA
$\overline{\text{PASO-Q}}$	1A17:26	2 PH
PAQ-CW1	1C17:2	2 HB
PARSETA	1A17:25	2 KC
$\overline{\text{PASKP}}$	1B16:6	1 QP
$\overline{\text{PAK23}}$	1A4:12	81 SR
PAASET	1E28:16	21 HP
PACWL	1D13:16	10 IF



FUNCTION	SIGNAL	COMMENTS
STEP 7	PASP7	STEP 7 is active. CW1 is to be unloaded.
CW1	PARE00	Inserts a 1-bit in the l. s. bit position of the encoder address. Enables the encoder to produce store address 256 + 4N + 1.
CW1 → STO	PACW-SAD	Encoder addresses store on the SAD highway.
WRITE	PARVW	Sets the store access request stat. WCR.
WCR → STO	PAWCR	To store. Requests a store access.
CW1 → K	PACW1-K	Transfers CW1 to the K highway.
K → PASO	PAK-SO	Transfers CW1 from the K highway to the PASO highway.
PASO → STO	PAOCC	Signal from store. Gates CW1 into store via the PASO and SO highways.
CLOCK	PAOCC	Starts the clock pulses.
UNSET CWL	PARCWL	Unsets the CWL (control words loaded) stat. which enables entry to STEP 8.
PRIORITIES	$\overline{\text{PASKP}}$	PATP strobes priorities.
STEP 8	PASP8	STEP 8 is active, CW0 is to be unloaded.
CW0	$\overline{\text{PARE00}}$ $\overline{\text{PARE01}}$	Encoder produces store address 256 + 4N + 0.
CW0 → STO	PACW-SAD	Encoder addresses store on the SAD highway.
WRITE	PARVW	Sets the store access request stat. WCR
WCR → STO	PAWCR	To store. Requests a store access.
CW0 → K	PACW0-K	Transfers CW0 to the K highway.
K → PASO	PAK-SO	Transfers CW0 from the K highway to the PASO highway.
PASO → STO	PAOCC	Signal from store. Gates CW0 into store via the PASO and SO highways.
CLOCK	PAOCC	Starts the clock pulses.
UNSET CT	PARCT	Unsets the CT stat. of the terminated peripheral channel, if set.
UNSET PT	PARPT	Unsets the PT stat. of the terminated peripheral channel, if set.
PRIORITIES	$\overline{\text{PASKP}}$	PATP strobes priorities.

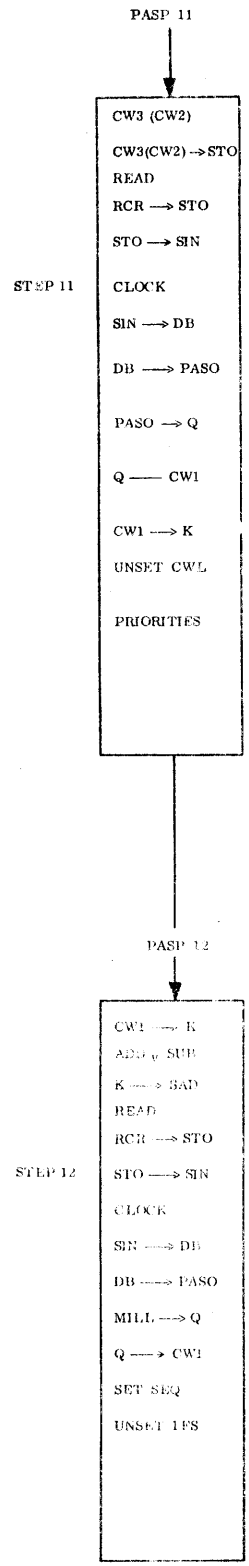
STEP 7 SIGNAL	M.P.	CONDITION
STEP 7 enabling signals		
$\overline{\text{PACWR}}$ $\overline{\text{PAGRSW}}$ $\overline{\text{PACWL}}$ $\overline{\text{PACT}}$ $\overline{\text{PASP6}}$	Refer to Column 4	Transfer is count terminated
PAPT $\overline{\text{PACWL}}$ $\overline{\text{PACT}}$ $\overline{\text{PASP6}}$	Refer to Column 4	Transfer is peripheral terminated
Enter STEP 7		E.D. REF. WCHØ3FN
PASP7	1B16:24	1 JN
PARE00	1B16:8	1 QT
PACW-SAD	1B17:6	2 GL
PARVW	1C17:4	2 SC
PAWCR	1B19:21	11 WS
PACW1-K	1B17:15	2 WM
PAK-SO	1B17:8	2 FJ
PAOCC	1C19:7	12 JA
$\overline{\text{PARCWL}}$	1B17:21	2 VG
$\overline{\text{PASKP}}$	1B16:6	1 QP
$\overline{\text{PACWR}}$	1A21:12	120 GN
$\overline{\text{PAGRSW}}$	1B21:12	120 GD
$\overline{\text{PACWL}}$	1D13:16	10 IF
$\overline{\text{PACT}}$	1D12:16	10 VF
$\overline{\text{PASP6}}$	1A16:4	1 FK
PAPT	1D11:16	10 IP
PACT	1D12:12	10 TD

STEP 8 SIGNAL	M.P.	CONDITION
STEP 8 enabling signals		
$\overline{\text{PACWL}}$ $\overline{\text{PAGRSW}}$ $\overline{\text{PACT}}$ $\overline{\text{PASEQ}}$	Refer to Column 10	Transfer is count terminated
$\overline{\text{PACWL}}$ PAPT $\overline{\text{PACT}}$	Refer to Column 10	Transfer is peripheral terminated
ENTER STEP 8		E.D. REF. WCHØ3FN
PASP8	1B16:22	1 JQ
PACW-SAD	1B17:6	2 GL
PARVW	1C17:4	2 SC
PAWCR	1B19:21	11 WS
PACW0-K	1B17:19	2 UL
PAK-SO	1B17:8	2 FJ
PAOCC	1C19:7	12 JA
PARCT	1C17:9	2 JI
PARPT	1B17:13	2 WH
$\overline{\text{PASKP}}$	1B16:6	1 QP
$\overline{\text{PACWL}}$	1D13:12	10 GD
$\overline{\text{PAGRSW}}$	1B21:12	120 GD
$\overline{\text{PACT}}$	1D12:16	10 VF
$\overline{\text{PASEQ}}$	1A17:3	2 OT
$\overline{\text{PACWL}}$	1D13:12	10 GD
PAPT	1D11:16	10 IP
$\overline{\text{PACT}}$	1D12:12	10 TD



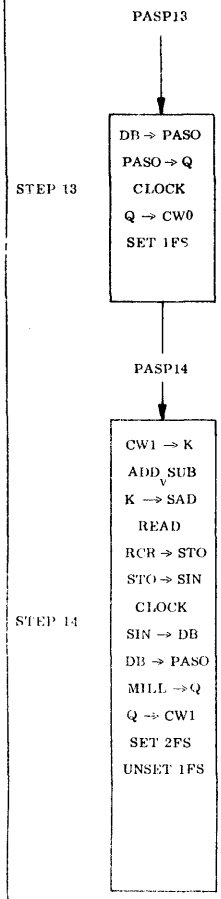
FUNCTION	SIGNAL	COMMENTS
STEP 9	PASP9	STEP 9 is active. Control word CW1 is to be recharged from store address 256 + 4N + 3 (i.e. CW3)
CW3	PARE00 PARE01	1 - bits are inserted in the two l.s. bit positions of the encoder address. Enables the encoder to produce store, address 256 + 4N + 3
CW3 → STO	PACW-SAD	Encoder address store on the SAD highway
READ	PARD	Initiates a store access request by setting the RCR stat.
RCR → STO	PARCR	To store. Requests store access.
STO → SIN	PADA	Signal from store which indicates that control word CW3 is present on the SIN highway.
CLOCK	PADA	Starts the clock pulses.
SIN → DB	PADA	Initiates the GSIN signal (e.g. PA0GSIN) which gates CW3 into the data buffer.
DB → PASO	$\overline{\text{PAK-SO}}$	Enables the GSO signal which gates the control word onto the PASO highway for checking of parity and for transfer to the control word buffer.
PASO → Q	PASO-Q	Transfers CW3 from the PASO highway to the Q highway.
Q → CW1	PAQ-CW1	Transfers CW3 into the CW1 section of the control word buffer. The control word will now be referred to as CW1.
CW1 → K	PACW1-K	Transfers CW1 to the K highway for display only.
SET 1FS	PASP 9	Sets the 1FS stat at clock PATA to enable entry to STEP 10
STEP 10	PASP10	STEP 10 is active. Control word CW0 is to be recharged from store address 256 + 4N + 2 (i.e. CW2).
CW2	PARE01	A 1-bit is inserted in bit position two of the encoder address. Enables the encoder to produce store address 256 + 4N + 2
CW2 → STO	PACW-SAD	Encoder address store on the SAD highway.
READ	PARD	Initiates a store access request by setting the RCR stat.
RCR → STO	PARCR	To store. Requests store access.
STO → SIN	PADA	Signal from store which indicates that control word CW2 is present on the SIN highway.
CLOCK	PADA	Starts the clock pulses.
SIN → DB	PADA	Initiates the GSIN signal which gates CW2 into the data buffer.
DB → PASO	$\overline{\text{PAK-SO}}$	Enables the GSO signal which gates the control word onto the PASO highway for checking of parity and for transfer to the control word buffer.
PASO → Q	PASO-Q	Transfers CW2 from the PASO highway to the Q highway
Q → CW0	PAQ-CW0	Transfers CW2 from the Q highway to the CW0 section of the control word buffer. The control word will now be referred to as CW0
CW0 → K	PACW0-K	Transfers CW0 to the K highway for display only.
UNSET CT	PARCT	Unsets the count-terminate stat. Enables entry to STEPS 3 and 4 for repetition of previous data block.
PRIORITIES	$\overline{\text{PASKP}}$	PATP strobes priorities.

STEP9 SIGNAL	M.P	E.D. REF WGHO3FN
STEP 9 Enabling signals		
PACWR	1A21:16	120 JP
$\overline{\text{PAGRSW}}$	1B21:12	120 GD
$\overline{\text{PA1FS}}$	1A17:13	2 UN
$\overline{\text{PASP6}}$	1A16: 4	1 FK
PACWL	1D13:16	10 IF
PACT	1D12:16	10 VF
Enter STEP 9		
PASP 9	1B16:15	1 FT
PARE00	1B16: 8	1 QT
PARE01	1B16:20	1 QS
PACW-SAD	1B17: 6	2 GL
PARD	1C17:10	2 PE
PARCR	1B19:22	11 WQ
$\overline{\text{PADA}}$	1C19:11	12 EA
$\overline{\text{PAK-SO}}$	1B17:10	2 EJ
PASO-Q	1B17: 4	2 PJ
PAQ-CW1	1C17: 2	2 HD
PACW1-K	1B17:15	2 WM
STEP10		
STEP 10 Enabling signals		
PACWR	1A21:16	120 JP
$\overline{\text{PAGRSW}}$	1B21:12	120 GD
PA1FS	1A17:15	2 VN
PACWL	1D13:16	10 IF
PACT	1D12:16	10 VF
Enter STEP 10		
PASP10	1B16:17	1 PA
PARE01	1B16:20	1 QS
PACW-SAD	1B17: 6	2 GL
PARD	1C17:10	2 PE
PARCR	1B19:22/24	11 WQ
$\overline{\text{PADA}}$	1C19:11	12 EA
$\overline{\text{PAK-SO}}$	1B17:10	2 EJ
PASO-Q	1B17: 4	2 PJ
PAQ-CW0	1C17: 3	2 HB
PACW0-K	1B17:19	2 VL
$\overline{\text{PARCT}}$	1C17: 9	2 JJ
$\overline{\text{PASKP}}$	1B16: 6	1 QP



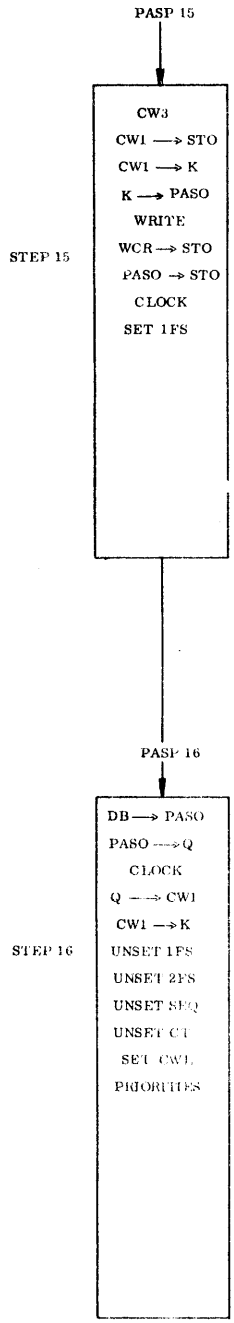
FUNCTION	SIGNAL	COMMENTS
	NOTE	Items in brackets refer to the CWR mode of transfer. This applies only to charts FC210, 211 and 212.
STEP 11	PASP 11	STEP 11 is active. CW3 (CW2) is to be loaded into the CW1 section of the control word buffer.
CW 3 (CW 2)	PARE00 / PARE01	Enables the encoder to produce the address of CW3 (CW2 i.e. 256 + 4N + 2)
CW3(CW2)→STO	PACW-SAD	Encoder address store on the SAD highway.
READ	PARD	Initiates a store access request by setting the RCR stat.
RCR→ STO	PARCR	To store. Requests store access.
STO → SIN	PADA	Signal from store which indicates that CW3 (CW2) is present on the SIN highway.
CLOCK	PADA	Starts the clock pulses.
SIN → DB	PADA	Initiates the GSIN signal which gates CW3 (CW2) into the data buffer.
DB → PASO	$\overline{\text{PAK-SO}}$	Enables the GSO signal which gates CW3 (CW2) from the data buffer to the PASO highway. Parity is checked.
PASO → Q	PASO-Q	Transfers CW3(CW2) from the PASO highway to the Q highway.
Q → CW1	PAQ-CW1	Transfers CW3 (CW2) to the CW1 buffer. The control word will now be referred to as CW1.
CW1 → K	PACW1-K	Transfers CW1 to the K highway for display only.
UNSET CWL	PARCWL	Unsets the control word loaded' stat. Enables entry to STEP 12.
PRIORITIES	$\overline{\text{PASKP}}$	PATP strobes priorities.
STEP 12	PASP 12	STEP 12 is active. Store is to be addressed from the CW1 buffer to obtain R + 2 (R) which will be transferred to the data buffer. CW1 is to be updated to obtain store address of item R + 3 (R + 1).
CW1→K	PACW1-K	Transfers CW1 to the K highway for addressing of store and for updating in the mill.
ADD / SUB	PAADD / PASUB	Updates CW1 Adds one for forward addressing Updates CW1 Subtracts for backward addressing.
K → SAD	PAK-SAD	CW1 addresses store via the K and SAD highways.
READ	PARD	Initiates a store access request by setting the RCR stat
RCR → STO	PARCR	To store. Requests store access.
STO → SIN	PADA	Signal from store which indicates that item R + 2 (R) from the table held in store is available on the SIN highway.
CLOCK	PADA	Starts the clock pulses.
SIN →DB	PADA	Initiates the GSIN signal which gates R + 2 (R) into the data buffer.
DB→ PASO	$\overline{\text{PAK-SO}}$	Enables the GSO signal which transfers R + 2 (R) to the PASO higiway. Parity is checked.
MILL → Q	PASO-Q	Connects the mill output to the Q highway.
Q → CW1	PAQ-CW1	CW1 (updated) is returned to the CW1 buffer.
SET SEQ UNSET IFS	PASP 12 PASP 12	SEQ stat sets IFS stat unsets } enables entry to STEP 13.

STEP / SIGNAL	M.P.	E.D. REF. WGHØ3FN
STEP 11 enabling signals		
$\overline{\text{PASP 6}}$	1A16: 4	1 FK
PAGRSW	1B21:16	120 IF
PACWL	1D12:16	10 IF
PACT	1D12:16	10 VF
Enter STEP 11		
PASP 11	1A16:12	1 PC
PARE00	1B16: 8	1 QT
PARE01	1B16:20	1 QS
PACW-SAD	1B17: 6	2 GL
PARD	1C17:10	2 PE
PARCR	1B19:22	11 WQ
PADA	1C19:11	12 EA
$\overline{\text{PAK-SO}}$	1B17:10	2 EJ
PASO-Q	1B17: 4	2 PJ
PAQ-CW1	1C17: 2	2 HD
PACW1-K	1B17:15	2 WM
$\overline{\text{PARCWL}}$	1B17:21	2 VG
$\overline{\text{PASKP}}$	1B16: 6	1 QP
STEP 12		
STEP 12 enabling signals		
PAGRSW	1B21:16	120 IF
$\overline{\text{PASEQ}}$	1A17: 3	2 OT
$\overline{\text{PACWL}}$	1D13:12	10 GD
PACT	1D12:16	10 VF
Enter STEP 12		
PASP 12	1B16:10/13	1 PE
PACW1-K	1B17:15	2 WM
PAADD	1A17:18	2 KO
PASUB	1A17:22	2 JN
PAK-SAD	1B17:12	2 HM
PARD	1C17:10	2 PE
PARCR	1B19:22	11 WQ
PADA	1C19:11	12 EA
$\overline{\text{PAK-SO}}$	1B17:10	2 EJ
$\overline{\text{PASO-Q}}$	1A17:26	2 PH
PAQ-CW1	1C17: 2	2 HD



FUNCTION	SIGNAL	COMMENTS
STEP 13	PASP 13	STEP 13 is active. Item R + 2(R) is to be transferred from the data buffer to the CW0 buffer.
DB → PASO	$\overline{\text{PAK-SO}}$	Enables the GSO signal which transfers R + 2(R) from the data buffer to the PASO highway.
PASO → Q	PASO-Q	Transfers R + 2(R) from the PASO highway to the Q highway.
CLOCK	PASP 13	Starts the clock pulses.
Q → CW0	PAQ-CW0	Transfers R + 2(R) from the Q highway to the CW0 buffer. The control word will now be referred to as CW0.
SET 1FS	PASP 13	The 1FS stat. sets to enable STEP 14.
STEP 14	PASP 14	STEP 14 is active. Store is to be addressed from the CW1 buffer to obtain item R + 3(R + 1) which will be read from store and transferred to the data buffer. CW1 is then to be updated to obtain address of R + 4(R + 2).
CW1 → K	PACW1-K	Transfers CW1 to the K highway for addressing of store and for updating in the mill.
ADD SUB	PAADD PASUB	Updates CW1. Adds 1 for forward addressing. Updates CW1. Subtracts 1 for backward addressing.
K → SAD	PAK-SAD	CW1 addresses store via the K and SAD highways.
READ	PARD	Initiates a store access request by setting the RCR stat.
RCR → STO	PARCR	To store. Requests read access.
STO → SIN	PADA	Signal from store which indicates that item R + 3(R + 1) is available on the SIN highway.
CLOCK	PADA	Starts the clock pulses.
SIN → DB	PADA	Initiates the GSIN signal which gates R + 3(R + 1) from the SIN highway into the data buffer.
DB → PASO	$\overline{\text{PAK-SO}}$	Enables the GSO signal which gates R + 3(R + 1) onto the PASO highway for the parity check.
MILL → Q	$\overline{\text{PASO-Q}}$	Connects the mill output to the Q highway.
Q → CW1	PAQ-CW1	Transfers the updated control word CW1 from the Q highway to the CW1 buffer.
SET 2FS	PASP 14	The 2FS stat. sets } enables STEP 15.
UNSET 1FS	PASP 14	The 1FS stat. unsets }

STEP13 / SIGNAL	M P	E.D REF WGH03FN
STEP 13 enabling signals		
$\overline{\text{PA1FS}}$	1A17:13	2 UN
$\overline{\text{PA2FS}}$	1A17:5	2 OQ
PASEQ	1A17:6	2 OT
Enter STEP 13		
$\overline{\text{PASP13}}$	1B16:19	1PG
$\overline{\text{PAK-SO}}$	1B17:10	2 EI
PASO-Q	1B17:4	2 PJ
PAQ-CW0	1C17:3	2 HB
STEP 14		
STEP 14 enabling signals		
$\overline{\text{PA1FS}}$	1A17:15	2 VN
$\overline{\text{PA2FS}}$	1A17:5	2 OQ
PASEQ	1A17:6	2 OT
Enter STEP 14		
PASP 14	1B16:9	1 RJ
PACW1-K	1B17:15	2 WM
PAADD	1A17:18	2 KO
PASUB	1A17:22	2 JN
PAK-SAD	1B17:12	2 HM
PARD	1C17:10	2 OE
PARCR	1B19:22	11 WQ
$\overline{\text{PADA}}$	1C19:11	12 EA
$\overline{\text{PAK-SO}}$	1B17:10	2 EI
$\overline{\text{PASO-Q}}$	1A17:26	2 PH
PAQ-CW1	1C17:2	2 HD



FUNCTION	SIGNAL	COMMENTS
STEP 15	PASP 15	STEP 15 is active. The contents of CW1 buffer i.e. R + 4 (R + 2) is to be written to store at address 256 + 4N + 3.
CW3	PARE00 PARE01	Insert 1 - bits in the two l.s. bit position of the encoder address. Enables the encoder to produce store address 256 + 4N + 3
CW1 → STO	PACW-SAD	Encoder addresses store on the SAD highway
CW1 → K	PACW1-K	Transfer CW1 from the control word buffer to the K highway
K → PASO	PAK-SO	Transfers CW1 from the K highway to the PASO and SO highways for writing to store when store access is obtained.
WRITE	PARVW	Initiates a store access request by setting the WCR stat.
WCR → STO	PAWCR	To store. Requests store access.
PASO → STO	PAOCC	Signal from store. CW1 is written to store from the PASO and SO highways at address 256 + 4N + 3
CLOCK	PAOCC	Starts the clock pulses.
SET 1FS	PASP15	1FS stat sets to enable entry to STEP 16.
STEP 16	PASP16	STEP 16 is active. Item R + 3 (R + 1) is to be transferred from the data buffer to the CW1 buffer.
DB → PASO	$\overline{\text{PAK-SO}}$	Enables the GSO signals which gate R + 3 (R + 1) onto the PASO highway.
PASO → Q	PASO-Q	Transfers R + 3 (R + 1) from the PASO highway to the Q highway
CLOCK	PASP16	Starts the clock pulses
Q → CW1	PAQ-CW1	Transfers R + 3 (R + 1) to the CW1 buffer. The control word is now referred to as CW1.
CW1 → K	PACW1-K	Transfers CW1 to the K highway.
UNSET 1FS	PASP16	1FS stat unsets
UNSET 2FS	PASP16	2FS stat unsets
UNSET SEQ	PASP16	SEQ stat unsets
UNSET CT	PARCT	CT stat unsets
SET CWL	PASCWL	CWL stat sets.
PRIORITIES	$\overline{\text{PASKP}}$	PATP strobes priorities

Enabling signals for the next step.

STEP15 / SIGNALS	M.P.	E.D REF WGHO3 FN
STEO 15 enabling signals		
PASEQ	1A17:6	2 OT
PA1FS	1A17:13	2 UN
PA2FS	1A17:7	2 OR
Enter STEP 15		
PASP 15	1B16:5	1 PK
PARE00	1B16:8	1 QT
PARE01	1B16:20	1 QS
PACW-SAD	1B17:6	2 GL
PACW1-K	1B17:15	2 WM
PAK-SO	1B17:8	2 FJ
PARVW	1C17:4	2 SC
PAWCR	1B19:21	11 WS
PAOCC	1C19:7	12 JA
STEP16 / SIGNALS		
STEP 16 enabling signals		
PASEQ	1A17:6	2 OU
PA1FS	1A17:15	2 VN
PA2FS	1A17:7	2 OR
Enter STEP 16		
PASP 16	1B16:7	1 PM
PAK-SO	1B17:10	2 EI
PASO-Q	1B17:4	2 PJ
PAQ-CW1	1C17:2	2 HD
PACW1-K	1B17:15	2 WM
PARCT	1C17:9	2 JI
PASCWL	1C17:7	2 JE
PASKP	1B16:6	1 QP

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