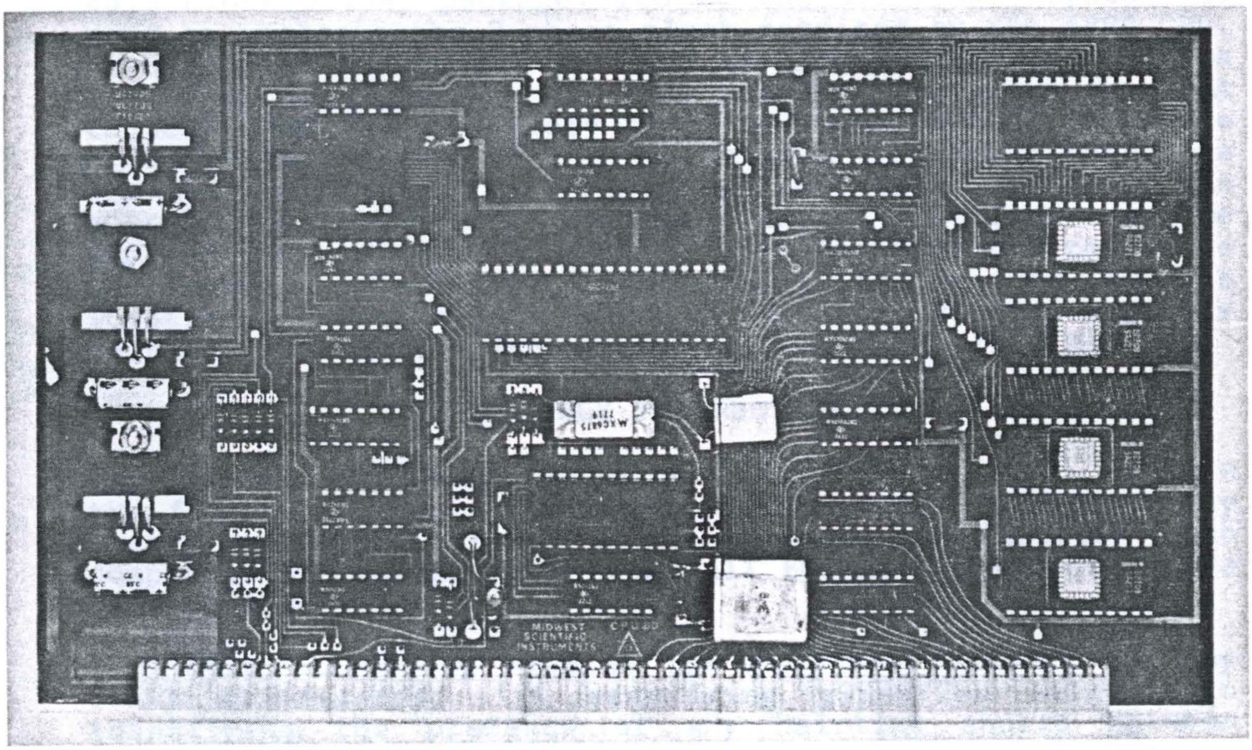
C P U BOARD

MODEL CP-1



Midwest Scientific Instruments, Inc.
Olathe, Kansas

CPU BOARD, MODEL CP-1

INTRODUCTION

The MSI Model CP-1 CPU, which is used in the MSI 6800 computer system, contains the central processing unit for the system. The CPU is based upon the Motorola 6800 microprocessor. The CPU board provides for up to 4K of EPROM memory consisting of four 2708 EPROM chips. The lowest 1K segment of the EPROM memory ($E000-$E3FF) is normally occupied by the MSI-BUG monitor routines. An additional 128 bytes of RAM is provided on the CPU board by a 6810 RAM chip.

The CPU board contains two separate clock circuits. A 14411 baud rate generator, with its associated 1.8432 MHz crystal, provides various baud rate clock frequencies which are required by serial input/output interfaces. A separate 6875 clock driver package, fed by the 3.579 MHz crystal, is used to generate the 2 phase clock required by the 6800 CPU. Bi-directional data bus drivers and address buffer packages are also provided on the CPU board. Provision for DMA request, DMA grant, memory clock and slow memory lines are provided for by the 6875 clock driver. If these functions are desired within a particular system, then, by use of the appropriate strappable options, these functions may be implemented. Strapping options are also provided to locate the onboard EPROM and RAM memory to desired address locations. Power to the board is provided by three separate voltage regulators which provide +5, -5, and +12 V.D.C.

ASSEMBLY INSTRUCTIONS

Before beginning assembly of the P.C. Board, perform the following steps. Referring to the parts list, carefully check the parts kit in order to properly identify each component and to make sure that all the necessary parts have been included.

Next, carefully examine the P.C. Board itself for any flaws or defects. A magnifying glass is helpful in identifying the presence of any hairline shorts between foils, incomplete etching of the board, or foil breaks. Such defects are rare but a careful preliminary examination is very worthwhile. Any defects should be corrected before beginning assembly of the board.

We recommend using a 30 watt soldering iron for all assembly. Use only solder having a resin core, never use any type of acid based solders. A 60/40 or 63/37 alloy is recommended.

Care should be taken when soldering transistors and integrated circuits, as over heating of the leads can destroy the device. Also be careful to orient the device correctly before soldering.

IC sockets may be used if desired. However, use only a high quality socket such as the Texas Instruments Low Profile Version. Inexpensive sockets can often cause more problems than they solve.

The P.C. board has been silk screened to show the proper placement of all major components. Refer also the the Assembly Drawing, No.100064, for correct placement and orientation of all components.

ASSEMBLY PROCEDURE

( ) Install the three voltage regulator packages, IC9 (7905), IC21 (7812), and IC1 (7805). Mount the regulators in the appropriate positions on the CPU card. Use 4-40 screws, #4 lock washers, hexnuts, and the heatsinks which have been provided for this purpose. After securing the regulators tightly in position, solder the leads to the pads provided. Refer to the Assembly Drawing, No. 100064, for correct screw orientation.

( ) Install the five female, 10 pin, Molex connectors on the bottom edge of the printed circuit board. The main body of the connector lies on the component side of the circuit board. Make sure that the body of the connector lies flat against the board and that it is pressed hard against the edge of the circuit board before soldering. Solder only the end pins on each connector first while holding the connector securely in position. After the connectors have been secured in this manner, the remaining pins may then be soldered.

( ) Install the 40 pin I.C. socket at position IC 11. Note that PIN 1 of the IC socket has a beveled edge. Orient the socket properly before soldering into position.

( ) Solder the 16 pin IC socket into position IC 18.

( ) Solder the six 24 pin IC sockets at the following positions, IC 23, IC 5, IC 13, IC 16, IC 20 and IC 28.

( ) Solder resistors R1 thru R6 and R9 thru R18 into their appropriate positions on the printed circuit board. Resistors R7 and R8 are optional and are not included with the kit. Install jumper wires in these positions if resistors are not used.

( ) Solder capacitors C1 thru C18 on the printed circuit board. On electrolytic capacitors, be careful to observe the polarity markings on the capacitor in order to be sure that they are oriented properly before soldering into position.

( ) Solder integrated circuit packages IC

2,3,4,6,7,8,10,12,14,15,17,19, 22,24,25,26,and 27 into their appropriate positions on the PCB. If sockets are being used, they should be soldered into position at this time. IC packages 5,11,18,23, and 28 will be installed following preliminary checkout of the board. If IC sockets are being used, all IC packages may be left out until preliminary board checkout and voltage measurements have been completed. IC packages 13,16, and 20 are optional EPROM positions, which are not included in the kit, but may be installed by the user.

( ) Locate the two crystals Y 1 and Y 2 and install them in the appropriate positions on the printed circuit board. Solder into position.

( ) Two positions for 1N4003 diodes are provided located at D1 and D2. These diodes are optional and are not provided with the CPU kit. They may be installed by the user if desired.

( ) Upon completion of the P.C. Board assembly, carefully examine the board for the presence of any solder splashes, solder bridges, or any other defects on the board. A magnifying glass helps to detect such flaws. Any such defects must be carefully removed prior to board checkout. Be particularly carefull to examine the board in the region of the EPROM sockets since the close tolerances between pads, and foils running in between, accounts for the majority of shorts which we have seen on this board.

( ) Install the index keying pin in the proper position of the bottom edge connector. This pin prevents the board from being accidentally plugged in backwards or with the pins offset.

( ) This completes the assembly procedure. Review the section covering strappable options in order to be sure the board is strapped properly for your desired configuration. Then proceed to the checkout section.

THEORY OF OPERATION

IC 3 and IC 7 are 74S138 decoder packages which provide decoded addresses for the four 2708 EPROM sockets. These sockets are normally strapped at base addresses E000, E400, E800 and EC00 but may be changed to reside at any high order address from 8 thru F. The standard MSI-BUG Monitor, Model MT-1, resides at base address $E000 and therefore this position may not be changed if the monitor is used in the system. The 6810 RAM chip, IC 5, may also be changed from its normal base address of $F000 to any other high order address from 8 thru F. These changes are made by changing the strappable options which are shown below:

Packages IC 4 and IC 8 are used to combine the appropriate outputs from the decoder packages in order to provide the chip enable signals to the 2708 EPROM position IC 13, IC 16, IC 20, and IC 28.

IC 2 provides address decoding for the restart vector PROM IC 6 (82S123).

IC 24 and IC 27 are 8T26 bi-directional bus driver packages which supply inverted data to the bus of the MSI-6800 Computer System.

IC 12, IC 15, and IC 19 are 8T97 buffer packages which drive the address bus of the MSI-6800 Computer System.

6875 CLOCK DRIVER PACKAGES

The 6875 Clock Driver is used on the MSI CPU Board. This package uses a 4X crystal frequency in order to generate the two phase non-overlapping clock required by the 6800 CPU. In addition, the master reset function for the processor is provided by the 6875 as well as several additional options. A DMA request/DMA grant function is available as well as a slow memory line. A memory clock signal is also available as well as a buffered phase two clock signal which drives the system bus. Several clock options are available with the 6875 including an R/C clock if desired, as well as an external clock input. All of these options have been brought to jumper pads on the CPU board where they may be implemented by the user if desired. When these options require additional motherboard lines, some unused baud rate signals or the user defined lines of the mother board may be reassigned. An appropriate jumper installed from the proper pad from the clock driver chip to the desired mother board line must then be installed in order to implement the desired function. Refer to the specification sheet for the 6875 clock driver which is included in the MSI-6800 Operating Manual

14411 BAUD RATE GENERATOR

The Motorola 14411 Baud Rate Generator is used on the MSI CPU board. This package requires a 1.8432 MHz crystal in order to generate the common baud rate frequencies which are required by serial I/O interfaces in the MSI system. All standard baud rates from 110 baud to 9600 baud are available. An additional output from the baud rate generator can be supplied to the 6875 clock generator package in order to drive the system clock if desired. However, since the 6875 requires a 4X crystal frequency, the system clock will only run at approximately 1/2 rated speed (.4608 MHz). The baud rate generator supplies the following baud rates to the mother board: 110, 150, 300, 9600 and 1200. If other baud rates are desired, then one of the existing baud rate signal lines must be used to carry the new desired frequency. An appropriate foil cut may be made on the CPU board and a jumper installed in order to bring the new clock to the mother board.

JUMPER SELECTABLE OPTIONS

Many jumper options are available on the MSI CPU card. Foil etch runs have been left in position in order to strap the board to its standard configuration. Therefore, unless the board is altered no jumper installation is required.

Jumper options are available to change the addresses of the four EPROMs or the 6810 RAM package, and to select various options associated with the 6875 clock driver packagbe. Each pad is identified with a number in order to facilitate desired changes. Identification of these straps is shown in the table below:

ON BOARD vs.OFF BOARD ADDRESSES

The MSI CPU board provides true buffer address information to the mother board of the MSI-6800 Computer System. However, data which is supplied to the data bus has been inverted by the 8T26 bi-directional bus driver packages. As a result, the data lines which communicate with the four 2708 EPROM packages, as well as the 6810 RAM package, come directly from the CPU chip before inversion by the bus driver packages. Therefore, when reading or writing to the on board memory locations, the bus driver packages must be enabled in the outward (write) direction in order to avoid interference by incoming data from the mother board. Therefore, a network of decoder packages is provided in order to distinguish between on board and off board addresses.

The standard configuration used in MSI 6800 Computer System provides that all addresses below $E000 are considered to be off the CPU board. Address $E000 and above are considered to be located on the CPU board, with exception of the block of memory from $F400 thru $F7FF which is reserved for the Interface Adapter Board and I/O interfaces. Any time that the standard configuration of the CPU board must be altered so as to provide on board memory, below address $E000, then the decoding circuitry must be changed appropriately. The most frequent occurrence of this modification would be the relocation of the 6810 RAM base address from $F000 to $A000 in order to preserve compatability with the SWTP 6800 system. IC 22 provides decoding of the appropriate address lines which are used to determine the on board/off board addresses. Pads are provided where jumpers can be cut in order to alter the addresses as desired.

RESTART AND INTERRUPT VECTORS

A restart and interrupt vector PROM (82S123, IC-6) provides the user with several selectable vector options. The standard configuration for the MSI 6800 system is for entry into the MSI-BUG monitor routines on RESET as well as on IRQ, NMI, or SWI. However, as shown in the table below, other combinations of vectors may be chosen as desired. By changing strap 20-21 and/or cutting address line A03 to the restart vector PROM, IC 6, and grounding the A03 input to the PROM, three optional sets of vectors may be selected, as described below.

GROUP 1 VECTORS (Standard)

This set of vectors allows the MSI-BUG monitor routines to be entered on system RESET at address $E0D0. The monitor routines are also entered on IRQ ($E000), NMI ($E005), and SWI ($E12E). Refer to the section covering the MSI-BUG monitor, Model MT-1, for further discussion of these functions, and the program source listings.

GROUP 2 VECTORS

This set of vectors is selected by cutting strap 20-21 and reinstalling strap 21-22. This allows the system to jump to address $D000 (MSI PROM DOS) on system RESET. The vectors for IRQ, NMI, and SWI remain the same as in the standard configuration described in GROUP 1. Address $D000 enters the MSI PROM version of the Disk Operating System.

GROUP 3 VECTORS

This group of vectors is selected by leaving strap 20-21 in place and cutting address line A03 to the restart vector PROM, IC 6. The A03 input to IC 6 must then be grounded. This set of vectors allows the DOS bootstrap routine, at address $EC00, to be entered on system RESET. Vectors for IRQ, NMI, and SWI remain the same as described above for GROUPS 1 and 2. The DOS bootstrap EPROM is MSI Model MIN-27-C, and is optional.

GROUP 4 VECTORS

This group of vectors is selected by changing strap 20-21 to position 21-22, cutting address line A03, and grounding the A03 input to IC 6. This set of vectors allows the user to define his own set of routines in PROM beginning at address $C000. The system RESET function jumps to address $C000. Three bytes are reserved here to allow the user to place a jump address ($7E XXXX) to his own restart routine. Three bytes are reserved for each interrupt vector to allow similar jump instructions to be placed in PROM as desired. The NMI vector is $C003, SWI is $C006, and IRQ is $C009. MSI MULTI-USER DISK EXTENDED BASIC utilizes this set of vectors to enter the multi-user operating system which resides at beginning address $C000.

TABLE OF RESTART AND INTERRUPT VECTOR OPTIONS

GROUP	STRAP	FUNCTION	VECTOR ADDRESS
1	20-21	RESET	$E0D0
		NMI	$E005
		SWI	$E12E
		IRQ	$E000
2	21-22	RESET	$D000
		NMI	$E005
		SWI	$E12E
		IRQ	$E000
3	20-21	RESET	$EC00
	A03 LOW	NMI	$E005
		SWI	$E12E
		IRQ	$E000
4	21-22	RESET	$C000
	A03 LOW	NMI	$C003
		SWI	$C006
		IRQ	$C009

CPU BOARD CHECKOUT PROCEDURE

( ) First carefully examine the circuit board for any obvious defects such as solder bridges and shorts.

( ) The important IC packages, which are normally plugged into IC sockets, should be removed before making the preliminary voltage checks on the board.

( ) Using an ohmmeter, measure between the output of each voltage regulator and ground to be sure that no shorts exist.

( ) Install the CPU board in the computer system and apply power to the system. Using a voltmeter or an oscilloscope, check the output of each of the voltage regulators for correct voltage level and for the absence of any ripple or oscillation.

( ) After ascertaining that the voltage levels are as expected, remove power from the system and install the remaining IC packages.

( ) With the complete set of boards installed in the system, and a terminal connected, the application of power to the system should result in an asterisk (*) being printed on the terminal as the prompt character.

( ) If the system fails to respond as expected, remove the CPU board and recheck for shorts using an ohm meter. Check for shorts between any two pins of the EPROM sockets, any two pins of the mother board connectors, and any two pins of the CPU chip. Most faults are the result of undesired shorts of this type.

If the fault cannot be located, refer to the section covering general system trouble shooting procedures.

CPU STRAPPABLE OPTIONS

SCHEMATIC ZONE	PAD NO.	IDENTIFICATION
2-C-6	1	Ground (Logic Common)
"	2	Enable (IC-3) Active Low
"	3	Phase 2 Clock from Bus
2-C-5	4	High order decoded address F
"	5	" " " " E
"	6	" " " " D
"	7	" " " " C
"	8	" " " " B
"	9	" " " " A
"	10	" " " " 9
"	11	" " " " 8
"	12	High order address select, on/off board decoder IC-22
"	13	" " " " , restart vector PROM IC-6
"	14	" " " " , IC-16
2-B-5	15	" " " " , IC-13
2-C-5	16	" " " " , IC-28
"	17	" " " " , IC-20
2-B-5	18	" " " " , IC-5
"	19	" " " " , IC-5
2-A-4	20	Ground
"	21	A4 address input, restart vector PROM IC-6
"	22	+5V
1-A-3	23	+5V
"	24	On/off board decoder input
"	25	F4-F7 decoded address block
"	26	Address A12
1-A-4	27	Ground
"	28	X2 input IC-18
"	29	X1 input IC-18
"	30	X1 input IC-18
1-A-2	31	Ground
"	32	IC-17 enable, - Pin 1
"	33	IC-17 enable, - Pin 15
1-A-4	34	Memory ready output IC-18
"	35	DMA request input IC-18
"	36	Memory clock output IC-18
"	37	DMA grant output IC-18
1-B-1	38	150 Baud clock signal output
"	39	300 " " " "
"	40	600 " " " "
"	41	1200 " " " "
"	42	2400 " " " "
"	43	4800 " " " "
"	44	9600 " " " "
1-A-3	45	On/off board decoder input, IC-22
"	46	Address A13
"	47	On/off board decoder input, IC-22
"	48	Address A14
"	49	On/off board decoder input, IC-22
"	50	Address A15
1-A-4	51	Ext clock input IC-18
"	52	Ground

1-B-1	53	1.8432 MHz clock output
1-B-2	54	RSA input IC-23, divide rate select
"	55	Ground
"	56	RSB input IC-23, divide rate select
"	57	Ground
"	58	+5V
"	59	+5V
1-B-1	60	110 Baud clock output
1-A-4	61	DBE control input, IC-25
1-B-5	62	Halt input enable (Halt Bus Lines)
"	63	" " " (CPU Halt Input)
1-B-3	64	NMI enable on/off board addresses (decoded off board)
"	65	" " " " " (Bus NMI)
1-C-1	66	Phase 1 clock output
"	67	Phase 1 clock bus line
"	68	150 Baud clock bus line
"	69	150 Baud clock signal output
"	70	BA output from CPU
"	71	110 Baud clock bus line
"	72	110 Baud clock signal output
"	73	BA Bus line
1-B-6	74	Bus line UD-1
"	75	" " UD-2

STRAP CONFIGURATIONS FOR CPU SELECTABLE OPTIONS

STRAP	IDENTIFICATION OR FUNCTION
1-2	Ø2 clock excluded from on-board address
2-3*	Ø2 " included " decoder
5-16*	IC 28 strapped for high order address $E
5-17*	IC 20 " " " " " "
5-14*	IC 16 " " " " " "
5-15*	IC 13 " " " " " "
12-13*	IC 5 strapped for high order address $F
18-19*	" " " " " " "
4-13*	IC 6 " " " " " "

Note-Pads #4-#11 are high order addresses $8-$F. Any of the above IC's may be strapped to any high order address.

STRAP	IDENTIFICATION OR FUNCTION
21-20*	Select group 1 restart vectors, IC 6
21-22	" " 2 " " , "
21-20 & A03 low	" " 3 " " , "
21-22 & A03 low	" " 4 " " , "

Note-See section covering restart vector selection for further discussion.

STRAP	IDENTIFICATION OR FUNCTION
45-46* 47-48* 49-50*	Select address $E000 as lower limit for on-board location. For example, cutting 47-48 and installing 47-23, would set lower limit for on-board address at $A000
24-25*	Exclude addresses $F400-$F7FF from on-board location
28-29* 29-30*	Connect X1 and X2 inputs together on IC 18 for Crystal Oscillator option
32-33*	Bus drivers enabled by BA signal
31-32	" " " at all times
51-52*	Ground ext input to 6875 clock driver
54-55*	Select ÷16 clock frequency on baud rate generator
56-58*	" " " " " " " "
58-59*	" " " " " " " "
62-63*	Halt input enable to CPU
64-65	NMI enable for off-board addresses
66-67*	Bus phase 1 clock enable
68-69*	" 150 baud clock enable
71-72*	" 110 " " "
70-73*	Bus BA signal enable

* Standard Configuration for MSI-6800 Computer

MSI 6800 COMPUTER, CP-1 CPU

PARTS LIST

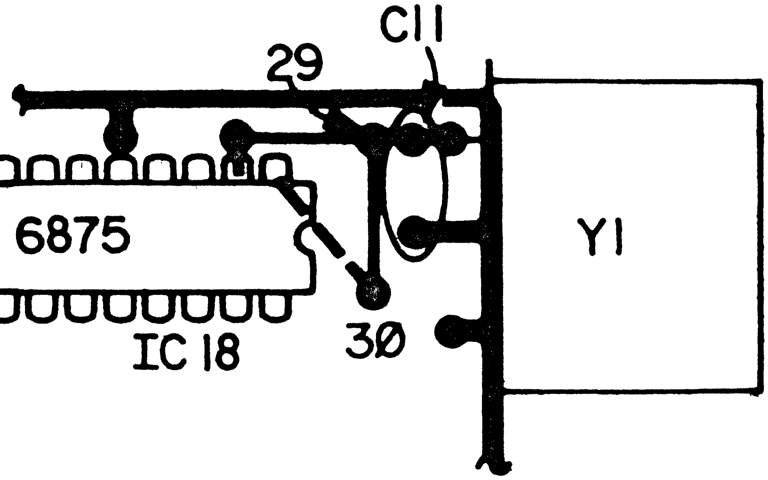
ITEM NO.	QTY.	DESCRIPTION	REFERENCE DESIGNATION	MSI PART NO.
1	1	PCB, CP-1, CPU		979
4	1	RESISTOR,120	R14	009
5	13	RESISTOR,6.8K	R1 thru R6,R9 thru R13,R15,R16	030
6	1	RESISTOR,39K	R17	038
7	1	RESISTOR,1MEG	R18	057
9	1	CAP.,Disc,120pf	C11	194
10	11	CAP.,Disc,.01uf,25V	C1,C3,C4,C5,C7,C9, C12 thru C15,C18	156
11	1	CAP.,Disc.0.1uf,25V	C10	159
12	1	CAP.,Electro.,2.2,uf, 50V, Radial	C6	1203
13	4	CAP.,Electro.,25uf,25V	C2,C8,C16,C17	177
17	1	CRYSTAL,1.8432 MHz	Y2	834
18	1	CRYSTAL,3.579 MHz	Y1	923
20	1	IC, 2708,PROM,MT-1 Monitor	IC28	MT-1
21	1	IC, 6800	IC11	397
22	1	IC, 6810	IC5	387
23	1	IC, 6875	IC18	393
24	1	IC, 7400	IC25	201
25	2	IC, 7402	IC4,IC10	203
26	3	IC, 7404	IC8,IC14,IC26	205
27	1	IC, 7420	IC22	221
28	1	IC, 7430	IC2	231
29	2	IC, 74S138	IC3,IC7	339
30	1	IC, 7805,+5V Regulator	IC1	495
31	1	IC, 7812,+12V Regulator	IC21	469
32	1	IC, 7905,-5V Regulator	IC9	493
33	2	IC, 8T26	IC24,IC27	428
34	3	IC, 8T97	IC12,IC15,IC19	420
35	1	IC, 8T98	IC17	419
36	1	IC, 82S123	IC6	445
37	1	IC, 14411	IC23	399
39	1	SOCKET, 16 Pin		705
40	6	SOCKET, 24 Pin		706
41	1	SOCKET, 40 Pin		727
43	5	CONNECTOR, 10 Pin, F.G.		1043
44	1	KEYING PIN, Molex		1051
45	3	HEATSINK		1822
46	3	SCREW, 4-40 x 3/8, B.H.M.		716
47	3	NUT, 4-40, Hex		714
48	3	WASHER, #4, I.T.L.		744

Note:
The following parts are optional and are not normally supplied with the parts kit. They may be installed by the user if desired

3	2	RESISTOR,20	R7,R8	067
15	2	DIODE,1N4003	D1,D2	102

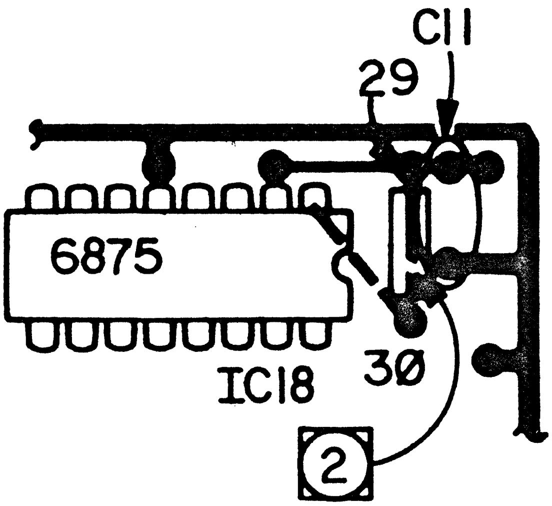
Note:
All resistors are in ohms, ± 10%, 1/4 W unless otherwise specified

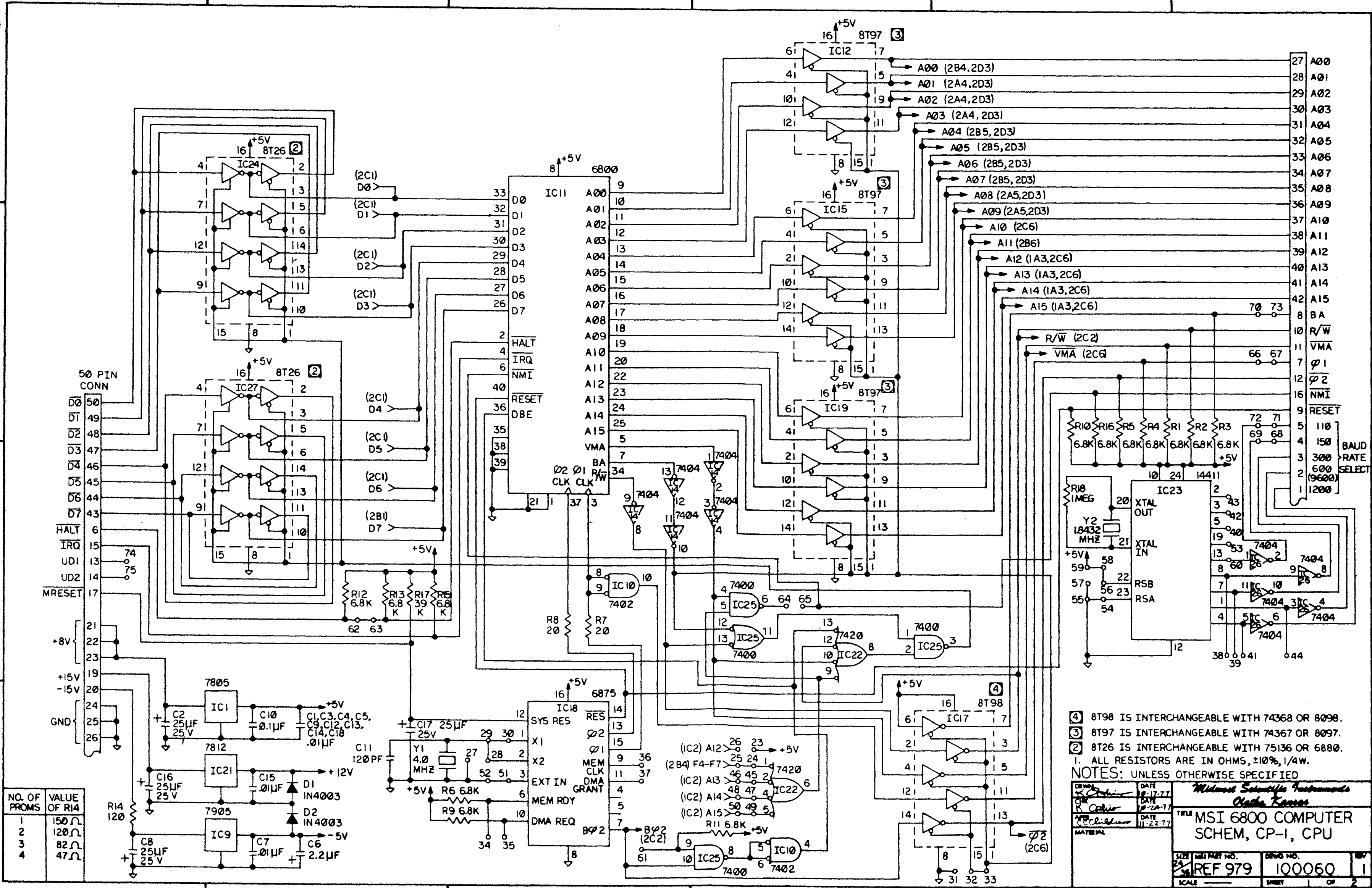
STANDARD CONFIGURATION FOR CLOCK DRIVER CIRCUIT AS FOLLOWS:



OPTIONAL CONFIGURATION FOR RC TIMING CIRCUIT AS FOLLOWS:

1. REMOVE CRYSTAL, Y1.
2. CUT ETCH BETWEEN JUMPER PADS 29 & 3Ø.
3. INSTALL APPROPRIATE RESISTOR IN JUMPER PADS 29 & 3Ø.
4. REMOVE GIVEN CAPACITOR FROM C11.
5. INSTALL APPROPRIATE CAPACITOR AT C11.





NO. OF PROMS	VALUE OF R14
1	150Ω
2	120Ω
3	82Ω
4	47Ω

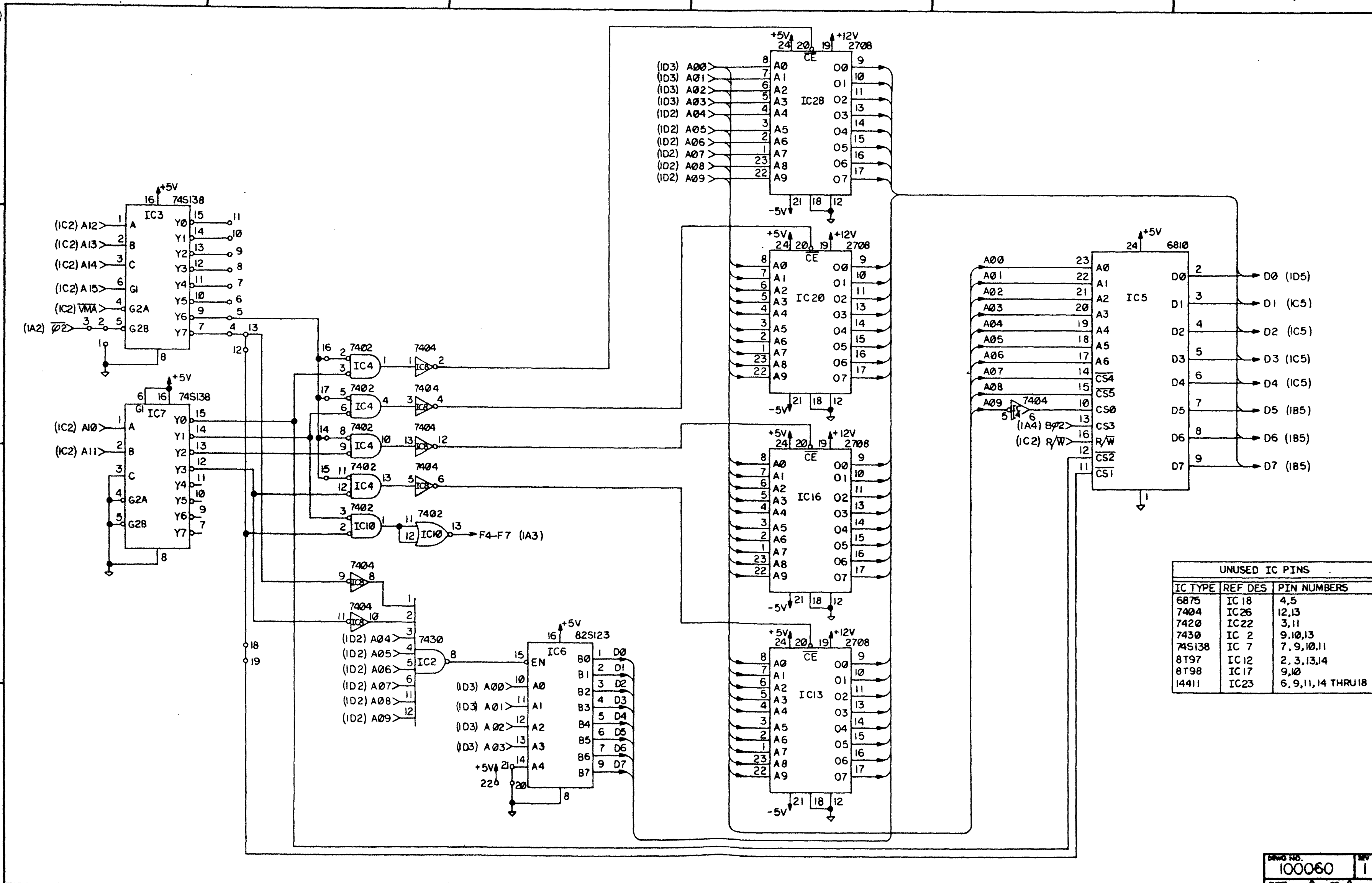
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, ±10%, 1/4W.
2 8T26 IS INTERCHANGEABLE WITH 75136 OR 6880.
3 8T97 IS INTERCHANGEABLE WITH 74367 OR 8097.
4 8T98 IS INTERCHANGEABLE WITH 74368 OR 8098.

Midwest Scientific Instruments
Olathe, Kansas

TITLE MSI 6800 COMPUTER SCHEM, CP-1, CPU

DRAWN	DATE 8-17-77
CHK	DATE 8-24-77
APPD	DATE 11-22-77
MATERIAL	

SIZE	MSI PART NO.	DRWG NO.	REV
24x36	REF 979	100060	1
SCALE		SHEET 1 OF 2	

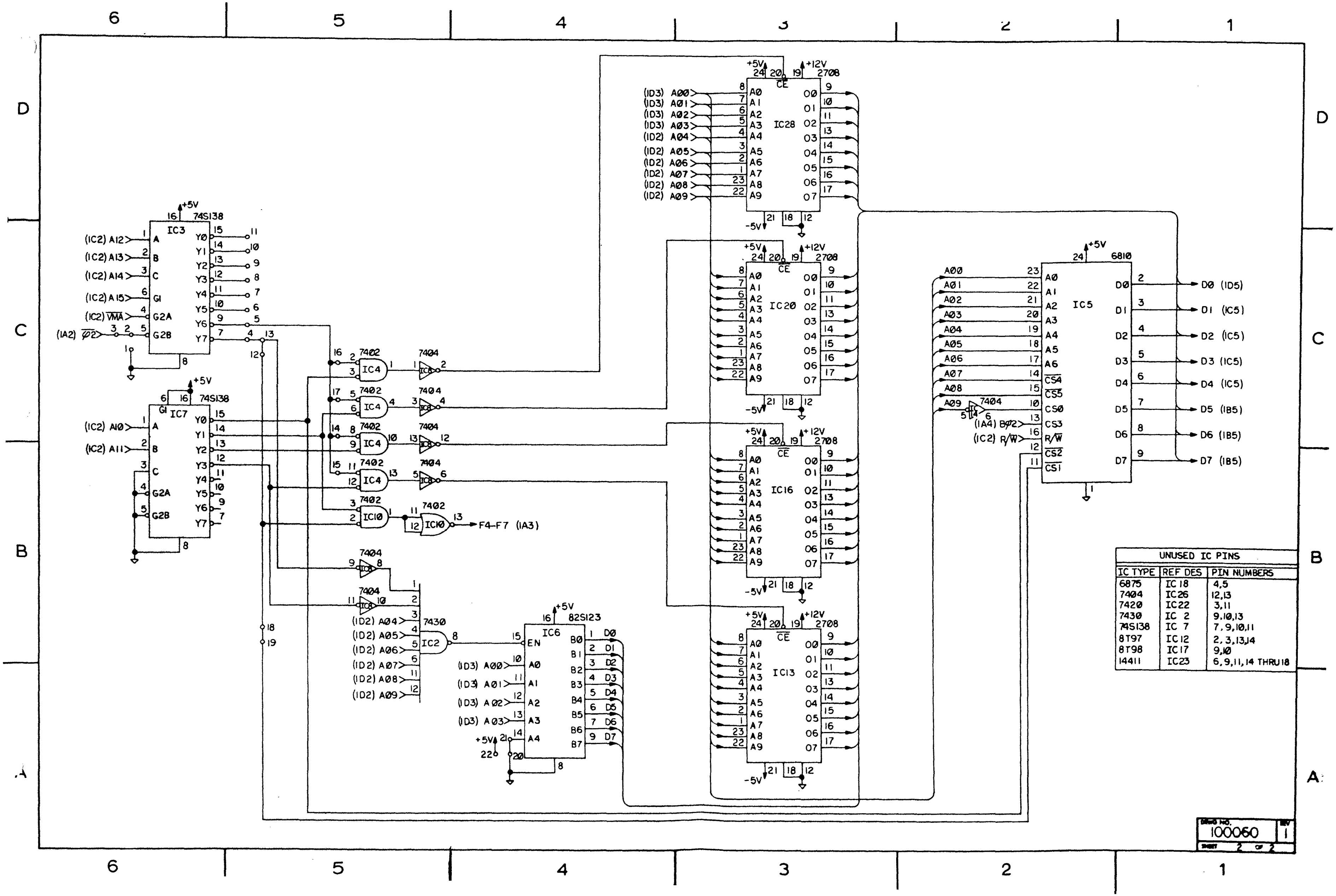


UNUSED IC PINS

IC TYPE	REF DES	PIN NUMBERS
6875	IC 18	4,5
7404	IC26	12,13
7420	IC22	3,11
7430	IC 2	9,10,13
74S138	IC 7	7,9,10,11
8T97	IC12	2,3,13,14
8T98	IC17	9,10
14411	IC23	6,9,11,14 THRU18

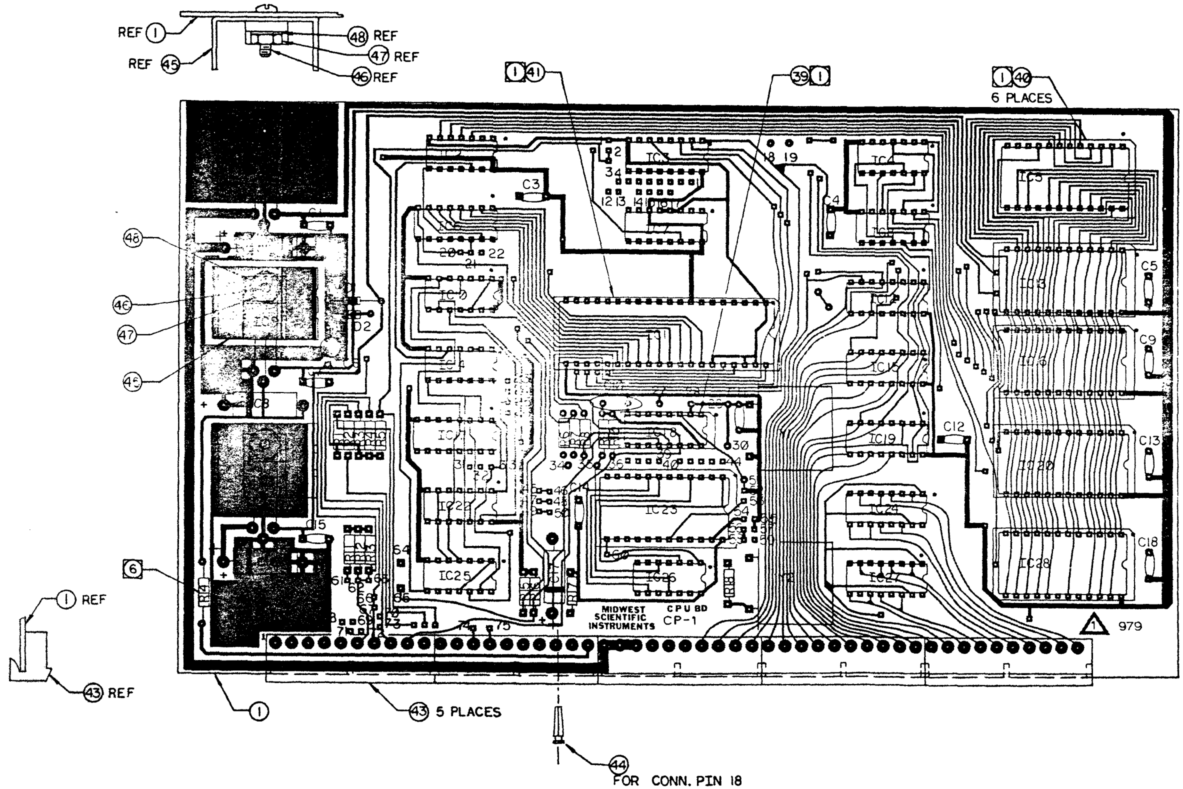
DWG NO. 100060 REV 1

SHEET 2 OF 2



UNUSED IC PINS		
IC TYPE	REF DES	PIN NUMBERS
6875	IC 18	4,5
7404	IC26	12,13
7420	IC22	3,11
7430	IC 2	9,10,13
74S138	IC 7	7,9,10,11
8T97	IC12	2,3,13,14
8T98	IC17	9,10
14411	IC23	6,9,11,14 THRU 18

DWG NO. 100060 REV 1
SHEET 2 OF 2



ITEM	QTY	PART NUMBER	DESCRIPTION	REF DES	MSI P. N.
48	3		WASHER, #4 I.T.L.		744
47	3		NUT, 4-40, HEX		714
46	3		SCREW, 4-40 X 3/8, BHM		716
45	3		HEATSINK		1822
44	1		KEYING PIN, MOLEX		1051
43	5		CONNECTOR, 10 PIN, F, G		1043
41	1	(1)	SOCKET, 40 PIN		727
42	6	(1)	SOCKET, 24 PIN		706
39	1	(1)	SOCKET, 16 PIN		705
37	1	14411	IC	IC23	399
36	1	82S123	IC	IC6	445
35	1	(5) 8T98	IC	IC17	419
34	3	(4) 8T97	IC	IC12, IC15, IC19	420
33	2	(3) 8T26	IC	IC24, IC27	428
32	1	7905	IC, -5V REGULATOR	IC9	493
31	1	7812	IC, +12V REGULATOR	IC21	469
30	1	7805	IC, +5V REGULATOR	IC1	495
29	2	74S138	IC	IC3, IC7	339
28	1	7430	IC	IC2	231
27	1	7420	IC	IC22	221
26	3	7404	IC	IC8, IC14, IC26	205
25	2	7402	IC	IC4, IC10	203
24	1	7400	IC	IC25	201
23	1	6875	IC	IC18	393
22	1	6810	IC	IC5	387
21	1	6800	IC	IC11	397
20	1	(6) 2708	IC, PROM, MT-1 MONITOR	IC28	
18	1		CRYSTAL, 3.579 MHZ	Y1	923
17	1		CRYSTAL, 1.8432 MHZ	Y2	834
15	2	IN4003 (1)	DIODE	D1, D2	102
13	4		CAP, ELECTRO., 25µF, 25V	C2, C8, C16, C17	177
12	1		CAP., ELECTRO., 2.2µF	C6	1203
11	1		CAP., DISC, 0.1µF, 25V	C10	159
10	11		CAP., DISC, .01µF, 25V	C1, C3, C4, C5, C7, C9, C12 THRU C15, C18	156
9	1		CAP., DISC, 120 PF	C11	194
7	1		RESISTOR, 1MEG, ±10%, 1/4W	R18	057
6	1		RESISTOR, 39K, ±10%, 1/4W	R17	038
5	13		RESISTOR, 6.8K, ±10%, 1/4W	R1 THRU R6, R9 THRU R13, R15, R16	030
4	1	(6)	RESISTOR, 120, ±10%, 1/4W	R14	009
3	2	(1)	RESISTOR, 20, ±10%, 1/4W	R7, R8	067
1	1		PCB, CP-1, CPU		979

PARTS LIST

(6) NO. OF PROMS (2708)	1	2	3	4
VALUE OF R14	150	120	82	47

(5) 8T98 IS INTERCHANGEABLE WITH 74368 OR 8098.

(4) 8T97 IS INTERCHANGEABLE WITH 74367 OR 8097.

(3) 8T26 IS INTERCHANGEABLE WITH 75136 OR 6880.

2. ALL RESISTORS ARE IN OHMS.

(1) OPTIONAL PARTS.

NOTES: UNLESS OTHERWISE SPECIFIED

REV	ZONE	DESCRIPTION	DR	CK	APR	DATE
1		UPDATED TO MATCH ETCH				11-30-77

REVISIONS

DRWN K. Ophir DATE 11-8-77
CHK K. Ophir DATE 11-16-77
APPR DOL DATE 11-30-77
MATERIAL

Midwest Scientific Instruments
Olathe, Kansas

TITLE MSI 6800 COMPUTER ASSY, CP-1, CPU

SIZE 24 x 36 | MSI PART NO. REF 979 | DRWG NO. 100064 | REV 1

SCALE 2/1 | SHEET 1 OF 1