Theory of Operations

Overview

This chapter describes the 8086 16-bit processor board. The 8086 16-bit board fits into the expansion board connector on Attache's main processor board, providing access to the system bus.

The following section describes the overall Attache 8:16 system flow. Subsequent sections describe in detail the individual logic sections of the 8086 16-bit board, which include: the 8086 CPU (Central Processing Unit) and associated control logic, 256K bytes of RAM (Random Access Memory), interface circuitry to the Z-80A main processor board, and optional circuitry. Optional circuitry includes the GPIB controller (General Purpose Interface Bus), the serial synchronous port, and the 8087 numeric coprocessor.

Hardware modifications upon Attache to construct Attache 8:16 include a secondary board connected to the 8086 16-bit board, a high-resolution graphics board fit onto the Z-80A main processor board, and alterations to the display circuitry on the main processor board. These modifications are described in the final sections of this chapter.

Schematics of the 8086 16-bit board, secondary board, graphics modification, and display modification are located in Appendix A. Specific chips are identified in this chapter by their schematic location number in parenthesis, as well as by their manufacturer's part number. Note that the manufacturers identified in this manual are for the primary chip source.

Logic Overview

The logic sections on the 8086 16-bit board are the processor, the RAM (Random Access Memory), the Z-80A interface, and circuitry for optional features.

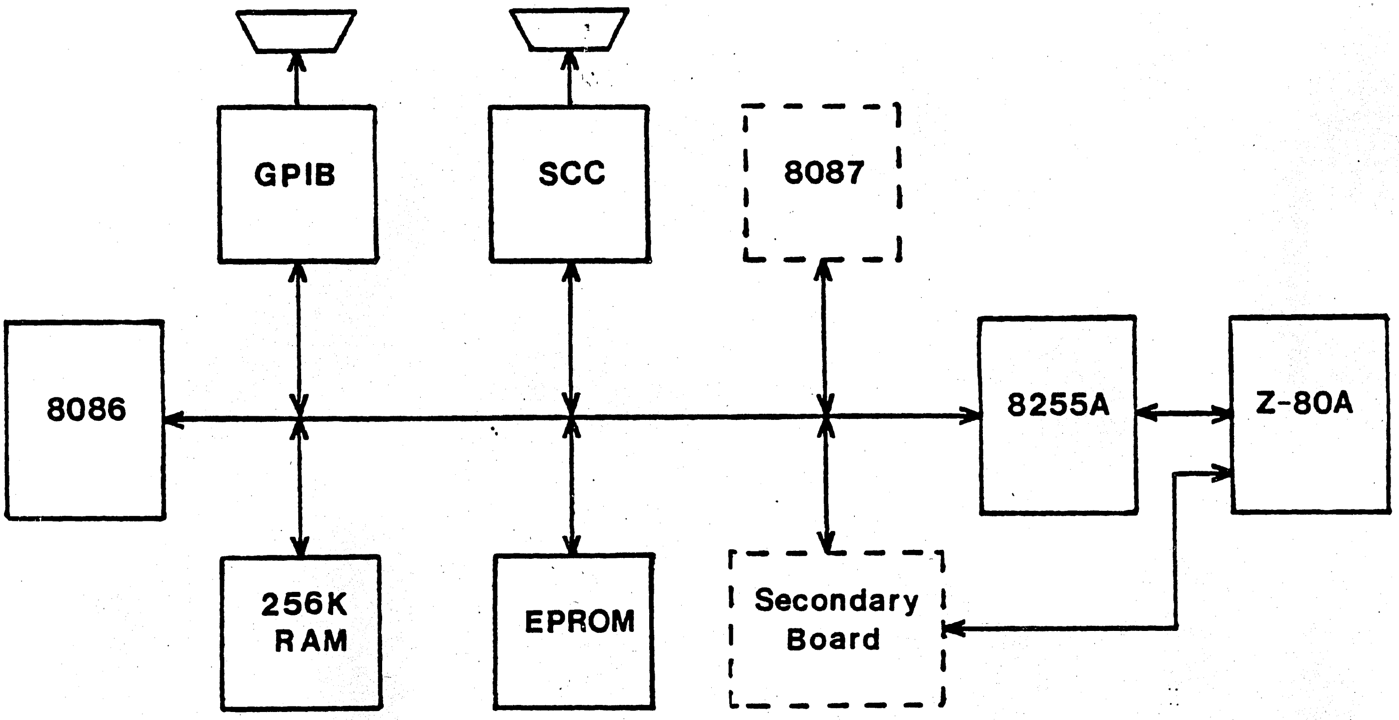
The CPU circuitry consists of an 8086, a clock generator, a wait state generator, and a processor command decoder. The 8086 processor is a true 16-bit processor with 20 address lines, capable of addressing up to 1 Megabyte of RAM.

The 8086 16-bit board contains 256K bytes of dynamic RAM, a capacitive method of storage which requires periodic refreshes.

A socket is located in parallel with the 8086 processor. This socket can contain either an 8087 numeric coprocessor or a secondary board. The secondary board issues hardware interrupts that allow Attache 8:16 to emulate IBM-PC hardware.

All interface between the Z-80A and the 8086 is handled through an 8255A interface chip. The Z-80A operates basically as an Input/Output handler, with the capability to interrupt the 8086. The 8086 cannot interrupt the Z-80A. The Z-80A/8086 interface is described in detail in the following section.

In addition to the 8087, optional features of the 8086 16-bit board include a synchronous serial port, and a GPIB (General Purpose Interface Bus) controller. These options are described in following sections.



System Block Diagram

Z-80A/8086 Interface

The Z-80A handles all low-level I/O in the system: character input and output buffering, disk reads and writes, and console (display and keyboard) activity. The 8086 BIOS (Basic Input Output System) converts DOS requests into requests to the Z-80A. The 8086 does very little I/O processing itself.

All data transfers are either data reads from the I/O devices on the Main Processor Board (via the Z-80A) or data writes from the 8086 to the Z-80A I/O devices.

Where possible, write commands (from 8086 to Z-80A) take advantage of the dual processor system. The 8086 does not wait for completion status of a given command, allowing simultaneous I/O processing. Read commands (from Z-80A to 8086) require the 8086 to wait for completion.

The two processors communicate through a single 8-bit parallel port. Since all transfers (commands, status, and data) flow through this port, a master/slave communication protocol is required. The 8086 acts as the master; all actions are the result of 8086 commands. The Z-80A receives commands, parameters and data, and returns data and status.

Interface with the Attache Z-80A bus is handled by an Intel 8255A Programmable Peripheral Interface chip. The 8255A has 24 I/O pins, which are programmed as two groups of 12 pins. One group operates in MODE 2 (a bidirectional mode using eight lines for a bus and five lines, borrowing one from the other group, for handshaking), and the other group operates in MODE 0 (which is programmed for output).

The Z-80A can interrupt the 8086, but the 8086 cannot interrupt the Z-80A. (The secondary board can interrupt the Z-80A, which places the 8086 into a wait state.) When the 8086 requires data from the Z-80A interface, it pulls signal INTREQ true. The Z-80A detects this flag, retrieves the requested information, and passes it to the 8086 via the 8255A.

The Z-80A is constantly operating as an I/O handler, handling all of the Z-80A board devices and awaiting INTREQ from the 8086.

Port assignments are as follows:

100	Port A - Read/Write
102	Port B - Read/Write
104	Port C - Read/Write
106	Control Port - Write only

Port A is used for bidirectional interface with the Z-80A bus.

Port B Bits 0 - 3 are used by the interrupt controller logic to mask out interrupts. Bit 4 enables WAIT logic, and Bit 5 is connected to J4 to enable or disable high-resolution graphics (1 = medium resolution, 0 = high resolution).

Port C Bits 3-7 contain PORT A status information as follows:

Bit 3	Interrupt request to 8086 if ON
Bit 4	Interrupt enable associated with IBF
Bit 5	IBF (Input Buffer Full) if ON
Bit 6	Interrupt enable associated with OBF/
Bit 7	OBF/ (Output Buffer Full) if low
Bit 0	DSR/ (Data Set Ready) from serial interface

Port C Bits 4 and 6 can be set or reset by writing to the control port as follows:

109H	Set IBF interrupt enable
108H	Clear IBF interrupt enable
10DH	Set OBF interrupt enable
10CH	Clear OBF interrupt enable

0C1H is written to the control port to initialize the 8255A with Port A in MODE 2 and Port B in MODE 0 (output).

The 8255A can interrupt the 8086 at interrupt level 3.

Z-80A Ports

The Z-80A communicates with Port A of the 8255A as follows:

Z-80A Port	Read	Write
B8	Data	Data
B9	Status	Control

Status Bits:

Bit 0	1 = no data ready 0 = data ready for read
Bit 1	1 = ready to accept data 0 = not ready to accept data

Control Bits:

Bit 0	1 = Reset 8086 0 = Set 8086 to run state

The Z-80A/8086 interface which occurs during the system boot and during specific commands is described in Chapter 3.

8086 CPU

The CPU circuitry consists of an 8086 processor (U5), a clock generator (U11), a wait state generator (U27), and a processor command decoder (U28). Additionally, chip location U10's signal lines are in parallel with the 8086.

The secondary board connects to the 8086 16-bit board at socket U10. U10 may optionally be used to attach an 8087 numeric coprocessor instead of the secondary board. This option is called an Attache 8:16A, and features an 8087 coprocessor, but does not feature IBM compatibility. The 8087 is described in a following section in this chapter.

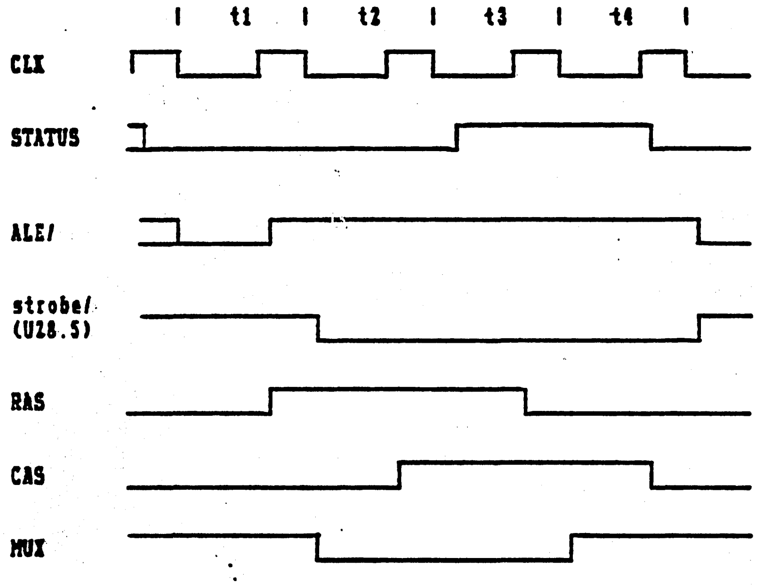
The 8086 (U5) is operated in maximum mode. The clock generator is an 8284A (U11) which derives its signal from a 24MHz crystal (X1) to provide an 8MHz, 1/3 duty cycle clock. Signal line /CLK is an inverted output from the 8284A, and DCLK is a twice-inverted delayed clock.

The 8284A (U11) also provides READY line synchronization. RAM cycles do not use wait states, except as provided by RAS/CAS circuitry during refreshes. For non-RAM cycles, wait states are provided according to the setting of jumper L on the output of flip-flop U27. In Attache 8:16, this jumper is connected to J to provide two wait states. When this jumper is connected from L to K, U27 generates a single wait state, L to J generates two wait states, and L to I generates three wait states.

Note that no bus controller chip is used. Instead, Address Latch Enable (ALE) is simulated by the flip-flop circuitry U62, U29, and U27. When ALE is high, addresses and status lines are allowed to settle. At the middle of T1, address and status lines have settled and are valid. The rising edge of the clock then sets ALE low, and address lines are latched by U16, U17 and U18, and the status lines are latched by an LS137 decoder (U28).

The LS137 decoder (U28) also decodes the status lines and provides strobed control lines which resemble 8288 bus controller lines. Control lines are enabled by U28 Pin 5, valid at the start of T2. For non-RAM cycles, U27 provides two wait states, as determined by the setting of jumper L.

Note that U28 is a socket which contains a header connecting to the secondary board. The LS137 decoder is actually U9 on the secondary board.



RAM Cycle

Dynamic RAM

The 64K x 1 dynamic RAM (Random Access Memory) chips comprise a 256K byte memory array on the 8086 16-bit board. Thirty-two chips (U34-41, U44-51, U54-61, U64-71) are organized into two 128K byte banks, addressed from 0 to 128K bytes and 128 to 256K bytes.

RAM address multiplexers (U25 and U26) multiplex 16 latched address lines (A1 - A16) into a row address and a column address. Gates U53 and U30 ensure that a RAM cycle is initiated on the rising edge of the clock during T1 when A18 and A19 are low (address 0 to 256K), and when a memory cycle has been indicated on 8086 status lines S0, S1, and S2.

Memory cycle timing is controlled by flip-flops U43 and U62. RAS (Row Address Strobe) is active for two clock cycles. CAS (Column Address Strobe) is also active for two cycles, but follows RAS by one cycle via the feed-back delay caused by U53 and U43.

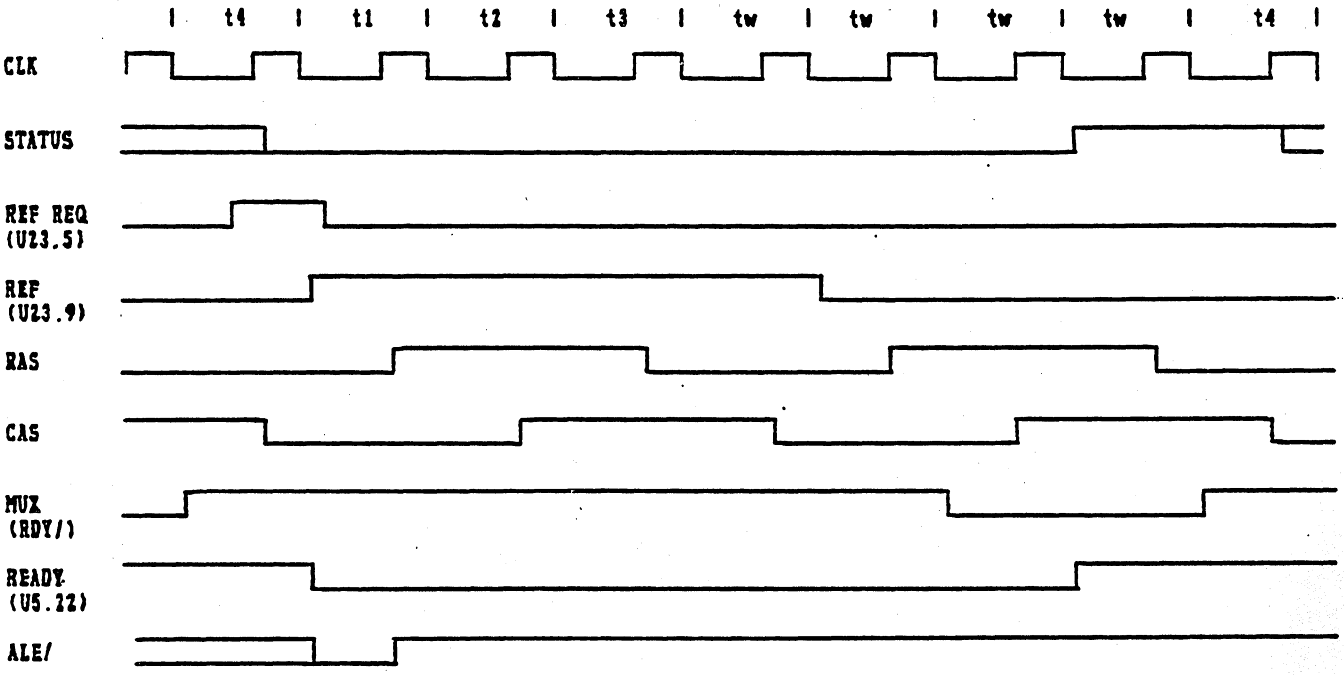
Signal line MUX toggles on the falling edge of RAS and CAS becoming active, which selects column address rather than row address from the U25 and U26 outputs.

Depending on the state of A17 (input to decoder U42), either signal RAS0 (driving the first 128K) or signal RAS1 (driving the second 128K) is generated by decoder U42 and gate U52. The 8086 can perform operations on a word (A0 and /BHE both low), on the high-byte only (A0 high /BHE low) or on the low-byte only (A0 low, /BHE high). OR gates in chip U29 control CAS for high-byte, low-byte or word operations, as required.

Counter (U14) divides the 8MHz system clock by 128, to provide a refresh request every 16 microseconds. A refresh is granted via flip-flop U23 Pin 9 when RAS and CAS are idle, which must occur within four clock cycles of a refresh request.

During refreshes, U25 and U26, the RAM address multiplexers, are disabled, and buffer (U24) is enabled. This gates the current refresh address from U15, an 8-bit counter which advances with every refresh request, onto the RAM address lines. RAS and CAS then perform a normal memory cycle sequence, except that signal line MUX remains high and CAS is blocked by NAND gate U72 so that CAS cannot reach the RAM.

During refresh cycles, memory cycles are held, which places the 8086 into a wait state. At the conclusion of the refresh cycle (when RAS and CAS are again inactive), flip-flop U23's output line REF is cleared. This allows any pending memory cycle to proceed, and consequently releases the 8086 wait state.



Refresh Cycle
(with delayed memory cycle)

Interrupt Structure

The Z-80A can interrupt the 8086, but the 8086 cannot interrupt the Z-80A. The secondary board interrupts the Z-80A and places the 8086 into a wait state during read/write operations to unique IBM-PC addresses. SINTR allows the Z-80A to interrupt the 8086 during timer tick interrupts (INT 1CH).

There are four signal lines capable of initiating on-board interrupts, depending on optional features which your 8086 16-bit board may contain. These interrupt lines are: the 8255A (PIO), the 8087 numeric processor extension (NPX), the Z8530 (SCC), and the TMS-9914A (GPIB). **Note:** When the secondary board is installed, PIO is driven by line SINTR (the interrupt signal from the Z-80A), and NPX is not applicable, as there is no numeric processor.

These interrupts can be masked by Port B Bits 0 - 3 of the 8255 as follows:

Bit 0	PIO
Bit 1	GPIB
Bit 2	SCC
Bit 3	NPX

An interrupt is allowed when the corresponding bit is set to one, and masked out if the bit is set to zero. Priority among any non-masked interrupt is determined by software. Fifteen interrupt vector locations (F0 - FE) are used. Each combination of interrupting device vectors form a unique location as follows:

With Secondary Board		With 8087	
F1	SCC GPIB SINTR	F0	NPX SCC GPIB PIO
F3	GPIB SINTR	F1	SCC GPIB PIO
F5	SCC SINTR	F2	NPX GPIB PIO
F7	SINTR	F3	GPIB PIO
F9	SCC GPIB	F4	NPX SCC PIO
FB	GPIB	F5	SCC PIO
FD	SCC	F6	NPX PIO
		F7	PIO
		F8	NPX SCC GPIB
		F9	SCC GPIB
		FA	NPX GPIB
		FB	GPIB
		FC	NPX SCC
		FD	SCC
		FE	NPX

Interrupt priority is then determined by which of the four routines each of these fifteen vectors indicate.

Interrupts are discussed in Chapter 3 of this manual.

TEST Circuit

The 8086 /TEST input, together with the WAIT instruction, can be used for synchronizing I/O to the NPX, SCC, GPIB, or PIO. If Bit 4 of the 8255 PORT B is set to one, the /TEST input is connected to signal line NPX BUSY, (Which NPX software expects). To use /TEST with other devices, bit 4 is set to zero, which essentially connects test to an interrupt request. By disabling 8086 interrupts and masking off all but the desired device, very fast transfers between the CPU and the SCC, GPIB, or PIO, can occur.

Optional Feature - Serial Port

The 8086 16-bit board has provisions for an optional serial port, which uses a Z8530 SCC (Synchronous Communications Controller) chip. The following ports are used:

144H	A	Control and Status
146H	A	Data
140H	B	Control and Status
142H	B	Data

RTxCA is connected to Pin 15 (transmit clock).

TRxCA is connected to Pin 17 (receive clock).

Only the A channel of the SCC chip is connected.

PCLK is driven at 4HMz. The SCC's baud rate generator divides the 4MHz clock to provide a 9600 baud rate.

Optional Feature - GPIB

A TMS9914A provides an optional GPIB (General Purpose Interface Bus) port. This GPIB port can be used to interface Attache 8:16 with the DA-10 Hard Disk Subsystem, a 10 Megabyte hard disk.

The following addresses are used as the TMS9914A registers:

Address {hex}	Read	Write
180	Int Status 0	Int mask 0
182	Int Status 1	Int mask 1
184	Address Status	
186	Bus Status	Auxiliary Command
188	Address Switch 1	Address Register
18A		Serial Poll
18C	Cmnd Pass Thru	Parallel Poll
18E	Data In	Data Out

Optional Feature - 8087

The 8087 Numeric Data Processor is a coprocessor that adds extensive high-speed numeric processing capabilities to the 8086. The 8087 performs arithmetic and logical operations on a variety of numeric data types.

The 8087 cannot coexist with the secondary board. (the board which fits onto the 8086 16-bit board and which makes the Attache 8:16 IBM compatible). The 8087 is an option available on the 8086 16-bit Processor Board instead of the IBM compatibility provided by the secondary board. A computer which contains this option is called an Attache 8:16A, and must be specially ordered from Otrona.

The Secondary Board - Overview

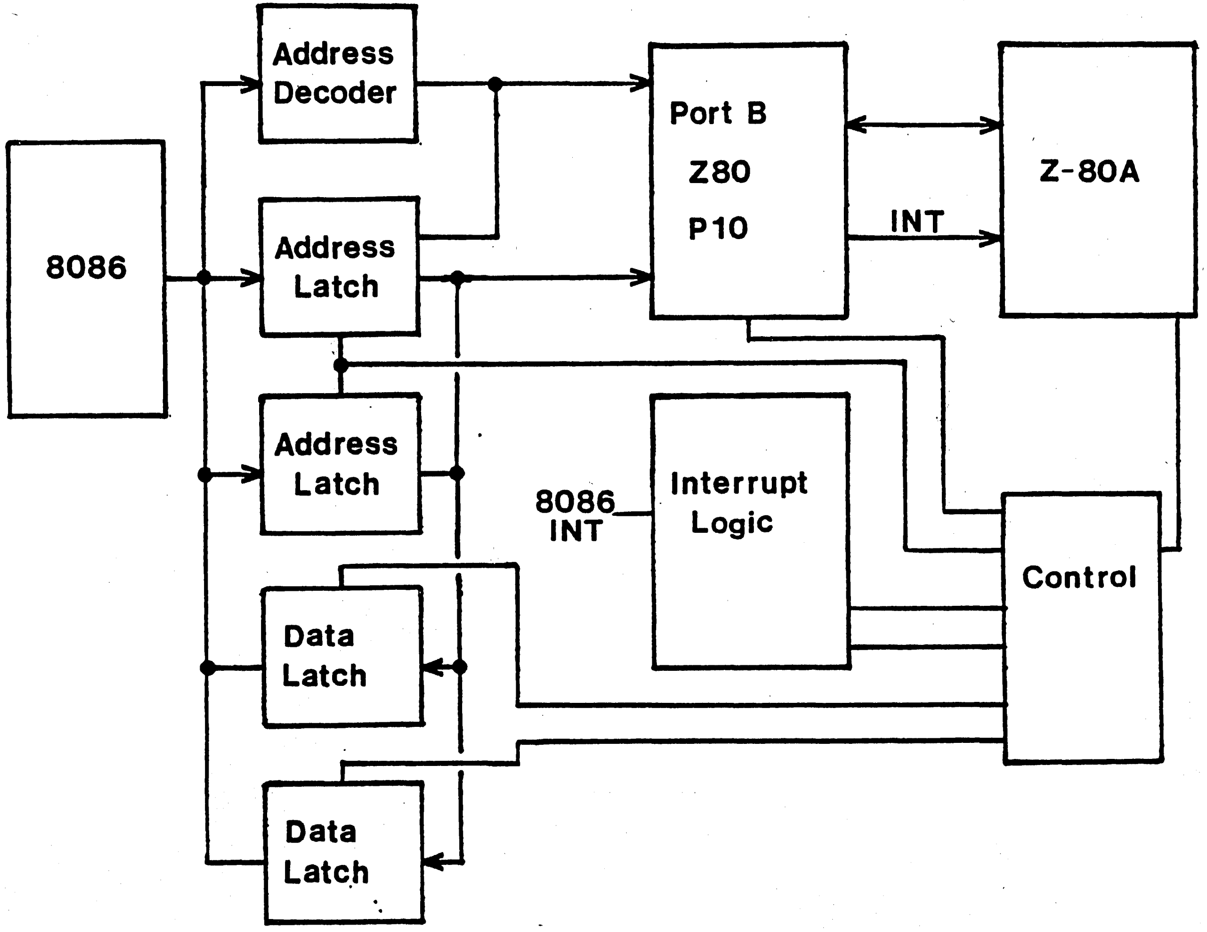
The secondary board on the 8086 16-bit board is designed to allow hardware which is not IBM compatible to be IBM compatible. The secondary board intercepts any 8086 requests that can be unique to IBM-PC hardware, and simulates this IBM-PC hardware.

To accomplish this PC simulation, the Z-80A is interrupted during 8086 I/O reads and writes **outside** the address range 0100-01FFH, and during 8086 memory reads and writes **inside** the range B0000-BFFFFH. When the Z-80A is interrupted, the 8086 is set into a wait state (via signal SRDY). The Z-80A interrupt service routine processes the respective read and write, simulating the IBM hardware, and then releases the 8086 from its wait state.

The process of interrupting the Z-80A during IBM-PC unique address calls is referred to as "trapping". The IBM-PC uses memory addresses B0000-BFFFFH for display memory and the 8086 16-bit board does not, so memory reads/writes in that range are trapped. The 8086 16-bit board uses I/O addresses in the range 0100-01FFH, which the IBM-PC does not, so all I/O read/writes except those in the identified range are trapped.

Initialization

Both ports of the Z-80A PIO (U8) operate in MODE 3, i.e., bidirectional bit-mode, and interrupts are enabled. (Port A is actually used as a 1-byte, 8-bit, bidirectional internal bus, but the port is initialized in bit mode to simplify the interrupt schemes.) Port B has two outputs, Bits 3 and 4, which are used to enable latch outputs onto the Port A bus. Bits 5 through 7 are inputs, used as the sources of interrupts. Bits 0 through 2 of Port B are inputs which indicate to the Z-80A how to process the interrupt.



Secondary Board Block Diagram

Address Decoding

As the 8086 executes code, it places addresses on lines AD0 through AD19 and strobes these addresses with ALE (Address Latch Enable, U9 Pin 4). The high- and low-order addresses are latched by U16 and U13 when ALE goes low.

The 8086 then puts data onto the AD0-AD15 lines, and continues operating unless the address is within the ranges that must be trapped. If the address must be trapped, the 8086 is placed into a wait state. The 8086 data is held on the bus for a write operation, or the 8086 waits to read data for a read operation. Note that regardless of whether or not the operation is trapped, U13 and U16 will have latched the address before any wait state occurs.

Two sets of address decoding logic are provided on the secondary board, each to detect the occurrence of one of two trapping conditions (either an 8086 memory read/write memory operation within addresses B0000H-BFFFFH, or an 8086 I/O read/write outside addresses 0100-01FFH).

The first set of address decoding logic detects memory addresses B0000-BFFFF {hex}. This logic consists of an LS20 (U6), two inverters (in U10 and U5), and an LS374 (U12). If the address output by the 8086 is in the range B0000H-BFFFFH, the output of the first LS20 gate is driven low.

Signal /S2 at a high state indicates that the address is a memory address, as opposed to an I/O address. /S2 ANDed with the inverted output of the first LS20 drives the output of the second LS20 low if this address is a memory address in the range B0000-BFFFFH. This low signal is then latched by U12 when ALE goes low. The output of this LS374 is the Bit 7 input of PIO Port B.

The second set of address decoding logic detects any I/O addresses which are not in the range 0100 through 01FF {hex}. This circuitry consists of two LS00 NAND gates (U10) and latch U12. The first NAND gate inverts AD9, thereby obtaining the proper level for the second NAND of U10.

If the I/O address is outside the range 0100-01FFH, the output of the second NAND goes high. This output is latched by the LS374 (U12) when ALE goes low. If the Pin 5 output of the latch is low, then the address is on the 8:16 board (i.e., within addresses 0100-01FFH).

The output of latch U12 is fed back (via signal line /8:16I/O) to the 8086 16-bit board to enable its address decoder when the address is on the 8086 16-bit board. If the output of the latch is high, then the address is not on the 8086 16-bit board and the 8086 address decoder is not enabled.

Latch U12's output is then NANDed with lines IOWR and IORD by the LS00 (U4). IOWR and IORD are the decoded and inverted outputs from the LS137 (U9). U4 consequently generates a signal indicating an I/O read or write outside 0100-01FFH to Bits 5 (I/O write) and 6 (I/O read) of PIO Port B.

Generating an Interrupt

The decoded signals /MEMACC (U12 output Pin 2, the decoded memory access signal within address range B0000 - BFFFF), /IORD, and /IOWR are the three inputs to the Z-80A PIO which cause it to interrupt the Z-80A (Port B, Bits 7, 6, and 5 respectively). The PIO issues an interrupt if any of the three inputs go low. This interrupt to the Z-80A causes it to jump to an interrupt service routine.

/MRD, /IORD, and /IOWR are decoded by U9 (the LS137) from 8086 inputs /S0 (U9 Pin 3), /S1 (U9 Pin 2), and /S2 (U9 Pin 1). /MRD is output on U9 Pin 10, /IORD on Pin 11, and /IOWR on Pin 13.

PIO inputs /IOWR, /IORD, and the /MEMACC signal are ANDed together by two LS08s (U3), so that any one of them going low causes the D input of U1 (half of an LS74 flip-flop) to go low. This input is then latched by the clock input (the output of the 8086 16-bit board wait state generator U27 Pin 6 inverted by an LS00 {U4}). This starts a synchronizing chain of LS74 flip-flops, which finally generates SRDY low, setting the 8086 into a wait state.

Decoding the Interrupt

With the 8086 in a wait state, the Z-80A interrupt service routine may now read Port B of the PIO to determine which Bit (5-7) caused the interrupt. It also reads Bits 0-2 of PIO Port B, which indicates how the interrupt should be handled. Bit 0 (/MWR) indicates whether the interrupt caused by a memory address in the range B0000-BFFFFH was a read or write operation, while Bits 1 and 2 (AD0 and BHE, latched by U12) indicate whether the data transfer was one or two bytes, according to the table below:

AD0	BHE	Bytes Transferred
0	0	Upper-byte on AD8-AD15 Lower-byte on AD0-AD7
0	1	Upper-byte only on AD8-AD15
1	0	Lower-byte only on AD0-AD7
1	1	No data is transferred

An LS138 (U7) appears as an I/O port to the Z-80A. It decodes the addresses of the PIO, and provides to the Z-80A a means to control the secondary board. The I/O map is as follows:

00-03H	CLEAR INTERRUPT TO 8086
04-07H	CLK Z-80A DATA INTO LOW BYTE LATCH
08-0BH	CLK 8086 DATA INTO U13 and U16
0CH	PIO PORT A DATA
0DH	PIO PORT A COMMAND
0EH	PIO PORT B DATA
0FH	PIO PORT B COMMAND/
10-13H	CLK Z-80A DATA INTO HIGH BYTE LATCH
14-17H	INTERRUPT THE 8086
18-1BH	UNUSED
1C-1FH	SET 8086 TO RUN STATE

The Z-80A reads the address that caused the interrupt (latched in U13 and U16) by using Bits 3 and 4 of the PIO to enable the output of these latches, and then reading Port A of the PIO for the data, one byte at a time. It then causes the 8086 data to be latched into these same latches by doing a dummy I/O write to address 08 - 0BH. The Z-80A can now use Bits 3 and 4 of the PIO Port B to enable the outputs of the latches, and then read the data into Port A of the PIO, one byte at a time.

If the cause of the interrupt was an I/O or memory read, the Z-80A must write data into U14 and U15 for the 8086. This is a one- or two-byte transfer, determined by the state of AD0 and BHE as read from the PIO Port B (listed in the preceding table.) This is accomplished by putting the data out on Port A of the PIO and latching it with a dummy write operation to I/O address 04-07H (for low-order bytes) or 10-13H (for high-order bytes). This data latching also sets U1 (the lower half of an LS74), which enables the output of these data latches onto the 8086 data bus.

Releasing the Interrupt

After the appropriate service has been performed, the Z-80A releases the 8086 from its wait state by doing a dummy write to an I/O address in the range 1C-1FH. This dummy write clears U1 (upper-half of an LS74) which clears SRDY.

The Z80 then executes a return from interrupt instruction. The 8086 now finishes the cycle it had started by reading the data that is on its bus from U14 and U15, if the operation was an 8086 read, or simply moving to the next instruction if it was a write.

The output of the LS08 that clocks the lower half of the LS74 (U1) goes low on either an /IORD or a /MRD. This readies the clock input for the positive-going transition that clocks the flip-flop. When the 8086 continues with its read operation, it brings /IORD or /MRD high, (the signal that caused the clock to go low). This low-to-high transition clocks the grounded D input to the output, causing /Q to go high. This, in turn, disables the output of U14 and U15, which completes the cycle and frees the bus. The next 8086 instruction is handled in the same manner.

To allow the Z80 to interrupt the 8086, the Y5 and Y0 outputs of the LS138 (U7) are tied to the Set and Reset inputs of half of an LS74 (U11) (and the 8086 must set 8255 Bit PB0 high). This flip-flop allows the Z80 to set the interrupt request to the 8086 by writing to addresses 14 - 17H and to clear the request by writing to 00 - 03H.

Additional logic on the secondary board is the LS08 (U3) on the M1 input to the PIO. Since the PIO interprets /M1 without an /IORO or /RD as a reset, the LS08 combines /RES with /M1 to reset the PIO when necessary.

25-Line Circuitry

The 25-line modification is a small circuit board with headers that fit into sockets U422 and U423. U422 is a 74LS157 which multiplexes the display's line number. The board contains this relocated multiplexer (U422) and a 6349 PROM which replaces an S283 counter (U423).

The S283 adder is used to remap the line and column address bits and output the unique character addresses to the character and attribute RAM chips.

The 25-line modification replaces adder U423 with a 6349 PROM, encoded to output to the character RAM the proper address for the line and column position of each character to be displayed.

A 25-line, 80 column display contains 2000 unique locations for characters (25 x 80 = 2000). The binary representation of 2000 is 2^{11}, which means that 11 address bits are required to address all 2000 locations. However, representing the column positions (80) in binary requires 2^7 (seven address lines) and the line number (25) requires 2^5 (five address lines). This results in 12 address lines, even though the upper address combinations of the columns and lines are not used ($2^7 = 120$; $2^5 = 32$)). The PROM is used to remap the 12 lines into 11 for optimized usage of RAM.

The PROM (U423) remaps the address bits by combining the upper three column address bits with all five line number address bits and reassigning the otherwise unused address combinations. Therefore, the lower four column address bits are allowed to input directly to the attribute and character RAM chips, while the PROM provides unique 7-bit outputs to any required address combination on its eight input lines.

High-Resolution Graphics Board

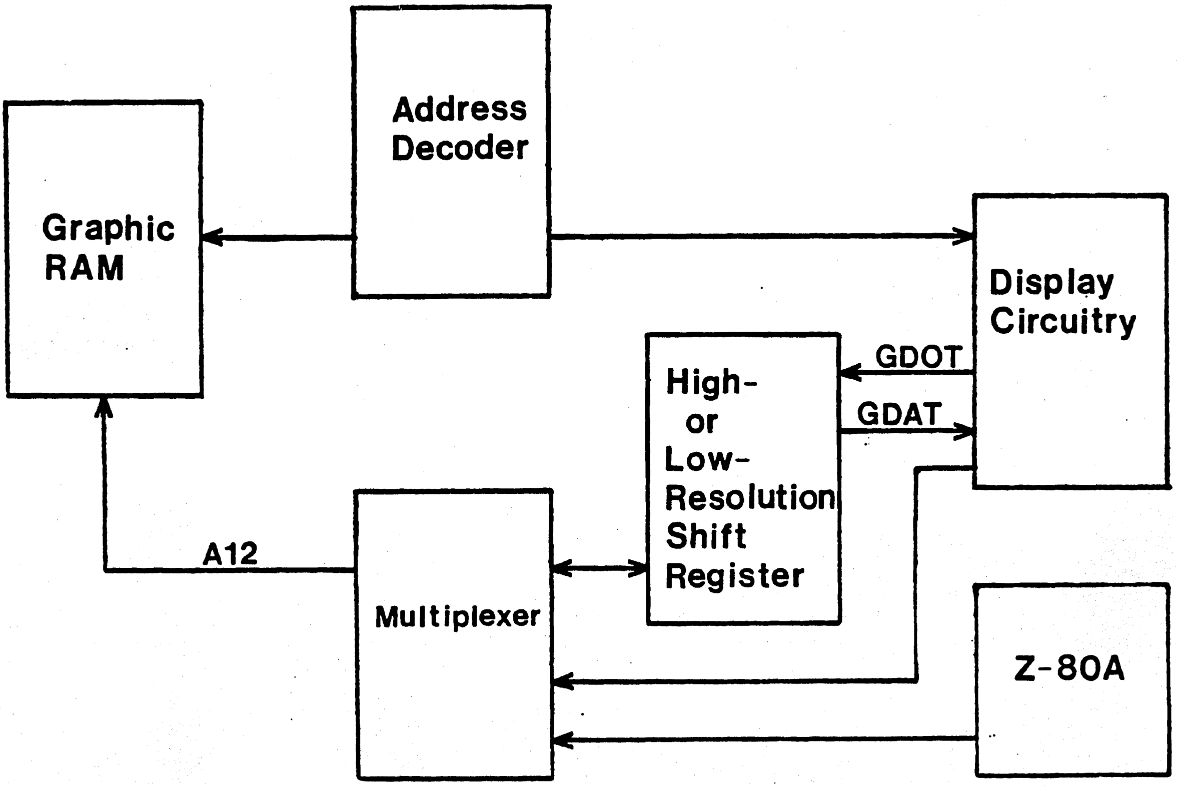
The high-resolution graphics board doubles the memory of the graphic RAM and provides the circuitry necessary to select between low-resolution and high-resolution graphics.

Hardware Modification

Several chips are removed from the Z-80A Main Processor Board, and are replaced with a graphics high-resolution board which plugs directly into the emptied chip sockets.

The modification removes the following chips: U703, an LS166 eight-bit shift register which serially outputs data to the display; U426, the LS138 address decoder which selects one of the graphic RAM chips (or the CRT controller, Attribute RAM or Character RAM); the five graphic RAM chips (MK4802's U704 - U708); and U416, a 2732 EPROM character generator.

The graphics high-resolution board contains three graphic RAM chips (HM6264's U6, U7, and U8), two 8-bit LS166 shift registers (U3 and U4), an LS138 decoder (U2), AND gates (LS08 U5), an LS153 multiplexer (U1), and a 2764 EPROM (U416). The board connects to the Z-80A Main Processor Board via connectors J1 through J7. Connector J1 fits into the U426 socket, J2 into the U703 socket, and J3 into the U708 socket, and J4 through J7 are hard-wired to the appropriate signal lines on the Z-80A processor board.



High-Resolution Graphics Block Diagram

Graphics Board Theory of Operations

The high-resolution graphics board replaces five 2K byte x 8-bit graphic RAM chips with three 8K byte x 8-bit chips. Since the graphics memory is doubled, the graphics board requires an additional address line, A12.

Address line A12 is input to graphic memory through multiplexer U1. This allows graphic memory to be selected by either the processor or the CRT (Cathode Ray Tube) controller. The CRT accesses graphics memory to display the current data via U1 input line R0, and the processor accesses graphics to update data via line A15.

Decoder U2 provides the chip selects to address RAM chip U6, U7, or U8. Additionally, U2 can select the attribute RAM (U432) or the character RAM (U433).

Multiplexer U1's enable line, Pin 14, selects between two 8-bit shift registers, U3 and U4. U3's input lines are coupled such that dots are addressed in pairs, as opposed to individually. U4's input lines select individual dots. When U1's Pin 14 enable is high, U3 is selected for medium-resolution. When Pin 14 is low, U4 is selected and high-resolution graphics is selected.

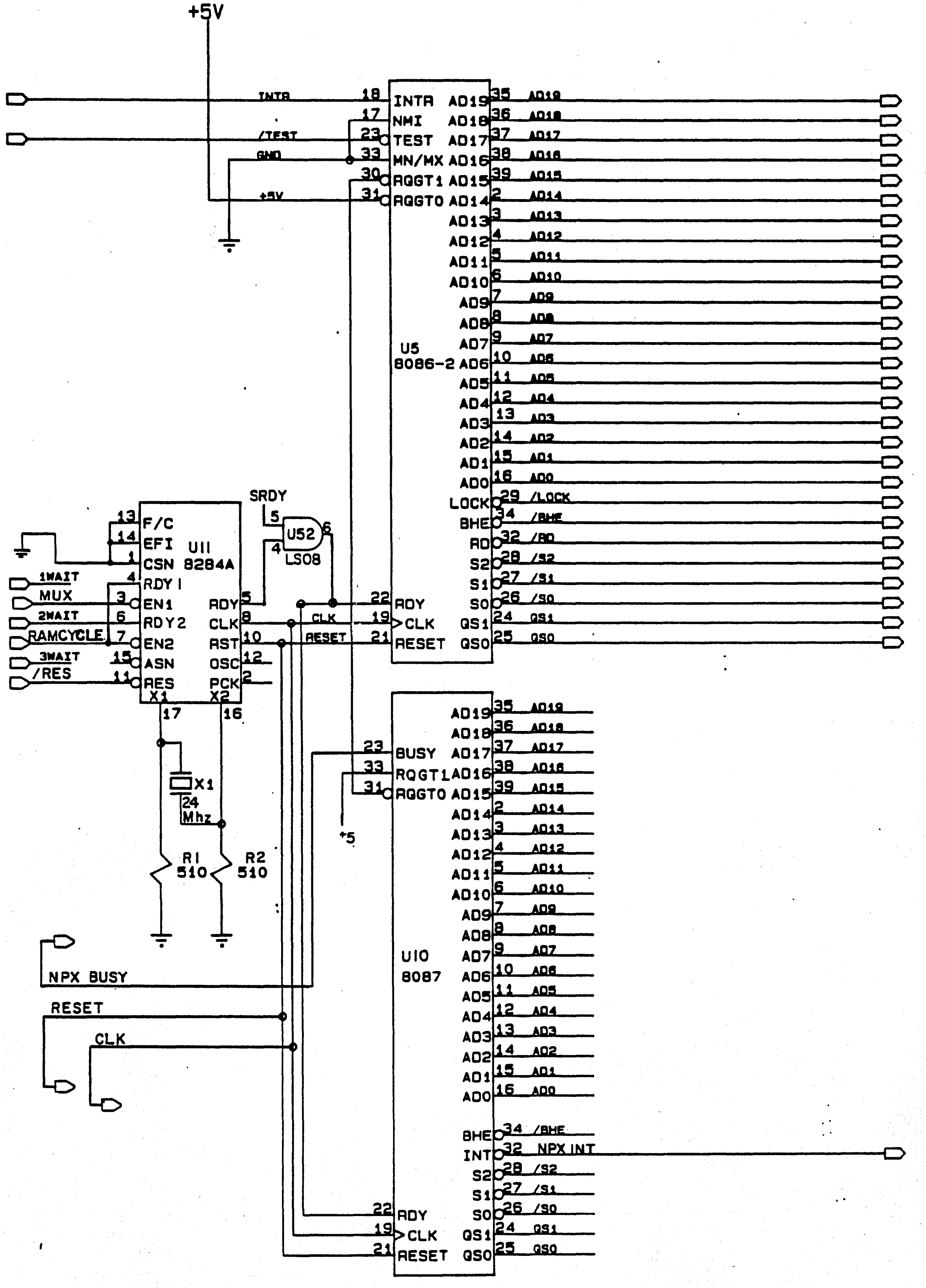
The shift registers (U3 and U4) are clocked by GDOT, which is input to the board through J2 Pin 7. Each GDOT clock pulse is the time that it takes to write one dot (pixel) to the display. The Pin 15 input to U3 and U4 select parallel load or serial output. When Pin 15 is low, the selected register loads data in parallel.

When Pin 15 is high, the selected register shifts serial graphic data out of Pin 13 to J2 Pin 13, which forms the display signal line GDAT, a direct output to the display interface circuitry.

Additional Circuitry

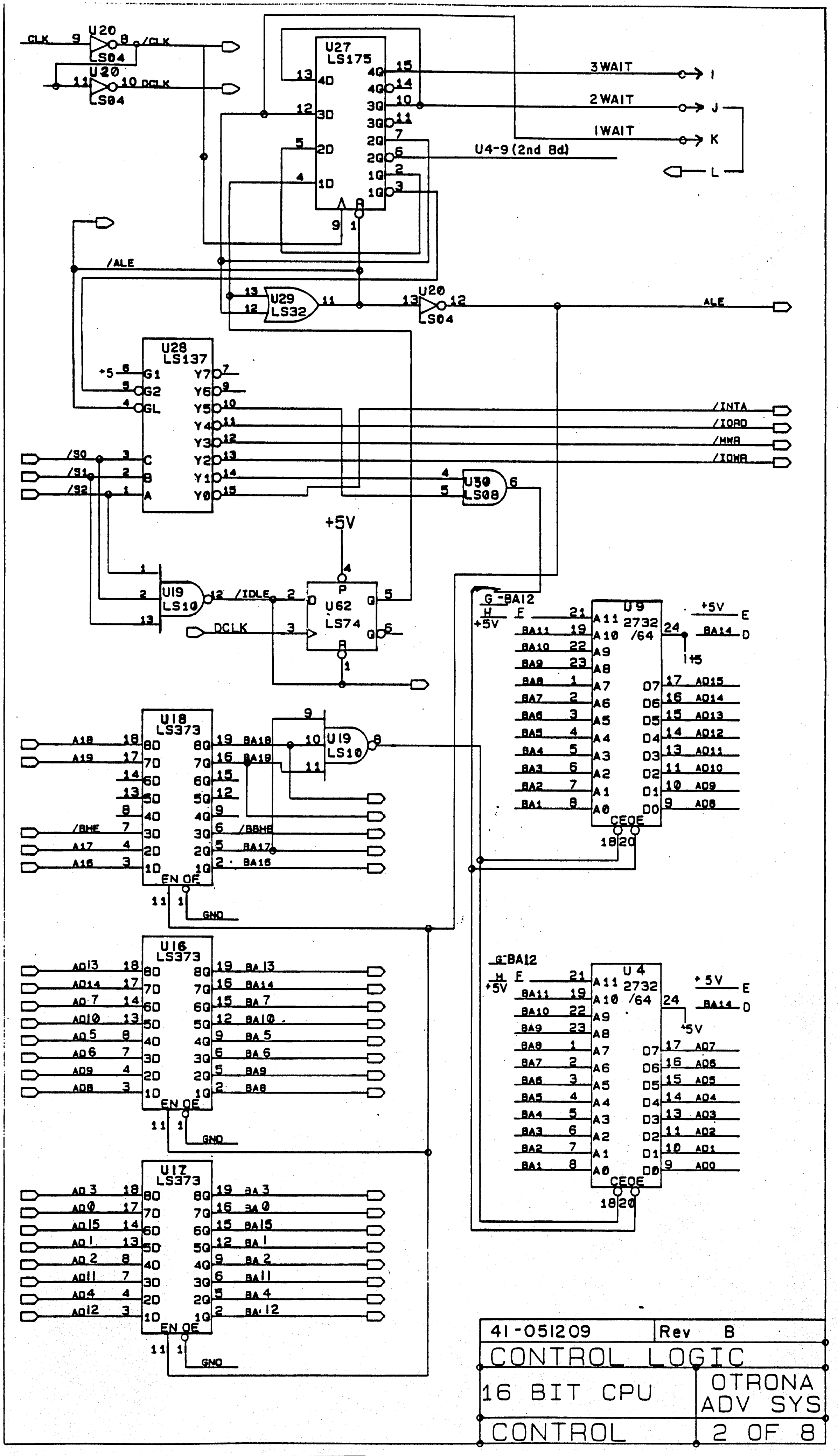
In addition to the circuitry provided by the high-resolution graphics board, EPROM U416 on the main processor board is replaced.

The new character generator EPROM (U416) contains the IBM character set, in addition to the complete ASCII character set and alternate character sets (Greek, mathematical symbols, business form and graph drawing symbols, German, Spanish, French, Italian, Swedish, and other alphabet symbols.)



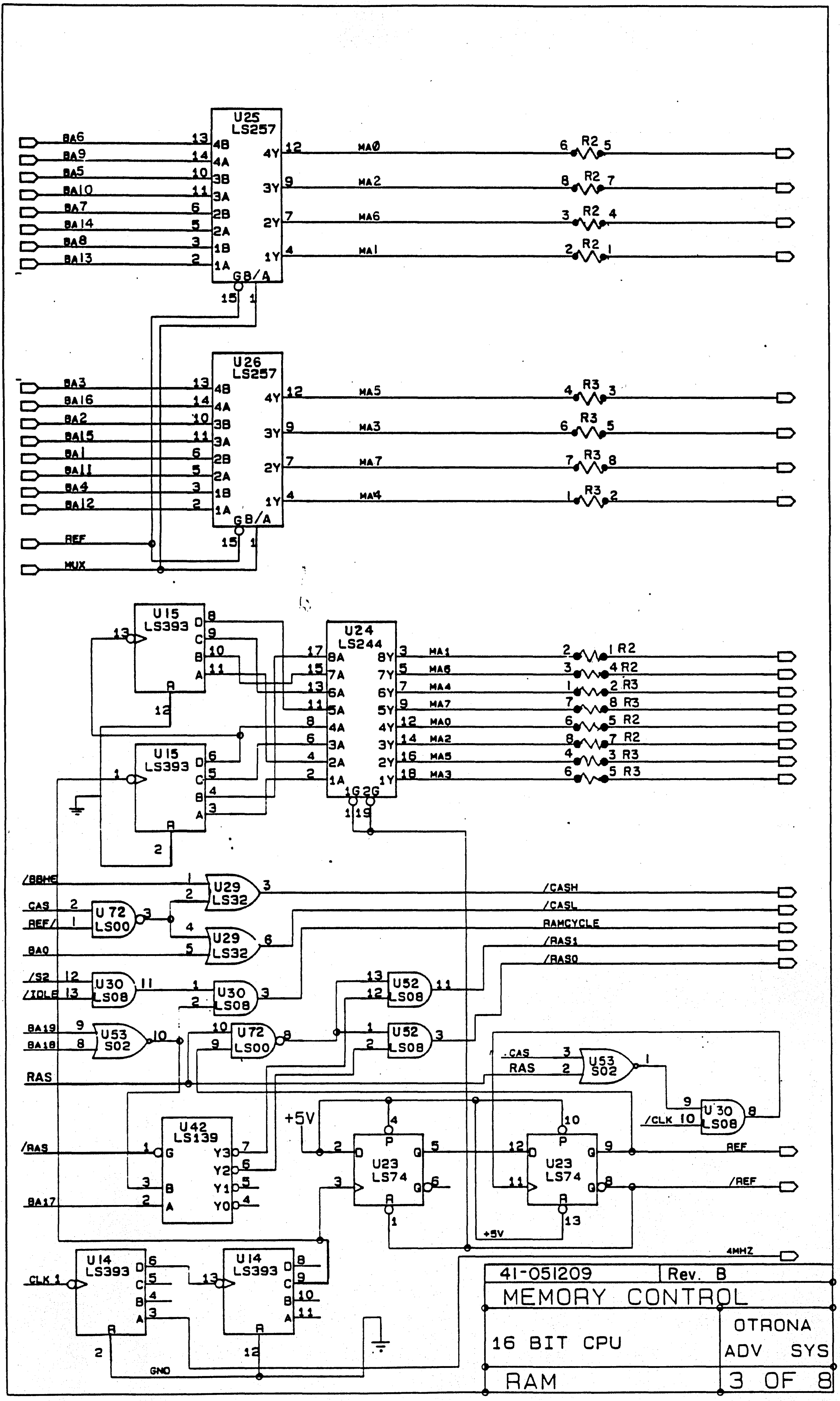
41-051209	Rev. B
PROCESSOR	
16 BIT CPU	OTRONA ADV SYS
CPU	1 OF 8

A1



41-051209	Rev B
CONTROL LOGIC	
16 BIT CPU	OTRONA ADV SYS
CONTROL	2 OF 8

A2



41-051209 Rev. B

MEMORY CONTROL

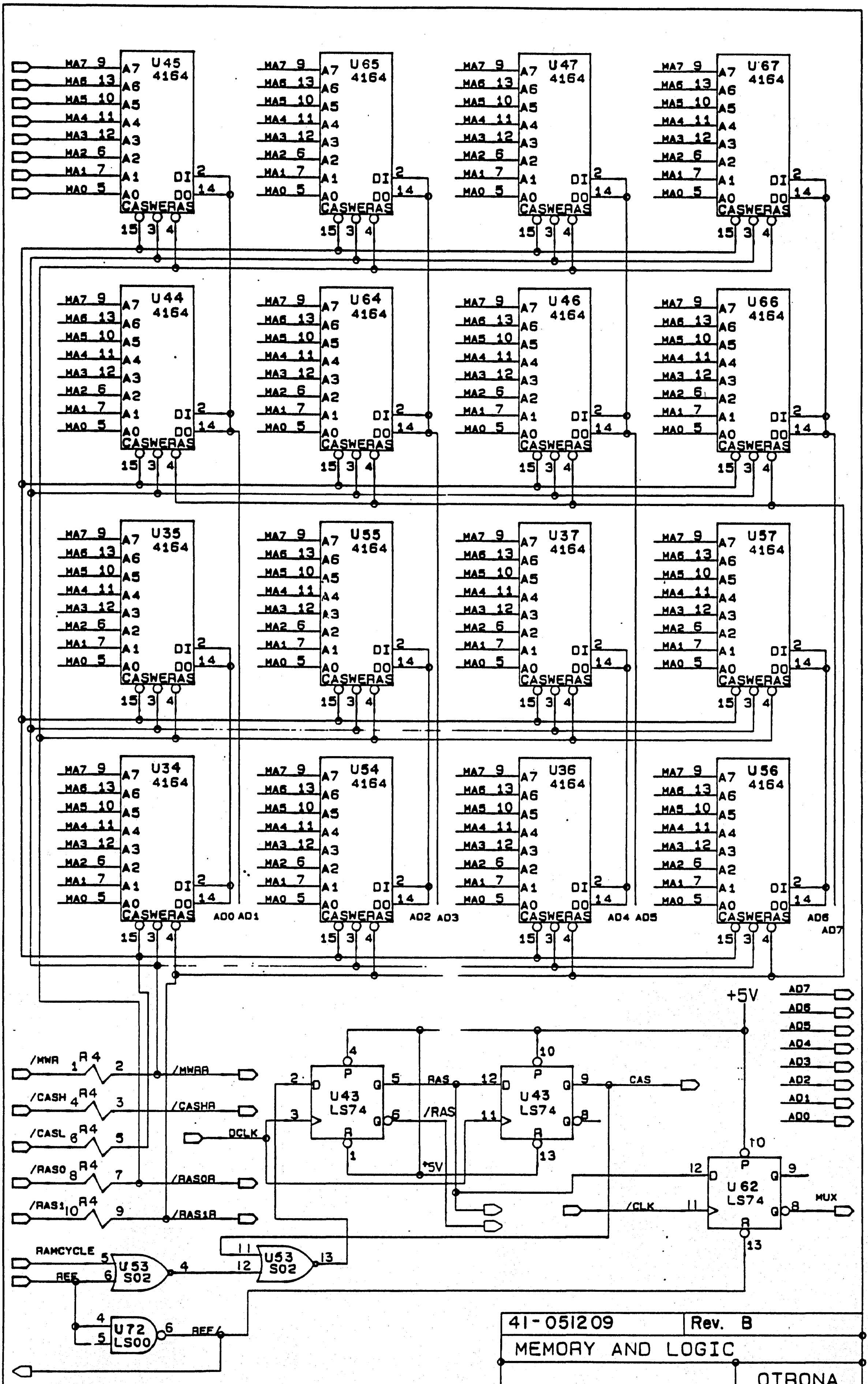
16 BIT CPU

OTRONA ADV SYS

RAM

3 OF 8

A3



41-051209 | Rev. B

MEMORY AND LOGIC

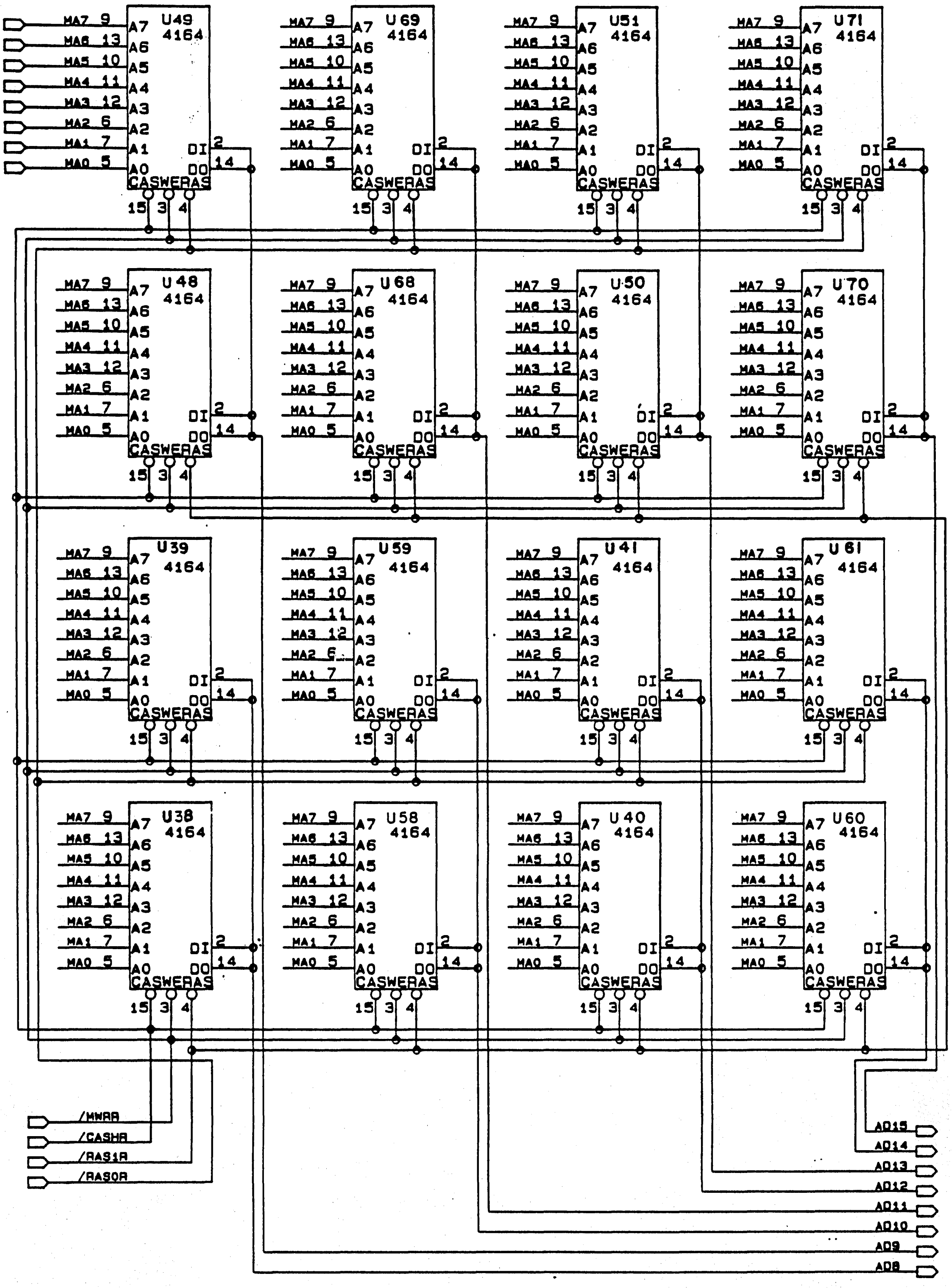
16 BIT CPU

OTRONA ADV SYS

RAM LOW

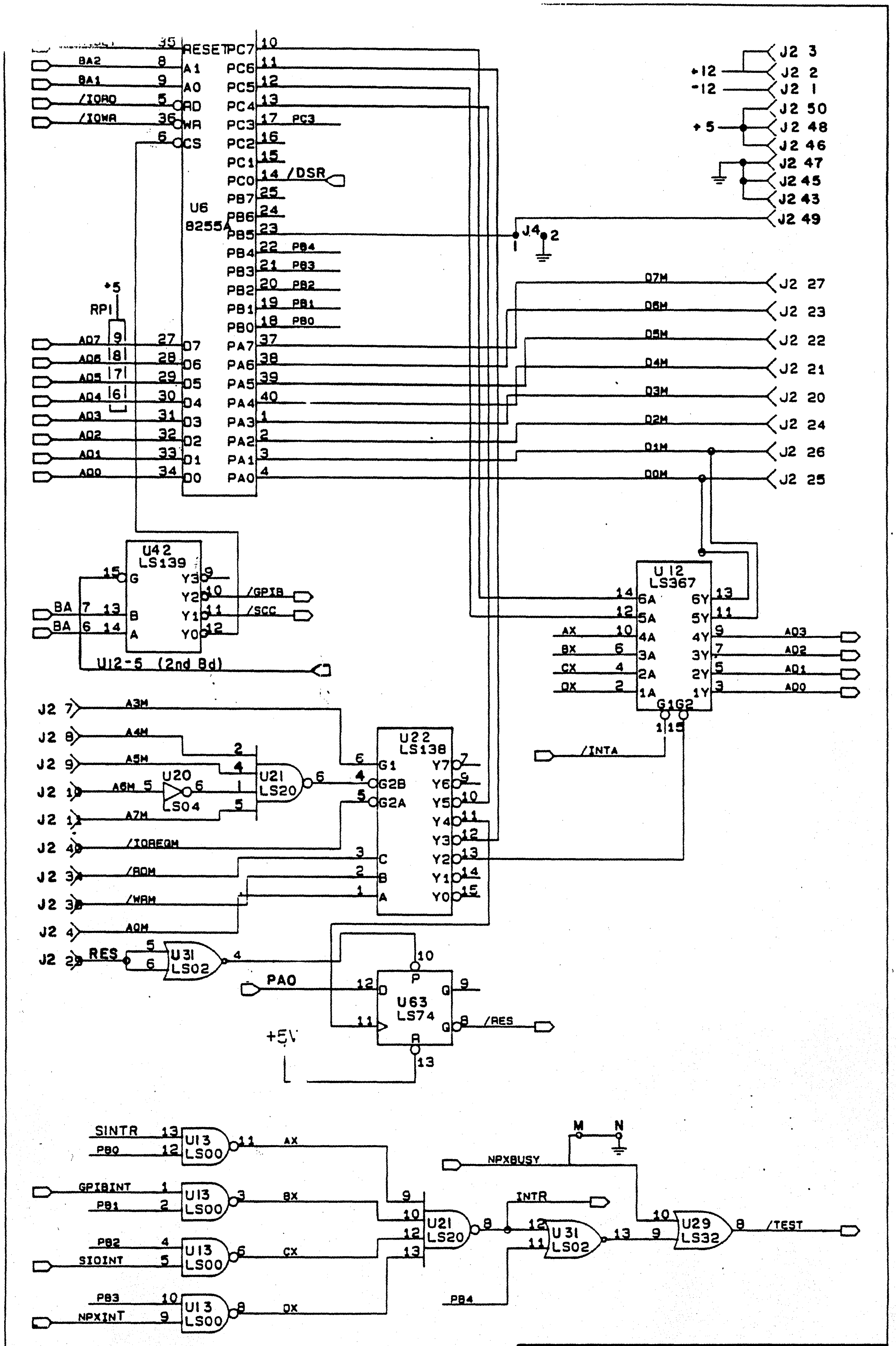
4 OF 8

A4



41-051209	Rev. B
RAM HIGH DATA	
16 BIT CPU	OTRONA ADV SYS
RAM HIGH	5 OF 8

A5



41-051209 Rev B

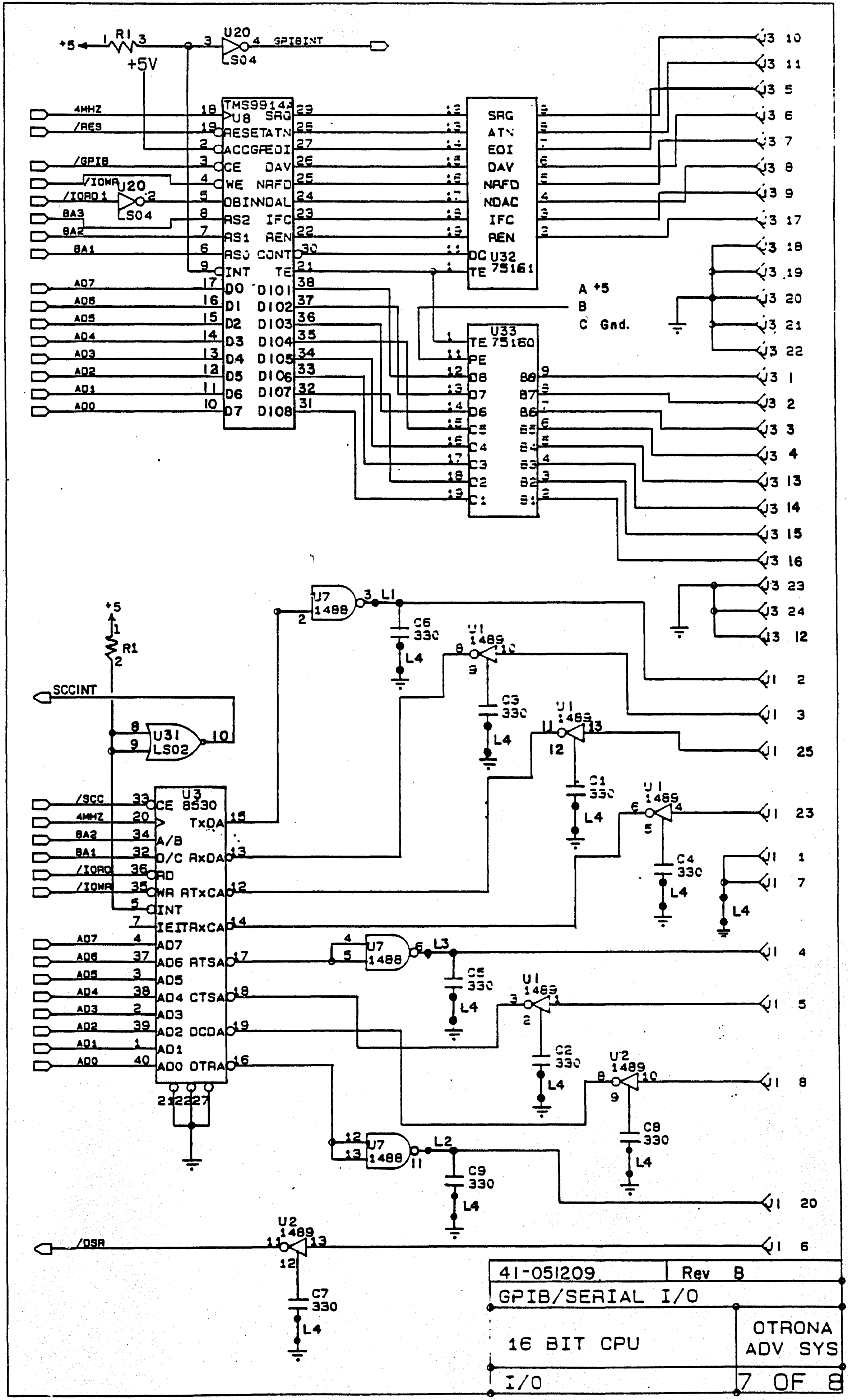
ATTACHE INTERFACE

16 BIT CPU

OTRONA ADV SYS

INTERFACE

6 OF 8



41-051209 Rev B

GPIB/SERIAL I/O

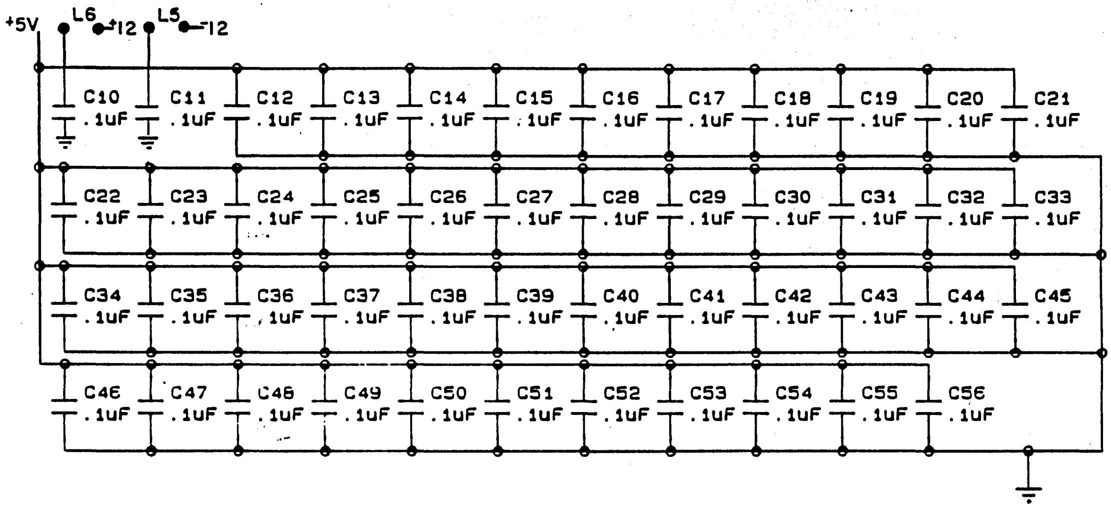
16 BIT CPU

OTRONA ADV SYS

I/O

7 OF 8

A7



41-051209 Rev B

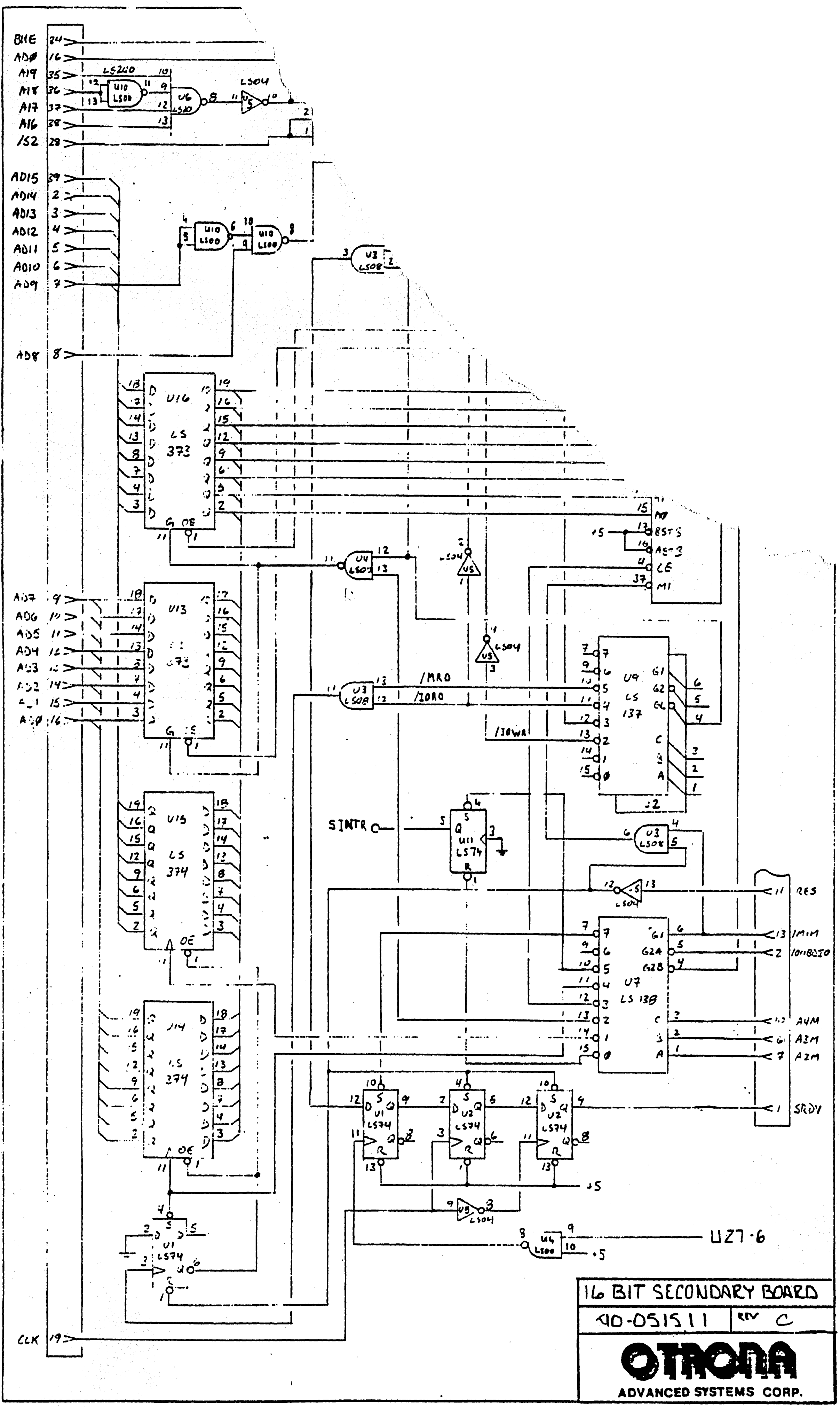
BY-PASS CAPS

16 BIT CPU

OTRONA
ADV SYS

BY-PASS

8 OF 8



16 BIT SECONDARY BOARD

40-051511 REV C

OTRONA
ADVANCED SYSTEMS CORP.

A9