FAIRCHILD® F100K ECL COMPONENTS LIBRARY

Schematic Symbols

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OVERVIEW

The PCAD/Fairchild® 100K ECL Schematic Symbols Library consists of this manual and two Fairchild 100K ECL Schematic Symbol diskettes. The library has been developed jointly with Fairchild at the request of our users, and we welcome any suggestions for improvements or additions.

The library diskettes contain the following files for use with the PC-CAPS schematic capture program:

- Component files
- Layer structure file LAYS.SCH
- Standard-size drawing sheet files, ASIZE.SCH through ESIZE.SCH
- F100K.FIL and F100K.LIB files

  F100K.FIL is a sample text file used as input into PREPACK to create the binary file F100K.LIB that contains packaging information for PC-PACK. Both F100K.FIL and F100K.LIB contain all the components in the Fairchild 100K ECL Library. Normal usage is to extract only those components used in a design and put them in a new .FIL file for input to PREPACK.

Storage of these files in a practical and efficient directory structure is discussed in the next section of this manual. The following section, "Creating a Design", tells you how to use the files with PC-CAPS.

The remainder of the manual is devoted to lists of components by sequence and function, component pin sequences, and component plots.

FILE MANAGEMENT

The complete Fairchild 100K ECL Symbols Library includes more than 500 KB of files. If you are loading the library onto the hard disk of your stand-alone computer, you should omit any of the components that you will not need in order to conserve disk space. This is especially important if you are using a 10 MB hard disk. If your hard disk space is very limited, you can remove individual unneeded components from the library. Each component is contained in a separate DOS file, and individual components can be erased using the DOS erase command. Refer to your IBM DOS manual or the "DOS Reference" chapter in your *PC-CAPS or PC-CARDS User's Manuals* for instructions on listing and erasing files.

P-CAD recommends a specific directory structure for efficient system operation. Your library symbols are normally placed in a specific subdirectory to make it easy to manage these files. The directory structure is described in your P-CAD *Installation Guide.*

CREATING A DESIGN

To use the library in a design, run PC-CAPS. Instructions are given in the "Using PC-CAPS" chapter of your *PC-CAPS User's Manual.* When the menu appears, select FILE/LOAD and load the layer structure. You can load LAYS.SCH or one of the standard-size drawing sheet files, ASIZE.SCH through ESIZE.SCH.

Layer Structure

One layer structure file, LAYS.SCH, is included with this library.

LAYS.SCH, shown in Table 1, is a standard P-CAD layer structure and is recommended when creating schematics.

Drawing Sheets

The standard-size drawing sheet files, ASIZE.SCH through ESIZE.SCH, were created using the LAYS.SCH layer structure. When loaded, they provide the correct layer structure for the library plus a standard-size drawing sheet border.

Components

When you have loaded your layer structure or drawing sheet file, you can enter the symbols, wires, text, instances, and net names. Complete instructions are given in the "Using PC-CAPS" chapter of your *PC-CAPS User's Manual.*

Table 1. LAYS.SCH Layer Structure

Layer	Name	Pen	Status	Use
1	WIRES	1	ABL (A)	Interconnecting wires
2	BUS	2	ABL	Interconnecting buses/wires
3	GATE	3	ON	Symbol graphics (ANSII)
4	IEEE	3	OFF	Symbol graphics (IEEE)
5	PINFUN	3	OFF	Pin functions (IEEE)
6	PINNUM	4	ON	Pin numbers
7	PINNAM	3	ON	Pin names
8	PINCON	4	ON	Pin connections
9	REFDES	5	ON	Reference designators
10	ATTR	6	OFF	Visible attributes
11	SDOT	1	ON	Solder dots (not used)
12	DEVICE	6	ON	Device name
13	OUTLIN	6	OFF	Component outline
14	ATTR2	7	OFF	Invisible attributes
15	NOTES	7	OFF	Notes/text/documentation
16	NETNAM	8	ABL	Net/signal names (schematic)
17	CMPNAM	8	OFF	Component instance names
18	BORDER	9	OFF	Drawing/schematic border

GENERAL INFORMATION

This library was created using the *Fairchild F100K ECL Data Book* and Fairchild's F100K ECL August 1986 Preliminary Data Sheet. IEEE representations of all the devices are included.

Two categories of symbols are included in this library; the symbol numbers ending in D have pin numbers appropriate for the DIP package, the symbol numbers ending in F are for use with the Cerpak (flatpack) package.

NAMING CONVENTIONS

In this library, all signal names are drawn exactly as shown in the *Fairchild F100K ECL Data Book* and the Preliminary Data Sheets. The actual signal names for the symbols are given in the Component Pin Sequences section of this manual.

COMPONENT LIST BY SEQUENCE

The component filename consists of the symbol number plus the extension .SYM; for example, 100142D.SYM. "Plot Number" refers to the plots in the last section of this manual.

Symbol Number	Disk Number	Plot Number (ANSI/IEEE)
100101D	1	1/1A
100102D	1	1/1A
100104D	1	1/1A
100107D	1	1/1A
100112D	1	1/1A
100113D	1	1/1A
100114D	1	1/1A
100117D	1	2/2A
100118D	1	2/2A
100121D	1	2/2A
100122D	1	2/2A
100123D	1	3/3A
100124D	1	3/3A
100125D	1	3/3A
100126D	1	3/3A
100128D	1	4/4A
100130D	1	4/4A
100131D	1	4/4A
100135D	1	4/4A
100136D	1	4/4A
100139D	1	4/4A
100140D	1	4/4A
100141D	1	5/5A
100142D	1	5/5A
100145D	1	5/5A
100150D	1	5/5A
100151D	1	5/5A

Symbol Number	Disk Number	Plot Number (ANSI/IEEE)
100155D	1	5/5A
100156D	1	6/6A
100158D	1	6/6A
100160D	1	6/6A
100163D	1	6/6A
100164D	1	6/6A
100165D	1	6/6A
100166D	1	6/6A
100170D	1	6/6A
100171D	1	7/7A
100175D	1	7/7A
100179D	1	7/7A
100180D	1	7/7A
100181D	1	7/7A
100182D	1	7/7A
100183D	1	7/7A
100241D	1	7/7A
100413D	1	7/7A
E100142D	1	5A
E100165D	1	6A
100101F	2	8/8A
100102F	2	8/8A
100104F	2	8/8A
100107F	2	8/8A
100112F	2	8/8A
100113F	2	8/8A
100114F	2	8/8A
100117F	2	9/9A
100118F	2	9/9A
100121F	2	9/9A
100122F	2	9/9A
100123F	2	10/10A
100124F	2	10/10A
100125F	2	10/10A
100126F	2	10/10A

Symbol Number	Disk Number	Plot Number (ANSI/IEEE)
100128F	2	11/11A
100130F	2	11/11A
100131F	2	11/11A
100135F	2	11/11A
100136F	2	11/11A
100139F	2	11/11A
100140F	2	11/11A
100141F	2	12/12A
100142F	2	12/12A
100145F	2	12/12A
100150F	2	12/12A
100151F	2	12/12A
100155F	2	12/12A
100156F	2	13/13A
100158F	2	13/13A
100160F	2	13/13A
100163F	2	13/13A
100164F	2	13/13A
100165F	2	13/13A
100166F	2	13/13A
100170F	2	13/13A
100171F	2	14/14A
100179F	2	14/14A
100180F	2	14/14A
100181F	2	14/14A
100182F	2	14/14A
100183F	2	14/14A
100241F	2	14/14A
100413F	2	14/14A
E100142F	2	12A
E100165F	2	13A

COMPONENT LIST BY FUNCTION

The components described below come in both DIP and flatpak-type packaging, except component 100175 which comes only in a DIP. To distinguish between the two types, DIP schematic symbols have a "D" suffix while the flatpak schematic symbols have an "F" suffix after the component's name. For instance, the 100101 component will have a file named 100101D.SYM for DIP packaging and one named 100101F.SYM for flatpak packaging.

AND/NAND Gates

100104	Quint 2-input

Arithmetic Operators

100156	4-bit mask-merge/latch
100158	8-bit shift matrix
100160	Dual 9-bit parity checker/generator
100165	8-input priority encoder
100166	9-bit comparator
100179	Carry lookahead
100180	High speed 6-bit adder
100181	4-bit binary/BCD ALU
100182	9-bit Wallace tree adder
100183	2x8 decode multiplier

Buffers

100121	9-bit inverter
100122	9-bit buffer
100126	9-bit backplane driver
100413	16x8 FIFO memory buffer

Content Addressable Memory

100142	4x4-bit content addressable memory

Counters/Prescalers

100136	4-bit binary (count up/down)
100139	4-bit binary (async reset)
100140	4-bit decade (count down)

Demultiplexer/Decoders

100170	Universal (dual 1 of 4/single 1 of 8)

Exclusive OR/NOR Gates

100107	Quint EXCLUSIVE OR/NOR

Flip-Flops

100131	Triple D (async set/reset)
100135	Triple J-K (async set)
100151	Hex D (async reset)

Latches

100130	Triple D (async set/reset)
100150	Hex D (async reset)
100155	Quad 2-input MUX/latch (async reset)
100175	Quint latch 100K in/10K out

Line Bus Drivers/Transceivers/Receivers

100112	Quad line driver
100113	Quad line driver
100114	Quint differential line receiver
100123	Hex bus driver

Multiplexers

100155	Quad 2-input MUX/latch (async reset)
100163	Dual 8-input MUX
100164	16-input MUX
100171	Triple 4-input MUX (W/enable)

OR-AND/OR-AND-INVERT Gates

100117	Triple 2-wide OA/OAI
100118	5-wide 5,4,4,4,2-input OA/OAI

OR/NOR Gates

100101	Triple 5-input
100102	Quint 2-input

RAMS

100145	16x4-bit register file

Shift Registers

100136	4-bit bidirectional
100141	8-bit bidirectional
100241	8-bit bidirectional

Translators

100124	Hex TTL-100K ECL
100125	Hex 100K ECL-TTL
100128	Octal ECL/TTL bidirectional

COMPONENT PIN SEQUENCES

DIP Pin Sequence List

100101D: Number of gates per package = 3

Pin	Signal	Pin	Signal	Pin	Signal
1	D3 (C)	9	O' (B)	17	D1 (B)
2	D4 (C)	10	O' (A)	18	VEE
3	D5 (C)	11	O (A)	19	D2 (B)
4	O (C)	12	D1 (A)	20	D3 (B)
5	O' (C)	13	D2 (A)	21	D4 (B)
6	VCC	14	D3 (A)	22	D5 (B)
7	VCCA	15	D4 (A)	23	D1 (C)
8	O (B)	16	D5 (A)	24	D2 (C)

100102D: Number of gates per package = 5

Pin	Signal	Pin	Signal	Pin	Signal
1	D2 (E)	9	O (C)	17	D2 (B)
2	O (E)	10	O (B)	18	VEE
3	O' (E)	11	O' (B)	19	E
4	O' (D)	12	O' (A)	20	D1 (C)
5	O (D)	13	O (A)	21	D2 (C)
6	VCC	14	D1 (A)	22	D1 (D)
7	VCCA	15	D2 (A)	23	D2 (D)
8	O' (C)	16	D1	24	D1 (E)

100104D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1 =	OE	9 =	OC	17 =	D2B
2 =	OE'	10 =	OB'	18 =	VEE
3 =	OD	11 =	OB	19 =	D1C
4 =	OD'	12 =	OA'	20 =	D2C
5 =	F	13 =	OA	21 =	D2D
6 =	VCC	14 =	D1A	22 =	D1D
7 =	VCCA	15 =	D2A	23 =	D1E
8 =	OC'	16 =	D1B	24 =	D2E

100107D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1 =	OE	9 =	OC	17 =	D2B
2 =	OE'	10 =	OB'	18 =	VEE
3 =	OD	11 =	OB	19 =	D1C
4 =	OD'	12 =	OA'	20 =	D2C
5 =	F	13 =	OA	21 =	D2D
6 =	VCC	14 =	D1A	22 =	D1D
7 =	VCCA	15 =	D2A	23 =	D1E
8 =	OC'	16 =	D1B	24 =	D2E

100112D: Number of gates per package = 4

Pin	Signal	Pin	Signal	Pin	Signal
1 =	O2' (D)	9 =	O2 (B)	17 =	D (B)
2 =	O2' (C)	10 =	O1' (B)	18 =	VEE
3 =	O1' (C)	11 =	O2' (B)	19 =	E
4 =	O2 (C)	12 =	O2' (A)	20 =	D (C)
5 =	O1 (C)	13 =	O1' (A)	21 =	D (D)
6 =	VCC	14 =	O2 (A)	22 =	O1 (D)
7 =	VCCA	15 =	O1 (A)	23 =	O2 (D)
8 =	O1 (B)	16 =	D (A)	24 =	O1' (D)

100113D: Number of gates per package = 4

Pin	Signal	Pin	Signal	Pin	Signal
1	O2' (D)	9	O2 (B)	17	D (B)
2	O2' (C)	10	O1' (B)	18	VEE
3	O1' (C)	11	O2' (B)	19	E
4	O2 (C)	12	O2' (A)	20	D (C)
5	O1 (C)	13	O1' (A)	21	D (D)
6	VCC	14	O2 (A)	22	O1 (D)
7	VCCA	15	O1 (A)	23	O2 (D)
8	O1 (B)	16	D (A)	24	O1' (D)

100114D: Number of gates per package = 5

Pin	Signal	Pin	Signal	Pin	Signal
1	D' (E)	9	O (C)	17	D' (B)
2	O' (E)	10	O' (B)	18	VEE
3	O (E)	11	O (B)	19	VBB
4	O' (D)	12	O' (A)	20	D (C)
5	O (D)	13	O (A)	21	D' (C)
6	VCC	14	D (A)	22	D (D)
7	VCCA	15	D' (A)	23	D' (D)
8	O' (C)	16	D (B)	24	D (E)

100117D: Number of gates per package = 3

Pin	Signal	Pin	Signal	Pin	Signal
1	D2 (C)	9	O' (B)	17	E (B)
2	D3 (C)	10	O' (A)	18	VEE
3	D4 (C)	11	O (A)	19	E (C)
4	O (C)	12	D1 (A)	20	D1 (B)
5	O' (C)	13	D2 (A)	21	D2 (B)
6	VCC	14	D3 (A)	22	D3 (B)
7	VCCA	15	D4 (A)	23	D4 (B)
8	O (B)	16	E (A)	24	D1 (C)

100118D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1 =	D2D	9 =	O	17 =	D3B
2 =	D3D	10 =	D1A	18 =	VEE
3 =	D4D	11 =	D2A	19 =	D4B
4 =	D1E	12 =	D3A	20 =	D1C
5 =	D2E	13 =	D4A	21 =	D2C
6 =	VCC	14 =	D5A	22 =	D3C
7 =	VCCA	15 =	D1B	23 =	D4C
8 =	O'	16 =	D2B	24 =	D1D

100121D: Number of gates per package = 9

Pin	Signal	Pin	Signal	Pin	Signal
1 =	VCCA	9 =	O' (G)	17 =	D (G)
2 =	O' (C)	10 =	O' (F)	18 =	VEE
3 =	O' (B)	11 =	O' (E)	19 =	VCCA
4 =	O' (A)	12 =	O' (D)	20 =	D (H)
5 =	O' (I)	13 =	VCCA	21 =	D (I)
6 =	VCC	14 =	D (D)	22 =	D (A)
7 =	VCCA	15 =	D (E)	23 =	D (B)
8 =	O' (H)	16 =	D (F)	24 =	D (C)

100122D: Number of gates per package = 9

Pin	Signal	Pin	Signal	Pin	Signal
1 =	VCCA	9 =	O (G)	17 =	D (G)
2 =	O (C)	10 =	O (F)	18 =	VEE
3 =	O (B)	11 =	O (E)	19 =	VCCA
4 =	O (A)	12 =	O (D)	20 =	D (H)
5 =	O (I)	13 =	VCCA	21 =	D (I)
6 =	VCC	14 =	D (D)	22 =	D (A)
7 =	VCCA	15 =	D (E)	23 =	D (B)
8 =	O (H)	16 =	D (F)	24 =	D (C)

100123D: Number of gates per package = 3

Pin	Signal	Pin	Signal	Pin	Signal
1	VCCA2 (C)	9	VCCA2 (A)	17	DE (B)
2	OA (C)	10	OB (A)	18	VEE
3	VCCA1 (C)	11	VCCA1 (B)	19	E
4	OB (B)	12	OA (B)	20	DE (C)
5	VCCA2 (B)	13	DA (B)	21	DB (C)
6	VCC	14	DB (A)	22	DA (C)
7	VCCA1 (A)	15	DA (A)	23	DB (B)
8	OA (A)	16	DE (A)	24	OB (C)

100124D: Number of gates per package = 6

Pin	Signal	Pin	Signal	Pin	Signal
1	O' (A)	9	O (D)	17	D (D)
2	O (B)	10	O' (D)	18	VEE
3	O' (B)	11	O' (E)	19	E
4	O' (C)	12	O (E)	20	VTTL
5	O (C)	13	O' (F)	21	D (A)
6	VCC	14	O (F)	22	D (B)
7	VCCA	15	D (F)	23	D (C)
8	VCCA	16	D (E)	24	O (A)

100125D: Number of gates per package = 6

Pin	Signal	Pin	Signal	Pin	Signal
1	O (F)	9	O (B)	17	VBB
2	O (E)	10	O (A)	18	VEE
3	O (D)	11	D' (A)	19	D (D)
4	VTTL	12	D (A)	20	D' (D)
5	VTTL	13	D' (B)	21	D (E)
6	VCC	14	D (B)	22	D' (E)
7	VCC	15	D' (C)	23	D (F)
8	O (C)	16	D (C)	24	D' (F)

100126D: Number of gates per package = 9

Pin	Signal	Pin	Signal	Pin	Signal
1	VCCA	9	O (G)	17	D (G)
2	O (C)	10	O (F)	18	VEE
3	O (B)	11	O (E)	19	VCCA
4	O (A)	12	O (D)	20	D (H)
5	O (I)	13	VCCA	21	D (I)
6	VCC	14	D (D)	22	D (A)
7	VCCA	15	D (E)	23	D (B)
8	O (H)	16	D (F)	24	D (C)

100128D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	E4	9	T7	17	LE
2	E5	10	T6	18	VEE
3	E6	11	T5	19	VCC
4	E7	12	T4	20	VTTL
5	OE	13	T3	21	E0
6	VCC	14	T2	22	E1
7	VCCA	15	T1	23	E2
8	DIR	16	T0	24	E3

100130D: Number of gates per package = 3

Pin	Signal	Pin	Signal	Pin	Signal
1	CD (C)	9	Q' (B)	17	EC'
2	E' (C)	10	Q' (A)	18	VEE
3	D (C)	11	Q (A)	19	MR
4	Q (C)	12	D (A)	20	SD (B)
5	Q' (C)	13	E' (A)	21	D (B)
6	VCC	14	CD (A)	22	E' (B)
7	VCCA	15	SD (A)	23	CD (B)
8	Q (B)	16	MS	24	SD (C)

100131D: Number of gates per package = 3

Pin	Signal	Pin	Signal	Pin	Signal
1	CD (C)	9	Q' (B)	17	CPC
2	CP (C)	10	Q' (A)	18	VEE
3	D (C)	11	Q (A)	19	MR
4	Q (C)	12	D (A)	20	SD (B)
5	Q' (C)	13	CP (A)	21	D (B)
6	VCC	14	CD (A)	22	CP (B)
7	VCCA	15	SD (A)	23	CD (B)
8	Q (B)	16	MS	24	SD (C)

100135D: Number of gates per package = 3

Pin	Signal	Pin	Signal	Pin	Signal
1	S (C)	9	Q (B)	17	S (B)
2	J (C)	10	Q' (A)	18	VEE
3	K (C)	11	Q (A)	19	K (B)
4	Q' (C)	12	S (A)	20	J (B)
5	Q (C)	13	C (A)	21	CP (B)
6	VCC	14	CP (A)	22	C (B)
7	VCCA	15	J (A)	23	CP (C)
8	Q' (B)	16	K (A)	24	C (C)

100136D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	TC'	9	Q2'	17	CP
2	Q0	10	Q3'	18	VEE
3	Q0'	11	Q3	19	MR
4	Q1'	12	D3	20	S0
5	Q1	13	P3	21	S1
6	VCC	14	P2	22	S2
7	VCCA	15	P1	23	CEP'
8	Q2	16	P0	24	D0/CET

100139D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1 =	P0	9 =	PE1	17 =	CP
2 =	Q0'	10 =	TC15'	18 =	VEE
3 =	Q0	11 =	TC14	19 =	CEP
4 =	Q1'	12 =	Q2'	20 =	MR
5 =	Q1	13 =	Q2	21 =	CET
6 =	VCC	14 =	Q3'	22 =	P3
7 =	VCCA	15 =	Q3	23 =	P2
8 =	TC14'	16 =	PE2	24 =	P1

100140D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1 =	P0	9 =	PE1	17 =	CP
2 =	Q0'	10 =	TC0'	18 =	VEE
3 =	Q0	11 =	TC1	19 =	CEP
4 =	Q1'	12 =	Q2'	20 =	MR
5 =	Q1	13 =	Q2	21 =	CET
6 =	VCC	14 =	Q3'	22 =	P3
7 =	VCCA	15 =	Q3	23 =	P2
8 =	TC1'	16 =	PE2	24 =	P1

100141D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1 =	D0	9 =	Q5	17 =	CP
2 =	Q0	10 =	Q6	18 =	VEE
3 =	Q1	11 =	Q7	19 =	S0
4 =	Q2	12 =	D7	20 =	S1
5 =	Q3	13 =	P7	21 =	P3
6 =	VCC	14 =	P6	22 =	P2
7 =	VCCA	15 =	P5	23 =	P1
8 =	Q4	16 =	P4	24 =	P0

100142D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	MK3	9	Q2	17	A2
2	M0	10	Q1	18	VEE
3	M1	11	Q0	19	WS
4	M2	12	MK1	20	A1
5	M3	13	D1	21	A0
6	VCC	14	MK0	22	D2
7	VCCA	15	D0	23	MK2
8	Q3	16	A3	24	D3

100145D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	AR2	9	Q3	17	WE2
2	AR1	10	D3	18	VEE
3	AR0	11	D2	19	MR
4	Q0	12	D1	20	AW0
5	Q1	13	D0	21	AW1
6	VCC	14	OE1	22	AW2
7	VCCA	15	OE2	23	AW3
8	Q2	16	WE1	24	AR3

100150D: Number of gates per package = 6

Pin	Signal	Pin	Signal	Pin	Signal
1	Q' (F)	9	Q (C)	17	D (D)
2	Q' (E)	10	Q' (B)	18	VEE
3	Q (E)	11	Q (B)	19	MR
4	Q' (D)	12	Q' (A)	20	EA'
5	Q (D)	13	Q (A)	21	EB'
6	VCC	14	D (A)	22	D (E)
7	VCCA	15	D (B)	23	D (F)
8	Q' (C)	16	D (C)	24	Q (F)

100151D: Number of gates per package = 6

Pin	Signal	Pin	Signal	Pin	Signal
1	Q' (F)	9	Q (C)	17	D (D)
2	Q' (E)	10	Q' (B)	18	VEE
3	Q (E)	11	Q (B)	19	MR
4	Q' (D)	12	Q' (A)	20	CPA
5	Q (D)	13	Q (A)	21	CPB
6	VCC	14	D (A)	22	D (E)
7	VCCA	15	D (B)	23	D (F)
8	Q' (C)	16	D (C)	24	Q (F)

100155D: Number of gates per package = 4

Pin	Signal	Pin	Signal	Pin	Signal
1	D1 (D)	9	Q (B)	17	S1
2	Q (D)	10	Q (A)	18	VEE
3	Q' (D)	11	Q' (A)	19	MR
4	Q' (C)	12	D0 (A)	20	E1'
5	Q (C)	13	D1 (A)	21	E2'
6	VCC	14	D0 (B)	22	D0 (C)
7	VCCA	15	D1 (B)	23	D1 (C)
8	Q' (B)	16	S0'	24	D0 (D)

100156D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	AM1	9	Q0	17	E'
2	A3	10	B0	18	VEE
3	B3	11	A0	19	AS0
4	Q3	12	B1	20	BS1
5	Q2	13	A1	21	AS1
6	VCC	14	B2	22	BM0
7	VCCA	15	A2	23	AM0
8	Q1	16	BS0	24	BM1

100158D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	Z7	9	Z2	17	S1
2	Z6	10	Z1	18	VEE
3	Z5	11	Z0	19	M
4	Z4	12	D0	20	S2
5	VCCA	13	D1	21	D4
6	VCC	14	D2	22	D5
7	VCCA	15	D3	23	D6
8	Z3	16	S0	24	D7

100160D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	I6B	9	IA	17	I7A
2	I7B	10	I0A	18	VEE
3	IB	11	I1A	19	I0B
4	ZB	12	I2A	20	I1B
5	C'	13	I3A	21	I2B
6	VCC	14	I4A	22	I3B
7	VCCA	15	I5A	23	I4B
8	ZA	16	I6A	24	I5B

100163D: Number of gates per package = 2

Pin	Signal	Pin	Signal	Pin	Signal
1	D3 (B)	9	D0 (A)	17	S0
2	D2 (B)	10	D1 (A)	18	VEE
3	D1 (B)	11	D2 (A)	19	S1
4	D0 (B)	12	D3 (A)	20	S2
5	Z (B)	13	D4 (A)	21	D7 (B)
6	VCC	14	D5 (A)	22	D6 (B)
7	VCCA	15	D6 (A)	23	D5 (B)
8	Z (A)	16	D7 (A)	24	D4 (B)

100164D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1 =	I3	9 =	I8	17 =	S0
2 =	I4	10 =	I9	18 =	VEE
3 =	I5	11 =	I10	19 =	S1
4 =	I6	12 =	I11	20 =	S2
5 =	I7	13 =	I12	21 =	S3
6 =	VCC	14 =	I13	22 =	I0
7 =	VCCA	15 =	I14	23 =	I1
8 =	Z	16 =	I15	24 =	I2

100165D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1 =	Q0	9 =	Q2	17 =	OE'
2 =	Q0'	10 =	Q2'	18 =	VEE
3 =	Q1'	11 =	Q3'	19 =	E'
4 =	Q1	12 =	Q3	20 =	M
5 =	GS1	13 =	I7	21 =	I3
6 =	VCC	14 =	I6	22 =	I2
7 =	VCCA	15 =	I5	23 =	I1
8 =	GS2	16 =	I4	24 =	I0

100166D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1 =	B2	9 =	A0	17 =	A8
2 =	B1	10 =	A1	18 =	VEE
3 =	B0	11 =	A2	19 =	B8
4 =	A<B	12 =	A3	20 =	B7
5 =	A=B	13 =	A4	21 =	B6
6 =	VCC	14 =	A5	22 =	B5
7 =	VCCA	15 =	A6	23 =	B4
8 =	A>B	16 =	A7	24 =	B3

100170D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	A1B	9	Z0	17	EB1
2	Z7	10	Z2	18	VEE
3	Z4	11	Z1	19	EB2
4	Z6	12	A0A	20	EA2
5	Z5	13	A1A	21	HA
6	VCC	14	M	22	HC
7	VCCA	15	A2A	23	HB
8	Z3	16	EA1	24	A0B

100171D: Number of gates per package = 3

Pin	Signal	Pin	Signal	Pin	Signal
1	I1 (C)	9	Z' (B)	17	S1
2	I2 (C)	10	Z' (A)	18	VEE
3	I3 (C)	11	Z (A)	19	E'
4	Z (C)	12	I0 (A)	20	I0 (B)
5	Z' (C)	13	I1 (A)	21	I1 (B)
6	VCC	14	I2 (A)	22	I2 (B)
7	VCCA	15	I3 (A)	23	I3 (B)
8	Z (B)	16	S0	24	I0 (C)

100175D: Number of gates per package = 5

Pin	Signal	Pin	Signal	Pin	Signal
1	VCCA	7	E2	12	D (E)
2	Q (A)	8	VEE	13	D (A)
3	Q (B)	9	D (B)	14	Q (D)
4	Q (C)	10	D (D)	15	Q (E)
5	D (C)	11	MR	16	VCC
6	E1				

100179D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	P1	9	CN+8	17	P6
2	G2	10	G3	18	VEE
3	P2	11	P3	19	CN
4	CN+2	12	G4	20	G7
5	CN+4	13	P4	21	P7
6	VCC	14	G5	22	G0
7	VCCA	15	P5	23	P0
8	CN+6	16	G6	24	G1

100180D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	A0	9	F5	17	A3
2	F0	10	P	18	VEE
3	F1	11	G	19	CN
4	F2	12	B5	20	B2
5	F3	13	A5	21	A2
6	VCC	14	B4	22	B1
7	VCCA	15	A4	23	A1
8	F4	16	B3	24	B0

100181D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	A0	9	P	17	S1
2	F0	10	G	18	VEE
3	F1	11	CN	19	E
4	F2	12	B0	20	S2
5	F3	13	B1	21	S3
6	VCC	14	B2	22	A3
7	VCCA	15	B3	23	A2
8	CN+4	16	S0	24	A1

100182D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	D1	9	PC	17	D6
2	D0	10	PS	18	VEE
3	CON+2	11	CI3	19	D5
4	CO3	12	CI2	20	{n/c}
5	CO1	13	CI1	21	{n/c}
6	VCC	14	CIN-2	22	D4
7	VCCA	15	D8	23	D3
8	CO2	16	D7	24	D2

100183D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	B0	9	F5	17	B4
2	F0	10	F6	18	VEE
3	F1	11	F7	19	A2
4	F2	12	F8'	20	A1
5	F3	13	B8	21	A0
6	VCC	14	B7	22	B3
7	VCCA	15	B6	23	B2
8	F4	16	B5	24	B1

100241D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	D0	9	Q5	17	CP
2	Q0	10	Q6	18	VEE
3	Q1	11	Q7	19	S0
4	Q2	12	D7	20	S1
5	Q3	13	P7	21	P3
6	VCC	14	P6	22	P2
7	VCCA	15	P5	23	P1
8	Q4	16	P4	24	P0

100413D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	Q0	9	Q4	17	IR
2	Q1	10	Q5	18	VEE
3	Q2	11	Q6	19	MR
4	Q3	12	Q7	20	TI
5	OR	13	D7	21	D3
6	VCC	14	D6	22	D2
7	VCCA	15	D5	23	D1
8	TO	16	D4	24	D0

E100142D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	MK3	9	Q2	17	A2
2	M0	10	Q1	18	VEE
3	M1	11	Q0	19	WS
4	M2	12	MK1	20	A1
5	M3	13	D1	21	A0
6	VCC	14	MK0	22	D2
7	VCCA	15	D0	23	MK2
8	Q3	16	A3	24	D3

E100165D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	Q0	9	Q2	17	I6
2	Q0'	10	Q2'	18	VEE
3	Q1'	11	Q3'	19	I5
4	Q1	12	Q3	20	I7
5	GS1	13	M	21	I1
6	VCC	14	OE'	22	I2
7	VCCA	15	E'	23	I3
8	GS2	16	I0	24	I4

Flatpak Pin Sequence List

100101F: Number of gates per package = 3

Pin	Signal	Pin	Signal	Pin	Signal
1	D5 (B)	9	VCC	17	D3 (A)
2	D1 (C)	10	VCCA	18	D4 (A)
3	D2 (C)	11	O (B)	19	D5 (A)
4	D3 (C)	12	O' (B)	20	D1 (B)
5	D4 (C)	13	O' (A)	21	VEE
6	D5 (C)	14	O (A)	22	D2 (B)
7	O (C)	15	D1 (A)	23	D3 (B)
8	O' (C)	16	D2 (A)	24	D4 (B)

100102F: Number of gates per package = 5

Pin	Signal	Pin	Signal	Pin	Signal
1	D1 (D)	9	VCC	17	D1 (A)
2	D2 (D)	10	VCCA	18	D2 (A)
3	D1 (E)	11	O' (C)	19	D1 (B)
4	D2 (E)	12	O (C)	20	D2 (B)
5	O (E)	13	O (B)	21	VEE
6	O' (E)	14	O' (B)	22	E
7	O' (D)	15	O' (A)	23	D1 (C)
8	O (D)	16	O (A)	24	D2 (C)

100104F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1 =	D1D	9 =	VCC	17 =	D1A
2 =	D1E	10 =	VCCA	18 =	D2A
3 =	D2E	11 =	OC'	19 =	D1B
4 =	OE	12 =	OC	20 =	D2B
5 =	OE'	13 =	OB'	21 =	VEE
6 =	OD	14 =	OB	22 =	D1C
7 =	OD'	15 =	OA'	23 =	D2C
8 =	F	16 =	OA	24 =	D2D

100107F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1 =	D1D	9 =	VCC	17 =	D1A
2 =	D1E	10 =	VCCA	18 =	D2A
3 =	D2E	11 =	OC'	19 =	D1B
4 =	OE	12 =	OC	20 =	D2B
5 =	OE'	13 =	OB'	21 =	VEE
6 =	OD	14 =	OB	22 =	D1C
7 =	OD'	15 =	OA'	23 =	D2C
8 =	F	16 =	OA	24 =	D2D

100112F: Number of gates per package = 4

Pin	Signal	Pin	Signal	Pin	Signal
1 =	O1 (D)	9 =	VCC	17 =	O2 (A)
2 =	O2 (D)	10 =	VCCA	18 =	O1 (A)
3 =	O1' (D)	11 =	O1 (B)	19 =	D (A)
4 =	O2' (D)	12 =	O2 (B)	20 =	D (B)
5 =	O2' (C)	13 =	O1' (B)	21 =	VEE
6 =	O1' (C)	14 =	O2' (B)	22 =	E
7 =	O2 (C)	15 =	O2' (A)	23 =	D (C)
8 =	O1 (C)	16 =	O1' (A)	24 =	D (D)

100113F: Number of gates per package = 4

Pin	Signal	Pin	Signal	Pin	Signal
1	O1 (D)	9	VCC	17	O2 (A)
2	O2 (D)	10	VCCA	18	O1 (A)
3	O1' (D)	11	O1 (B)	19	D (A)
4	O2' (D)	12	O2 (B)	20	D (B)
5	O2' (C)	13	O1' (B)	21	VEE
6	O1' (C)	14	O2' (B)	22	E
7	O2 (C)	15	O2' (A)	23	D (C)
8	O1 (C)	16	O1' (A)	24	D (D)

100114F: Number of gates per package = 5

Pin	Signal	Pin	Signal	Pin	Signal
1	D (D)	9	VCC	17	D (A)
2	D' (D)	10	VCCA	18	D' (A)
3	D (E)	11	O' (C)	19	D (B)
4	D' (E)	12	O (C)	20	D' (B)
5	O' (E)	13	O' (B)	21	VEE
6	O (E)	14	O (B)	22	VBB
7	O' (D)	15	O' (A)	23	D (C)
8	O (D)	16	O (A)	24	D' (C)

100117F: Number of gates per package = 3

Pin	Signal	Pin	Signal	Pin	Signal
1	D3 (B)	9	VCC	17	D3 (A)
2	D4 (B)	10	VCCA	18	D4 (A)
3	D1 (C)	11	O (B)	19	E (A)
4	D2 (C)	12	O' (B)	20	E (B)
5	D3 (C)	13	O' (A)	21	VEE
6	D4 (C)	14	O (A)	22	E (C)
7	O (C)	15	D1 (A)	23	D1 (B)
8	O' (C)	16	D2 (A)	24	D2 (B)

100118F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	D3C	9	VCC	17	D5A
2	D4C	10	VCCA	18	D1B
3	D1D	11	O'	19	D2B
4	D2D	12	O	20	D3B
5	D3D	13	D1A	21	VEE
6	D4D	14	D2A	22	D4B
7	D1E	15	D3A	23	D1C
8	D2E	16	D4A	24	D2C

100121F: Number of gates per package = 9

Pin	Signal	Pin	Signal	Pin	Signal
1	D (A)	9	VCC	17	D (D)
2	D (B)	10	VCCA	18	D (E)
3	D (C)	11	O' (H)	19	D (F)
4	VCCA	12	O' (G)	20	D (G)
5	O' (C)	13	O' (F)	21	VEE
6	O' (B)	14	O' (E)	22	VCCA
7	O' (A)	15	O' (D)	23	D (H)
8	O' (I)	16	VCCA	24	D (I)

100122F: Number of gates per package = 9

Pin	Signal	Pin	Signal	Pin	Signal
1	D (A)	9	VCC	17	D (D)
2	D (B)	10	VCCA	18	D (E)
3	D (C)	11	O (H)	19	D (F)
4	VCCA	12	O (G)	20	D (G)
5	O (C)	13	O (F)	21	VEE
6	O (B)	14	O (E)	22	VCCA
7	O (A)	15	O (D)	23	D (H)
8	O (I)	16	VCCA	24	D (I)

100123F: Number of gates per package = 3

Pin	Signal	Pin	Signal	Pin	Signal
1 =	DA (C)	9 =	VCC	17 =	DB (A)
2 =	DB (B)	10 =	VCCA1 (A)	18 =	DA (A)
3 =	OB (C)	11 =	OA (A)	19 =	DE (A)
4 =	VCCA2 (C)	12 =	VCCA2 (A)	20 =	DE (B)
5 =	OA (C)	13 =	OB (A)	21 =	VEE
6 =	VCCA1 (C)	14 =	VCCA1 (B)	22 =	E
7 =	OB (B)	15 =	OA (B)	23 =	DE (C)
8 =	VCCA2 (B)	16 =	DA (B)	24 =	DB (C)

100124F: Number of gates per package = 6

Pin	Signal	Pin	Signal	Pin	Signal
1 =	D (B)	9 =	VCC	17 =	O (F)
2 =	D (C)	10 =	VCCA	18 =	D (F)
3 =	O (A)	11 =	VCCA	19 =	D (E)
4 =	O' (A)	12 =	O (D)	20 =	D (D)
5 =	O (B)	13 =	O' (D)	21 =	VEE
6 =	O' (B)	14 =	O' (E)	22 =	E
7 =	O' (C)	15 =	O (E)	23 =	VTTL
8 =	O (C)	16 =	O' (F)	24 =	D (A)

100125F: Number of gates per package = 6

Pin	Signal	Pin	Signal	Pin	Signal
1 =	D' (E)	9 =	VCC	17 =	D (B)
2 =	D (F)	10 =	VCC	18 =	D' (C)
3 =	D' (F)	11 =	O (C)	19 =	D (C)
4 =	O (F)	12 =	O (B)	20 =	VBB
5 =	O (E)	13 =	O (A)	21 =	VEE
6 =	O (D)	14 =	D' (A)	22 =	D (D)
7 =	VTTL	15 =	D (A)	23 =	D' (D)
8 =	VTTL	16 =	D' (B)	24 =	D (E)

100126F: Number of gates per package = 9

Pin	Signal	Pin	Signal	Pin	Signal
1	D (A)	9	VCC	17	D (D)
2	D (B)	10	VCCA	18	D (E)
3	D (C)	11	O (H)	19	D (F)
4	VCCA	12	O (G)	20	D (G)
5	O (C)	13	O (F)	21	VEE
6	O (B)	14	O (E)	22	VCCA
7	O (A)	15	O (D)	23	D (H)
8	O (I)	16	VCCA	24	D (I)

100128F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	E1	9	VCC	17	T2
2	E2	10	VCCA	18	T1
3	E3	11	DIR	19	T0
4	E4	12	T7	20	LE
5	E5	13	T6	21	VEE
6	E6	14	T5	22	VCC
7	E7	15	T4	23	VTTL
8	OE	16	T3	24	E0

100130F: Number of gates per package = 3

Pin	Signal	Pin	Signal	Pin	Signal
1	E' (B)	9	VCC	17	CD (A)
2	CD (B)	10	VCCA	18	SD (A)
3	SD (C)	11	Q (B)	19	MS
4	CD (C)	12	Q' (B)	20	EC'
5	E' (C)	13	Q' (A)	21	VEE
6	D (C)	14	Q (A)	22	MR
7	Q (C)	15	D (A)	23	SD (B)
8	Q' (C)	16	E' (A)	24	D (B)

100131F: Number of gates per package = 3

Pin	Signal	Pin	Signal	Pin	Signal
1	CP (B)	9	VCC	17	CD (A)
2	CD (B)	10	VCCA	18	SD (A)
3	SD (C)	11	Q (B)	19	MS
4	CD (C)	12	Q' (B)	20	CPC
5	CP (C)	13	Q' (A)	21	VEE
6	D (C)	14	Q (A)	22	MR
7	Q (C)	15	D (A)	23	SD (B)
8	Q' (C)	16	CP (A)	24	D (B)

100135F: Number of gates per package = 3

Pin	Signal	Pin	Signal	Pin	Signal
1	C (B)	9	VCC	17	CP (A)
2	CP (C)	10	VCCA	18	J (A)
3	C (C)	11	Q' (B)	19	K (A)
4	S (C)	12	Q (B)	20	S (B)
5	J (C)	13	Q' (A)	21	VEE
6	K (C)	14	Q (A)	22	K (B)
7	Q' (C)	15	S (A)	23	J (B)
8	Q (C)	16	C (A)	24	CP (B)

100136F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	S2	9	VCC	17	P2
2	CEP'	10	VCCA	18	P1
3	D0/CET	11	Q2	19	P0
4	TC'	12	Q2'	20	CP
5	Q0	13	Q3'	21	VEE
6	Q0'	14	Q3	22	MR
7	Q1'	15	D3	23	S0
8	Q1	16	P3	24	S1

100139F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	P3	9	VCC	17	Q3'
2	P2	10	VCCA	18	Q3
3	P1	11	TC14'	19	PE2
4	P0	12	PE1	20	CP
5	Q0'	13	TC15'	21	VEE
6	Q0	14	TC14	22	CEP
7	Q1'	15	Q2'	23	MR
8	Q1	16	Q2	24	CET

100140F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	P3	9	VCC	17	Q3'
2	P2	10	VCCA	18	Q3
3	P1	11	TC1'	19	PE2
4	P0	12	PE1	20	CP
5	Q0'	13	TC0'	21	VEE
6	Q0	14	TC1	22	CEP
7	Q1'	15	Q2'	23	MR
8	Q1	16	Q2	24	CET

100141F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	P2	9	VCC	17	P6
2	P1	10	VCCA	18	P5
3	P0	11	Q4	19	P4
4	D0	12	Q5	20	CP
5	Q0	13	Q6	21	VEE
6	Q1	14	Q7	22	S0
7	Q2	15	D7	23	S1
8	Q3	16	P7	24	P3

100142F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	D2	9	VCC	17	MK0
2	MK2	10	VCCA	18	D0
3	D3	11	Q3	19	A3
4	MK3	12	Q2	20	A2
5	M0	13	Q1	21	VEE
6	M1	14	Q0	22	WS
7	M2	15	MK1	23	A1
8	M3	16	D1	24	A0

100145F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	AW2	9	VCC	17	OE1
2	AW3	10	VCCA	18	OE2
3	AR3	11	Q2	19	WE1
4	AR2	12	Q3	20	WE2
5	AR1	13	D3	21	VEE
6	AR0	14	D2	22	MR
7	Q0	15	D1	23	AW0
8	Q1	16	D0	24	AW1

100150F: Number of gates per package = 6

Pin	Signal	Pin	Signal	Pin	Signal
1	D (E)	9	VCC	17	D (A)
2	D (F)	10	VCCA	18	D (B)
3	Q (F)	11	Q' (C)	19	D (C)
4	Q' (F)	12	Q (C)	20	D (D)
5	Q' (E)	13	Q' (B)	21	VEE
6	Q (E)	14	Q (B)	22	MR
7	Q' (D)	15	Q' (A)	23	EA'
8	Q (D)	16	Q (A)	24	EB'

100151F: Number of gates per package = 6

Pin	Signal	Pin	Signal	Pin	Signal
1 =	D (E)	9 =	VCC	17 =	D (A)
2 =	D (F)	10 =	VCCA	18 =	D (B)
3 =	Q (F)	11 =	Q' (C)	19 =	D (C)
4 =	Q' (F)	12 =	Q (C)	20 =	D (D)
5 =	Q' (E)	13 =	Q' (B)	21 =	VEE
6 =	Q (E)	14 =	Q (B)	22 =	MR
7 =	Q' (D)	15 =	Q' (A)	23 =	CPA
8 =	Q (D)	16 =	Q (A)	24 =	CPB

100155F: Number of gates per package = 4

Pin	Signal	Pin	Signal	Pin	Signal
1 =	E2' (C)	9 =	VCC	17 =	E2' (B)
2 =	D0 (C)	10 =	VCCA	18 =	D0 (B)
3 =	E2' (D)	11 =	Q' (B)	19 =	D1
4 =	D0 (D)	12 =	Q (B)	20 =	S0'
5 =	Q (D)	13 =	Q (A)	21 =	VEE
6 =	Q' (D)	14 =	Q' (A)	22 =	S1
7 =	Q' (C)	15 =	E2' (A)	23 =	MR
8 =	Q (C)	16 =	D0 (A)	24 =	E1'

100156F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1 =	BM0	9 =	VCC	17 =	B2
2 =	AM0	10 =	VCCA	18 =	A2
3 =	BM1	11 =	Q1	19 =	BS0
4 =	AM1	12 =	Q0	20 =	E'
5 =	A3	13 =	B0	21 =	VEE
6 =	B3	14 =	A0	22 =	AS0
7 =	Q3	15 =	B1	23 =	BS1
8 =	Q2	16 =	A1	24 =	AS1

100158F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	D5	9	VCC	17	D2
2	D6	10	VCCA	18	D3
3	D7	11	Z3	19	S0
4	Z7	12	Z2	20	S1
5	Z6	13	Z1	21	VEE
6	Z5	14	Z0	22	M
7	Z4	15	D0	23	S2
8	VCCA	16	D1	24	D4

100160F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	I3B	9	VCC	17	I4A
2	I4B	10	VCCA	18	I5A
3	I5B	11	ZA	19	I6A
4	I6B	12	IA	20	I7A
5	I7B	13	I0A	21	VEE
6	IB	14	I1A	22	I0B
7	ZB	15	I2A	23	I1B
8	C'	16	I3A	24	I2B

100163F: Number of gates per package = 2

Pin	Signal	Pin	Signal	Pin	Signal
1	D6 (B)	9	VCC	17	D5 (A)
2	D5 (B)	10	VCCA	18	D6 (A)
3	D4 (B)	11	Z (A)	19	D7 (A)
4	D3 (B)	12	D0 (A)	20	S0
5	D2 (B)	13	D1 (A)	21	VEE
6	D1 (B)	14	D2 (A)	22	S1
7	D0 (B)	15	D3 (A)	23	S2
8	Z (B)	16	D4 (A)	24	D7 (B)

100164F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	I0	9	VCC	17	I13
2	I1	10	VCCA	18	I14
3	I2	11	Z	19	I15
4	I3	12	I8	20	S0
5	I4	13	I9	21	VEE
6	I5	14	I10	22	S1
7	I6	15	I11	23	S2
8	I7	16	I12	24	S3

100165F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	I2	9	VCC	17	I6
2	I1	10	VCCA	18	I5
3	I0	11	GS2	19	I4
4	Q0	12	Q2	20	OE'
5	Q0'	13	Q2'	21	VEE
6	Q1'	14	Q3'	22	E'
7	Q1	15	Q3	23	M
8	GS1	16	I7	24	I3

100166F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	B5	9	VCC	17	A5
2	B4	10	VCCA	18	A6
3	B3	11	A>B	19	A7
4	B2	12	A0	20	A8
5	B1	13	A1	21	VEE
6	B0	14	A2	22	B8
7	A<B	15	A3	23	B7
8	A=B	16	A4	24	B6

100170F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	HC	9	VCC	17	M
2	HB	10	VCCA	18	A2A
3	A0B	11	Z3	19	EA1
4	A1B	12	Z0	20	EB1
5	Z7	13	Z2	21	VEE
6	Z4	14	Z1	22	EB2
7	Z6	15	A0A	23	EA2
8	Z5	16	A1A	24	HA

100171F: Number of gates per package = 3

Pin	Signal	Pin	Signal	Pin	Signal
1	I2 (B)	9	VCC	17	I2 (A)
2	I3 (B)	10	VCCA	18	I3 (A)
3	I0 (C)	11	Z (B)	19	S0
4	I1 (C)	12	Z' (B)	20	S1
5	I2 (C)	13	Z' (A)	21	VEE
6	I3 (C)	14	Z (A)	22	E'
7	Z (C)	15	I0 (A)	23	I0 (B)
8	Z' (C)	16	I1 (A)	24	I1 (B)

100179F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	G0	9	VCC	17	G5
2	P0	10	VCCA	18	P5
3	G1	11	CN+6	19	G6
4	P1	12	CN+8	20	P6
5	G2	13	G3	21	VEE
6	P2	14	P3	22	CN
7	CN+2	15	G4	23	G7
8	CN+4	16	P4	24	P7

100180F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1 =	B1	9 =	VCC	17 =	B4
2 =	A1	10 =	VCCA	18 =	A4
3 =	B0	11 =	F4	19 =	B3
4 =	A0	12 =	F5	20 =	A3
5 =	F0	13 =	P	21 =	VEE
6 =	F1	14 =	G	22 =	CN
7 =	F2	15 =	B5	23 =	B2
8 =	F3	16 =	A5	24 =	A2

100181F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1 =	A3	9 =	VCC	17 =	B2
2 =	A2	10 =	VCCA	18 =	B3
3 =	A1	11 =	CN+4	19 =	S0
4 =	A0	12 =	P	20 =	S1
5 =	F0	13 =	G	21 =	VEE
6 =	F1	14 =	CN	22 =	E
7 =	F2	15 =	B0	23 =	S2
8 =	F3	16 =	B1	24 =	S3

100182F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1 =	D4	9 =	VCC	17 =	CIN-2
2 =	D3	10 =	VCCA	18 =	D8
3 =	D2	11 =	CO2	19 =	D7
4 =	D1	12 =	PC	20 =	D6
5 =	D0	13 =	PS	21 =	VEE
6 =	CON+2	14 =	CI3	22 =	D5
7 =	CO3	15 =	CI2	23 =	{n/c}
8 =	CO1	16 =	CI1	24 =	{n/c}

100183F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	B3	9	VCC	17	B7
2	B2	10	VCCA	18	B6
3	B1	11	F4	19	B5
4	B0	12	F5	20	B4
5	F0	13	F6	21	VEE
6	F1	14	F7	22	A2
7	F2	15	F8'	23	A1
8	F3	16	B8	24	A0

100241F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	P2	9	VCC	17	P6
2	P1	10	VCCA	18	P5
3	P0	11	Q4	19	P4
4	D0	12	Q5	20	CP
5	Q0	13	Q6	21	VEE
6	Q1	14	Q7	22	S0
7	Q2	15	D7	23	S1
8	Q3	16	P7	24	P3

100413F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	D2	9	VCC	17	D6
2	D1	10	VCCA	18	D5
3	D0	11	TO	19	D4
4	Q0	12	Q4	20	IR
5	Q1	13	Q5	21	VEE
6	Q2	14	Q6	22	MR
7	Q3	15	Q7	23	TI
8	OR	16	D7	24	D3

E100142F: Number of gates per package = 1

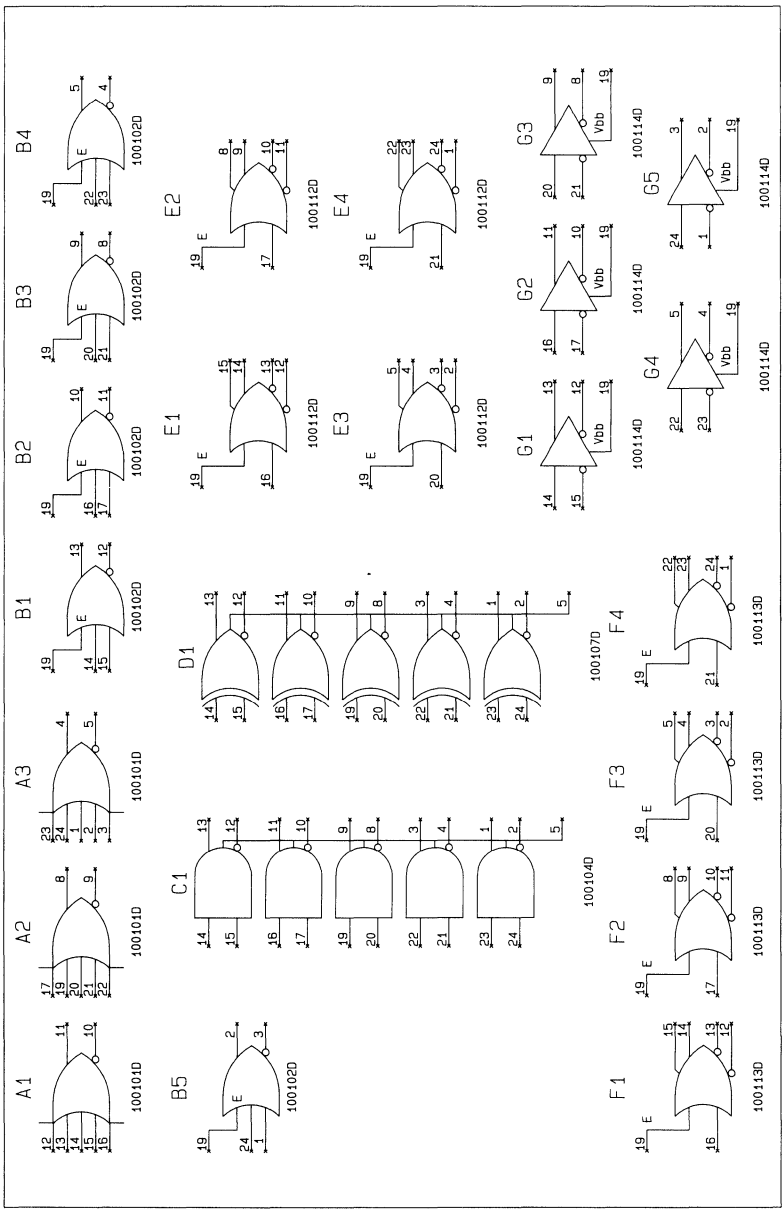
Pin	Signal	Pin	Signal	Pin	Signal
1	D2	9	VCC	17	MK0
2	MK2	10	VCCA	18	D0
3	D3	11	Q3	19	A3
4	MK3	12	Q2	20	A2
5	M0	13	Q1	21	VEE
6	M1	14	Q0	22	WS
7	M2	15	MK1	23	A1
8	M3	16	D1	24	A0

E100165F: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	I2	9	VCC	17	I6
2	I1	10	VCCA	18	I5
3	I0	11	GS2	19	I4
4	Q0	12	Q2	20	OE'
5	Q0'	13	Q2'	21	VEE
6	Q1'	14	Q3'	22	E'
7	Q1	15	Q3	23	M
8	GS1	16	I7	24	I3

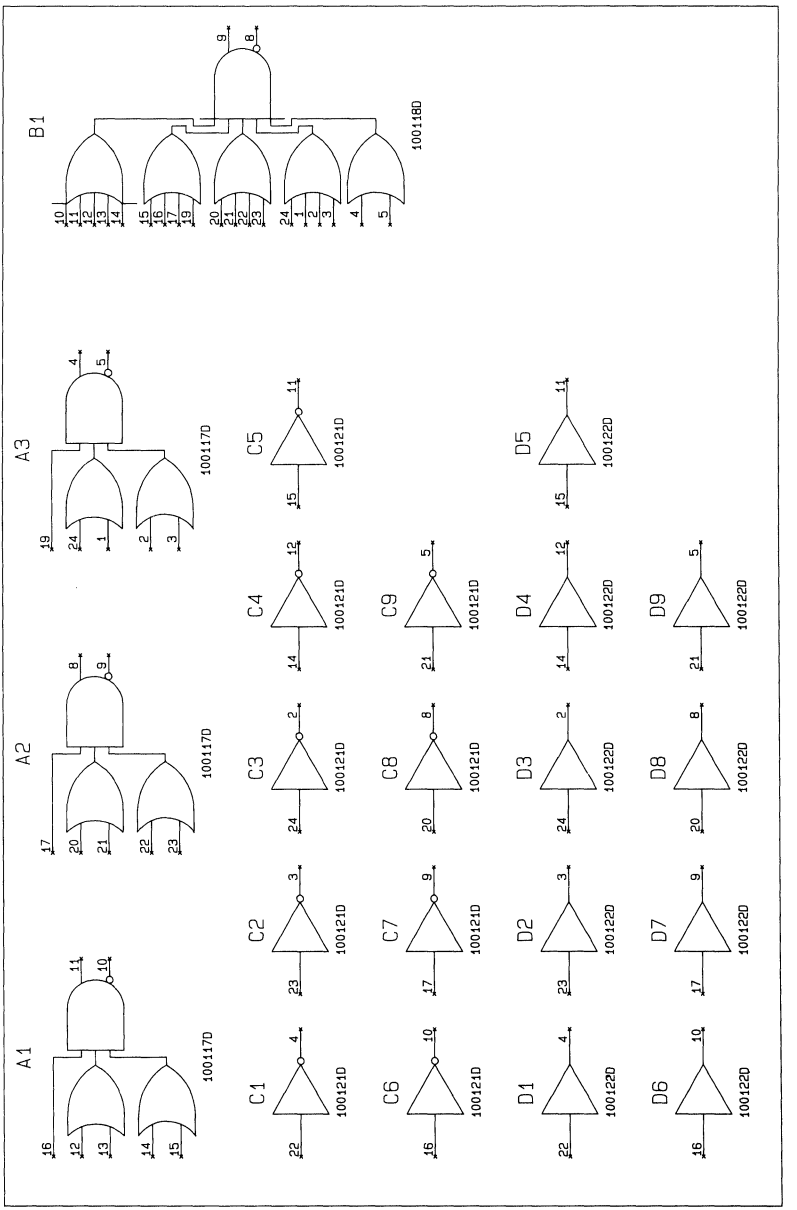
COMPONENT PLOTS

Plot 1



COMPONENT PLOTS

Plot 2



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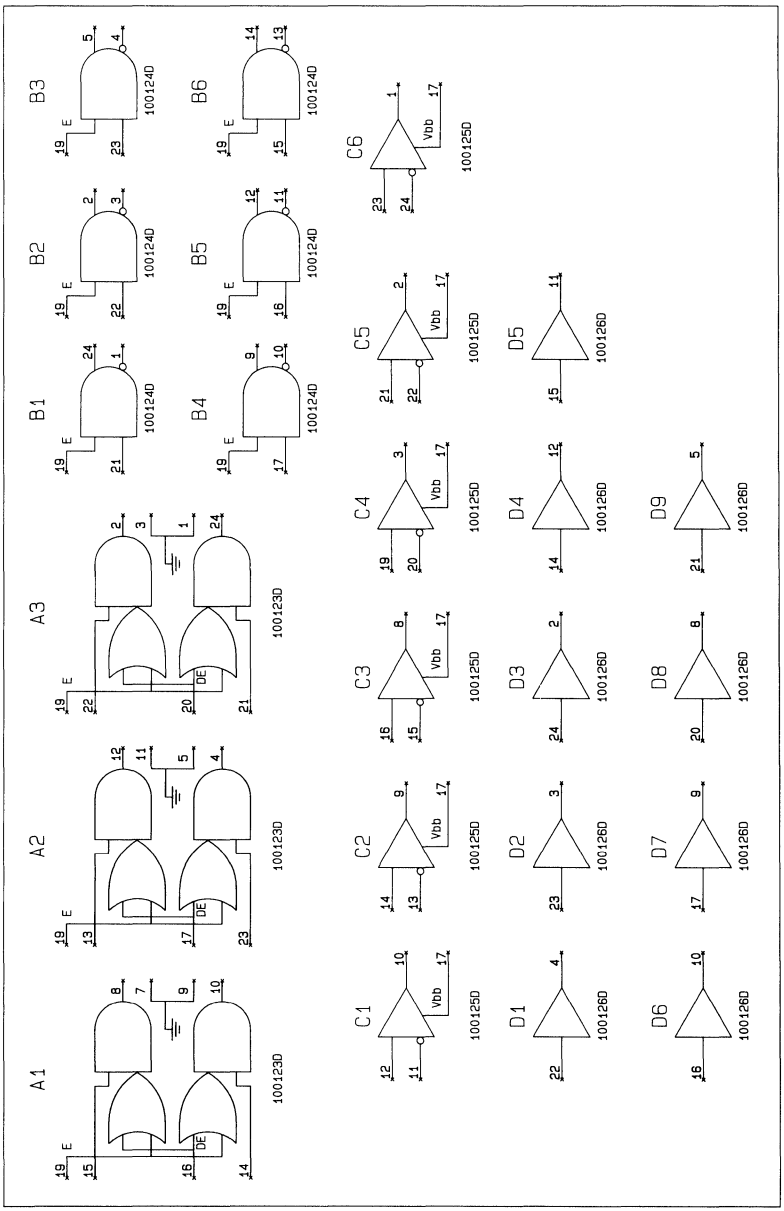
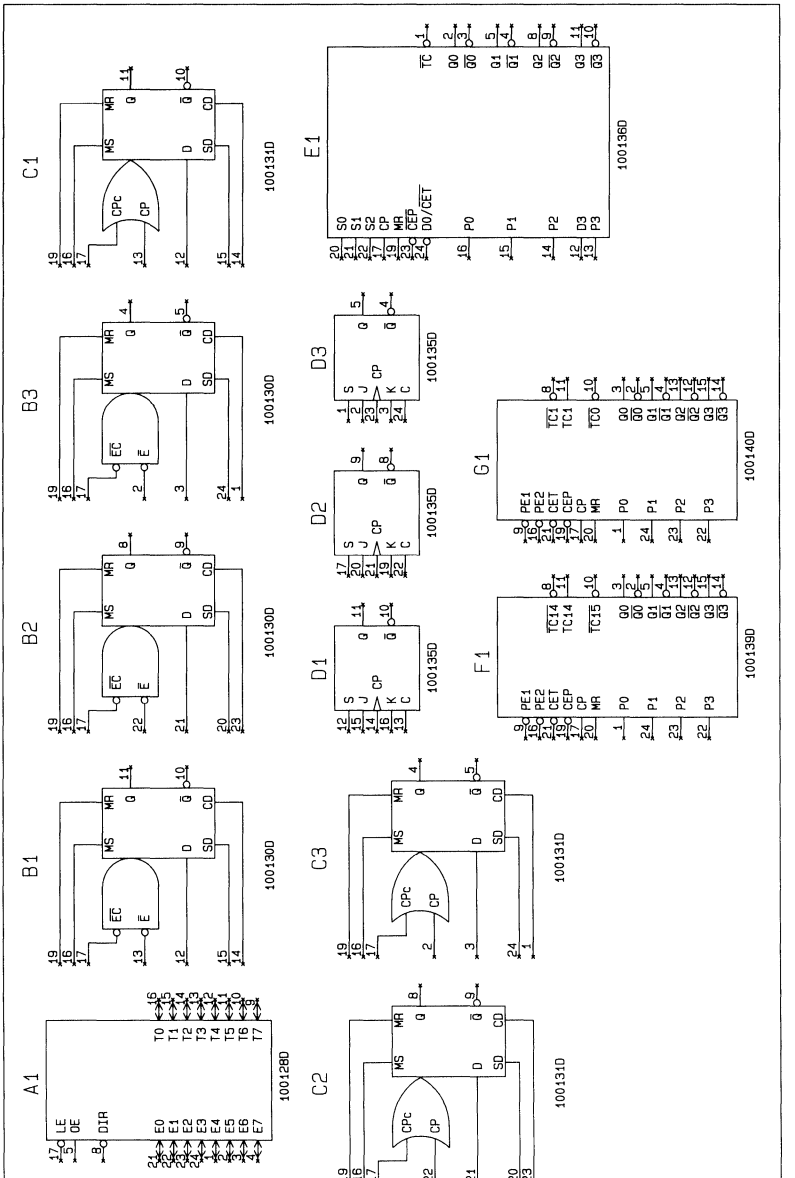
COMPONENT PLOTS

Plot 3



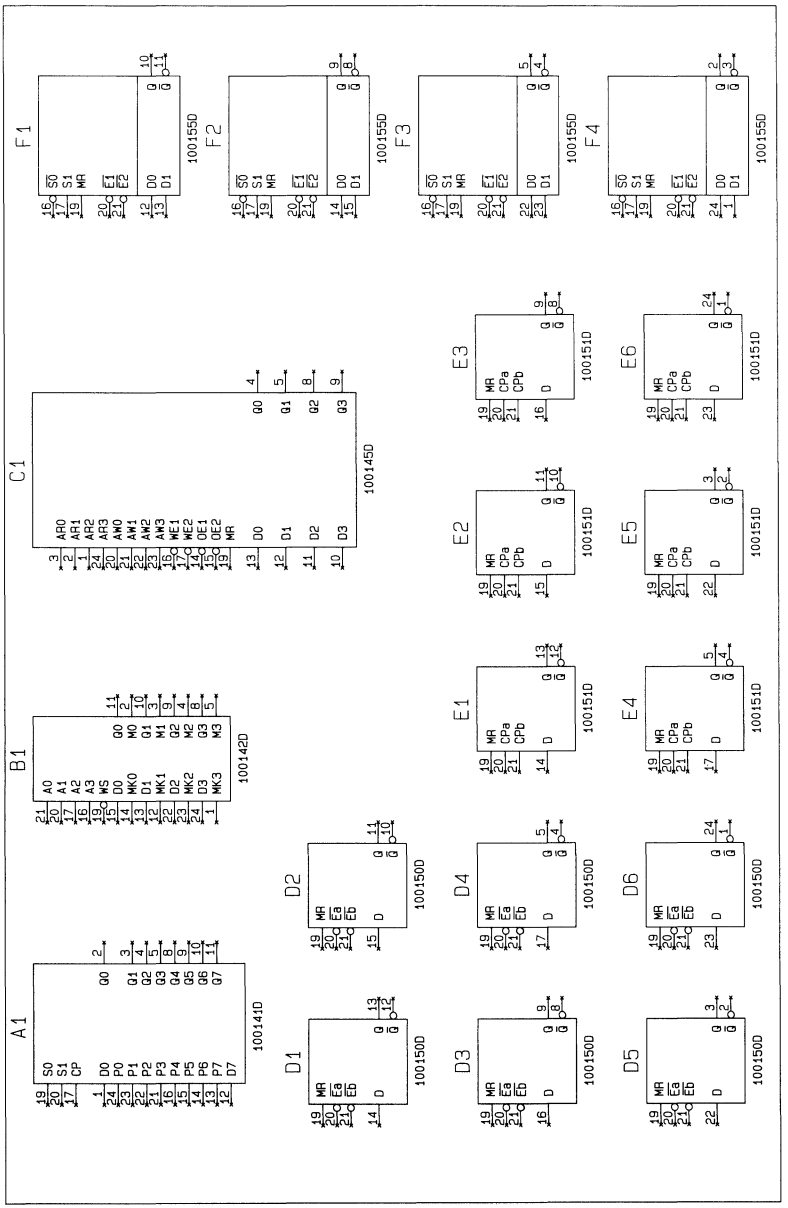
COMPONENT PLOTS

Plot 4



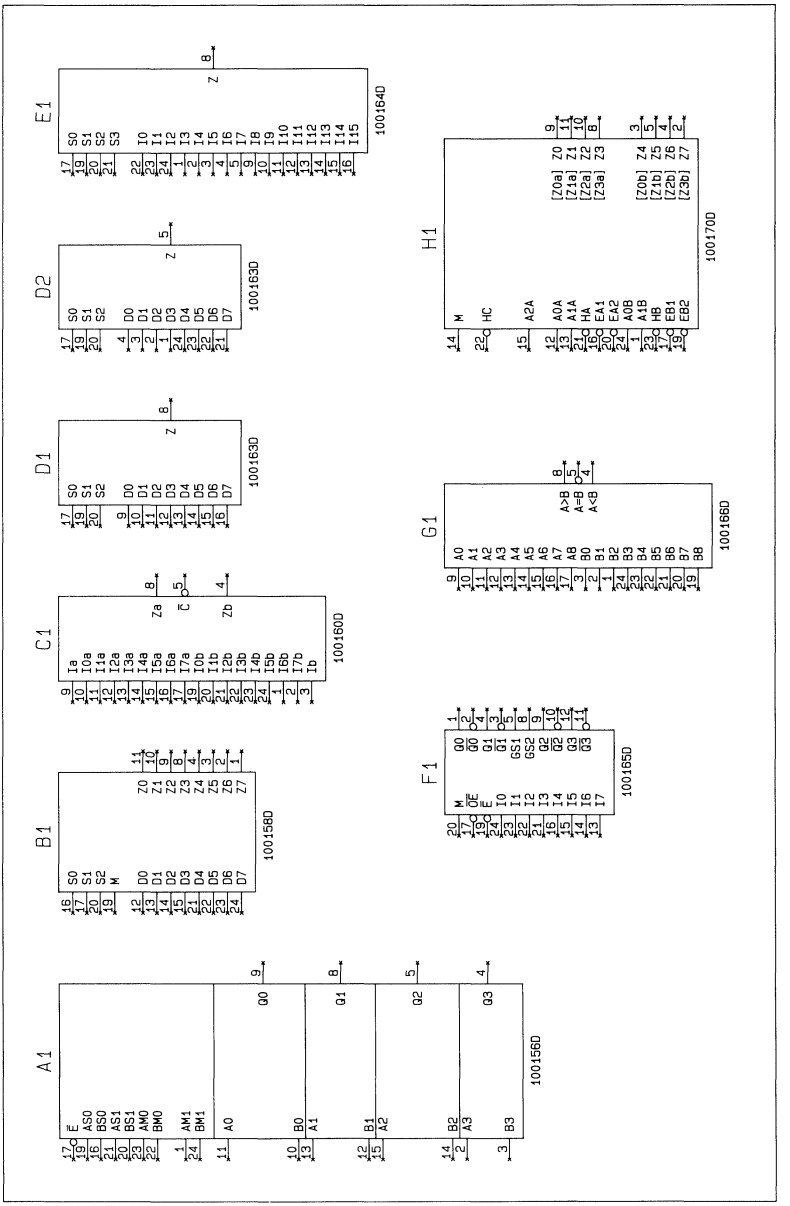
COMPONENT PLOTS

Plot 5



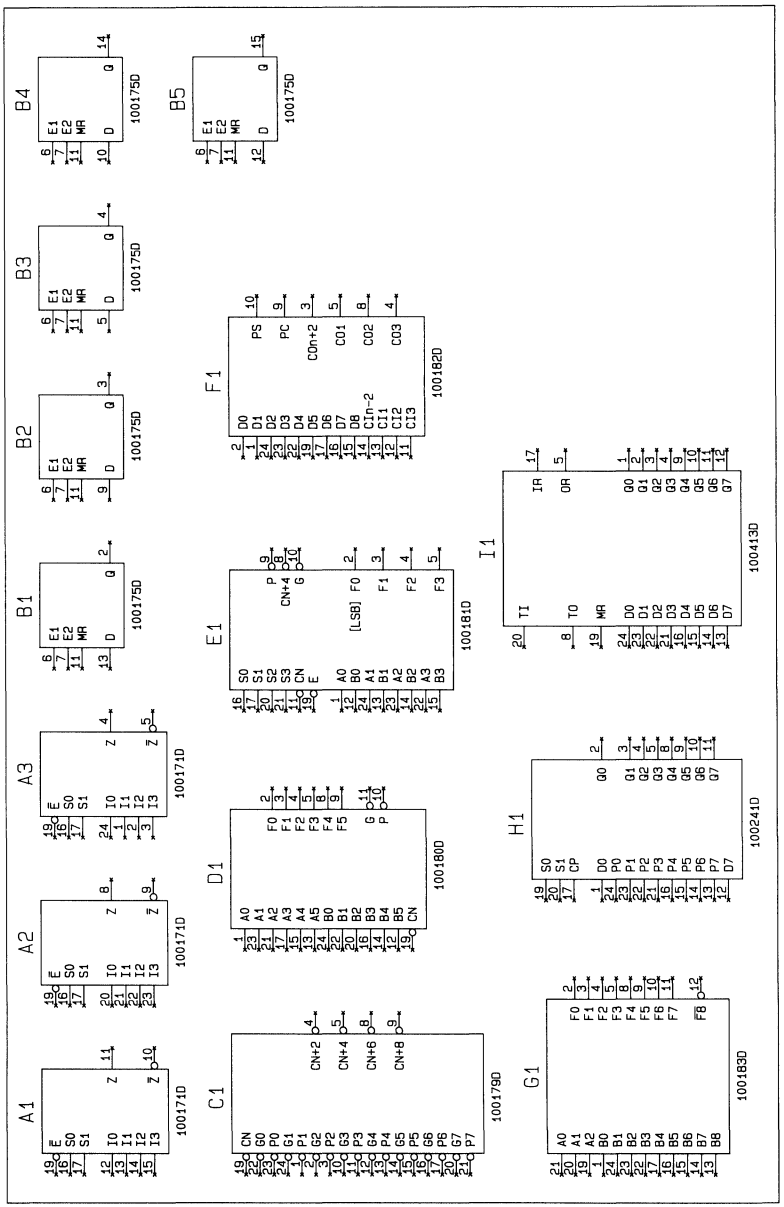
COMPONENT PLOTS

Plot 6



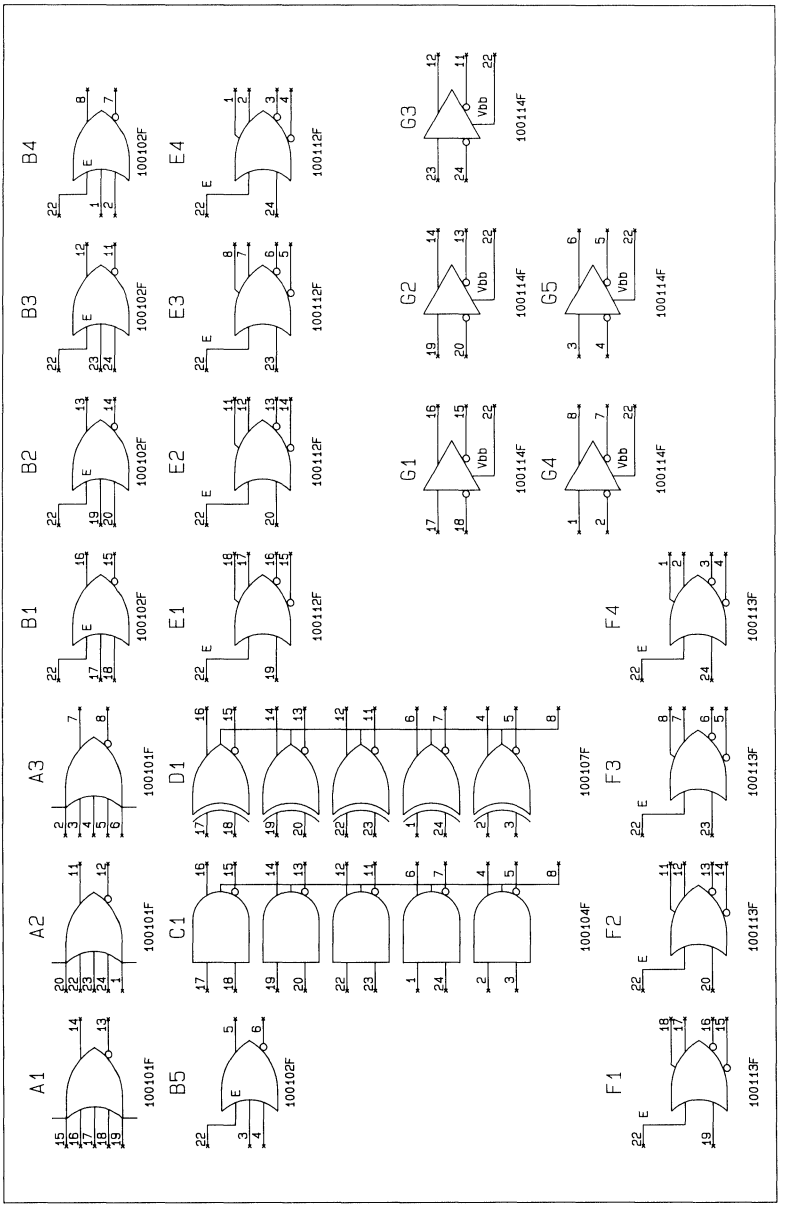
COMPONENT PLOTS

Plot 7



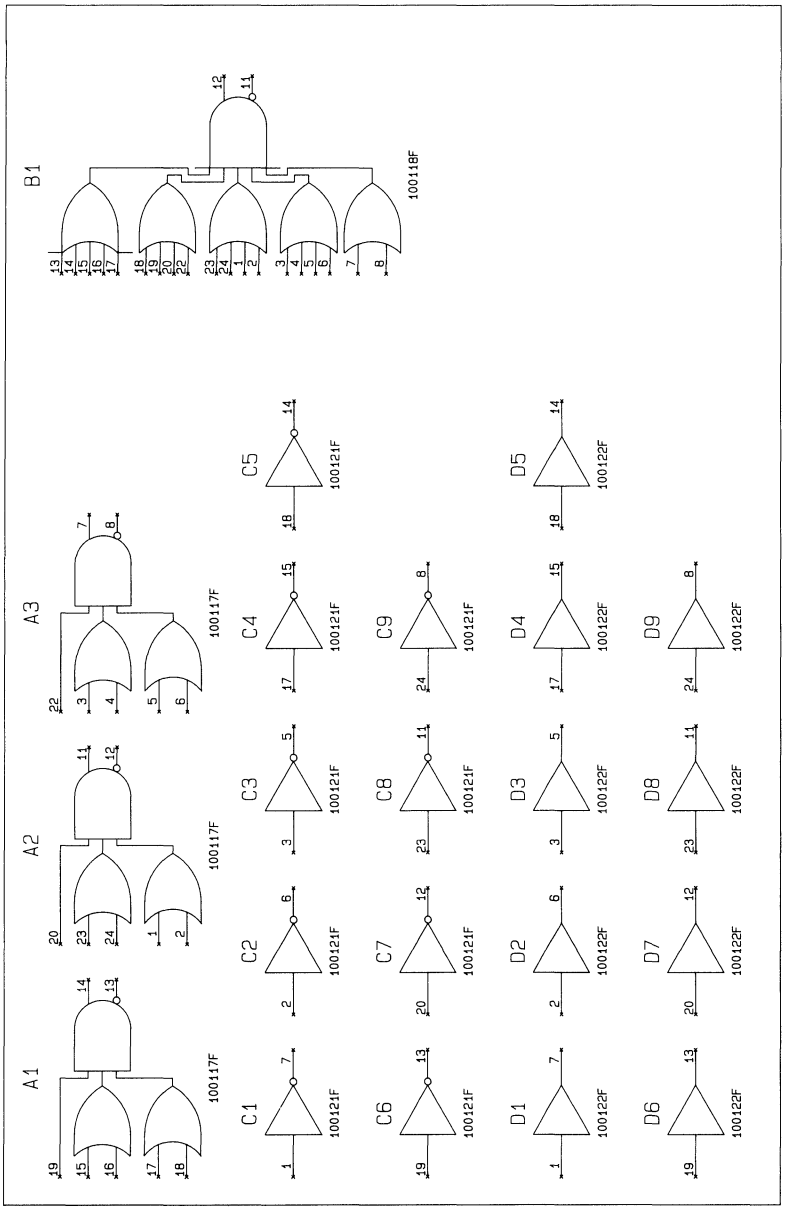
COMPONENT PLOTS

Plot 8



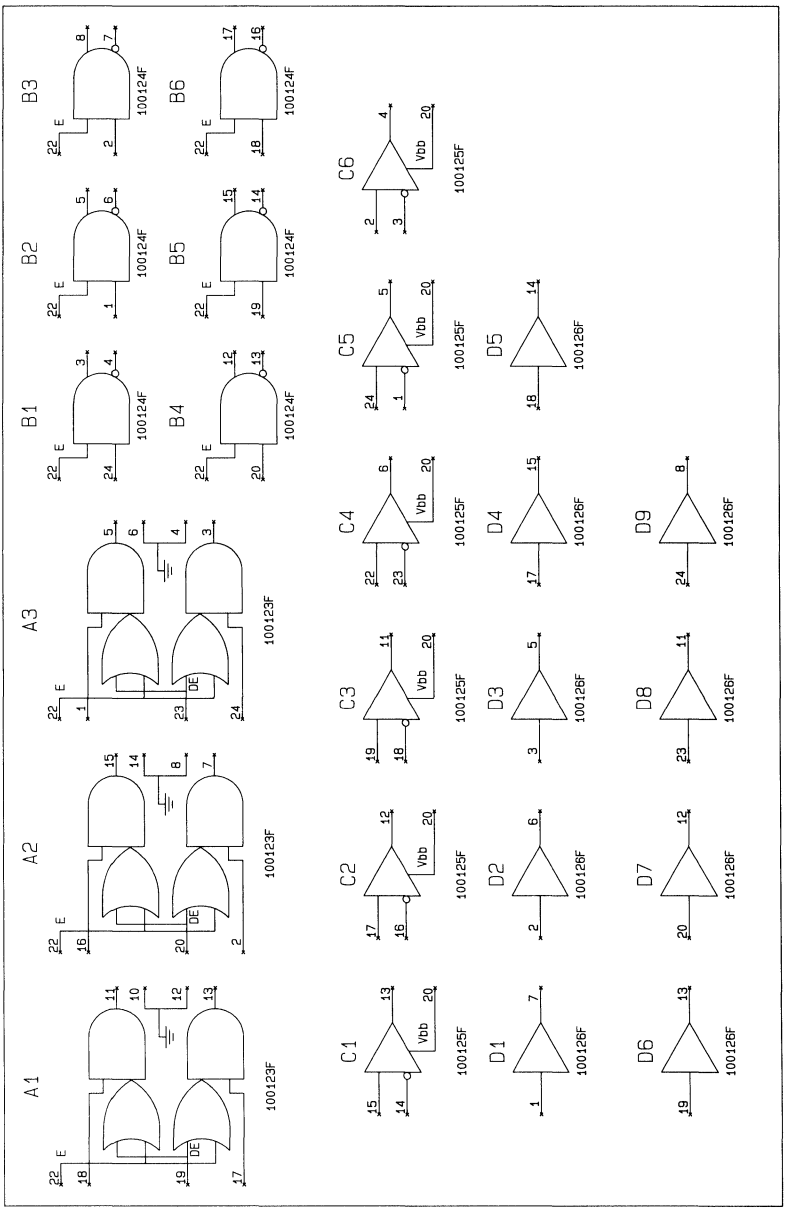
COMPONENT PLOTS

Plot 9



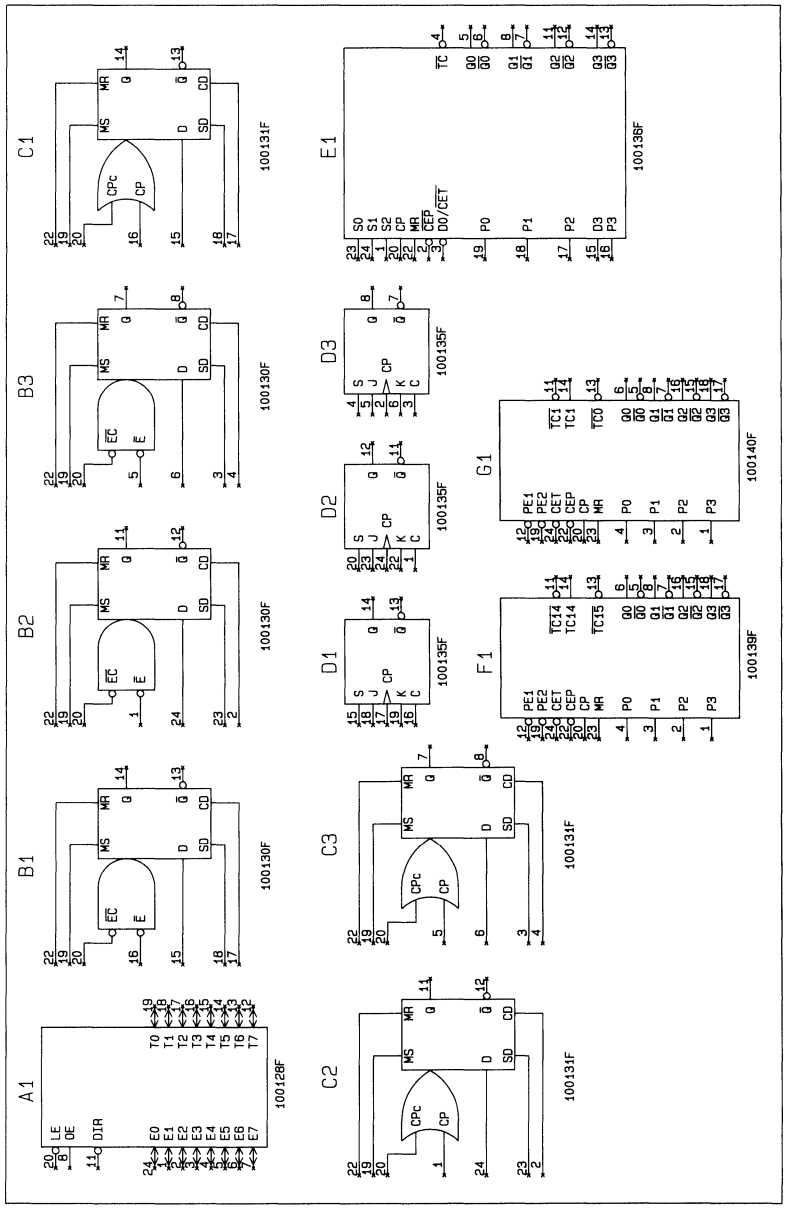
COMPONENT PLOTS

Plot 10



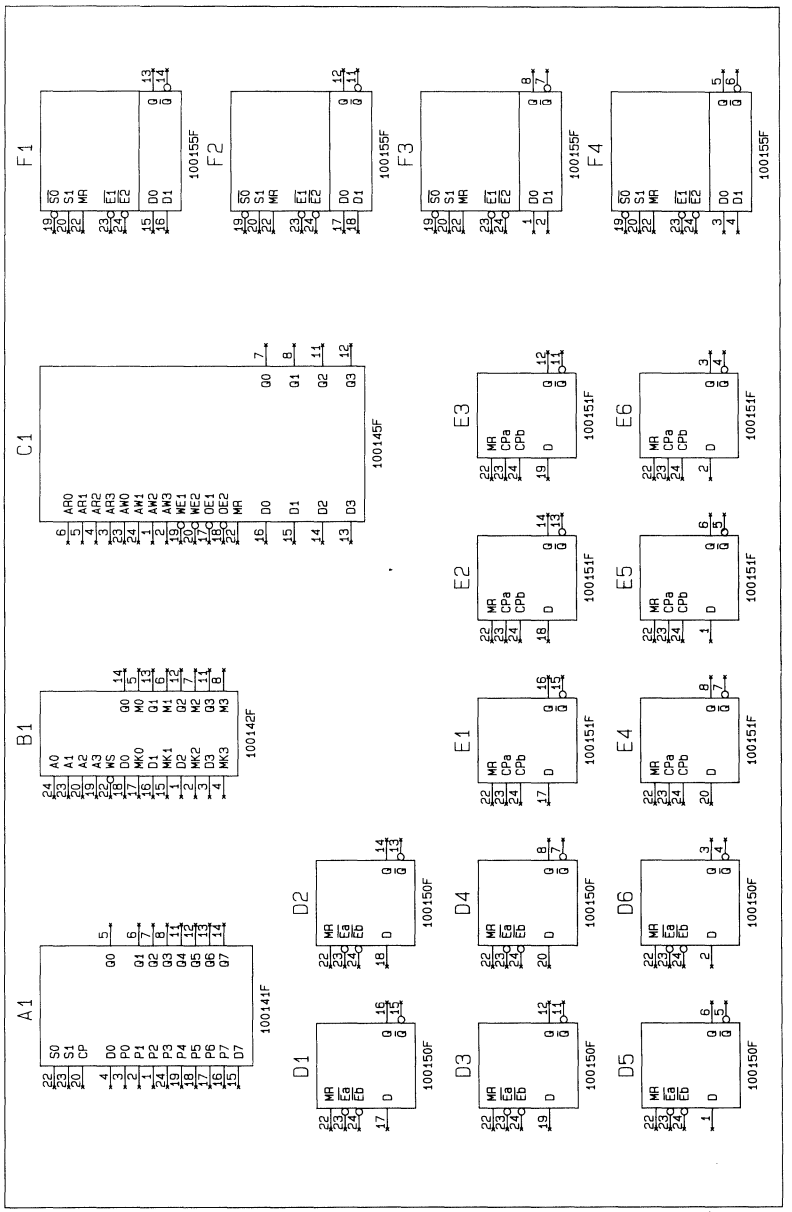
COMPONENT PLOTS

Plot 11



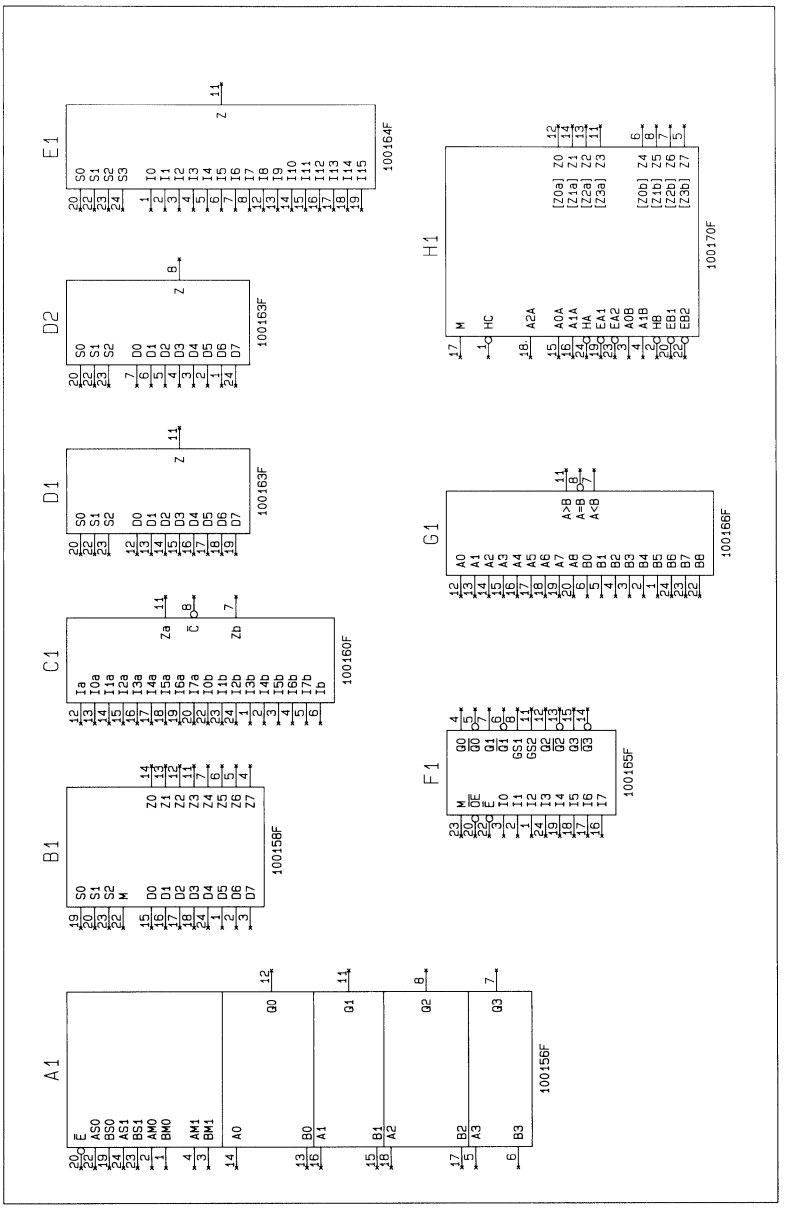
COMPONENT PLOTS

Plot 12



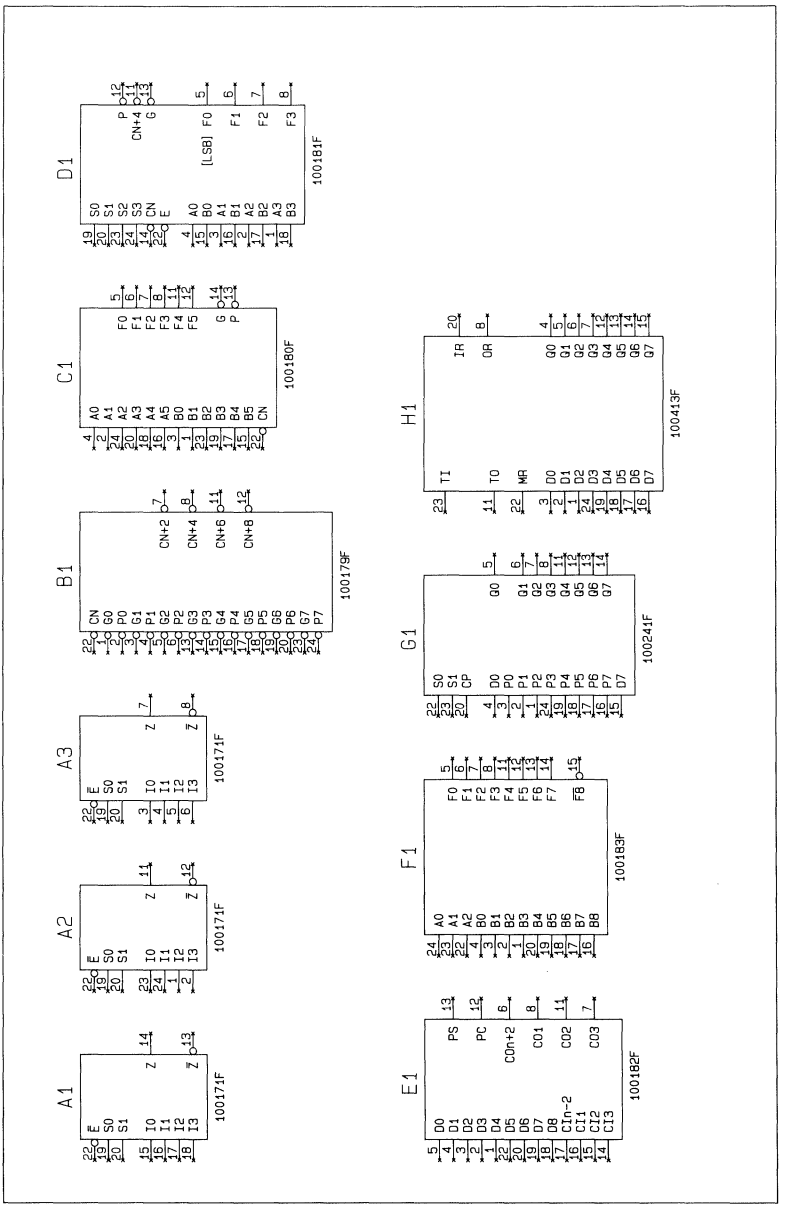
COMPONENT PLOTS

Plot 13



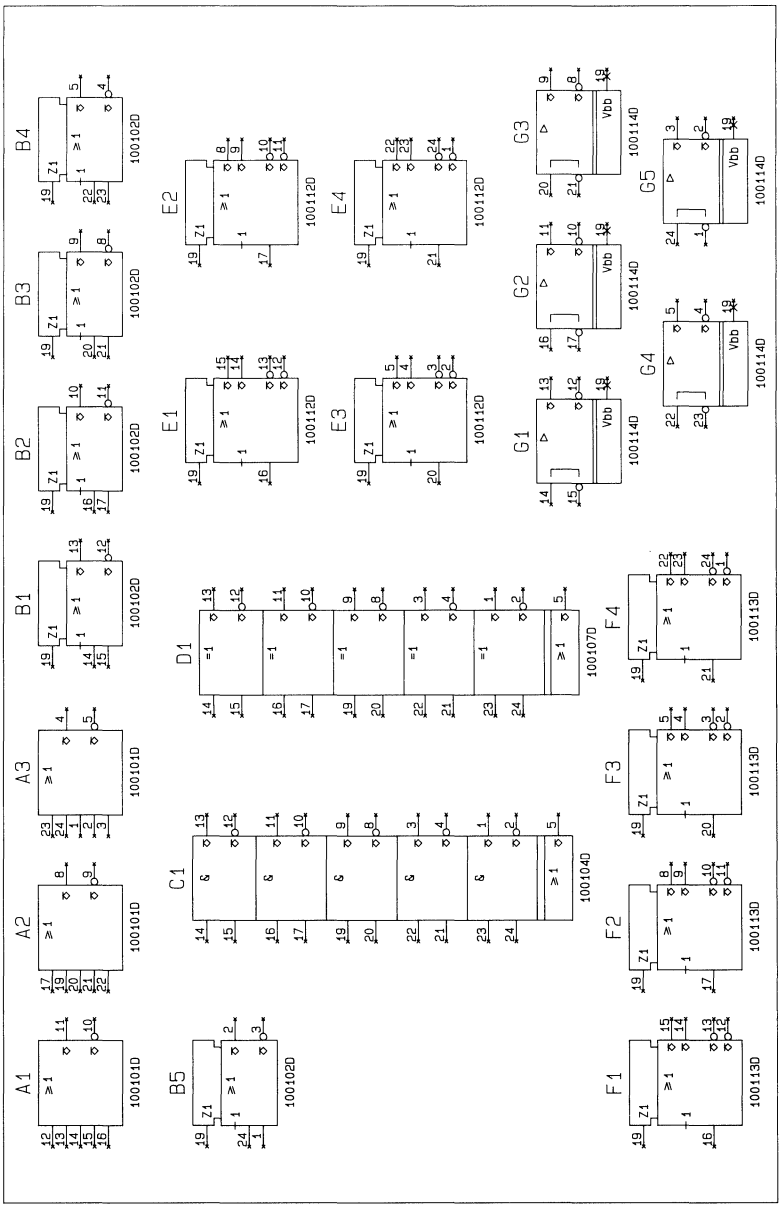
COMPONENT PLOTS

Plot 14



COMPONENT PLOTS

Plot 1A



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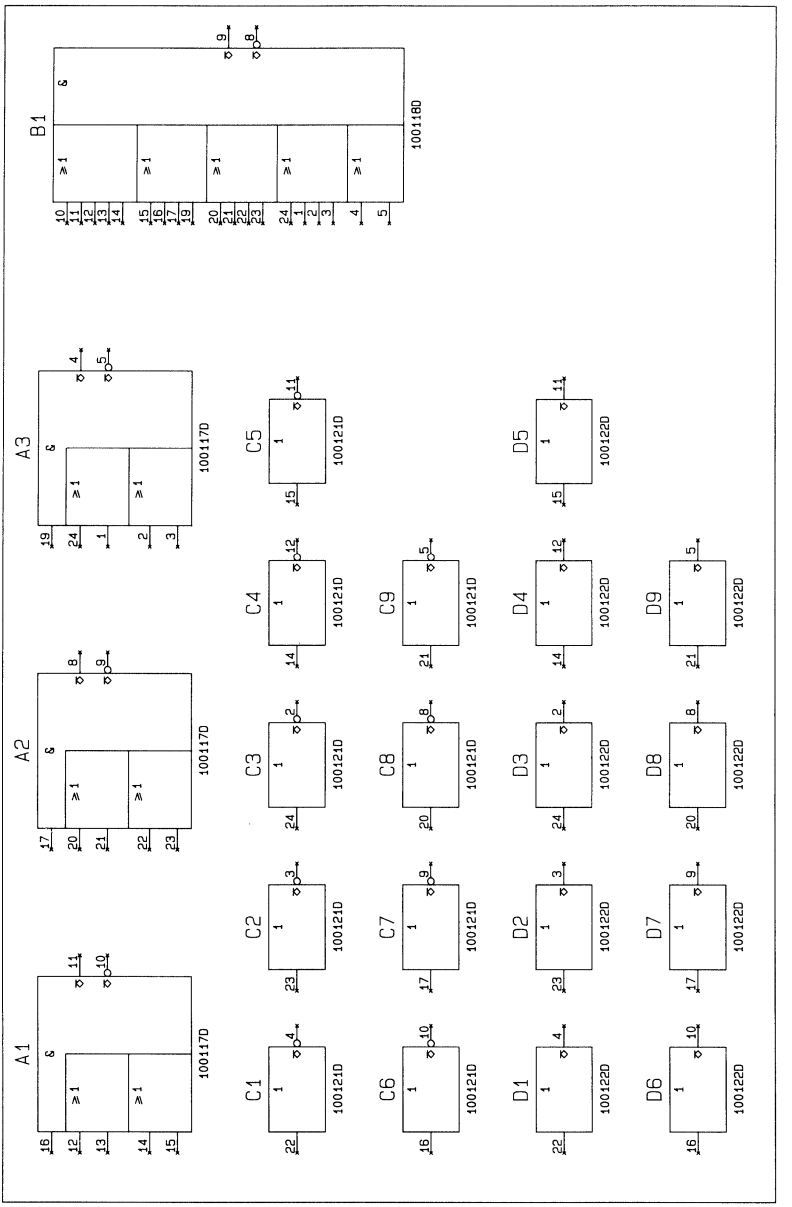
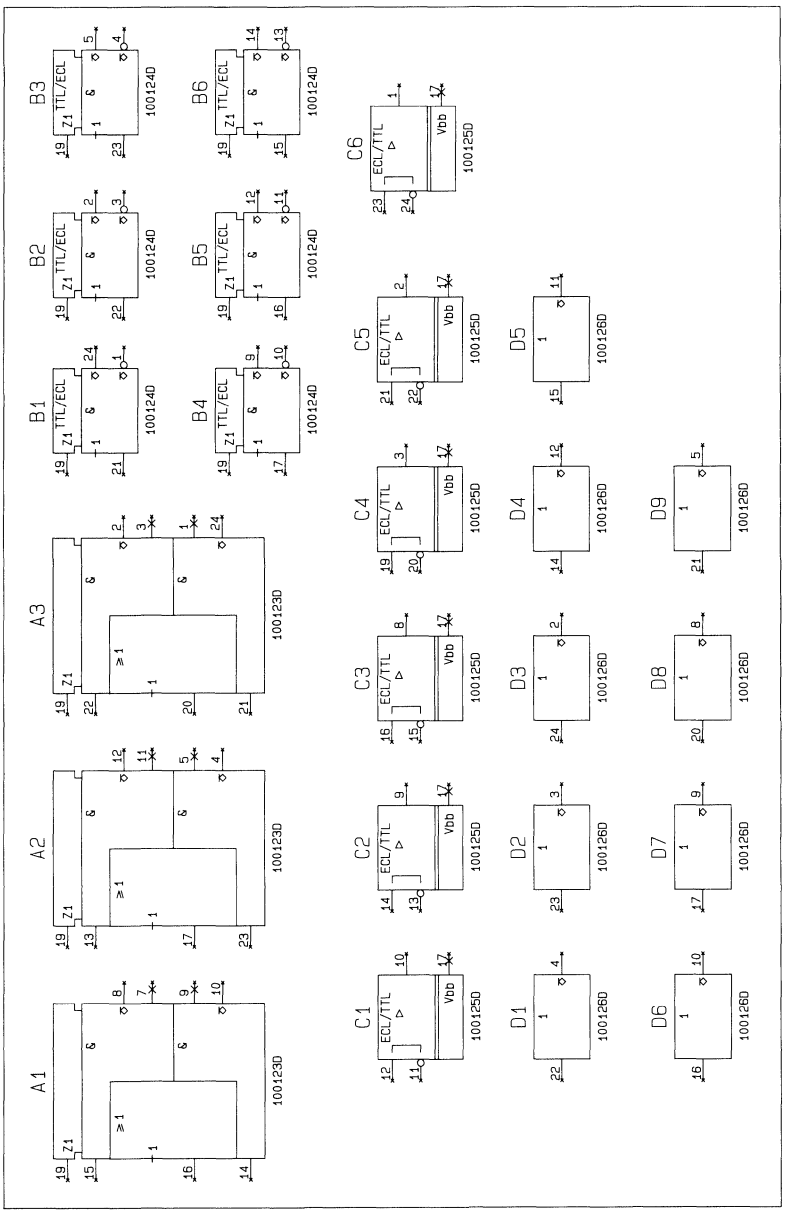
COMPONENT PLOTS

Plot 2A



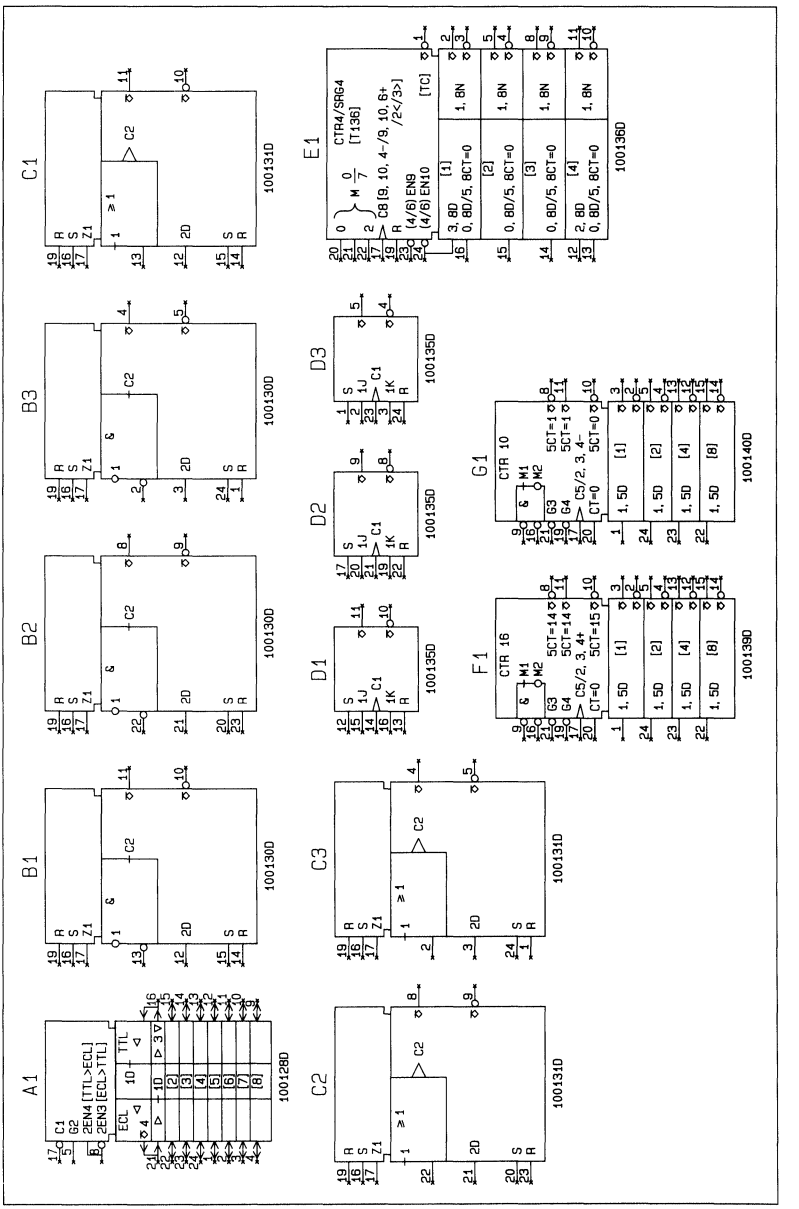
COMPONENT PLOTS

Plot 3A



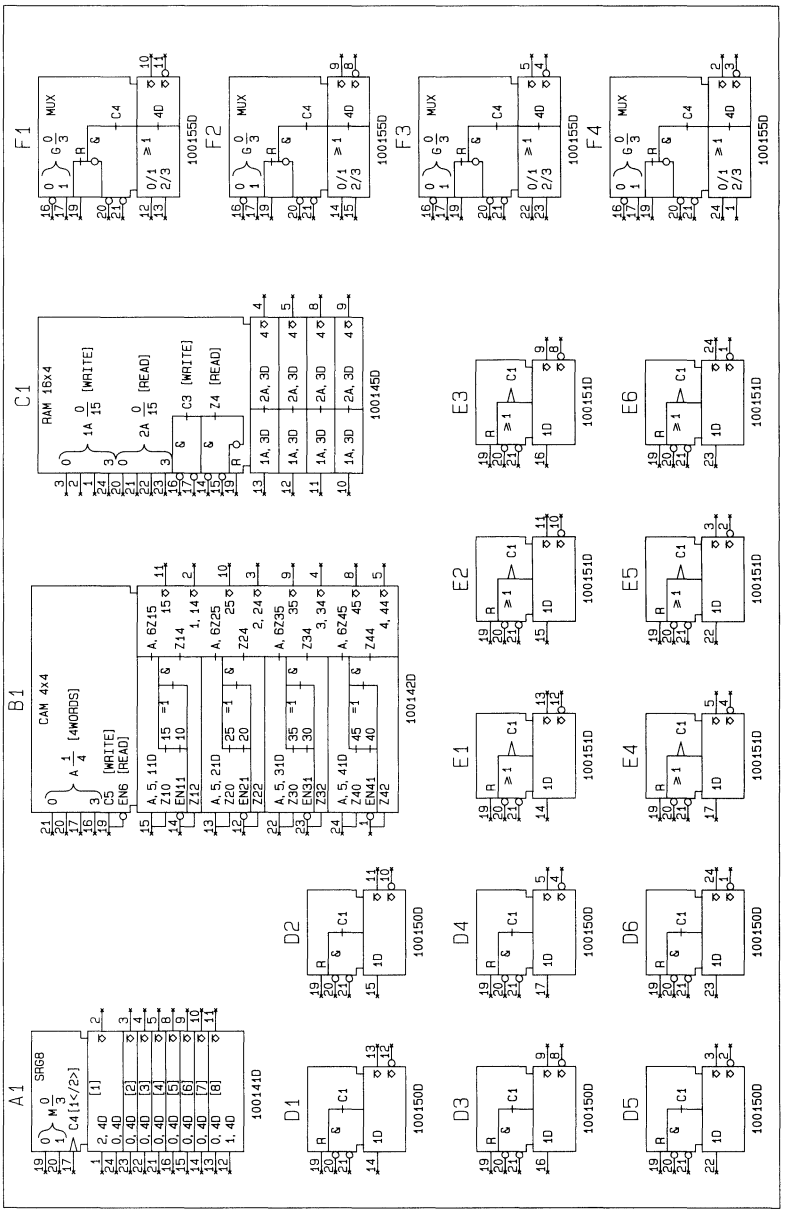
COMPONENT PLOTS

Plot 4A



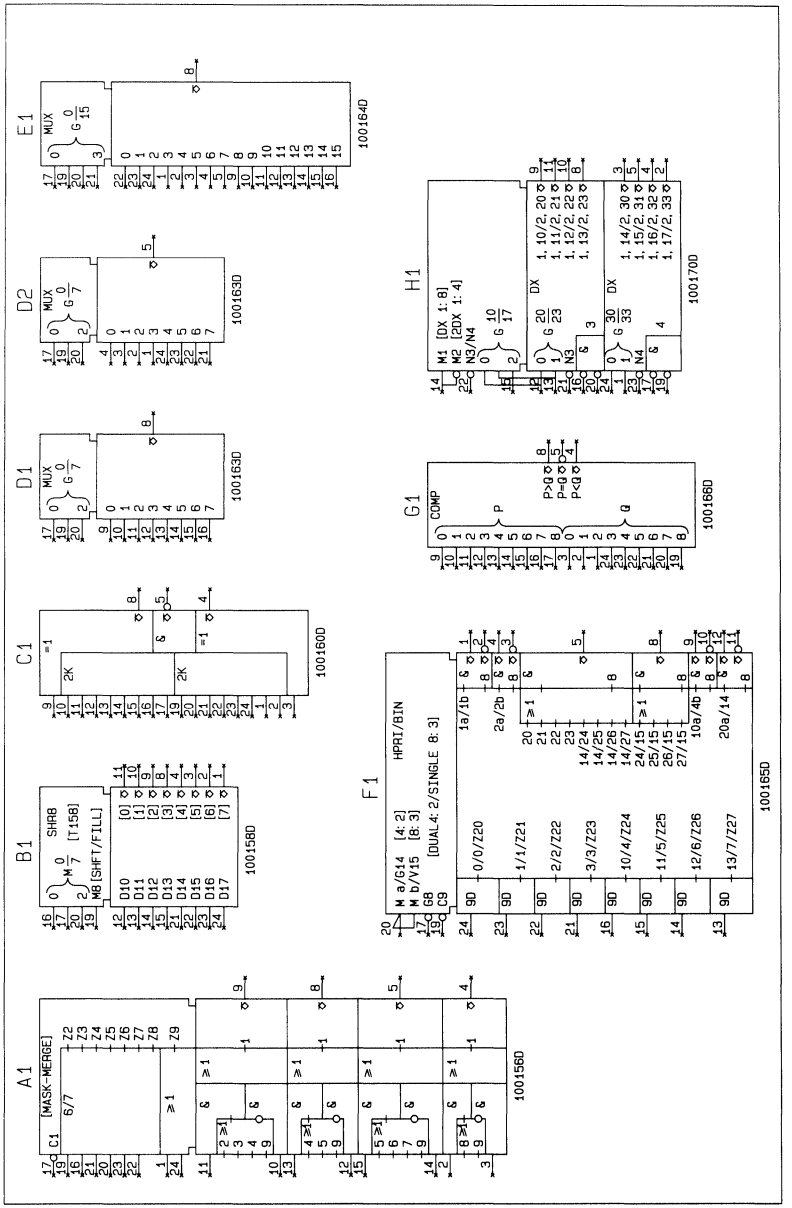
COMPONENT PLOTS

Plot 5A



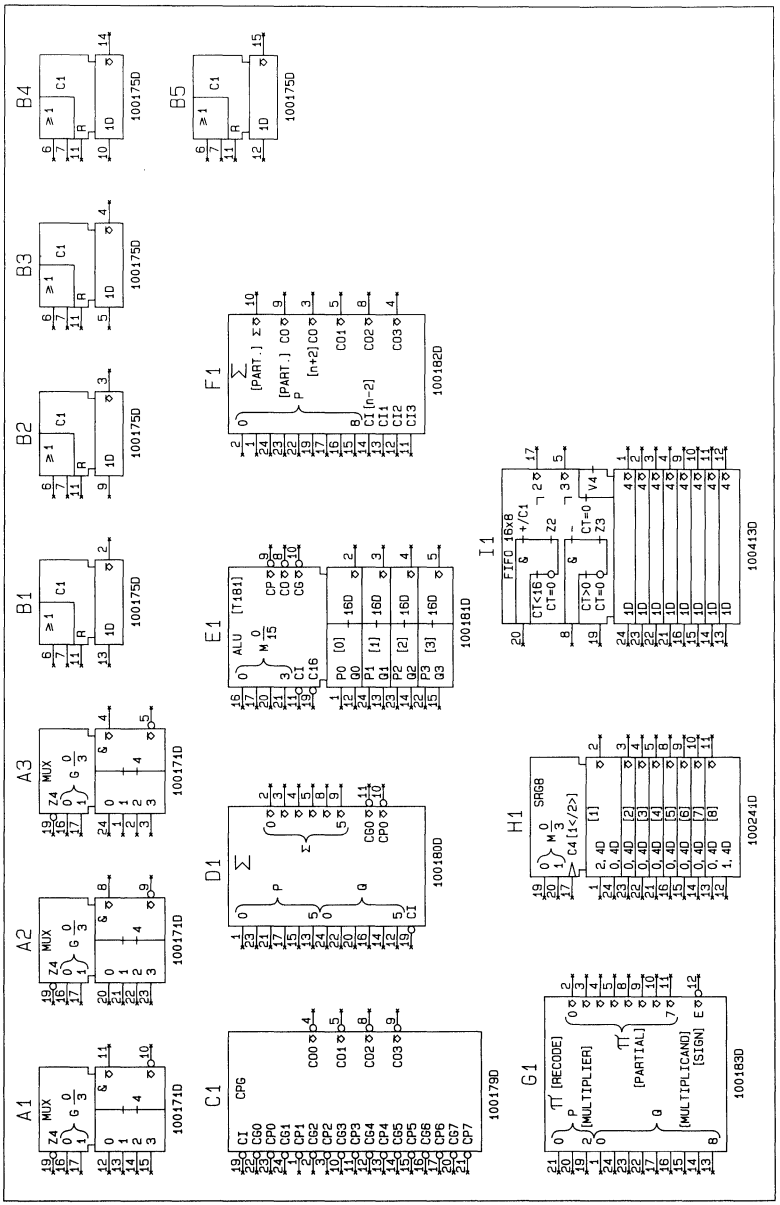
COMPONENT PLOTS

Plot 6A



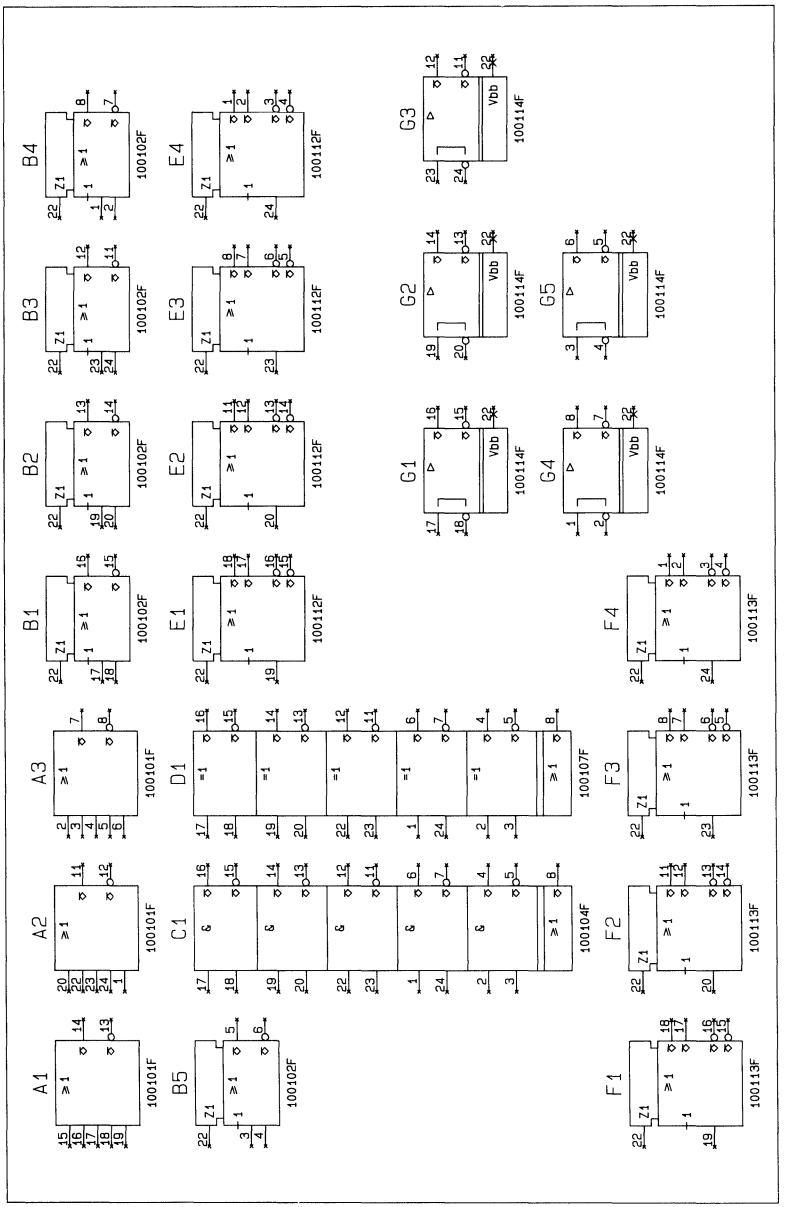
COMPONENT PLOTS

Plot 7A



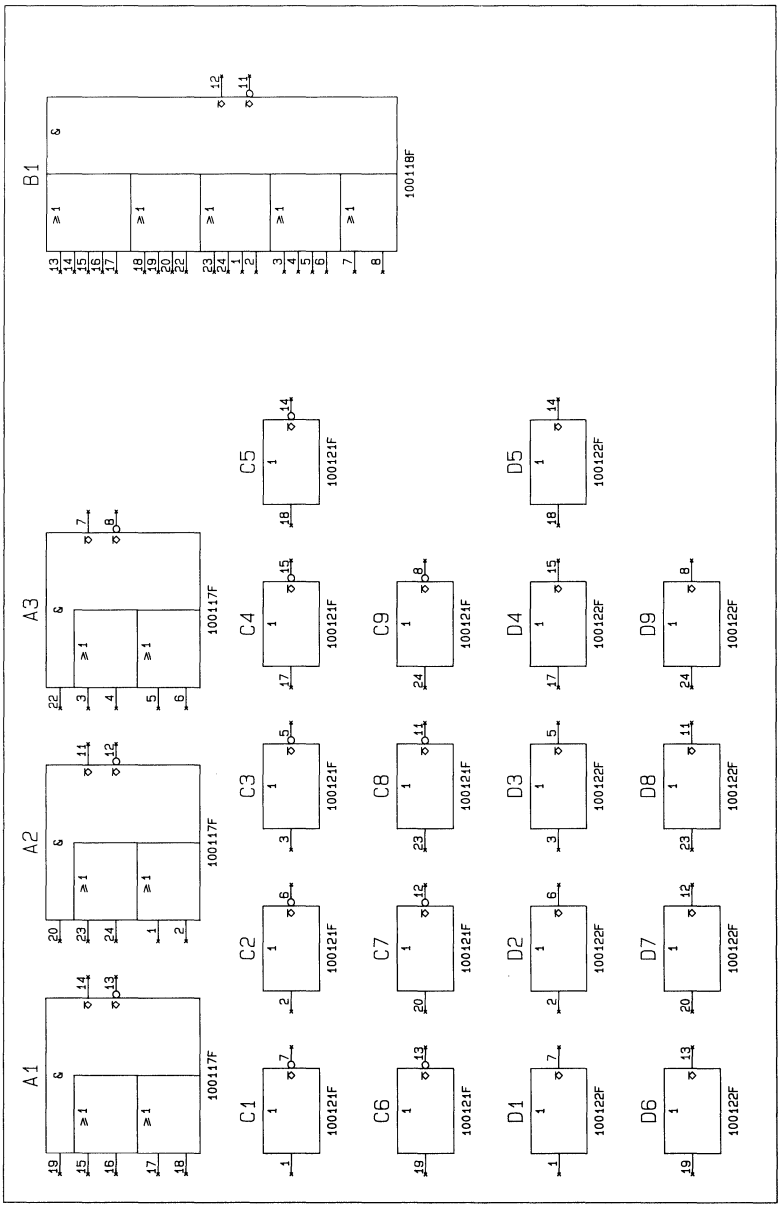
COMPONENT PLOTS

Plot 8A



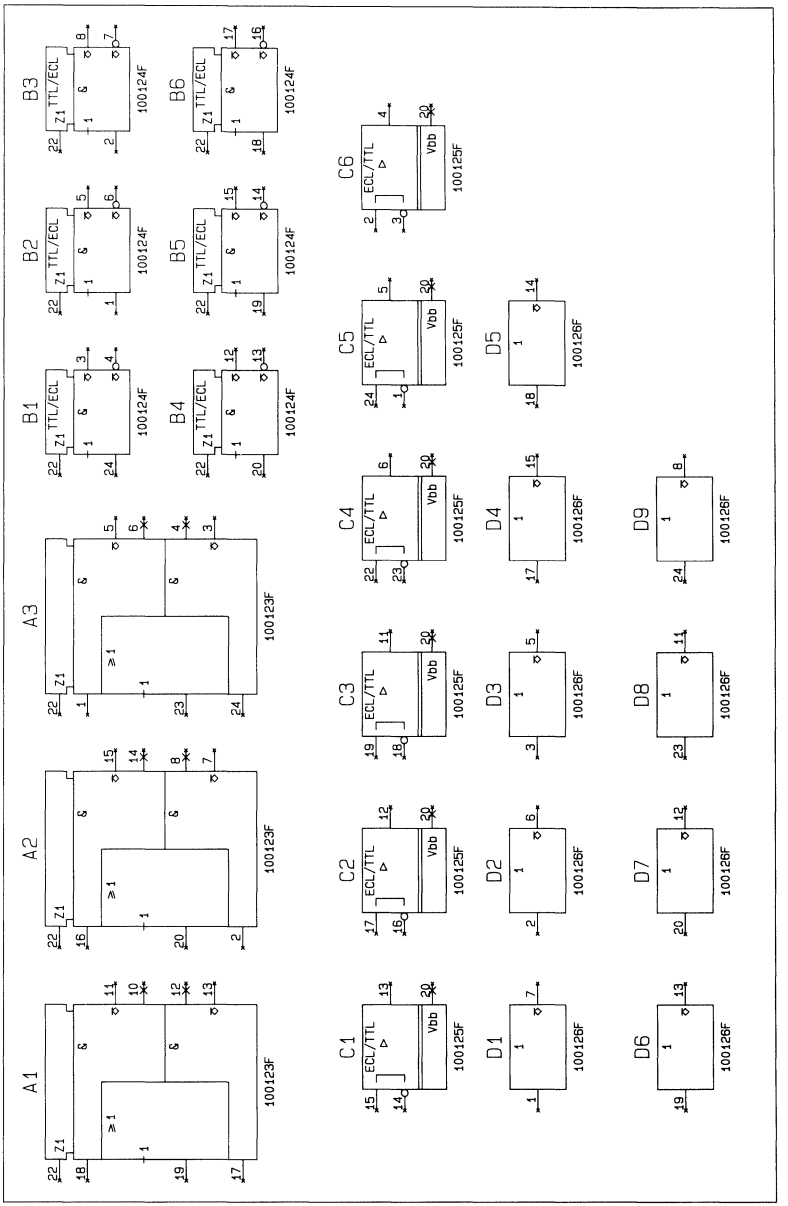
COMPONENT PLOTS

Plot 9A



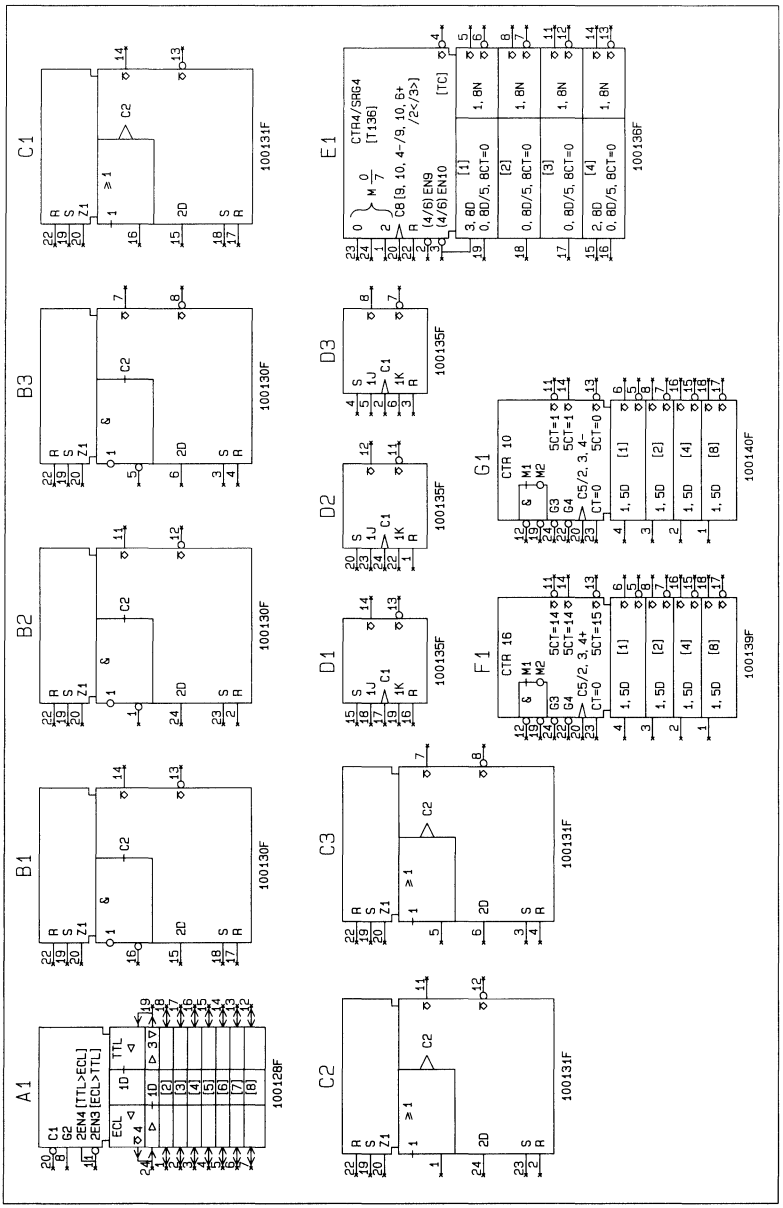
COMPONENT PLOTS

Plot 10A



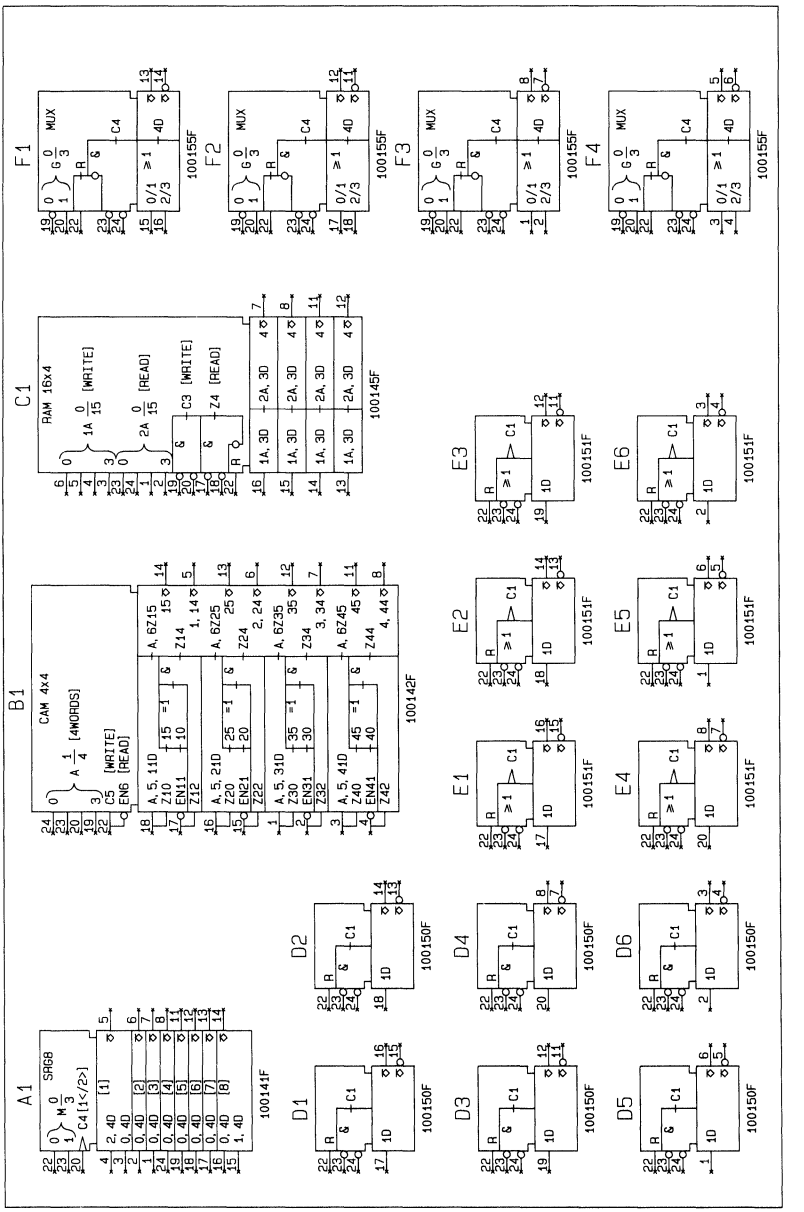
COMPONENT PLOTS

Plot 11A



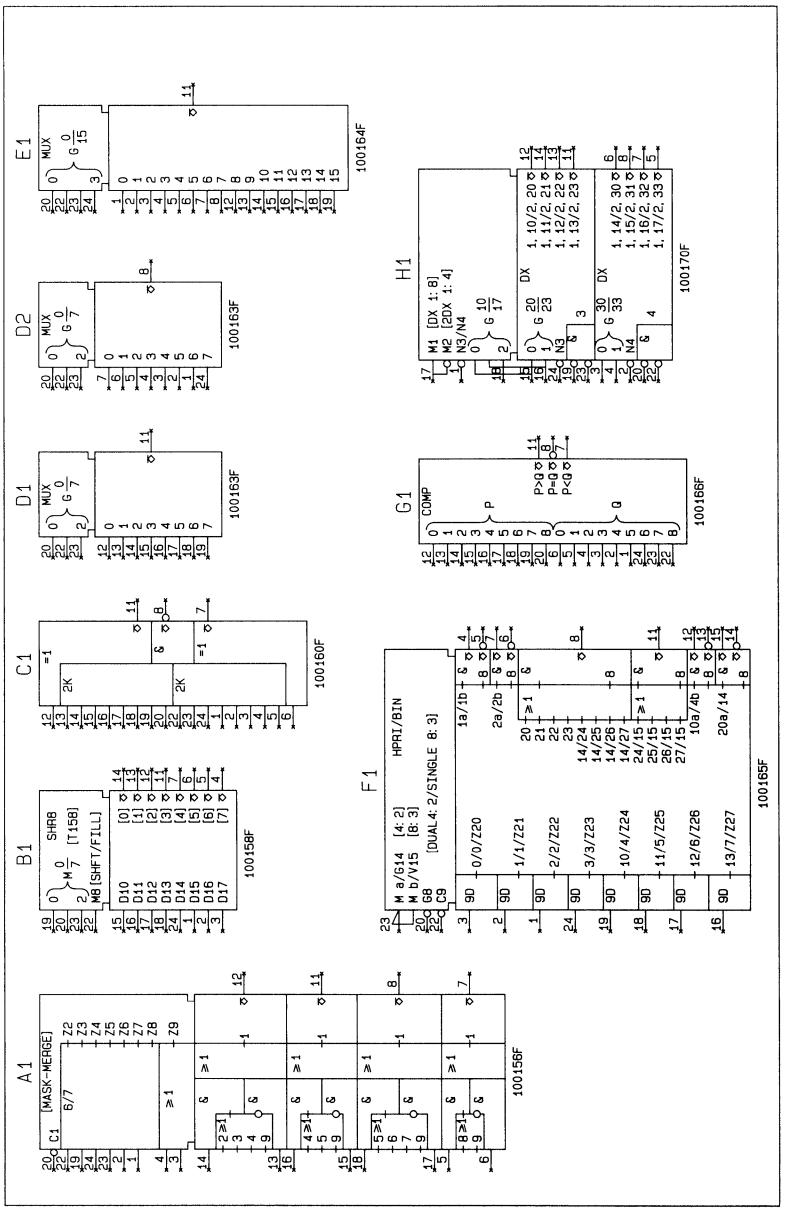
COMPONENT PLOTS

Plot 12A



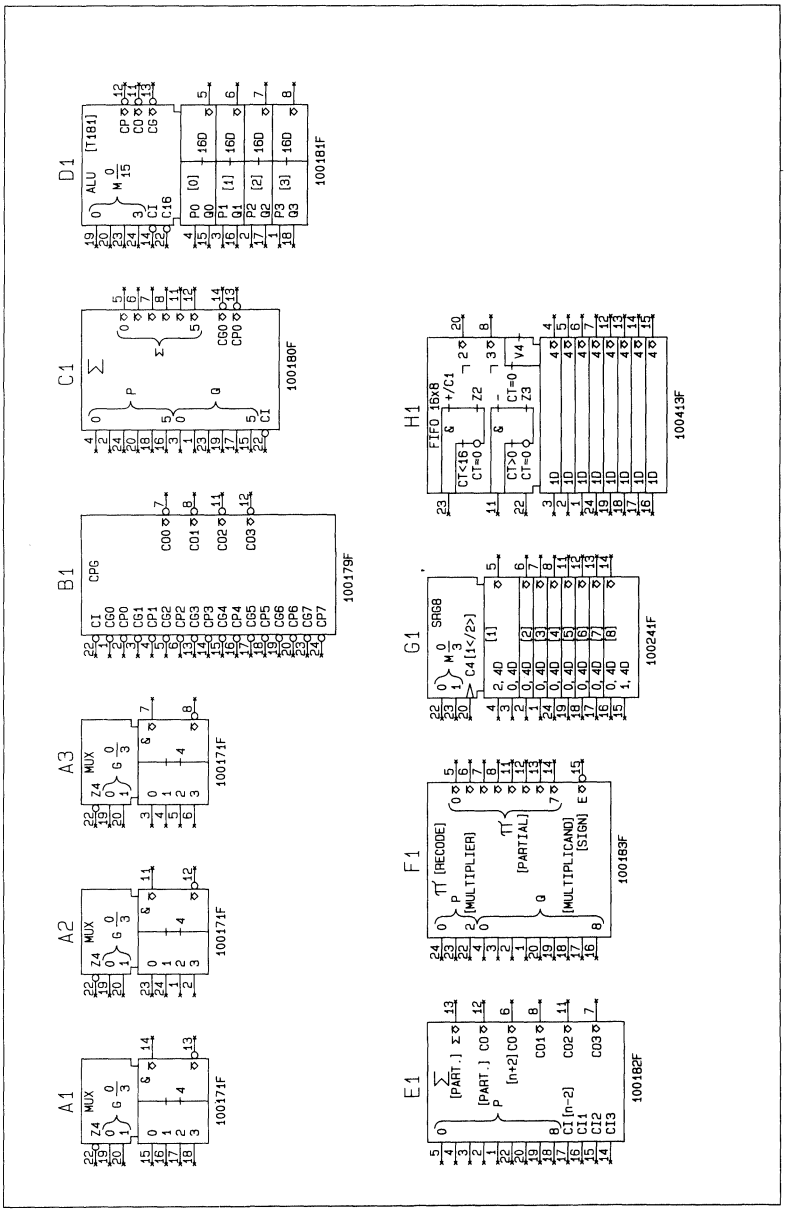
COMPONENT PLOTS

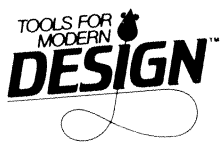
Plot 13A



COMPONENT PLOTS

Plot 14A

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