pb 250

Interface Manual

PBC 1005

pb Packard Bell Computer

A SUBSIDIARY OF PACKARD BELL ELECTRONICS
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PREFACE

The PB 250 Interface Manual is provided as a reference for the PB 250 Computer input, output information, electronic coupling data, timing and associated services.

This manual should be used in conjunction with the PB 250 Computer Reference Manual, Technical Manual Volume I, and Technical Manual Volume II.

CONTENTS

Contents (cont.)

Contents (cont.)

Contents (cont.)

FIGURES

TABLES

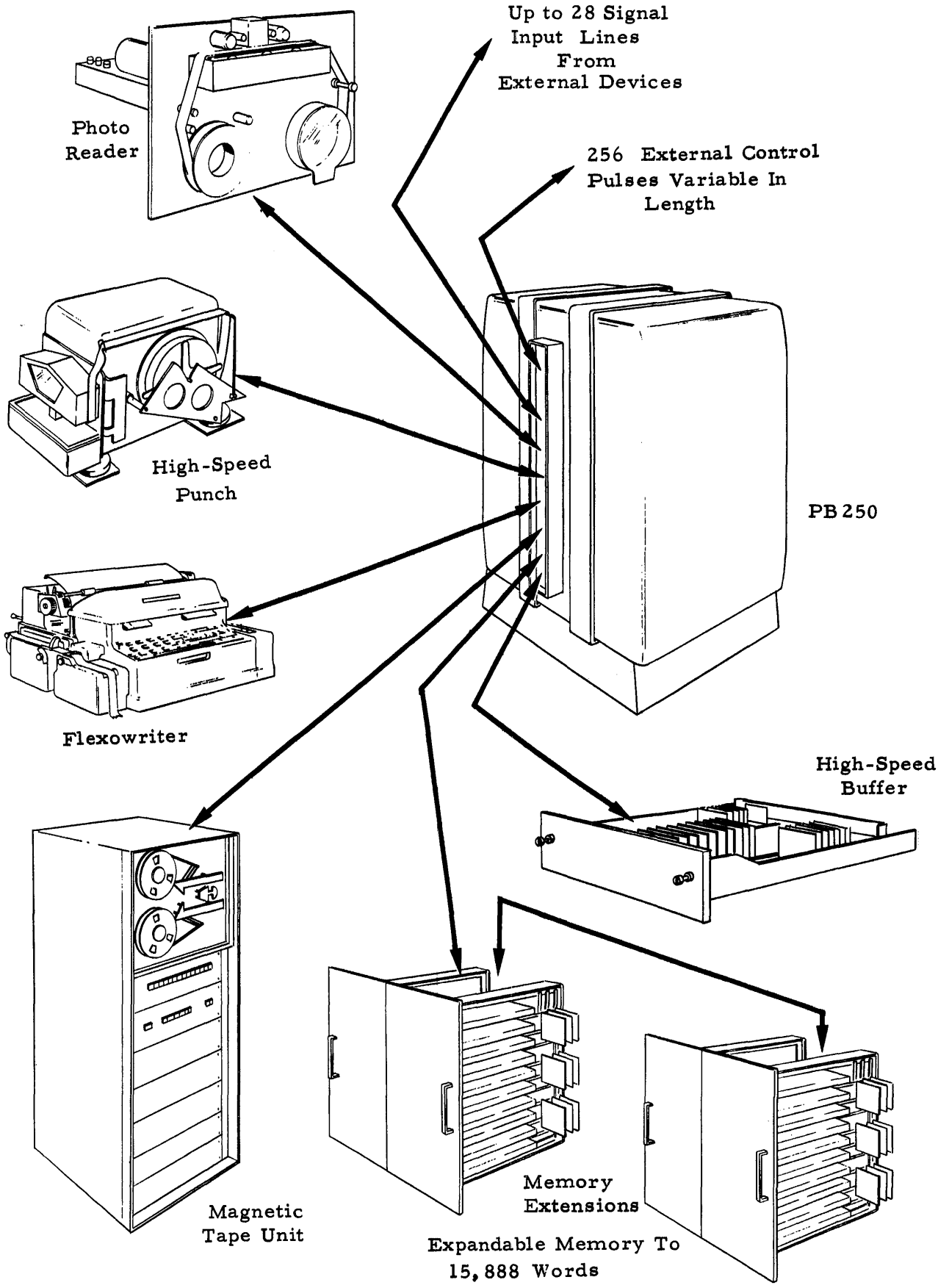


Figure 1-1. PB 250 Connection to Optional Input Equipment, Typical

I. PB 250 COMPUTER INPUT-OUTPUT SECTION

A. INTRODUCTION

The PB250 general purpose digital computer is designed with built-in versatility on input and output to function efficiently as a systems component. Typical installation of the PB 2 50 connected to optional input equipment is illustrated in Figure 1-1.

The computer is designed to communicate directly with such devices as magnetic tape units, high speed photo reader, Flexowriter, high speed punch and serial transistorized, high speed buffers. The buffers can be used to communicate with a large variety of devices, such as analog-to-digital converters, digital-to-analog converters, ac digital-to-analog converters, and core memories.

The computer has as standard equipment, ten signal input lines which can be used to control an internal program. Optionally, the number of signal input lines can be increased to 28.

To control other apparatus, the computer is capable of sending out 32 differently coded control pulses, each with a programmable length of 12 μsec to 3 msec in 12 μsec increments. These pulses are also used in the control of optional input and output devices.

For systems communication, the computer also sends out an eight level character output pulse with a programmable length of 12 μsec to 25 sec in 12 μsec increments.

Positions of the various input and output connectors on the back of the PB 250 Computer are shown in Figure 1-2. Table 1-1 indicates the functions of the input and output connectors.

Table 1-1

INPUT-OUTPUT CONNECTORS

Cannon Connector	Number	Mate Number	Function
J1	DC-37-P	DC-37-S	Flexowriter Input
J2	DA-15-S	DA-15-P	Character Output
J3	DA-15-S	DA-15-P	Character Output
J4	DB-25-S	DB-25-P	Flexowriter Output
J5	DA-15-P	DA-15-S	Computer Coupling to Other PB 250
J6	DA-15-P	DA-15-S	Spare
J7	DB-25-P	DB-25-S	Memory Extension
J8	DA-A11-CIP	DA-A11-CIS	Jump Control Inputs (Signal Input Lines)
J9	DA-A11-CIP	DA-A11-CIS	Jump Control Inputs (Signal Input Lines)
J10	DA-A11-CIP	DA-A11-CIS	Jump Control Inputs (Signal Input Lines)
J11	DA-A11-CIP	DA-A11-CIS	Jump Control Inputs (Signal Input Lines)
J12	DD-50-P	DD-50-S	For Bootstrap Control
J14	DC-37-S	DC-37-P	Photo Reader
J15	DA-15-P	DA-15-S	Control Pulse Out
J16	DA-15-P	DA-15-S	Control Pulse Out
J17	DE-9-P	DE-9-S	Serial Input and Output
J18	DC-37-S	DC-37-P	Magnetic Tape Input and Output
J19	DE-9-S	DE-9-P	Spare

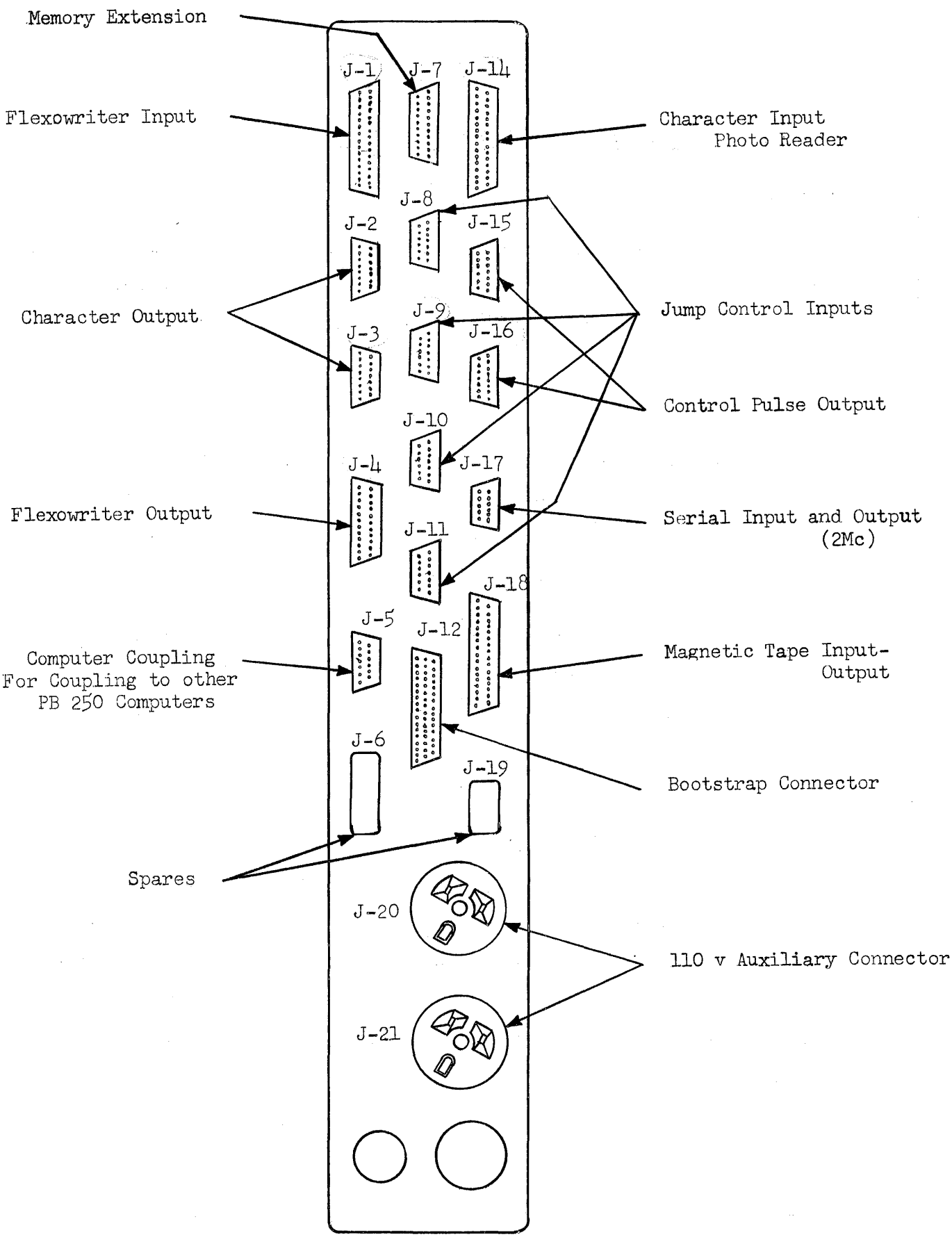


Figure 1-2. Input-Output Connector Panel

B. CHARACTER INPUT, PHOTO READER (J14)

1-1. INPUT SIGNAL

The character input section from the photo reader is designed to handle up to eight channels or levels of information. These channels are designated (S1) through (S8), and are gated by the sprocket signal so that all signals are identical in width and timing.

1-2. SPROCKET SIGNAL

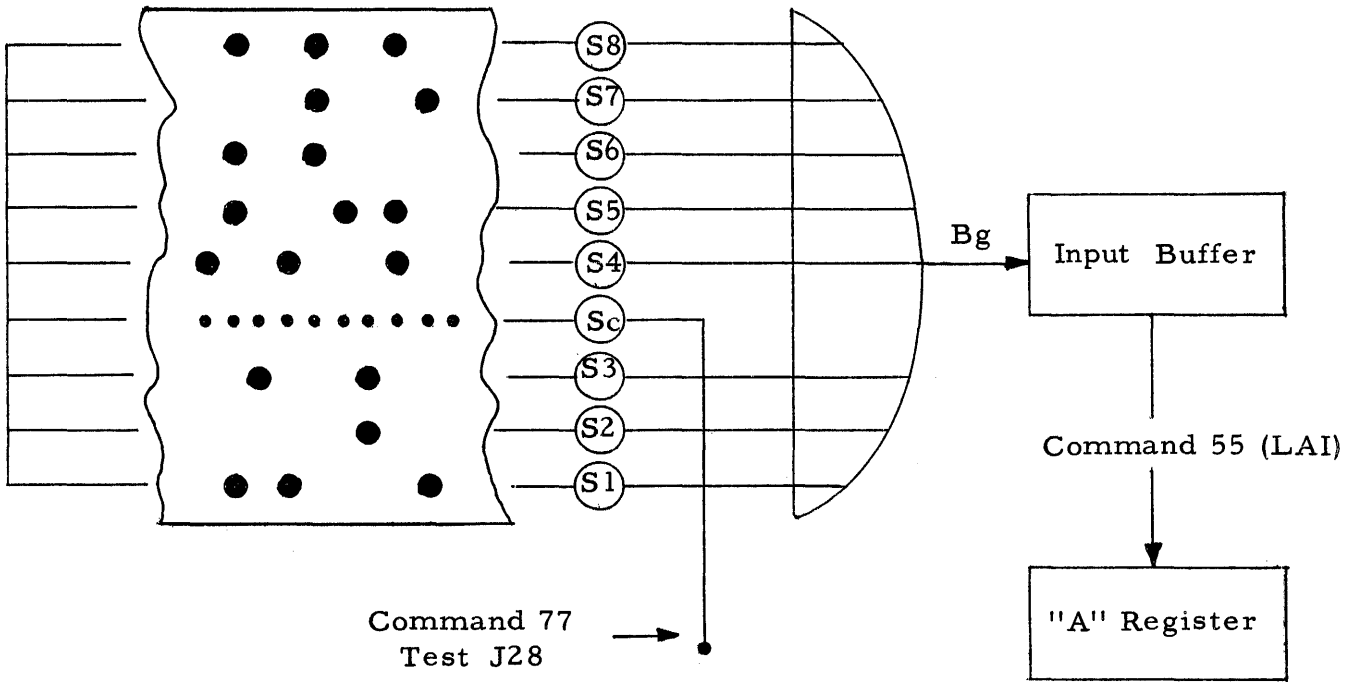
This signal is generated by the small sprocket holes in the perforated tape. The computer tests for the sprocket signal (Sc), as this indicates that the input buffer has received the information from the tape unit.

1-3. START AND STOP CONTROL

The photo reader is started and stopped by a PTU (Pulse to Specified Unit) command which must be decoded by the reader. The following are the operand flip-flop configurations which have been assigned for control of the high speed reader:

START	L5 L4 L3 $\overline{L2}$ $\overline{L1}$
STOP	L5 L4 L3 $\overline{L2}$ L1

Only the true sides of the flip-flops are made available for decoding. If more than one high speed reader is to be controlled, the command flip-flops K1, K2, and K3 can be decoded. However, this causes minor restrictions in programming, see Figure 1-3. When decoded, these signals must be "AND gated" with Cpg which is the activation pulse generated during the execution of command 70.



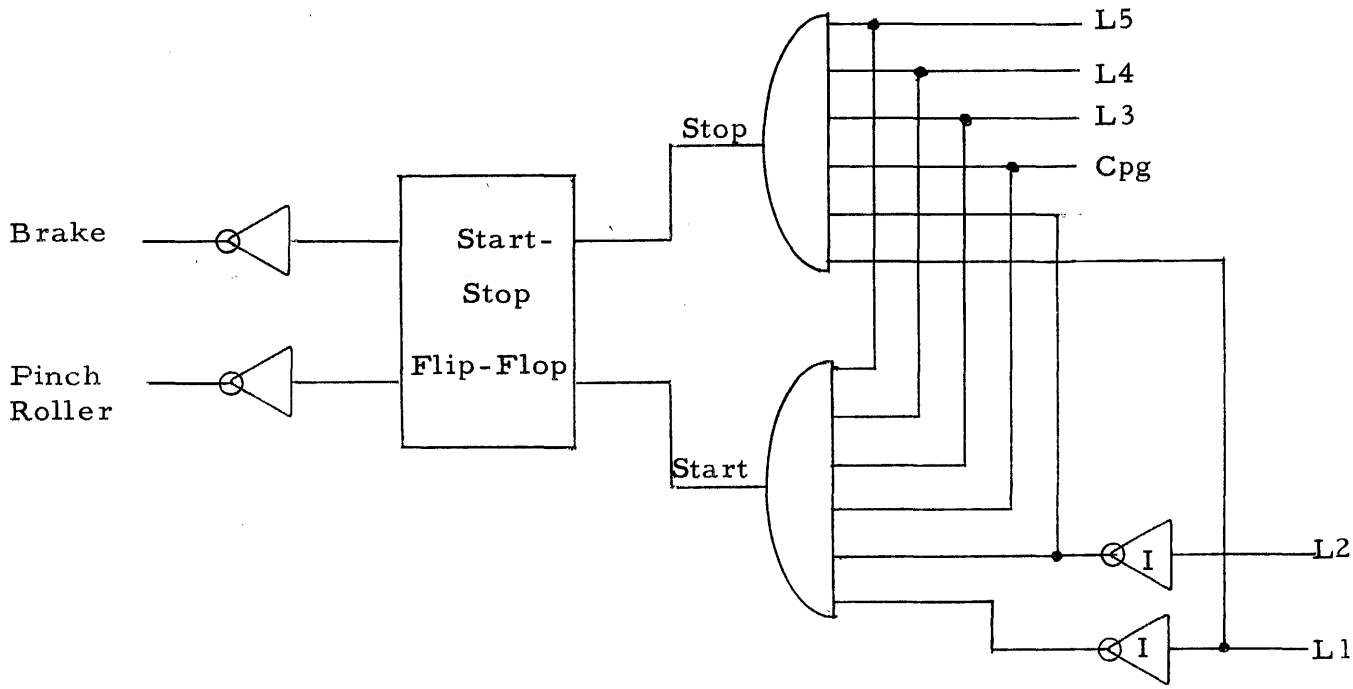


Figure 1-3. Photo Reader Input Control

1-4. POWER

Power is supplied from the reader power supply to drive the coupling logic.

C. CHARACTER INPUT, MAGNETIC TAPE READER (J18)

1-5. INPUT SIGNAL

The character input section from the magnetic tape units is designed to handle up to eight levels or channels, the MTU-1 and MTU-2 utilize seven of these levels; six channels of information and a seventh channel which is used for odd lateral parity checks. With proper coupling logic and circuitry, up to six magnetic tape units can operate in conjunction with the PB 250 Computer.

1-6. CLOCK SIGNAL

The clock signal is generated in the magnetic tape unit by OR gating the six channels of information and the parity bit. The computer uses the detection of the arrival of the clock signal to indicate that information has been read into the input buffer.

1-7. START AND STOP CONTROL

The magnetic tape units, see Figure 1-4, are controlled by a series of PTU (Pulse to Specified Unit) commands. The information contained in these commands must be decoded externally as described in paragraph 1-3. The outputs of the three command flip-flops are available for additional control versatility; however, this requires additional decoding and limits the programming. Required configurations of the operand section for control of the maximum of six magnetic tape units are as follows:

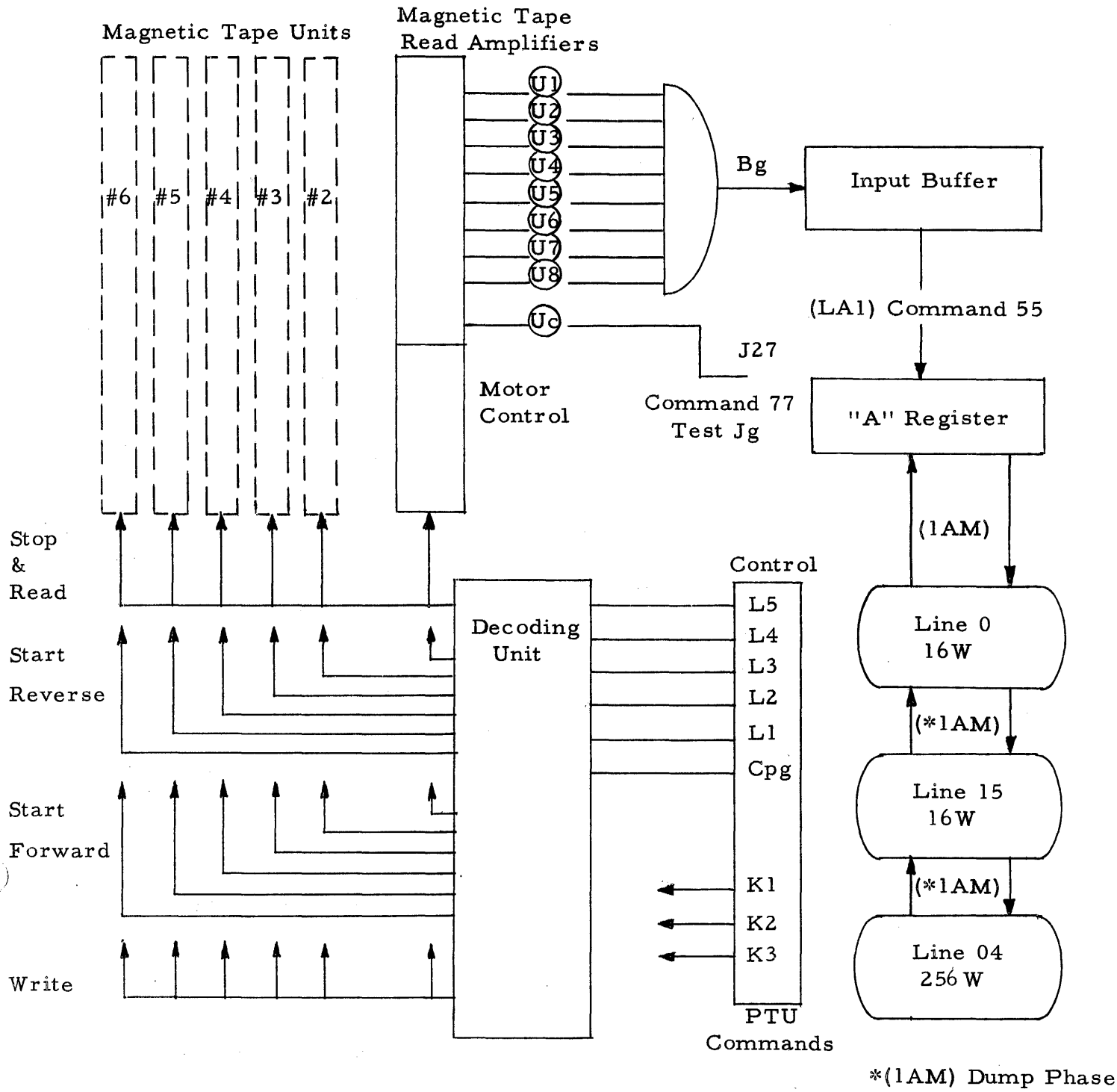


Figure 1-4. Reading Magnetic Tape

$\overline{L5}$ L4 $\overline{L3}$ $\overline{L2}$ L1	Unit 1	Start reverse
$\overline{L5}$ L4 $\overline{L3}$ L2 $\overline{L1}$	Unit 2	Start reverse
$\overline{L5}$ L4 $\overline{L3}$ L2 L1	Unit 3	Start reverse
$\overline{L5}$ L4 L3 $\overline{L2}$ $\overline{L1}$	Unit 4	Start reverse
$\overline{L5}$ L4 L3 $\overline{L2}$ L1	Unit 5	Start reverse
$\overline{L5}$ L4 L3 L2 $\overline{L1}$	Unit 6	Start reverse
$\overline{L5}$ L4 L3 L2 L1	All Units	Stop and read set
$\overline{L5}$ $\overline{L4}$ $\overline{L3}$ $\overline{L2}$ $\overline{L1}$	All Units	Write set
L5 $\overline{L4}$ $\overline{L3}$ $\overline{L2}$ L1	Unit 1	Start forward
L5 $\overline{L4}$ $\overline{L3}$ L2 $\overline{L1}$	Unit 2	Start forward
L5 $\overline{L4}$ $\overline{L3}$ L2 L1	Unit 3	Start forward
L5 $\overline{L4}$ L3 $\overline{L2}$ $\overline{L1}$	Unit 4	Start forward
L5 $\overline{L4}$ L3 $\overline{L2}$ L1	Unit 5	Start forward
L5 $\overline{L4}$ L3 L2 $\overline{L1}$	Unit 6	Start forward

These signals must be "AND gated" with Cpg which is the activation signal for the PTU command.

1-8. POWER

Power is supplied from the magnetic tape unit power supply to drive the coupling logic.

D. CHARACTER OUTPUT (J2) (J3)

The character output is used to send information to devices such as: card punch, magnetic tape, high speed punch and line printer, by use of the WOC (Write Output Character) command, see Figure 1-5.

1-9. DESTINATION

The command flip-flops determine which external device is to receive the output character. The decoding of the command flip-flops is effected

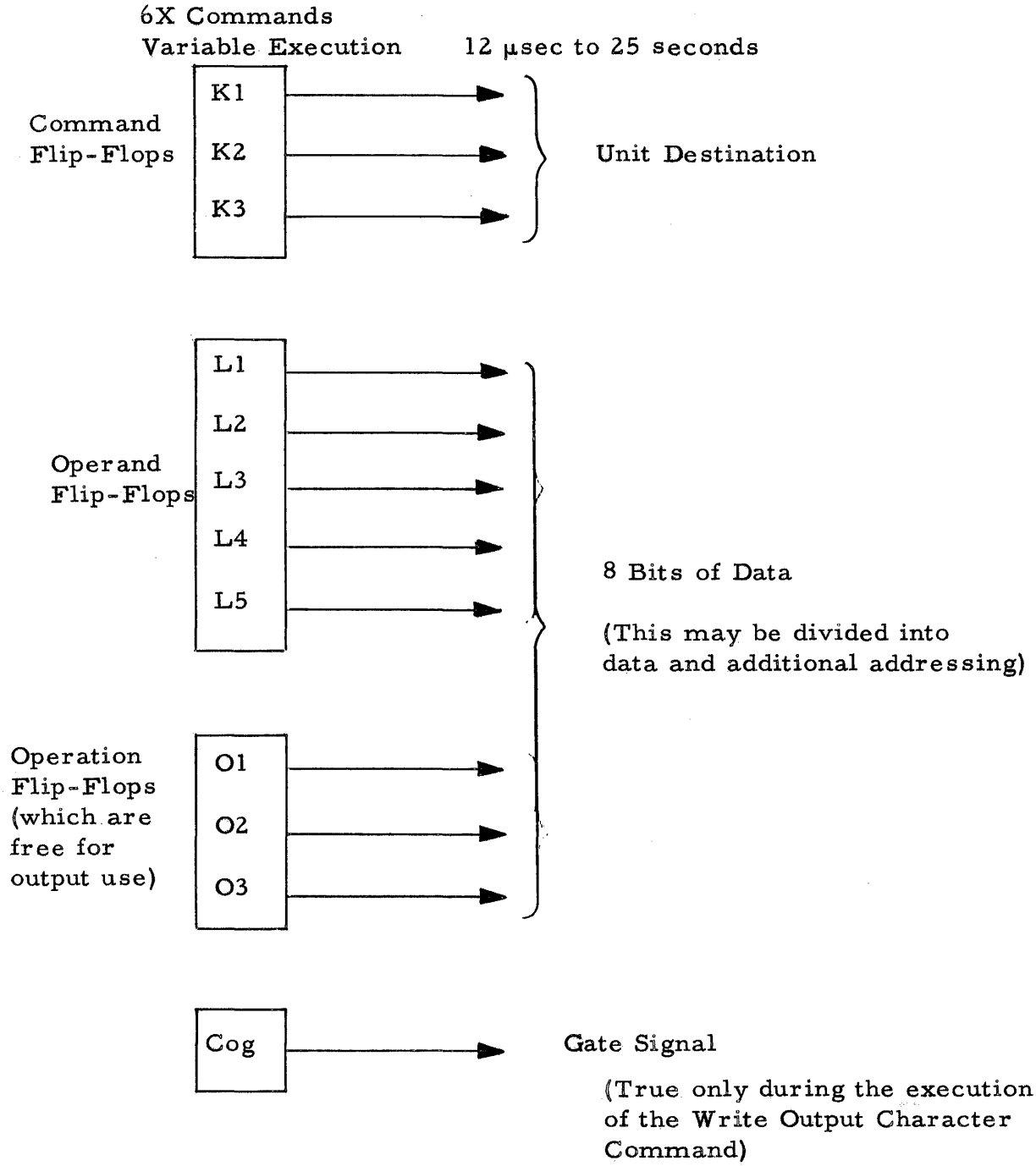


Figure 1-5. Write Output Character

externally. Part of the output code can be combined with the destination code to control a larger number of output devices. The destination codes which have been assigned to various output and control devices, are as follows:

Line 0	$\overline{K3}\ \overline{K2}\ \overline{K1}$	Magnetic tape line 00 High speed punch line 00
Line 1	$\overline{K3}\ \overline{K2}\ K1$	Card punch
Line 2	$\overline{K3}\ K2\ \overline{K1}$	Multiplexer
Line 5	$K3\ \overline{K2}\ K1$	Typewriter
Line 6	$K3\ K2\ \overline{K1}$	Flexowriter punch
Line 7	$K3\ K2\ K1$	Line printer

1-10. OUTPUT CODE

The output code consists of up to eight bits using the operand register and the first three (lower order) flip-flops of the operation register.

1-11. EXECUTE SIGNAL

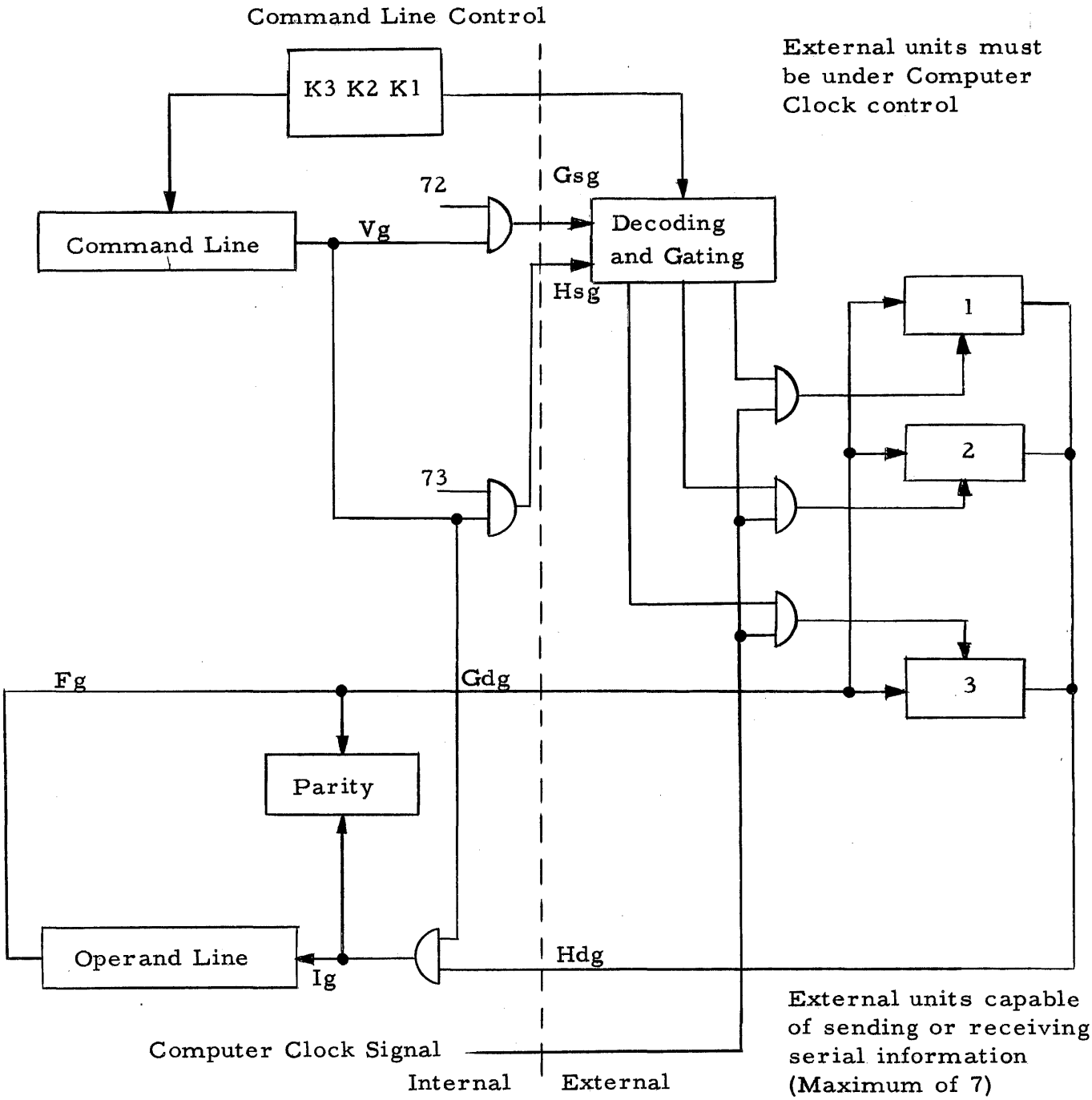
The execute signal is designated Cog. The length of execution of the WOC command is variable from 12 μsec to 25 seconds. This signal must be "AND gated" with the output code signals.

1-12. POWER

Power is supplied from the computer power supply to drive the external coupling and decoding logic only in those cases where it is not available at the auxiliary unit.

E. SERIAL INPUT-OUTPUT (J17)

The serial input and output section, see Figure 1-6, is used to transfer information to and from the computer at an 85 kc word rate or 2 megacycle clock rate. This serial information does not pass through any buffering



Ig = Information Gate
Fg = Fetch Gate
Vg = Command Gate

Figure 1-6. Serial Input and Output

equipment but operates directly with memory. It is used in conjunction with other systems, buffer registers and certain types of additional storage.

1-13. SOURCE CODE

The command flip-flops K1, K2, and K3, can be decoded as the input or output unit source code. The operand portion of the instruction will designate which line is to receive the information or which line is to output the information. Input and output are under the control of a mask which must be in the command line.

1-14. INPUT SHIFT SIGNAL

The input shift signal (designated Hsg) is generated from the data contained in the command line between the sector in which the command was read and the sector designated by the MS number of the command. The preceding data, (designated Vg) is further qualified by the execution phase of the BSI command to form Hsg. Hsg is then gated with the computer clock, outside the computer, to form the shift signals, which shift the data from the external device into the computer. When there are zero bits in Hsg, zeros will be shifted into the memory line. A parity adjustment is made on the incoming information as it is stored in the designated memory line.

1-15. INPUT DATA SIGNAL

The input signal (designated Hdg) is the serial output signal of the external device which is sending information to the PB 250 Computer.

1-16. CLOCK SIGNAL

This is the two megacycle computer clock signal which should be gated with the input and output shift signals.

1-17. OUTPUT SHIFT SIGNAL

The output shift signal (designated Gsg) is generated from the data contained in the command line between the sector in which the command was read and the sector designated by the MS number of the command. The preceding data (designated Vg) is further qualified by the execution phase of the BSO command to form Gsg. Gsg is then gated with the computer clock, outside the computer, to form the shift signals which shift the serial data from the computer into the external device. When there are zeros in Gsg, the information coming from the computer is not shifted into the external device.

1-18. OUTPUT DATA SIGNAL

The output signal (designated Gdg) is directly generated by the fetch gate (Fg) and will include the parity and guard bits. These two bits are excluded by the mask in the command line.

F. MEMORY ACCESSORY

The memory accessory connector, see Figure 1-7, is used for expanding the memory beyond the 16-line internal capacity. Coupling is effected directly with the external addressing and access system in the same way as the coupling of the internal storage.

1-19. SELECTOR SIGNALS

The selector signals are the series of addressing signals (Mog, Nog, etc) which are internally decoded from the operand select register (L1, L2, L3, L4, and L5) and are used to address the reading of information from a storage line or to address the storing of information into a particular storage line. The selector signals must be gated externally for the addressing of

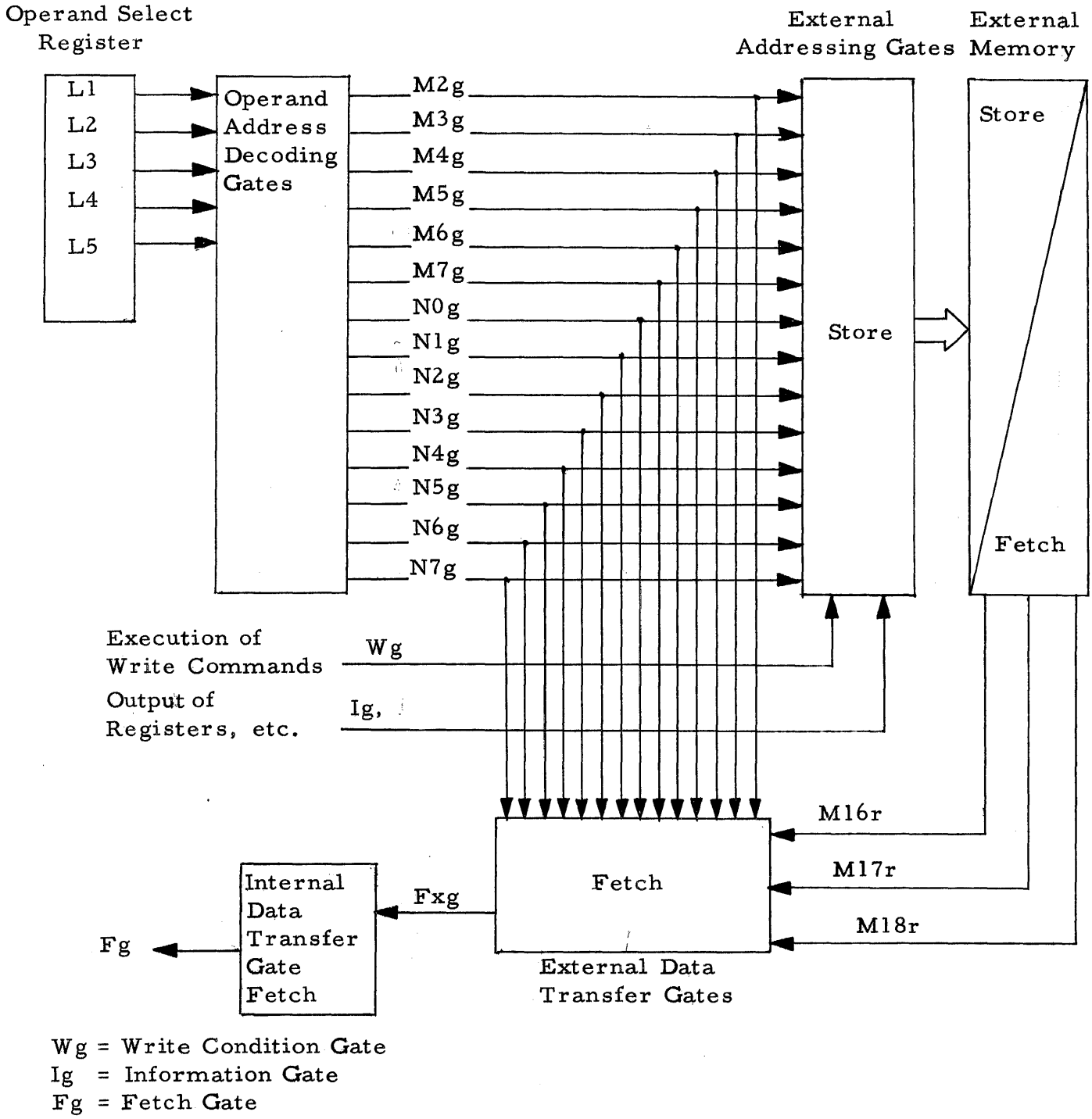
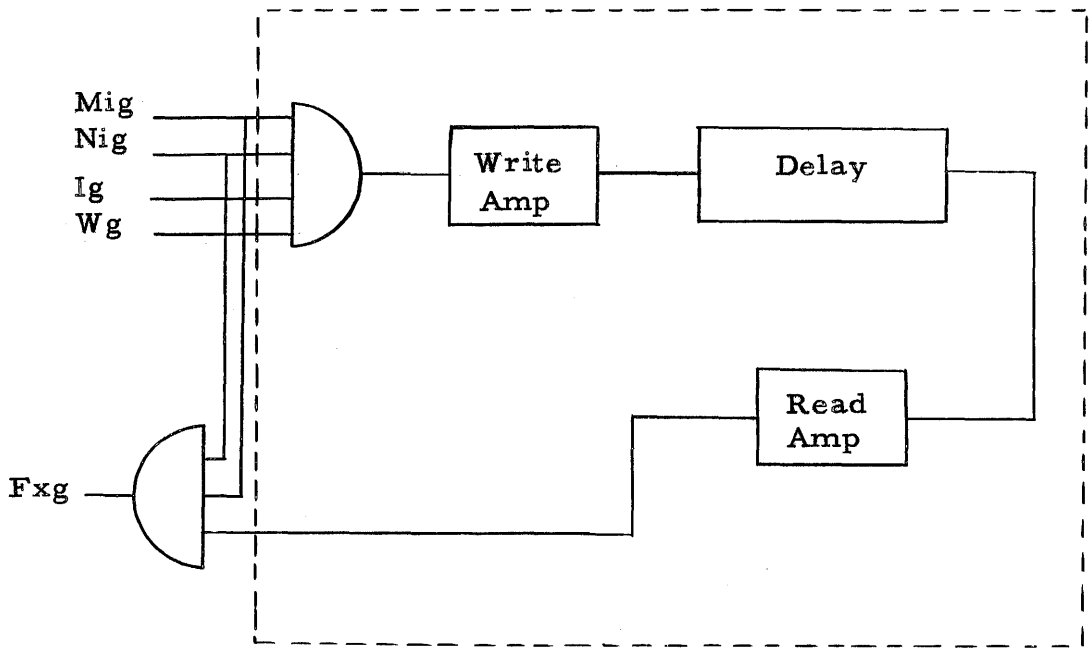


Figure 1-7. Memory Accessory

memory lines. This is normally performed on the memory modules.

1-20. WRITE GATE

The "write gate" signal (designated Wg) is true for the execution phase of all commands which store information. This signal is gated with the selector signals and the data information.



1-21. INFORMATION GATE

The "information gate" signal (designated Ig) is generated from the command line and the arithmetic registers. This signal is gated with the selector signal and the write condition signal.

1-22. FETCH GATE

The "fetch gate" signal, (designated Fxg, External Fetch Signal) is generated by the external gating of the addressing signals and the read flip-flops of the external memory lines, see Figure 1-7. The external fetch or

read data signal is internally "OR gated" with the internal fetch signals to become Fg.

1-23. CLOCK SIGNALS

Both memory clock and computer clock signals are generated in the external memory from a 2 megacycle sine wave generated in the PB 250.

1-24. POWER

Power is supplied from the computer power supply to drive the required circuitry and logic for external memory.

G. JUMP CONTROL INPUTS (J8, J9, J10, J11) (SIGNAL INPUT LINE)

The jump control inputs, see Figure 1-8, are the means by which the computer may examine external conditions and act accordingly. The external conditions must be presented as "true" or "false" logic levels on one of a maximum of 28 input lines. The computer, during the execution of command 77, will test one of these jump control lines, selected by the addressing of the operand register. If this line is true, the computer will read the next command from the address specified by the MS number; otherwise it will read the next command in sequence. Jump control lines 18 through 28 are supplied with the basic computer.

1-25. CONNECTOR NO. 1 (J8)

Input lines 0 through 7 (optional).

1-26. CONNECTOR NO. 2 (J9)

Input lines 8 through 15 (optional).

1-27. CONNECTOR NO. 3 (J10)

Input lines 15 through 17 (optional).

Input lines 18 through 23 (standard).

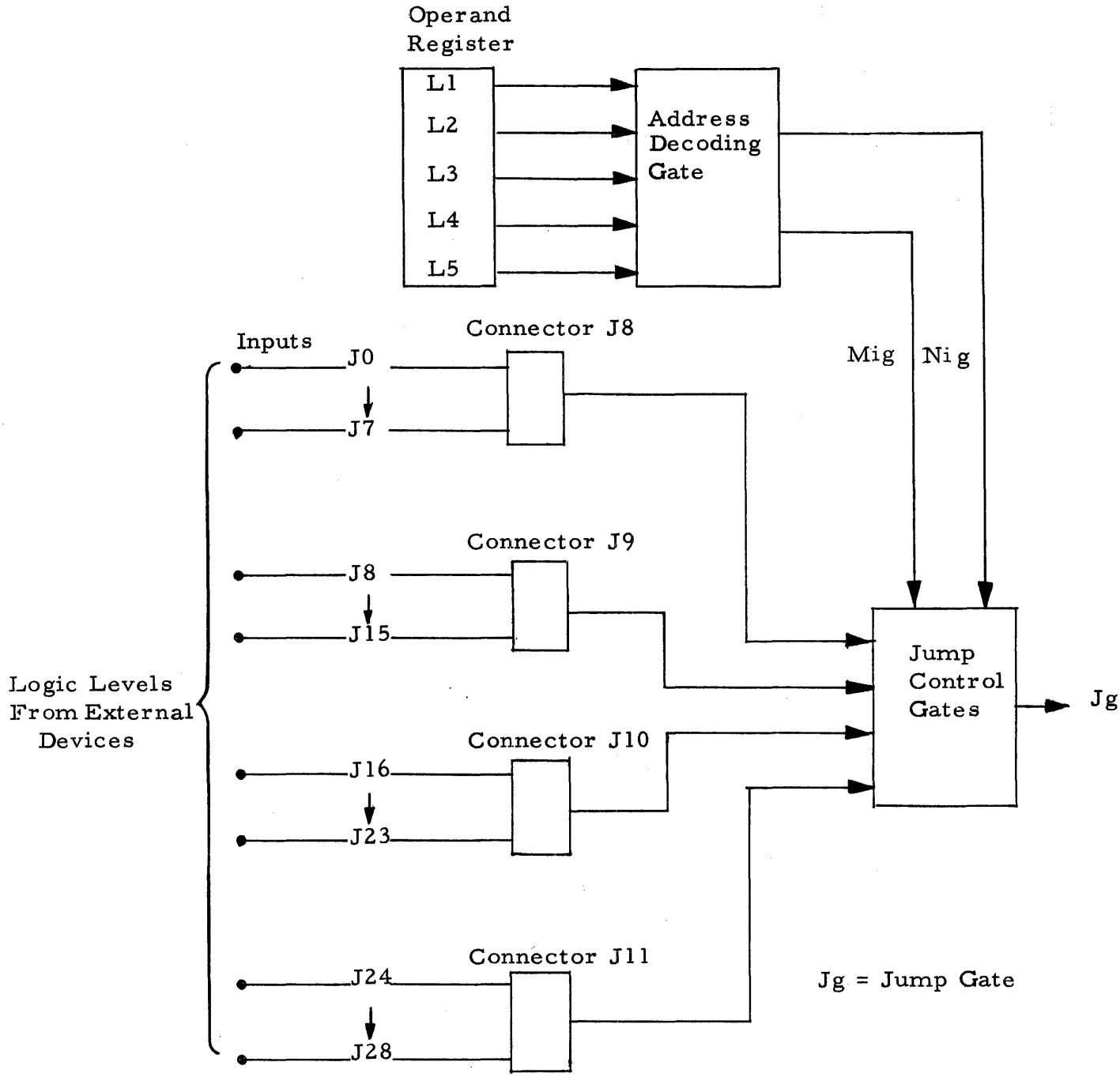


Figure 1-8. Jump Control Inputs (Signal Input Lines)

1-28. CONNECTOR NO. 4 (J11)

Input lines 24 through 28 (standard).

H. BOOTSTRAP INPUT (J12)

This connector serves as a patchboard for programming the bootstrap input, see Figures 1-9, 1-10, 1-11, and 1-12. The PB 250 Computer will accept information through the bootstrap mechanism from the mechanical reader, photo reader, and magnetic tape unit. The applicable bootstrap connections are given in Table 1-2.

1-29. INPUT CHARACTERS

The input characters designated (B6) (B5) (B4) (B1) are internal signals which must be connected to proper external signals by means of the bootstrap connector.

1-30. MECHANICAL READER CONTROL LEVELS

The control levels (Mr) and ($\overline{\text{Mr}}$) are used to designate whether or not the mechanical reader is being used for bootstrap. When the mechanical reader is being used (Mr) should be connected to -12v and ($\overline{\text{Mr}}$) to ground. These connections should be reversed when the mechanical reader is not being used.

1-31. BOOTSTRAP START, BOOTSTRAP STOP

These are internal signals associated with the parity flip-flop. They must be connected through the bootstrap connector to the appropriate external Stop and Start signals.

1-32. POWER

Power is supplied from the computer power supply for the required logic signals.

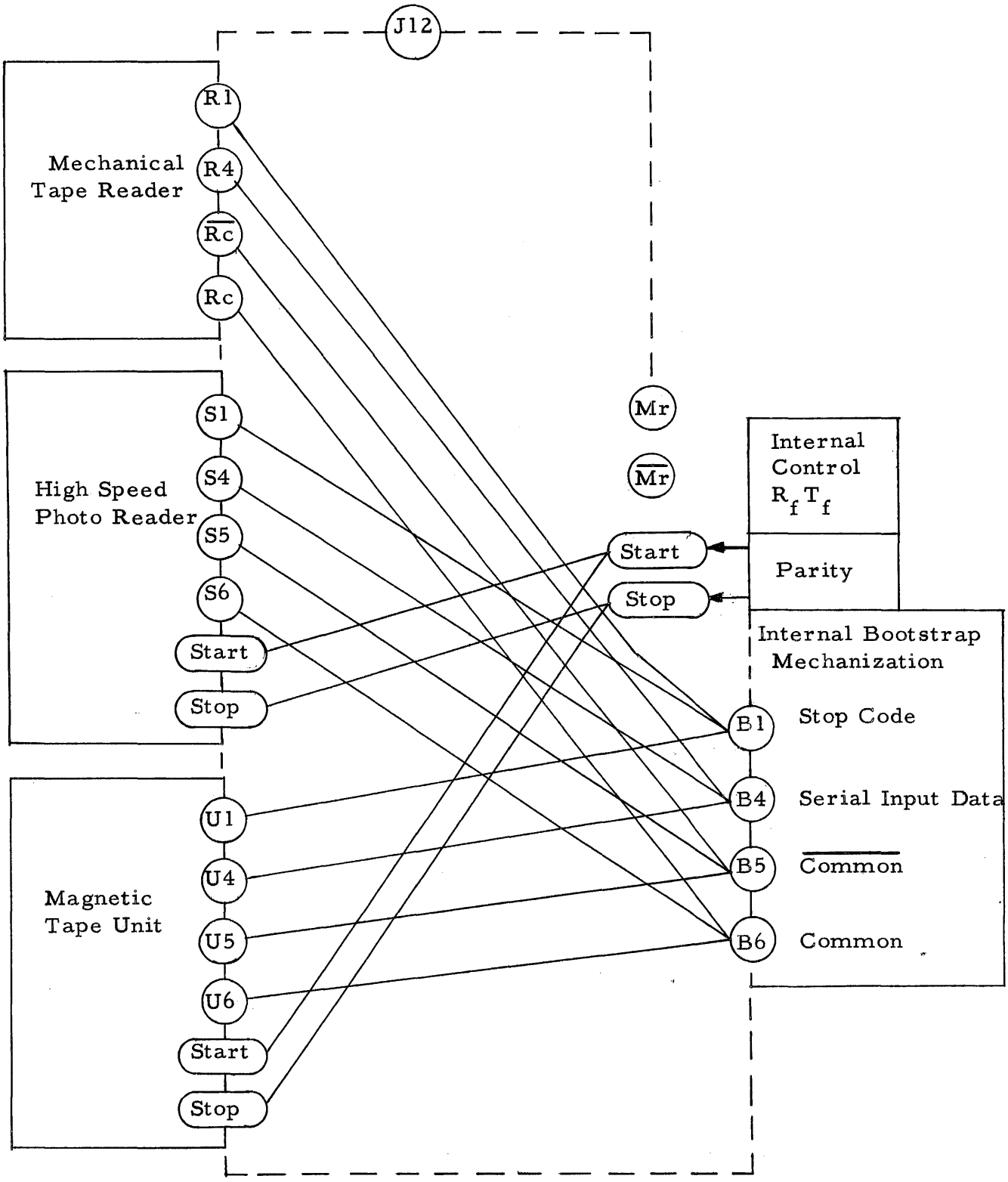


Figure 1-9. Bootstrap Input Connector

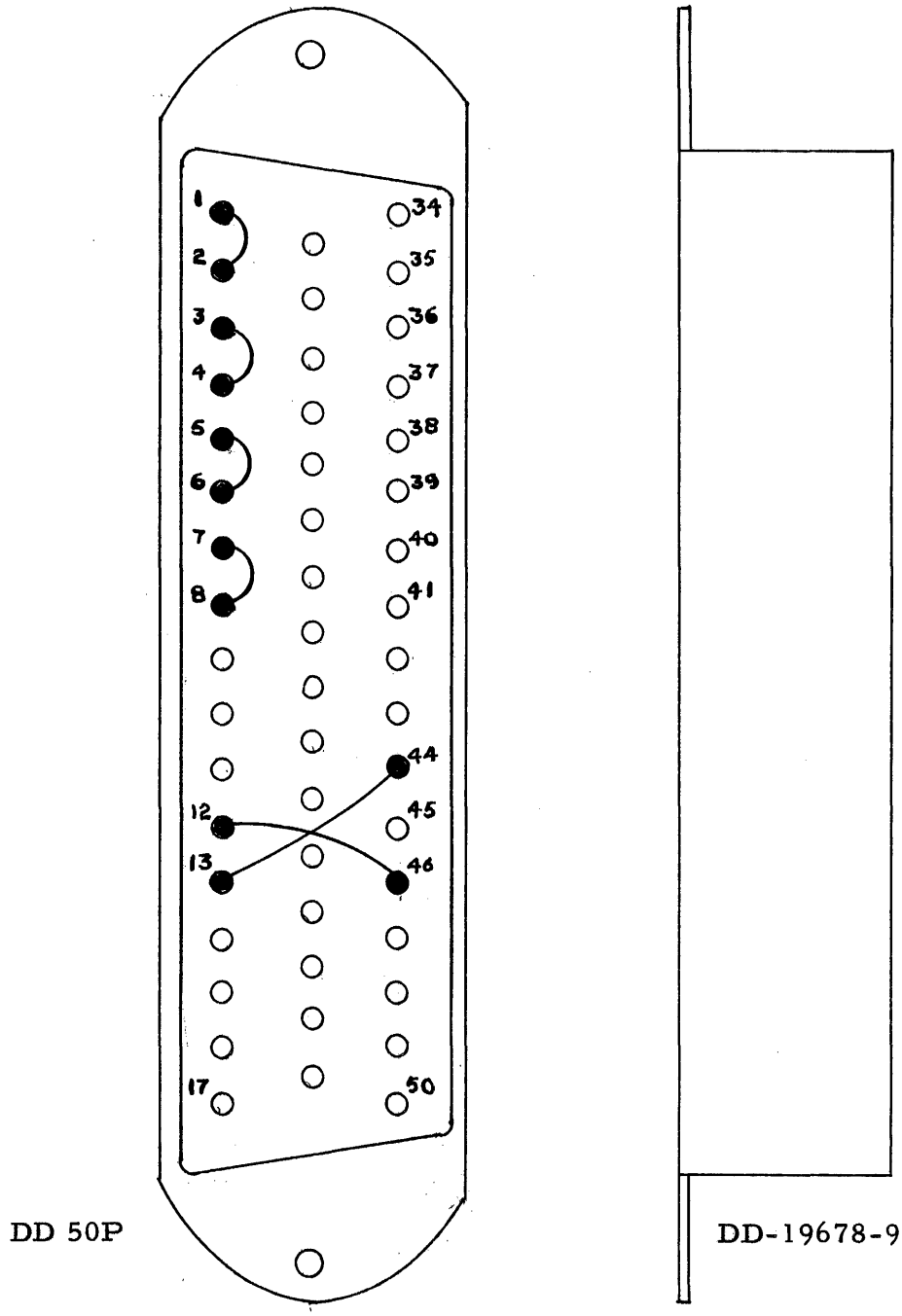


Figure 1-10. Bootstrap Input Connections for Flexowriter

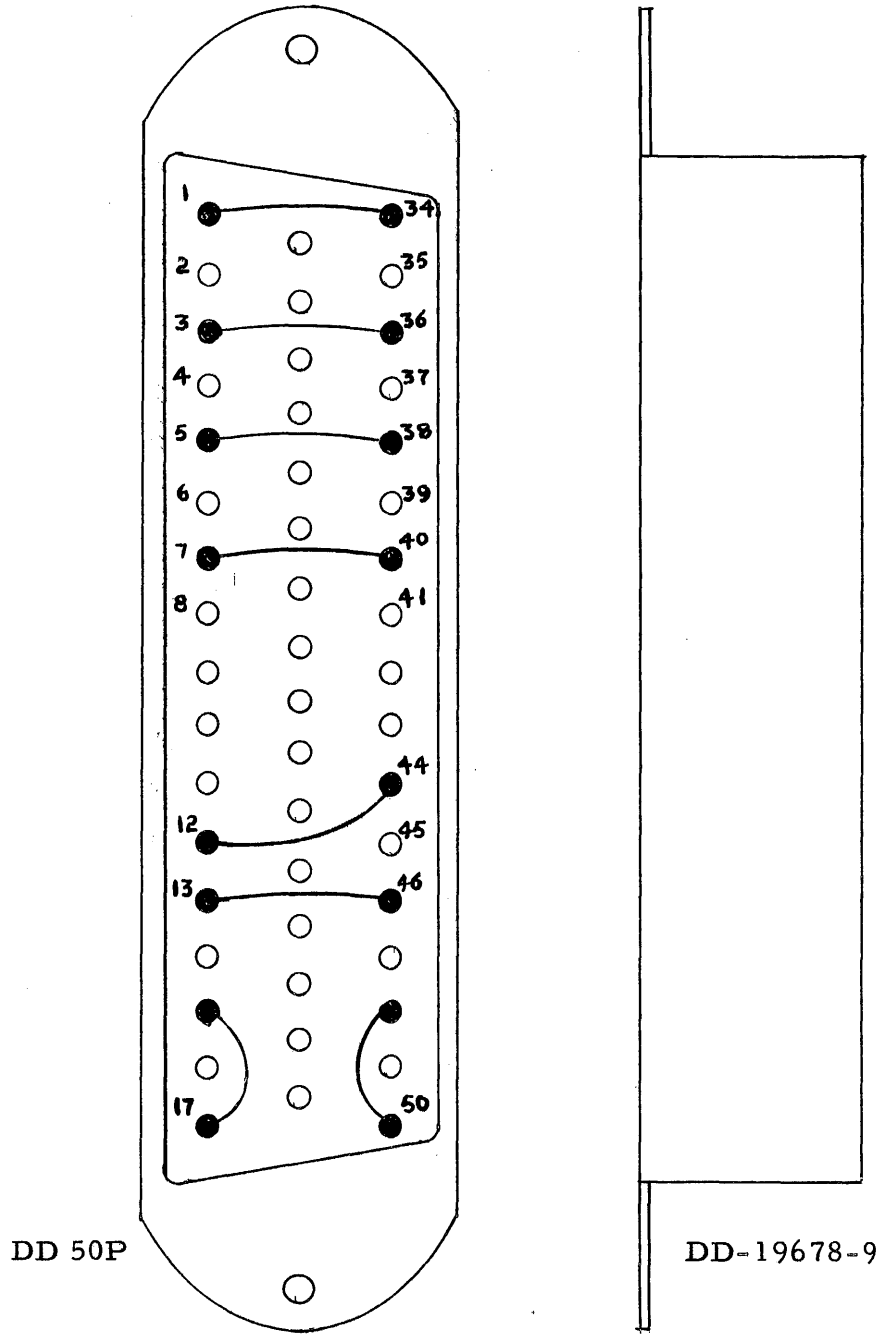


Figure 1-11. Bootstrap Input Connections for Photo Reader

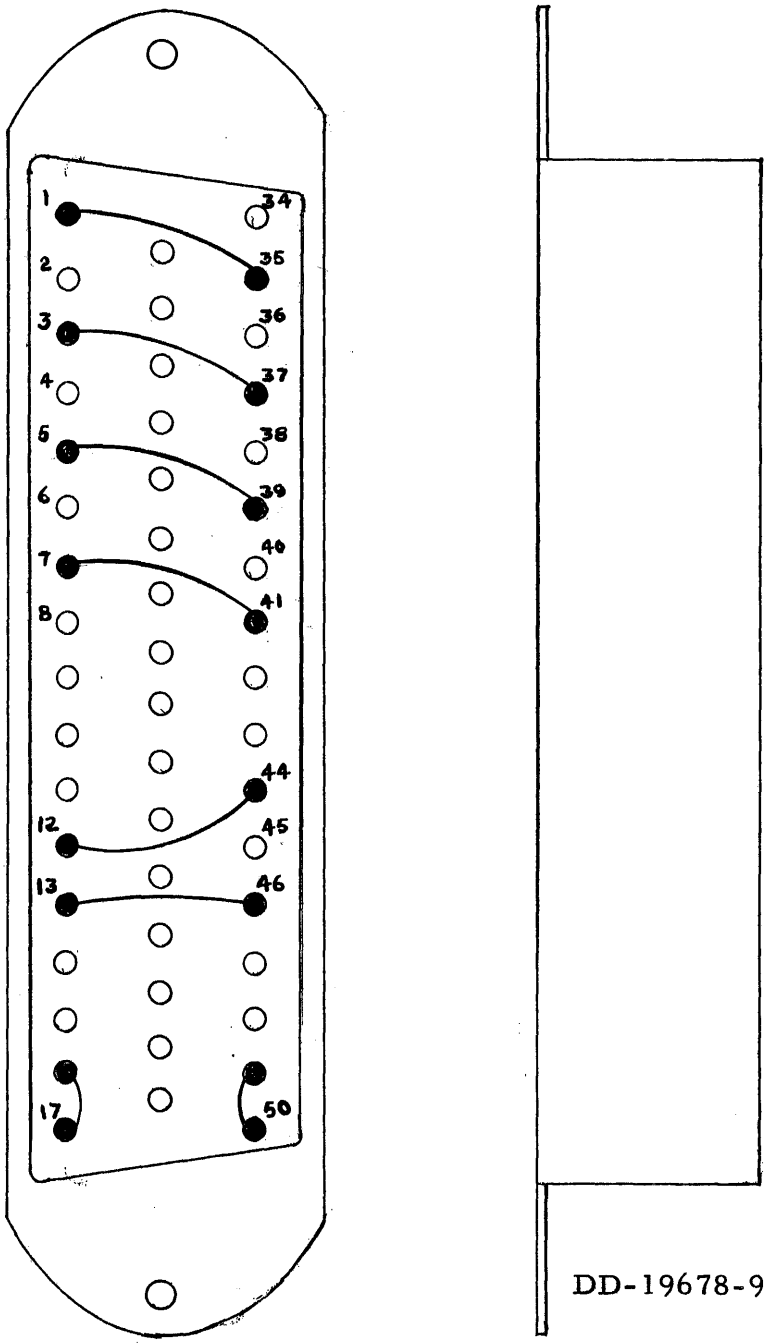


Figure 1-12. Bootstrap Input Connections for Magnetic Tape

Table 1-2

BOOTSTRAP CONNECTIONS

Flexowriter		
12P1	-	12P2
12P3	-	12P4
12P5	-	12P6
12P7	-	12P8
12P12	-	12P46
12P13	-	12P44

Magnetic Tape Unit		
12P1	-	12P35
12P3	-	12P37
12P5	-	12P39
12P7	-	12P41
12P12	-	12P44
12P13	-	12P46
12P17		
12P50		

Photo Reader		
12P1	-	12P34
12P3	-	12P36
12P5	-	12P38
12P7	-	12P40
12P12	-	12P44
12P13	-	12P46
12P17		
12P50		

1-33. TYPEWRITER INFORMATION AND CONTROL SIGNALS

The signals designated (R1) (R4) (Rc) ($\overline{Rc}$) are the stop code, serial data, common signal and inverted common signal respectively, from the mechanical reader.

1-34. PHOTOTAPE INFORMATION AND CONTROL SIGNALS

The signals designated (S1) (S4) ($\overline{S5}$) (S6) are the stop code, serial data, common signal and inverted common signal respectively. Connections are also made for photo reader Stop and photo reader Start, see Figure 1-9.

1-35. MAGNETIC TAPE INFORMATION AND CONTROL SIGNALS

The signals designated (U1) (U4) ($\overline{U5}$) (U6) are the stop code, serial data, common signal and inverted common signal respectively. Connections are also made for magnetic tape unit Start and magnetic tape unit Stop.

I. CONTROL PULSE OUTPUT (J15, J16) PTU command

For communication with, or direct control of, external devices and systems, the PB 250 Computer is equipped with two control pulse output connectors as follows:

1-36. ADDRESSING

The true outputs of the command line flip-flops (K1, K2, and K3) and the operand flip-flops (L1, L2, L3, L4, and L5) are made available for decoding. This decoded address will specify which external device or input on that particular device should be activated.

1-37. EXECUTE PULSE

The execute pulse signal (designated Cpg) is supplied to perform activation (a variable length pulse, 12 μsec to 3 msec) at the proper time.

1-38. POWER

Power is supplied from the local supply to drive the external decoding and coupling logic.

J. COMPUTER COUPLING (J5)

The PB 250 Computer has been designed to couple directly with another PB 250, complete with a small amount of built-in "common" memory. For systems application, this ability makes the PB 250 Computer an expandable digital component.

1-39. PULSE SYNCHRONIZATION

A basic counter signal (F5) is extended to the external slave computer to synchronize its pulse counter.

1-40. SECTOR SYNCHRONIZATION

To synchronize the "Sector Times" of the two computers, an initial program is loaded into the PB 250 acting as the master computer, which will execute a PTU with an operand address of 37 during sector 000. The execute signal (Cpg) of the PTU command is sent to the slave computer and clears it's sector counter to 000 during sector 000 of the master computer, placing the two computers in full synchronization.

1-41. MEMORY COUPLING

The master computer and slave computer each have access to line eight of the others memory by addressing memory line position 20 of their own memory. This is further shown in Figure 1-13.

1-42. CLOCK SIGNALS

All clock signals for both master and slave computers are derived from a 2 megacycle sine wave generated by the master computer. This ensures

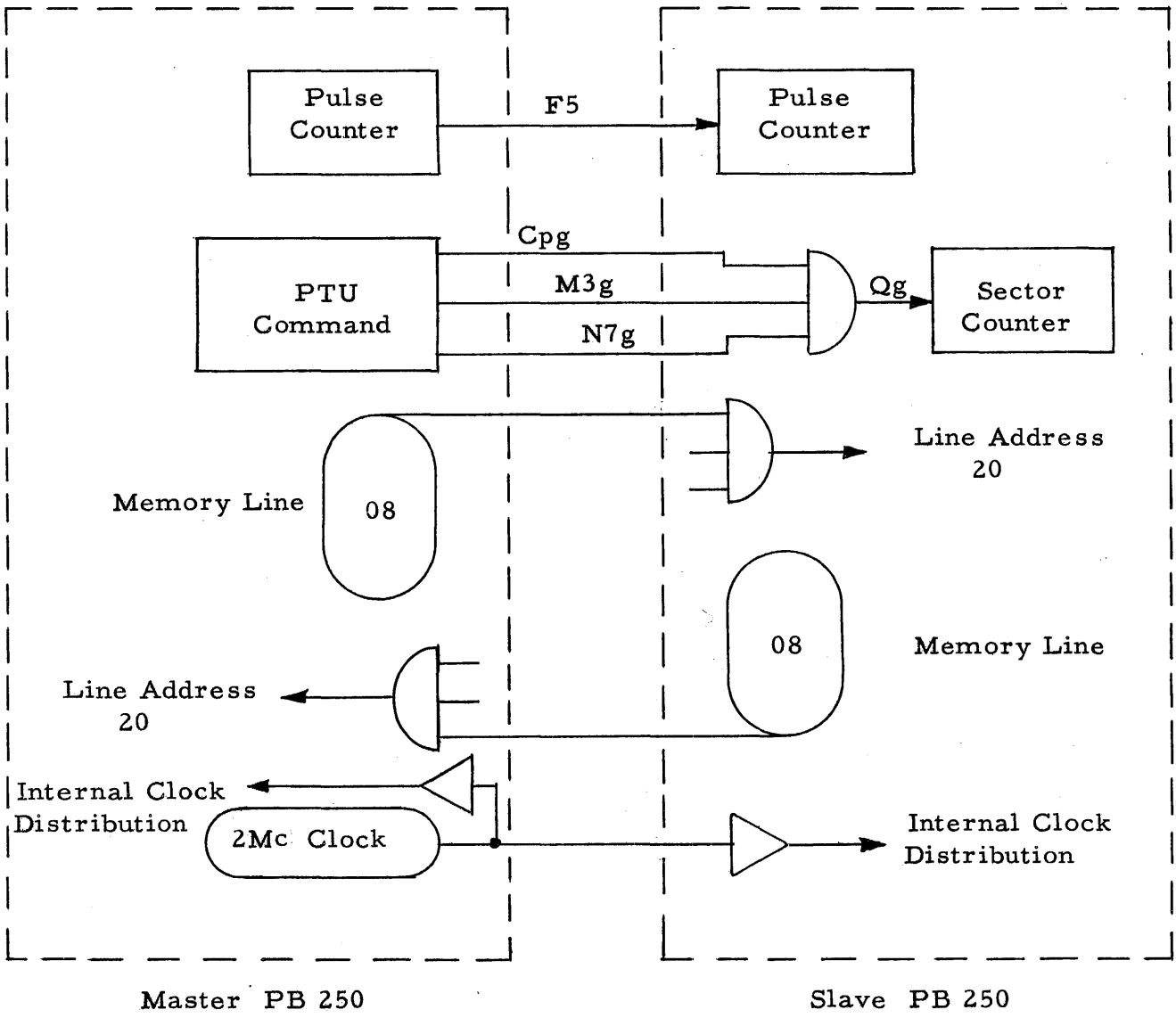


Figure 1-13. Computer Coupling

that both computers will be in phase.

NOTE

There is no increase in the access time for data and generally the transfer time (computer-to-computer) for data, is zero. Additionally, line 08 still functions in its normal manner for internal operation.

For special applications, the number of computers to be interconnected can be increased to four.

Table 1-3 (Sheet 1 of 2)

CONTROL PULSE ASSIGNMENTS FOR PB 250 PERIPHERAL EQUIPMENT

Code	Unit	Function
$\overline{L5}$ $\overline{L4}$ L3 $\overline{L2}$ $\overline{L1}$		Punch one card
$\overline{L5}$ $\overline{L4}$ $\overline{L3}$ $\overline{L2}$ L1	Card Punch	Punch continuous
$\overline{L5}$ $\overline{L4}$ $\overline{L3}$ L2 $\overline{L1}$	Card Reader	Read one card
$\overline{L5}$ $\overline{L4}$ $\overline{L3}$ L2 L1		Read continuous
$\overline{L5}$ $\overline{L4}$ L3 $\overline{L2}$ $\overline{L1}$	SSH with $\overline{K3}$ K2 K1	Open aperture - close aperture
$\overline{L5}$ $\overline{L4}$ L3 $\overline{L2}$ L1		
$\overline{L5}$ $\overline{L4}$ L3 L2 $\overline{L1}$	Dump	
$\overline{L5}$ $\overline{L4}$ L3 L2 L1	A to D Converter	Read first character
$\overline{L5}$ L4 $\overline{L3}$ $\overline{L2}$ $\overline{L1}$		Read second character
$\overline{L5}$ L4 $\overline{L3}$ $\overline{L2}$ L1		Unit 1
$\overline{L5}$ L4 $\overline{L3}$ L2 $\overline{L1}$	Magnetic Tape	Start reverse 2
$\overline{L5}$ L4 $\overline{L3}$ L2 L1		3
$\overline{L5}$ L4 L3 $\overline{L2}$ $\overline{L1}$		4
$\overline{L5}$ L4 L3 $\overline{L2}$ L1		5
$\overline{L5}$ L4 L3 L2 $\overline{L1}$		6
$\overline{L5}$ L4 L3 L2 L1		Stop & read set
L5 $\overline{L4}$ $\overline{L3}$ $\overline{L2}$ $\overline{L1}$	Magnetic Tape	Write set
L5 $\overline{L4}$ $\overline{L3}$ $\overline{L2}$ L1		Start forward Unit 1
L5 $\overline{L4}$ $\overline{L3}$ L2 $\overline{L1}$		2

Table 1-3 (Sheet 2 of 2)

CONTROL PULSE ASSIGNMENTS FOR PB 250 PERIPHERAL EQUIPMENT

Code	Unit	Function
L5 $\overline{L4}$ $\overline{L3}$ L2 L1	Magnetic Tape	Start forward Unit 3
L5 $\overline{L4}$ L3 $\overline{L2}$ $\overline{L1}$		4
L5 $\overline{L4}$ L3 $\overline{L2}$ L1		5
L5 $\overline{L4}$ L3 L2 $\overline{L1}$		6
L5 $\overline{L4}$ L3 L2 L1	A to D Converter	Convert
L5 L4 $\overline{L3}$ $\overline{L2}$ $\overline{L1}$	H S Buffer	
L5 L4 $\overline{L3}$ $\overline{L2}$ L1	Use K's for	
L5 L4 $\overline{L3}$ L2 $\overline{L1}$	Multiple units	
L5 L4 $\overline{L3}$ L2 L1		
L5 L4 L3 $\overline{L2}$ $\overline{L1}$	H S Reader	Start
L5 L4 L3 $\overline{L2}$ L1	H S Reader	Stop
L5 L4 L3 L2 $\overline{L1}$	H S Punch	Start
L5 L4 L3 L2 L1	H S Punch	Stop

II. OUTPUT AND INPUT LOADING, TIMING AND COUPLING CONSIDERATIONS

A. INPUTS

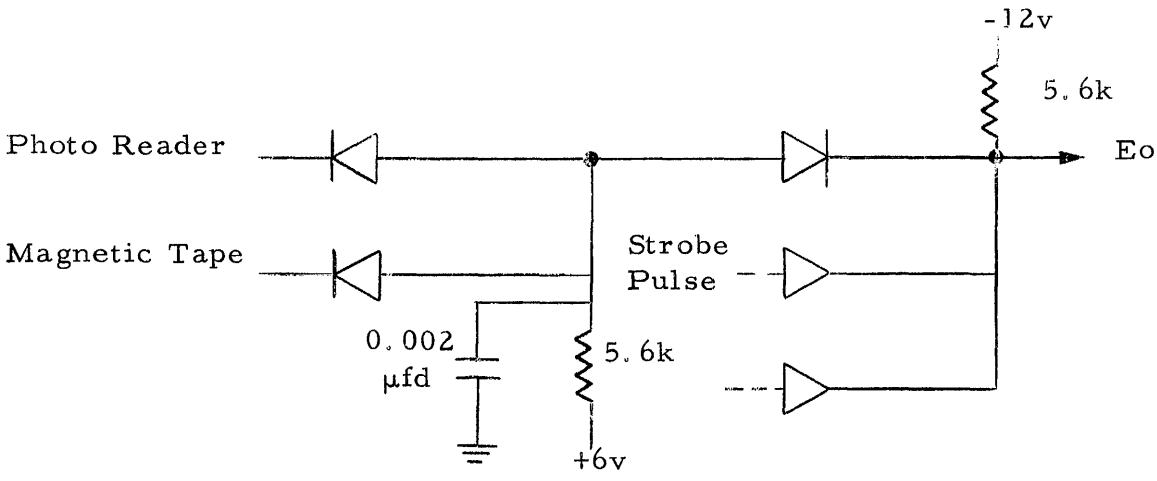
The logic voltage levels for all inputs are as follows:

True	=	-10v	±	2v
False	=	0v	±	0.25v

The rise and fall times of the incoming signals will depend on the program being used and the external logic.

2-1. EIGHT BIT BUFFER INPUT

The data inputs from the photo reader connector and the magnetic tape connector feed in parallel to a serializing gate (designated Bg) which in turn feeds the 8-bit input buffer. The input circuit to Bg is as follows:

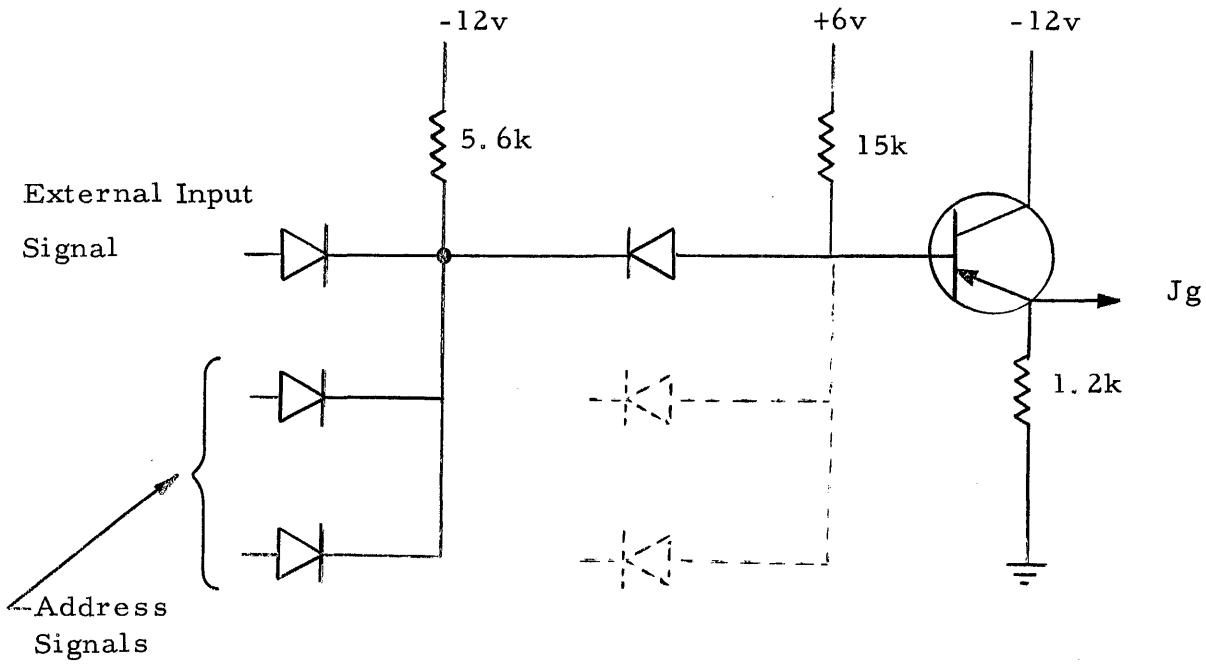


When the inputs are open, or at ground level, no current is required.

When the input signal is at a true level (-12v) it must be capable of delivering 3.2 ma. It is recommended that the input program be written such that the Bg gate strobes the input signal for several sector times.

2-2. JUMP CONTROL INPUTS

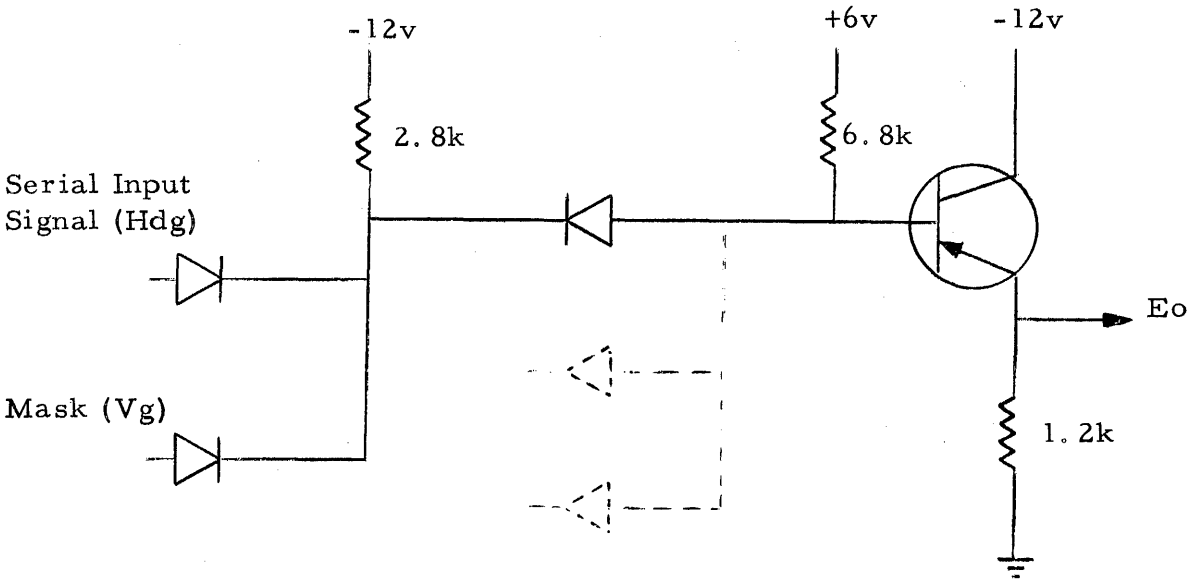
The jump control lines from external devices feed into the following type of circuit:



When the jump control signal is true (-12v) the input current requirement is nil. When the input signal is false (0v) it must be capable of delivering 2 ma.

2-3. SERIAL INPUT SIGNAL (Hdg)

The serial input signal from external shift registers feeds into the following circuit:



When the input signal is true (-12v) the input current requirement is nil. When the signal is false, it must be capable of delivering 4.3 ma.

B. OUTPUTS

All signal outputs from the computer have the following logic voltage levels:

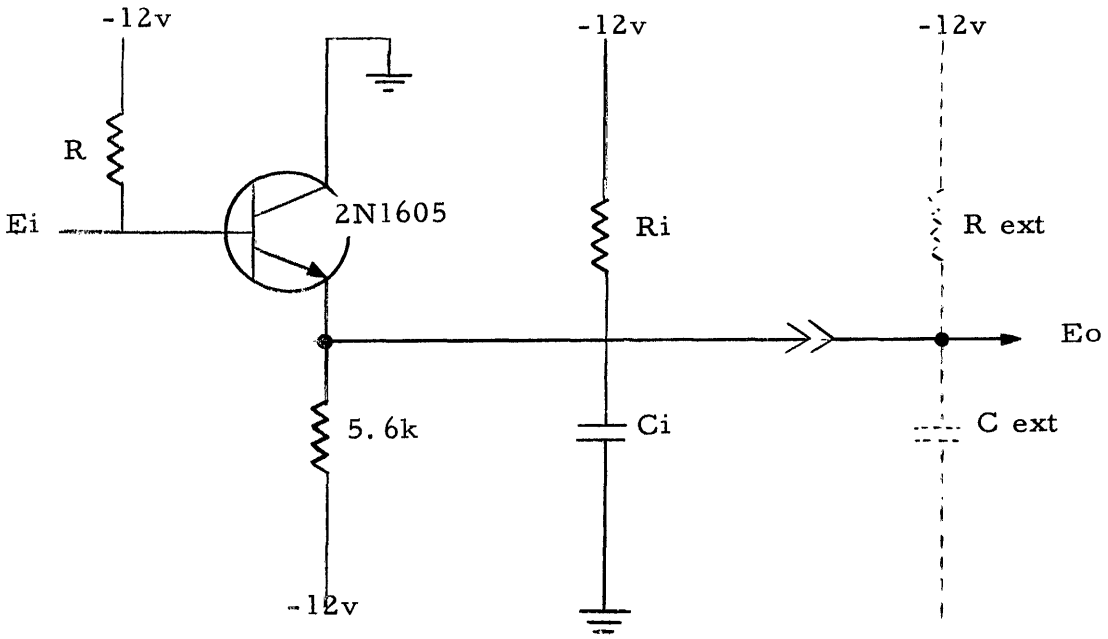
True	=	-10v	±	2v
False	=	0v	±	0.25v

For maximum versatility and reliability many of the internal flip-flops are time-shared in their output functions. As an example, the operand line address flip-flops (L1, L2, L3, L4, and L5) appear in several output connectors. For this reason, the output loading and timing is described in terms

of flip-flops and drivers, rather than connectors.

2-4. OPERAND LINE FLIP-FLOPS (L1, L2, L3, L4, L5)

The true outputs of the "L" flip-flops are fed through the emitter follower circuit shown in this paragraph. Because of internal capacity and loading, the external capacity should be restricted to 500 μμf and the external load to 2 ma to -12v. An external amplifier or emitter follower is recommended in all cases.



The maximum rise and fall time of the unloaded signal is as follows:

Rise	=	0.07 μsec
Fall	=	1.00 μsec

2-5. OPERATION CODE FLIP-FLOPS (01, 02, 03)

Loading and timing is the same as described in paragraph 2-4.

2-6. COMMAND LINE FLIP-FLOPS (K1, K2, K3)

Loading and timing is the same as described in paragraph 2-4.

2-7. CONTROL PULSE EXECUTE SIGNAL (Cpg)

The Cpg signal arrives from an EF-100 emitter follower circuit, but because of no internal loading, the allowable output loading is as follows:

Capacity	500 μμf
Current	25 ma to -12v

The maximum rise and fall time of the unloaded signal is as follows:

Rise Time	=	0.07 μsec
Fall Time	=	1.00 μsec

2-8. HIGH SPEED START SIGNAL (RfTf)

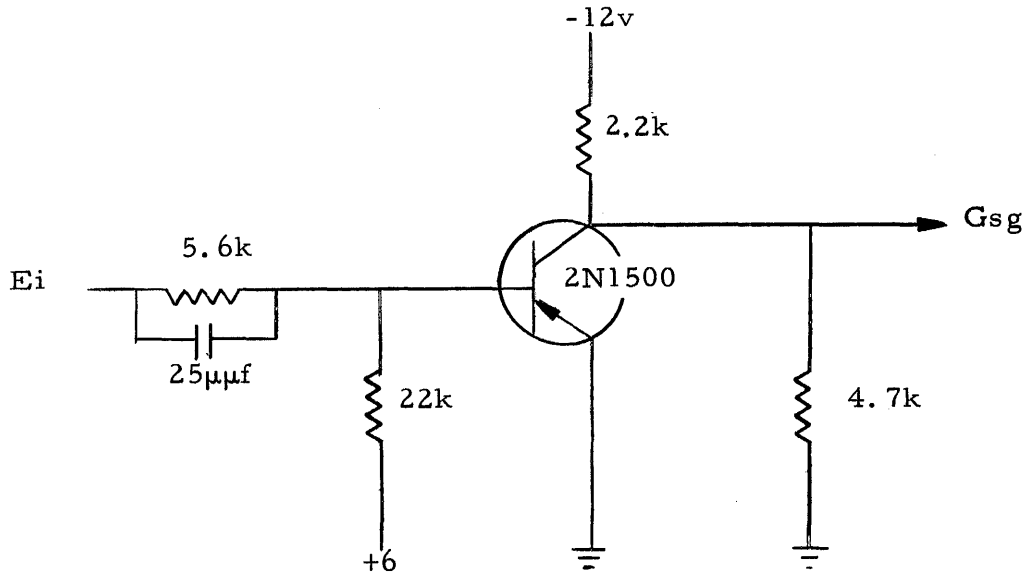
Loading and timing is the same as described in paragraph 2-7.

2-9. CHARACTER OUTPUT SIGNAL (Cog)

Loading and timing is the same as described in paragraph 2-7.

2-10. SERIAL INPUT SHIFT SIGNAL (Gsg)

The Gsg shift signal is driven by two cascaded inverters, one of which is shown in this paragraph. Output loading should be limited to 500 μμf and 4 ma to -12v.

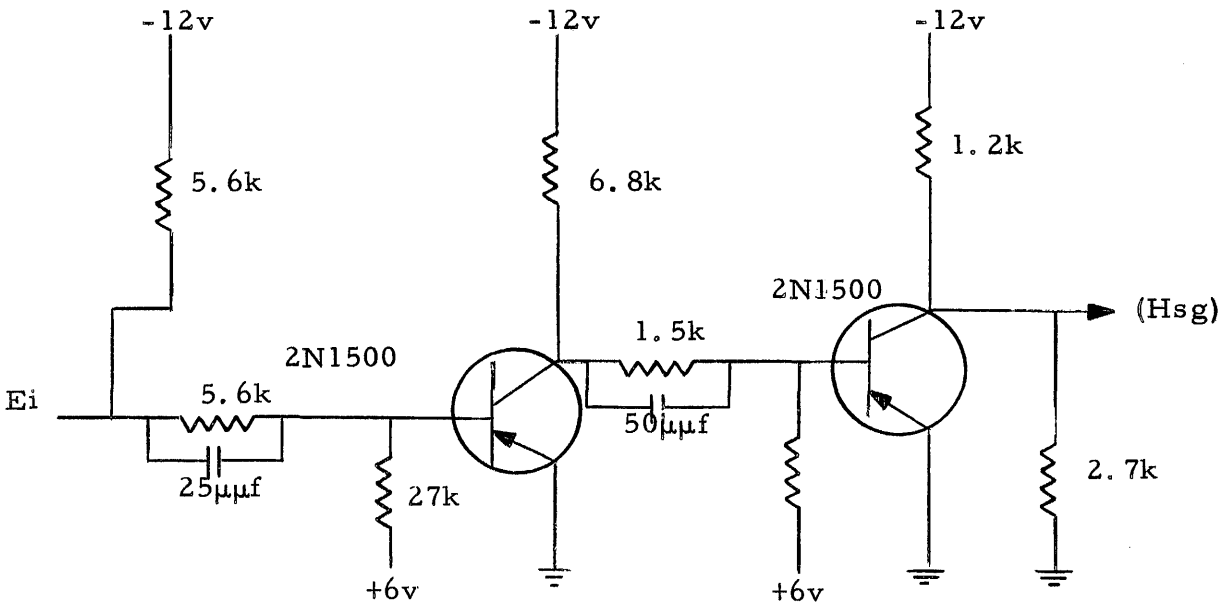


The maximum rise and fall time of the unloaded signal is as follows:

Rise Time	=	0.07 μsec
Fall Time	=	0.70 μsec

2-11. SERIAL OUTPUT SHIFT SIGNAL (Hsg)

The Hsg shift signal is driven from a GD-100 clock driver module. External capacity should be limited to 500 μμf and 20 ma to -12v. The circuitry is as follows:



The maximum rise and fall time of the unloaded signal is as follows:

Rise Time	=	0.05 μsec
Fall Time	=	0.70 μsec

2-12. SERIAL OUTPUT DATA SIGNAL (Gdg)

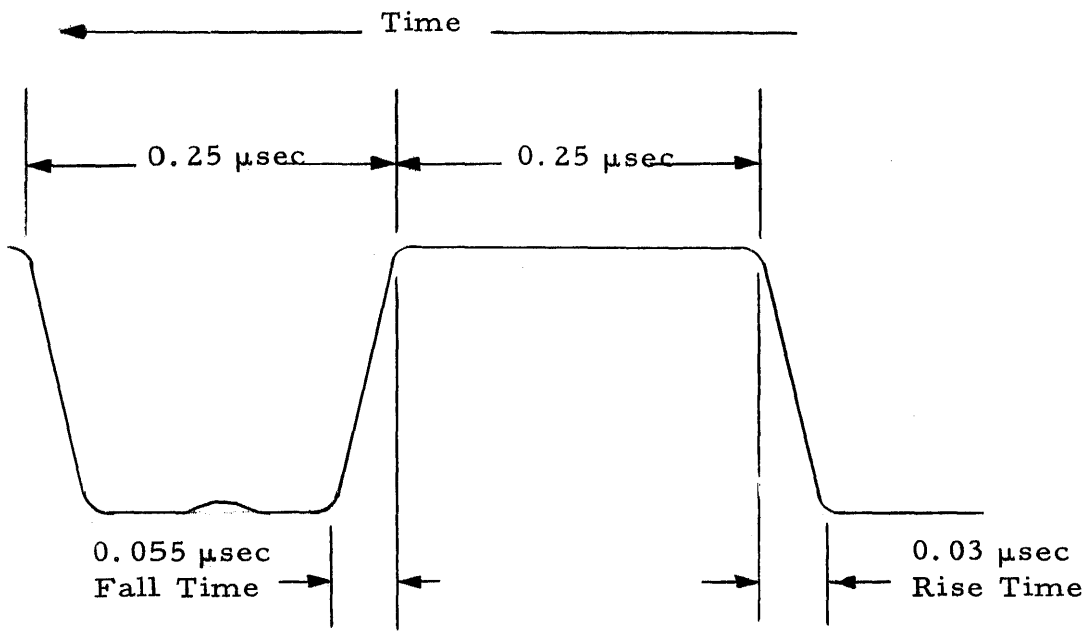
The Gdg signal is driven by an inverter and the loading and timing is the same as described in paragraph 2-10.

2-13. COMPUTER CLOCK (C1)

The computer clock signal supplied for external use is driven from an SA-100 sine wave driver. The output of this amplifier is also used internally. This signal should be connected to the shaper input (pin 14) of a PBC XCG-100 module by a 90 ohm coaxial cable. The computer clock output of this module should be connected to a CD-100 module to drive the gates in the

external unit.

The waveform for computer clock signal is as follows:



2-14. POWER SUPPLY (PS-7)

The power supply is designed to supply power to auxiliary circuitry as well as internal computer logic. The extra available power is as follows:

+ 6 volt supply	1 amp
-12 volt supply	3 amp

2-15. SA 100 SINEWAVE AMPLIFIER

The SA 100 sinewave amplifier module (see Figure 2-1), is a tuned class C amplifier used for synchronization of a PB 250 Computer system consisting of one or more computers and their peripheral equipment. Figure 2-2 shows an example of a distribution system from an SA 100 module to a PB 250 Computer system consisting of three computers (one master and two slaves) each with a Memory Unit and two High-Speed Buffers.

The SA 100 accepts the two megacycle sinewave generated by the oscillator section of an XCG 100 module, amplifies and distributes it to the various units which comprise a PB 250 system. The output of the SA 100 is processed in each unit by the shaper section of the XCG 100 module to produce computer and memory clock signals. Distribution of the SA 100 output is established to allow synchronization of the clock signals within 0.01 microsecond between the computer system units. Specifications of the SA 100 are given in Table 2-1.

Table 2-1

SA 100 SPECIFICATIONS

Requirements	Measurements
Input (sinewave with the following characteristics)	
Frequency	2 Mc
Amplitude	3.5 to 5.5 v rms
Impedance	4.3 Kilohms at 2 Mc
Output (at maximum load)	
Number of XCG shapers	12
Distribution cabling capacitance	1500
Power	
-12 v	22 ma
+ 6 v	6 ma

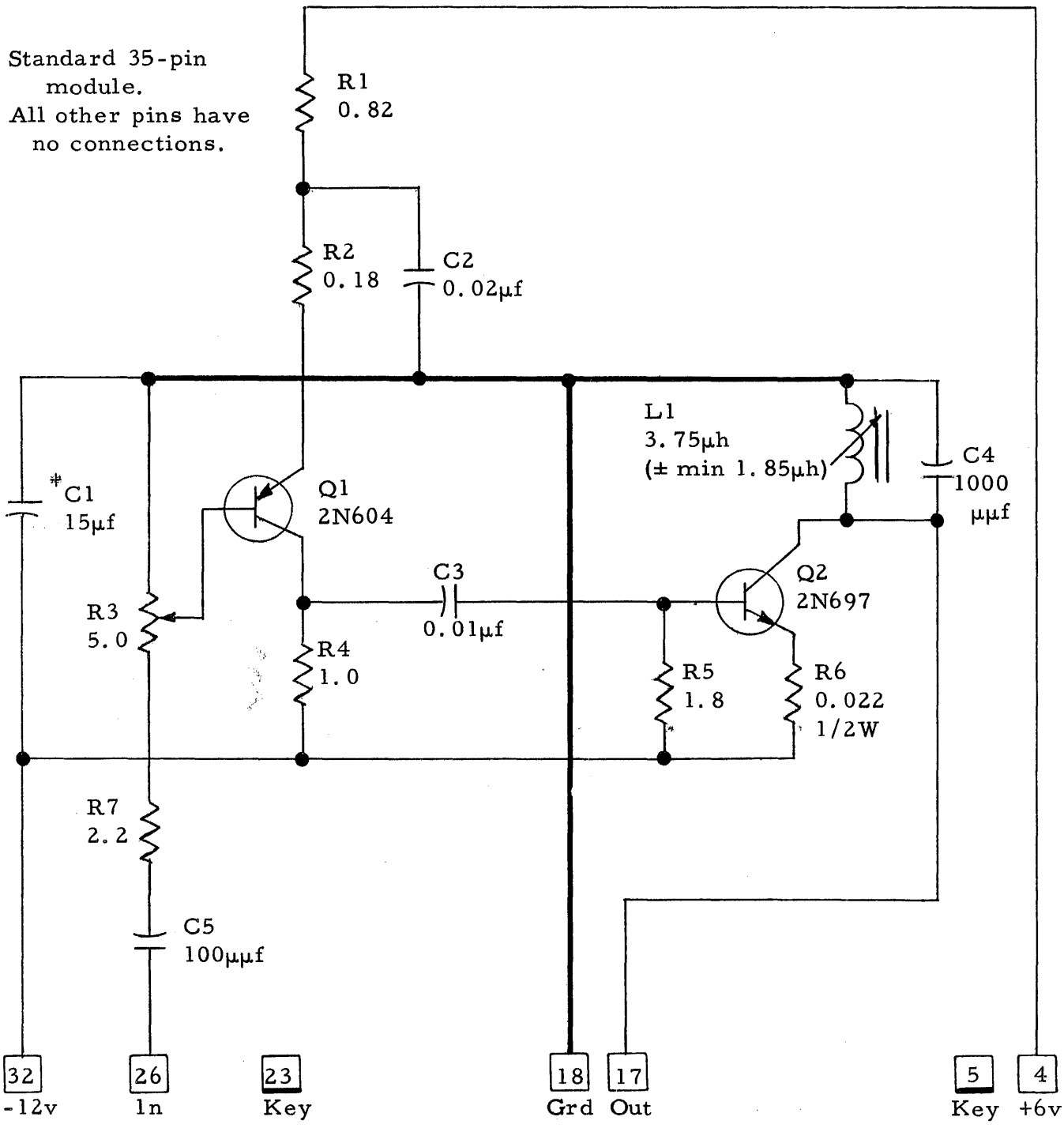
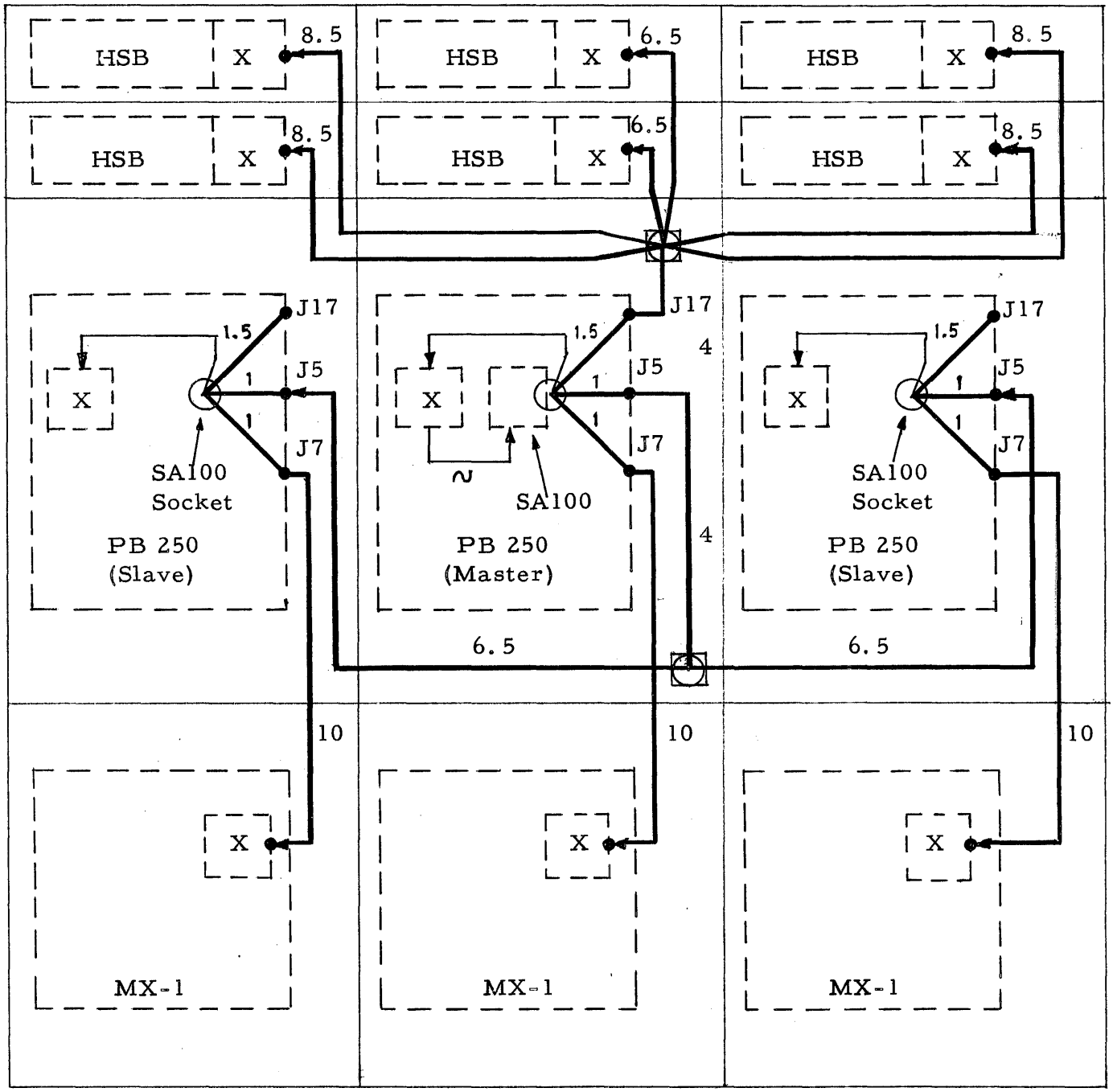


Figure 2-1. SA 100 Sinewave Amplifier Schematic



Symbols:

X XCG100

Coaxial Distribution Cable

Connector

Fan-out Junction

Junction Box

All dimensions are in feet

Figure 2-2. SA 100 Clock Distribution Example

2-16. Distribution Cabling

The first cable junction is at the socket of the SA 100, with a maximum fan-out of four primary lines. Any one of the primary lines may in turn have one junction with a maximum fan-out of six secondary lines. Where a primary line fans out into two secondary lines only, each secondary line is allowed a third junction with a fan-out of two tertiary lines.

Applicable cabling details are as follows:

a) All connections are made with Microdot 95-3920 coaxial cable (Z_o = 95 ohms, capacitance per foot = 13 μμf).

b) Total cable length in distribution system is a maximum of 110 ft.

c) Cable length from the SA 100 to any load point is a maximum of 24 ft.

2-17. Final Adjustment

After the clock system is installed and turned on, the SA 100 is first tuned for maximum output by means of variable inductor L1 (see Figure 2-3). The output amplitude is then set to 12 volts peak-to-peak by means of potentiometer R 3 (see Figure 2-3).

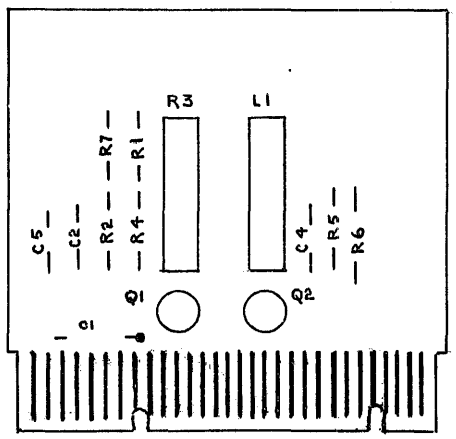


Figure 2-3. SA 100 Printed Wiring Assembly

To tune the SA 100 module for maximum output, it is necessary to remove the locking screw from the variable inductor L 1. After the required adjustment has been made, the locking screw must be replaced.

APPENDIX A

INPUT-OUTPUT PIN CONNECTIONS

Table A-1 (Sheet 1 of 12)

TYPE 37P, NO. 1J, FLEXOWRITER INPUT FUNCTION

Origin	Pin No.	Destination	Term	Origin	Pin No.	Destination	Term
	1	23A5	(T1)		15	23A21	(R8)
	2	24A12	(T2)		16	25A28	(Rc)
	3	23A13	(T3)		17	25A31	($\overline{Rc}$)
	4	25A12	(T4)	1J27	18	23A34	((En) + RfTf)
	5	24A5	(T5)	1J26	19	24A34	(Rf Tf)
	6	25A5	(T6)		20	25A25	(Tb)
	7	23A31	(Tc)		21	24A28	(En)
	8	23A8	(R1)		22	24A31	($\overline{En}$)
	9	24A15	(R2)		23	24A25	(Bp)
	10	23A15	(R3)	1J25	24	23E5L	-12v
	11	25A15	(R4)	1J28	25	1J24	-12v
	12	24A8	(R5)		26	1J19	(Rf $\overline{Tf}$)
	13	25A8	(R6)		27	1J18	((En) + Rf Tf)
	14	24A21	(R7)		28	1J25	-12v

Table A-1 (Sheet 2 of 12)

TYPE 15 S, NO. 2J
CHARACTER OUTPUT FUNCTION

Origin	Pin No.	Destination	Term
3J1	1	14J10	K3'
3J2	2	14J11	K2'
3J3	3	14J12	K1'
3J4	4	14J13	L1'
3J5	5	14J14	L2'
3J6	6	14J15	L3'
3J7	7	14J16	L4'
3J8	8	14J17	L5'
3J9	9	14J18	01'
3J10	10	14J19	02'
3J11	11	14J20	03'
3J12	12	18J26	Cog
3J13	13	15J13	Gnd
3J14	14	15J14	+6v
3J15	15	15J15	-12v

TYPE 15 S, NO. 3 J
CHARACTER OUTPUT FUNCTION

Origin	Pin No.	Destination	Term
18A26	1	2J1	K3'
18A29	2	2J2	K2'
19B5	3	2J3	K1'
26D7	4	2J4	L1'
23C11	5	2J5	L2'
23C8	6	2J6	L3'
23C5	7	2J7	L4'
19B29	8	2J8	L5'
45B35	9	2J9	01'
36B34	10	2J10	02'
36B33	11	2J11	03'
18A23	12	2J12	Cog
	13	2J13	Gnd
	14	2J14	+6v
	15	2J15	-12v

Table A-1 (Sheet 3 of 12)

TYPE 25S, NO. 4J, FLEXOWRITER OUTPUT FUNCTION

Origin	Pin No.	Destination	Term
	1	26E24	LTC
	2	26C5	LT1
	3	26C9	LT2
	4	26C13	LT3
	5	26C20	LT4
	6	26C24	LT5
	7	26C28	LT6
	8	26E13	LPC
	9	26D5	LP1
	10	26D9	LP2
	11	26D13	LP3
	12	26D20	LP4
	13	26D24	LP5
	14	26D28	LP6
	15	27E5	LP7
	16	27E9	LP8
	17	26E9	(Rf $\overline{\text{Tf}}$)
	18	26E5	($\overline{\text{Rf}}$ Tf)
	19		Spare
	20		Spare
	21	4J24	- 48 v
	22	4J23	
4J22	23		
4J21	24	4J25	-48 v
4J24	25	23E6R	- 48 v

Table A-1 (Sheet 4 of 12)

TYPE DA-B11C1S, NO. 5J, COMPUTER COUPLING FUNCTION

Origin	Pin No.	Destination	Term
21A33	1		N7g
21A34	2		M3g
21A35	3		Cpg
27B33	4		M8r
26B20	5		F5
21A20	6		F5
24E1R	7		Gnd
26B6	8		M8r
	9		
24B17	A1		SA out 2

Table A-1 (Sheet 5 of 12)

TYPE 25P, NO. 7J, EXTERNAL MEMORY FUNCTION

Origin	Pin No.	Destination	Term
23C26	1		M2g
38B5	2		M3g
25D5	3		M4g
25D8	4		M5g
25D11	5		M6g
25D14	6		M7g
25C5	7		N0g
25C8	8		N1g
25C11	9		N2g
25C14	10		N3g
25C20	11		N4g
25C23	12		N5g
25C26	13		N6g
35D26	14		N7g
26B14	15		Wg
26B24	16		Ig
27C12	17		Ig
	18	40B20	Fxg
14J21	19	18A20	Cpg
	20		E5
	21	22E2R	+6v
	22	17J6	0
	23	23E5b	- 12 v
Shield	24		
24B13	25		SA out 4

TYPE 11C1P, NO. 8J
JUMP CONTROL INPUT FUNCTION

Origin	Pin No.	Destination	Term
42B33	1		J0
42B27	2		J1
42B23	3		J2
42B10	4		J3
42B6	5		J4
39B29	6		J5
41B33	7		J6
41B27	8		J7
	9	9J9	Gnd

TYPE 11C1P, NO. 9J
JUMP CONTROL INPUT FUNCTION

Origin	Pin No.	Destination	Term
41B23	1		J8
41B10	2		J9
41B5	3		J10
39B25	4		J11
40B33	5		J12
40B27	6		J13
40B23	7		J14
40B10	8		J15
8J9	9	10J9	Gnd

TYPE 11C1P, NO. 10J
JUMP CONTROL INPUT FUNCTION

TYPE 11C1P, NO. 11J
JUMP CONTROL INPUT FUNCTION

Origin	Pin No.	Destination	Term	Origin	Pin No.	Destination	Term
40B6	1		(J16)	38B8	1	16J9	(J24)
39B12	2		(J17)	39B10	2	15J9	(J25)
36B12	3		(J18)	37B33	3	18J27	(J26)
36B7	4		(J19)	37B27	4	18J9	(J27)
38B35	5		(J20)	37B23	5	14J9	(J28)
38B29	6		(J21)		6		Spare
38B25	7		(J22)		7		Spare
38B12	8		(J23)		8		Spare
9J9	9	11J9	Gnd	10J9	9	24E5L	Gnd

Table A-1 (Sheet 8 of 12)

TYPE DDM50S, NO. 12J, BOOTSTRAP INPUT FUNCTION

Origin	Pin No.	Destination	Term	Origin	Pin No.	Destination	Term
	1	2D25	(B6)		26		
	2	25A27	(Rc)		27		
	3	9C2	(B5)		28		
	4	25A33	($\overline{Rc}$)		29		
	5	9C16	(B4)		30		
	6	25A14	(R4)		31		
	7	16D2	(B1)		32		
	8	23A7	(R1)		33		
	9				34	14J6	(S6)
	10				35	18J6	(U6)
	11				36	14J5	(S5)
	12	13A25	(Mr)		37	18J5	(U5)
	13	22C34	($\overline{Mr}$)		38	14J4	(S4)
	14				39	18J4	(U4)
	15	14J33	Start		40	14J1	(S1)
	16	18J33			41	18J1	(U1)
14E33	17		HS Read Start		42		
	18				43		
	19			18J24	44	12J45	Gnd
	20			12J44	45	24E4R	Gnd
	21			18J25	46	12J47	-12 v
	22			12J46	47	23E4R	-12 v
	23				48	14J37	Stop
	24				49	18J37	
	25			23B1	50		HS Read Stop

Table A-1 (Sheet 9 of 12)

TYPE 37S, NO. 14J, PHOTO READER INPUT FUNCTION

Origin	Pin No.	Destination	Term	Origin	Pin No.	Destination	Term
12J40	1	23A3	(S1)	2J10	19	18J19	02'
	2	24A16	(S2)	2J11	20	18J20	03'
	3	23A16	(S3)	15J12	21	7J19	Cpg
12J38	4	25A16	(S4)	18A14	22	18J22	(Rf Tf)
12J36	5	24A3	(S5)		23	18J23	+6 v
12J34	6	25A3	(S6)		24	18J24	0
	7	24A20	(S7)		25	18J25	-12 v
	8	23A20	(S8)		26		
	9	11J5	(Sc)		27		
2J1	10	15J1	K3'		28		
2J2	11	15J2	K2'		29		
2J3	12	15J3	K1'		30		
2J4	13	15J4	L1'		31		
2J5	14	15J5	L2'		32		
2J6	15	15J6	L3'	12J15	33		Start
2J7	16	15J7	L4'		34		
2J8	17	15J8	L5'		35		
2J9	18	18J18	01'		36		
				12J48	37		Stop

Table A-1 (Sheet 10 of 12)

TYPE 15P, NO. 15J

PULSE CONTROL OUTPUT FUNCTION

Origin	Pin No.	Destination	Term
14J10	1	16J1	K3'
14J11	2	16J2	K2'
14J12	3	16J3	K1'
14J13	4	16J4	L1'
14J14	5	16J5	L2'
14J15	6	16J6	L3'
14J16	7	16J7	L4'
14J17	8	16J8	L5'
11J2	9		J25
	10		
	11		
16J12	12	14J21	Cpg
2J13	13	16J13	Gnd
2J14	14	16J14	+6 v
2J15	15	16J15	- 12 v

TYPE 15P, NO. 16J

PULSE CONTROL OUTPUT FUNCTION

Origin	Pin No.	Destination	Term
15J1	1	17J1	K3'
15J2	2	17J2	K2'
15J3	3	17J3	K1'
15J4	4	18J13	L1'
15J5	5	18J14	L2'
15J6	6	18J15	L3'
15J7	7	18J16	L4'
15J8	8	18J17	L5'
11J1	9		J24
	10		
	11		
18J21	12	15J12	Cpg
15J13	13	24E3L	Gnd
15J14	14	22E4L	+6 v
15J15	15	23E5R	- 12 v

Table A-1 (Sheet 11 of 12)

TYPE 9 P, NO. 17 J, SERIAL INPUT OUTPUT FUNCTION

Origin	Pin No.	Destination	Term
16J1	1	18J10	K3'
16J2	2	18J11	K2'
16J3	3	18J12	K1'
	4	20A30	Hsg
	5	14B7	Hdg
7J22	6	24E6R	Gnd
	7	27B19	Gsg
	8	35B19	Gdg
24B15	9		SA out 3

Table A-1 (Sheet 12 of 12)

TYPE 37S 18J, MAGNETIC TAPE READER INPUT FUNCTION

Origin	Pin No.	Destination	Term	Origin	Pin No.	Destination	Term
12J41	1	23A2	(U1)	14J19	19		02'
	2	24A17	(U2)	14J20	20		03'
	3	23A17	(U3)		21	16J12	Cpg
12J39	4	25A17	(U4)	14J22	22		(Rf Tf)
12J37	5	24A2	(U5)	14J23	23	22E4L	+6 v
	6	25A2	(U6)	14J24	24	12J44	0
	7	24A19	(U7)	14J25	25	12J46	-12 v
	8	23A19	(U8)	2J12	26		Cog
	9	11J4	(Uc)	11J3	27		(J26)
17J1	10		K3'		28		
17J2	11		K2'		29		
17J3	12		K1'		30		
16J4	13		L1'		31		
16J5	14		L2'		32		
16J6	15		L3'	12J16	33		Start
16J7	16		L4'		34		
16J8	17		L5'		35		
14J18	18		01'		36		
				12J49	37		Stop