SMART INTERFACE
PRODUCT SPECIFICATION

9/03/80

I. INTRODUCTION

A. Purpose

This specification describes the performance, the logical interface, the electrical interconnection, and the physical interconnection of the PRIAM SMART Interface. This document provides the reference technical specifications required by OEM users to connect the PRIAM SMART Interface to a host system with or without the use of a Direct Memory Access (DMA) port.

B. General Description

The PRIAM SMART Interface is a complete preprogrammed microprocessor based controller for the entire line of PRIAM Winchester Disc Drives. Up to four drives in any combination may be interconnected. The controller supports a variety of Read Sector, Write Sector, and Format commands. The data for the sector operations is transferred across an 8-bit parallel bidirectional data bus. The data transfers may be either programmed I/O or DMA transfers. Thus, the controller performs the entire function of detailed disc control while presenting to the host a basic and cost effective interface. The controller board may be mounted separately or attached to a PRIAM DISKOS drive, either 8-inch or 14-inch.

C. Feature

1. Controls up to four PRIAM disc drives.

2. Supports all PRIAM 8-inch and 14-inch disc products in any combination.

3. Designed for easy attachment to the typical microprocessor bus.

4. Controller does all bit serialization, and format related functions. The host uses a simple byte-wide interface.

5. User selectable sector sizes of 128, 256, 512, or 1024 bytes.

6. Full sector buffering which supports data transfers at any rate below 2 megabytes per second.

7. Both interrupt driven and polled operation supported.

8. On board 16-bit CRC on both ID header and data.

9. Automatic alternate sector assignment and usage to handle media defects transparent to the host.

10. Overlapped commands are supported. For example, three drives may be seeking, while seeking, reading, or writing on another drive.

11. The controller supports implied operations. For example, issuing a Read Command to a drive may cause it to Sequence Up, Restore, Seek to the desired Cylinder, Select the appropriate Head, and Read the desired sector.

12. Versatile verify functions which may be used for seek verification, sector data verification, track data verification, cylinder data verification, and complete disc data verifications.

13. Resident micro diagnostics.

II. PRODUCT DESCRIPTION

A. Physical

The controller logic is packaged on a single printed circuit board which may be mounted on either a 14-inch or 8-inch drive. There are three connectors, one for host bus connector, one for drives connection, and a third for D.C. power.

B. DC Power Requirements

+ 5 VDC, $\pm$ 5%, 3 AMP maximum

C. Environmental Limits

Ambient Temperature 0° C to 50° C
Relative Humidity 10% to 80% non-condensing.

III. INTERFACE

A. General

Commands are transferred across an 8-bit bidirectional bus under control of host generated HRD and HWR strobes. Registers within the Controller are selected by the decode of three address lines HAD2, HAD1, and HAD0. Command information is transferred over the three-state bidirectional bus (HCBUS7 to HCBUS0). An active HRD signal places the bus in the transmit mode while an active HWR signal places the bus in the receive mode.

Table 1 shows the addressing required to select each of the control registers.

TABLE 1. Control Register Assignment

AD2	AD1	AD0	RD	WR	Register
0	0	0	1	0	Controller Status
0	0	1	1	0	Disc Data-Read
0	1	0	1	0	Result 0
0	1	1	1	0	Result 1
1	0	0	1	0	Result 2
1	0	1	1	0	Result 3
1	1	0	1	0	Result 4
1	1	1	1	0	Result 5
0	0	0	0	1	Command
0	0	1	0	1	Disc Data-Write
0	1	0	0	1	Parameter 0
0	1	1	0	1	Parameter 1
1	0	0	0	1	Parameter 2
1	0	1	0	1	Parameter 3
1	1	0	0	1	Parameter 4
1	1	1	0	1	Parameter 5

B. Interface Signals

The interface signals are defined in this section. Table 2 shows the connector pin assignment. All controller signal connections are via a single 40 PIN ribbon cable connector.

1. HCBUS0H thru HCBUS7H

This is the host command bus. It is a high active 8-bit wide bidirectional bus used to transfer control and status information. Data may be transferred across this bus under control of the host by successive operations with the Disc Data Register. The most significant bit is HCBUS7. The bus is TRISTATE with the drivers enabled when the HRD signal is active. The receivers are enabled when the HRD signal is inactive.

Recommended termination for this bus is a 330 OHM resistor to +5 volts and a 390 OHM resistor to ground.

2. HRD/

This low active signal is used to gate the contents of the selected register (decode of HAD2, HAD1, HAD0) onto the HCBUS. See Table 1 for register decode assignment. This signal is terminated at the controller with a 220 OHM resistor to +5 volts and a 330 OHM resistor to ground.

3. HWR/

This low active signal is used to gate the contents of the HCBUS into the selected register (decode of HAD2, HAD1, HAD0). See Table 1 for register decode assignment. This signal is terminated at the controller with a 220 OHM resistor to +5 volts and a 330 OHM resistor to ground.

4. HAD2H HAD1H HAD0H

A high active 3-bit wide address bus used to select one of eight register pairs. One member of the pair is used to store the HCBUS contents while the contents of the other may be placed on the HCBUS depending upon the host's manipulation of HRD and HWR.

These signals are terminated at the controller with a 220 OHM resistor to +5 volts and a 330 OHM resistor to ground.

TABLE 2. Interface Connector Pin Assignment

HOST INTERFACE CABLE (J2)

PIN Number	Signal	PIN Number	Signal
1	Ground	31	Reserved
2	HCBUS0	32	Reserved
3	HCBUS1	33	Reserved
4	HCBUS2	34	Reserved
5	HCBUS3	35	Reserved
6	HCBUS4	36	Reserved
7	HCBUS5	37	Reserved
8	HCBUS6	38	Reserved
9	HCBUS7	39	Reserved
10	Ground	40	Reserved
11	HRD/		
12	Ground		
13	HWR/		
14	Ground		
15	HAD2		
16	HAD1		
17	HAD0		
18	Ground		
19	RESET/		
20	Ground		
21	HIR/		
22	Ground		
23	HREAD/HWRITE		
24	DBUSENA/		
25	Ground		
26	DTREQ/		
27	Ground		
28	Reserved		
29	Reserved		
30	Reserved		

5. RESET/

This low active signal resets the controller logic and places it into the initialized state. The Controller Busy bit will be set while initialization is in process.

This signal is terminated at the controller with a 220 OHM resistor to +5 volts and a 330 OHM resistor to ground.

6. HIR/

This low active signal may be used by the host as an interrupt request. It is set active coincident with the setting of Command Completion bit in the Controller Status Register and it is cleared upon the receipt of the Completion Acknowledge Command.

Recommended termination for this signal is a 220 OHM resistor to +5 volts and a 330 OHM resistor to ground.

7. HREAD/HWRITE

A signal from the controller to indicate the direction of data transfer across the HDBUS. If this signal is high, a read (data from controller to host) is the expected direction. A low on this line indicates that a write (data from the host to the controller) is expected.

Recommended termination for this signal is a 220 OHM resistor to +5 volts and a 330 OHM resistor to ground.

8. DBUS ENA/ (CBusy)

A low active signal from the controller to the host indicating that the controller is enabled and ready to transfer data.

Recommended termination for this signal is a 220 OHM resistor to +5 volts and a 330 OHM resistor to ground.

9. DTREQ/

A low active signal from the controller to the host used to request data transfers across the host command bus (HCBUS).

Recomended termination for this signal is a 220 OHM resistor to +5 volts and 330 OHM resistor to ground.

C. Commands

A command is issued whenever the host loads the command register. Therefore, all the appropriate Parameter Registers should be loaded prior to loading the Command Register. When the Command Register is loaded, the Busy bit in the Controller Status Register will be set and will remain set until the received command is processed. A flow chart representing this technique is shown in Figure 1.

The Controller Status Register contains information pertaining to the current state of the controller. The contents of the Controller Status Register is shown below:

7	6	5	4	3	2	1	0
CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0

Controller Status Register

where

Bit	Name	Description
CS7	Command Reject	An undefined or invalid command was received.
CS6	Controller Completion Request	The Controller has performed the requested function and the transaction status is available in the Transaction Status Register.
CS5,4	--	Not Used
CS3	Controller Busy	The Controller has received a command and is busy performing the requested command.
CS2	Data Transfer Request	This bit indicates the state of the data transfer request interface line.
CS1	Read/Write Request	If this bit is active and the Data Transfer Request line is active an input data operation is required. If this bit is not active and the Data Transfer Request line is active an output data operation is required.
CS0	Data Bus Enable	The Data Enable indicates that the controller has successfully completed its self test.

The Transaction Status Register (Result 0) is used to indicate the result of a Controller command. When the Controller Status Register indicates that a Controller completion request is pending, the host processor should read the Transaction Status Register to determine the outcome of the command. There are four major types of completion:

GOOD COMPLETION - 00

This type of completion indicates that the command was successfully completed.

SYSTEM ERROR - 01

These errors are errors that result from a system or controller problem.

OPERATOR INTERVENTION - 02

These types of errors require human intervention for recovery.

COMMAND/DRIVE ERROR - 03

Command errors are probably due to a user program error.

7	6	5	4	3	2	1	0
D1	D0	T1	T0	CC3	CC2	CC1	CC0

Transaction Status Register

Bit	Name	Description
D1,D0	Drive	This field provides an indication of which drive is supply transaction status.
CC3,CC2,CC1 CC0	Completion Code	The Completion Codes provide a detailed description of the command termination.
T1, T0	Completion Type	The Completion Type field defines four major classes of completion.

The Completion Code provides more detailed information about the completion. The completion codes are defined below.

Completion Type	Completion Code	Meaning
00	00	Good Completion-No retries
	01	Good Completion-Motion retry
	02	Good Completion-Data retry
	03	Good Completion-Alternate Sector/Track Used
01	00	Late Data Transfer
	01	CRC Error
	02	Seek Fault-Drive Reported
	03	Drive Fault
	04	Defect Map Error
	05	Seek Fault-Cylinder Mismatch
	06	Initialization Complete
	07	SMART Interface Stack Error
	08	SMART Interface Hardware Trap
	09	Read Loss Synchronization
02	00	Drive Not Ready
	01	Write Protect
	02	Drive Not Present
	03	Sector Size Invalid
	04	Alternate Area Overflow
03	00	Sector Not Found
	01	SMART Command Reject
	02	Drive Busy Command Time Out
	03	Data Transfer Time Out
	04	Illegal Cylinder/Head
	05	Invalid Drive Number
	06	Sector Number Invalid
	07	DCB Busy
	08	Command Double Write
	09	Drive Command Reject
	0A	Multi-Sector Operation Error

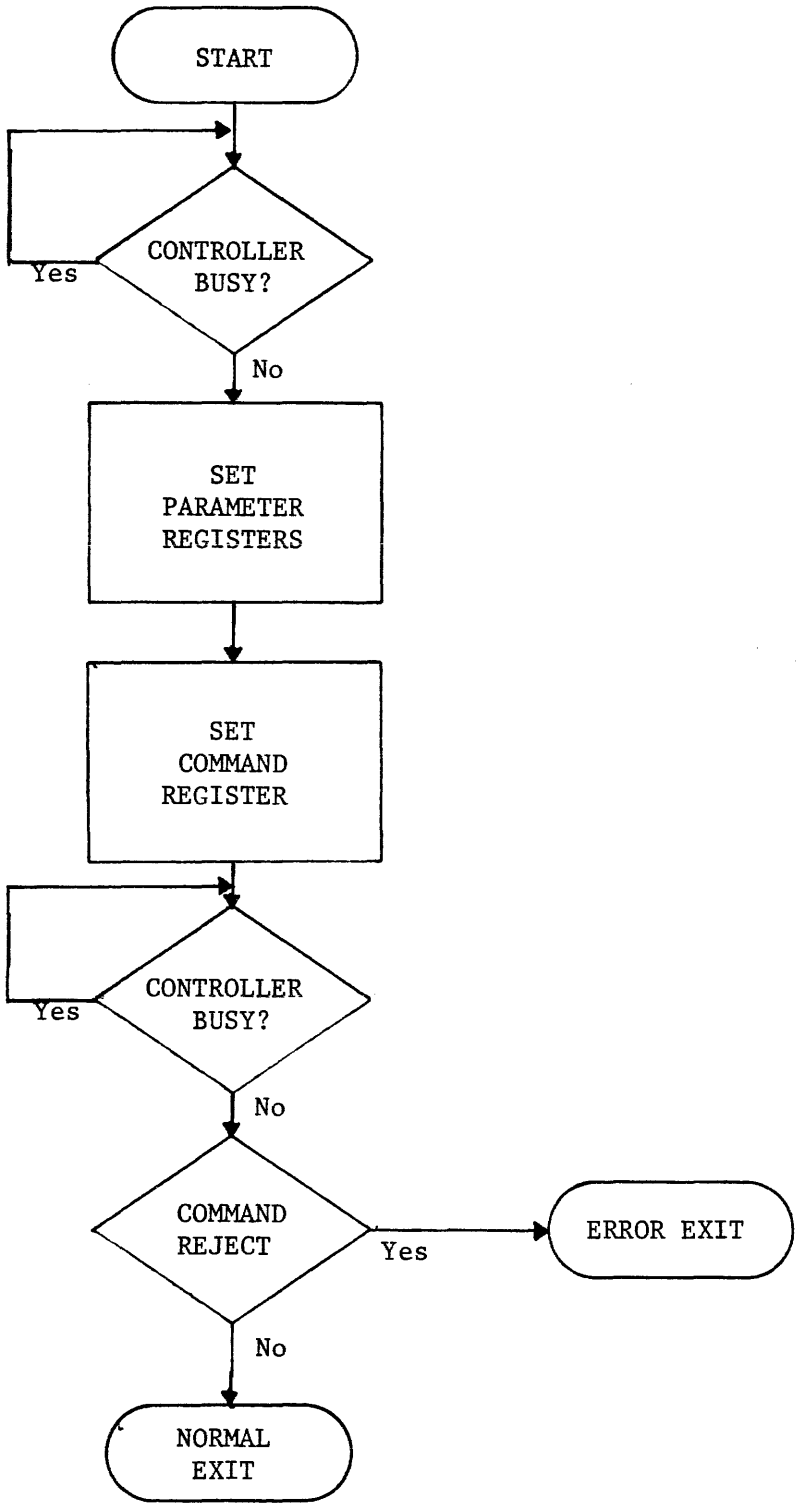


Figure 1. Basic Command Flow

1. Completion Acknowledge

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Command

Upon completion of a previously issued command the Controller Completion Request bit in the Controller Status Register will be set. After noticing that the bit is set, the host system would read the appropriate result registers then reset the Command Completion Request bit by issuing the Completion Acknowledge command.

If another pending command has been completed, (i.e., overlapped seeks), the bit will again be set immediately after updating the result registers, requiring another Completion Acknowledge command to clear it.

2. Read Buffer Command

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	1	1	Command

The Read Buffer command is used to read the contents of the data buffer data. Data in the buffer is transferred to the host automatically when a Read command is performed.

The Read Buffer command may be used to list the buffer or in error recovery operations. Data may be transferred either via DMA or by successive reads of the Disc Data Register (Address 1). The Command Completion bit is set when the last byte in the buffer is read.

3. Write Buffer Command

7	6	5	4	3	2	1	0	
0	0	0	0	0	1	0	0	Command

The Write Buffer command is used to transfer data from the host to the controller data buffer. Data is transferred from the host to the data buffer automatically when a Write command is performed. This command may be used in conjunction with the Read Buffer command to test the controller's data buffer. Data may be transferred either via DMA or by successive writes of the Disc Data Register (Address 1). The Command Completion bit is set when the last byte required to fill the buffer is transferred.

4. Read Drive Status

7	6	5	4	3	2	1	0
1	0	0	0	0	0	0	0

Command

The Read Drive Status command is used to obtain the status of the drive selected by the contents of Parameter Register 0. The status of the selected drive will be reported via Result Register 1.

The sequence to execute this command is as follows:

a. Load the Parameter Register 0 (Address 2) according to the following format:

7	6	5	4	3	2	1	0
0	0	0	0	0	0	D_1	D_0

Parameter 0

Where

D_1	D_0	
0	0	Drive 1
0	1	Drive 2
1	0	Drive 3
1	1	Drive 4

b. Issue the Read Drive Status command by loading the Command Register (Address0) with a 80H.

c. Wait for either Command Completion bit or Command Reject bit to be set in the Controller Status Register (Address 0). Only one command per drive is allowed to be in process; thus, if a command for the assigned drive is in process all ensuing commands for that drive will be rejected until the command in process is completed.

d. When the Command Completion bit is set, the host system reads the Transaction Status Register (Result Register 0) to verify that the command is for the assigned drive. See the section on the Transaction Status Register.

If the Transaction Status Register contains the expected status, then the host would continue the sequence.

e. Read Result Register 1 (Address 3) which contains the selected drives status. The contents of this register is as follows:

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

Result Register 0

Bit	Name	Description
B0	Ready	The drive is up to speed, servo system is locked onto a servo track, and the unit is in a state to read, write, or seek.
B1	Seek Complete	This bit is set when a seek operation is completed.
B2	Seek Fault	A fault was detected during a seek operation.
B3	Cylinder Zero	The access arm is set to Cylinder 0.
B4	Busy	The drive is in process of executing a command.
B5	Drive Fault	A fault was detected during a write operation or a drive unsafe condition was detected.
B6	Write Protect	The head selected is write protected. Write protection is set by switches in the drive or when the drive is not sequenced up.
B7	Command Reject	Control or Register Load command received while drive is not ready, or improper command received.

f. Issue a Command Acknowledge to clear the Command Completion bit.

5. Sequence Down Command

7	6	5	4	3	2	1	0
1	0	0	0	0	0	0	1

Command

The Sequence Down Command causes the disc drive defined by the contents of Parameter Register 0 to position its heads over the landing zone. The spindle motor's dynamic braking is initiated. The drive will set its Write Protect status bit and clear its Ready Bit. When dynamic braking is initiated the Command Completion bit will be set with the drive status in Result Register 1.

6. Sequence Up-Return Command

7	6	5	4	3	2	1	0
1	0	0	0	0	0	1	1

Command

The Sequence Up-Return command will cause the disc drive defined by the contents of Parameter Register 0 to power-up its spindle motor. When the command is accepted by the selected drive the Command Completion bit is set and the drive status will be in Result Register 1. The operation is similar to that in Sequence Up-Wait command but the controller does not wait until the drive is up to speed and the heads positioned over Cylinder 0 before posting the command completion.

7. Sequence Up-Wait Command

7	6	5	4	3	2	1	0	
1	0	0	0	0	0	1	0	Command

The Sequence Up-Wait Command causes the disc drive defined by the contents of Parameter Register 0 to power its spindle motor. The disc drive will monitor the rotational speed of the disc and when it is at speed and stable, the drive will position it heads at cylinder zero. When this is completed the Command Completion bit will be set with the drive status in Result Register 1.

The Command sequence is similar to that previously discussed except this command will require about 30 seconds to complete.

8. Drive Restore Command

7	6	5	4	3	2	1	0	
0	1	0	0	0	0	0	0	Command

The Restore Command causes the access arm on the drive defined by the contents of Parameter Register 0 to be positioned over cylinder zero. If the drive is Sequence Down (spindle motor off) when the Restore command is issued, the controller will automatically Sequence Up the drive prior to doing the Restore. Therefore, when the host issues a command, it implies that the controller should automatically condition the drive to execute that command.

Upon completion of the disc's restore operation, the Command Completion bit will be set with the current cylinder MSB and Head in Result Register 1 and current cylinder LSB in Result Register 2.

The format of Result Registers is shown below:

7	6	5	4	3	2	1	0
0	H2	H1	H0	C11	C10	C9	C8

Result Register 1

where: H2, H1, H0 defined current selected head address C11, C10, C9, C8 are the upper binary bits of the current cylinder address.

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0

Result Register 2

where: C7 through C0 are the eight least significant bits of the current cylinder address.

10. Seek Command

7	6	5	4	3	2	1	0
0	1	0	R	0	0	0	1

Command

where: R is the Retry enable bit.

The Seek Command uses the drive address defined in Parameter Register 0 and the contents of Parameter Registers 1 and 2 for the target cylinder address. The format of Parameter Registers 1 and 2 is as follows:

7	6	5	4	3	2	1	0
0	0	0	0	C11	C10	C9	C8

Parameter Register 1

where: C11, C10, C9, C8 are the upper binary bits of the target cylinder address.

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0

Parameter Register 2

where: C7 through C0 are the eight least significant bit of the target cylinder address.

The controller will command the drive to seek to the target cylinder. When this is complete, the Command Completion bit will be set with the current cylinder MSB in Result Register 1 and current cylinder LSB in Result Register 2 as discussed in the Restore command section.

If the Retry bit is set, the seek will be retried if the first attempt is unsuccessful. This retry will be reported in the Transaction Status Register.

Also, Sequence Up is implied upon the receipt of this command if the selected drive is sequenced down when this command is received by the controller.

11. Write Data Command

7	6	5	4	3	2	1	0
0	1	0	R	0	0	1	0

Command

where: R is the Retry enable bit.

The Write Data command causes data to be written to the disc in accordance with the Parameters specified. The parameters specify which drive, which cylinder, which head, which logical sector, and how many contigious logical sectors. The command defines whether or not the write operation will be retried if the first attempt is unsuccessful. Also, Sequence Up and Seek are implied by this command. Thus, this complete set forms a powerful command.

The formats of the Parameter Registers are as follows:

7	6	5	4	3	2	1	0
0	0	0	0	0	0	D1	D0

Parameter Register 0

where: D1, D0 define the address of the selected drive.

7	6	5	4	3	2	1	0
0	H2	H1	H0	C11	C10	C9	C8

Parameter Register 1

where: H2, H1, H0 define the target head address and C11, C10, C9, C8 are the upper binary bits of the target cylinder address.

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0

Parameter Register 2

where: C7 through C0 are the eight least significant bits of target cylinder address.

7	6	5	4	3	2	1	0
0	S6	S5	S4	S3	S2	S1	S0

Parameter Register 3

where: S6 through S0 are the seven binary bits defining the target sector.

7	6	5	4	3	2	1	0
0	M6	M5	M4	M3	M2	M1	M0

Parameter Register 4

where: M6 through M0 are the seven binary bits defining the total number of consecutive logical sectors to be written.

The command execution sequence is described below.

a. Signal data request to the host and continue to request data until either the sector count is zeroed or the buffer is full.

b. If drive is not sequence-up, then the controller issues a Sequence Up command to drive and wait for drive READY or time-out.

c. If access arm is not over the desired cylinder, a seek is issued to the drive to position at the target cylinder.

d. If the desired head is not selected, then the appropriate head is selected.

e. Consecutive ID fields on the target track are read until a match is found between the recorded logical sector number and the desired sector number.

f. Then the data field is written from the buffer.

g. Then, the multiple sector count in Parameter Register 4 is decremented.

h. If the multiple sector count has terminated, then command is complete and the appropriate Result Registers are set according to the following format.

7	6	5	4	3	2	1	0
0	H2	H1	H0	C11	C10	C9	C8

Result Register 1

where: H2, H1, H0 define the current selected head address
C11, C10, C9, are the upper binary bit of the current cylinder address

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0

Result Register 2

where: C7 through C0 are the eight least significant bits of target cylinder address.

7	6	5	4	3	2	1	0
0	S6	S5	S4	S3	S2	S1	S0

Result Register 3

where: S6 through S0 define the number of the last sector.

7	6	5	4	3	2	1	0
0	M6	M5	M4	M3	M2	M1	M0

Result Register 4

where: M6 through M0 indicate the residual sector count (non-zero if an un-recovered error occurred).

i. If the multiple sector count is non-zero, the sector number is incremented (modulo the number of sectors per track), then the buffer contents is checked. If Buffer is empty, then go to Step a. and continue. However, since the buffer is 1024 bytes, and sectors may be 128, 256, or 512 bytes; the ensuing sector data may be resident in the buffer. If the sector number is zero, then the next head is selected unless we are currently on the last head of the cylinder. If not, then go to Step e. and continue. If at last head, then the head address is set to zero and the cylinder address is incremented. Then go to Step c. and continue.

The Command Completion bit is set whenever the complete command is completed or an un-recovered error occurs.

12. Read Data Command

7	6	5	4	3	2	1	0	
0	1	0	R	0	0	1	1	Command

where: R is the Retry enable bit.

The Read Data command causes data to be read from the disc in accordance with the parameters specified. These parameters are of the same format as defined in the Write Data command discussion.

The command execution sequence is as described below:

a. If drive is not sequenced up, then the controller issues a Sequence Up command to the selected drive.

b. If access arm is not over the desired cylinder, a seek command is issued to the drive to position over the desired cylinder.

c. The desired head is selected.

d. Consecutive ID fields on the target track are read until a match is found between the recorded logical sector number and the desired sector number.

e. Then the data field is read from the disc into the buffer.

f. Then, the multiple sector count in Parameter Register 4 is decremented.

g. If the multiple sector count is zero, then a data transfer request from the controller to the host is signalled. The controller waits for the data transfer to complete and when complete, the Command Completion bit is set and the Result Registers are updated. The format of the Result Registers is a defined in the Write Data command discussion.

h. If the multiple sector count is non-zero, then the sector count is updated, also head and cylinder address are updated as required. If Buffer space is available for the next sector then go repeat step b, and continue.

i. If buffer is full, then request a data transfer operation as discussed in Step g. When transfer is done, go repeat Step b. and continue.

13. Write ID Command

7	6	5	4	3	2	1	0
0	1	0	R	0	1	0	1

Command

This command causes the four byte ID field to be written at the physical sector location specified. The logical sector number is selected from the buffer data. The command execution sequence is similar to the Write Data command with the following exception. The writing is enabled when the physical sector count (number of sector marks past index) matches the sector number.

Command Completion is set when the multiple sector count is zero.

14. Read ID Command

7	6	5	4	3	2	1	0
0	1	0	R	0	1	1	0

This command causes the four byte ID field to be read from the physical sector location specified. The command execution sequence is similar to the Write ID Command except the ID fields are read.

Command Completion is set when the multiple sector count is zero.

15. Read ID Immediate Command

7	6	5	4	3	2	1	0
0	1	0	R	0	1	1	1

Command

This command causes the ID field at the next sector mark encountered to be read and transferred to the buffer. Only Parameter Register 0 containing the selected drive address is required for this command.

16. Verify Data Command

7	6	5	4	3	2	1	0
0	1	0	0	0	1	0	0

Command

This command causes the data to be read from the disc in accordance with the parameters specified except no data will be transferred to the host. The CRC will be checked in order to verify that the data was written without disc generated errors.

The execution of this command is similiar to the Read Data command except no data is transferred.

17. Verify ID Command

7	6	5	4	3	2	1	0
0	1	0	0	1	0	0	0

Command

This command causes the ID field to be read from the disc in accordance with the parameters specified except no data will be transferred to the host. The ID fields CRC will be checked in order to verify that the ID was written without a disc generated error.

The execution of this command is similiar to the Read ID command except no data is transferred.

18. Read Defect Field Command

7	6	5	4	3	2	1	0
0	1	0	R	1	0	0	1

Command

This command causes the skip defect field to be read from the disc in accordance with parameters specified. The execution of this command is similiar to the Read ID command except the skip defect field is read instead of ID's.

19. Write Defect Field Command

7	6	5	4	3	2	1	0
0	1	0	R	1	0	1	0

Command

This command causes the skip defect field to be written to the disc in accordance with the specified parameters. The execution of this command is similiar to the Read Defect Field command except the skip defect field is written instead of read.

20. Format Disc Command

7	6	5	4	3	2	1	0
1	0	1	0	D	0	0	0

Command

Where D is defect mapping enable.

This command is used to format the disc. It performs a complete disc format operation including, if defect mapping is enabled, assigning alternate sectors for each sector containing a defect. The defective areas on the disc are determined by the information contained in the PRIAM skip Defect Records recorded at the beginning of each track.

The Parameter Registers format is as follows.

7	6	5	4	3	2	1	0
0	0	0	0	0	0	D1	D0

Parameter Register 0

where: D1, D0 define the selected drive.

7	6	5	4	3	2	1	0
0	H2	H1	H0	C11	C10	C9	C8

Parameter Register 1

where: H2, H1, H0 defines the starting head address and C11, C10, C9, C8 are the most significant binary bits of the starting cylinder address.

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0

Parameter Register 2

where: C7 through C0 are the least significant binary bits of the starting cylinder address.

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Parameter Register 3

Must be set to zero.

21. Format Cylinder Command

7	6	5	4	3	2	1	0
1	0	1	0	0	0	0	1

Command

This command functions similarly to the Format Disc command except only a single cylinder is formatted.

22. Format Track Command

7	6	5	4	3	2	1	0
1	0	1	0	0	0	1	0

Command

This command functions similarly to the Format Disc command except only a single track is formated

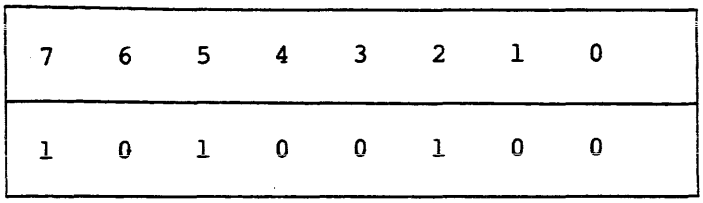
23. Verify Disc Command

7	6	5	4	3	2	1	0
1	0	1	0	0	0	1	1

Command

This command is used to verify that a disc is completely and correctly formatted. Every ID and sector from the starting address is read and its CRC is checked. The parameters are as defined in the Format Disc command discussion.

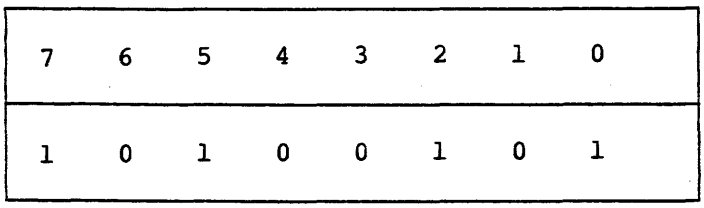
24. Verify Cylinder Command



7	6	5	4	3	2	1	0	
1	0	1	0	0	1	0	0	Command

This command functions similarly to the Verify Disc Command except only a single cylinder is verified.

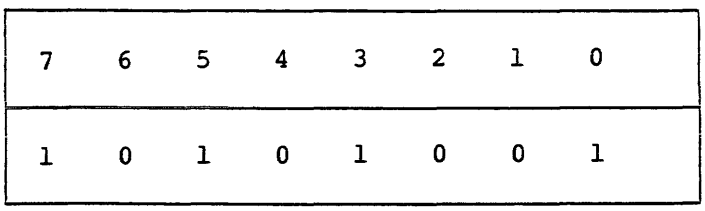
25. Verify Track Command



7	6	5	4	3	2	1	0	
1	0	1	0	0	1	0	1	Command

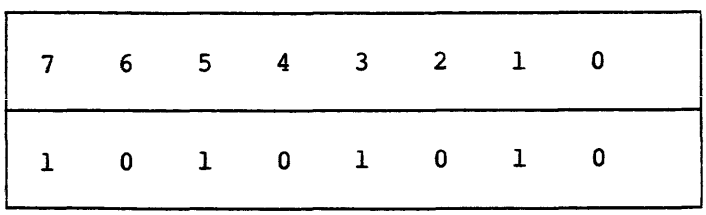
This command functions similarly to the Verify Disc Command except only a single track is verified.

26. Specify Bad Track



7	6	5	4	3	2	1	0	
1	0	1	0	1	0	0	1	Command

27. Specify Bad Sector



7	6	5	4	3	2	1	0	
1	0	1	0	1	0	1	0	Command

D. Error Technique

If an error occurs during the execution of the command and the retry feature is selected (i.e., retry enable bit is set to one), the Controller will automatically retry the command.

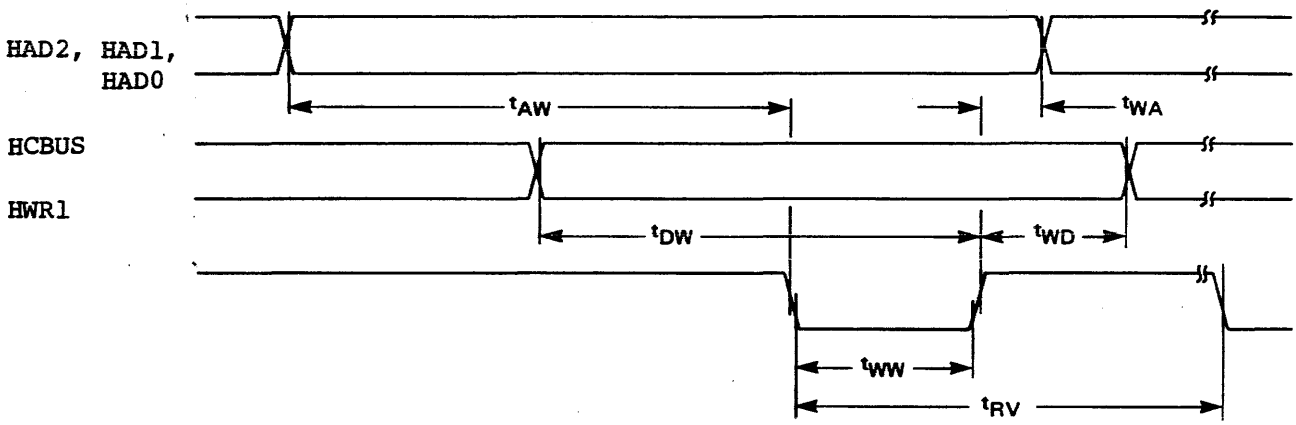
1. DMA Data Transfer

The DMA Data Transfer is performed through the use of the Controller HCBUS. See figures 2, 3, and 4.

2. Programmed I/O

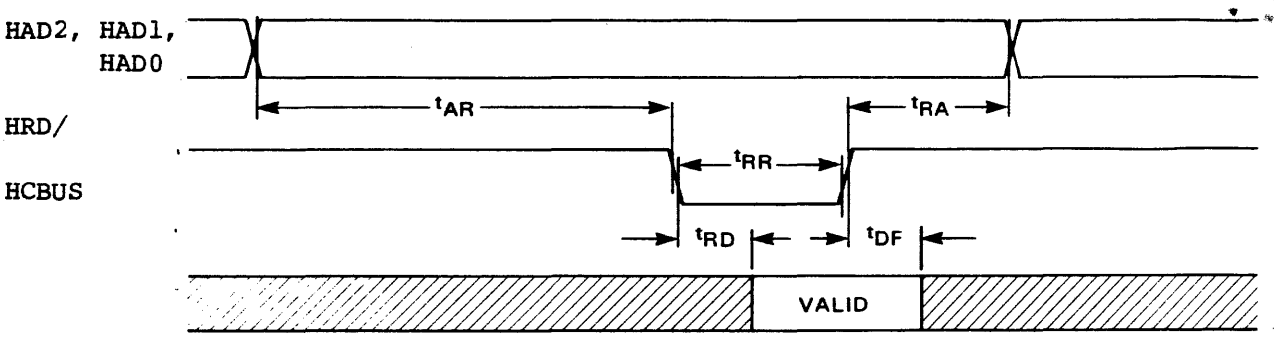
The programmed I/O method of data transfer is performed under the direct control of the host processor. The Controller status register indicates when a data byte should be read or written. The host reads or writes the data byte through the control register interface described previously.

The Controller fills the data buffer prior to initiating a buffered mode data transfer to the disc. During a buffered mode read from the disc the data is transferred to the host.



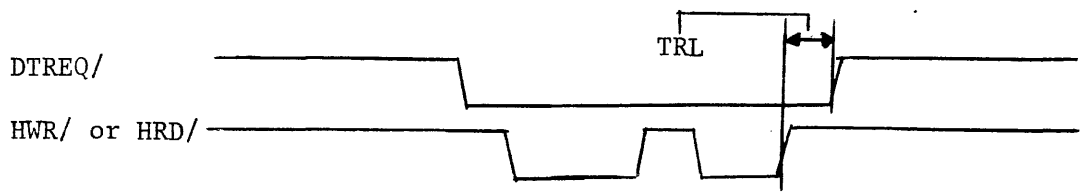
SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{AW}	Address stable before WR	60		ns
t_{WA}	Address hold time for WR	30		ns
t_{WW}	WR pulse width	250		ns
t_{DW}	Data set up time for WR	60		ns
t_{WD}	Data hold time for WR	30		ns
t_{RV}	Recovery time between WR	500		ns

Figure 2. Register Write AC Characteristics



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{AR}	Address stable before RD	60		ns
t_{RA}	Address hold time for RD	30		ns
t_{RR}	RD pulse width	250		ns
t_{RD}	Data delay from RD		120	ns
t_{DF}	RD to data floating	10	40	ns

Figure 3. Register Read AC Characteristics



SYMBOL	PARAMETER	MIN	MAX	UNITS
T_{RL}	Data Transfer Release		200	ns

Figure 4. Data Request AC Characteristics

TABLE 4. Defect Record Format

DECIMAL LOCATION	DATA
000-022	Gap 1 - 23 Zeros
023	Defect Record Sync (FB Hex)
024	1st Address MSB
025	2nd Address LSB
026	2nd Address MSB
027	2nd Address LSB
028	3rd Address MSB
029	3rd Address LSB
030	Checksum MSB
031	Checksum LSB
032	Fill (Zero)
033	Fill (Zero)

d. ID Gap (Gap 2)

The ID Gap, or Gap 2, separates each successive Identification Field from its Data Field. It contains 11 bytes of zeros.

e. Data Field

Following Gap 2, the Data Field consists of 133, 261, 517, or 1029 bytes depending on the selected data length. The first byte is the data sync (hexadecimal pattern FD), while the last four bytes consist of two bytes of CRC and two bytes of zeros for filling.

f. Pre-Index Gap (Gap 3)

The Pre-Index Gap, or Gap 3, is used only once on a track. It appears at the end of the last data field and persists until INDEX/. This gap contains zeros.

F. Disc Format

The disc format is described in the following two sections. The first section discusses the sector format used by the Controller. The second section presents how defect mapping is performed.

1. Sector Format

The soft sector format shown in Figure 5 is used by the Controller.

Each track starts with an INDEX/ pulse, which corresponds to a certain area of the servo track. The servo track also provides rotational position information for the generation of SECTOR/ pulses. A sector pulse precedes each record and successive records are separated by gaps within which the sector pulses occur.

a. Pre-Record Gap (Gap 1)

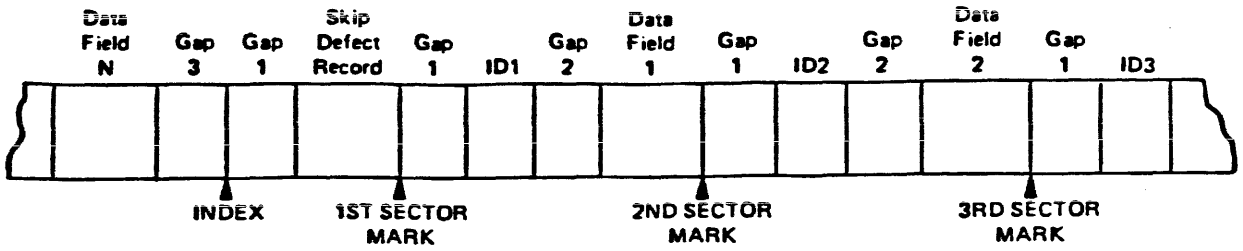
The Pre-Record Gap, or Gap 1, appears at the beginning of every record. It consists of 23 bytes of zeros. The length of Gap 1 never varies. The first Gap 1, after INDEX/, is followed by the Skip Defect Record. All other Gap 1's, after SECTOR/ pulses, are followed by ID records.

b. Skip Defect Record

The Skip Defect Record (Table 4) consists of 11 bytes: a Data Sync using the hexadecimal pattern FB, the physical address of the first defect using two bytes, the physical address of the second defect using two bytes, the physical address of the third defect using two bytes, a checksum across the previous six bytes using two bytes, and fill characters of zeros using two bytes.

c. ID Field

This Identification Field uses 9 bytes: an ID sync using the hexadecimal pattern F9, the head address and high order cylinder address of one byte, the low order cylinder address of one byte, the sector number of one byte, a sector length and flag bytes, two CRC (cyclic redundancy check) bytes, and two bytes of zeros for filling. The cylinder and head address, along with the sector number, verify that the drive has addressed the correct track and sector.



Index:	Derived from servo track	
Gap 1:	Zeros	23 Bytes
Skip Defect Record:	Data Sync, FB Hex	1 Byte
	1st defect address	2 Bytes
	2nd defect address	2 Bytes
	3rd defect address	2 Bytes
	Checksum	2 Bytes
	Fill characters - zeros	2 Bytes
Sector Mark:	Derived from INDEX and servo clock	
ID Field:	ID Sync, F9 Hex	1 Byte
	Sector address	1 Byte
	Head and high cylinder address	1 Byte
	Low order cylinder address	1 Byte
	ID Control	1 Byte
	CRC	2 Bytes
	Fill characters - zeros	2 Bytes
Gap 2:	Zeros	11 Bytes
Data Field:	Data Sync, FD Hex	1 Byte
	Data	128,256,512,or1024 Bytes
	CRC	2 Bytes
	Fill characters - zeros	2 Bytes
Gap 3:	Zeros (Size depends on data field size)	

Figure 5. Soft Sector Format

G. Defect Mapping

During the operation of the Format command the Controller may encounter a defective sector on a track. The defect mapping capabilities of the Controller allow the Controller to assign alternate areas for the defective areas. The Controller creates the defect map described in the next section during the Format operation. Each PRIAM drive has an area reserved for alternate sectors.

Table 5 lists the various soft sector formats.

TABLE 5. Soft Sector Format Information

Data Field Length (bytes)	Sector Length	Sectors Per Track	Gap 1 (bytes)	Gap 2 (bytes)	Gap 3 (bytes)	Data Per Track (bytes)	Data Capacity (bytes)	Percent Utilization (bytes)
128	176	113	23	11	50	14,464	24,082,560	72.4%
256	304	65	23	11	178	16,640	27,705,600	83.3%
512	560	35	23	11	338	17,920	29,836,800	89.7%
1024	1072	18	23	11	642	18,432	30,689,280	92.3%

Table 6 describes the sector format.

TABLE 6. Sector Format Summary

Logical Size	Physical Size	Sector/Track	Switch Setting
182	192	104	5,6
256	320	62	4,6
512	576	34	3,6
1024	1088	18	2,6

1. Defect Map Format

The Defect Map is written on the last head of the last cylinder. For example the Controller will write the Defect Map on cylinder 560 head two of the DISKOS 3350 drive. If the last cylinder is defective the Controller will decrement the head and cylinder addresses until a good track is found for the Defect Map. The format of the Defect Map is displayed in Table 6.

When a defective record is accessed during a disc command the Controller uses the defect map to locate the alternate sector.

TABLE 7. Defect Map Format

Location	Description
0, 1	Set to F5 E5-defect map flag.
3	Disc record size 0 = 128 1 = 256 2 = 512 3 = 1024
4+ (End of Record - 4)	Defect record addresses (see Table 7).
End of Record	CRC

TABLE 8. Defect Record Address

Location	Description
0	Defect Cylinder MSB and Head
1	Defect Cylinder LSB
2	Defect Sector Number
3	Alternate Cylinder MSB and Head
4	Alternate Cylinder LSB
5	Alternate Sector Number