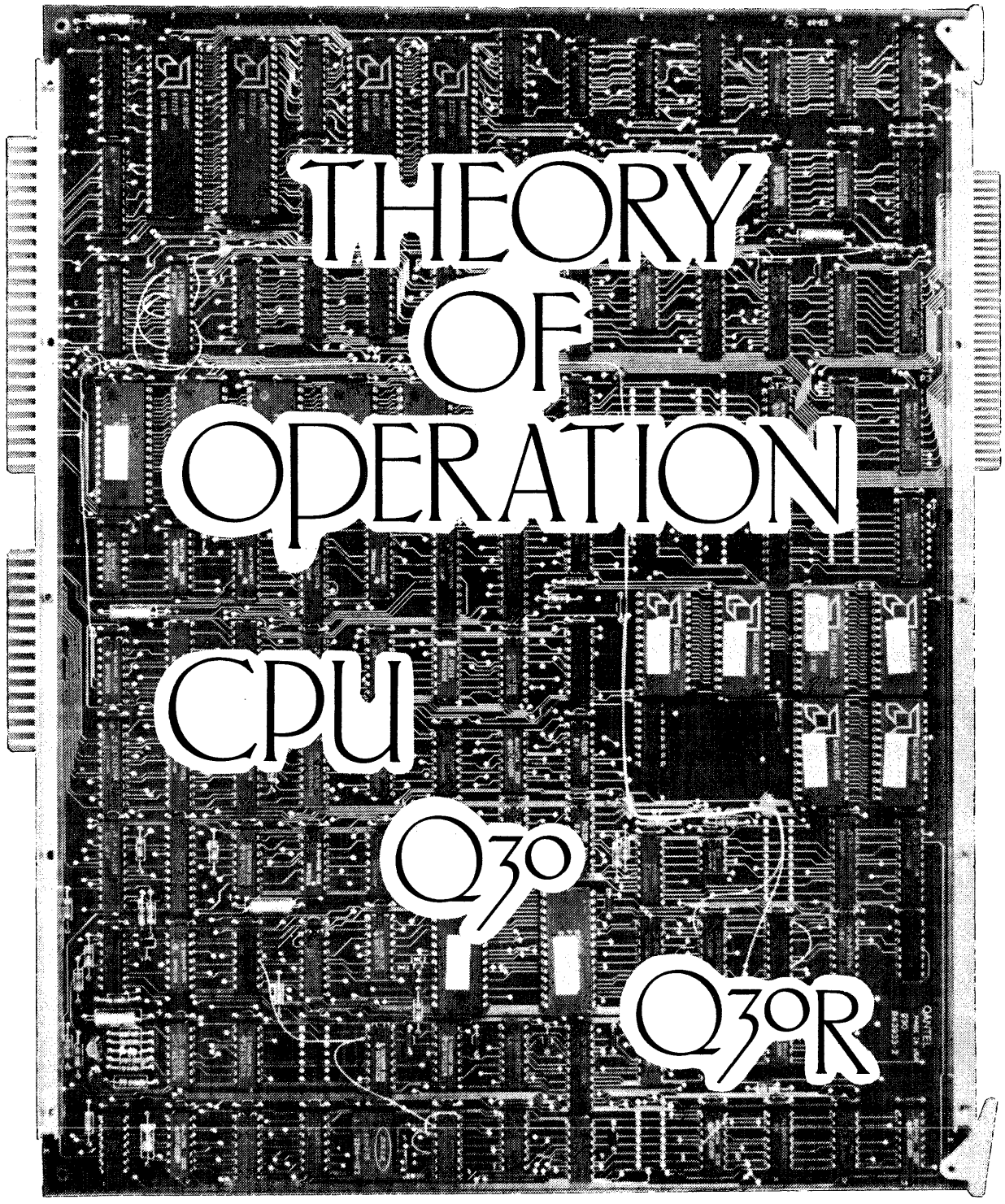
MDS MOHAWK DATA SCIENCES

SERVICE DIVISION



THEORY OF OPERATION

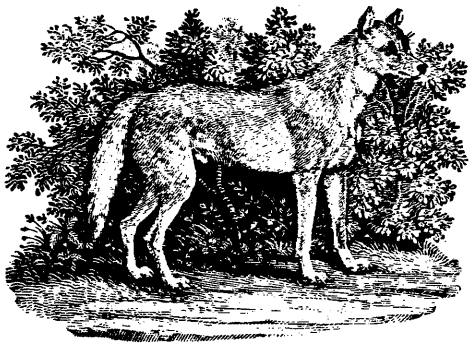
CPU Q30 Q30R

M-4908
(TD-4255)

TECHNICAL MANUAL

CPU

Q30 Q30R



TECHNICAL MANUAL TD-4255

ABSTRACT

This manual describes MDS Qantel's Q30 (six layer) and Q30R (four layer) single board CPU. Included are: CPU architecture, microcode formats, a gate-by-gate hardware explanation of the logic diagrams, timing diagrams, and FPLA equations.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

1.1 GENERAL DESCRIPTION

The Q30 is a register-oriented Central Processing Unit. It is a single board CPU, utilizing bipolar chip-slice microprocessing elements, field programmable logic arrays (FPLA), and a pipelined architecture. The standard Qantel instruction set is interpreted by ROM microcode residing on the CPU assembly. The Q30 is an improved version of the Q29 CPU. It has an extended microword which eliminates some of the FPLA decoding delays found in the Q29. Almost all the microinstructions are at least one timing state shorter than their Q29 equivalents and the master CPU clock runs at a slightly higher frequency than used by the Q29 CPU.

The Q30 CPU is used by all models of the MDS Qantel System 40 Series. It is also possible to upgrade 200/300 Series Systems, 2X Series Systems, 1400 Series Systems, and 900 Series Systems by installing the proper backplane. Please refer to the Installation Instructions for the Q30 Enhancement Kits listed in the Related Documents Section below.

1.2 RELATED DOCUMENTS

The following is a selected list of Q30 and Q30R documents available from the MDS Qantel Drafting Department.

D32136 --- Q30 Logics
D32155 --- Q30R Logics
A32142 --- Backplane Pin Listing BP6L and BP6S
A42243 --- INSTR-1 FPLA Listing
A42244 --- INSTR-2 FPLA Listing
A42246 --- STATUS FPLA Listing

RELATED DOCUMENTS LIST (continued)

A44000 --- BUS/CTL FPLA Listing A44001 --- 30TMG-1 FPLA Listing A44002 --- 30TMG-2 FPLA Listing A44003 --- 30 MISC FPLA Listing A42247 --- Programmed PROM7 Specification D43933 --- Q30 PCB Fabrication D44086 --- Q30R PCB Fabrication

Installation instructions for the Q30 Enhancement Kits are available from the MDS Service Documentation Distribution Office.

TD-4027 -- Upgrading 1400 Series Systems TD-4028 -- Upgrading 2X Series Systems TD-4029 -- Upgrading 900 Series Systems TD-4030 -- Upgrading Series 200/300 Systems

2.0 Q30 BASICS

This section deals with the basic architectural concepts of the Q30. The 2901B and FPLA integrated circuits are discussed, followed by an expanding sequence of block diagrams showing the relationship between the major circuit networks in the Q30 architecture. The microcode is then explained in the following chapter. Chapter 2 is intended to highlight the architectural concepts just enough to make a detailed explanation of the microcode meaningful. It is imperative that the reader thoroughly comprehend the Q30 microcode before attempting an in-depth study of Q30 CPU operation.

2.1 THE 2901B MICROPROCESSING ELEMENT

The Q30 architecture supports four cascaded 2901B bit slice microprocessor devices. Each 2901B is a 4 bit wide processing element containing a 16 location register file, a high speed ALU, and all the necessary decoders and multiplexers for ALU function decoding, data routing, and shifting operations.

A block diagram of the internal circuitry of the 2901B is given is Figure 2-1. The 16 location register file has 2 output ports permitting 2 file registers to be accessed simultaneously. The A port and B port register addresses specify the location of the registers in the register file.

Data outputted from the register file is captured and held by the A latch and B latch when the clock input is driven low. When the clock input is high, the A latch and B latch are transparent; Their outputs follow the data present at their inputs.

Nine Instruction Control inputs (I_0-I_8) are formatted as three 3 bit fields (see Table A). The I_0-I_2 inputs are used to select the data sources for the R and S inputs of the ALU. The I_3-I_5

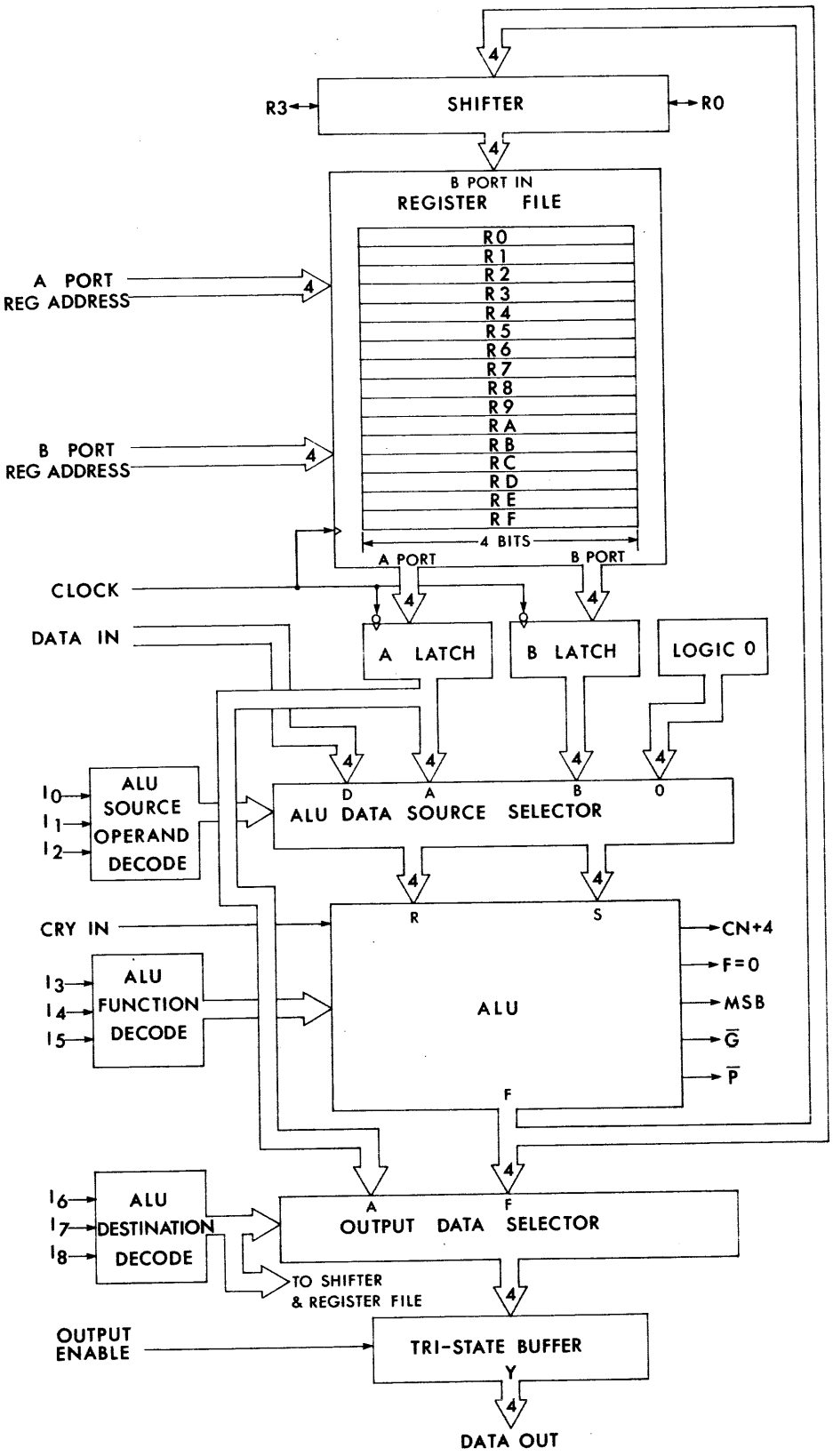


FIGURE 2-1

2901B INTERNAL CIRCUITRY

ALU SOURCE OPERAND CONTROL					
MICRO CODE				ALU SOURCE OPERANDS	
I_2	I_1	I_0	OCTAL CODE	R	S
L	L	H	1	A	B
L	H	H	3	Ø	B
H	L	L	4	Ø	A
H	L	H	5	D	A
H	H	H	7	D	Ø

ALU FUNCTION CONTROL				
MICRO CODE				ALU FUNCTION
I_5	I_4	I_3	OCTAL CODE	
L	L	L	0	R Plus S
L	L	H	1	S Minus R
L	H	L	2	R Minus S
L	H	H	3	R OR S
H	L	L	4	R AND S
H	H	L	6	R EX-OR S
H	H	H	7	R EX-NOR S

ALU DESTINATION CONTROL								
MICRO CODE				RAM FUNCTION		Y	RAM SHIFTER	
I_8	I_7	I_6	OCTAL CODE	SHIFT	LOAD	OUTPUT	RAM_0	RAM_3
L	L	L	0	X	NONE	F	X	X
L	H	L	2	NONE	F→B	A	X	X
H	L	L	4	DOWN	F/2→B	F	F_0	IN_3
H	H	L	6	UP	2F→B	F	IN_0	F_3

TABLE A

inputs are used to specify the ALU function. The I_6-I_8 inputs are used to select the destination for the resutant of a completed operation.

The ALU in the 2901B can receive its input operands from: the contents of any combination of register pairs, direct data inputted to the 2901B, or forced zeros multiplexed onto the R or S inputs of the ALU. Seven ALU functions are employed: three arithmetic and four logicals. The data outputted from the 2901B (Y output pins) may be the resultant data emerging from the F outputs of the ALU or the contents of the A latch.

If the ALU resultant is placed in the register file, the destination register address must be supplied via the B port register address inputs. The register file input port has shift capability. The resultant of an ALU operation may be divided by 2 or multiplied by 2 via the shifter before being loaded into the

register file. Note, when the ALU resultant is placed into the register file with no shift function, the contents of the A latch is placed on the 2901B data outputs (Y pins). During shift operations, the unshifted ALU resultant is outputted by the 2901B. The ALU in the 2901B generates 5 status signals that are used in the Q30. These include: ALU resultant equals zero (F=Ø), most significant bit (F3), the carry out signals (CN+4), carry generate ($\overline{G}$), and carry propagate ($\overline{P}$). Carry Generate and Carry Propagate are designed for use with the Carry Lookahead Generator IC. This technique permits carries to be anticipated before the ALU operation is completed, relieving the requirement for the more significant ALU slices to wait for a ripple carry to propagate through all the cascaded slices.

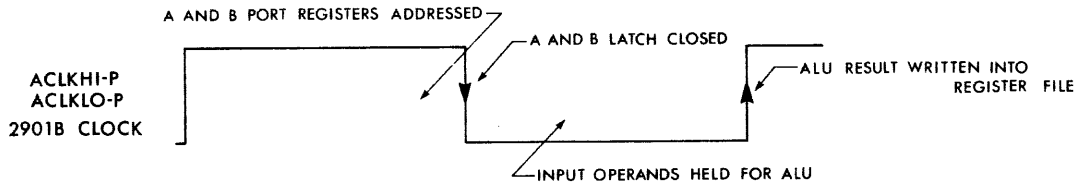


FIGURE 2-2

2901B CLOCK

The 2901B clock signal controls the internal A latch and B latch, and specifies when data is written into the register file. When the clock signal is high the A and B latch are transparent. If the register file addresses and the I control signals are stable, the register files may be accessed and the ALU will function without the clock dropping low. When the resultant of an ALU operation is to be deposited into a register file, the B port register address must specify the register. The data will be written on the positive-going edge of the clock.

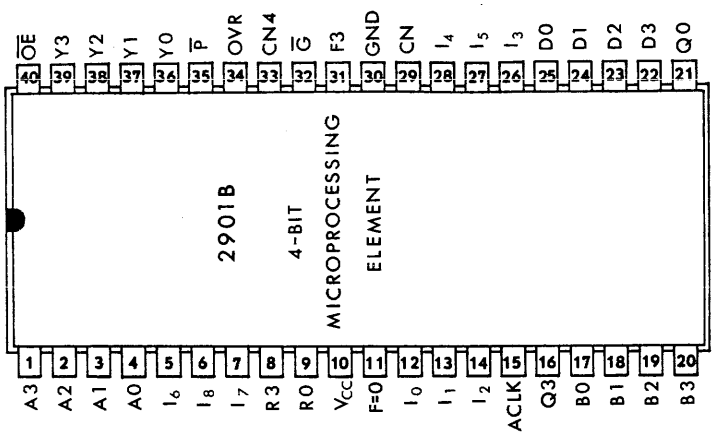


TABLE B

AØ-A3 A PORT REGISTER ADDRESS INPUTS used to specify one of the 16 register file locations, causing its contents to be routed to the A port output of the register file.

I_6-I_8 INSTRUCTION CONTROL INPUTS used to specify the destination for the resultant of an ALU operation, specifies the source of the data outputted from the 2901B (pins YØ-Y3) and defines any shift operation (see Table A).

R3 MSB RAM SHIFTER The most significant bit of the shifter situated on the data inputs of the register file. Serves as an input on shift right operations and an output on shift left operations. When the I_6-I_8 inputs do not specify a shift operation, R3 enters tri-state mode.

Vcc POSITIVE SUPPLY TERMINAL +5V power supply connection.

F = Ø ZERO OUTPUT an ALU status signal indicating the resultant of an ALU operation equals zero.

I_0-I_2 INSTRUCTION CONTROL INPUTS used to specify the sources of the input operands to the ALU (see Table A).

ACLK CLOCK INPUT used to control the A latch and B latch, and specifies the time when data is written into the register file (see Figure 2-2).

Q3 MSB Q SHIFTER most significant bit of the Q shifter. The Q register and its shifter are not used in the Q30 design and are thus omitted from Figure 2-1.

BØ-B3 B PORT REGISTER ADDRESS INPUTS used to select one of the 16 register file locations, causing its contents to be presented to the B port output of the register file and acting as a destination pointer when data is written into the register file.

QØ LSB Q SHIFTER least significant bit of the Q shifter. The Q register and its shifter are not used in the Q30 design and are thus omitted from Figure 2-1.

DØ-D3 DIRECT DATA INPUTS a 4-bit slice of data entering the 2901B which may be selected as one of the input operands of the ALU by the I_0-I_2 Instruction Control Inputs.

I_3-I_5 INSTRUCTION CONTROL INPUTS used to specify what function the ALU will perform (see Table A).

CN CARRY INPUT the carry in to the ALU.

GND GROUND TERMINAL ØV power supply connection.

F3 MOST SIGNIFICANT BIT an ALU status signal displaying the state of the most significant bit of the resultant of an ALU operation.

$\overline{G}$ CARRY GENERATE an ALU status signal routed to the carry lookahead generator, indicates (even before the ALU operation begins) that the most significant bits of the ALU input operands are high and a carry is inevitable.

CN4 CARRY OUT the carry out from the ALU.

OVR OVERFLOW an ALU status signal, not used in the Q30.

$\overline{P}$ CARRY PROPAGATE an ALU status signal routed to the carry lookahead generator indicates (by examination of the ALU input operands) there will be a carry propagated out of this 2901B if a carry enters from a less significant ALU slice.

YØ-Y3 DATA OUTPUTS four bits of data are outputted when these tri-state lines are enabled. Data may be outputted from the ALU or the contents of the A latch may be outputted. The source of the output data is specified by I_6-I_8 (see Table A).

$\overline{OE}$ OUTPUT ENABLE when logically high the YØ-Y3 outputs are disabled and enter tri-state mode.

RØ The least significant bit of the shifter situated on the data inputs of the register file. Serves as an input on shift left operations and as an output on shift right operations. When the I_6-I_8 inputs do not specify a shift operation, RØ enters tri-state mode.

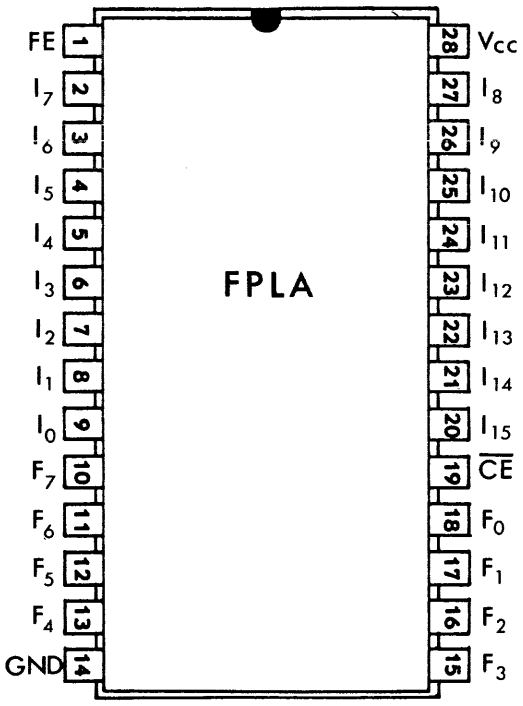


FIGURE 2-3

2.2 FIELD PROGRAMMABLE LOGIC ARRAYS

The pin configuration of the Field Programmable Logic Arrays (FPLA) is shown above. The Q30 uses the FPLA for instruction decoding, terms collection, and time state sequencing. Note the similarity to a PROM. The FPLA has 16 address inputs (I_0-I_{15}), 8 outputs (F_0-F_7), a chip enable input ($\overline{CE}$), and a fuse enable input (FE). The fuse enable input is used during programming. Once programmed, no circuit connection is necessary to pin 1.

The FPLA is a fuseable link, nichrome technology PROM. However, due to differences in the input structure, the FPLA may be thought of as a conditionally addressable PROM. While the FPLA is a relatively small PROM in terms of storage, it may (when properly programmed) select as active locations any unrelated address found within the 64K realm of its 16 bit address.

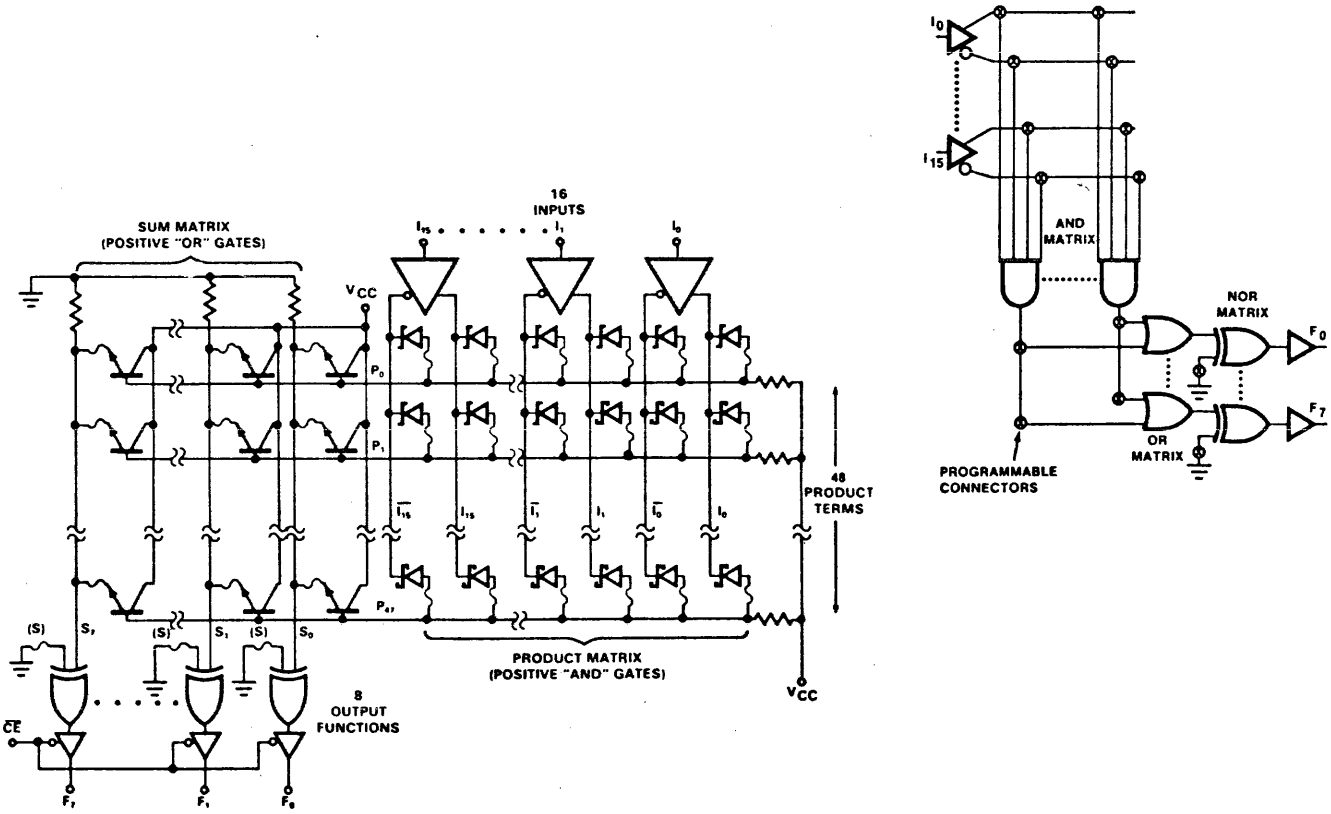


FIGURE 2-4

FPLA EQUIVALENT CIRCUITS

The FPLA is basically a collection of And/Or, Exclusive-Or combinational logic elements tied together with fuseable link programmable connectors. By selectively removing connectors (blowing fuseable links by exceeding their current limit) any combination of FPLA output signals can be programmed to enter their active state upon receiving a specific combination of address bits. The address bit inputs can be programmed to be active high, active low, or not programmed to remain as don't care states. The outputs of the FPLA may also be programmed to respond active high or active low by the removal or preservation of the fuseable link that applies Ø volts to one input of the Exclusive-Or gate on each of the 8 outputs (see Figure 2-4).

The 16 address inputs enter buffers with differential outputs. Each of these 32 outputs are routed into a product matrix of 48 thirty-two input And gates. A programmable connector is situated

at each input of all the And gates. The outputs of the 48 And gates are routed through programmable connectors to a sum matrix of eight 48 input Or gates.

The eight outputs of the sum matrix then pass through Exclusive-Or gates which may be programmed to be non-inverting by opening the programmable connectors at their inputs that connect to ground. The outputs then exit the chip through tri-state buffers.

A total of 48 unique product terms each defining an active 16 bit input address may be programmed into the FPLA. This is performed by removing unwanted connectors in the product matrix, routing the selected inverted or non-inverted outputs of the input buffers to the inputs of each of the 48 And gates. Since some bits of each product term can be left intentionally unprogrammed (both the connectors from the inverting and non-inverting side of an input buffer are preserved at one of the And gates). The outputted logic function then becomes active from more than one specified address. Thus, one product term entered into the And matrix of the FPLA may provide active output signals during numerous address states.

A particular product term when met by its corresponding input address may drive from only one to all eight of the output lines active, depending on what connectors have been preserved in the sum matrix where a logical Or of the 48 product terms is performed for each output bit. Since all 48 product terms programmed into the And matrix are presented with the input address simultaneously, up to 8 different product terms may be satisfied by the input address at once, each driving one of the 8 output signals active.

2.3 COMPUTER CONTROL UNIT

The portion of the Q30 hardware that fetches microcode from the microprogram ROM is called the Computer Control Unit (CCU). The architecture utilized by the CCU portion of a computer determines the speed and versatility of the machine. Since all routines from machine initialization through macroinstruction fetch, down to the specific algorithms for executing the fetched machine instructions are built from assemblages of microinstructions, a CPU design basically unfolds from its CCU section.

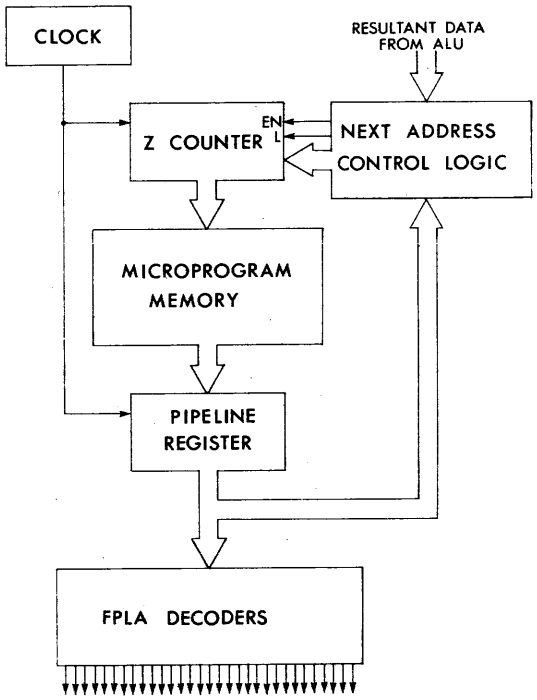


FIGURE 2-5

A simplified diagram of the CCU portion of the Q30 architecture is shown above. The Z counter addresses the microprogram memory where the CPU firmware resides. A pipeline register (a holding register) captures the data outputted from the microprogram memory.

In this example, the clock signal is routed to the clock input of both the Z counter and the pipeline register. Assume the Z counter is outputting a stable address to the microprogram memory and the contents of that location has propagated to the outputs of the memory. The positive-going edge of the clock loads the outputted microword into the pipeline register, and simultaneously clocks the Z counter causing it to increment. Incrementing the Z counter does not affect the data being loaded into the pipeline register because a finite period of time passes before the Z counter's outputs assume the incremented state. Another finite period of time passes before the newly accessed location propagates to the outputs of the microprogram memory. Therefore, the maximum frequency that the Z counter and pipeline register can be clocked is governed only by the propagation times of the Z counter and the microprogram memory added to the required set-up time required at the inputs of the pipeline register. These delays amount to less than 50 nSec in the Q30 allowing the clock oscillator to run an 11MHz microcycle (providing 90.9 nSec. processor time states).

While the Z counter constantly receives the free-running clock pulses, it is not always incremented every clock cycle. The next address control logic can inhibit the Z counter. In this case, the contents of the same microprogram memory location is repeatedly loaded into the pipeline register by the clock. On conditional branch instructions, if the test conditions are met the branch address (which originates as part of a microword resident in the microprogram memory) is parallel loaded into the Z counter. Likewise, an unconditional branch instruction without having to make a condition test, parallel loads the Z counter with a branch address that originates as part of the microinstruction. The next address control logic also has the ability to perform a multi-way branch.

With the multi-way branch feature, the resultant data from an ALU operation provides the branch address that is loaded into the Z counter. This provides a means for quickly decoding op-codes and variants of the machine language. For example, tables of unconditional branch instructions (each pointing to the starting address of a firmware routine for a machine instruction) are located in the microprogram ROM. By simply adding the specific machine instruction opcode to the table starting address and parallel loading the result into the Z counter, the Z address points to the appropriate unconditional branch instruction in the branch table. Upon execution of the unconditional branch, the Z counter will point to the starting address of the firmware routine for the specific opcode group of machine instruction requested.

The FPLA devices perform microinstruction decoding as well as the generation of control and timing signals. The pipelined architecture overlaps the decoding of the the microinstruction in the pipeline register with the fetching of the next microword from the microprogram memory.

2.4 MICROCODE INSTRUCTION FORMATS

The Q30 microprogram ROMs are 24 bits wide. The microinstructions reside in the ROM, their lengths being, 1, 2, or 3 sequential locations. As shown in Figure 2-6, the single, double, or triple microword instructions fall into one of four coding formats. A triple microword instruction thus requires 3 microinstruction fetch cycles. The microwords of constant data and condition code/branch address utilize only 16 bits of the 24 bit ROM microword.

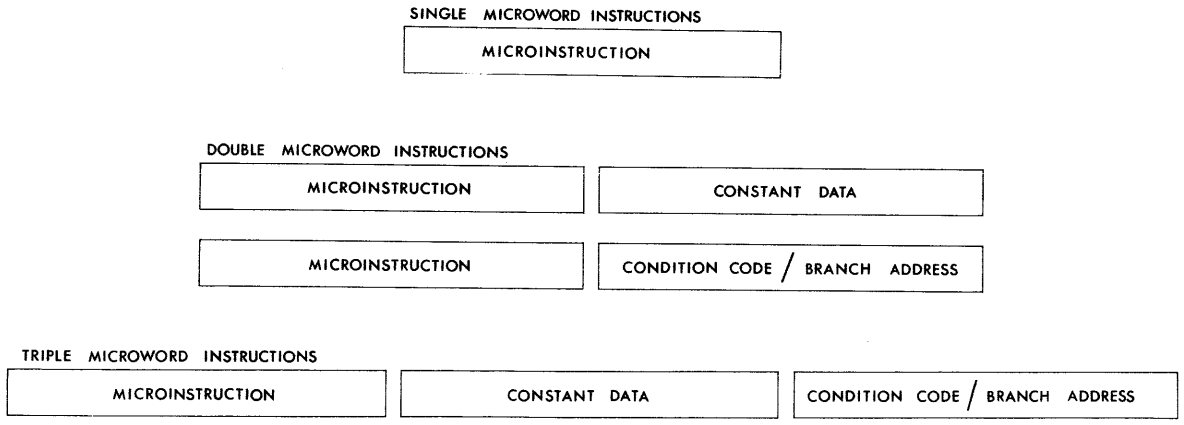


FIGURE 2-6

MICROCODE INSTRUCTION FORMATS

2.5 INSTRUCTION REGISTERS

A more detailed illustration of the CCU architecture is now given in Figure 2-7. Three instruction registers (E, C, and Z) have been added and perform as pipeline registers. The E register will receive the microinstruction portion of all single, double, or triple microword instructions. The E register presents some of the microinstruction microword bits to the FPLAs for decoding, while, some of the microinstruction microword bits are used directly from the E register as decoded signals (the Extention bits). The C register receives the constant data microword of a double or triple microword instruction. The constant data can then be used as one of the input operands to the ALU or loaded into the register file. The Z register receives all condition code/branch address microwords. The condition code bits are routed to the condition code multiplexer which selects the requested condition status bit. If the tested condition is present, the branch address held in the Z register is parallel loaded into the Z counter.

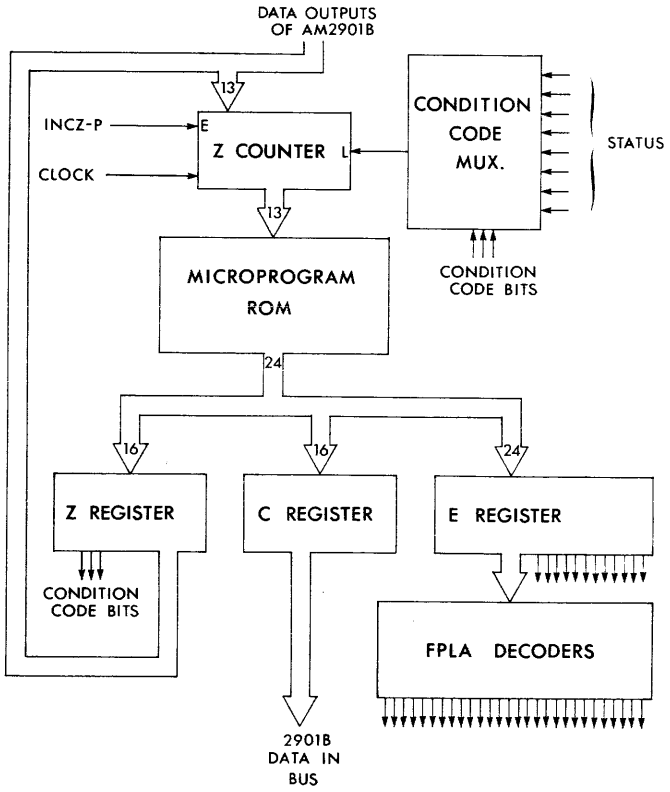


FIGURE 2-7

SIMPLIFIED BLOCK DIAGRAM

INCZ-P (Increment Z) is the enable signal for the Z counter. It is generated by an FPLA and controls the number of microwords to be fetched for each microcode instruction. Once the first microword (the microinstruction portion) is in the E register, the FPLAs begin decoding and determine if the instruction is of the single, double, or triple microword variety. The FPLAs generate INCZ-P as many times as required to fetch each microcode instruction from the microprogram ROM.

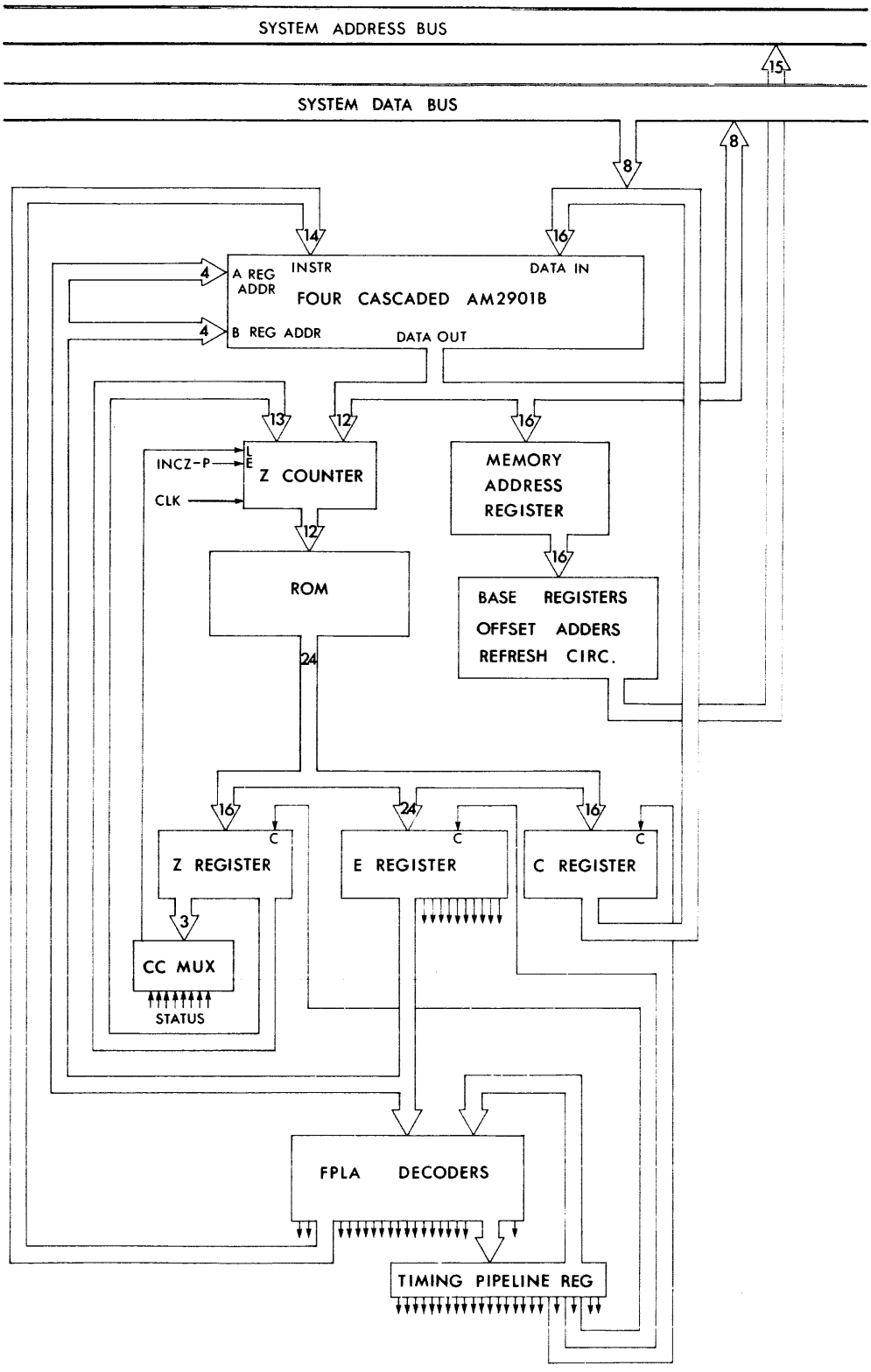


FIGURE 2-8

BLOCK DIAGRAM

In Figure 2-8 a block diagram is given including the four cascaded 2901B bit-slice microprocessing elements. Notice, the Instruction Control inputs to the 2901B (I_0-I_8) are generated by the FPLAs as a result of the microinstruction in the E register. The A port register address and B port register address to the register file are specified directly by the microinstruction in the E register. Notice, timing is generated by the FPLAs and is pipelined at the 11MHz rate with the present processor state fed-back to the inputs of the timing FPLA. This permits the timing FPLAs to prepare their output signals for the next processor state while the present state is performing its function. The clock signals for the E (microinstruction) register, C (constant) register, and Z (condition code/branch address) register are all generated one state premature by the FPLAs and are synchronized through the timing pipeline register.

2.6 BASE REGISTERS AND MEMORY ADDRESSING

The Q30 uses base register addressing. Sixteen base registers are used, each 20 bits wide. The base registers are fashioned from five 16 by 4 RAMs.

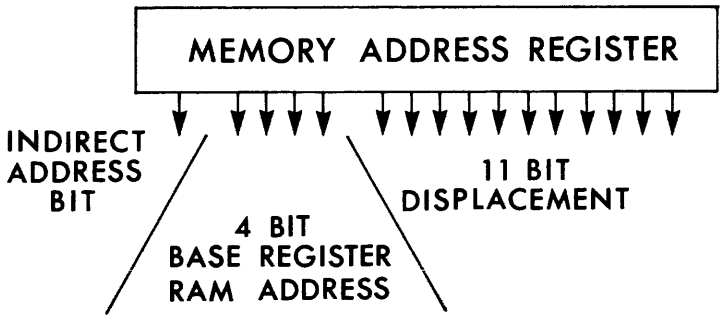


FIGURE 2-9

MAR CONVENTIONS

Memory addresses referenced in machine instructions are 16 bits wide. Address bit 15, the most significant bit, is the indirect address bit and is resolved by the CPU firmware. Address bits 11-14 address the base register RAMs and select a particular base register ($Ø-F). Address bits Ø-1Ø generate a displacement value which is added to the contents of the selected base register. The 11 bit displacement value points to a specific location in each 2K memory partition.

During every memory reference operation, the Q30 hardware adds the 11 bit displacement value to the 20 bit offset value contained in the selected base register. By loading the base registers with offset values separated by $8ØØ increments (2K)* any 32K block of memory may be selected from the 1 Megabyte territory. The 20 bit offset value from the base register RAMs added to the 11 bit displacement value generates the desired 20 bit address from the 15 bit machine instruction address.

The sixteen 20 bit base registers are loaded from the register file via the 2901B data output lines. Since the four cascaded 2901B devices create a register file 16 bits wide, the 20 bit offset values must occupy two register file locations. The upper 12 bits of the offset value are loaded into a specific base RAM location from the three least significant 2901B devices. Then, the lower eight bits of the offset value are loaded (from a different register file location) into the same base register from the two least significant 2901B devices (see Figure 2-10).

Likewise, the 20 bit contents of any base register may be read into the register files, or used as an input operand to the ALU by a similar two process operation. The upper 12 bits of the

*throughout this manual the $ symbol will be used to indicate hexadecimal notation.

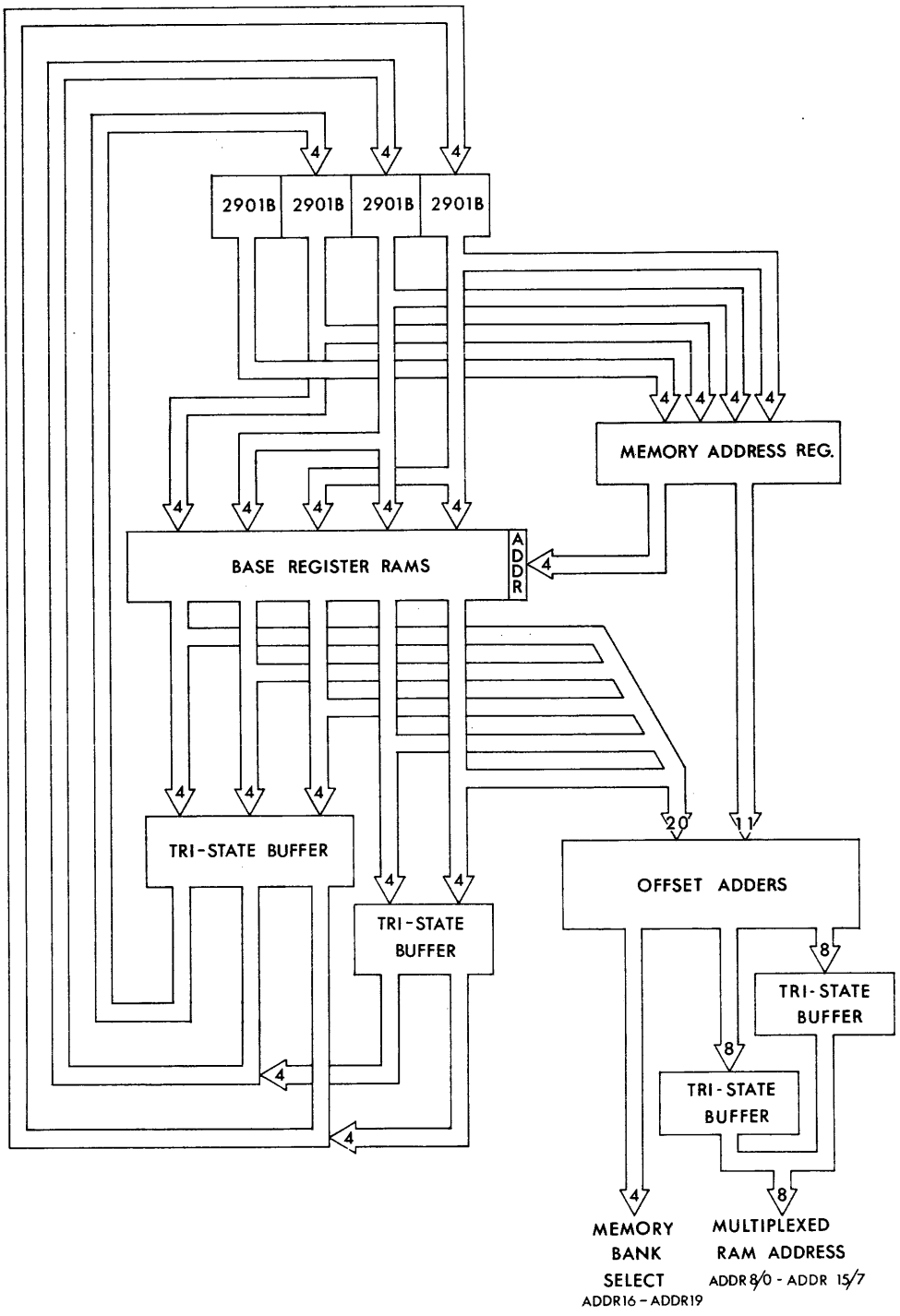


FIGURE 2-10

EXTENDED MEMORY ADDRESSING LOGIC

selected base register is enabled onto the data inputs of the three least significant 2901B devices via tri-state buffers. The lower eight bits of the base register are then enabled onto the data inputs of the two least significant 2901B devices via tri-state buffers where they are loaded into a different register file location.

The offset adders output the 20 bit address capable of addressing 1 Megabyte of memory. The 16 least significant address bits are multiplexed via 2 time states onto an 8 bit address bus, as required by the 64K by 1 memory chips used on the MEM7B memory boards. The address multiplex timing is controlled by FPLA intelligence.

The 4 bank select bits from the offset adders specify which one of the MEM7B boards on the MEM7AR assembly will be accessed. Each MEM7B board has 128Kilobytes of RAM fashioned from 64K by 1 memory chips. The least significant bank select bit enables a 64K by 8 bank of RAMs on the selected 128K by 8 MEM7B board.

2.7 FILE ADDRESS MULTIPLEXERS

If all ALU operations and register file referencing was performed with 16 bit operands, the simplified block diagram given as Figure 2-8 would work fine. However, the Q30 has the ability to manipulate 8 bit operands as well. Considering the four cascaded 2901B devices, the eight upper register file locations (R8-RF) may be used as 8 bit high and 8 bit low locations as well as 16 bit registers (see Figure 2-11). For example, the contents of as 8 bit high register may be added to the contents of a 16 bit register file location.

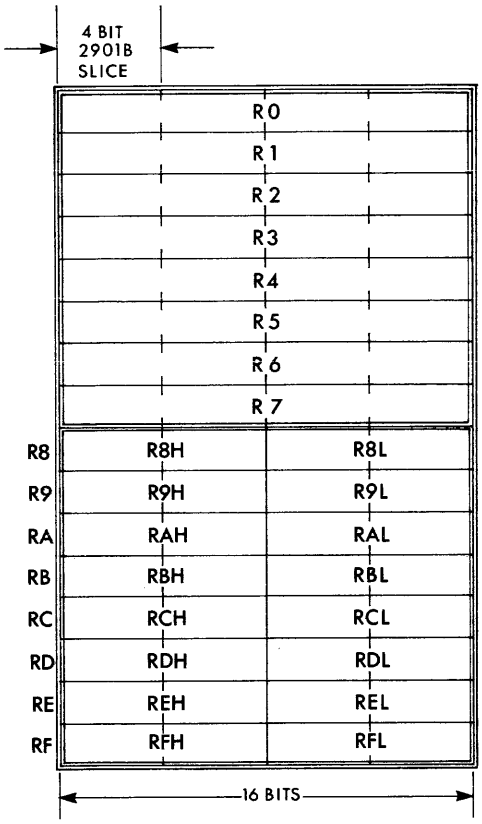


FIGURE 2-11

REGISTER FILES

The register file addresses to the 2901B devices originate from the microinstruction presently in the E register (microcode formats are discussed in depth in the following chapter). A close examination of the I_0-I_2 instruction control signals (Table A) shows that data entering the data inputs of the 2901B can only be multiplexed onto the R inputs of the ALU. Furthermore, only the contents of a register addressed by the A register address port or forced zeros may be multiplexed to the S inputs of the ALU while the data inputs supply the R operand to the ALU. The B register address port must be used to specify a destination when data is written into a register file.

For example, the contents of an 8 bit high register is added to the contents of a 16 bit register and the result is placed back into the 16 bit register. Assume, the 8 bit high register is REH and the 16 bit register is R8. The A register address port to the two high byte 2901B devices must receive the register address for REH and the proper instruction control codes to enable the contents of REH out the data ouptuts of the high byte 2901B devices. The low byte 2901B devices receive the

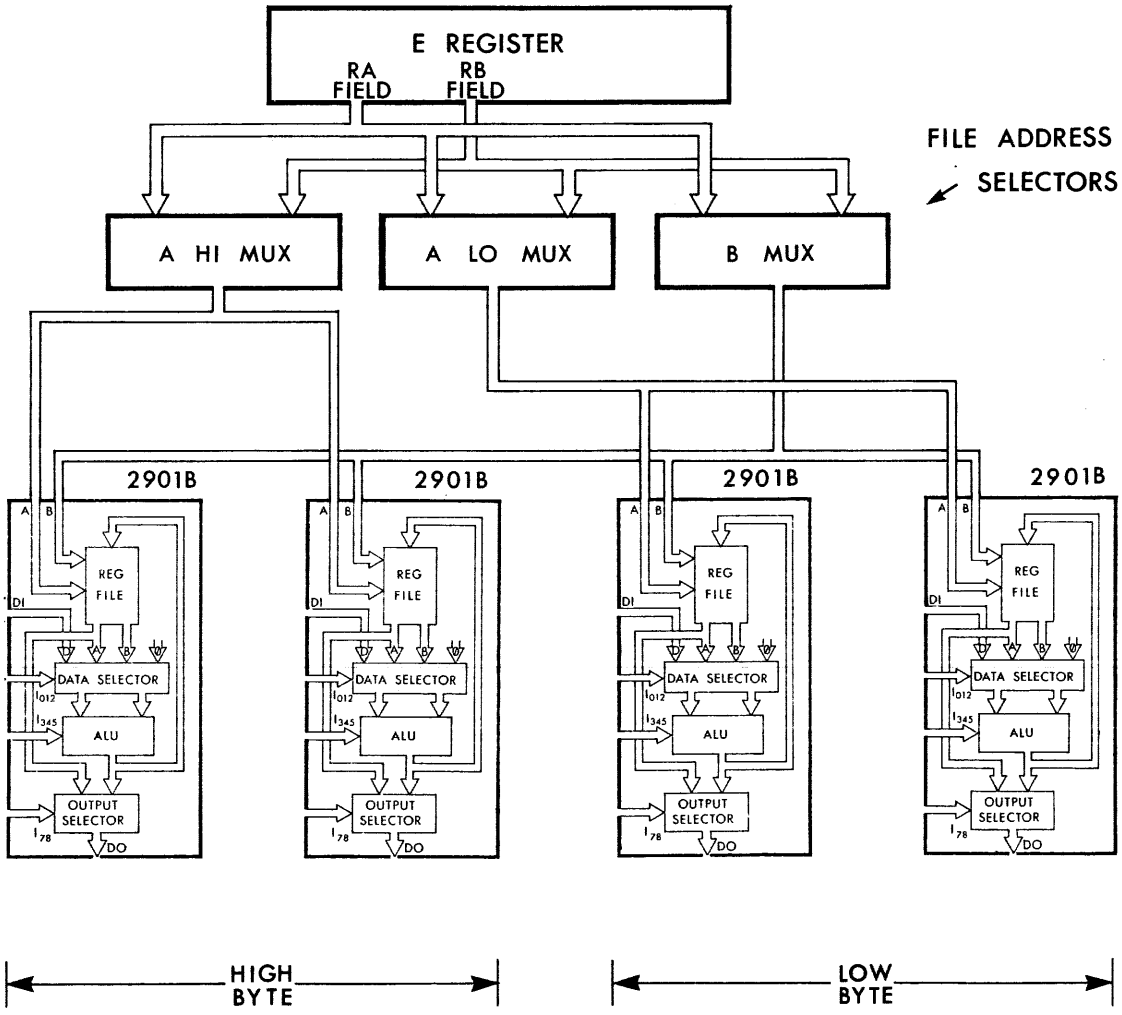


FIGURE 2-12

FILE ADDRESS SELECTORS

proper instruction control code to multiplex the data out of the high byte 2901B devices onto the R inputs of the ALU in the low byte 2901B devices. Therefore, the A register address port of the two low byte 2901B devices must receive the address for register R8 since its contents will be multiplexed to the S inputs of the ALU. The B register address port of all four 2901B devices must receive the register address for R8 since the ALU result will be placed back into the 16 bit register R8.

The file address selectors are situated between the E register and the A and B register address ports of the 2901B devices. The A register address is routed to separate A Hi and A Lo buses while only one B register address multiplexer is needed since writing to an 8 bit high or 8 bit low register is performed by inhibiting the clock signal to the two undesired 2901B devices. Each multiplexer has the ability to select either the RA field or the RB field of the microinstruction and permit any combination of 8 bit high, 8 bit low, or 16 bit operand manipulation. The selection control of these file address multiplexers is generated by two control bits expressed directly as part of the microinstruction microword.

2.8 STATUS REGISTERS

A discrete status register on the Q30 is updated by the E register clock as it clocks a new microinstruction into the E register. The following status condition flags are held:

```
Power Failure ------- from power supply monitor circuit
Parity Fault -------- from main memory
Start/Stop ---------- from operator's control panel
Power Down Request -- from operator's control panel
Enabled Interrupt --- from an I/O controller
Most Significant Bit- from ALU
Zero Bit ------------ from ALU
Carry Bit ----------- from ALU
```

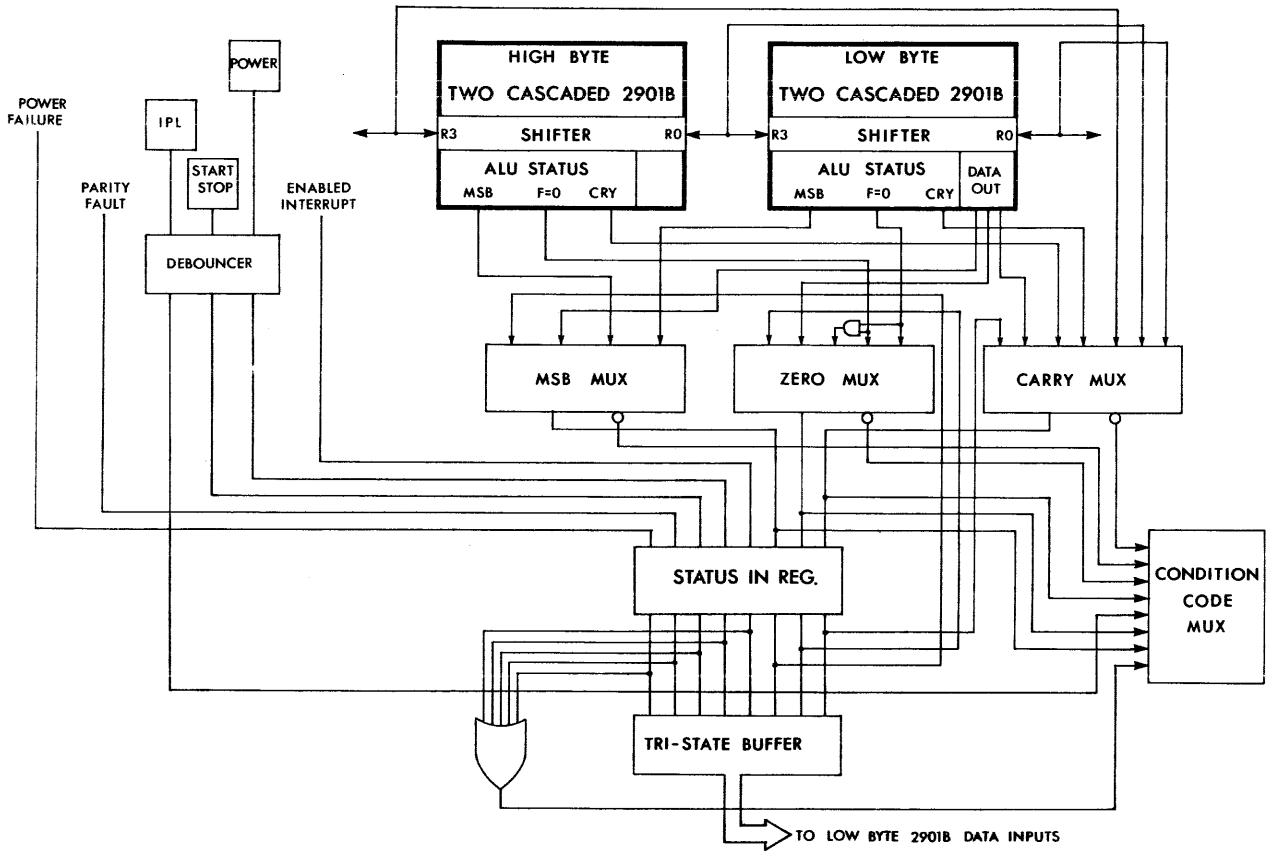


FIGURE 2-13

STATUS FLAG SELECTORS

The three ALU status bits (MSB, Zero, Carry) are each supplied to the Status In register via a multiplexer, allowing the status of high byte, low byte, and/or 16 bit operations to be examined. The select inputs of the MSB, Zero, and Carry multiplexers are driven by an FPLA dedicated to status control. The multiplexers output complementary versions of the selected input. The non-inverted outputs are routed to the Status In register while the inverted outputs are routed to the condition code multiplexer along with the non-inverted outputs. This permits the condition code multiplexer to perform conditional branch testing on the presence or absence of any one of the status bits.

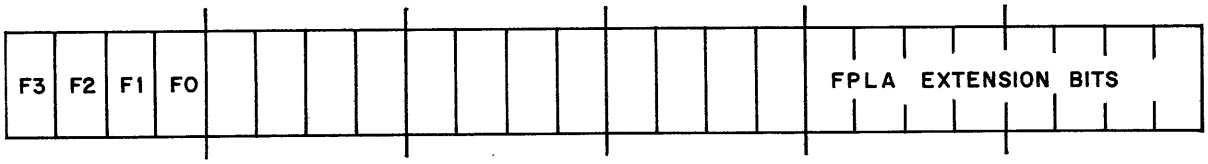
The value of the MSB, Zero, and Carry bit presently in the Status In register is routed back to one input of its corresponding multiplexer. This permits the previous (or historical) value of the MSB, Zero, or Carry bit to be retained when the Status In register is updated. In this case, the STATUS FPLA has inhibited the updating of the ALU status bits.

The Carry multiplexer selects the right hand shifter output from the low byte 2901B devices on 16 bit or 8 bit low shift right into carry and rotate right into carry operations. The bi-directional line between the high byte and low byte 2901B shifters is selected on low byte rotate left into carry and low byte shift left into carry as well as high byte rotate right into carry. Likewise, the carry multiplexer selects the left hand shifter output from the high byte 2901B devices during 16 bit or 8 bit high rotate left into carry or shift left into carry operations. It is the STATUS FPLA decoding the microinstruction in the E register that selects the proper inputs to the carry multiplexer.

During memory read or write operations, a multiplexer (not shown in Figure 2-13) routs the output of the Data Bus Equals Zero detector to the Zero mux inplace of the F=Ø outputs from the ALU. Likewise, the same multiplexer routs the most significant bit of the low byte data bus to the MSB mux inplace of the low byte MSB and high byte MSB outputs from the ALU (during memory read of write operations).

3.0 Q30 MICROCODE

This chapter deals with the format of Q30 microinstructions. The microinstruction coding follows easily learned patterns and retains consistent field designations. The microcode instructions resident in the ROMs of the Q30 are 1, 2, or 3 ROM locations in length (see Figure 2-6). The first microword of each microinstruction specifies the type of operation by its four bit function field (FØ-F3).



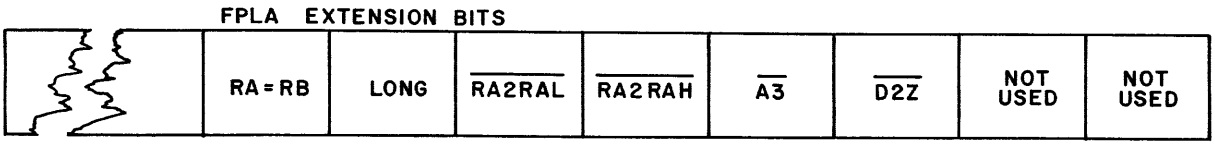
FØ-F3 the Function Field bits specify one of 16 opcodes:

$Ø	Single Operand, Miscellaneous
$1	Compare or Test Bit
$2	Add
$3	Subtract
$4	Add with Carry
$5	Subtract with Carry
$6	Exclusive Or
$7	Inclusive Or
$8	Logical And
$9	Move
$A	Jump
$C	Main Memory Read/Write
$D	I/O

The least significant 8 bits of the first microword of each microinstruction are the FPLA extension bits. On the Q29 CPU these signals were generated by FPLA decoding. Having the

the $ symbol indicates hexadecimal notation

signals directly present in the microword has alleviated the FPLA propagation delay which before accompanied each signal. This permits the Q30 to operate substantially faster.

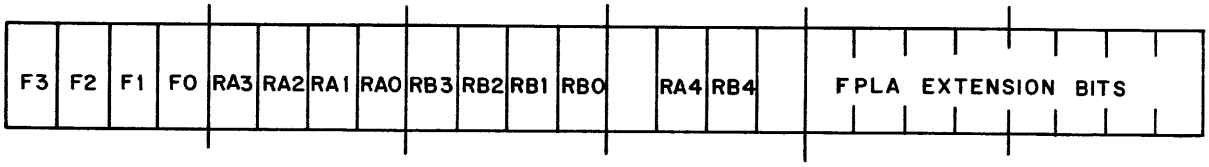


FPLA Extension bits:

RA=RB	RA field and RB field are equal
LONG	long microinstruction timing cycle
RA2RAL	RA field (E Reg) to low byte 2901B
RA2RAH	RA field (E Reg) to high byte 2901B
A3	Most Significant Bit of RA field
D2Z	2901B outputs to Z Counter presets

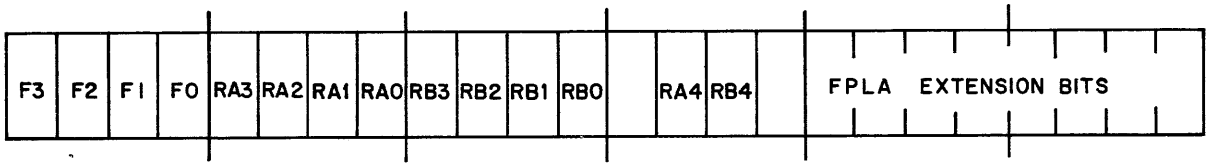
3.1 DOUBLE OPERAND INSTRUCTIONS

Opcodes $1 through $9 are two operand instructions requiring an A port register address and B port register address for the cascaded register files of the 2901B devices. The register addresses are specified by the two 5 bit fields RaØ-Ra4 and RbØ-Rb4.



RaØ-Ra4 specifies a register file location whose contents will perform as the A operand of the microinstruction. The contents of this source register may be selected as an input operand to the ALU or be routed directly through the data outputs of the 2901B depending on the specific instruction.

The cascaded register files contained in the four 2901B devices may be designated as 16 registers each 16 bits wide, or, the upper 8 sixteen bit registers may be accessed as sixteen 8 bit registers (see Table C). The Ra field is thus 5 bits wide. When Ra4 is logically high, an 8 bit register is specified. Assuming Ra4 is logically high, the Ra3 bit when logically high specifies an 8 bit high register. Likewise, Ra4 high and Ra3 low specifies an 8 bit low register. Table C shows the register orientation and tabulates the Ra field codes with their corresponding register.



RbØ-Rb4 specifies a register file location whose contents will will perform as the B operand of the microinstruction. This field also specifies the destination register for the resultant data from the ALU. The registers are coded exactly as tabulated for the Ra field (see Table C). When Rb4 is logically high, an 8 bit register is specified. With Rb4 logically high, an 8 bit high register is specified when Rb3 is also logically high. Likewise, Ra4 high and Ra3 low specifies an 8 bit low register.

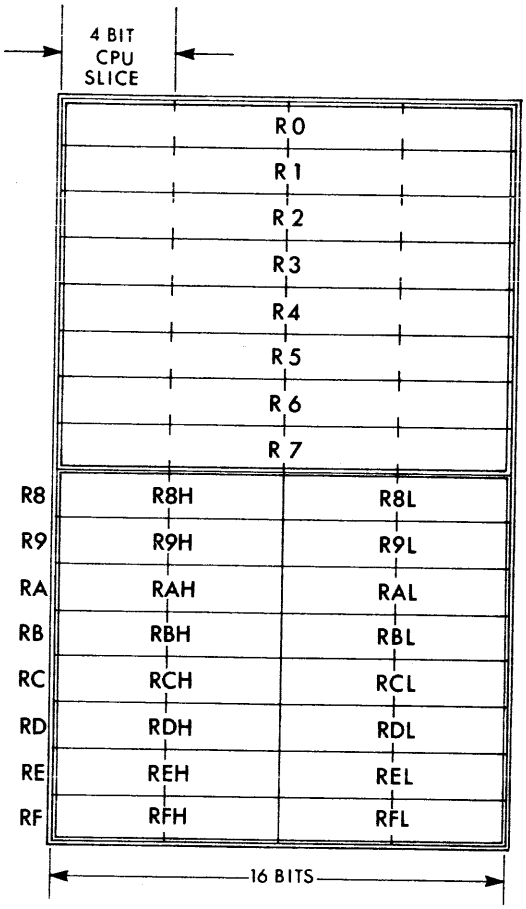
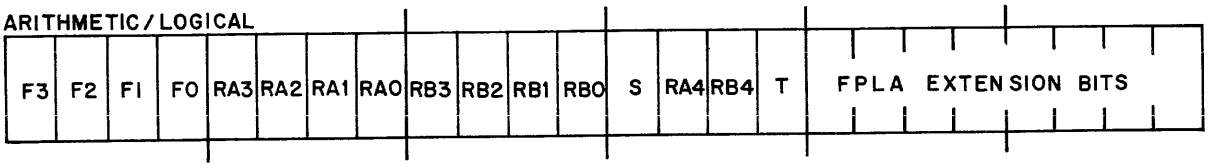


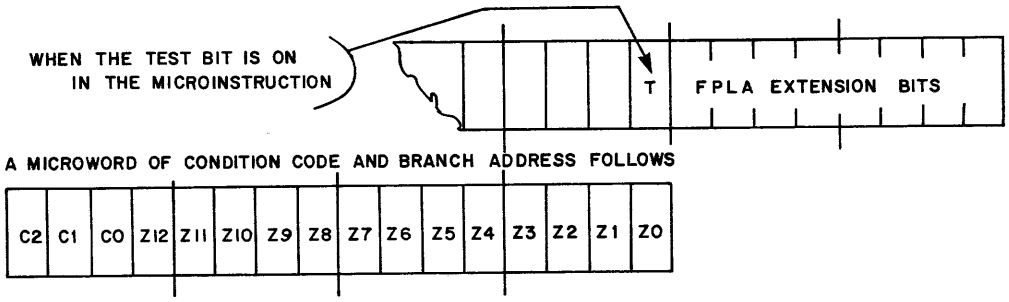
TABLE C

RaØ-Ra4 RbØ-Rb4	REGISTER	RaØ-Ra4 RbØ-Rb4	REGISTER
$00	RO	$10	R8L
$01	R1	$11	R9L
$02	R2	$12	RAL
$03	R3	$13	RBL
$04	R4	$14	RCL
$05	R5	$15	RDL
$06	R6	$16	REL
$07	R7	$17	RFL
$08	R8	$18	R8H
$09	R9	$19	R9H
$0A	RA	$1A	RAH
$0B	RB	$1B	RBH
$0C	RC	$1C	RCH
$0D	RD	$1D	RDH
$0E	RE	$1E	REH
$0F	RF	$1F	RFH

All arithmetic, logical, and move operations (Function Fields of 2 through 9) code the remaining bits as the Status Enable bit (S) and Test Bit (T).

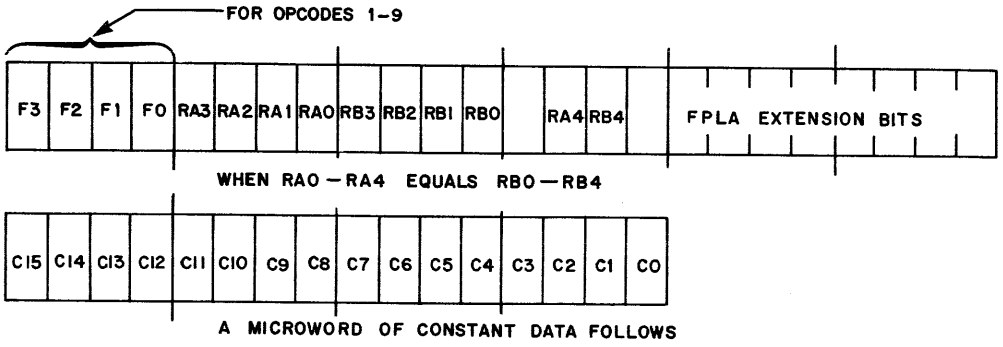


S The Status Enable bit, when logically high causes the proper MSB, Zero, and Carry bit to be selected through the FPLA driven status multiplexers. These flags are then clocked into the Status In register at the end of the operation. When the Status Enable bit is logically low the status multiplexers rout the previous value of the MSB, Zero, and Carry flag (from the previous operation) back to the inputs of the Status In register where they are re-entered at the end of the operation.



T The Test bit specifies the testing for a conditional branch following the operation. When the T bit is logically high the next microword is interpreted as: a 3 bit condition code and a 13 bit branch address (if the operation is a double microword instruction). If the T bit is asserted in the microinstruction portion of a triple microword instruction, the condition code and branch address follow as the third microword of the instruction. When the T bit is logically low no microword of condition code and branch address follow the microinstruction microword.

When the Function Field is equal to 1 through 9 and the Ra and Rb fields are equal, a microword of constant data follows the microinstruction microword in the ROM.



With the Ra and Rb fields equal, the constant data microword may serve as if pointed to by either the Ra or Rb field. The constant data will act as if supplied from a register in the register file. The S and T bits are decoded to determine what field (register contents) the constant data will replace.

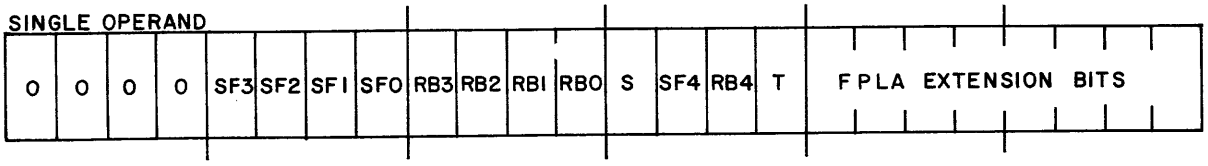
	T	S	Field replaced by CONSTANT OPERAND
Opcodes 2-9 Ra=Rb	Ø	Ø	Ra
	Ø	1	Ra
	1	Ø	Rb
	1	1	Ra

When T=1 and S=Ø the constant data microword replaces whatever register contents the Rb field pointed toward. The constant data thus becomes the input operand to the ALU (through the D inputs of the 2901B) along with the contents of the register pointed to by the Ra field. The resultant data from the ALU operation becomes the third microword of the instruction and is loaded into the Z counter. This is a triple microword instruction because Ra=Rb and the T bit is logically high. The result of this instruction is a multi-way branch operation. If an 8 bit high register is specified by the Ra and Rb field (Ra=Rb), the operation occurs between the register and the high order 8 bits of the constant.

A conditional branch is allowed on any of the arithmetic/logical instructions (opcodes 2 through 9) except for the special case when Ra=Rb, S=Ø, and T=1, When these three conditions are met a microword of condition code and branch address does not follow even though the T bit is logically high.

3.2 SINGLE OPERAND INSTRUCTIONS

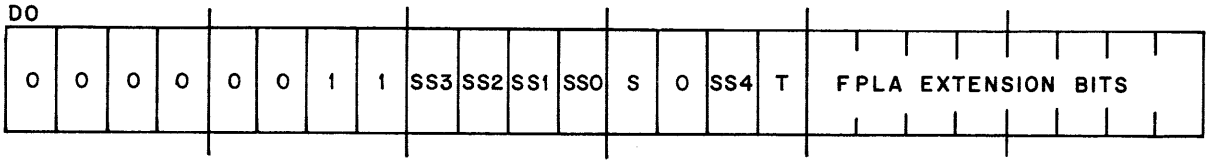
Opcode Ø specifies a group of miscellanous single operand instructions. These instructions specify a single register file location. The contents of this register is manipulated and returned to the same register or it may be moved to or filled from a discrete register of the Q30 as the base registers or the status registers. The S and T bits are retained and have the same meaning as explained for the two operand instructions.



SFØ-SF4 becomes the Secondary Function Field when the primary function field displays opcode Ø. The SF field specifies one of 32 possible single operand instructions.

$ØØ No Operation	$ØC Rotate Right through Carry
$Ø1 Zero Register	$ØD Rotate Left through Carry
$Ø2 Test Write	$1Ø Decrement Register
$Ø3 "Do" Instructions	$12 Increment Register
$Ø4 Write to Flag Register	$18 Write Base Low
$Ø5 Write to Flag Bits	$1A Write Base High
$Ø6 Input Flag Register	$1C Read Base Low
$Ø8 Shift Right into Carry	$1E Read Base High
$Ø9 Shift Left into Carry	

The "Do" instructions are a special case under the opcode Ø group. When the F field equals $Ø and the SF field equals $Ø3 the Rb field becomes a third function field. The "Do" instructions use no register file locations, so no operand fields are required.

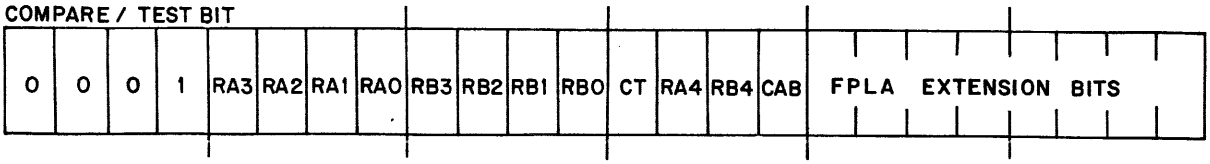


SSØ-SS4 This field specifies the type of "Do" instruction. Currently, only one "Do" instruction has been defined.

SS	OPERATION
$ØØ	Zero Flag Register The MSB, Zero, and Carry bits of the Status In register are cleared.

3.3 COMPARE/TEST BIT INSTRUCTIONS

The Compare/Test Bit instructions are a special case of the double operand group. The opcode $1 in the Function Field specifies this instruction group. Being double operand instructions, two registers are specified by the Ra and Rb fields as operands. A microword of condition code and branch address always follows every Compare/Test Bit instruction. If the Ra field equals the Rb field the instruction will be of the triple microword variety with a microword of constant data followed by a microword of condition code and branch address.

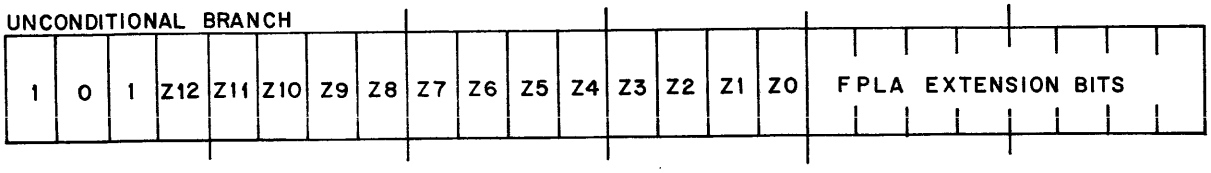


CT used only for opcode $1, this bit specifies whether the instruction is a Compare (CT=1) or Test Bit (CT=Ø) operation.

CAB is defined as the Constant Ra/Rb bit. When Ra=Rb the CAB bit specifies whether the constant will be used as the Ra field (CAB=Ø) or the Rb field (CAB=1). It is used only for Opcode 1 when the Ra field equals the Rb field. Otherwise, it should be set to a logical one. A Compare operation is basically a non-destructive subtract operation with the resulting ALU status flag setting being the important resultant. The CAB bit permits testing for "greater than" or "less than" conditions by providing the flexibility which allows the constant to be subtracted from the contents of the addressed register file location, or vice versa, the contents of the register file is subtracted from the constant microword. The following condition code and branch address microword will specify which ALU status flag will be tested (the "greater than" or "less than" compare operations will test the carry bit, "equal to" will test the zero bit).

3.4 UNCONDITIONAL BRANCH INSTRUCTIONS

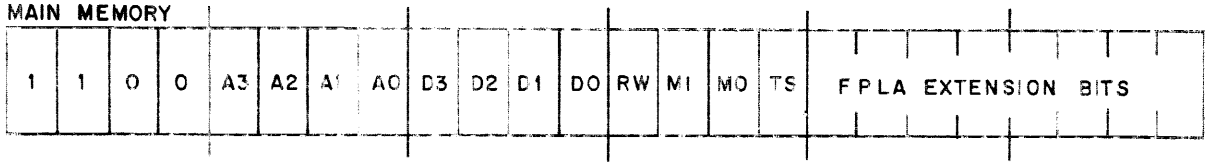
The Unconditional Branch microinstruction is always a single microword instruction and is specified by the opcode $A in the Function Field.



The instruction causes the Z counter to be loaded with the address specified by the ZØ-Z12 field. While similar in format to a condition code and branch address microword, this is a single microword microinstruction.

3.5 MAIN MEMORY READ/WRITE INSTRUCTIONS

Opcode $C in the Function Field specifies a memory reference operation. Memory Write operations move data from a register file location to a memory location specified in another register file location. Likewise, a Memory Read operation moves data from a memory location whose address is specified in one of the register file registers and deposits the data in one of the register file locations. The instruction can be programmed to automatically increment, decrement, or not change the memory address pointer after the address has been clocked into the memory address register for use during the memory access operation in progress.



AØ-A3 The Address Register field specifies a 16 bit register file register (RØ-RF). The contents of this register is used as the address pointer to memory.

DØ-D3 The Data Register field specifies one of the 8 bit high or 8 bit low register file registers. This register will contain the byte to be written or will specify the destination for a read byte.

DØ-D3	REGISTER	DØ-D3	REGISTER
$Ø	R8L	$8	R8H
$1	R9L	$9	R9H
$2	RAL	$A	RAH
$3	RBL	$B	RBH
$4	RCL	$C	RCH
$5	RDL	$D	RDH
$6	REL	$E	REH
$7	RFL	$F	RFH

RW The Read/Write bit specifies if the operation is a Read (RW=1) or Write (RW=Ø).

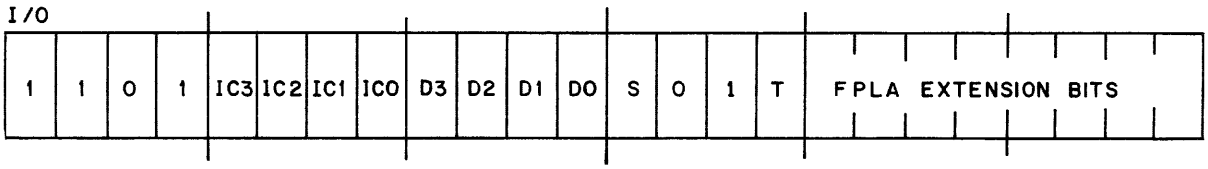
MØ-M1 The Modify bits specify how the contents of the address pointer register (specified by AØ-A3) will be modified after the memory reference operation.

M1	MØ	Memory Address Pointer
Ø	Ø	No Change
Ø	1	No Change
1	Ø	Decrement by 1
1	1	Increment by 1

TS The Test/Status bit is a dual purpose bit. When TS=1, it is equivalent to having the T bit and S bit of the arithmetic/logical instructions (opcodes 2-9) both on simultaneously. With TS=1, the ALU status flags will reflect the condition of the data read (the carry bit will remain unchanged) and these status bits will be updated in the Status In register. Also, the microinstruction will be followed by a microword of condition code and branch address. When TS=Ø, the MSB, Zero, and Carry bits of the Status In register will not be updated and no condition code and branch address microword follows the microinstruction.

3.6 INPUT/OUTPUT INSTRUCTIONS

Input/Output operations are specified by the opcode $D in the Function Field. The instruction specifies the type of I/O function within the microword. The S and T bit retain the same meaning as used during the arithmetic/logical instructions.



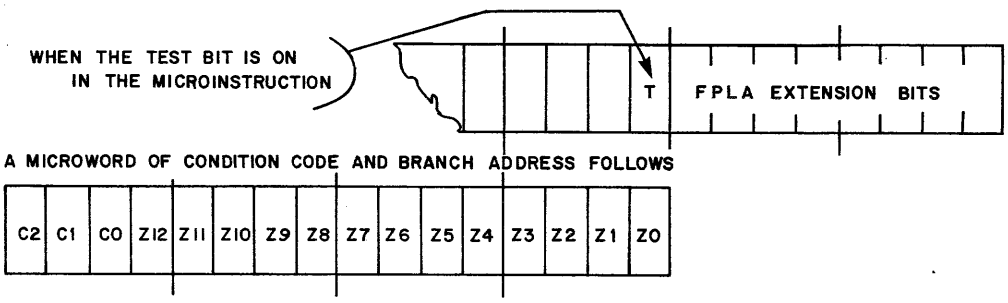
ICØ-IC3 The I/O control bits specify the I/O instruction to be performed. The control codes are consistent with existing Qantel control bytes.

IC	CONTROL COMMAND
$Ø	Read Data from I/O Bus
$1	Read Status Ø
$2	Write Data onto I/O Bus
$3	Write Control Byte onto I/O Bus
$4	Reset the I/O Device selected
$5	Set Read
$6	Set Write
$7	Set Terminate Command to I/O Controller
$8	Read Status 1
$9	Read Status 2
$A	Set Cylinder
$B	Set Head
$C	Set Difference
$D	Disc Control
$E	Set Sector
$F	Select an I/O Device

DØ-D3 The Data Register bits specify an 8 bit high or 8 bit low register file location which will be the source of data for output instructions and the destination of the input data for input instructions. The 8 bit low or high registers are coded following the same convention as the DØ-D3 field under Main Memory Read/Write Instructions (see Section 3.5).

3.7 CONDITIONAL BRANCHING

Any microinstruction containing a logically high T bit (or TS bit) also has the capability of performing a conditional branch. The T (or TS) bit indicates a microword consisting of 3 bits of condition code and a 13 bit branch address directly following the microinstruction in the ROM.



CCØ-CC2 The condition code bits define which status condition flag will be selected by the condition code multiplexer. If the selected condition is true it will cause the Z counter to be loaded from the Z register (which now contains the branch address specified by the ZØ-Z12 field.

CCØ-CC2	STATUS CONDITION FLAG
$Ø ESC2	Escape 2
$1 ESC1	Escape 1
$2 NMSB	Not Most Significant Bit
$3 MSB	Most Significant Bit
$4 NZ, NE	Nonzero
$5 Z, EQ	Zero
$6 NC	No Carry (Borrow True)
$7 C	Carry (Borrow False)

3.8 MICROINSTRUCTION DESCRIPTIONS

The complete microinstruction set is listed here in opcode sequence along with a description of each instruction. Under the mnemonic for each instruction the codes for the instruction's characteristic fields are abbreviated. Any effect the instruction might have on the MSB, Zero, or Carry Flags in the Status In register is given at the right of each description. If the flags are affected in accordance with the resultant data from the operation, an X is shown under the appropriate flag. If a flag is not changed by the operation, NC is shown. If the flag is reset by the operation, a Ø is shown. If the T (or TS) bit is logically low in the microinstruction the previous value of the MSB, Zero, and Carry flags will be retained and the resultant of the executing instruction will not affect the flags.

NOP		MSB	Z	C
F=$Ø, SF=$ØØ	No Operation	NC	NC	NC

No Operation. However, if the test bit is on and the condition specified in the condition code and branch address microword is present, the branch address is loaded into the Z counter.

ZERO		MSB	Z	C
F=$Ø, SF=$Ø1	Zero Register	Ø	Ø	NC

The contents of the register file location specified by the Rb field is cleared. The Zero and Most Significant Bit status flags are reset.

TWRITE		MSB	Z	C
F=$Ø, SF=$Ø2	Test Write from Panes	X	X	X

The contents of the data register in the Q30 test panel is moved to the register file location specified by the Rb field.

DO	Zero Flag Register	MSB	Z	C
F=$Ø, SF=$Ø3, SS=$ØØ		Ø	Ø	Ø

The MSB, Zero, and Carry flags in the Status In register are reset.

OUTFLAG	Write to Flag Register	MSB	Z	C
F=$Ø, SF=$Ø4		X	X	X

The contents of the register file location specified by the Rb field is moved to the Status Out register. The following data lines are latched into this flag register with the designations listed below:

DBØ3	INTERRUPTS ENABLED
DBØ4	POWER DOWN (POWER ON LAMP)
DBØ5	HALT LIGHT (START/STOP LAMP)

WFLAG	Write to Flag Bits	MSB	Z	C
F=$Ø, SF=$Ø5		X	X	X

Moves the 3 least significant bits of the contents of the register file location specified by the Rb field through the Status multiplexers, causing them to be latched into the MSB, Zero, and Carry bits of the Status In register.

INFLAG	Read from Flag Register	MSB	Z	C
F=$Ø, SF=$Ø6		NC	NC	NC

Moves the present contents of the Status In register (all 8 bits) to the register file location specified by the Rb field.

SHR	Shift Right	MSB	Z	C
F=$Ø, SF=$Ø8		X	X	X

The contents of the register file location specified by the Rb field is shifted one bit position right and returned to the same register file location. A logical low is shifted into the most

significant bit of the data word. The Carry flag is set to the logical value of the bit shifted out. The Zero and MSB flags reflect the status of the unshifted data.

SHL	Shift Left	MSB	Z	C
F=$Ø, SF=$Ø9		X	X	X

The contents of the register file location specified by the Rb field is shifted one bit position left and returned to the same register file location. A logical low is shifted into the least significant bit of the data word. The Carry flag is set to the logical value of the bit shifted out. The Zero and MSB flags reflect the status of the unshifted data.

ROR	Rotate Right	MSB	Z	C
F=$Ø, SF=$ØC		X	X	X

The contents of the register file location specified by the Rb field is rotated one bit position right. The least significant data bit is moved into the Carry flag and the logical value of the of the Carry flag is moved into the most significant bit position of the data word. The Zero and MSB flags reflect the status of the unrotated data.

ROL	Rotate Left	MSB	Z	C
F=$Ø, SF=$ØD		X	X	X

The contents of the register file location specified by the Rb field is rotated one bit position left. The most significant data bit is moved into the Carry flag and the logical value of the Carry flag is moved into the least significant bit position of the data word. The Zero and MSB flags reflect the status of the unrotated data.

DEC	Decrement Register	MSB	Z	C
F=$Ø, SF=$1Ø		X	X	X

The contents of the register file location specified by the Rb field is decremented by one.

INC	Increment Register	MSB	Z	C
F=$Ø, SF=$12		X	X	X

The contents of the register file location specified by the Rb field is incremented by one.

WBASEL	Write Base Low	MSB	Z	C
F=$Ø, SF=$18		X	X	X

The low byte, 8 bit contents of the register file location specified by the Rb field is moved to the low 8 bits of the selected base register. The 4 most significant bits of the register file location pointed to by the Rb field specify the base register RAM location.

WBASEH	Write Base High	MSB	Z	C
F=$Ø, SF=$1A		X	X	X

The least significant 12 bits of the register file location specified by the Rb field are moved to the high 12 bits of the selected base register. The 4 most significant bits of the register file location pointed to by the Rb field specify the base register RAM location.

RBASEL	Read Base Low	MSB	Z	C
F=$Ø, SF=$1C		X	X	X

The 8 least significant bits of the selected base register are logically ORed with the contents of the file register specified by the Rb field, and the resultant is placed into the same register file location. The 4 most significant bit of the register file location specified by the Rb field contain the address ($Ø-F) of the base register and the remaining 12 bits should be cleared before the operation is performed.

RBASEH	Read Base High	MSB	Z	C
F=$Ø, SF=$1E		X	X	X

The 12 most significant bits of the selected base register are logically ORed with the contents of the file register specified by the Rb field, the resultant being placed back into the specified register file location. The 4 most significant bits of the register specified by the Rb field should contain the address of the base register and the remaining 12 bits should be cleared before the operation is performed.

CMP	Compare	MSB	Z	C
F=$1, CT=$1		X	X	X

The contents of the file register addressed by the Ra field is compared with (subtracted from) the contents of the file register addressed by the Rb field. The flags are affected according to the result of the subtraction. The Zero flag is set if the compared values are equal. The Carry flag is set if the contents of the file register addressed by Ra is less than or equal to the contents of the file register addressed by Rb.

All Compare instructions are followed by a conditional branch microword. If the Ra field is equal to the Rb field, a microword of constant data follows the microinstruction. The state of the CAB bit specifies which source field the constant data will supplement. (CAB=$Ø, Ra field or CAB=$1, Rb field).

TBT	Test Bit	MSB	Z	C
F=$1, CT=$Ø		X	X	NC

The contents of the file register addressed by the Ra field is bit tested (logically ANDed) with the contents of the file register addressed by the Rb field. The Zero and MSB flags are changed according to the result of the operation. If the tested bit is found to be not logically high, the Zero flag is set. All Test Bit instructions are followed by a conditional branch microword. If the Ra field is equal to the Rb field, a microword of constant data follows the microinstruction. The state of the CAB bit is not important on a Test Bit instruction since it does not matter during a logical AND operation which source field the constant data supplements.

ADD	Add	MSB	Z	C
F=$2		X	X	X

The contents of the register file locations specified by the Ra and Rb fields are added with the result going back into the location specified by the Rb field.

SUB	Subtract	MSB	Z	C
F=$3		X	X	X

The contents of the register specified by the Ra field is subtracted from the contents of the register specified by the Rb field. The resultant data is placed in the register specified by the Rb field. Carry is set if no borrow occurred.

ADC	Add with Carry	MSB	Z	C
F=$4		X	X	X

The contents of the register specified by the Ra field and the present value of the Carry bit are added to the contents of the register specified by the Rb field. The resultant is returned to the register specified by the Rb field.

SBC	Subtract with Carry	MSB	Z	C
F=$5		X	X	X

The contents of the register specified by the Ra field and the present value of the Carry bit are subtracted from the contents of the register specified by the Rb field. The resultant is returned to the register specified by the Rb field. The Carry bit is set if no borrow occurred.

XOR	Exclusive Or	MSB	Z	C
F=$6		X	X	NC

The contents of the register specified by the Ra field is exclusive ORed with the contents of the register specified by the Rb field. The resultant data is placed in the register specified by the Rb field. The Carry flag is not affected.

OR	Logical OR	MSB	Z	C
F=$7		X	X	NC

The contents of the register specified by the Ra field is logically ORed with the contents of the register specified by the Rb field. The resultant data is placed in the register specified by the Rb field. The Carry flag is not affected.

AND	Logical AND	MSB	Z	C
F=$8		X	X	NC

The contents of the register specified by the Ra field is logically ANDed with the contents of the register specified by the Rb field. The resultant is placed in the register specified by the Rb field. The Carry flag is not affected.

MOV	Move	MSB	Z	C
F=$9		X	X	NC

The contents of the register specified by the Ra field is moved to the register specified by the Rb field. The Carry flag is not affected.

JMP	Unconditional Branch	MSB	Z	C
F=$A		NC	NC	NC

The Z counter is loaded unconditionally from the Z register which contains the ZØ-Z12 field of the microinstruction.

READ	READ+1	READ-1	Memory Read	MSB	Z	C
F=$C, R/W=$1				X	X	NC

The Ra field specifies the 16 bit location of a main memory or I/O two-port memory address. The contents of this register is moved to the memory address register (MAR) where it addresses the base register RAMs by its 4 most significant bits (not including the indirect address bit). The least significant 12 bits in the MAR are then added to the contents of the selected base register, and the resulting address is sent to memory. The D field specifies an 8 bit (high or low) register file location in which the read data byte will be placed. The MSB and Zero flags will be affected according to the data byte read only if the TS bit is logically high. The high TS bit indicates that a conditional branch microword follows. The M field specifies how the main memory address (or two-port memory address) stored in the location specified by the Ra field is to be modified after being loaded into the MAR.

M=$3, Increment by 1, READ+1 instructions
M=$2, Decrement by 1, READ-1 instructions
M=$Ø, or $1, No change, READ instructions

WRITE	WRITE+1	WRITE-1	Memory Write	MSB	Z	C
F=$C, R/W=$Ø				X	X	NC

The Ra field specifies the 16 bit register location containing the main memory or I/O two-port memory address. The contents of this register is moved to the memory address register (MAR) where it addresses the base register RAMs by its 4 most significant bits (not including the indirect address bit). The least significant 12 bits in the MAR are then added to the contents of of the selected base register, and the resulting add-

ress is sent to memory. The D field specifies an 8 bit (high or low) register file location containing the data byte to be written. The TS bit should be left logically low during write instructions, leaving the flags unaffected and indicating that no unconditional branch microword follows.

IO	Input/Output	MSB	Z	C
F=$D		X	X	NC

The contents of the IC field directly specifies the I/O instructions to be performed. The D field specifies an 8 bit (high or low) register file location which contains the data to be outputted, or where the input data byte will be stored.

IORDD	Read Data from I/O Bus	MSB	Z	C
F=$D, IC=$Ø		X	X	NC

An 8 bit byte of data is read via the data bus from the selected controller and stored in an 8 bit (high or low) register file location specified by the D field. A $Ø is placed on the E bus.

IORSØ	Read Status Ø	MSB	Z	C
F=$D, IC=$1		X	X	NC

The contents of the Status Ø register of the selected controller is read via the data bus and stored in an 8 bit (high or low) register file location specified by the D field. A $1 is sent on the E bus.

IOWRD	Write Data to I/O Bus	MSB	Z	C
F=$D, IC=$2		X	X	NC

The contents of the 8 bit (high or low) register file location specified by the D field is written via the data bus to the selected controller. A $2 is sent on the E bus.

IOCTL	Write Control Byte to I/O Bus	MSB	Z	C
F=$D, IC=$3		X	X	NC

A device control character contained in an 8 bit (high or low) register file location specified by the D field is written via the data bus to the selected controller. A $3 is sent on the E bus.

IORIO	Reset I/O	MSB	Z	C
F=$D, IC=$4		X	X	NC

The selected controller is sent a reset command. A $4 is sent on the E bus. The Rb field has no meaning for this instruction.

IOSRD	Set Read	MSB	Z	C
F=$D, IC=$5		X	X	NC

The selected controller is issued a Set Read command. A $5 is sent via the E bus. The Rb field has no meaning for this instruction. The command causes the controller to enter Read mode by setting Read Busy in its Status Ø register.

IOSWR	Set Write	MSB	Z	C
F=$D, IC=$6		X	X	NC

The selected controller is issued a Set Write command. A $6 is sent via the E bus. The Rb field has no meaning. The command causes the controller to enter Write mode by setting Write Busy in its Status Ø register.

IOTERM	Terminate	MSB	Z	C
F=$D, IC=$7		X	X	NC

Used after a Write instruction has transferred all its data, or when the count is reached on a Read with Count instruction, the selected controller is issued a terminate command. A $7 is sent via the E bus. The Rb field has no meaning for this instruction.

IORS1	Read Status 1	MSB	Z	C
F=$D, IC=$8		X	X	NC

The contents of the Status 1 register of the selected controller is read via the data bus and stored in the 8 bit (high or low) register file location specified by the D field.

IORS2	Read Status 2	MSB	Z	C
F=$D, IC=$9		X	X	NC

The contents of the Status 2 register of the selected controller is read via the data bus and stored in the 8 bit (high or low) register file location specified by the D field.

IOCYL	Set Cylinder	MSB	Z	C
F=$D, IC=$A		X	X	NC

This instruction sets the cylinder number in the selected disc controller. A $A is sent via the E bus. The D field has no meaning. The instruction must be preceded by an IOWRD instruction which writes the actual cylinder number to the selected disc controller. The IOCYL instruction then specifies that the previous byte contained cylinder address information.

IOHEAD	Set Head	MSB	Z	C
F=$D, IC=$B		X	X	NC

This instruction sets the head number in the selected disc controller. A $B is sent via the E bus. The D field has no meaning. The instruction must be preceded by an IOWRD instruction which writes the actual head number to the selected disc controller. The IOHEAD instruction then specifies that the byte contained head address information.

IODIFF	Set Difference	MSB	Z	C
F=$D, IC=$C		X	X	NC

This instruction sets the difference and direction information between the old and new cylinder address in the selected disc controller. Also, used to also send an upper byte of cylinder address for discs with cylinder numbers of 9 or more bits. A $C is sent via the E bus. The D field has no meaning. The instruction must be preceded by an IOWRD instruction which writes the actual byte of difference information (or upper cylinder address) to the selected disc controller.

IODCTL	Disc Control	MSB	Z	C
F=$D, IC=$D		X	X	NC

This instruction sets a special control byte in the selected disc controller. A $D is sent via the E bus. The D field is not used. The instruction must be preceded by an IOWRD instruction which writes the actual special control byte to the selected disc controller. The IODCTL instruction then specifies that a previous byte contained a special control character.

IOSECT	Set Sector	MSB	Z	C
F=$D, IC=$E		X	X	NC

This instruction sets the sector number in the selected disc controller. An $E is sent via the E bus. The D field has no meaning. The instruction must be preceded by an IOWRD instruction which writes the actual sector number to the selected disc controller. The IOSECT instruction then specifies that the previous byte contained sector number information.

IOSEL	Select	MSB	Z	C
F=$D, IC=$F		X	X	NC

This instruction selects one of 16 controllers. Since only one controller is selected at a time, the previously selected controller is deselected as a new controller is selected. An $F is sent via the E bus and the contents of the register file location specified by the D field is placed on the data bus. The 4 least significant bits of this file register's contents should contain the address of the controller to be selected.

3.9 MICROINSTRUCTION SUMMARY

Figure 3-1 summarizes the formatting of all microinstruction fields used by the Q30. If the Arithmetic/logical instructions (F=$2-$9) are considered as the model for the group, the fields (or bits) unique to the other instruction types are noted in heavier borders. The vertical arrows indicate shared field designations. The FPLA Extension bits are exactly the same for all microinstructions.

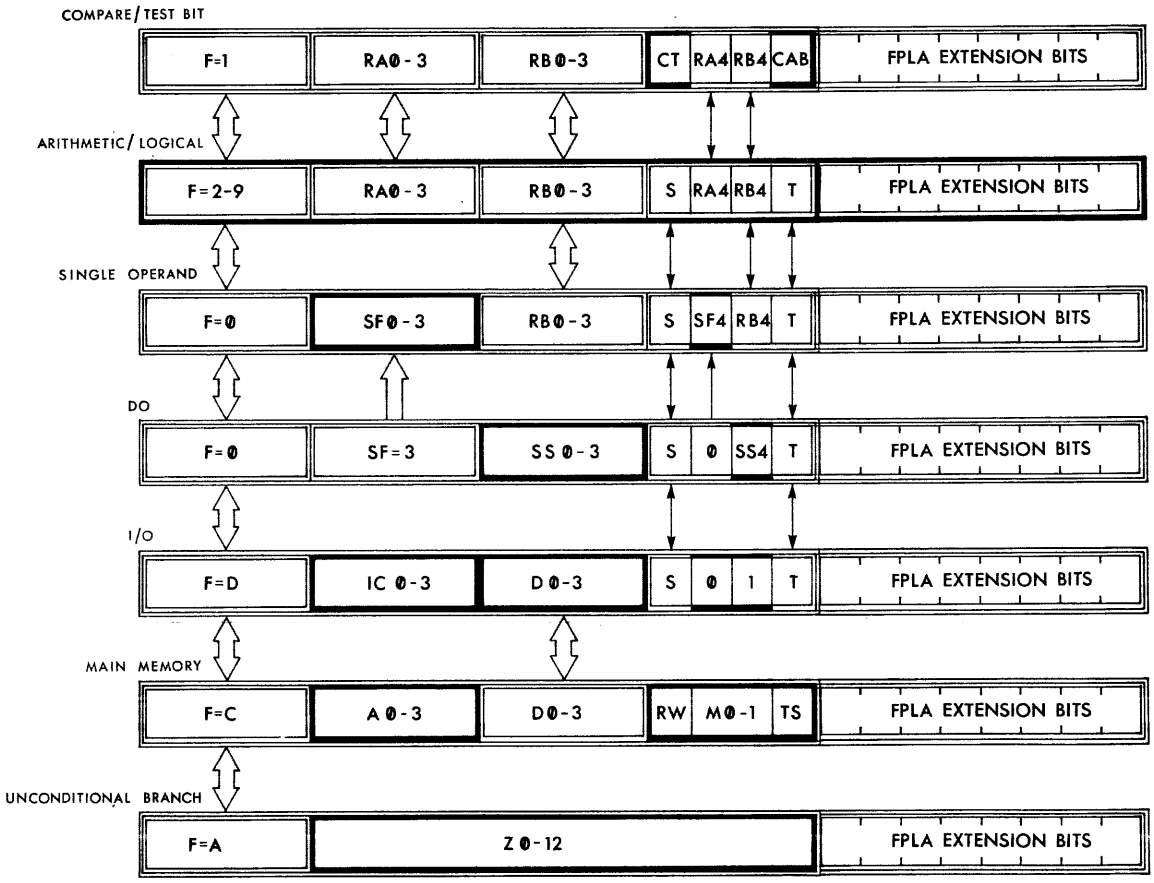


FIGURE 3-1

MICROINSTRUCTION FORMATS

4.0 THEORY OF OPERATION

This section provides a detailed gate-by-gate hardware explanation of the logic drawings included as Z folded pages at the end of this manual.

Several conventions are employed in this section to aid circuit explanation. Integrated circuit devices are specified by their board location coordinates (as, the Carry Lookahead Generator at 7F). A particular gate in an IC package is specified by its board location followed by the pin number of its principle output (as, the Nand gate at 2M-3).

Only very slight differences are found between the Q30 logics and the Q30R logics (pull-down resistors are found in places on the Q30R which are connected directly to ground on the Q30). However, the actual IC locations on the two boards differ radically. The set of Q30 logics reproduced at the end of this manual have been altered to also include the corresponding IC locations for each chip of the Q30R assembly as well. The IC locations for the Q30R chips are found encircled, on or beside the logic symbols.* The original Q30 chip locations remain in their original form (uncircled) on the logic drawings.

The discussion which follows in this chapter references the original Q30 IC locations NOT the encircled Q30R chip locations. The Q30R locations have been added only for emergency cross-references and to verify the similarity between the assemblies. Those working on Q30R boards are urged to order a set of Q30R logics (drawing number D32155) from the drafting department. The gate-by-gate hardware explanation in this section very sufficiently provides Theory of Operation documentation for both the Q30 and Q30R.

*When different pins in a multiple gate IC are used, the corresponding Q30 pin numbers are given around the encircled location.

Since FPLA intelligence performs instruction decoding, bus control, terms collection, and timing control, it is important for the technician to understand the FPLA output functions by their programmed product terms. This is essential for determining what microinstruction to enter via the test panel when a particular portion of the hardware is to be exercised and examined. Therefore, the transfer function expressions for the FPLA generated signals are included in this section. When expressed in terms of microinstruction fields, the specific field name will be abbreviated as done in Section 3 (for example, F=$2-9, Function Field equals 2 through 9). The transfer formula for each FPLA output signal is reduced to a simple sum of products expression, with the + symbol indicating logical OR and the · symbol indicating logical AND. A table of transfer formulas for all of the FPLA generated signals as well as the FPLA extension bits is given in Appendix A of this manual. Those interested in checking the FPLA expressions printed here will find a short discourse on "How to Read FPLA Listings" given in Appendix B.

The active state of the terms used in the FPLA logic equations are indicated by their suffix; -N indicating an active low signal, -P indicating an active high signal. For example, RB3-P indicates a logic high will be present on the RB3-P line when this bit is active. The negation sign will be used to indicate a signal in its inactive state. Therefore, $\overline{\text{RA4-P}}$ indicates a logic low on the RA4-P line. Likewise, $\overline{\text{INHSTS-N}}$ indicates a logic high on the active low INHSTS-N line.

Section 4.1 lists the signal acronyms used by the Q30 and Q30R logics and gives a brief definition of each acronym. Section 4.2 through 4.30 discuss the functioning of the hardware in detail beginning with Sheet 2 of the logics. The block diagram on Sheet 1 of the logics may be used for reference.

4.1 Q30 ACRONYMS

A3	Logical collection of the 2 most significant Ra terms
ACLKLO	Clock signal to the low byte 2901B devices
ACLKHI	Clock signal to the high byte 2901B devices
ADDCNX	Carry signal to the memory offset adders
ADDCNY	Carry signal to the memory offset adders
ADDCNZ	Carry signal to the memory offset adders
ADDR8/Ø-ADDR15/7	Eight bit multiplexed address sent to MEM7AR
ADDR16-ADDR19	Memory bank select signals sent to MEM7AR
AHI	Clock inhibit signal controlling ACLKHI
ALO	Clock inhibit signal controlling ACLKLO
ARAMHØ-ARAMH3	A port register file address to the high byte 2901B devices
ARAMLØ-ARAML3	A port register file address to the low byte 2901B devices
B3	Logical collection of the 2 most significant Rb terms
BASE	Base register address control signal used during Read and Write Base Reg. instructions
BASEHI	Decoded BUSCTL signal enables high 12 bits of selected base register onto 2901B Data In bus
BASELO	Decoded BUSCTL signal enables low 8 bits of selected base register onto 2901B Data In bus
BCLKHI	11MHz clock used in writing to Base Reg. RAM
BCONLOD	Buffered CONLOD signal routed to test panel
BRØ-BR15	Outputs of Base Register RAMs
BRAMØ-BRAM3	B port register file address to all 2901B
BUSCTLØ-BUSCTL2	Encoded bus enable information generated by the BUS CTL FPLA
BZAADRØ-BZADDR12	Z address bus to test panel
CCØ-CC2	Condition code, selects status bit for conitional branch test
CENA	C register clock generated by the Timing FPLA
CIPL	Operator's Initial Program Load button

Q30 ACRONYMS CONTINUED

CLHI	Free running 11 MHz processor clock
CLODI	Synchronized Conditional load signal
CLK	11MHz clock signal to test panel
CLK BHI	Write enable signal to the high 12 bits of the base registers
CLK BLO	Write enable signal to the low 8 bits of the base registers
CLKHI	11MHz processor clodk sent to the MEM7AR
CONLOD	Indicates conditional branch taken, loads the Z counter
CN+8	Carry out from low byte 2901B devices
CN+16	Carry out from high byte 2901B devices
CNX	Carry into low byte, high nibble 2901B from the carry lookahead generator
CNY	Carry into high byte, low nibble 2901B from the carry lookahead generator
CNZ	Carry into high byte, high nibble 2901B from the carry lookahead generator
CRY2	Historical carry flag from Status In register
CRYIN	Carry bit generated by MISC FPLA
CRYOUT	Carry bit from the status multiplexers
DAØØ-DA13	Backplane data bus
DATENA	Tri-state enable for Data In and Data Out buffers
DB=Ø	Data bus equals zero
DBH2H	Tri-state enable for high byte to high byte data buffer
DBH2L	Tri-state enable for high byte to low byte data buffer
DBL2L	Tri-state enable for low byte to low byte data buffer
DBIØ-DBI7	Data In bus to the low byte 2901B devices
DBI8-DBI15	Data In bus to the high byte 2901B devices

Q30 ACRONYMS CONTINUED

DBOØ-DBO7	Data Out bus from low byte 2901B devices
DBO8-DBO15	Data Out bus from high byte 2901B devices
DMCY	Dynamic memory cycle
DMOP	Dynamic memory operation
DMOP2	Delayed dynamic memory operation
DMWR	Dynamic memory write
D2Z	Enables data from ALU onto the Z counter load inputs during a multi-way branch
ECLK	FPLA generated E register clock
ENAC	Tri-state enable for the C register
ENAWRD	Enable signal to microprogram ROMs
ENRAM7•8	Enables carry flag onto the shifter node between the high and low byte 2901B devices
ENA STS	Enables contents of the Status In reg onto the low byte 2901B Data In bus
ESC11	Logical OR of the following status conditions: Enabled Interrupt, Stop Request, Start/stop, Parity Fault, Power failure
ESC21	Debounced IPL from the operator's panel
FØ-F3	The Function field in the E register
F=ØH	ALU status signal indicating a zero resultant in the high byte 2901B devices
F=ØL	ALU status signal indicating a zero resultant in the low byte 2901B devices
FLGCTLØ-FLGCTL1	Status control signals from the status FPLA
GADD3-GADD4	Carry generate signals from the memory offset adders
GENØ-GEN2	Carry generate signals from the 2901B devices
HALTIF	Half signal from the test panel
HLT LT	Control signal to Start/stop lamp on control panel
IOEØØ-IOEØ3	E bus, control bus used on I/O instructions
INCZ	Increment Z counter
INHSTS	Inhibit status on conditional load or state 7

Q30 ACRONYMS CONTINUED

Ix	Instruction control signal to all 2901B devices, x indicates number of signal (Ø-7)
IxH	Instruction control signal to high byte 2901B devices
IxHH	Instruction control signal to high byte, high nibble 2901B devices
IxHL	Instruction control signal to high byte, low nibble 2901B devices
IxL	Instruction control signal to low byte 2901B devices
LONG	Indicates long microinstruction cycle
MARØ-MAR14	Memory address register
MARENA	Clock signal to memory address register
MCLKHI	11MHz clock to memory board
MEMSIG	Memory signal, Mem check counter overflow
MSB2	Historical Most Significant Bit flag from Status In register
MSB7	Most Significant Bit signal from the low byte 2901B devices
MSB15	Most significant bit signal from tne high byte 2901B devices
MSB OUT	Most significant bit from the status multiplexers
MSTAT	Memory status signal
MWBØ-MWB23	Microword bus at the outputs of the microprogram ROMs
PADD3-PADD4	Carry propagate signal from the memory offset adders
PANMWØ-PANMW23	Buffered microword bus from microprogram ROMs to test panel
PAN WRT	Test panel write
PAR FLT	Parity fault
PDN1	Pull down resistor
PFL	Power failure
PRPØ-PRP2	Carry propagate from the 2901B devices

Q30 ACRONYMS CONTINUED

PURST	Pulse reset to sequence control logic
PWR DWN	Power down signal, controls the Power lamp on the operator's panel
RAØ-RA4	The Ra field from the E register
RA2B	Control signal to file address mux, routs the Ra field in the E register to the B port register address inputs of the 2901B devices
RA=RB	Ra field equals Rb field, bit in E register
RA2•CRY2	Enabled historical carry flag
RAMØ	The least significant bidirectional node of the cascaded shifter in the 2901B devices
RAM7•8	The midpoint bidirectional node of the cascaded shifter in the 2901B devices
RAM15	The most significant bidirectional node of the cascaded shifter in the 2901B devices
RBØ-RB4	The Rb field in the E register
READ	Read or Write operation, Function field = C
REEF	Refresh, indicates refresh in progress
REF REQ	Refresh request
REFRSH	Feedback signal to timing FPLAs
RF	Refresh signal sent to memory
RIP CRY	Ripple carry, tri-state buffer enable at the inputs of the carry lookahead generator
RSTZ	Reset Z counter
R/W	Read/Write bit in E register, also formatted as the S bit in microcode
S7	Timing state 7
SCENA	Preliminary C register clock
SCLKBHI	Preliminary Write Base Register high clock from BUS CTL FPLA
SCLKBLO	Preliminary Write Base Register low clock from BUS CTL FPLA
SMPCLK	Sample clock used as a switch debouncer
SRA2AL	Bit in E register, routs the Ra field to the A port address inputs of the low byte 2901B.

Q30 ACRONYMS CONTINUED

SRA2AH	Bit in E register, routs Ra field to A port register address inputs of the high byte 2901B
STB	Strobe signal from the sequence control logic
STDATA	Preliminary TDATA signal
STLOD	Preliminary TLOD signal
STP REQ	Stop request signal from the Power switch
STROBE	Strobe signal issued on the backplane
STS	Start/Stop from the operator's control panel
SUM12-SUM19	Outputs of the 8 most significant memory address offset adders
SYS RES	System reset
SZLOD	Preliminary ZLOD signal
T	Test bit from the E register
TØ-T2	Binary encoded processor timing states
TDATA	Transfer data
TDATA2	Preliminary TDATA signal
TLOD	Condition code multiplexer enable signal
UNCBR	Unconditional branch
QØ•Q15	Q shifter connection
Q7•8	Q shifter connection
QSTOP	Qantel instruction halt
XSCENA	C register clock at it origin, the TMG1 FPLA
XTDATA2	TDATA2 feedback signal at TMG1 FPLA
XDBIØ-XDBI15	Data bus routed to the test panel
Z2	Historical zero flag from Status In register
ZADDRØ-ZADDR12	Microprogram address from Z counter
ZBUSØ-ZBUS12	Branch address bus from Z register to Z counter
ZLOD	Z register clock signal
ZOUT	Zero bit from the status multiplexers
22MCLK-P	22MHz master clock used for synchronization

SHEET 2

4.2 HIGH BYTE 2901B DEVICES

The two high byte 2901B devices are located at 5A and 6A. The ARAMHØ-P through ARAMH3-P bus carries the A port register file address while the BRAMØ-P through BRAM3-P bus carries the B port register file address. The I signals are routed from the INST1 and INST2 FPLAs and perform the instruction control. Note that I_6 is not used and hardwired to ground. The data inputs of the 2901B devices are fed by the high byte Data In bus, DBI8-P through DBI15-P. However, if an active low PAN WRT-N is sent from the test panel to Octal Transceiver 11D, data on the test panel data bus (high byte) XDBI8-P through XDBI15-P will be enabled onto the D inputs of the high byte 2901B devices. Normally, with PAN WRT-N logically high, the contents of the high byte DBI8-P through DBI15-P bus is being enabled onto the test panel data bus (high byte) XDBI8-P through XDBI15-P. YØ through Y3, the outputs of the 2901B devices drive the high byte Data Out bus DBO8-P through DBO15-P. These outputs never enter tri-state mode since the output enable pins on the 2901B devices are hardwired logically low.

CNY-P is the Carry In signal to the high byte, low nibble 2901B at 6A. CNZ-P is the Carry In signal to the high byte, high nibble 2901B at 5A. GEN2-N (Carry Generate) and PRP2-N (Carry Propagate) are generated from 6A and routed to the carry look-ahead generator on Sheet 4. The F=Ø ALU status signal from 5A and 6A are tied together and pulled up by a resistor. When both 5A-11 and 6A-11 are generating a logical high, F=ØH-P is generated indicating a zero resultant in the high byte of an ALU operation. CN+16-P is the high byte Carry Out signal. MSB15-P is the high byte Most Significant Bit signal. MSB15-P, CN=16-P, and F=ØH-P are routed to the status multiplexers at the inputs of the Status In Register.

SHEET 2 CONTINUED

The bi-directional shifter outputs RØ and R3 are cascaded to provide left or right, shift or rotate operations. Since these operations may involve all four 2901B devices or just the high or low byte 2901B devices, the bi-directional RAM7·8-P line provides access to the least significant bit of the cascaded high byte 2901B devices (this is also connected to the most significant bit of the cascaded low byte 2901B devices). RAM7·8-P is routed to the status multiplexers.

The R3 shifter terminal at 5A-8 will function as an input on 16 bit or 8 bit high, shift right or rotate right instructions. (Shift Right, F=Ø·SF=Ø8). During both Shift Right and Rotate Right through Carry operations the least significant bit of the SF field is logically low. This appears as a low from the RAØ-P bit in the E Register, which drives 2L-6 high enabling Tri State Buffer 1M-8. If the instruction is a Rotate Right through Carry operation (F=Ø·SF=ØC), the RA2-P bit will be logically high in the E Register. On Sheet 3, RA2-P is Anded with CRY2-P the historical Carry bit held in the Status In Register. Thus, RA2·CRY2-P the enabled carry bit is shifted into 5A-8 on Rotate Right through Carry operations.

ACLKHI-P the clock signal for the high byte 2901B devices originates from the Timing 2 FPLA as the clock signal for both high and low byte 2901B devices. Two separate clock inhibit gates controlled by the BUS CTL FPLA generate ACLKHI-P and ACLKLO-P (the clock for the low byte 2901B devices).

The following tables relate the 2901B Instruction Control codes to their FPLA programmed logic equations. The Instruction Control signals are grouped according to their control function (source operand control, ALU function, and ALU destination control). Where separate I control signals are generated for the

high and low nibble of the cascaded 2901B byte it has been necessary to make 2 tables for the control function.

The following tables bring out some of the basic identities of the Instruction 1 and 2 FPLAs. Due to the nature of the FPLA firmware, the table cannot be simplified to discrete microcode instructions. Therefore, some overlapping of the active logic equations will exist. If the instruction in the E Register satisfies the requirements of two different logic equations that reside in the tables under different I field control codes, the active bits must be superimposed to form a new code. In the FPLA some I signals are programmed as active high while others require fewer product terms if programmed as active low. Thus, an H (high) or L (low) has been indicated above each I signal column in the tables. In the event multiple logic equations are satisfied and I codes must be superimposed, an H will indicate a logic 1 will take precedence over a Ø in the column. Likewise, an L indicates a Ø as an active state, being able to pull down any 1 generated by a superimposed code.

TABLE D

HIGH BYTE LOW NIBBLE

ALU SOURCE OPERAND R	ALU SOURCE OPERAND S	I2H-P (L)	I1H-P (H)	IØHL-P (H)	LOGIC EQUATION
		Ø	Ø	Ø	NOT USED
A	B	Ø	Ø	1	F=Ø•RA3-P•RA4-P +F=Ø•$\overline{\text{RA2-P}}$•$\overline{\text{RAØ-P}}$•RA4-P +F=1-8•Ra≠Rb•$\overline{\text{RA4-P}}$•$\overline{\text{RB4-P}}$ +F=1-8•Ra≠Rb•$\overline{\text{RA3-P}}$•$\overline{\text{RB4-P}}$ +F=1-8•Ra≠Rb•RA3-P•RA4-P
		Ø	1	Ø	NOT USED
Ø	B	Ø	1	1	F=C,E•$\overline{\text{TDATA2-N}}$•RA4-P
Ø	A	1	Ø	Ø	F=9•Ra≠Rb•RA3-P•RA4-P•$\overline{\text{RB4-P}}$ +F=9•Ra≠Rb•RA3-P•$\overline{\text{RB3-P}}$•RB4-P
D	A	1	Ø	1	F=1-8•Ra≠Rb•$\overline{\text{RA3-P}}$•$\overline{\text{RB3-P}}$•RB4-P +F=1-8•Ra≠Rb•$\overline{\text{RB3-P}}$•$\overline{\text{RA4-P}}$•RB4-P +F=2-8•Ra=Rb•RA3-P•RA4-P•$\overline{\text{R/W-P}}$•T-P +F=2-7•Ra=Rb•RA3-P•RA4-P•R/W-P +F=8•Ra=Rb•RA3-P•RA4-P +F=Ø-8
		1	1	Ø	NOT USED
D	Ø	1	1	1	F=1-8•RA4-P•$\overline{\text{RB4-P}}$ +F=1-8•$\overline{\text{RB3-P}}$•RA4-P +F=9•Ra=Rb•$\overline{\text{T-P}}$ +F=9•Ra=Rb•R/W-P +F=9•Ra≠Rb•RB3-P•$\overline{\text{RA4-P}}$•RB4-P +F=9•Ra≠Rb•$\overline{\text{RA3-P}}$•RB3-P•RB4-P +F=Ø +F=C

TABLE E

HIGH BYTE HIGH NIBBLE

ALU SOURCE OPERANDS R	S	I2H-P (L)	I1H-P (H)	IØHH-P (H)	LOGIC EQUATION
		Ø	Ø	Ø	NOT USED
A	B	Ø	Ø	1	F=1-8
		Ø	1	Ø	NOT USED
Ø	B	Ø	1	1	F=C•$\overline{\text{TDATA2-N}}$•RA4-P
Ø	A	1	Ø	Ø	F=9•Ra≠Rb•RA3-P•RA4-P•$\overline{\text{RB4-P}}$ +F=9•Ra≠Rb•RA3-P•$\overline{\text{RB3-P}}$•RB4-P
D	A	1	Ø	1	F=1-8•Ra≠Rb•$\overline{\text{RA3-P}}$•$\overline{\text{RB3-P}}$•RB4-P +F=1-8•Ra≠Rb•$\overline{\text{RB3-P}}$•$\overline{\text{RA4-P}}$•RB4-P +F=2-8•Ra=Rb•RA3-P•RA4-P•$\overline{\text{R/W-P}}$•T-P +F=2-7•Ra=Rb•RA3-P•RA4-P•R/W-P +F=8•Ra=Rb•RA3-P•RA4-P
		1	1	Ø	NOT USED
D	Ø	1	1	1	F=1-8•$\overline{\text{RB3-P}}$•RA4-P +F=1-8•RA4-P•$\overline{\text{RB4-P}}$ +F=9•$\overline{\text{RA3-P}}$•RB3-P•Ra≠Rb•RB4-P +F=9•RB3-P•Ra≠Rb•$\overline{\text{RA4-P}}$•RB4-P +F=9•Ra=Rb•R/W-P +F=9•Ra=Rb•$\overline{\text{T-P}}$ +F=C,D

TABLE F

HIGH BYTE HIGH NIBBLE

ALU FUNCTION	I_5 H	I_{4H} L	I_3 L	LOGIC EQUATION
R Plus S	Ø	Ø	Ø	F = 2 +F = 4 +F = Ø•SF = 12
S Minus R	Ø	Ø	1	F = 1,3,5•Ra≠Rb +F = 1,3,5•$\overline{\text{T-P}}$ +F = 1,3,5•R/W-P +F = Ø•SF = 1Ø +F = 9•RA4-P•$\overline{\text{RB4-P}}$ +F = 9•$\overline{\text{RA3-P}}$•Ra=Rb•$\overline{\text{R/W-P}}$•RA4-P•T-P +F = C,E•$\overline{\text{TDATA2-N}}$•RA4-P•RB4-P +F = C,E•$\overline{\text{TDATA2-N}}$•RA4-P•$\overline{\text{RB4-P}}$
R Minus S	Ø	1	Ø	F = 1•Ra=Rb•T-P +F = 3,5•Ra=Rb•$\overline{\text{R/W-P}}$•T-P +F = C,E•HALTIF-P•$\overline{\text{TDATA2-N}}$•RA4-P•$\overline{\text{RB4-P}}$ +F = C,E•$\overline{\text{TDATA2-N}}$•$\overline{\text{HALTIF-P}}$•RA4-P•RB4-P
R OR S	Ø	1	1	F = Ø•$\overline{\text{RA4-P}}$ +F = Ø•$\overline{\text{RA3-P}}$ +F = Ø•RA3-P•$\overline{\text{RA4-P}}$•$\overline{\text{RB4-P}}$ +F = Ø•RA3-P•$\overline{\text{RAØ-P}}$•$\overline{\text{RA4-P}}$ +F = Ø•RA3-P•RB3-P•$\overline{\text{RA4-P}}$ +F = 1,3,5,7,C,D,E +F = 2-9•Ra=Rb•$\overline{\text{R/W-P}}$•T-P +F = 9•RA3-P•Ra=Rb•$\overline{\text{R/W-P}}$•RA4-P•T-P +F = 9•Ra=Rb•$\overline{\text{T-P}}$ +F = 9•Ra=Rb•R/W-P +F = 9•RB3-P•$\overline{\text{RA4-P}}$•RB4-P +F = 9•$\overline{\text{RA3-P}}$•RB3-P•RB4-P

TABLE F cont.

HIGH BYTE HIGH NIBBLE CONTINUED

	H	L	L	
ALU FUNCTION	I_5	I_{4H}	I_3	LOGIC EQUATION
R AND S	1	Ø	Ø	F = 8 +F = Ø·SF = Ø1 +F = 1·$\overline{R/W-P}$
	1	Ø	1	NOT USED
R EX-OR S	1	1	Ø	F = 6,9
R EX-NOR S	1	1	1	F = Ø·SF = 18, 1A

TABLE G

HIGH BYTE LOW NIBBLE

Y OUTPUT	SHIFT	LOAD	I_{8H} H	I_{7L} L	I_6 L	LOGIC EQUATION
F	X	NONE	Ø	Ø	Ø	F=Ø•SF=18,1A +F=Ø•RA3-P•$\overline{\text{RAØ-P}}$•$\overline{\text{RA4-P}}$ +F=2-9•Ra=Rb•$\overline{\text{R/W-P}}$•T-P
			Ø	Ø	1	NOT USED
A	NONE	F ► B	Ø	1	Ø	F=2-9,C,D,E +F=Ø•SF=Ø1,1Ø,12 +F=Ø•$\overline{\text{RA4-P}}$ +F=Ø•$\overline{\text{RA3-P}}$ +F=1•$\overline{\text{R/W-P}}$ +F=1,3,5•Ra≠Rb +F=1,3,5•$\overline{\text{T-P}}$
			Ø	1	1	NOT USED
F	DOWN	F/2 ► B	1	Ø	Ø	F=Ø SF=08,0C
			1	Ø	1	NOT USED
F	UP	2F ► B	1 1	1 1	Ø Ø	F=Ø•RA3-P•$\overline{\text{RA4-P}}$•$\overline{\text{RB4-P}}$ +F=Ø•RA3-P•RB3-P•$\overline{\text{RA4-P}}$
			1	1	1	NOT USED

TABLE H

HIGH BYTE HIGH NIBBLE
H L L

Y OUTPUT	SHIFT	LOAD	I_{8H}	I_{7HH}	I_6	LOGIC EQUATION
F	X	NONE	Ø	Ø	Ø	F=Ø•RA3-P•$\overline{\text{RAØ-P}}$•$\overline{\text{RA4-P}}$ +F=2-9•Ra=Rb•$\overline{\text{R/W-P}}$•T-P
			Ø	Ø	1	NOT USED
A	NONE	F ➤ B	Ø	1	Ø	F=2-9, C,D,E +F=Ø•SF=Ø1, 1Ø, 12, 18, 1A +F=Ø•$\overline{\text{RA4-P}}$ +F=Ø•$\overline{\text{RA3-P}}$ +F=1•$\overline{\text{R/W-P}}$ +F=1,3,5 • Ra≠Rb +F=1,3,5 •$\overline{\text{T-P}}$
			Ø	1	1	NOT USED
F	DOWN	F/2 ➤ B	1	Ø	Ø	F=Ø SF=08,0C
			1	Ø	1	NOT USED
F	UP	2F ➤ B	1	1	Ø	F=Ø•RA3-P•$\overline{\text{RA4-P}}$•$\overline{\text{RB4-P}}$ +F=Ø•RA3-P•RB3-P•$\overline{\text{RA4-P}}$
			1	1	1	NOT USED

SHEET 3

4.3 LOW BYTE 2901B DEVICES

The two low byte 2901B devices are located at 2A and 3A. ARAMLØ-P through ARAML3-P carries the A port register file address while BRAMØ-P through BRAM3-P carries the B port register file address. The I signals are routed from the INST1 and INST2 FPLAs. The I_6 inputs are not used and hardwired to ground. The data inputs of the 2901B devices are fed by the low byte Data In bus, DBIØ-P through DBI7-P. However, if an active low PAN WRT-N is sent from the test panel to the Octal Transceiver 13D, data on the test panel data bus (low byte) XDBØ-P through XDB7-P will be enabled onto the the D inputs of the low byte 2901B devices. Normally, with PAN WRT-N logically high, the contents of the low byte DBIØ-P through DBI7-P bus is being enabled onto the test panel data bus (low byte) XDBØ-P through XDB7-P. The data outputs YØ through Y3 drive the low byte Data Out bus DBOØ-P through DBO7-P. Again, these outputs never enter tri-state mode, the output enable pins on the 2901B devices are hardwired low.

CRYIN-P the carry signal input to the 2901B at 3A is generated by the MISC FPLA. CRYIN-P is generated during Add with Carry and Subtract with Carry operations if the Carry flag in the Status In Register is set. During memory operations (F=C), The modify bits can specify an automatic increment or decrement of the memory address pointer. This is accomplished by respectively adding or subtracting the carry bit from the present address pointer value. CRYIN-P is also generated during Subtract operations to indicate Borrow Not. CNX-P is the Carry In signal to the low byte, high nibble 2901B device 2A from the Carry Lookahead Generator. GENØ-N (Carry Generate) and PRPØ-P (Carry Propagate) from 3A and GEN1-N and PRP1-N from 2A are routed to the inputs of the Carry Lookahead Generator.

SHEET 3 CONTINUED

The F=Ø ALU status signal from 2A and 3A are tied together and pulled up by a resistor. When both 2A-11 and 3A-11 are generating a logical high, F=Ø-P is generated indicating a zero resultant in the low byte of an ALU operation. CN+8-N is the low byte Carry Out signal. MSB7-P is the Most Significant Bit for 8 bit low operations. MSB7-P, CN+8-P, and F=Ø-P are routed to the status multiplexers at the inputs of the Status In Register.

R3, the shifter access point at 2A-8 will perform as an output on all shift or rotate left operations and will perform as an input on all shift or rotate right operations. During Rotate through Carry instructions (F=Ø•SF=ØC,ØD) the carry bit (CRY2-P) will be enabled through And gate 2M-3 by RA2-P generating RA2•CRY2-P. If an 8 bit high or 8 bit low register is specified by the Rb field during a Rotate through Carry instruction, the STATUS FPLA will generate ENRAM7•8-P enabling Tri State Buffer 1M-3.

On Rotate Left through Carry (F=Ø•SF=ØD) bits RA2-P and RAØ-P from the E Register will be logically high. This enables RA2•CRY2-P from 2M-3 through Tri State Buffer 1M-11 onto the RØ node of 3A-9 which will be functioning as an input.

The Q shifter access points (QØ, Q3) are simply tied into a closed loop comprising all four 2901B devices. The Q shifter is not used by the Q30.

The following tables relate the I Control signal activity to the microinstruction present in the E Register. The logic equations illustrate some of the basic identities decoded by the INST1 and INST2 FPLA for the low byte 2901B devices. These tables are functionally similar to the tables given for the high byte 2901B devices and all that has been said about the tables in Section 4.2 likewise applies to these tables.

TABLE I

ALU SOURCE OPERANDS R	ALU SOURCE OPERANDS S	LOW BYTE L I2L	LOW BYTE H I1L	LOW BYTE H IØL	LOGIC EQUATION
		Ø	Ø	Ø	NOT USED
A	B	Ø	Ø	1	F=1-8•$\overline{RB3-P}$•Ra≠Rb•$\overline{RA4-P}$•RB4-P +F=1-8•Ra≠Rb•$\overline{RA4-P}$•$\overline{RB4-P}$ +F=1-8•$\overline{RA3-P}$•$\overline{RB3-P}$•Ra≠Rb•RB4-P +F=Ø•$\overline{RA2-P}$•$\overline{RAØ-P}$•RA4-P +F=Ø•RA3-P•RA4-P +F=2,3,6,7•Ra≠Rb•$\overline{RB4-P}$ +F=1,4-8•$\overline{RA3-P}$•Ra≠Rb•$\overline{RB4-P}$ +F=C,E•$\overline{TDATA2-N}$•RA4-P
		Ø	1	Ø	NOT USED
		Ø	1	1	NOT USED
Ø	A	1	Ø	Ø	F=1-8•RA3-P•Ra≠Rb•RA4-P +F=1-8•RA4-P•$\overline{RB4-P}$ +F=1-8•$\overline{RB3-P}$•RA4-P +F=9•RB3-P•Ra=Rb•$\overline{RA4-P}$•RB4-P +F=9•$\overline{RA3-P}$•RB3-P•Ra≠Rb•RB4-P
D	A	1	Ø	1	F=Ø-8
		1	1	Ø	NOT USED
		1	1	1	F=Ø +F=2-8•RA3-P•Ra=Rb•$\overline{R/W-P}$•RA4-P•T-P +F=2-7•RA3-P•Ra=Rb•R/W-P•RA4-P +F=8•RA3-P•Ra=Rb•RA4-P

TABLE J

ALU FUNCTION	H I_5	L I_{4L}	L I_3 LOW BYTE	LOGIC EQUATION
R Plus S	Ø	Ø	Ø	F=2 +F=4 +F=Ø•SF=12
S minus R	Ø	Ø	1	F=1,3,5•Ra≠Rb +F=1,3,5•$\overline{\text{T-P}}$ +F=1,3,5•R/W-P +F=Ø•SF=1Ø +F=C,E•$\overline{\text{TDATA2-N}}$•RA4-P•RB4-P +F=C,E•$\overline{\text{TDATA2-N}}$•RA4-P•$\overline{\text{RB4-P}}$ +F=9•RA3-P•Ra=Rb•$\overline{\text{R/W-P}}$•RA4-P•T-P
R minus S	Ø	1	Ø	F=1•Ra=Rb•T-P +F=3,5•Ra=Rb•$\overline{\text{R/W-P}}$•T-P +F=C,E•HALTIF-P•TDATA2-N•RA4-P•$\overline{\text{RB4-P}}$ +F=C,E•$\overline{\text{TDATA2-N}}$•$\overline{\text{HALTIF-P}}$•RA4-P•RB4-P
R or S	Ø	1	1	F=Ø•$\overline{\text{RA4-P}}$ +F=Ø•$\overline{\text{RA3-P}}$ +F=Ø•RA3-P•$\overline{\text{RA4-P}}$•$\overline{\text{RB4-P}}$ +F=Ø•RA3-P•$\overline{\text{RAØ-P}}$•$\overline{\text{RA4-P}}$ +F=Ø•RA3-P•RB3-P•$\overline{\text{RA4-P}}$ +F=1,3,5,7,C,D,E +F=2-9•Ra=Rb•$\overline{\text{R/W-P}}$•T-P +F=9•Ra=Rb•$\overline{\text{T-P}}$ +F=9•Ra=Rb•R/W-P +F=9•RB3-P•$\overline{\text{RA4-P}}$•RB4-P +F=9•$\overline{\text{RA3-P}}$•RB3-P•RB4-P

TABLE J cont.

LOW BYTE CONTINUED

ALU FUNCTION	H I_5	L I_{4L}	L I_3	LOGIC EQUATION
R and S	1	Ø	Ø	F=8 +F=Ø·SF=Ø1 +F=1·$\overline{R/W-P}$
	1	Ø	1	NOT USED
R EX-OR S	1	1	Ø	F=6,9
R EX-NOR S	1	1	1	F=Ø·SF=18,1A

TABLE K

LOW BYTE

Y OUTPUT	SHIFT	LOAD	H I_{8L}	L I_{7L}	L I_{6L}	LOGIC EQUATION
F	X	NONE	Ø	Ø	Ø	F=2-9·Ra=Rb·$\overline{R/W-P}$·T-P +F=Ø·SF=18,1A +F=D·IC=2,3,F
			Ø	Ø	1	NOT USED
A	NONE	F ► B	Ø	1	Ø	F=2-9·Ra≠Rb
			Ø	1	1	NOT USED
F	DOWN	F/2 ► B	1	Ø	Ø	F=Ø·SF=08,0C
			1	Ø	1	NOT USED
F	UP	2F ► B	1	1	Ø	F=Ø·SF=09, 0D
			1	1	1	NOT USED

SHEET 4

4.4 CARRY LOOAHEAD GENERATOR

The carry lookhead generator at 7F provides flash carry signals to the 3 most significant 2901B devices by sensing the Carry Generate and Carry Propagate signals outputted by the 3 least significant 2901B devices. RIPCRY-P controls the Multiplexer at 8F. RIPCRY-P is logically high during all operations employing 16 bit and 8 bit low ALU operands. RIPCRY-P is generated by the Miscellaneous FPLA and is programmed to go inactive (logically low) when the Rb field specifies an 8 bit high register according to the following logic equation:

$$\overline{\text{RIPCRY-P}} = \text{F=Ø-9,D} \cdot \text{RB3-P} \cdot \text{RB4-P}$$

The CRYIN-P signal enables the Carry Propagate signals (PRPØ-N, PRP1-N, PRP2-N) into the carry lookahead generator, allowing them to propagate left towards the more significant carry outputs. The Carry Generate signals (GENØ-N, GEN1-N, GEN2-N) have more significance than their corresponding Carry Propagate signals and immediately cause a carry to the next more significant 2901B device, as well as enabling propagated carries to higher significant nibbles. The carry signals generated by the Carry Lookahead Generator conform to the following logic equations:

$$\text{CNX-P} = \text{GENØ-N} + \text{PRPØ-N} \cdot \text{CRYIN-P}$$

$$\text{CNY-P} = \text{GEN1-N} + \text{PRP1-N} \cdot \text{GENØ-N} + \text{PRP1-N} \cdot \text{PRPØ-N} \cdot \text{CRYIN-P}$$

$$\text{CNZ-P} = \text{GEN2-N} + \text{PRP2-N} \cdot \text{GEN1-N} + \text{PRP2-N} \cdot \text{PRP1-N} \cdot \text{GENØ-N} + \text{PRP2-N} \cdot \text{PRP1-N} \cdot \text{PRPØ-N} \cdot \text{CRYIN-P}$$

The CRYIN-P signal to the Carry Lookahead Generator is issued from the Miscellaneous FPLA when the microinstruction in the E register meets one of the following identities:

SHEET 4 CONTINUED

$$\begin{aligned}\text{CRYIN-P=}\quad & F=\emptyset \cdot RA4\text{-}P \cdot \overline{RA3\text{-}P} \cdot \overline{RA2\text{-}P} \cdot RA1\text{-}P \ (SF=\$12,13)\\ & +F=1 \cdot R/W\text{-}P \ (CT \text{ bit})\\ & +F=3\\ & +F=4,5 \cdot CRY2\text{-}P\\ & +F=C \cdot HALTIF\text{-}P \cdot RA4\text{-}P \cdot \overline{RB4\text{-}P} \ (M=\$2)\\ & +F=C \cdot \overline{HALTIF\text{-}P} \cdot RA4\text{-}P \cdot RB4\text{-}P \ (M=\$3)\end{aligned}$$

When RIPCRY-P is low it disables carry information from the two low byte 2901B devices when the Rb (destination) field specifies an 8 bit high register. CRYIN-N is enabled through the Multiplexer 8F instead of GEN1-N and PRP1-N is deselected and the Carry Lookahead Generator input is held high by a pull-up resistor (R23 at 8E). During all operations employing 16 bit and 8 bit low ALU operands RIPCRY-P is logically high selecting GEN1-N and PRP1-N through the Multiplexer at 8F.

4.5 IOE AND STROBE BUFFERS

During I/O instructions (F=D), the four least significant bits of the Ra field become the IC field (which specifies the particular I/O microinstruction). The $D in the Function field nibble of the E register is decoded by Nand gate 7M-8. The low from 7M-8 enables RAØ-P through RA3-P (the IC field) through the inverting Tri-State Buffer at 2C onto the active-low backplane IOE bus. The low from 7M-8 is inverted, enabling Nand gate 6F-6, which allows the STROBE-N signal onto the backplane. SSTB-P (strobe) is generated by the TMG2 (timing 2) FPLA according to the following formula:

$$\begin{aligned}SSTB\text{-}P = \ & F=D \cdot S1\\ & +F=D \cdot S4\end{aligned}$$

SHEET 4 CONTINUED

SSTB-P is pipelined and becomes STB-P, which appears at Nand gate 6F-6 during timing states S4 and S5 of I/O instructions.

When a $D is not present in the Function Field nibble of the E register, Nand gate 7M-8 outputs a high enabling the Tri-State Buffers 8M-6,8. Since the inputs to these TSBs are grounded the IOEØ3-N and IOEØ2-N lines are forced active-low. This provides extra protection, making it impossible for any code lower than $C to be erroneously strobed into a controller.

Power supply bypass and despiking capacitors are shown at the right of Sheet 4 along with the finger numbers for the supply lines and ground returns. The supply lines followed by the subscript R (+5VR, +12VR, -12VR) are separate power buses for supplying battery backup during power failure.

SHEET 5

4.6 MEMORY ADDRESS REGISTER

The memory address register (MAR) consists of two Tri-State octal Latches at 7E and 4F. MARHI the high byte of the Memory Address Register (7E) is loaded from the data output bus DBO8-P through DBO15-P from the two high byte 2901B devices. The MARLO register (4F) is the low byte of the Memory Address Register. MARLO is loaded from DBO8-P through DBO15-P via Tri-State Buffer 4A or from the DBOØ-P through DBO7-P data out bus from the low byte 2901B devices.

The MAR Octal Latches 7E and 4F are transparent (gate the data present at their inputs directly through to their outputs) when MARENA-P (MAR enable) is active high. The negative-going trailing edge of MARENA-P latches the data present at the inputs. This data value is held as long as MARENA-P is logically low. MARENA-P is a pipelined version of the XSCENA-P signal from the TMG1 FPLA.

Octal Latch 4F has its tri-state control input always enabled (4F-1). Octal Latch 7E is normally enabled, but its outputs are driven into tri-state mode when BASE-P goes logically high. BASE-P comes from combinational gating on Sheet 19 and is generated during Read Base High, Read Base Low, Write Base High, and Write Base Low microinstructions. During these instructions the Base register address is supplied by the 4 most significant bits of the register file locations specified instead of the MAR11-P through MAR14-P bits.

SHEET 5 CONTINUED

4.7 DATA BUS BUFFERING

DBH2L-N (Data Bus High to Low) the enable signal for Tri-State buffer 4A is driven active low by the conditions listed below:

$$\begin{aligned} \text{DBH2L-N} = \; & F=1\text{-}9 \cdot Ra \neq Rb \cdot \overline{RB3\text{-}P} \\ & + F=1\text{-}9 \cdot Ra \neq Rb \cdot \overline{RB4\text{-}P} \\ & + F=C,E \cdot RB3\text{-}P \cdot TDATA2\text{-}N \\ & + F=\emptyset,D \cdot RB3\text{-}P \cdot RB4\text{-}P \end{aligned}$$

The high byte data output bus DBO8-P through DBO15-P may be enabled onto the backplane data bus DAØØ-P through DA13-P when Tri-State Buffer 4A is enabled by DBH2L-N and Tri-State Buffer 1A is enabled by a logically low DATENA-P. Tri-State Buffer 1A is normally enabled. DATENA-P goes logically high upon the occurence of the following conditions:

$$\begin{aligned} \text{DATENA-P} = \; & F=C \cdot TDATA2\text{-}N \cdot R/W\text{-}P \\ & + F=D \cdot IC=\emptyset,1,8,9 \end{aligned}$$

DBO8-P through DBO15-P can be routed to the data in bus of the two low byte 2901B devices (DBIØ-P through DBI7-P) if DBH2L-N enables Tri-State Buffer 4A and DBL2L-N (data bus low to low) enabled Tri-State Buffer 1C. DBL2L-N goes active low under the following situations:

$$\begin{aligned} \text{DBL2L-N} = \; & F=\emptyset \cdot SF=\emptyset,1 \\ & + F=1\text{-}9 \cdot Ra \neq Rb \\ & + F=C \cdot \overline{TDATA2\text{-}N} \end{aligned}$$

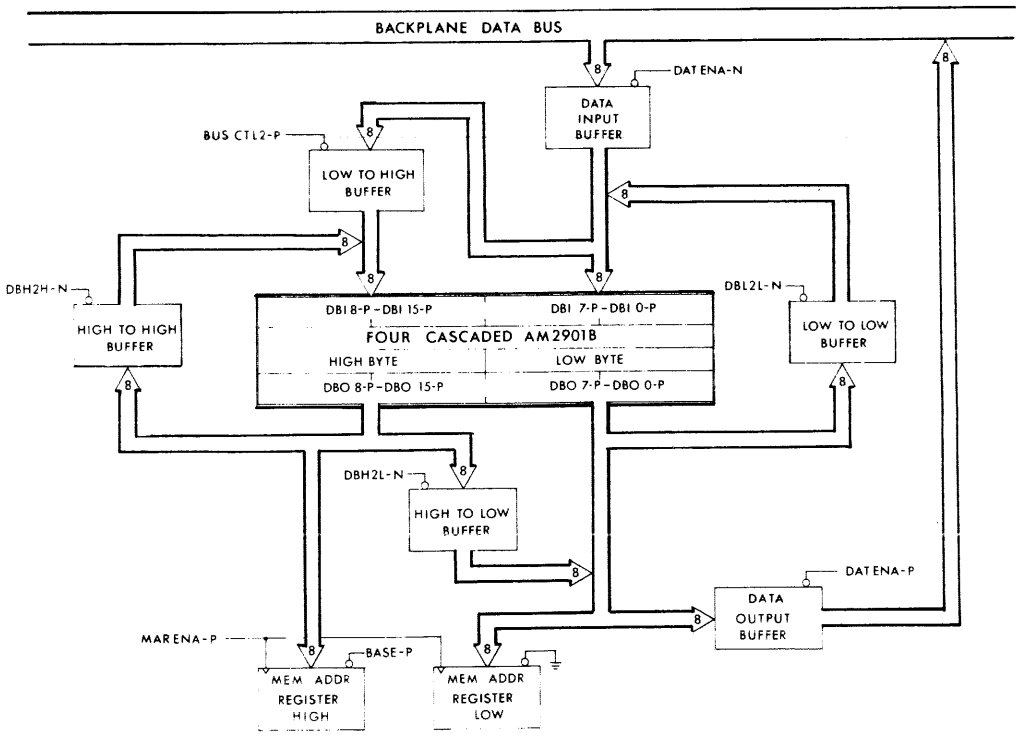
SHEET 5 CONTINUED

Tri-State Buffer 4B residing on the data input bus of the two high byte 2901B devices is enabled when BUSCTL2-P is logically low. BUSCTL2-P is logically low under the following conditions:

$$\overline{\text{BUSCTL2-P}} = \text{F=}\emptyset\ \overline{\text{RA3-P}}\ \text{RA2-P}\ \text{RA1-P}\ \overline{\text{RA}\emptyset\text{-P}}\ \overline{\text{RA4-P}}\ (\text{SF=}\emptyset 6)$$
$$+\text{F=C}\ \text{TDATA2-N}\ \text{R/W-P}$$
$$+\text{F=D}\ \text{IC=}\emptyset,1,8,9$$

Data entering the Q30 from the system backplane is enabled through Tri-State Buffer 1B by an active low DATENA-N signal. DATENA-N is simply the inverse of DATENA-P whose transfer function is given earlier. Therefore, when the Data In Buffer 1B is enabled the Data Out Buffer 1A is disabled and vice versa.

The dual 5 input Nor gate at 1E along with the And gate 2E-6 form a zero detector. An active high DB=Ø-P is generated from 2E-6 when all lines of the low byte data bus (DBIØ-P through DBI7-P) are logically low.



SHEET 6

4.8 FLAG REGISTERS

The Q30 Flag Registers are made up of the Status In Register 12J and the Status Out Register 4K. The Status In Register is an Octal Latch and is updated by the positive transition of each ECLK-P. The register records the following conditions: PFL-P (Power Failure), PAR FLT-P (Parity Fault), Start Stop, and Power Down Request (from the operator's panel), Enabled Interrupt, MSB OUT-P (Most Significant Bit), Z OUT-P (Zero), and CRY OUT-P (Carry).

ESC11-P (Escape 11) is generated from Nand gate 11K-8 whenever the Power Failure, Parity Fault, Start/Stop, Stop Request, or Enabled Interrupt bit is asserted in the Status In Register. PFL-N from Inverter 1J-3 is routed to the backplane to notify I/O controllers and memory in the event of a power failure.

The contents of the Status In Register are enabled onto the low byte 2901B Data In bus (DBIØ-P through DBI7-P) when ENA STS-N goes active low enabling Tri-State Buffer 13J. ENA STS-N is generated by the Input Flag Register microinstruction:

$$\text{ENA STS-N} = F=Ø \cdot \overline{RA3\text{-}P} \cdot RA2\text{-}P \cdot RA1\text{-}P \cdot \overline{RAØ\text{-}P} \cdot \overline{RA4\text{-}P}$$

The contents of the Status In Register may thus be moved into any register file location specified by the Input Flag Register microinstruction.

The MSB-P, Z2-P, and CRY2-P bits are the historical status bits. If status updating has been inhibited in the microinstruction (S bit logically low) the MSB2-P, Z2-P, and CRY2-P signals will

be selected by the status multiplexer (sheet 12) and reclocked into the Status In Register by the next positive-going edge of ECLK-P.

The Status Out Register 4K is a quad two-input multiplexer with an internal negative-edge triggered latch. The outputs of 4K are fed back to the second input of each of the quad two-input multiplexer inputs. Each negative-going transition of the ECLK-N signal latches the information present at the selected inputs of the device. Nand gate 3J-8 is normally high selecting the fed back outputs of 4K. Each ECLK-N thus reclocks the previously latched information.

A logically high FLG CTLØ-P and RA2-P drives Nand gate 3J-8 logically low and causes the DBO3-P through DBO6-P (2901B data output bus) bits to the selected inputs of 4K. The "Write to Flag Register" microinstruction (F=Ø, SF=Ø4) generates FLG CTLØ-P and drives Nand gate 3J-8 logically low, causing the Ø3 through Ø6 bits of the specified register file location to be selected at 4K and clocked into its internal latch by the next ECLK-N.

A logical high clocked into 4K (by ECLK-N) from the DBO3-P line (during a Write to Flag register) enables Nand gate 10L-11. INT-N (interrupt) from the backplane can then drive 10L-11 low. The low is clocked into the Status In Register and generates from 11K-8 the ESC11-P signal which is routed to the condition code multiplexer.

The power drivers at 10J-3 and 10J-5, when their outputs are low, provide a current sink path for the operator's panel Halt lamp and Power lamp respectively. The low from Inverter 5F-10 also generates QSTOP-N which indicates a machine instruction halt to the test panel.

SHEET 6 CONTINUED

The 8 bit register with common clear at 2J serves as a switch debouncer. Activation of the STS-N (Start/Stop)pushbutton or CIPL-N (Initial Program Load) pushbutton drives Nand gate 1K-6 high, removing the direct reset from 2J. SMP CLK-P (most signif icant Refresh Counter bit clocks a high into 2J from the activated switches. The outputs of 2J are fed back and reclocked through the chip again by SMP CLK-P. Any switch depressed for at least two SMP CLK-P pulses will pass through 2J. All switch contact bounce and noise is avoided. The activated signal will remain active at the outputs of 2J for one SMP CLK period after the switch is deactivated.

4.9 POWER-UP RESET LOGIC

The power-up reset logic is shown at the right end of Sheet 6. Assume, the +5V and +5VS (memory refresh standby supply) are both off. As the machine is powered on, both supplies rise towards +5 volts. No voltage drop is developed across the 47 µfd. capacitor as power comes up. When the +5V supply has risen enough to avalanche bias the Zener diode to 3.3 volts the current through the voltage divider at the base of the transistor turns the transistor on. The event of the Zener reaching its 3.3 volt level insures that all chips on the board have reached their minimum supply voltage for safe operation. The forward biased transistor provides a short to ground for one end of the 47 µfd. capacitor. This causes the voltage at both ends of the capacitor to drop to zero volts since the voltage across a capacitor cannot be changed instantaneously. This drives 2K-6 high and generates RSTZ-P (reset Z counter) from 1K-8, RSTZ-N from 2L-4, and SYS RES-N (System Reset) from 1J-9.

SHEET 6 CONTINUED

Reset Z remains active for approximately 40 msec. as the end of the 47 ufd. capacitor connected to 2K-4,5 charges toward +5 volts, eventually causing 2K-6 to go low, sending Reset Z and System Reset back to their inactive state.

In the event of a power failure, the +5V supply would dropout and the transistor would not be forward biased. The 47 µfd. capacitor would discharge until zero voltage drop is across the capacitor (both leads of the capacotor would reach +5VS, the standby supply voltage). The high at the transistor's collector would force RSTZ and SYS RES active. Note, Reset Z and System Reset can also be generated when CIPL-N (IPL from the operator's panel) generates ESC21-P if the IPL mini-jumper is installed.

SHEET 7

4.10 CONDITION CODE MULTIPLEXER

The condition code multiplexer 8H is addressed by CCØ-P through CC2-P, the condition code bits from the Z register. CCØ-P through CC2-P select the proper input to the 8 to 1 line multiplexer. TLOD-N the enable signal for 8H causes the selected input to be present at the complementary outputs of 8H. TLOD-N originates from the STLOD-N signal generated by the TMG2 FPLA:

$$
\begin{aligned}
\text{STLOD-N} = {} & \text{F=2-9}\cdot\text{S5}\cdot\text{Ra}\neq\text{Rb}\cdot\text{T-P} \\
& +\text{F=2-9}\cdot\text{S5}\cdot\text{R/W-P}\cdot\text{T-P} \\
& +\text{F=2-9}\cdot\overline{\text{HALTIF-N}}\cdot\text{SØ},\ \text{S1}\cdot\overline{\text{CLOD1-P}}\cdot\overline{\text{LONG-P}}\cdot\text{Ra=Rb} \\
& \quad \cdot\text{T-P} \\
& +\text{F=4-9}\cdot\overline{\text{HALTIF-N}}\cdot\text{SØ},\ \text{S1}\cdot\text{CLOD1-P}\cdot\overline{\text{LONG-P}}\cdot\text{R/W-P} \\
& \quad \cdot\text{T-P} \\
& +\text{F=1}\cdot\overline{\text{HALTIF-N}}\cdot\text{SØ},\ \text{S1}\cdot\overline{\text{CLOD1-P}}\cdot\overline{\text{LONG-P}}\cdot\text{T-P} \\
& +\text{F=1}\cdot\overline{\text{HALTIF-N}}\cdot\text{SØ},\ \text{S1}\cdot\overline{\text{CLOD1-P}}\cdot\overline{\text{LONG-P}}\cdot\text{Ra=Rb} \\
& +\text{F=Ø}\cdot\overline{\text{HALTIF-N}}\cdot\text{SØ},\ \text{S1}\cdot\overline{\text{CLOD1-P}}\cdot\text{T-P} \\
& +\text{F=C}\cdot\text{S5}\cdot\text{DMOP-N}\cdot\text{MEMSIG-N}\cdot\text{R/W-P}\cdot\text{T-P} \\
& +\text{F=D}\cdot\text{S5}\cdot\text{T-P} \\
& +\text{F=1}\cdot\text{S5}\cdot\text{T-P} \\
& +\text{F=1}\cdot\text{S5}\cdot\text{Ra=Rb} \\
& +\text{F=2,3,6,7}\cdot\overline{\text{HALTIF-N}}\cdot\text{SØ},\ \text{S1}\cdot\overline{\text{CLOD1-P}}\cdot\overline{\text{LONG-P}} \\
& \quad \cdot\overline{\text{R/W-P}}\cdot\text{T-P}
\end{aligned}
$$

The signal is delayed one processor state through a pipeline register before being presented to the Condition Code Multiplexer 8H as TLOD-N.

The Condition Code Multiplexer can thus test for the presence or absence of the Carry, Zero, or Most Significant Bit in the ALU status bits or test for the occurence of ESC11-P (Enabled Interrupt, Stop Request, Start/Stop, Parity Fault, or Power Failure) or ESC21-P (IPL).

SHEET 7 CONTINUED

If the tested condition (specified by CCØ-P through CC2-P) is present, CON LOD-N goes active low driving Negative Or gate 7H-11 low. This causes the Z Counter to synchronously parallel load from the Z bus with the branch address held in the Z Register.

4.11 Z COUNTER

The Z Counter consisting of the cascaded counters 11B, 12B, 11A, and 12A generates the 13 bit ZADDRØ-P through ZADDR12-P address to the microprogram ROMs.

The Z Counters are clocked by the free-running 11MHz CLKHI-N. However, to increment the counters must be enabled by INCZ-P (increment Z Counter) prior to the positive-going edge of CLKHI-N. INCZ-N is generated by the TMG2 FPLA and is inverted once before being routed to the Z Counters as INCZ-P.

$$
\begin{aligned}
\text{INCZ-N} = \; & F{=}1\text{-}9 \cdot \overline{\text{HALTIF-N}} \cdot S\text{Ø} \cdot Ra{=}Rb \\
& + F{=}\text{Ø}\text{-}9 \cdot \overline{\text{HALTIF-N}} \cdot S\text{Ø} \cdot T\text{-}P \\
& + F{=}2\text{-}9 \cdot S5 \cdot R/W\text{-}P \cdot Ra{=}Rb \cdot T\text{-}P \\
& + F{=}1 \cdot S5 \cdot Ra{=}Rb \\
& + S6 \\
& + F{=}D \cdot \overline{\text{HALTIF-N}} \cdot S\text{Ø} \cdot T\text{-}P \cdot \overline{\text{CLOD-P}} \\
& + F{=}C,E \cdot \overline{\text{HALTIF-N}} \cdot S\text{Ø} \cdot R/W\text{-}P \cdot T\text{-}P \\
& + S\text{Ø} \cdot \text{CLOD-P}
\end{aligned}
$$

Since INCZ is not pipelined, it is generated during the timing states noted above, only the propagation delay through the FPLA needs to be considered. Negative Or gate 7H-11 can also be driven low (generating a synchronous load signal to the Z Counters) when a low is generated from the branch decoders formed of the Nand gates, And gate and Inverter 12M-6,8, 13M-8 and 11M-6.

SHEET 7 CONTINUED

13M-8 may be driven low by either the unconditional branch decoder 12M-6 or the multi-way branch decoder 12M-8.

During an unconditional branch (Opcode $A), if CLOD1 is inactive, Nand gate 12M-6 will go low except when disabled by an active T1-P (encoded time state signal).

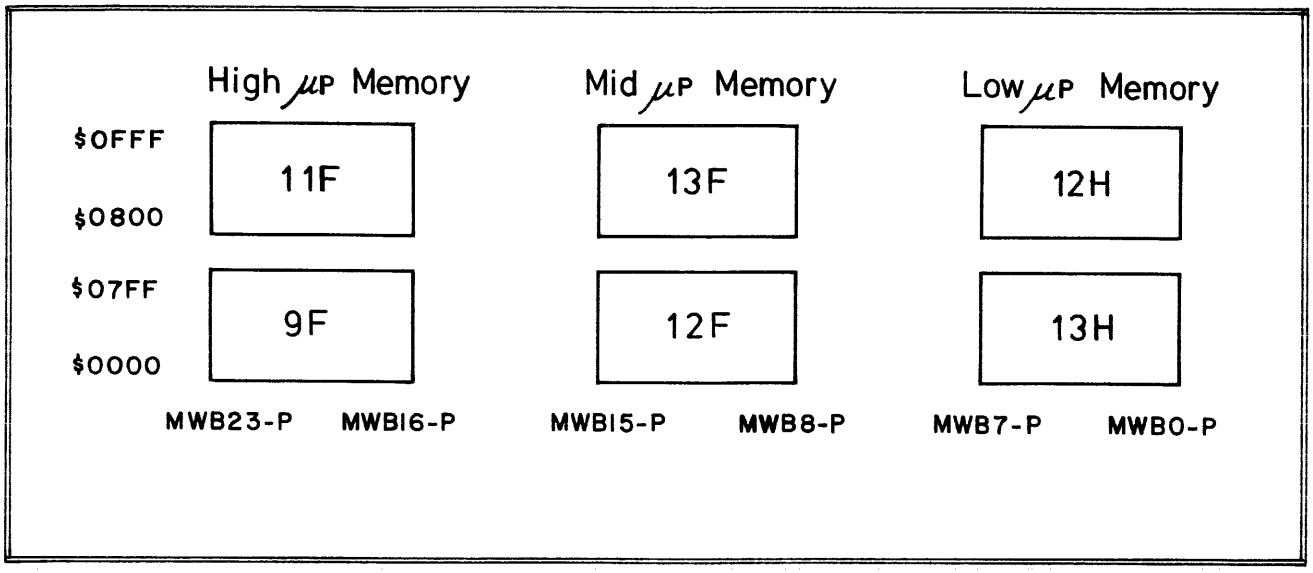
Nand gate 12M-8 senses the multi-way branch signal D2Z-P (inversion of the E register FPLA Extension bit D2Z-N). D2Z-P is strobed through 12M-6 when the encoded time state signals specify state 5. 12M-6 drives 13M-8 and 7H-11 low enabling a synchronous parallel load of the Z counters on the next positive-going transition of CLKHI-N. The branch address is enabled from the DBØØ-P through DB11-P bus onto the parallel load inputs of the Z counters when D2Z-N enables the Tri-State Buffers at 10A and 10B.

The Tri-State Buffers at 13A and 13B buffer the Z counter outputs onto the BZADDRØ-P through BZADDR11-P bus which goes to the test panel via P3.

SHEETS 8 & 9

4.12 MICROPROGRAM ROMS

The microprogram ROMs are shown on Sheets 8 and 9. Each ROM chip is 8 bits wide and 2K deep. Three ROMs are enabled at a time creating a 4K by 24 bit block. ENWRD-N is generated during SØ (State Ø) when the ZADDR bus value is less than $1000. ZADDR11-P and ZADDR12-N are used to select/enable the ROM groups. The following memory map correlates the ROM chip address boundaries to their physical location on the Q30 assembly.



SHEET 10 and 11

4.13 INSTRUCTION REGISTERS

The 16 bit C and Z Registers and the 24 bit E Register are shown on Sheets 10 and 11. They are loaded from the MWB bus (microword from the ROMs).

Octal Flip Flops 8D, 11E, and 7D are used for the E Register. The tri-state outputs of the E Register are always enabled. A new microword is clocked into the E Register by a positive-going transition of ECLK-P. This signal originates as SECLK-P from the TMG 1 FPLA.

$$\begin{aligned} \text{SECLK-P} &= S\emptyset \cdot \text{CLOD1-P} \\ &\quad + S6 \\ &\quad + S7 \end{aligned}$$

SECLK-P is pipelined once and appears as ECLK-P one state later than the states mentioned above. Notice, the hardware names for the 24 bits of the E Register are the signal names used for the FPLA logic equations given in the Appendix.

Tri-state gated latches are used for the C Regiater (11C and 12D). The C Register is transparent while the clock signal (CENA-P) is logically high as long as the tri-state outputs are enabled. The negative-going transition of CENA-P latches the data present at the Register inputs. CENA-P always occurs 1 processor state following each ECLK-P. The C Register outputs are normally in tri-state mode. ENAC-N (Enable C) goes active-low only when a microword of constant data follows the microinstruction.

$$\text{ENAC-N} = F{=}1\text{-}B \cdot Ra{=}Rb$$

The Z Register 10C and 8C is clocked by ZLOD-P (Z Register Load). This signal originates from the TMG 2 FPLA as $\overline{\text{SZLOD-N}}$.

$$
\begin{aligned}
\overline{\text{SZLOD-N}} \;=\; & \text{F=1}\cdot\overline{\text{HALTIF-N}}\cdot\text{SØ,S1}\cdot\text{Ra=Rb} \\
& +\text{F=2-9}\cdot\text{S5}\cdot\text{R/W-P}\cdot\text{Ra=Rb}\cdot\text{T-P} \\
& +\text{F=Ø-9}\cdot\overline{\text{HALTIF-N}}\cdot\text{SØ,S1}\cdot\text{T-P} \\
& +\text{F=1}\cdot\text{S5}\cdot\text{Ra=Rb} \\
& +\text{S6} \\
& +\text{S7} \\
& +\text{F=D}\cdot\overline{\text{HALTIF-N}}\cdot\text{S1}\cdot\text{T-P} \\
& +\text{F=C,E}\cdot\overline{\text{HALTIF-N}}\cdot\text{SØ,S1}\cdot\text{R/W-P}\cdot\text{T-P} \\
& +\text{SØ}\cdot\text{CLOD1-P}
\end{aligned}
$$

$\overline{\text{SZLOD-N}}$ is pipelined and arrives one processor state later as ZLOD-P. The tri-state enable signal to the Z Register D2Z-P is the inversion of D2Z-N, a bit in the microintruction held in the E Register. D2Z-P goes logically high sending the Z Register outputs into tri-state mode only during a multi-way branch.

SHEET 12

4.14 STATUS FLAG MULTIPLEXERS

The STATUS FPLA generates the enable and select addresses for the Carry Multiplexer 6J, the Zero Multiplexer 7J, and the Most Significant Bit Multiplexer (MSB Mux) 8J. The Zero and MSB mux are addressed by the same signals while the STATUS FPLA 6D generates unique select addresses for the Carry Multiplexer.

The STATUS FPLA instructs the multiplexers to select the appropriate status flag depending on the specific instruction. Examine the inputs to the Carry Multiplexer 6J. For different Shift or Rotate operations, the righthand, lefthand, or between byte carry from the 2901B shifters can be selected. During arithmetic operations the ALU Carry signal from the most significant nibble of the low byte or the high byte 2901B devices can be selected. The DBØØ-P line can be selected, routing the least significant bit of the selected register file location through the multiplexer. If status updating has been inhibited, CRY2-P the Carry Status signal held in the Status In Register as a result of a previous operation is selected by the Carry Multiplexer.

The Zero Multiplexer 7J can select the ALU Zero Status signal from the low byte or high byte 2901B device, or the output of the Data Bus Zero detector DB=Ø-P. When READ-P is high (READ-P is active high on any memory operation, read or write) the B inputs to Multiplexer 9H are selected. The $Ø2 weight bit from any selected register file location, routed via the DB01-P line, can be selected, or, Z2-P the historical zero status bit already in the Status In Register can be selected if status updating has been inhibited. The logical And of both the high and low byte Zero status signal from the 2901B devices is pro-

vided to the Zero Multiplexer inputs through And gate 7H-6.

The Most Significant Bit Multiplexer 8J can select from the low byte or high byte ALU most significant bit status signal, the $Ø4 weight bit from any selected register file location, or if status updating has been inhibited, the MSB2-P historical status signal. On any memory read or write operation, READ-P will be active-high, selecting DBI7-P (most significant bit of the data bus) through Multiplexer 9H.

The outputs of the MSB, Zero, and Carry Multiplexers are routed to the Status In Register and to the Condition Code Multiplexer. Notice that the least significant bit of the select address to the MSB and Zero Mux is driven by RB3-P which is low when 8 bit low or 16 bit register file locations are specified.

The multiplexer select address codes are tabulated with the logic equations (for generating each select code) in Tables L and M. The Carry Multiplexer select codes (Table L) are separate from the Zero and MSB mux select codes (Table M) since different FPLA outputs drive the Carry Multiplexer. The multiplexer's selected input signal combinations must be present at the STATUS FPLA inputs to generate the specific select codes.

Some explanation of the terms used in the logic equations of Table L and M is necessary. To simplify the table, all product terms with the function field equal to Ø (single operand) have their Ra field given as SF (secondary function field). However, all other signals retain their hardware signal name as it appears in the E Register. For example, while the R/W-P signal is the E Register hardware name, when F=Ø,2-9,D this is the S bit (Status update enable).

SHEET 12 CONTINUED

The term INHSTS-N is the active-low output from Nor gate 7H-8. This signal goes active-low only during timing State 7 (only when the test panel is attached) or when a conditional branch is taken. When the logic equation requires $\overline{\text{INHSTS-N}}$ this demands that 7H-10 be logically high (inactive).

FLG CTLØ-P is generated from the STATUS FPLA on a Write to Flag Register instruction:

$$\text{FLG CTL}\emptyset\text{-P} = \text{F}=\emptyset \cdot \overline{\text{RA3-P}} \cdot \text{RA2-P} \cdot \overline{\text{RA1-P}} \cdot \overline{\text{RA}\emptyset\text{-P}} \cdot \overline{\text{INHSTS-N}} \cdot \overline{\text{RA4-P}}$$

This signal enables new data to be clocked into the Status Out Register.

FLG CTL1-P from the STATUS FPLA is generated by the following equations:

$$\begin{aligned}\text{FLG CTL1-P} = {} & \text{F}=\emptyset \cdot \overline{\text{RA3-P}} \cdot \text{RA2-P} \cdot \overline{\text{RA1-P}} \cdot \overline{\text{RA}\emptyset\text{-P}} \cdot \overline{\text{INHSTS-N}} \cdot \overline{\text{RA4-P}} \\ & + \text{F}=\emptyset \cdot \text{RA3-P} \cdot \overline{\text{RA}\emptyset\text{-P}} \cdot \overline{\text{INHSTS-N}} \cdot \text{RA4-P} \\ & + \text{F}=\emptyset \cdot \overline{\text{RA3-P}} \cdot \overline{\text{RA2-P}} \cdot \text{RA1-P} \cdot \text{RA}\emptyset\text{-P} \cdot \overline{\text{INHSTS-N}} \cdot \overline{\text{RA4-P}}\end{aligned}$$

If FLG CTL1-P and RAØ-P is logically high, And gate 7H-3 goes high and disables the MSB, Zero, and Carry Multiplexers. This occurs only on the "DO" instruction (F=Ø, SF=Ø3, SS=ØØ) which clears the MSB, Zero and Carry bits in the Status In Register.

ENRAM7•8 from the STATUS FPLA goes active during the shift and rotate group of instructions when the Rb field specifies an 8 bit low register file location. If the instruction is a Rotate Left through Carry, ENRAM7•8 will enable the historical carry bit (CRY2-P) onto the cascaded 2901B RAM Shifter Bus between the high byte and low byte 2901B devices.

TABLE L

CARRY MUX

SELECTED INPUT SIGNAL	SELECT CODE C	B	A	LOGIC EQUATION
RAMØ-P	Ø	Ø	Ø	F = Ø·SF = Ø8,ØC·$\overline{\text{RB3-P}}$·RB4-P·$\overline{\text{INHSTS-N}}$·R/W-P +F = Ø·SF = Ø8,ØC·$\overline{\text{INHSTS-N}}$·R/W-P·$\overline{\text{RB4-P}}$
RAM7·8-P	Ø	Ø	1	F = Ø·SF = Ø8,ØC·RB3-P·RB4-P·$\overline{\text{INHSTS-N}}$·R/W-P +F = Ø·SF = Ø9,ØD·$\overline{\text{RB3-P}}$·RB4-P·$\overline{\text{INHSTS-N}}$·R/W-P
RAM15-P	Ø	1	Ø	F = Ø·SF = Ø9,ØD·$\overline{\text{INHSTS-N}}$·R/W-P·$\overline{\text{RB4-P}}$ +F = Ø·SF = Ø9,ØD·RB3-P·R/W-P·$\overline{\text{INHSTS-N}}$
GROUND	Ø	1	1	NOT USED
Cn+8-P	1	Ø	Ø	F = 2-5·$\overline{\text{RB3-P}}$·RB4-P·$\overline{\text{INHSTS-N}}$·R/W-P +F = Ø·SF = 1Ø,12·$\overline{\text{RB3-P}}$·RB4-P·$\overline{\text{INHSTS-N}}$·R/W-P +F = 1·$\overline{\text{RB3-P}}$·Ra = Rb·$\overline{\text{INHSTS-N}}$·R/W-P +F = 1·$\overline{\text{RB3-P}}$·RB4-P·$\overline{\text{INHSTS-N}}$·R/W-P·$\overline{\text{T-P}}$
Cn+16-P	1	Ø	1	F = 2-7·$\overline{\text{INHSTS-N}}$·R/W-P·$\overline{\text{RB4-P}}$ +F = 2-7·RB3-P·$\overline{\text{INHSTS-N}}$·R/W-P +F = Ø·SF = 1Ø,12·$\overline{\text{INHSTS-N}}$·R/W-P·$\overline{\text{RB4-P}}$ +F = Ø·SF = 1Ø,12·RB3-P·$\overline{\text{INHSTS-N}}$·R/W-P +F = 1·$\overline{\text{INHSTS-N}}$·R/W-P·$\overline{\text{RB4-P}}$ +F = 1·RB3-P·$\overline{\text{INHSTS-N}}$·R/W-P +F = 1·Ra = Rb·$\overline{\text{INHSTS-N}}$·R/W-P·T-P
DBØØ-P	1	1	Ø	F = Ø·SF = Ø5·$\overline{\text{INHSTS-N}}$
CRY2-P	1	1	1	DEFAULT CONDITION

T A B L E M

MSB MUX ZERO MUX

SELECTED INPUT SIGNAL	SELECTED INPUT SIGNAL	SELECT CODE C	B	A	LOGIC EQUATION
MSB7-P	F = ØL-P	Ø	Ø	Ø	F = Ø•SF = Ø8,Ø9,ØC,ØD,1Ø,12•R/W-P•$\overline{\text{INHSTS-N}}$•RB4-P +F = 2-5•$\overline{\text{INHSTS-N}}$•R/W-P•RB4-P +F = 1•$\overline{\text{INHSTS-N}}$•R/W-P•RB4-P•T-P +F = 1•Ra = Rb•$\overline{\text{INHSTS-N}}$•R/W-P +F = 1•Ra = Rb•$\overline{\text{INHSTS-N}}$•R/W-P•T-P +F = Ø•SF = Ø8,Ø9,ØC,ØD•$\overline{\text{INHSTS-N}}$•R/W-P•$\overline{\text{RB4-P}}$ +F = 1•$\overline{\text{INHSTS-N}}$•R/W-P•$\overline{\text{RB4-P}}$ +F = Ø•SF = Ø8,ØC•$\overline{\text{INHSTS-N}}$•RB4-P +F = Ø•SF = 18,1A,1C,1E•$\overline{\text{INHSTS-N}}$ +F = Ø•SF = 10,12•$\overline{\text{INHSTS-N}}$•R/W-P
MSB15-P	F = ØH-P	Ø	Ø	1	F = Ø•SF = Ø3•$\overline{\text{INHSTS-N}}$ +F = Ø•SF = Ø8,Ø9,ØC,ØD,1Ø,12•$\overline{\text{INHSTS-N}}$•R/W-P•$\overline{\text{RB4-P}}$ +F = Ø•SF = Ø8,Ø9,ØC,ØD•$\overline{\text{INHSTS-N}}$•R/W-P•RB4-P +F = Ø•SF = Ø9,ØD,1Ø,12•$\overline{\text{INHSTS-N}}$•R/W-P +F = 1-7•$\overline{\text{INHSTS-N}}$•R/W-P•$\overline{\text{RB4-P}}$ +F = 1-7•$\overline{\text{INHSTS-N}}$•R/W-P +F = 1•Ra = Rb•$\overline{\text{INHSTS-N}}$•R/W-P•T-P +F = Ø•SF = 18 1A,1C,1E
MSB15-P	F = ØL-P F = ØH-P	Ø	1	X	F = 2,3,6,7•$\overline{\text{Ra4-P}}$•$\overline{\text{RB4-P}}$ +F = 1,4-9,•$\overline{\text{RB4-P}}$ +F = Ø•$\overline{\text{R/W-P}}$•RA4-P +F = Ø•RA4-P•$\overline{\text{RB4-P}}$ +F = Ø•RA3-P•$\overline{\text{R/W-P}}$ +F = Ø•RA3-P•$\overline{\text{RB4-P}}$ +F = Ø•$\overline{\text{RA2-P}}$•$\overline{\text{R/W-P}}$ +F = Ø•$\overline{\text{RA2-P}}$•$\overline{\text{RB4-P}}$ +F = Ø•RA1-P•$\overline{\text{R/W-P}}$ +F = Ø•RA1-P•$\overline{\text{RB4-P}}$

X = Don't Care

TABLE M CONTINUED

MSB MUX ZERO MUX

SELECTED INPUT SIGNAL	SELECTED INPUT SIGNAL	SELECT CODE C	B	A	LOGIC EQUATION
DBO2-P	DBO1-P	1	Ø	X	F = Ø•SF = Ø5 +F = Ø•SF = Ø4
MSB2-P	Z2-P	1	1	X	F = 2-F•$\overline{\text{R/W-P}}$ +F = A,B +F = C•$\overline{\text{R/W-P}}$•$\overline{\text{T-P}}$ +F = C•$\overline{\text{TDATA2-N}}$ + INHSTS-N

X = Don't Care

SHEET 13

4.15 INSTRUCTION AND ADDRESS DECODING

The INST 1 FPLA generates some of the Instruction Control signals for the 2901B devices. If the signal name has no direct alphabetic subscript (as I5-P) it is routed to all four 2901B devices. If there is a single alphabetical character subscript (as I2L-P) it is routed to two 2901B devices (the L indicates the two low byte 2901B). If two alphabetical character subscripts are given (as IØHH-P) the signal goes to a specific 2901B device (the HH indicates high byte, high nibble). I7L-P is an exception to the rule and is routed to the 3 least significant 2901B devices. The signal RA2B-P causes the file address multiplexers to switch the microinstruction's Ra field onto the B port register file address inputs of the 2901B devices. RA2B-P is generated from 7L-6 during the data transfer portion of a memory access operation (F=C·TDATA-N).

While the microinstruction formats allow for a 5 bit Ra field and Rb field, the fifth bit specifies if all 16 bits or if only 8 bits (high or low byte) of the register file location will be used. However, the 2901B devices have register file address ports only 4 bits wide. A logically high RB3-P or RB4-P will generate B3-P from 3J-3. B3-P is the most significant bit of the Rb field register file address routed to the 2901B devices via the file address multiplexers. TDATA-N also generates B3-P during the data transfer period of a memory access operation.

SCLKBHI-P (Set Base Register Clock High) and SCLKBLO-P (Set Base Register Clock Low) are the select enable signals used in the generation of the write enable clocks for the base registers.

$$\text{SCLKBHI-P} = \text{F=Ø}\cdot\text{SF=1A}\cdot\overline{\text{CLOD1-P}}$$
$$\text{SCLKBLO-P} = \text{F=Ø}\cdot\text{SF=18}\cdot\overline{\text{CLOD1-P}}$$

The signals ALO-N and AHI-N from the FPLA at 4D are clock inhibit signals. They have the ability to inhibit the FPLA generated 2901B clock (SACLK) from reaching either the low byte or high byte 2901B devices.

ALO-N inhibits the clock to the low byte 2901B devices. ALO-N is generated by the following identities:

$$\begin{aligned}\text{ALO-N} = {} & \text{F=Ø-B,D}\cdot\text{RB3-P}\cdot\text{RB4-P}\\ & +\text{F=2-9}\cdot\text{Ra=Rb}\cdot\overline{\text{R/W-P}}\cdot\text{T-P}\\ & +\text{F=C}\cdot\text{RB3-P}\cdot\text{TDATA2-N}\\ & +\text{F=C}\cdot\text{TDATA2-N}\cdot\overline{\text{R/W-P}}\\ & +\text{F=C}\cdot\text{TDATA2-N}\cdot\overline{\text{RB4-P}}\\ & +\text{F=D}\cdot\text{RA1-P}\\ & +\text{F=D}\cdot\text{RA2-P}\\ & +\text{F=A,B}\\ & +\text{F=1}\\ & +\text{F=Ø}\cdot\text{SF=ØØ,Ø3,Ø4,Ø5,18,1A}\end{aligned}$$

AHI-N inhibits the clock to the high byte 2901B devices:

$$\begin{aligned}\text{AHI-N} = {} & \text{F=Ø-B,D}\cdot\overline{\text{RB3-P}}\cdot\text{RB4-P}\\ & +\text{F=2-9}\cdot\text{Ra=Rb}\cdot\overline{\text{R/W-P}}\cdot\text{T-P}\\ & +\text{F=C}\cdot\overline{\text{RB3-P}}\cdot\text{TDATA2-N}\\ & +\text{F=C}\cdot\text{TDATA2-N}\cdot\overline{\text{R/W-P}}\\ & +\text{F=C}\cdot\overline{\text{TDATA2-N}}\cdot\overline{\text{RA4-P}}\\ & +\text{F=D}\cdot\text{RA1-P}\\ & +\text{F=D}\cdot\text{RA2-P}\end{aligned}$$

SHEET 13 CONTINUED

```
          AHI-N   = +F=A,B
(continued)       +F=1
                  +F=Ø·SF=ØØ,Ø3,Ø4,Ø5,18,1A
```

The Bus Control signals BUS CTLØ-P through BUS CTL2-P are decoded on Sheet 15. The decoded Bus Control signals specify what sources have access to the principle data buses. A table relating the decoded tri-state enable signals to the BUS CTL logic equations is given in the explanation of Sheet 15 (Bus Control Decoder). The logic equations for each specific BUS CTL signal is given in the Appendix.

SHEET 14

4.16 INSTRUCTION AND MISCELLANEOUS DECODING

The INST 2 FPLA generates the remainder of the I Control signals for the 2901B devices. These signals are discussed in the explanation of Sheet 2 and 3 (2901B devices) and are given in the Appendix.

The MISC FPLA generates various control signals, bus enable signals, and timing control signals. Notice, the historical carry signal CRY2-P and HALTIF-P (halt signals from the test panel) are input to the FPLA. The logic equations for RIPCRY and CRYIN have been given int the explanation of Sheet 4. DBH2L and DBL2L have been identified in the explanation of Sheet 5. READ-P is generated during and memory operation:

$$\text{READ-P} = \text{F=C}$$

D2Z-N from the microinstruction in the E Register, is high during a multi-way branch. D2Z-N is inverted by 5F-8 to become D2Z-P the signal that controls the tri-state outputs of the Z Register.

4.17 REGISTER FILE ADDRESS MULTIPLEXERS

The file address multiplexers 5C, 3C, 4C are situated between the outputs of the E Register and the A and B register address ports of the 2901B devices. A unique A port register address may be sent to the high byte and the low byte 2901B devices by the ARAMHØ-P through ARAMH3-P and ARAMLØ-P through ARAML3-P buses respectively. The B port register address, used to specify the register file destination for resultant data, is routed to all four 2901B devices via the BRAMØ-P through BRAM3-P

bus. Only one B file address multiplexer is needed, since, writing to an 8 bit high or 8 bit low register file location is performed by inhibiting the clock signal to the two undesired 2901B devices.

Each multiplexer has the ability to select either the Ra field or the Rb field of the microinstruction. This is necessary to permit ALU operations with any combination of 8 bit high register, 8 bit low register, or 16 bit register operand manipulation.

SRA2AH-P and SRA2AL-P (microinstruction bits from the E Register) are the selection control signals to the file address multiplexers 5C and 3C. An active high SRA2AH-P selects the Ra field (RAØ-P through RA2-P and A3-P) for the high byte 2901B A port register address bus ARAMHØ-P through ARAM3-P. Likewise, an active high SRA2AL-P selects the Ra field for the low byte 2901B A port register address bus ARAMLØ-P through ARAML3-P.

RA2B-P is the selection control signal for the B port file address multiplexers 4C. An active high RA2B-P causes the Ra field to be selected through the mux at 4C and be placed on the B port register file address bus. RA2B-P is only high during the data transfer portion of a memory operation. Notice, if RA2B-P is high and SRA2AH-P and/or SRA2AL-P are high at Exclusive-Or gates 9C-3 and 9C-6, the Rb field can be placed onto the A port register file address bus (high and/or low byte).

SHEET 15

4.18 BUS CONTROL DECODER

The Octal Decoder at 8E decodes the Bus Control signals BUSCTLØ-P through BUSCTL2-P from the BUSCTL FPLA. The decoder is disabled only by PAN WRT-N (Panel Write) from the test panel. The following signals are generated from 8E: BASEHI-N and BASELO-N are tri-state enable signals for the buffers which allow the contents of the selected base register onto the Data In bus of the 2901B devices. DBH2H-N enables the high byte of data out of the 2901B devices onto the Data In bus of the same 2901B devices. ENAC-N is routed to the tri-state output control pins of the C Register, enabling constant data from the C Register onto the Data In bus of the 2901B devices. DAT ENA-N and DAT ENA-P are the tri-state enable signals for the Data In and Data Out Buffers respectively (interfacing the CPU with the backplane Data Bus). ENA STS-N enables the tri-state buffer which places the contents of the Status In Register onto the Data In bus of the low byte 2901B devices. Table N given below summarizes the decoded bus control signals and expresses what logic equations generated the specific BUS CTL codes.

TABLE N

BUS CTL2-P	BUS CTL1-P	BUS CTLØ-P	DECODED SIGNAL	LOGIC EQUATION
Ø	Ø	Ø	NOT USED	
Ø	Ø	1	ENA STS-N	F=Ø·SF=Ø6
Ø	1	Ø	NOT USED	
Ø	1	1	DAT ENA-P DAT ENA-N	F=C·TDATA2-N·R/W-P +F=C HALTIF-P +F=D·IC=0,1,8,9
1	Ø	Ø	ENAC-N	F=1-B·Ra=Rb
1	Ø	1	DBH2H-N	F=Ø·SF=ØØ,Ø2 +F=C·$\overline{\text{TDATA-N}}$
1	1	Ø	BASELO-N	F=Ø·SF=1C
1	1	1	BASEHI-N	F=Ø·SF=1E

SHEET 15 CONTINUED

4.19 CLOCK AND REFRESH REQUEST LOGIC

All processor timing is derived from the hybrid 22 MHz oscillator module at 5M. The 22MCLK-P signal is divided by 2 by an inverter-pipeline arrangement on Sheet 21 and re-emerges on Sheet 15 as the 11 MHz CLKHI-P signal. CLKHI-P is routed to the D input of the synchronizing Flip Flop 9E-6 generating the 11 MHz MCLKHI-N and CLK-N from 2C-16 and 2C-14 respectively.

The binary counter 5L is clocked by CLKHI-P. Each time 5L reaches its maximum count, the carry out pin 5L-15 goes high enabling Nand gate 2M-8. The CLKHI-P signal also clocks the Refresh Request Counter. Normally, the carry output of counter 6M is logically low (no carry being generated) driving Inverter 4M-10 high and enabling And gate 2M-8. Each carry out from counter 5L drives 2M-8 high enabling the Refresh Request Counter 6M. The Refresh Request Counter is allowed to increment once each time counter 5L overflows (as long as 6M is not overflowing).

REEF-N (Refresh) is generated when a refresh operation goes into effect and causes 6M to be synchronously loaded to $5. The CLKHI-P signal divided by the inclusive division ratios of the counters (5L and 6M) generates a REF REQ-P (Refresh Request) approximately every 14 uSec. However, if a memory operation is in progress the refresh operation is delayed until the memory cycle is complete. If a refresh request is granted precisely before a dynamic memory cycle is about to start, the memory cycle is delayed and the refresh request is granted.

SHEET 16

4.20 HIGH TO HIGH BUFFER

The tri-state buffer at 7A enables the 8 bit high byte of the data output bus from the two high byte 2901B devices onto the high byte data input bus of the same 2901B devices. DBH2H-N (Data Bus High to High) is generated from the bus control decoder on Sheet 15.

$$\text{DBH2H-N} = F=\emptyset \cdot SF=\emptyset\emptyset,\emptyset 2 + F=C \cdot \overline{\text{TDATA-N}}$$

4.21 REFRESH ACKNOWLEDGE LOGIC

The Refresh Acknowledge Flip Flop is shown at 3K-8. REF REQ-P (Refresh Request) from the Refresh Request Counter (Sheet 15) is enabled through Nand gate 3L-3 if no dynamic memory operation is in progress (DMOP-N logically high) and if MEM SIG-N (4M-4) is inactive (logically high). Clocked by the free-running CLKHI-N, Flip Flop 3K-8 will be clocked set and generate an active low REEF-N when a REF REQ-P is enabled through Nand gate 3K-8. This will enable Nor gate 13K-4 to continue to generate REFRESH-N from the start of REF REQ-P until the Refresh Flip Flop is reset. If DMOP-N is generated and disables Nand gate 3L-3 before a REF REQ-P enters, the dynamic memory operation will go into effect and the refresh request will not be granted until after the memory operation. DMOP-N drives And gate 2M-6 low generating DMCY-N (Dynamic Memory Cycle) which is routed to the memory. A low from 2M-11 drives 3L-6 high and enables the Mem Check Counter.

SHEET 16 CONTINUED

The Mem Check Counter 3M is incremented by CLKHI-N until MSTAT-N (Memory Status), a handshaking signal from memory, is received. MSTAT-N when active low tells the CPU to output Write Data or that Read Data is valid. MSTAT-N is double inverted before sending an active low to the synchronous load input of counter 3M. The next positive-going transition of CLKHI-N loads all highs into counter 3M, causing the ripple carry 3M-15 to go high. This generates MEM SIG-N from 4M-4 which sends the Refresh Flip Flop 3K-8 back to its inactive state (reset).

When the system configures itself, it attempts to write, then read all possible memory locations to determine how much memory is actually present in the machine. When a location cannot be read because the memory paddle-board is not physically present at that location, MSTAT-N is not received from memory. In this situation, the Mem Check counter would continue to increment after being enabled by DMOP-N until a ripple carry is generated from 3M-15. This prevents the system from hanging up on memory that is not installed and permits standard CPU evaluation of the amount of memory present.

SHEET 17

4.22 MICROWORD BUFFERS

The Octal Transceivers 13C, 12C, and 13E place the 24 bits of data present at the outputs of the microprogram ROMs onto the PAN MWBØ-P through PAN MWB23-P bus (Test Panel Microword Bus) whenever ENA WRD-N is active low. ENA WRD-N is low during SØ (State Ø) when the address on the ZADDR bus is less than $1000 (indicating the microprogram ROMs are being accessed). When ENA WRD-N is logically high (inactive) the transceivers permit the test panel to jam a 24 bit microword onto the MWBØ-P through MWB23-P bus for testing purposes.

SHEET 18

4.23 REFRESH ADDRESS COUNTER

The 8 bit Memory Refresh address is generated by the cascaded synchronous Counters 5H and 4H. The counters are incremented by the positive-going transition of each REF REQ-P (refresh request). When a refresh operation takes place, REEF-N goes active low enabling Tri State Buffer 3H. This enables 7 of the 8 refresh address bits onto the backplane address bus. The eighth refresh address bit is generated from SMP CLK-P and is buffered on Sheet 19 before enabled onto ADDR15/7-P. RF-N is the refresh signal sent to the memory board.

4.24 MEMORY ADDRESS OFFSET ADDERS

The Schottky Full Adders at 2F, 3F, and 1F are 3 of the 5 full adders used to perform the arithmetic addition of the contents of the memory address register's least significant 11 bits and the 20 bit contents of the selected location in the Base Register RAMs. 5K is a Lookahead Carry Generator for the Adders.

SHEET 18 CONTINUED

4.25 ADDRESS MULTIPLEXING LOGIC

The 16 bit memory address required by the 64K by 1 RAMs on the memory board is multiplexed over 2 time states via an 8 bit bus (ADDR8/Ø-P through ADDR15/7-P). The Flip Flop at 3K-6 controls the address multiplexing, Flop 3K-6 is held directly reset by the inactive DMOP-P before the memory access instruction begins. DMOP-P goes active high removing the direct reset from 3K-6 and enabling Nand gate 3J-6. This drives 3J-6 logically low and enables Tri-State Buffer 2H. This enables the high 8 bits of the multiplexed address onto the backplane. DMOP-P remains active high and is pipelined 2 more times by the sequence logic to appear as DMOP2-N. The positive-going trailing edge of DMOP2-N clocks 3K-6 set. This enables Tri-State Buffer 1H and places the low 8 bits of the multiplexed address onto the ADDR8/Ø-P through ADDR15/7-P bus.

SHEET 19

4.26 BASE REGISTER ADDRESS AND DATA BUFFERS

On any read or write operation to the high or low segment of a base register, the address to the base register RAMs comes via DBO12-P through DBO15-P from the specified register file location. This occurs when FLG CTL1-P and RA3-P drive Nand gate 9J-8 low enabling DBO12-P through DBO15-P onto the MAR11-P through MAR14-P bus. Nand gate 9J-8 goes active low generating BASE-P from 2L-12 according to the following equation:

$$\text{BASE-P} = \text{F=Ø} \cdot \text{SF=18,1A,1C,1E} \cdot \overline{\text{INHSTS-N}}$$

SHEET 19 CONTINUED

BASE-P is the tri-state disable signal to the high byte of the memory address register on Sheet 5.

BASEHI-N from the bus control decoder (Sheet 15) enables the high 12 bits of the specified base register's contents (BR8-P through BR19-P) onto the DBIØ-P through DBI11-P inputs of the 3 least significant 2901B devices. BASEHI-N enables Tri-State Buffers 6E and 7C-3,5,7,9 on Sheet 19 on all Read Base High instructions (F=Ø SF=1E).

BASELO-N from the bus control decoder (Sheet 15) enables the low 8 bits of the specified base register's contents (BRØ-P through BR7-P) onto DBIØ-P through DBI7-P, the inputs to the 2 least significant 2901B devices. This occurs when BASELO-N enables Tri State Buffer 6C on all Read Base Low instructions (F=Ø SF=1C).

4.27 ADDRESS STEERING LOGIC

The least significant 16 bits of the 20 bit resultant formed by the addition of the memory address register's contents and the selected base registers contents are multiplexed onto the least significant 8 bits of the backplane address bus. The next 4 more significant bits from the offset adders SUM16-P through SUM19-P are buffered by the Tri State Buffer 4E. When a refresh operation takes place, REEF-N enables SMP CLK-P through 4E generating the most significant refresh address bit onto backplane address line ADDR15/7-P.

SHEET 20

4.28 BASE REGISTERS AND OFFSET ADDERS

The sixteen, 20 bit wide, base registers are fashioned from the five 16 by 4 Schottky RAMs at 7B, 8B, 8A, 9B, and 9A. They are addressed by MAR11-P through MAR14-P which originates from the memory address register except on Read or Write Base Register operations when the base register address must be specified in the selected register file location and is then enabled onto the MAR11-P through MAR14-P bus.

CLK BHI-N is generated during Write Base High instructions from the Sequence logic (Sheet 21) and serves as the write enable signal to the 3 most significant RAMs 7B, 8B, and 8A. Likewise, CLK BLO-N is generated during Write Base Low instructions and serves as the write enable signal to the 2 least significant RAMs 9B and 9A. During a Write Base High operation RAMs 7B, 8B, and 8A are loaded from the register file location specified in the microinstruction via the DBOØ-P through DBO11-P lines. On a Write Base Low operation, RAMs 9B and 9A are loaded from the register file location specified in the microinstruction via the DBOØ-P through DBO7-P lines.

The 2 most significant of the 5 offset adders are shown at 3E and 5E. Their primary function is to propagate any carry signals generated by the 3 least significant adders. Remember, the offset adders sum the 20 bit contents of the base register location (specified by bits 12 through 15 of the memory address register) with the 11 least significant bits of address in the memory address register. GADD3-N, PADD3-N, GADD4-N and PADD4-N are the carry generate and propagate signals routed to the carry lookahead generator on Sheet 18.

SHEET 21

4.29 TIMING 1 FPLA

Octal Flip Flop 10K is a pipeline register, clocked by the free-running 22MHz signal 22MCLK-P. The 11MHz signal CLKHI-P is generated by feeding back the output of 10K-2 through Inverter 11M-4, causing CLKHI-P to change state on every positive-going transition of 22MCLK-P. BCLKHI-P is generated from 10M-6 and is a 11MHz free-running clock used in creating the clock signal for the Base Register RAMs. BCLKHI-P is also used to create CLKHI-N from 10K-15, the complement of CLKHI-P.

XSCENA-P from the FØ output of the TMG1 FPLA at 8K is pipeline delayed one processor state on Sheet 22, only to return to Sheet 21 as SCENA-P where it is enabled through And gate 10M-11 during the logically high portion of CLKHI-N. The output of 10M-11 is clocked into pipeline register 10K on the next positive-going transition of 22MCLK-P generating CENA-P the clock signal used by the C Register.

SECLK-P from the TMG1 FPLA is pulsed through And gate 10M-3 by the logically high portion of BCLKHI-P. It is then synchronized through pipeline register 10K to generated ECLK-P the E Register clock. Likewise, SZLOD-N (from the TMG2 FPLA, Sheet 22) is conditioned and synchronized to generate ZLOD-P the Z Register clock from pipeline register 10K.

SDMOP-N from the F1 output of the TMG1 FPLA at 8K is clocked into pipeline register 9K by the positive-going edge of CLKHI-N generating DMOP-N. DMOP-N, as well as being routed to the TMG2 FPLA on Sheet 22, is inverted and returns to Sheet 21 where it is enabled through Nand gate 10L-3 by the logically high portion of BCLKHI-P. The output of 10L-3 is clocked into pipeline

register 10K by the next positive-going edge of 22MCLK-P generating DMOP2-N. DMOP2-N is used to toggle the memory address multiplexing logic on Sheet 18.

From the BUS CTL FPLA, SCLKBHI-P is generated on a Write Base High instruction and SCLKBLO-P on a Write Base Low instruction. If HALTIF-N (from the test panel) is inactive (high) and the F7 output of the TMG1 FPLA (SFETCH-P) is high, SCLKBHI-P or SCLKBLO-P can enable the 11MHz BCLKHI-P through 5J-8 or 5J-6 respectively. The base register write enable clocks are synchronized with 22MCLK-P at pipeline register 10K before being routed to the Base Register RAMs as CLKBHI-N and CLKBLO-N.

The TMG1 FPLA generates 3 binary coded time-state signals; STØ-P, ST1-P, and ST2-P from its F4, F5, and F6 outputs. These signals are clocked into pipeline register 9K by the positive-going transition of CLKHI-N generating TØ-P, T1-P, and T2-P. These time-state signals are routed back to the inputs of both the TMG1 and TMG2 FPLA as well as to the Unconditional Branch Decoder on Sheet 7. The TMG1 FPLA provides the intelligence to specify the time-state sequencing for any particular instruction type. Nand gate 9J-6 is a State 7 decoder. State 7 is only entered if the test panel is attached. Notice, HALTIF-N must be active low for Nand gate 9J-6 to be enabled and generate S7-N.

A conditional load (CON LOD-N) or Fetch operation (a logical low from Inverter 7L-2) will drive 9L-3 low and cause pipeline register 9K to send the FETCH signal to the test panel on the next positive-going transition of the CLKHI-N clock.

SHEET 21 CONTINUED

STDATA-N and STLOD-N from Sheet 22 are also pipelined through 9K. Notice that the output XTDATA2-N is routed back to one of the inputs of the TMG1 FPLA. RSTZ-P (Reset Z) is generated at power-up or by IPL. A logically high RSTZ-P will disable the tri-state outputs of 9K.

SHEET 22

4.30 TIMING 2 FPLA

The TMG2 FPLA generates the remaining load, clock enable, and increment signals for the Q30. There is a slight variation in the input terms sent to the TMG2 FPLA, RA=RB-P and T-P are routed to the TMG2 FPLA while REFRESH-N is input only to the TMG1 FPLA. STLOD-N and SZLOD-N from 6K are routed to the pipeline register on Sheet 21. The F7 output of the TMG2 FPLA (INCZ-N) is inverted by 7L-4 and routed to Sheet 7 as INCZ-P where it enables incrementation of the Z Counter. The INCZ mini-jumper at 6K permits the repair technician to disable the Z Counter.

The TMG2 FPLA generates the clock for the 2901B devices (SACLK-N from the F2 output of 6K). This signal is routed to the Negative-Nor gates 9L-6 and 9L-8. AHI-N and ALO-N are the clock inhibit signals from the BUS CTL FPLA (Sheet 13). A logically low AHI-N or ALO-N will disable 9L-8 or 9L-6 respectively. The outputs of 9L-6 and 9L-8 are clocked into pipeline register 8L by the positive-going edge of CLKHI-N. ACLKHI-P is routed to the two high byte 2901B devices, while, ACLKLO-P is routed to the two low byte 2901B devices.

SHEET 22 CONTINUED

MARENA-P (Memory Address Enable) is the clock signal for the Memory Address Register (Sheet 5). MARENA-P is generated from 8L using the XSCENA-P term from the TMG1 FPLA and is identical to SCENA-P.

STB-P (Strobe) from pipeline register 8L is set up one state earlier from the F3 output of 6K as the signal SSTB-P.

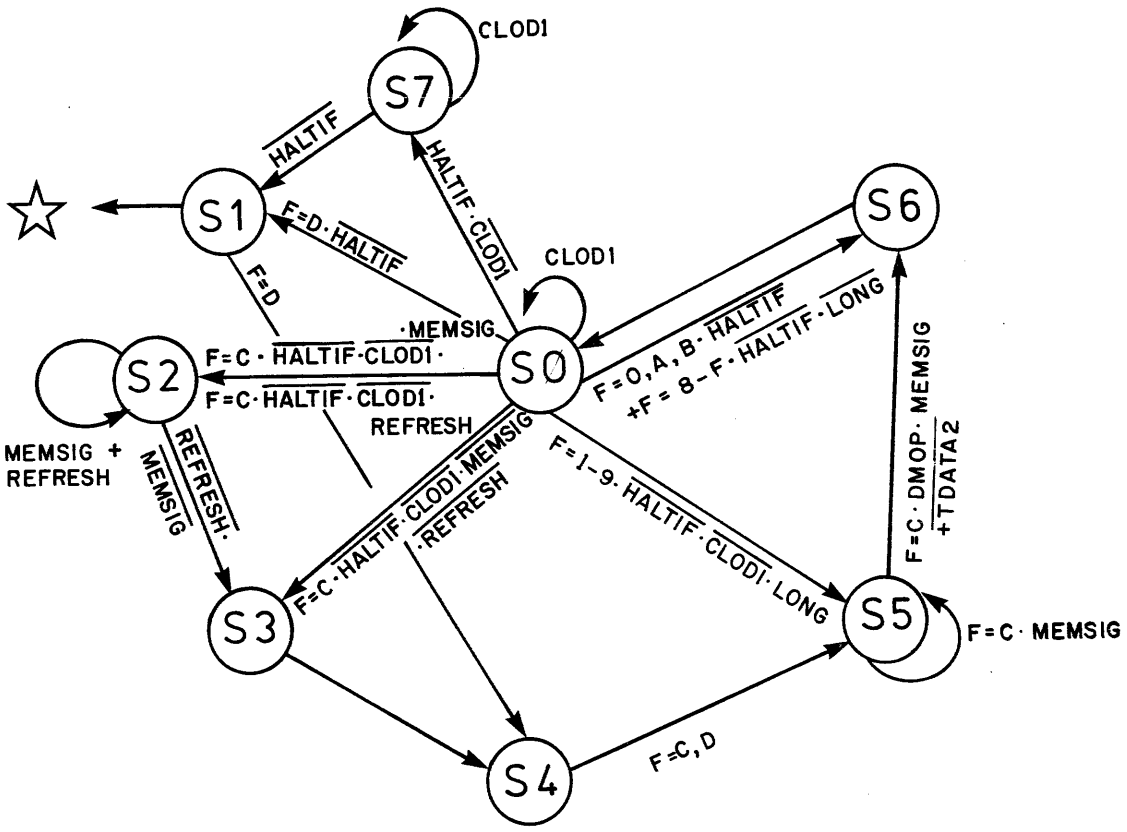
$$\text{SSTB-P} = \text{F=D}\cdot\text{S4} + \text{F=D}\cdot\text{S1}$$

The conditional Load signal CON LOD-P from the condition code multiplexer (Sheet 7) is pipelined through 8L where CLODI-P and CLODI-N are generated. CON LOD-P is buffered by 13B-9 and sent to the test panel as BCON LOD-P.

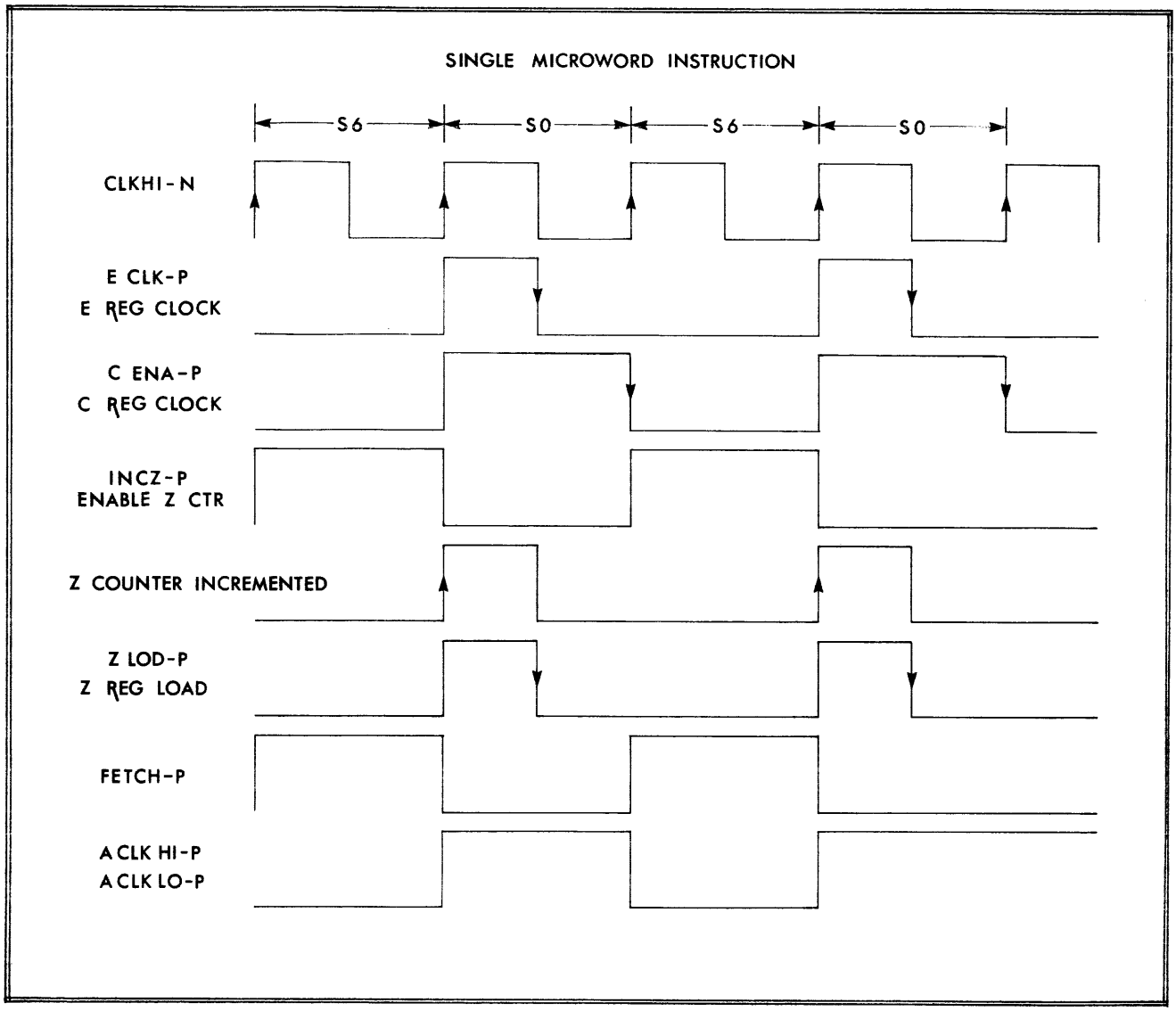
ENA WRD-N a select-enable signal sent to the microprogram ROMs is generated from 6L-8 if the ZADDR12-N bit is inactive (high). This indicates a Z address of less than or equal to ØFFF, which is the microprogram ROM address space.

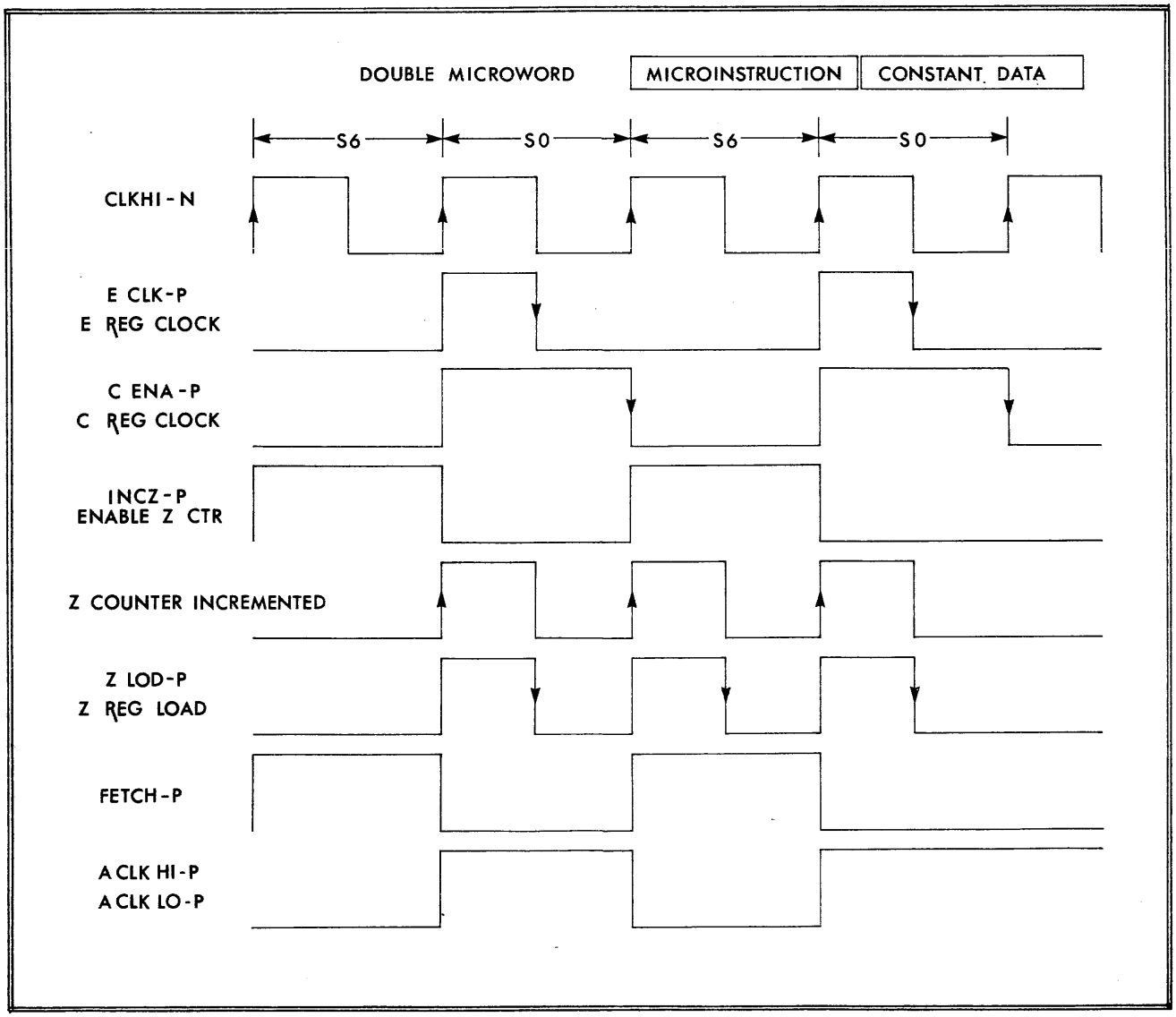
On a dynamic memory operation DMOP-N is generated by the TMG1 FPLA pipeline. DMOP-N is inverted by 6L-3, generating DMOP-P which enables the R/W-P (Read/Write bit from the E Register) through And gate 6L-6 (unless the test panel disables Negative-Nand gate 13K-1 with an active high HALTIF-P). A logically low R/W-P bit will generate DMWR-N (Dynamic Memory Write) from 6L-6.

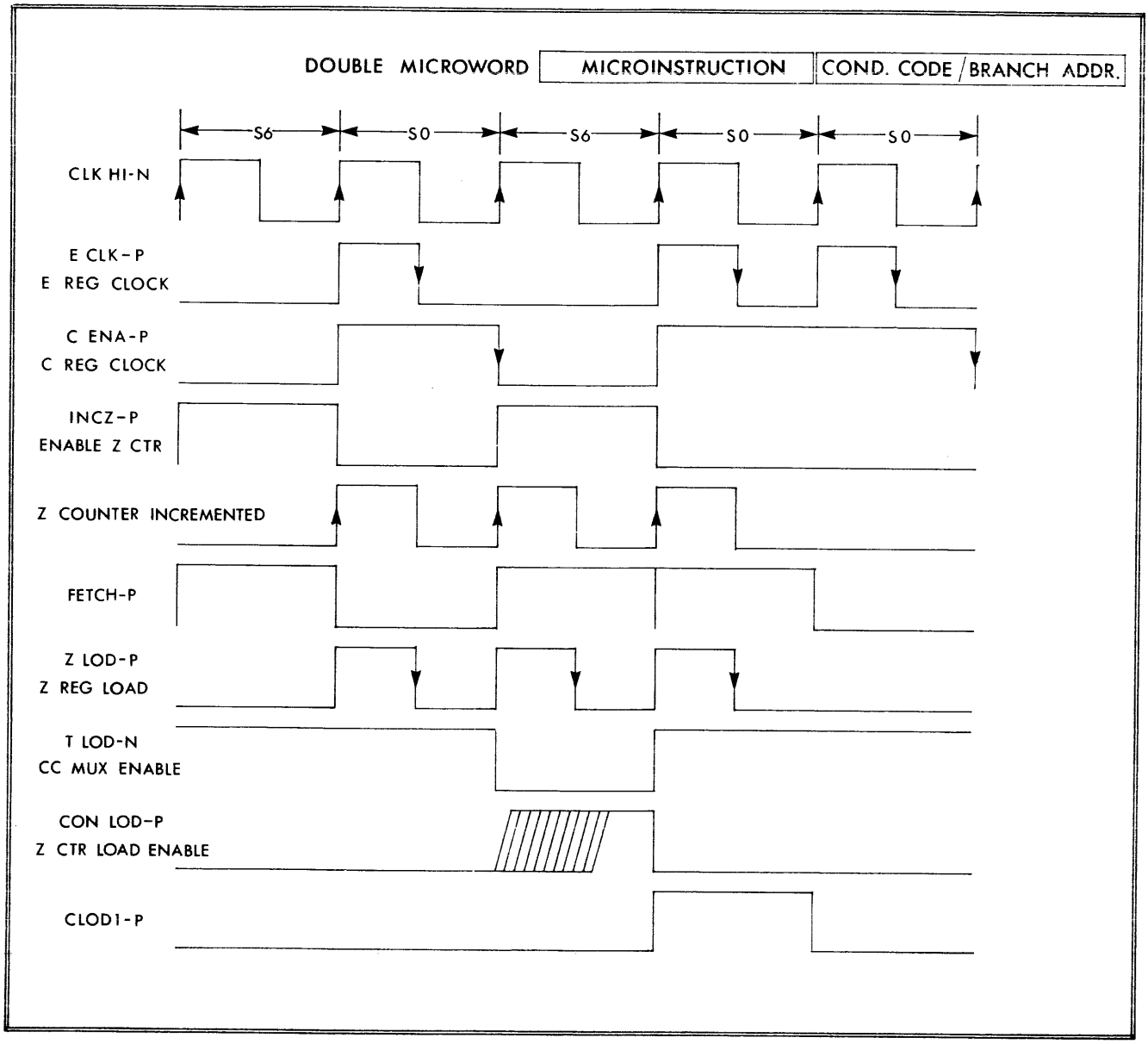
5.0 TIMING DIAGRAMS AND STATE FLOW DIAGRAM

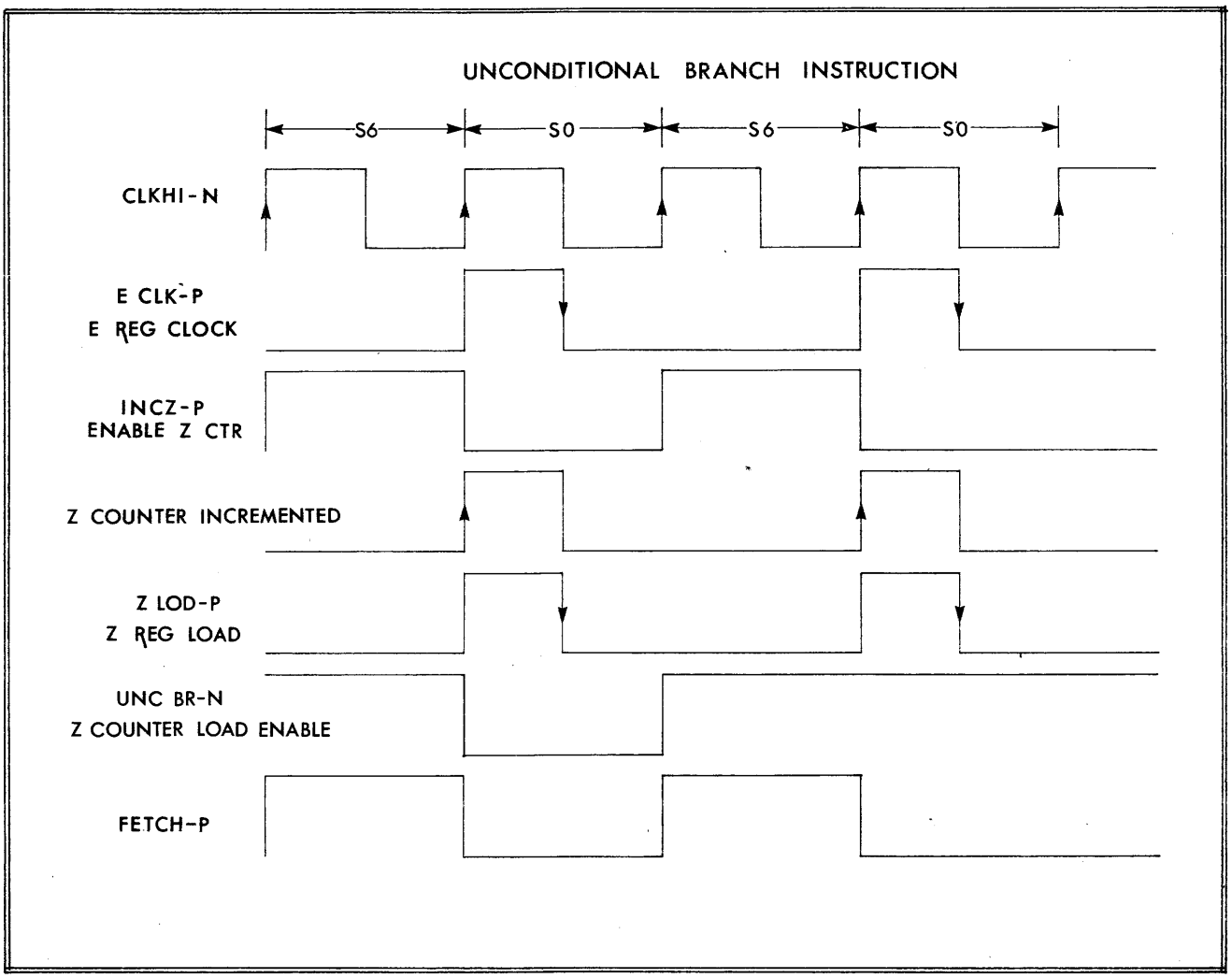


☆ WHEN EXITING STATE 1, ANY OF THE EXIT PATHS FROM STATE Ø MAY BE TAKEN EXCEPT THE RETURN TO STATE 1 (CONDITION F=D·$\overline{\text{HALTIF}}$) OR THE LOOP ON STATE Ø (IF CLOD1 IS ACTIVE).

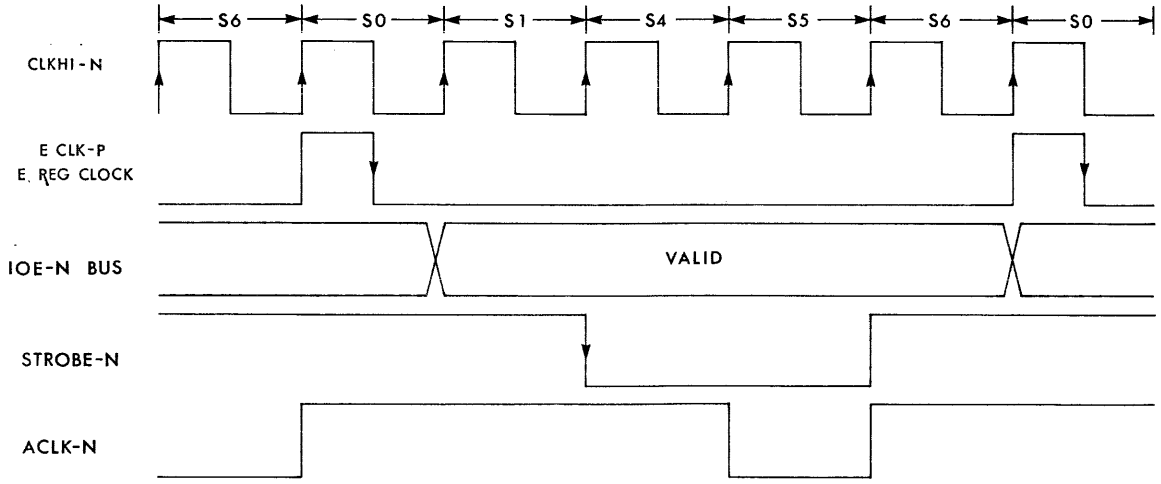

SINGLE MICROWORD INSTRUCTION
S6
S0
S6
S0
CLKHI-N
E CLK-P
E REG CLOCK
C ENA-P
C REG CLOCK
INCZ-P
ENABLE Z CTR
Z COUNTER INCREMENTED
Z LOD-P
Z REG LOAD
FETCH-P
A CLK HI-P
A CLK LO-P


DOUBLE MICROWORD
MICROINSTRUCTION
CONSTANT DATA
S6
S0
S6
S0
CLKHI-N
E CLK-P
E REG CLOCK
C ENA-P
C REG CLOCK
INCZ-P
ENABLE Z CTR
Z COUNTER INCREMENTED
Z LOD-P
Z REG LOAD
FETCH-P
A CLK HI-P
A CLK LO-P

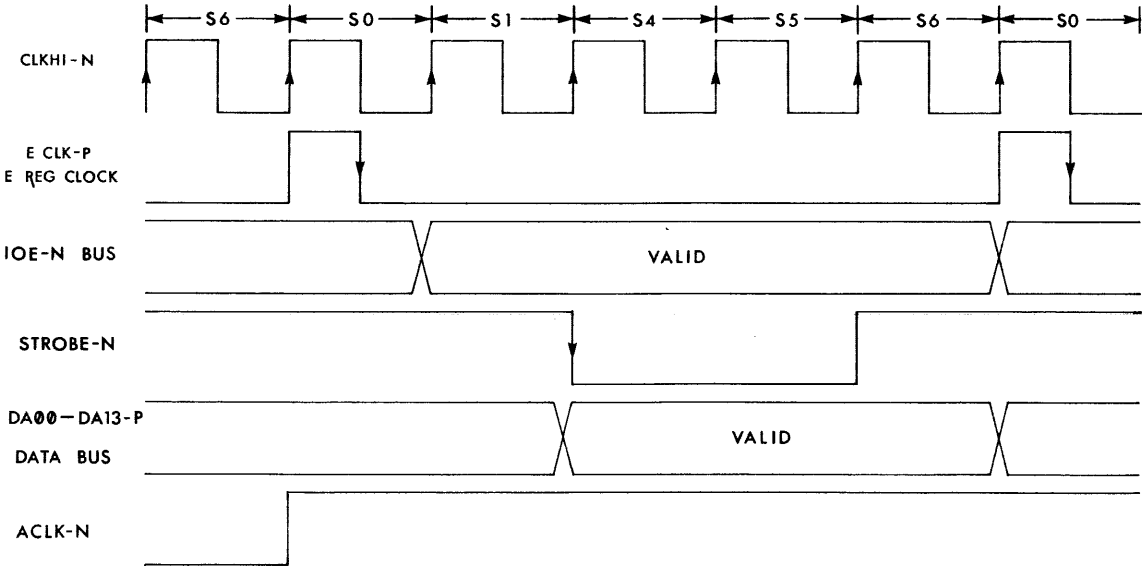

DOUBLE MICROWORD
MICROINSTRUCTION
COND. CODE / BRANCH ADDR.
S6
S0
S6
S0
S0
CLK HI-N
E CLK-P
E REG CLOCK
C ENA-P
C REG CLOCK
INCZ-P
ENABLE Z CTR
Z COUNTER INCREMENTED
FETCH-P
Z LOD-P
Z REG LOAD
T LOD-N
CC MUX ENABLE
CON LOD-P
Z CTR LOAD ENABLE
CLOD1-P

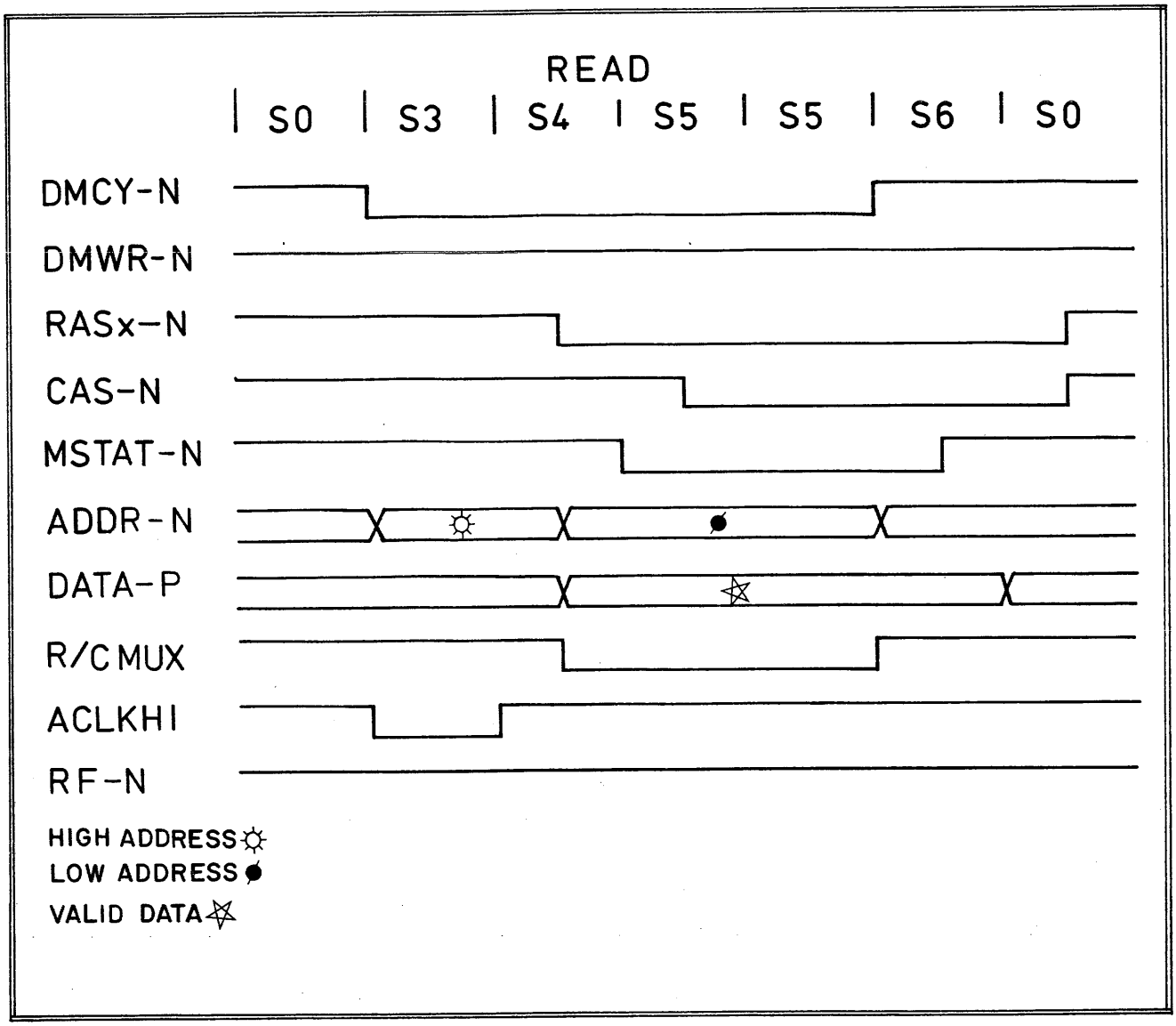

UNCONDITIONAL BRANCH INSTRUCTION
S6
S0
S6
S0
CLKHI-N
E CLK-P
E REG CLOCK
INCZ-P
ENABLE Z CTR
Z COUNTER INCREMENTED
Z LOD-P
Z REG LOAD
UNC BR-N
Z COUNTER LOAD ENABLE
FETCH-P

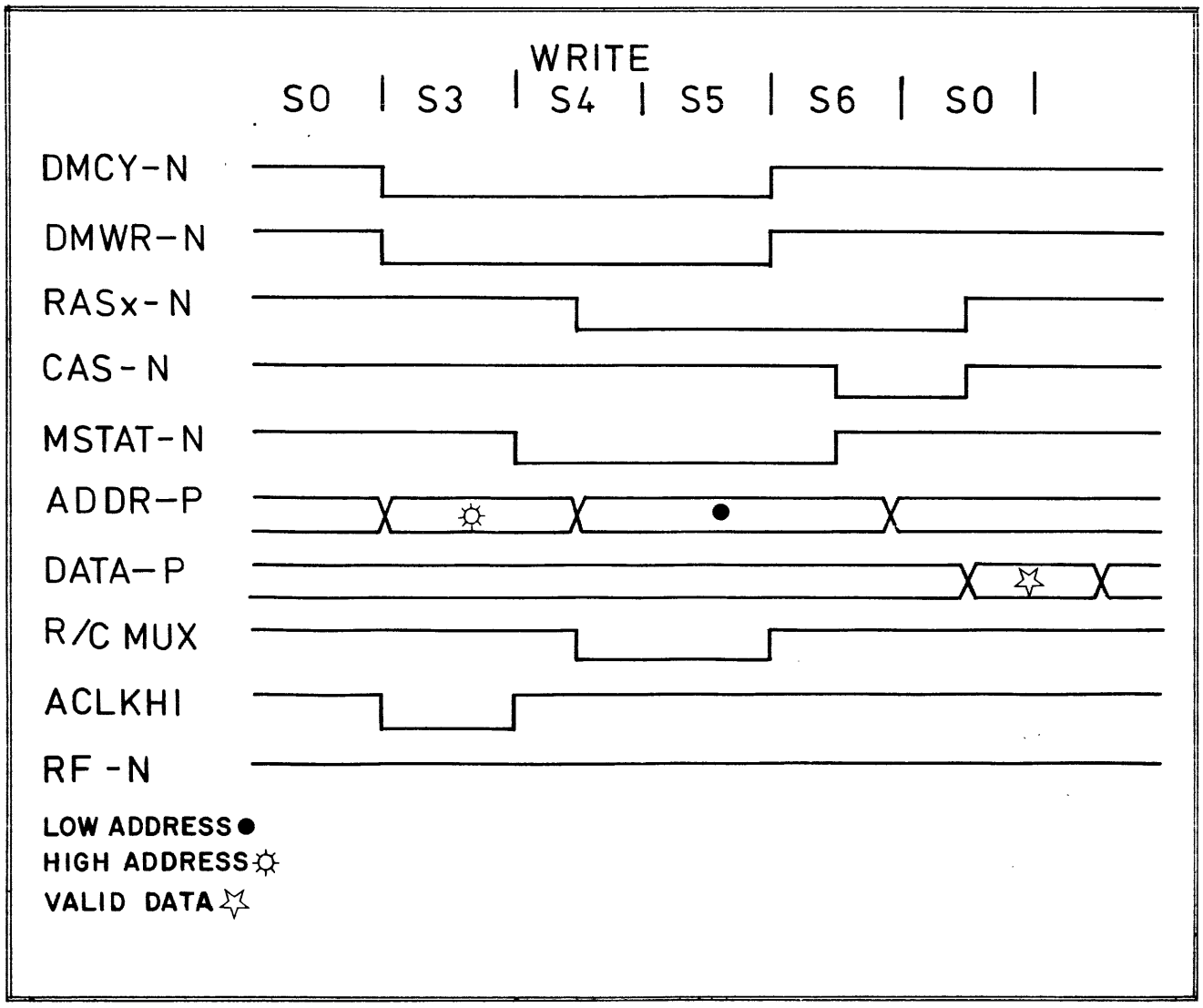
I/O READ

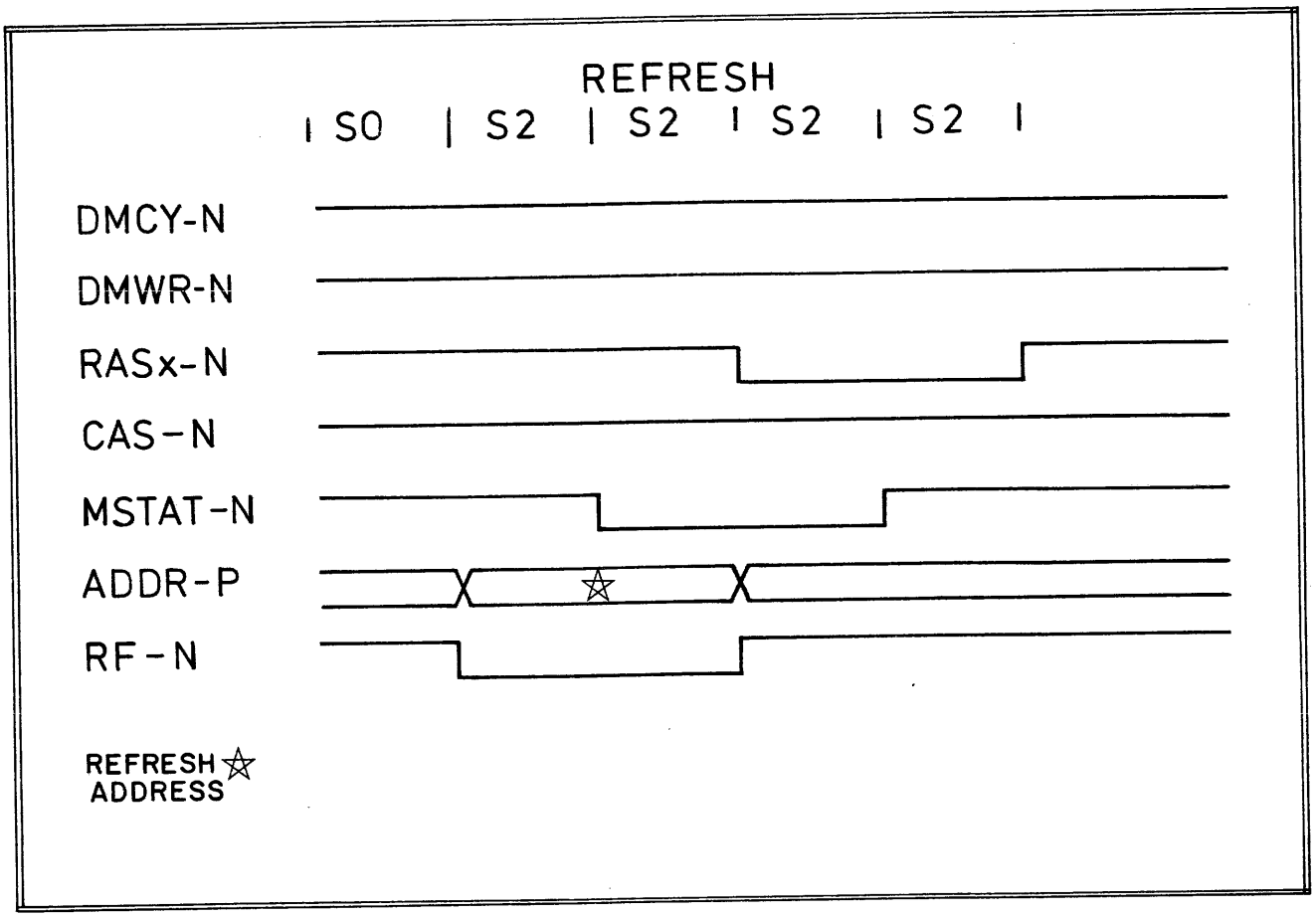


I/O WRITE




READ
S0
S3
S4
S5
S5
S6
S0
DMCY-N
DMWR-N
RASx-N
CAS-N
MSTAT-N
ADDR-N
DATA-P
R/C MUX
ACLKHI
RF-N
HIGH ADDRESS
LOW ADDRESS
VALID DATA


WRITE
S0
S3
S4
S5
S6
S0
DMCY-N
DMWR-N
RASx-N
CAS-N
MSTAT-N
ADDR-P
DATA-P
R/C MUX
ACLKHI
RF -N
LOW ADDRESS ●
HIGH ADDRESS ☼
VALID DATA ☆


REFRESH
S0
S2
S2
S2
S2
DMCY-N
DMWR-N
RASx-N
CAS-N
MSTAT-N
ADDR-P
RF-N
REFRESH ADDRESS

APPENDIX A

FPLA EXTENSION BITS

Fpø-Fp7-P are the FPLA Extension bits. In the Q29 CPU these bits were generated by FPLAs. The bits are now immediately present in the Q30 extended microword.

Bit	Name	Logic Equation
Fp7	RA=RB	Ra=Rb
Fp6	LONG	F=1•Ra=Rb +F=2-9•Ra=Rb•T-P +$\overline{\text{RA3-P}}$•RB3-P•RB4-P +RB3-P•$\overline{\text{RA4-P}}$•RB4-P +RA3-P•$\overline{\text{RB3-P}}$•RA4-P +RA3-P•RA4-P•$\overline{\text{RB4-P}}$
Fp5	RA2RAL	F=ø +F=ø-B•RA3-P•RA4-P +F=C +F=D
Fp4	RA2RAH	F=ø +F=ø-B•$\overline{\text{RA3-P}}$•RB3-P•RB4-P +F=ø-B•RB3-P•$\overline{\text{RA4-P}}$•RB4-P +F=C +F=D
Fp3	A3	$\overline{\text{RA3-P}}$•$\overline{\text{RA4-P}}$ +F=C•$\overline{\text{RA3-P}}$
Fp2	D2Z	F=2-9•Ra=Rb•$\overline{\text{R/W-P}}$•T-P
Fp1	Not Used	
Fpø	Not Used	

TIMING 1 FPLA

```
SFETCH-P  = F=Ø,A,B·HALTIF-N·SØ,S1
          +F=Ø-B·HALTIF-N·SØ,S1·LONG-P
          +F=C·S5·DMOP-N·MEMSIG-N·TDATA2-N
          +S5·TDATA2-N

ST2-P     = SØ·CLOD1-P
          +S6
          +S1·MEMSIG-N·REFRESH-N
          +F=C·HALTIF-N·SØ,S1·CLOD1-P·MEMSIG-N·REFRESH-N
          +S7·HALTIF-N
          +F=D·HALTIF-N·SØ·CLOD1-P
          +F=C·HALTIF-N·SØ,S1·CLOD1-P·MEMSIG-N
          +F=C·HALTIF-N·SØ,S1·CLOD1-P·REFRESH-N
          +S1·MEMSIG-N
          +S1·REFRESH-N

ST1-P     = SØ·CLOD1-P
          +S6
          +S3
          +F=1-9·HALTIF-N·SØ,S1·CLOD1-P·LONG-P
          +F=C·S5·MEMSIG-N
          +HALTIF-N·S7
          +F=C·S4
          +F=D·HALTIF-N·SØ·ClOD1-P
          +F=D·S1,S4

STØ-P     = S2·MEMSIG-N·REFRESH-N
          +F=1-9·HALTIF-N·SØ,S1·CLOD1-P·LONG-P
          +F=C·S5·MEMSIG-N
          +HALTIF-N·SØ·CLOD1-P
          +S7
```

TIMING 1 FPLA CONTINUED

$$
\begin{aligned}
\text{STØ-P} &= F{=}C \cdot \overline{\text{HALTIF-N}} \cdot S\text{Ø}, S1 \cdot \overline{\text{CLOD1-P}} \cdot \overline{\text{MEMSIG-N}} \cdot \overline{\text{REFRESH-N}} \\
\text{(continued)} \quad &+ S7 \cdot \overline{\text{HALTIF-N}} \\
&+ F{=}C \cdot S4 \\
&+ F{=}D \cdot \overline{\text{HALTIF-N}} \cdot S\text{Ø} \cdot \overline{\text{CLOD1-P}} \\
&+ F{=}D \cdot S4
\end{aligned}
$$

$$
\begin{aligned}
\text{SECLK-P} &= S\text{Ø} \cdot \text{CLOD1-P} \\
&+ S6 \\
&+ S7
\end{aligned}
$$

$$
\begin{aligned}
\text{STDATA2-N} &= S2 \cdot \overline{\text{MEMSIG-N}} \cdot \overline{\text{REFRESH-N}} \\
&+ S3 \\
&+ F{=}C \cdot S5 \cdot \overline{\text{MEMSIG-N}} \\
&+ F{=}C \cdot \overline{\text{HALTIF-N}} \cdot S\text{Ø}, S1 \cdot \overline{\text{CLOD1-P}} \cdot \overline{\text{MEMSIG-N}} \cdot \overline{\text{REFRESH-N}} \\
&+ F{=}C \cdot S4
\end{aligned}
$$

$$
\begin{aligned}
\text{SDMOP-P} &= S2 \cdot \overline{\text{MEMSIG-N}} \cdot \overline{\text{REFRESH-N}} \\
&+ S3 \\
&+ F{=}C \cdot S5 \cdot \overline{\text{MEMSIG-N}} \\
&+ F{=}C \cdot \overline{\text{HALTIF-N}} \cdot S\text{Ø}, S1 \cdot \overline{\text{CLOD1-P}} \cdot \overline{\text{MEMSIG-N}} \cdot \overline{\text{REFRESH-N}} \\
&+ F{=}C \cdot S4
\end{aligned}
$$

$$
\begin{aligned}
\text{SCENA-P} &= S\text{Ø} \cdot \text{CLOD1-P} \\
&+ S6 \\
&+ S7
\end{aligned}
$$

TIMING 2 FPLA

```
INCZ-N  = F=1-9·HALTIF-N·SØ·Ra=Rb
        +F=Ø-9·HALTIF-N·SØ·T-P
        +F=2-9·S5·R/W-P·Ra=Rb·T-P
        +F=1·S5·Ra=Rb
        +S6
        +F=D·HALTIF-N·SØ·T-P·CLOD-P
        +F=C,E·HALTIF-N·SØ·R/W-P·T-P
        +SØ·CLOD-P

STLOD-N = F=2-9·S5·Ra≠Rb·T-P
        +F=2-9·S5·R/W-P·T-P
        +F=2-9·HALTIF-N·SØ,S1·CLOD1-P·LONG-P·Ra≠Rb
              ·T-P
        +F=4-9·HALTIF-N·SØ,S1·CLOD1-P·LONG-P·R/W-P
              ·T-P
        +F=1·HALTIF-N·SØ,S1·CLOD1-P·LONG-P·T-P
        +F=1·HALTIF-N·SØ,S1·CLOD1-P·LONG-P·Ra=Rb
        +F=Ø·HALTIF-N·SØ,S1·CLOD1-P·T-P
        +F=C·S5·DMOP-N·MEMSIG-N·R/W-P·T-P
        +F=D·S5·T-P
        +F=1·S5·T-P
        +F=1·S5·Ra=Rb
        +F=2,3,6,7·HALTIF-N·SØ,S1·CLOD1-P·LONG-P
                  ·R/W-P·T-P
```

TIMING 2 FPLA CONTINUED

```
SZLOD-N = F=1·HALTIF-N·SØ,S1·Ra=Rb
         +F=2-9·S5·R/W-P·Ra=Rb·T-P
         +F=Ø-9·HALTIF-N·SØ,S1·T-P
         +F=1·S5·Ra=Rb
         +S6
         +S7
         +F=D·HALTIF-N·S1·T-P
         +F=C,E·HALTIF-N·SØ,S1·R/W-P·T-P
         +SØ·CLOD1-P

 SSTB-P = F=D·S4
         +F=D·S1

SACLK-N = S7
         +S6
         +F=D·S5
         +F=C·HALTIF-N·S4·R/W-P
         +SØ·CLOD1-P
         +F=D·HALTIF-N·SØ
         +S2,S3
         +HALTIF-N·SØ
```

INSTRUCTION 1 FPLA

$$\overline{I8H\text{-}P} = F=\emptyset \cdot RA3\text{-}P \cdot RB\text{-}P \cdot \overline{RA4\text{-}P}$$
$$+F=\emptyset \cdot RA3\text{-}P \cdot \overline{RA4\text{-}P} \cdot \overline{RB4\text{-}P}$$

$$\overline{I7HH\text{-}P} = F=2\text{-}9 \cdot Ra=Rb \cdot \overline{R/W\text{-}P} \cdot T\text{-}P$$
$$+F=\emptyset \cdot SF=\emptyset 8,\emptyset C$$

$$\overline{I7L\text{-}P} = F=\emptyset \cdot SF=18,1A$$
$$+F=2\text{-}9 \cdot Ra=Rb \cdot \overline{R/W\text{-}P} \cdot T\text{-}P$$
$$+F=\emptyset \cdot SF=\emptyset 8,\emptyset C$$

$$I5\text{-}P = F=\emptyset \cdot SF=\emptyset 1,18,1A$$
$$+F=1 \cdot \overline{R/W\text{-}P}$$
$$+F=6,8,9$$

$$\overline{I4H\text{-}P} = F=\emptyset \cdot SF=\emptyset 1,1\emptyset,12$$
$$+F=1 \cdot \overline{R/W\text{-}P}$$
$$+F=1,3,5 \cdot \overline{T\text{-}P}$$
$$+F=1,3,5 \cdot Ra \neq Rb$$
$$+F=2,4,8$$
$$+F=3,5 \cdot R/W\text{-}P$$
$$+F=9 \cdot \overline{RA3\text{-}P} \cdot Ra=Rb \cdot \overline{R/W\text{-}P} \cdot RA4\text{-}P \cdot T\text{-}P$$
$$+F=9 \cdot RA4\text{-}P \cdot \overline{RB4\text{-}P}$$
$$+F=C \cdot \overline{TDATA2\text{-}N} \cdot RA4\text{-}P \cdot \overline{RB4\text{-}P}$$
$$+F=C \cdot \overline{TDATA2\text{-}N} \cdot RA4\text{-}P \cdot RB4\text{-}P$$

$$\overline{I4L\text{-}P} = F=\emptyset \cdot SF=\emptyset 1,1\emptyset,12$$
$$+F=1 \cdot \overline{R/W\text{-}P}$$
$$+F=1,3,5 \cdot \overline{T\text{-}P}$$
$$+F=1,3,5 \cdot Ra \neq Rb$$
$$+F=3 \cdot R/W\text{-}P$$
$$+F=2,4,8$$

INSTRUCTION 1 FPLA CONTINUED

$\overline{\text{I4L-P}}$ = F=9·RA3-P·Ra=Rb·R/W-P·RA4-P·T-P
(continued) +F=C·$\overline{\text{TDATA2-N}}$·RA4-P·$\overline{\text{RB4-P}}$
+F=C·$\overline{\text{TDATA2-N}}$·RA4-P·RB4-P

$\overline{\text{I3-P}}$ = F=Ø·SF=Ø1,12
+F=1·Ra=Rb·T-P
+F=1·$\overline{\text{R/W-P}}$
+F=2,4,6,8,9
+F=3,5·Ra=Rb·$\overline{\text{R/W-P}}$·T-P
+F=C·$\overline{\text{TDATA2-N}}$·$\overline{\text{HALTIF-P}}$·RA4-P·RB4-P
+F=C·$\overline{\text{TDATA2-N}}$·HALTIF-N·RA4-P·$\overline{\text{RB4-P}}$

IØHH-P = F-Ø·$\overline{\text{RA3-P}}$
+F=Ø·$\overline{\text{RA4-P}}$
+F=1-8,C,D
+F=9·$\overline{\text{RA3-P}}$·RB3-P·RB4-P
+F=9·RB3-P·$\overline{\text{RA4-P}}$·RB4-P
+F=9·Ra=Rb·R/W-P
+F=9·Ra=Rb·$\overline{\text{T-P}}$

INSTRUCTION 2 FPLA

$\overline{\text{I2H-P}}$ = F=Ø·SF=Ø8,Ø9,ØC,ØD,1Ø,12,18,1A
+F=1-8·Ra≠Rb·$\overline{\text{RB4-P}}$·$\overline{\text{RA4-P}}$
+F=1-8·Ra≠Rb·$\overline{\text{RA3-P}}$·$\overline{\text{RB4-P}}$
+F=1-8·Ra≠Rb·RA3-P·RA4-P
+F=C·$\overline{\text{TDATA2-N}}$·RA4-P

$\overline{\text{I2L-P}}$ = F=1-8·Ra≠Rb·$\overline{\text{RB3-P}}$·$\overline{\text{RA4-P}}$·RB4-P
+F=1-8·Ra≠Rb·$\overline{\text{RA3-P}}$·$\overline{\text{RB3-P}}$·RB4-P
+F=1-8·Ra≠Rb·$\overline{\text{RA3-P}}$·$\overline{\text{RB4-P}}$
+F=1-8·Ra≠Rb·$\overline{\text{RA4-P}}$·$\overline{\text{RB4-P}}$

I1H-P = F=1-8·$\overline{\text{RB3-P}}$·RA4-P
+F=1-8·RA4-P·$\overline{\text{RB4-P}}$
+F=Ø
+F=9·Ra=Rb·$\overline{\text{T-P}}$
+F=9·Ra=Rb·R/W-P
+F=9·Ra≠Rb·RB3-P·$\overline{\text{RA4-P}}$·RB4-P
+F=9·Ra≠Rb·$\overline{\text{RA3-P}}$·RB3-P·RB4-P
+F=C,D

I1L-P = F=1-8·Ra=Rb·RA3-P·$\overline{\text{R/W-P}}$·RA4-P·T-P
+F=2-7·Ra=Rb·RA3-P·R/W-P·RA4-P
+F=8·Ra=Rb·RA3-P·RA4-P
+F=Ø
+F=9·Ra≠Rb·RA3-P·$\overline{\text{RB3-P}}$·RA4-P
+F=9·Ra≠Rb·RA3-P·RA4-P·$\overline{\text{RB4-P}}$
+F=9·Ra=Rb·R/W-P
+F=9·Ra=Rb·$\overline{\text{T-P}}$
+F=C,D

INSTRUCTION 2 FPLA CONTINUED

$$
\begin{aligned}
I\emptyset HL\text{-}P = {} & F=\emptyset\text{-}8,C,D \\
& + F=9 \cdot Ra \neq Rb \cdot \overline{RA3\text{-}P} \cdot RB3\text{-}P \cdot RB4\text{-}P \\
& + F=9 \cdot Ra \neq Rb \cdot RB3\text{-}P \cdot \overline{RA4\text{-}P} \cdot RB4\text{-}P \\
& + F=9 \cdot Ra=Rb \cdot R/W\text{-}P \\
& + F=9 \cdot Ra=Rb \cdot \overline{T\text{-}P}
\end{aligned}
$$

$$
\begin{aligned}
I\emptyset L\text{-}P = {} & F=\emptyset\text{-}8,C,D \\
& + F=9 \cdot Ra \neq Rb \cdot RA3\text{-}P \cdot \overline{RB3\text{-}P} \cdot RA4\text{-}P \\
& + F=9 \cdot Ra \neq Rb \cdot RA3\text{-}P \cdot RA4\text{-}P \cdot \overline{RB4\text{-}P} \\
& + F=9 \cdot Ra=Rb \cdot R/W\text{-}P \\
& + F=9 \cdot Ra=Rb \cdot \overline{T\text{-}P}
\end{aligned}
$$

MISCELLANEOUS FPLA

CRYIN-P = F=Ø·RA4-P·$\overline{\text{RA3-P}}$·$\overline{\text{RA2-P}}$·RA1-P (SF=$12 or 13)
+F=1·R/W-P
+F=3
+F=4,5·CRY2-P
+F=C,E·HALTIF-P·RA4-P·$\overline{\text{RB4-P}}$ (M=$2)
+F=C,E·$\overline{\text{HALTIF-P}}$·RA4-P·RB4-P (M=$3)

$\overline{\text{RIPCRY-P}}$ = F=Ø-9,D·RB3-P·RB4-P

DBH2L-N = F=1-9·Ra≠Rb·$\overline{\text{RB3-P}}$
+F=1-9·Ra≠Rb·$\overline{\text{RB4-P}}$
+F=C,E·RA3-P·TDATA2-N
+F=Ø,D·RB3-P·RB4-P

DBL2L-N = F=Ø·SF=Ø,1
+F=1-9·Ra≠Rb
+F=C·$\overline{\text{TDATA2-N}}$

READ-P = F=C

I8L-P = F=Ø·RA3-P·$\overline{\text{RB3-P}}$·$\overline{\text{RA4-P}}$
+F=Ø·RA3-P·$\overline{\text{RA4-P}}$·$\overline{\text{RB4-P}}$

STATUS FPLA

```
FLG CTL1-P  = F=Ø·SF=Ø4·INHSTS-N
              +F=Ø·SF=18,1A,1C,1E·INHSTS-N
              +F=Ø·SF=Ø3·INHSTS-N

FLG CTLØ-P  = F=Ø·SF=Ø4·INHSTS-N

ENRAM7·8-P  = F=Ø·RA3-P·RAØ-P·RB3-P·INHSTS-N·RA4-P·RB4-P
              +F=Ø·RA3-P·RAØ-P·RB3-P·INHSTS-N·RA4-P·RB4-P

STS CTL1-P  = F=Ø·RA1-P·RB4-P
              +F=Ø·RA1-P·R/W-P
              +F=Ø·RA2-P·RB4-P
              +F=Ø·RA2-P·R/W-P
              +F=Ø·RA3-P·RB4-P
              +F=Ø·RA3-P·R/W-P
              +F=Ø·RA4-P·RB4-P
              +F=Ø·R/W-P·RA4-P
              +INHSTS-N
              +F=1,4-9·RB4-P
              +F=2,3,6,7·RA4-P·RB4-P
              +F=C·TDATA2-N
              +F=C·R/W-P·T-P
              +F=A,B
              +F=2-D·R/W-P

STS CTL2-P  = F=Ø·RA3-P·RA2-P·RA1-P·RAØ-P·INHSTS-N·RA4-P
              +INHSTS-N
              +F=Ø·RA3-P·RA2-P·RA1-P·RAØ-P·INHSTS-N
              +F=C·TDATA2-N
              +F=C·R/W-P·T-P
              +F=A,B
              +F=Ø,2-D·R/W-P
```

$\overline{\text{STS CTL3-P}}$ = F=Ø·SF=Ø4·$\overline{\text{INHSTS-N}}$

+F=1·$\overline{\text{RB3-P}}$·$\overline{\text{INHSTS-N}}$·R/W-P·RB4-P·$\overline{\text{T-P}}$

+F=1·Ra≠Rb·$\overline{\text{INHSTS-N}}$·R/W-P·$\overline{\text{RB3-P}}$

+F=2-5·$\overline{\text{RB3-P}}$·$\overline{\text{INHSTS-N}}$·R/W-P·RB4-P

+F=Ø·$\overline{\text{RA3-P}}$·$\overline{\text{RA2-P}}$·$\overline{\text{RAØ-P}}$·$\overline{\text{RB3-P}}$·$\overline{\text{INHSTS-N}}$·R/W-P ·RA4-P·RB4-P

+F=Ø·RA3-P·RAØ-P·RB3-P·$\overline{\text{INHSTS-N}}$·R/W-P·$\overline{\text{RA4-P}}$

+F=Ø·RA3-P·RAØ-P·$\overline{\text{INHSTS-N}}$·R/W-P·$\overline{\text{RA4-P}}$·$\overline{\text{RB4-P}}$

+F=Ø·RA3-P·$\overline{\text{RAØ-P}}$·$\overline{\text{RB3-P}}$·$\overline{\text{INHSTS-N}}$·R/W-P·$\overline{\text{RA4-P}}$ ·RB4-P

+F=Ø·$\overline{\text{RA3-P}}$·RA2-P·$\overline{\text{RA1-P}}$·RAØ-P·$\overline{\text{INHSTS-N}}$

$\overline{\text{STS CTL4-P}}$ = F=1·Ra=Rb·$\overline{\text{INHSTS-N}}$·R/W-P·T-P

+F=1·RB3-P·$\overline{\text{INHSTS-N}}$·R/W-P

+F=1·$\overline{\text{INHSTS-N}}$·R/W-P·$\overline{\text{RB4-P}}$

+F=1·$\overline{\text{RB3-P}}$·$\overline{\text{INHSTS-N}}$·R/W-P·RB4-P·$\overline{\text{T-P}}$

+F=1·$\overline{\text{RB3-P}}$·Ra≠Rb·$\overline{\text{INHSTS-N}}$·R/W-P

+F=Ø·$\overline{\text{RA3-P}}$·$\overline{\text{RA2-P}}$·$\overline{\text{RAØ-P}}$·RB3-P·$\overline{\text{INHSTS-N}}$·R/W-P ·RA4-P

+F=Ø·$\overline{\text{RA3-P}}$·$\overline{\text{RA2-P}}$·$\overline{\text{RAØ-P}}$·$\overline{\text{INHSTS-N}}$·R/W-P·RA4-P ·$\overline{\text{RB4-P}}$

+F=Ø·$\overline{\text{RA3-P}}$·$\overline{\text{RA2-P}}$·$\overline{\text{RAØ-P}}$·$\overline{\text{RB3-P}}$·$\overline{\text{INHSTS-N}}$·R/W-P ·RA4-P·RB4-P

+F=Ø·RA3-P·$\overline{\text{RAØ-P}}$·RB3-P·$\overline{\text{INHSTS-N}}$·R/W-P·$\overline{\text{RA4-P}}$ ·RB4-P

+F=Ø·RA3-P·$\overline{\text{RAØ-P}}$·RB3-P·$\overline{\text{INHSTS-N}}$·R/W-P·$\overline{\text{RA4-P}}$ ·RB4-P

+F=Ø·RA3-P·$\overline{\text{RAØ-P}}$·$\overline{\text{INHSTS-N}}$·R/W-P·$\overline{\text{RA4-P}}$·$\overline{\text{RB4-P}}$

+F=Ø·$\overline{\text{RAØ-P}}$·$\overline{\text{RB3-P}}$·$\overline{\text{INHSTS-N}}$·R/W-P·$\overline{\text{RA4-P}}$·RB4-P ·RA3-P

+F=2-5·$\overline{\text{RB3-P}}$·$\overline{\text{INHSTS-N}}$·R/W-P·RB4-P

+F=2-7·$\overline{\text{INHSTS-N}}$·R/W-P·$\overline{\text{RB4-P}}$

+F=2-7·RB3-P·$\overline{\text{INHSTS-N}}$·R/W-P

STATUS FPLA CONTINUED

$$\overline{\text{STS CTL5-P}} = F=\emptyset \cdot \text{RA3-P} \cdot \text{RA}\emptyset\text{-P} \cdot \text{RB3-P} \cdot \overline{\text{INHSTS-N}} \cdot \text{R/W-P} \cdot \overline{\text{RA4-P}}$$

$$+F=\emptyset \cdot \text{RA3-P} \cdot \text{RA}\emptyset\text{-P} \cdot \overline{\text{INHSTS-N}} \cdot \text{R/W-P} \cdot \overline{\text{RA4-P}} \cdot \overline{\text{RB4-P}}$$

$$+F=\emptyset \cdot \text{RA3-P} \cdot \text{RA}\emptyset\text{-P} \cdot \overline{\text{RB3-P}} \cdot \overline{\text{INHSTS-N}} \cdot \text{R/W-P} \cdot \overline{\text{RA4-P}} \cdot \text{RB4-P}$$

$$+F=\emptyset \cdot \text{RA3-P} \cdot \overline{\text{RA}\emptyset\text{-P}} \cdot \text{RB3-P} \cdot \overline{\text{INHSTS-N}} \cdot \text{R/W-P} \cdot \overline{\text{RA4-P}} \cdot \text{RB4-P}$$

$$+F=\emptyset \cdot \text{RA3-P} \cdot \overline{\text{RA}\emptyset\text{-P}} \cdot \overline{\text{INHSTS-N}} \cdot \text{R/W-P} \cdot \overline{\text{RA4-P}} \cdot \overline{\text{RB4-P}}$$

$$+F=\emptyset \cdot \text{RA3-P} \cdot \overline{\text{RA}\emptyset\text{-P}} \cdot \text{RB3-P} \cdot \overline{\text{INHSTS-N}} \cdot \text{R/W-P} \cdot \overline{\text{RA4-P}} \cdot \text{RB4-P}$$

$$+F=\emptyset \cdot \overline{\text{RA3-P}} \cdot \overline{\text{RA2-P}} \cdot \text{RA1-P} \cdot \text{RA}\emptyset\text{-P} \cdot \overline{\text{INHSTS-N}} \cdot \overline{\text{RA4-P}}$$

BUS CTL FPLA

SCLKBH1-P = F=Ø·SF=1A·$\overline{\text{CLOD1-P}}$

SCLKBLØ-P = F=Ø·SF=18·$\overline{\text{CLOD1-P}}$

AHI-N = F=Ø-B,D·$\overline{\text{RB3-P}}$·RB4-P
+F=Ø·SF=ØØ,Ø3,Ø4,Ø5,18,1A
+F=1
+F=2-9·Ra=Rb·$\overline{\text{R/W-P}}$·T-P
+F=A,B
+F=C·$\overline{\text{RB3-P}}$·TDATA2-N
+F=C·TDATA2-N·$\overline{\text{R/W-P}}$
+F=C·$\overline{\text{TDATA2-N}}$·$\overline{\text{RA4-P}}$
+F=D·RA1-P
+F=D·RA2-P

ALO-N = F=Ø-B,D·RB3-P·RB4-P
+F=Ø·SF=ØØ,Ø3,Ø4,Ø5,18,1A
+F=1
+F=2-9·Ra=Rb·$\overline{\text{R/W-P}}$·T-P
+F=A,B
+F=C·RB3-P·TDATA2-N
+F=C·TDATA2-N·$\overline{\text{R/W-P}}$
+F=C·TDATA2-N·$\overline{\text{RA4-P}}$
+F=D·RA1-P
+F=D·RA2-P

BUSCTL2-P = F=Ø·SF=ØØ,Ø2,1C,1E
+F=1-B·Ra=Rb
+F=C·$\overline{\text{TDATA2-N}}$

BUS CTL FPLA CONTINUED

```
BUSCTL1-P  =  F=Ø·SF=1C,1E
              +F=C·TDATA2-N·R/W-P
              +F=D·IC=Ø,1,8,9

BUSCTLØ-P  =  F=Ø·SF=ØØ,Ø2,Ø6,1E
              +F=C·TDATA2-N·R/W-P
              +F=C·¯TDATA2-N¯
              +F=D·IC=Ø,1,8,9
```

APPENDIX B

HOW TO READ FPLA LISTINGS

The document numbers for the program listings of the 7 programmed FPLA devices used in the Q30 are given below:

BUS CTL FPLA	A44000
TIMING 1 FPLA	A44001
TIMING 2 FPLA	A44002
INSTRUCTION 1 FPLA	A42243
INSTRUCTION 2 FPLA	A42244
MISCELLANEOUS FPLA	A44003
STATUS FPLA	A42246

Since it will be necessary for technicians and engineers to learn to decipher these listings directly, a short course is given here on reading FPLA program listings.

1) Always work from the output signal backwards. From the list of OUTPUT SIGNALS at the right of each page determine the F number (FØ through F7) of the signal to be investigated.

2) In the group of 8 columns in the center of the sheet, locate the desired F number column under ACTIVE OUTPUT.

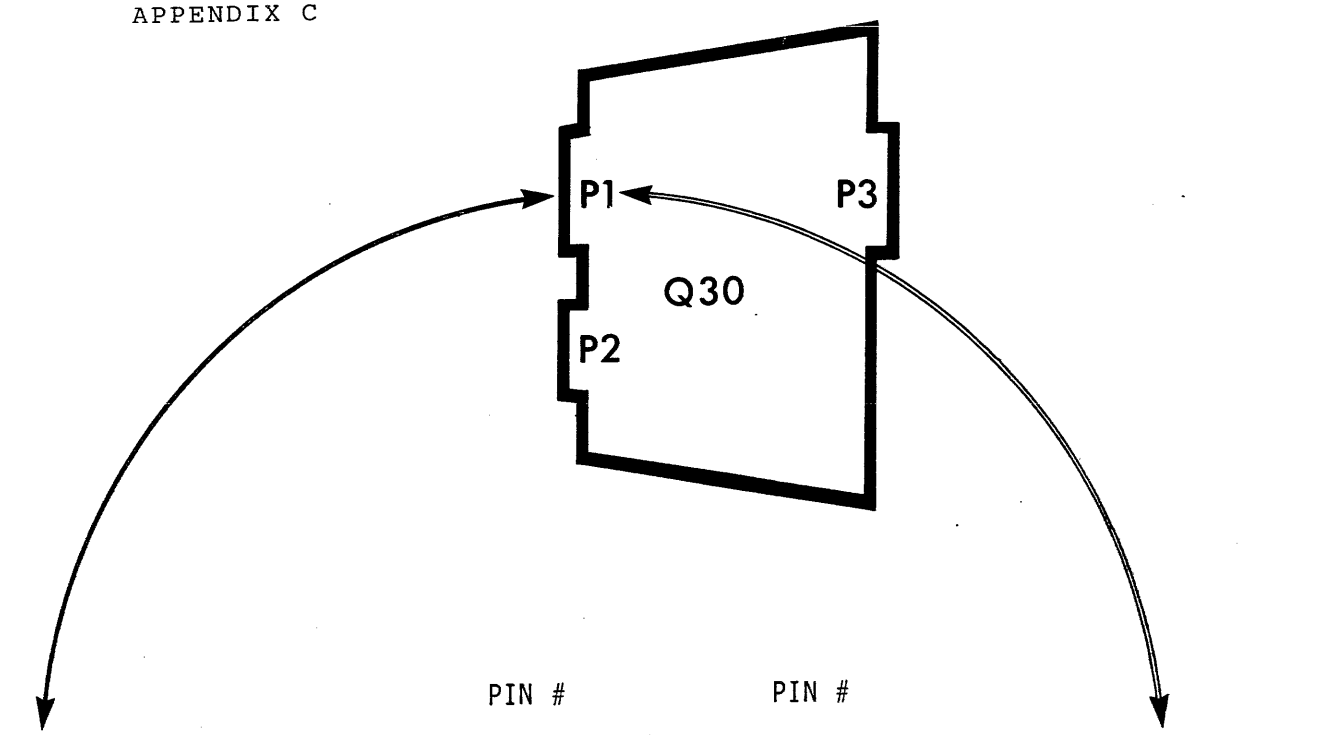
3) Determine if the signal has been programmed as active high or active low by examining the box directly above the column number. The H or L under OUTPUT LEVEL specifies if the output signal column has been programmed as active high (H) or active low (L). If the output signal acronym ends in -P and an H appears under OUTPUT LEVEL, each horizontal entry in the

PRODUCT TERM table noted by an A under the output signals ACTIVE OUTPUT column indicates an input condition that will drive the output line logically high. Occasionally it takes fewer product terms to program a signal for its inactive state. Always compare the contents of the signal's OUTPUT LEVEL box with the signal acronym's active state definition (-P, -N). If the output signal acronym ends in -P and an L appears in under the signals OUTPUT LEVEL designation, each active product term will drive the signal logically low.

4) Assume a signal acronym ending in -N whose OUTPUT LEVEL box contains an L. The active logic equations will drive the output signal logically low. Reading down the ACTIVE OUTPUT column having the correct F number for this output signal, stop at each A encountered and decode the product term situated on this line, horizontally to the left. The input variables assume numbered columns in the PRODUCT TERM table. A list relating the numbers of the input variables (Ø-15) to the signal acronyms is given at the right of the sheet under INPUT SIGNALS. Only those input variables specified by an H (high) or an L (low) need to be considered. All other boxes marked with a hyphen (-) may be disregarded.

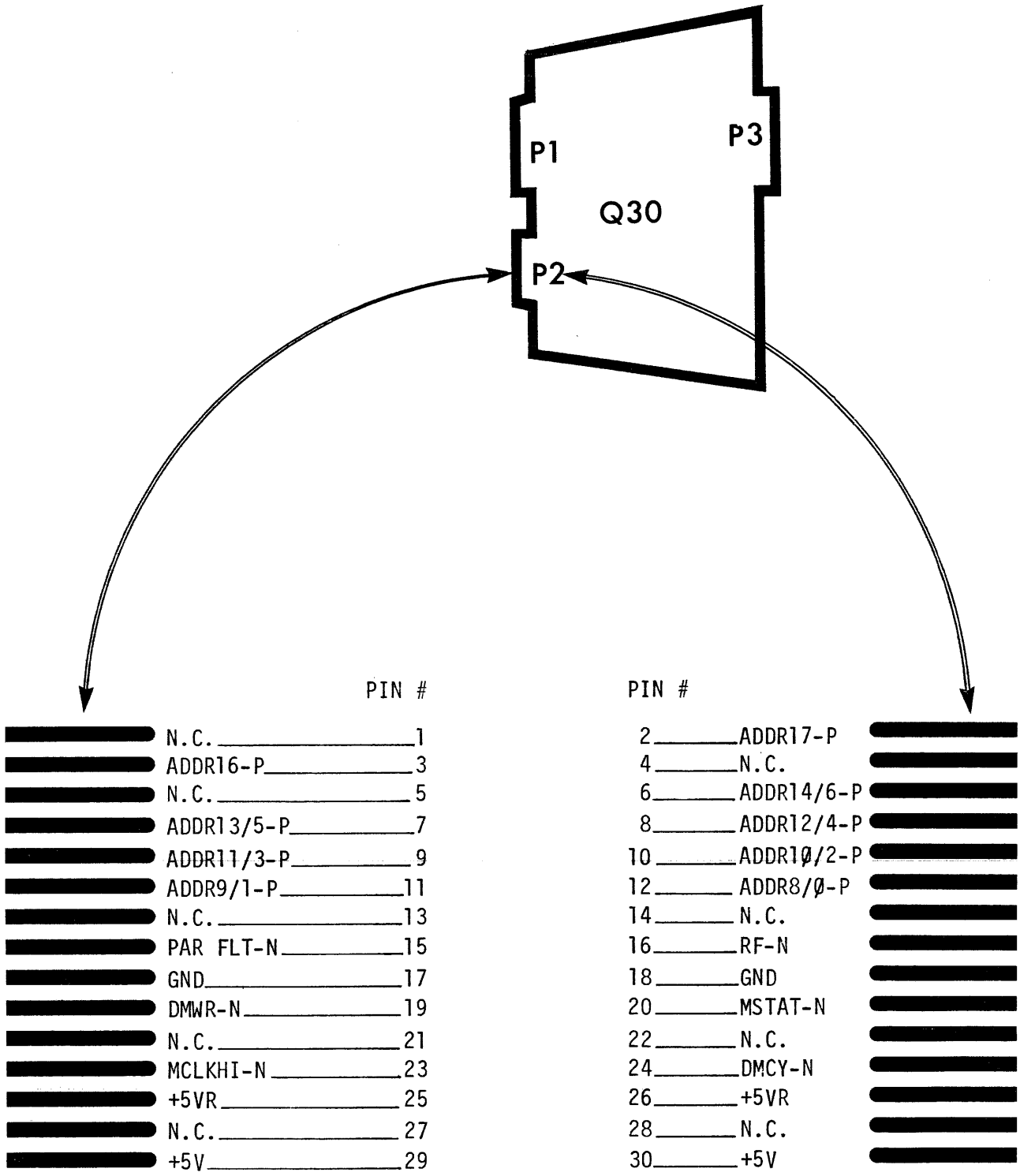
5) The output signals logic equation is then written by expressing the logical And of all the input variables of each active product term, then write the logical Or of all these active product expressions. This yields the logic equations familiar "sum of products" form. Often many of the product terms in the logic expression overlap each other and can be reduced to fewer terms.

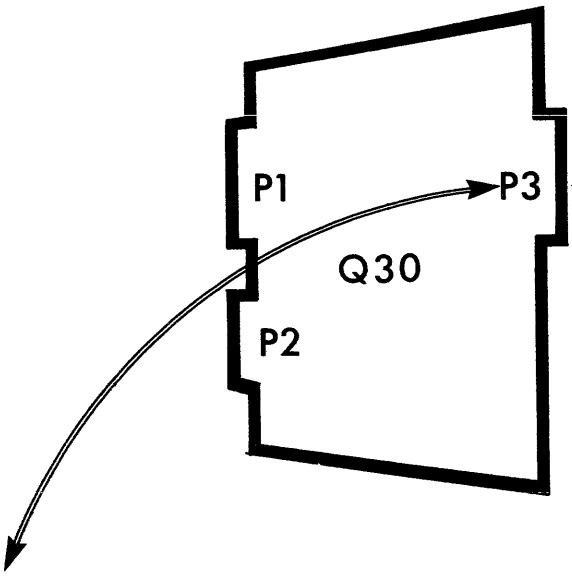
APPENDIX C



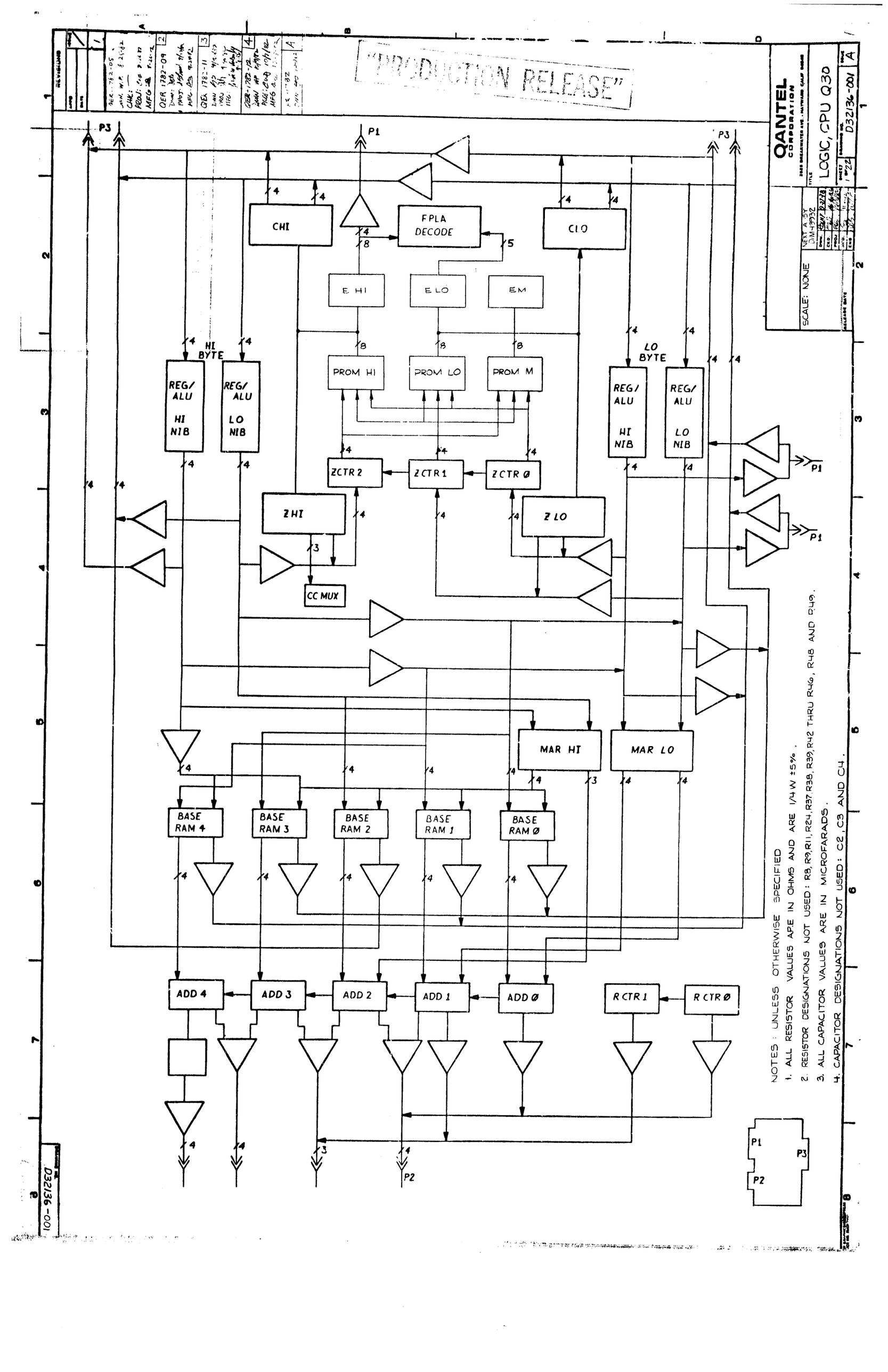
PIN #		PIN #	
1	+5V	2	+5V
3	STROBE-N	4	GND
5	N.C.	6	IOEØØ-N
7	IOEØ1-N	8	IOEØ2-N
9	IOEØ3-N	10	GND
11	INT-N	12	ISEL-P (GND)
13	DAØØ-P	14	DAØ1-P
15	DAØ2-P	16	DAØ3-P
17	DA1Ø-P	18	DA11-P
19	DA12-P	20	DA13-P
21	GND	22	GND
23	GND	24	GND
25	PFL-N	26	GND
27	N.C.	28	SYS RES-N
29	N.C.	30	N.C.
31	STS-N	32	HLT LT-N
33	N.C.	34	N.C.
35	CIPL-N	36	N.C.
37	PFL-P	38	N.C.
39	N.C.	40	N.C.
41	N.C.	42	N.C.
43	N.C.	44	N.C.
45	STP REQ-N	46	PWR DWN-N
47	ADDR18-P	48	ADDR19-P
49	ADDR15/7-P	50	N.C.

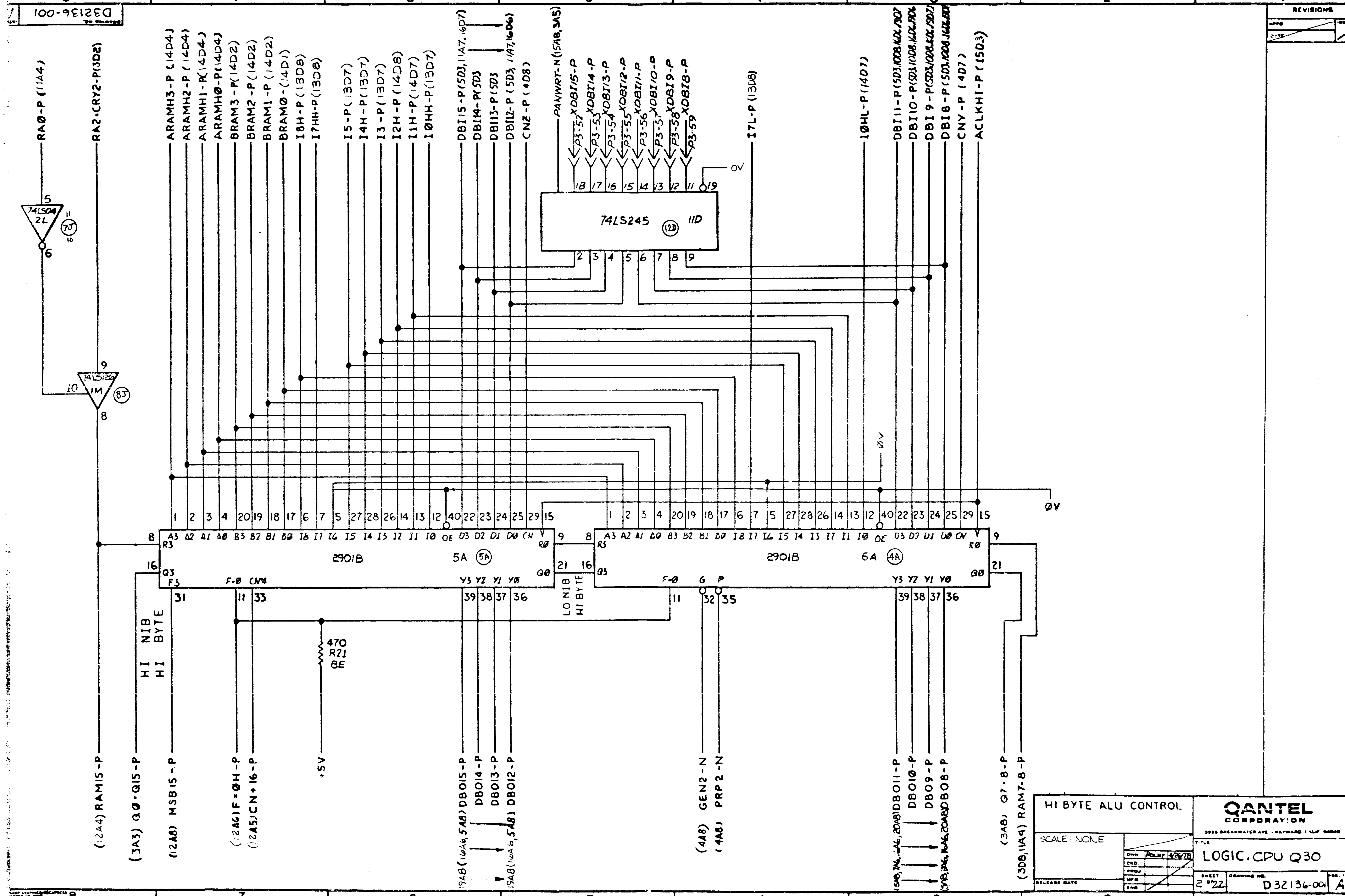
N.C. = no connection


P1
P3
Q30
P2
PIN #
N.C. 1
ADDR16-P 3
N.C. 5
ADDR13/5-P 7
ADDR11/3-P 9
ADDR9/1-P 11
N.C. 13
PAR FLT-N 15
GND 17
DMWR-N 19
N.C. 21
MCLKHI-N 23
+5VR 25
N.C. 27
+5V 29
PIN #
2 ADDR17-P
4 N.C.
6 ADDR14/6-P
8 ADDR12/4-P
10 ADDR10/2-P
12 ADDR8/0-P
14 N.C.
16 RF-N
18 GND
20 MSTAT-N
22 N.C.
24 DMCY-N
26 +5VR
28 N.C.
30 +5V



GND	1	2	GND
+5V	3	4	+5V
PANMW23-P	5	6	PANMW22-P
PANMW21-P	7	8	PANMW2Ø-P
BZADDR6-P	9	10	HALTIF-N
BZADDR1-P	11	12	BZADDR7-P
BZADDR3-P	13	14	BZADDRØ-P
PANMW13-P	15	16	BZADDR5-P
TDATA2-N	17	18	PANWRT-N
FETCH	19	20	BZADDR4-P
PANMW11-P	21	22	BZADDR2-P
PANMW9-P	23	24	CLK-N
XDB6-P	25	26	BZADDR12-P
XDB1-P	27	28	PANMW1Ø-P
XDBØ-P	29	30	BZADDR8-P
XDB4-P	31	32	PANMW8-P
XDB5-P	33	34	BZADDR9-P
XDB3-P	35	36	BZADDR1Ø-P
XDB2-P	37	38	BZADDR11-P
XDB7-P	39	40	PANMW12-P
PANMW19-P	41	42	PANMW18-P
PANMW17-P	43	44	PANMW16-P
PANMW15-P	45	46	PANMW14-P
+5V	47	48	+5V
GND	49	50	GND
N.C.	51	52	XDBI15-P
XDBI14-P	53	54	XDBI13-P
XDBI12-P	55	56	XDBI11-P
XDBI1Ø-P	57	58	XDBI9-P
XDBI8-P	59	60	N.C.
PANMW6-P	61	62	PANMW7-P
PANMW4-P	63	64	PANMW5-P
PANMW2-P	65	66	PANMW3-P
PANMWØ-P	67	68	PANMW1-P
BCONLOD-P	69	70	N.C.


"PRODUCTION RELEASE"
QANTEL CORPORATION
LOGIC, CPU Q30
D32136-001
SCALE: NONE
P3
P1
CHI
FPLA DECODE
CLO
E HI
E LO
EM
HI BYTE
LO BYTE
PROM HI
PROM LO
PROM M
REG/ ALU HI NIB
REG/ ALU LO NIB
ZCTR 2
ZCTR 1
ZCTR Ø
ZHI
ZLO
CC MUX
MAR HI
MAR LO
BASE RAM 4
BASE RAM 3
BASE RAM 2
BASE RAM 1
BASE RAM Ø
ADD 4
ADD 3
ADD 2
ADD 1
ADD Ø
RCTR 1
RCTR Ø
P2
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS AND ARE 1/4 W ±5%.
2. RESISTOR DESIGNATIONS NOT USED: R8, R9, R11, R24, R37, R38, R39, R42 THRU R46, R48 AND R49.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. CAPACITOR DESIGNATIONS NOT USED: C2, C3 AND C4.



HI BYTE ALU CONTROL

SCALE: NONE

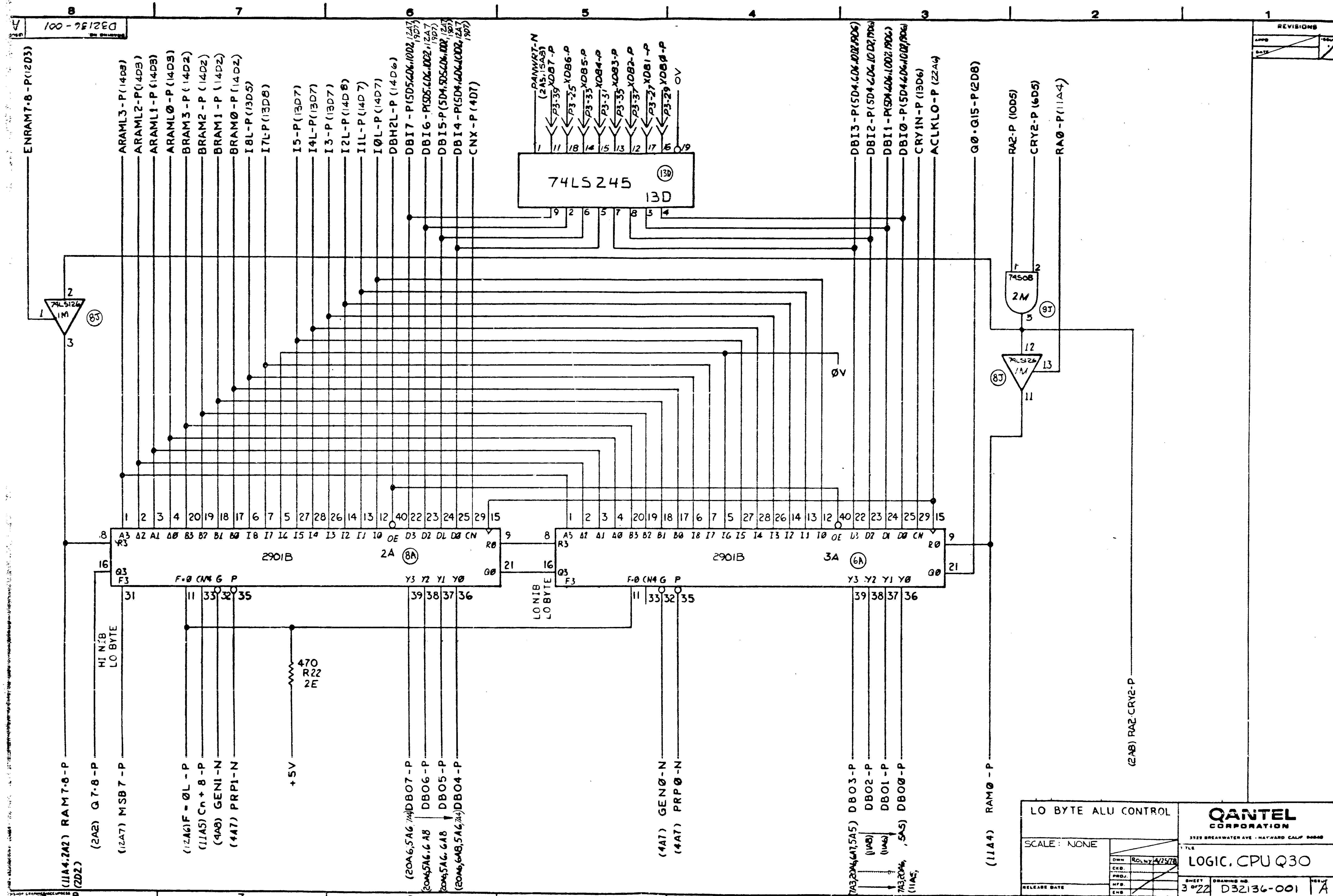
QANTEL CORPORATION

LOGIC. CPU Q30

SHEET 2 OF 22

DRAWING NO. D32136-001

REV. A



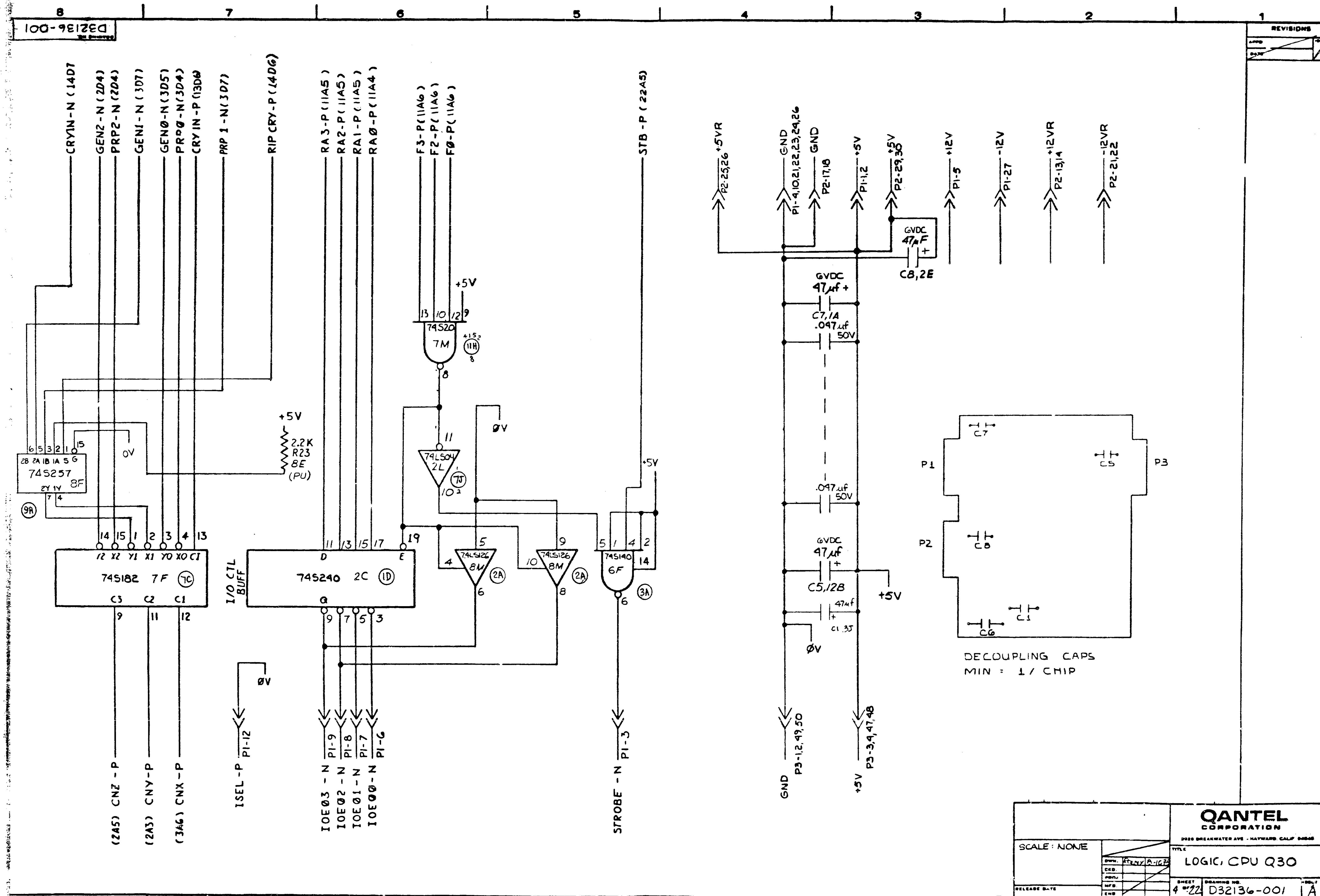
LO BYTE ALU CONTROL

SCALE: NONE

QANTEL CORPORATION

LOGIC, CPU Q30

SHEET 3 OF 22 DRAWING NO. D32136-001 ISSUE A

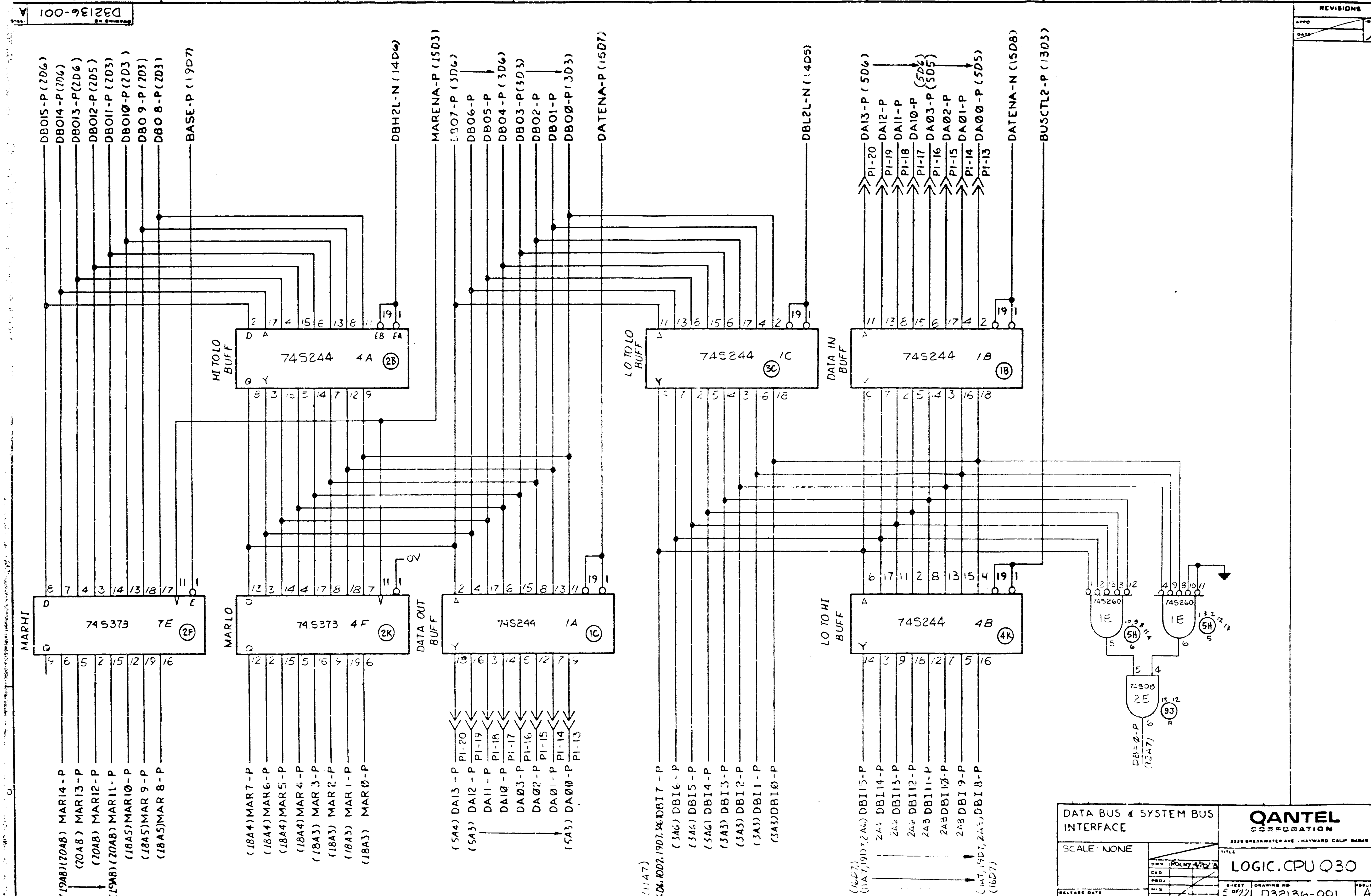


QANTEL CORPORATION

SCALE: NONE

LOGIC, CPU Q30

SHEET 4 OF 22 — DRAWING NO. D32136-001 — A



DATA BUS & SYSTEM BUS INTERFACE

SCALE: NONE

QANTEL CORPORATION

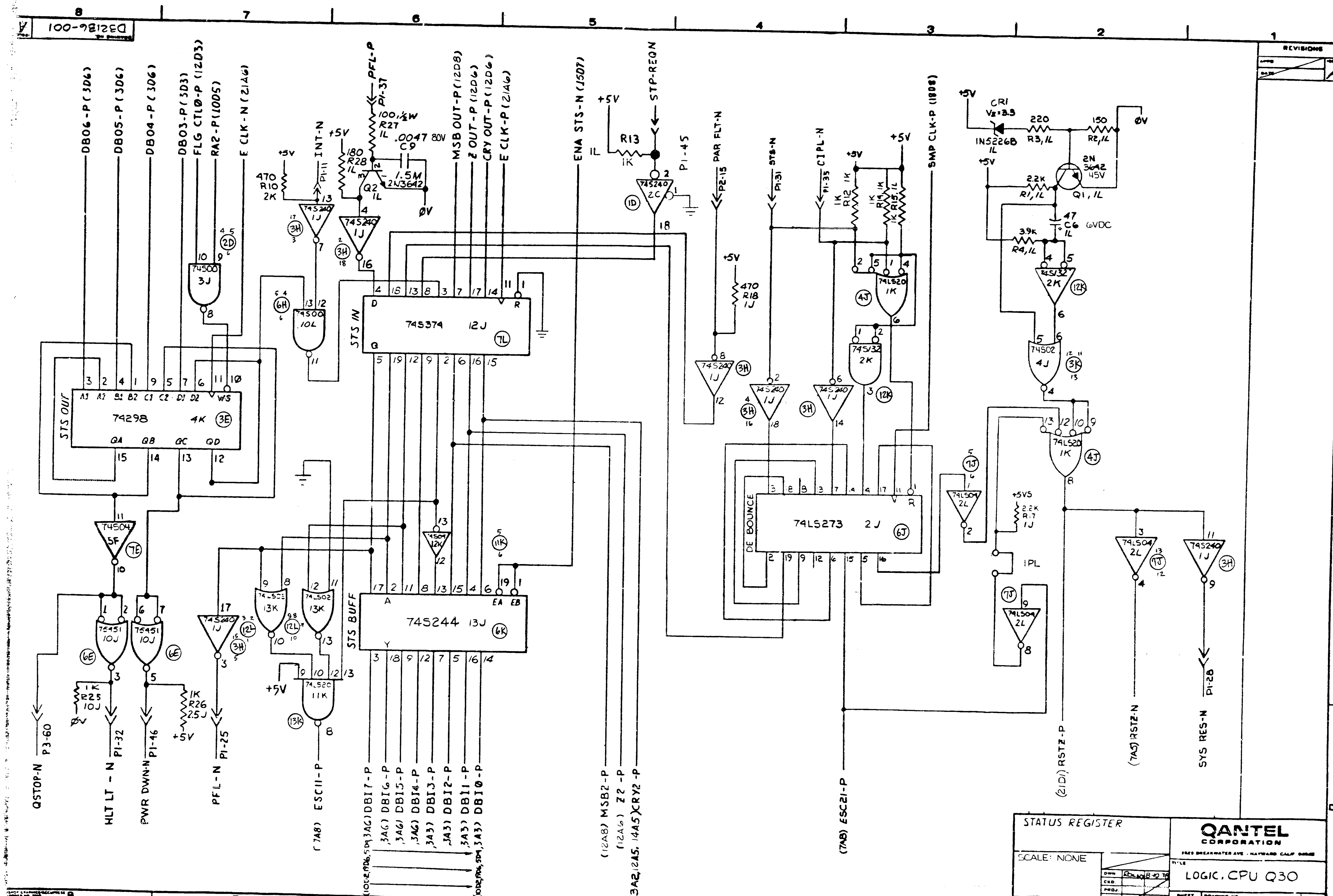
3525 BREAKWATER AVE · HAYWARD CALIF 94545

LOGIC. CPU Q30

SHEET 5 OF 22

DRAWING NO. D32136-001

REV A



STATUS REGISTER

SCALE: NONE

QANTEL CORPORATION

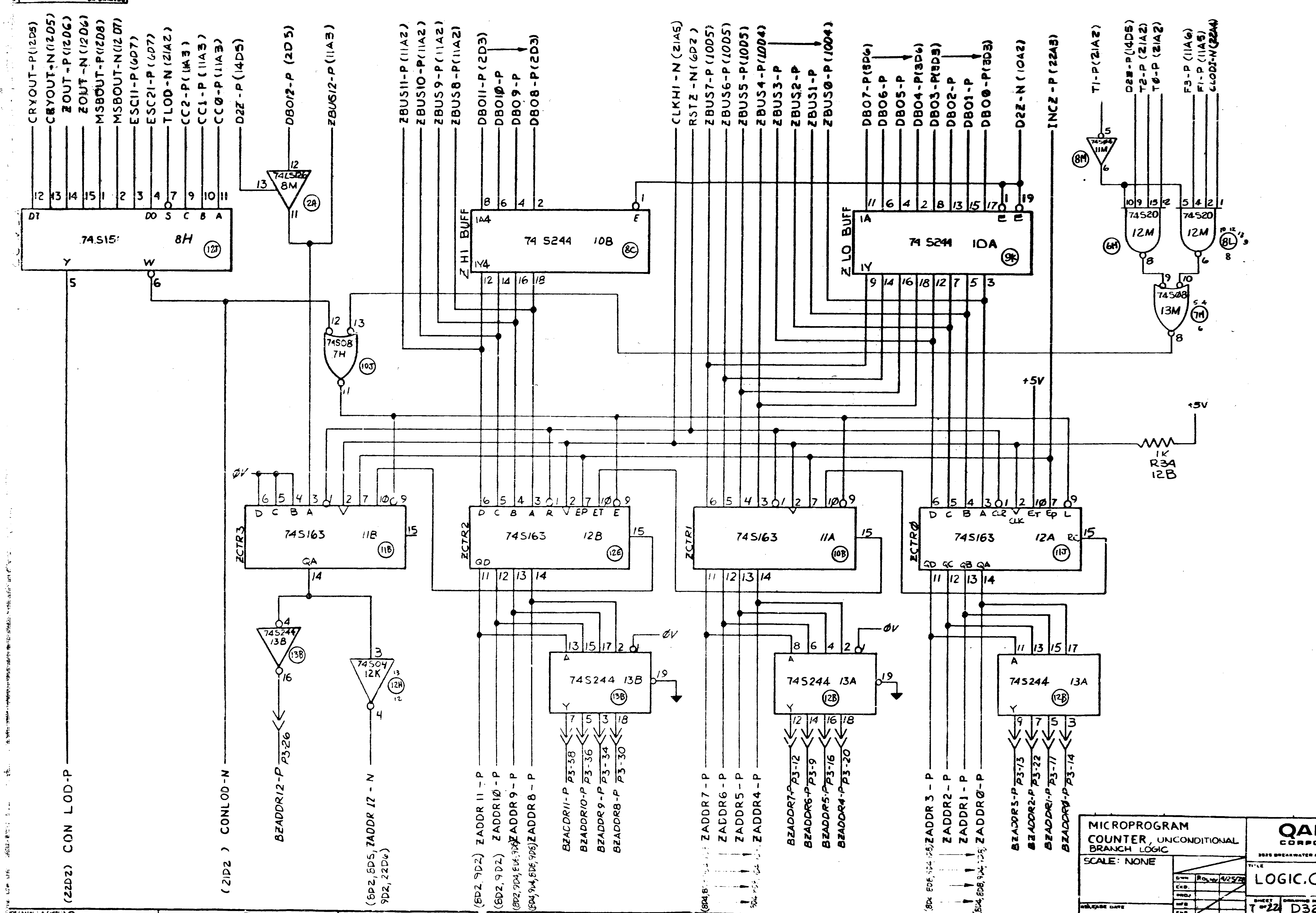
LOGIC, CPU Q30

SHEET 6 OF 22

DRAWING NO. D32136-001

REV. A

D32136-001



MICROPROGRAM COUNTER, UNCONDITIONAL BRANCH LOGIC

SCALE: NONE

QANTEL CORPORATION

LOGIC.CPU Q30

D32136-001 A

ZADDR10-P (7D6)
ZADDR9-P (7D6)
ZADDR8-P (7D5)
ZADDR7-P (7D4)
ZADDR6-P (7D4)
ZADDR5-P (7D4)
ZADDR4-P (7D4)
ZADDR3-P (7D3)
ZADDR2-P (7D3)
ZADDR1-P (7D3)
ZADDRØ-P (7D3)
ENAWRD-N (22A5)
ZADDR12-N (7D6)
ZADDR11-P (7D6)

74S04 7L (12A)

MID MICROPROGRAM MEMORY

Q30-1M 825191 13F (8F)
Q30-2M 825191 12F (6F)

AIO AØ CE1 CE2 CE3
21 22 23 1 2 3 4 5 6 7 8 20 19 18
D8 D1
17 16 15 14 13 11 10 9

MWB15-P
MWB14-P
MWB13-P
MWB12-P
MWB11-P
MWB10-P
MWB9-P
MWB8-P

(17D4) (10D5)
(17D4)
(17D5)
(17D5) (10D5)

(8D1, 9D2) ENAWRD-P

HIGH MICROPROGRAM MEMORY

Q30-1H 825191 11F (10F)
Q30-2H 825191 9F (9F)

MWB23-P
MWB22-P
MWB21-P
MWB20-P
MWB19-P
MWB18-P
MWB17-P
MWB16-P

(11D7)
(17D8)
(17D8)
(17D7)
(17D7)
(21D7)

SIZE	DWG NO.	REV.
D	32136-001	A
SCALE NONE	SHEET 8 OF 22	

FORM 687-C 9/88

ZADDR10-P (7D6)
ZADDR9-P (7D6)
ZADDR8-P(7D5)
ZADDR7-P(7D4)
ZADDR6-P (7D4)
ZADDR5-P(7D4)
ZADDR4-P(7D4)
ZADDR3-P(7D3)
ZADDR2-P(7D3)
ZADDR1-P(7D8)
ZADDR0-P(7D3)

ENAWRD-N(15D3,2245)
ZADDR12-N(7D6)
ZADDR11-P(7D6)

ENAWRD-P(8A5)

LOW MICROPROGRAM MEMORY

Q30-1L
82S191
12L
(12F)

Q30-2L
82S191
12H
(11F)

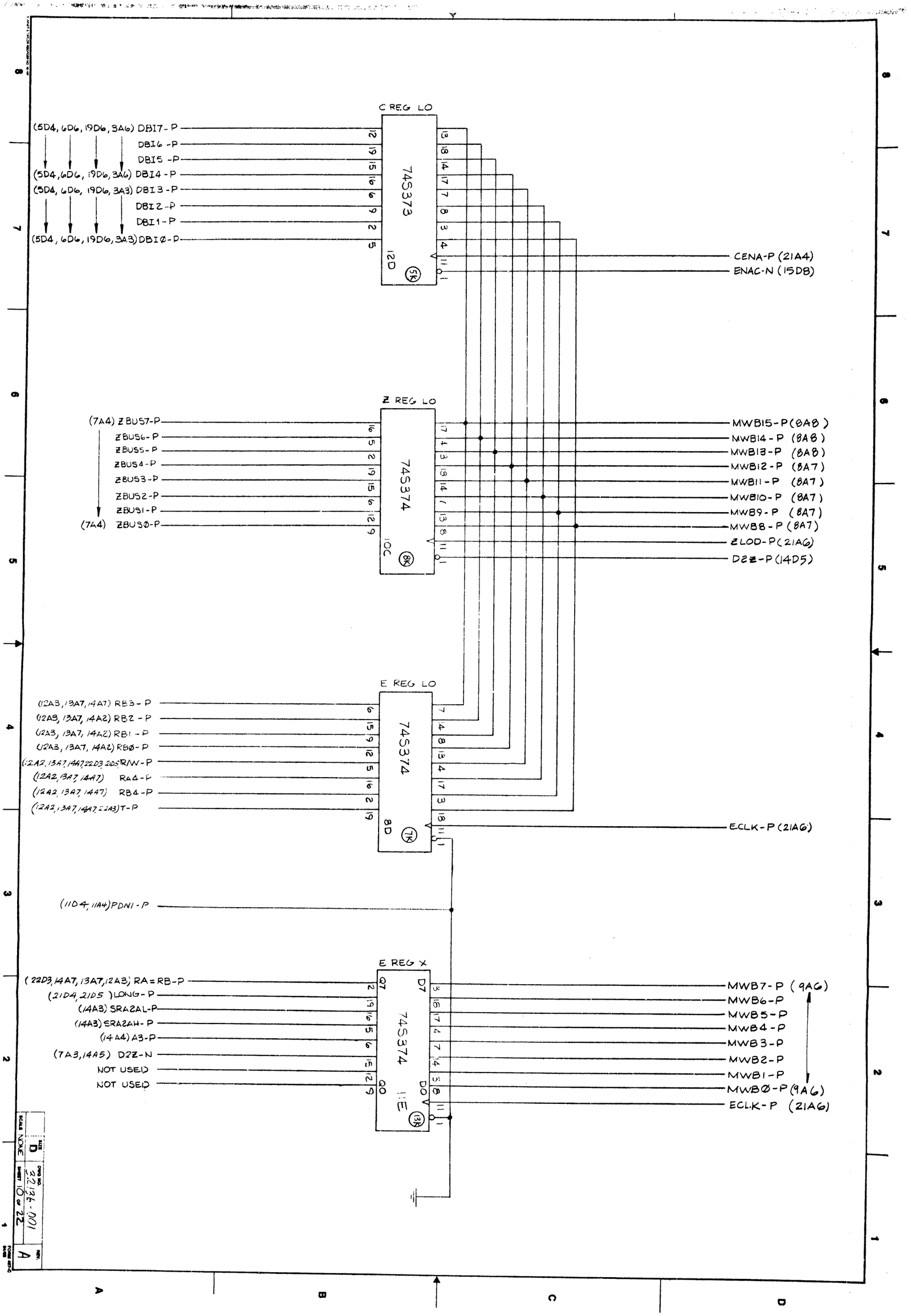
A10 A0 CE1 CE2 CE3
21 22 23 1 2 3 4 5 6 7 8 20 19 18
D8 D1
17 16 15 14 13 11 10 9

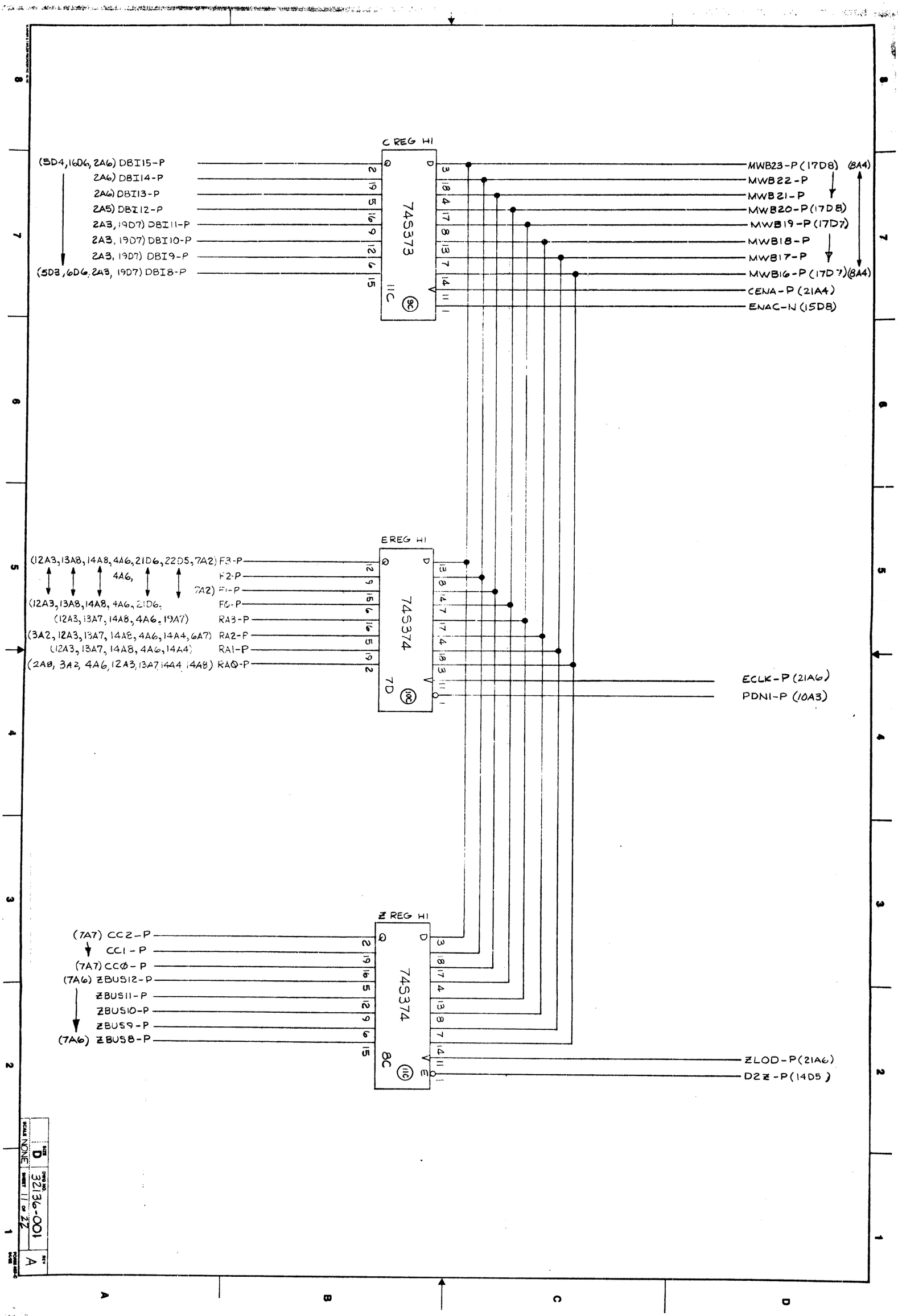
MWB7-P
MWB6-P
MWB5-P
MWB4-P
MWB3-P
MWB2-P
MWB1-P
MWB0-P

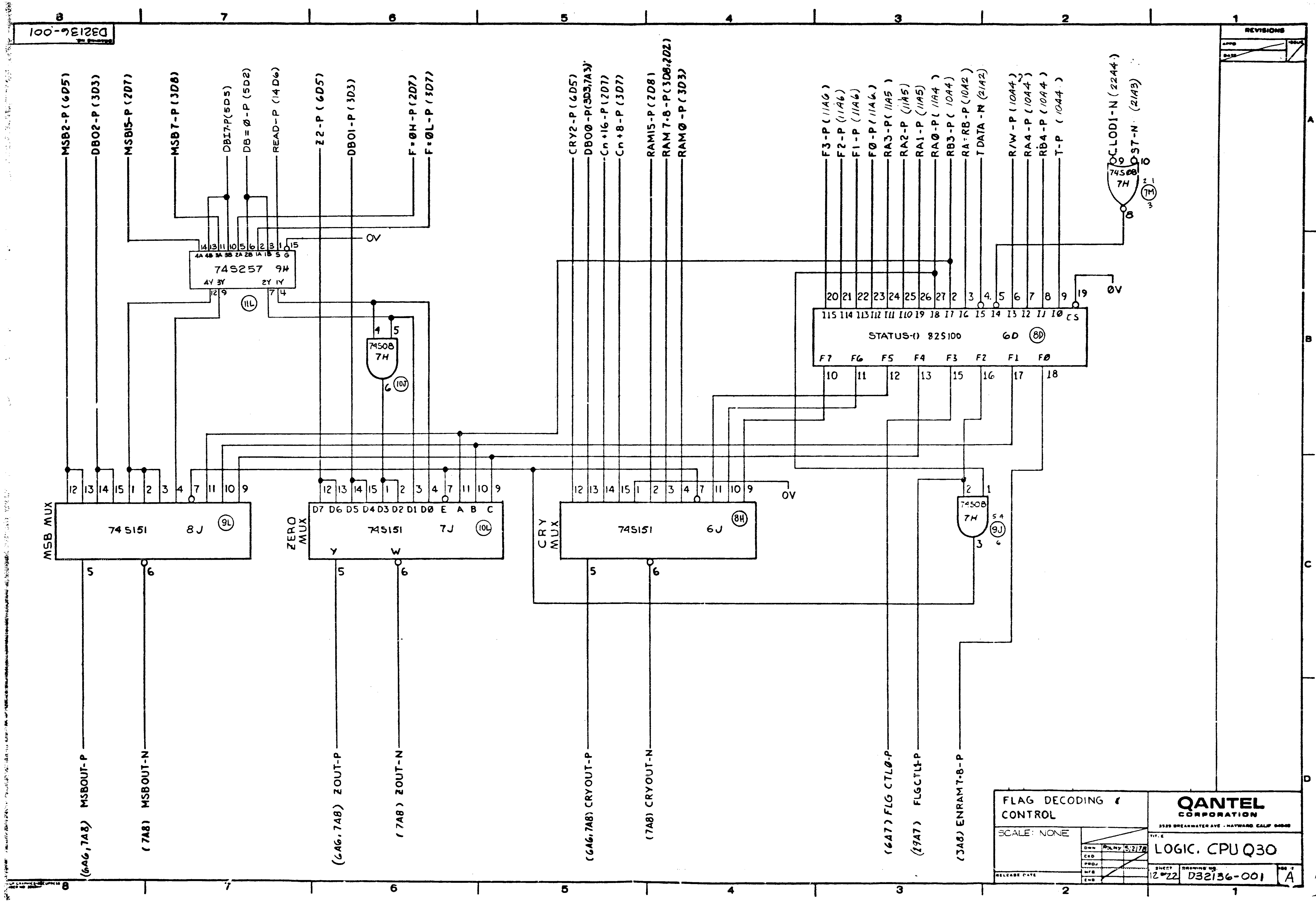
(17D3, 10D2)
(17D2, 10D2)

SIZE	DWG NO.	REV
D	32136-001	A
SCALE NONE	SHEET 9 OF 22	

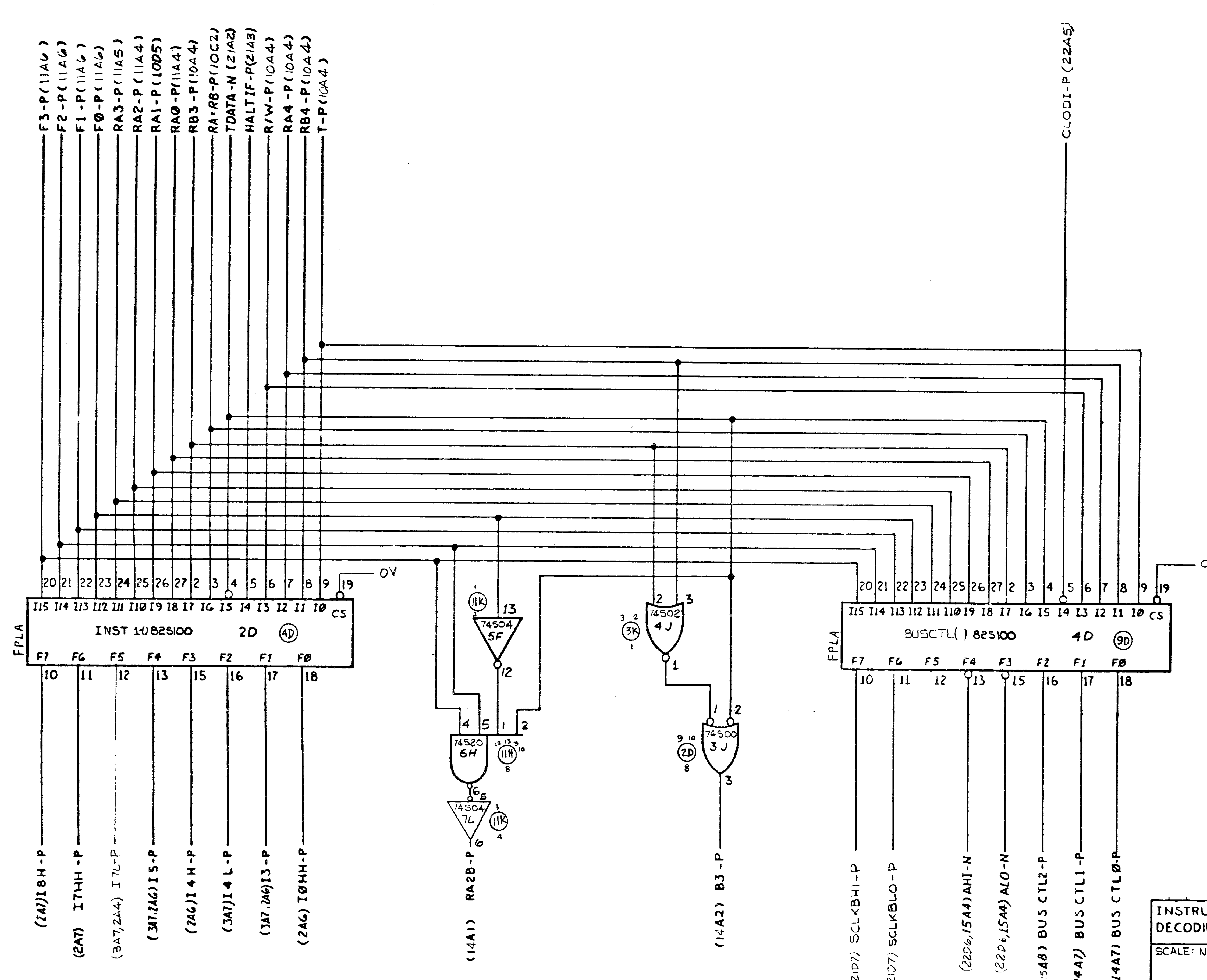
FORM 659-C 04/85


C REG LO
(5D4, 6D6, 19D6, 3A6) DBI7-P
DBI6-P
DBI5-P
(5D4, 6D6, 19D6, 3A6) DBI4-P
(5D4, 6D6, 19D6, 3A3) DBI3-P
DBI2-P
DBI1-P
(5D4, 6D6, 19D6, 3A3) DBIØ-P
74S373
12D
5K
CENA-P (21A4)
ENAC-N (15D8)
N REG LO
(7A4) ZBUS7-P
ZBUS6-P
ZBUS5-P
ZBUS4-P
ZBUS3-P
ZBUS2-P
ZBUS1-P
(7A4) ZBUSØ-P
74S374
10C
8K
MWBI5-P (8A8)
MWBI4-P (8A8)
MWBI3-P (8A8)
MWBI2-P (8A7)
MWBII-P (8A7)
MWBIO-P (8A7)
MWB9-P (8A7)
MWB8-P (8A7)
ZLOD-P (21A6)
D2Z-P (14D5)
E REG LO
(12A3, 13A7, 14A7) RB3-P
(12A3, 13A7, 14A2) RB2-P
(12A3, 13A7, 14A2) RB1-P
(12A3, 13A7, 14A2) RBØ-P
(12A2, 13A7, 14A7, 22D3, 20D5) R/W-P
(12A2, 13A7, 14A7) RA4-P
(12A2, 13A7, 14A7) RB4-P
(12A2, 13A7, 14A7, 22A3) T-P
74S374
8D
7K
ECLK-P (21A6)
(11D4, 11A4) PDNI-P
E REG X
(22D3, 14A7, 13A7, 12A3) RA=RB-P
(21D4, 21D5) LONG-P
(14A3) SRA2AL-P
(14A3) SRA2AH-P
(14A4) A3-P
(7A3, 14A5) D2Z-N
NOT USED
NOT USED
74S374
11E
13K
MWB7-P (9A6)
MWB6-P
MWB5-P
MWB4-P
MWB3-P
MWB2-P
MWB1-P
MWBØ-P (9A6)
ECLK-P (21A6)
SIZE D
DWG NO 22134-001
SHEET 10 OF 22
REV A
SCALE NONE


C REG HI
(5D4,16D6,2A6) DBI15-P
2A6) DBI14-P
2A6) DBI13-P
2A5) DBI12-P
2A3,19D7) DBI11-P
2A3,19D7) DBI10-P
2A3,19D7) DBI9-P
(5D3,6D6,2A3,19D7) DBI8-P
74S373
11C
MWB23-P (17D8) (8A4)
MWB22-P
MWB21-P
MWB20-P (17D8)
MWB19-P (17D7)
MWB18-P
MWB17-P
MWB16-P (17D7) (8A4)
CENA-P (21A4)
ENAC-N (15D8)
EREG HI
(12A3,13A8,14A8,4A6,21D6,22D5,7A2) F3-P
4A6,
F2-P
7A2) F1-P
(12A3,13A8,14A8,4A6,21D6,
F0-P
(12A3,13A7,14A8,4A6,19A7)
RA3-P
(3A2,12A3,13A7,14A8,4A6,14A4,6A7) RA2-P
(12A3,13A7,14A8,4A6,14A4)
RA1-P
(2A8,3A2,4A6,12A3,13A7,14A4,14A8) RA0-P
74S374
7D
ECLK-P (21A6)
PDN1-P (10A3)
Z REG HI
(7A7) CC2-P
CC1-P
(7A7) CC0-P
(7A6) ZBUS12-P
ZBUS11-P
ZBUS10-P
ZBUS9-P
(7A6) ZBUS8-P
74S374
8C
ZLOD-P (21A6)
D2Z-P (14D5)
SIZE D
SCALE NONE
ORDER NO. 32136-001
SHEET 11 OF 22
REV A



FLAG DECODING & CONTROL
QANTEL CORPORATION
SCALE: NONE
LOGIC. CPU Q30
12 OF 22
D32136-001
A



INSTRUCTION & ADDRESS DECODING

SCALE: NONE

QANTEL CORPORATION

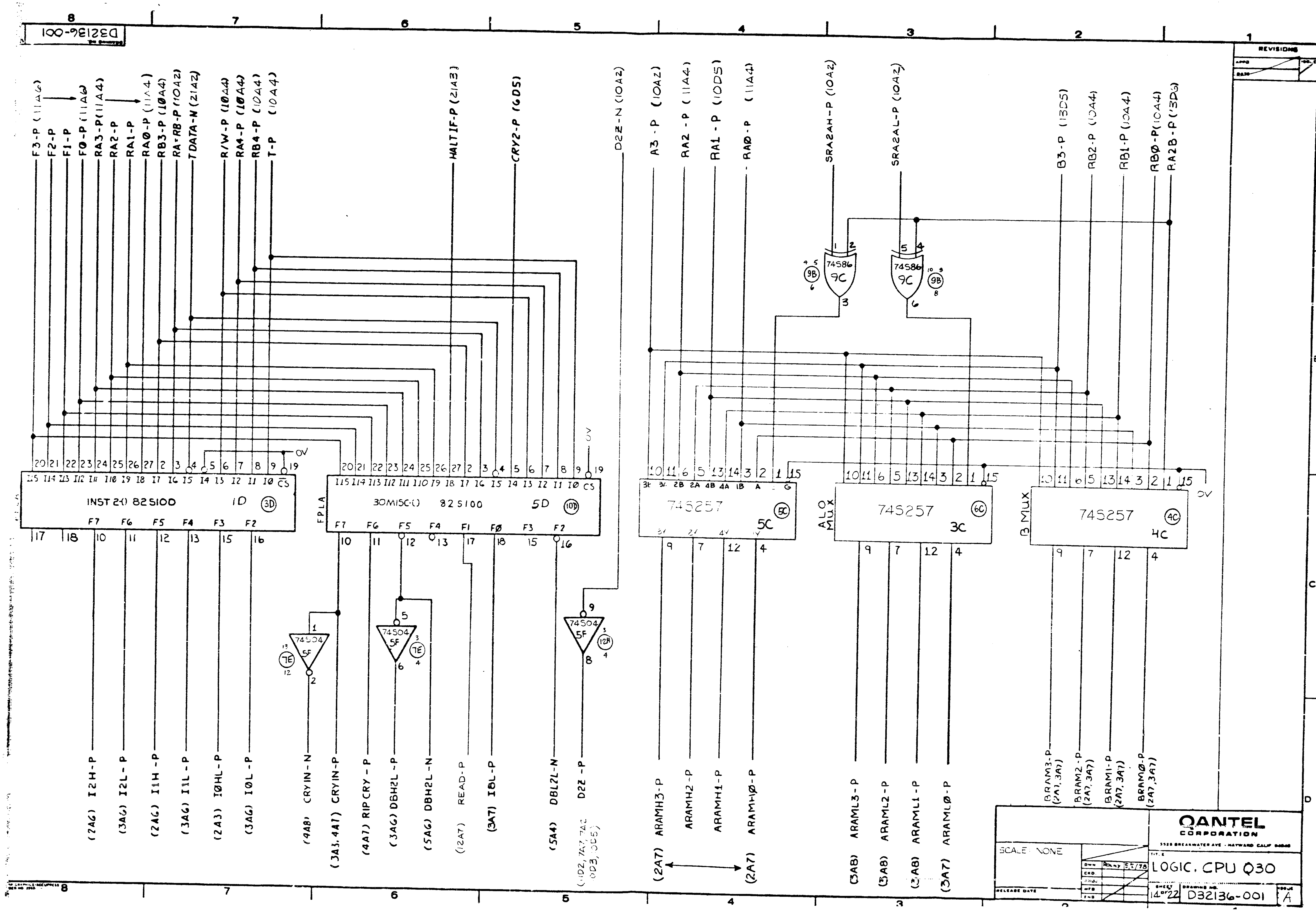
3525 BREAKWATER AVE · HAYWARD CALIF 94545

TITLE: LOGIC, CPU Q30

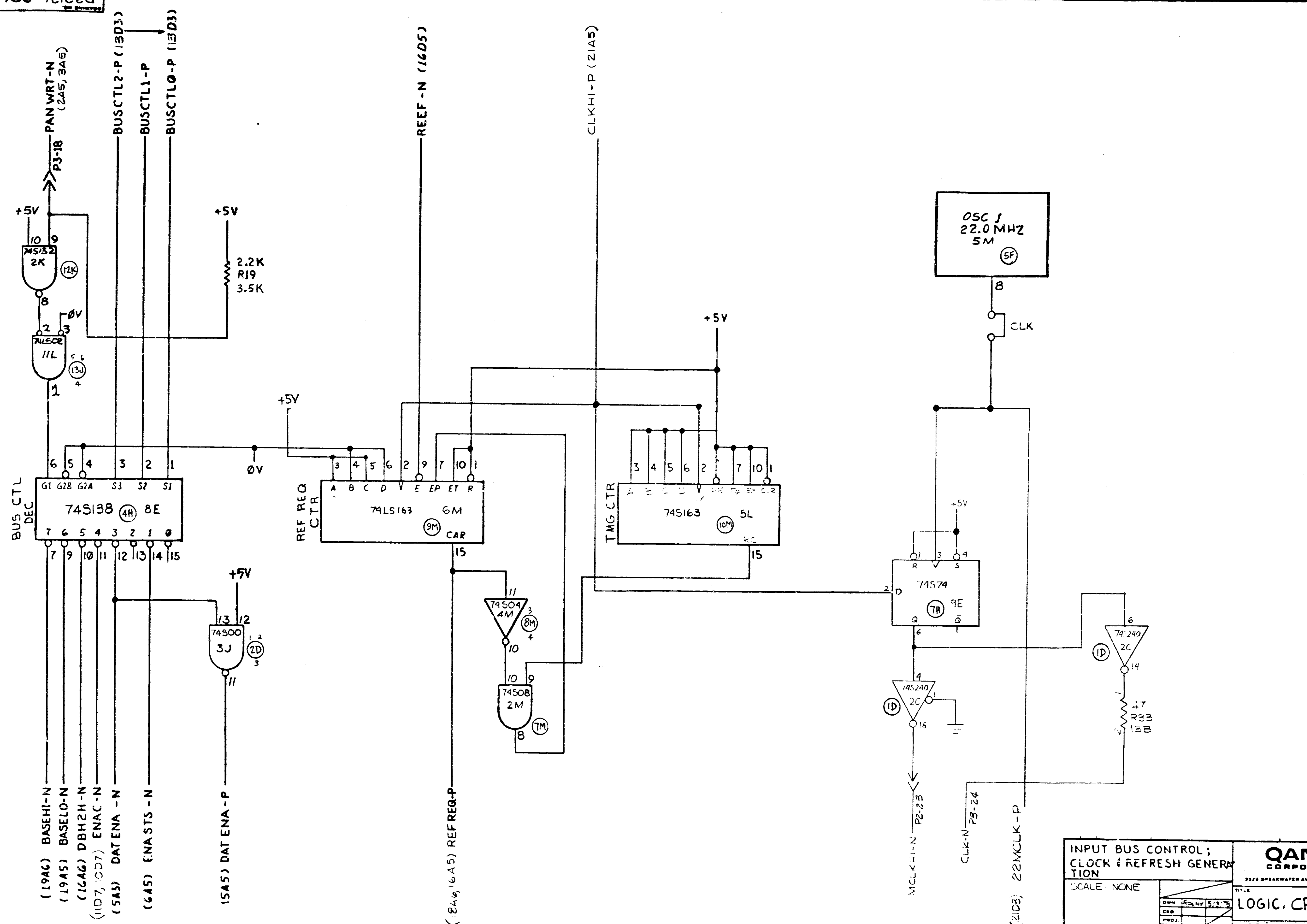
SHEET 13 OF 22 — DRAWING NO. D32136-001 — REV. A

DWN 5/3/78

D32136-001



D32136-001
F3-P (11A6)
F2-P
F1-P
F0-P (11A6)
RA3-P (11A4)
RA2-P
RA1-P
RA0-P (11A4)
RB3-P (10A4)
RA=RB-P (10A2)
TDATA-N (21A2)
R/W-P (10A4)
RA4-P (10A4)
RB4-P (10A4)
T-P (10A4)
HALTIF-P (21A3)
CRY2-P (6D5)
D2Z-N (10A2)
A3-P (10A2)
RA2-P (11A4)
RA1-P (10D5)
RA0-P (11A4)
SRA2AH-P (10A2)
SRA2AL-P (10A2)
B3-P (13D5)
RB2-P (10A4)
RB1-P (10A4)
RB0-P (10A4)
RA2B-P (13D6)
74S86
9C
INST 2() 82S100
1D
30MISC-() 82S100
5D
FPLA
74S257
5C
ALU MUX
3C
B MUX
4C
74S04
5F
(2A6) I2H-P
(3A6) I2L-P
(2A6) I1H-P
(3A6) I1L-P
(2A3) I0HL-P
(3A6) I0L-P
(4A8) CRYIN-N
(3A3,4A1) CRYIN-P
(4A1) RIPCRY-P
(3A6) DBH2L-P
(5A6) DBH2L-N
(12A7) READ-P
(3A7) IBL-P
(5A4) DBL2L-N
D2Z-P
(2A7) ARAMH3-P
ARAMH2-P
ARAMH1-P
(2A7) ARAMH0-P
(3A8) ARAML3-P
(3A8) ARAML2-P
(3A8) ARAML1-P
(3A7) ARAML0-P
BRAM3-P (2A7,3A7)
BRAM2-P (2A7,3A7)
BRAM1-P (2A7,3A7)
BRAM0-P (2A7,3A7)
REVISIONS
QANTEL CORPORATION
SCALE: NONE
LOGIC, CPU Q30
SHEET 14 OF 22
D32136-001
A



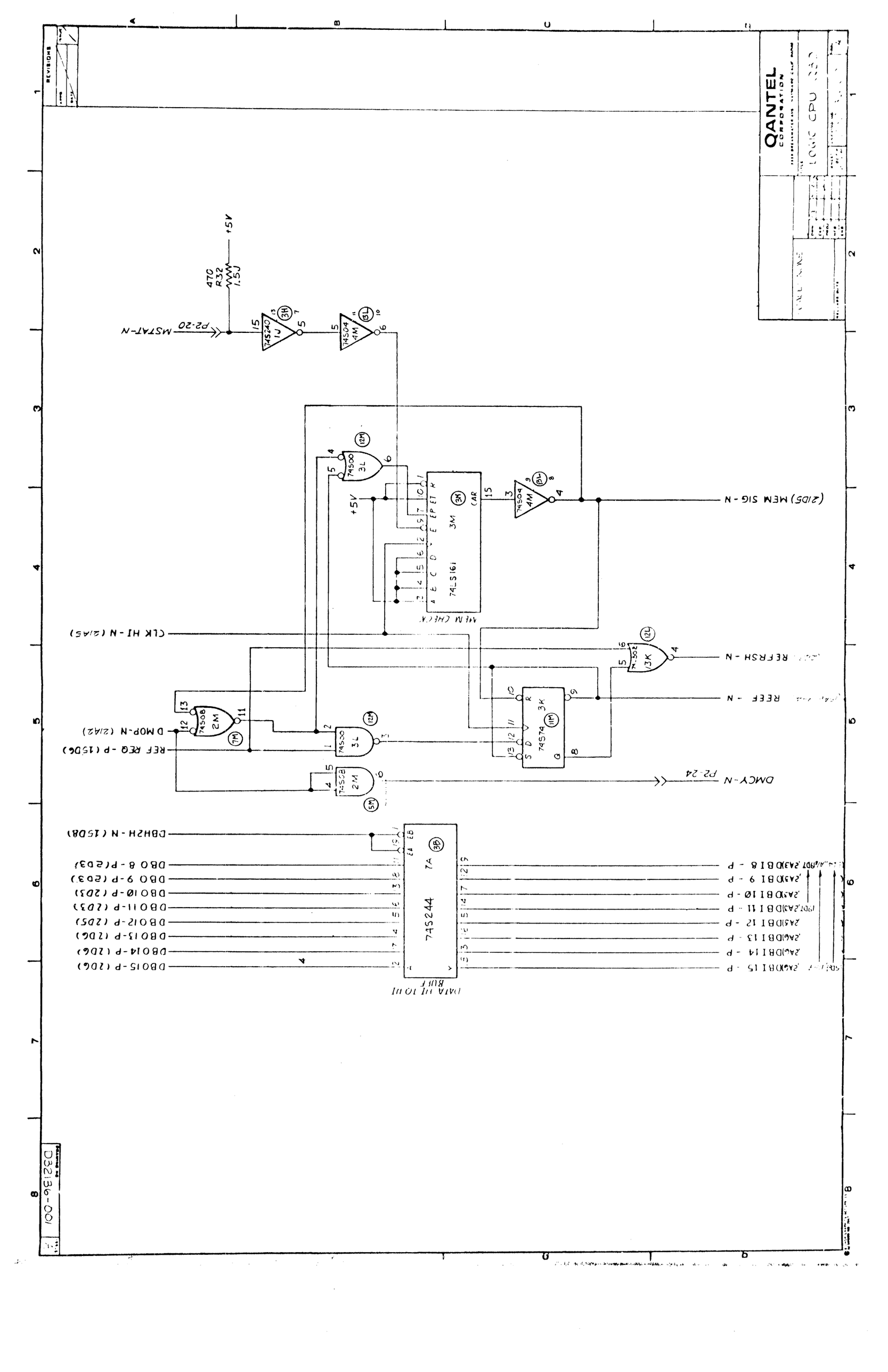
INPUT BUS CONTROL;
CLOCK & REFRESH GENERATION

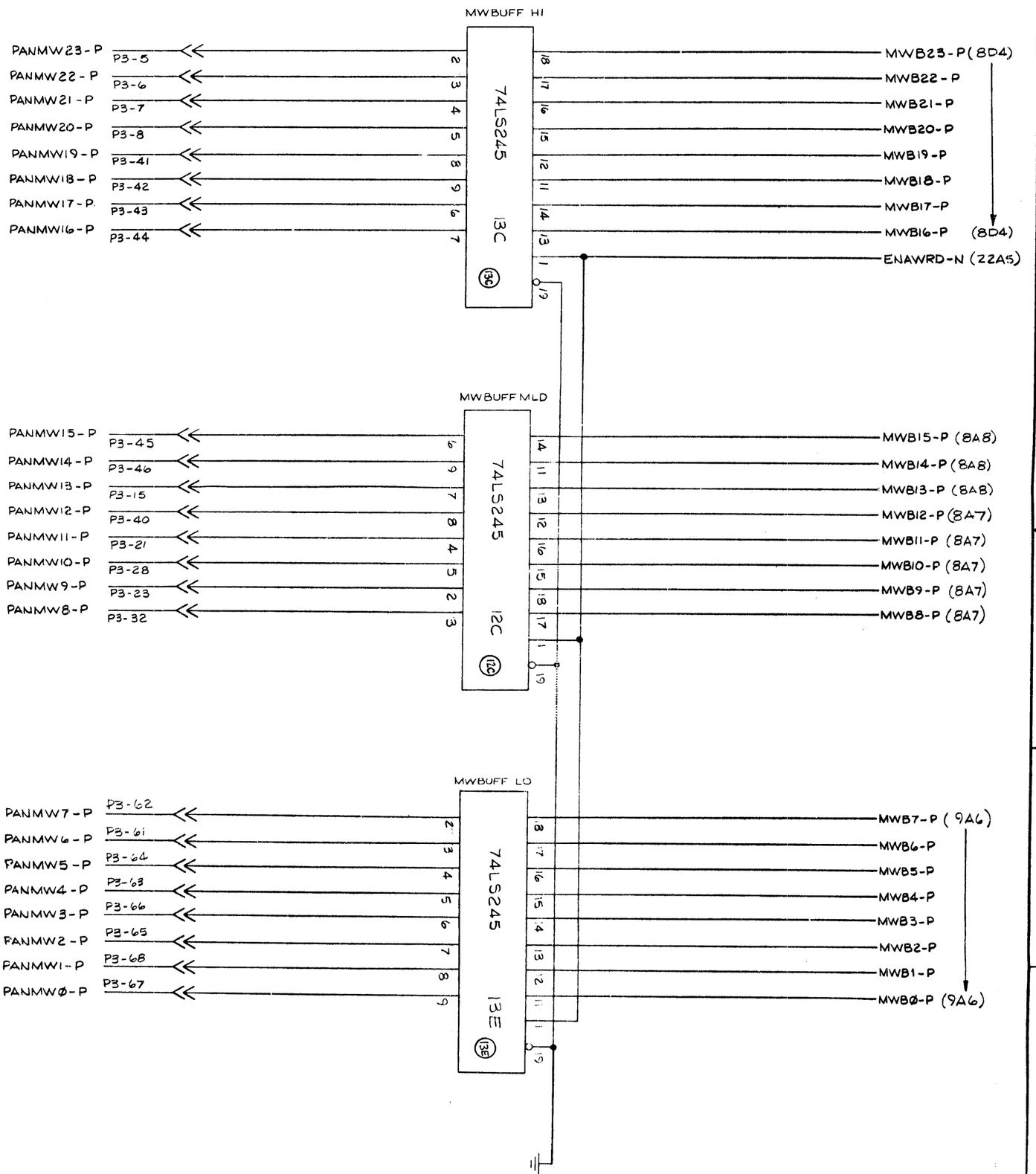
SCALE: NONE

QANTEL CORPORATION

LOGIC, CPU Q30

SHEET 15 OF 22 DRAWING NO. D32136-001 REV. A


QANTEL
CORPORATION
LOGIC CPU
REVISIONS
+5V
470
R32
1.5J
MSTAT-N
P2-20
74S240
1J
74S04
4M
74S00
3L
74S161
3M
MEM CHECK
MEM SIG - N (21D5)
CLK HI - N (21A5)
74S02
13K
REFRSH - N
REF - N
74S74
3K
74S08
2M
DMOP-N (21A2)
REF REQ - P (15D6)
DMCY-N
P2-24
DBH2H - N (15D8)
74S244
7A
DATA IN TO MI BUF
DB0 8 - P (2D3)
DB0 9 - P (2D3)
DB0 10 - P (2D3)
DB0 11 - P (2D3)
DB0 12 - P (2D5)
DB0 13 - P (2D6)
DB0 14 - P (2D6)
DB0 15 - P (2D6)
D3213-001



SIZE D	DWG NO. 32136-001	REV A
SCALE NONE	SHEET 17 OF 22	

D32136-001

REVISIONS

REFREQ-P(15D6)

REEF-N (16D5)
SUM13-P (20D6)
SUM12-P (20D6)
SUM13-P (20D6)
SUM12-P (20D6)

BR11-P (20D5)
BR10-P
BR9-P
BR8-P (20D5)
MAR10-P (5D8)
MAR9-P (5D8)
MAR8-P (5D8)
ADDCNX-P(18D3)
PUP 21B5

BR7-P(20D4)
BR6-P
BR5-P
BR4-P (20D4)
MAR7-P (5D7)
MAR6-P
MAR5-P
MAR4-P
PUP 21B5

BR3-P (20D3)
BR2-P
BR1-P
BR0-P (20D3)
MAR3-P(5D7)
MAR2-P(5D7)
MAR1-P(5D7)
MAR0-P(5D7)

GADD 4-N(20D7)
PADD 4-N(20D7)
GADD3-N (20D5)
PADD3-N (20D5)

DMOP2-N (20A5)
DMOP-P (21A1)

+5V

ØV

REF CTRI
74LS161 5H (4M)

REF CTR Ø
74LS161 4H (3M)
D C B A CLK L EP ET R
QD QC QB QA CAR

ADD 2
74S381 3F (1E)
B3 B2 B1 B0 A3 A2 A1 A0 CIN
COU F3 F2 F1 F0 G P

ADD 1
74S381 2F (2M)

ADD Ø
74S283 1F (1K)

74S74 3K (11M)
S D CLK R Q

74S00 3J (4L)

REF BUFF
74S244 3H (3L)

HI ADDR BUFF
74S244 2H (1F)

LO ADDR BUFF
74S244 1H (1L)
A Y EA EB

74S182 5K (1M)
G1 P1 G0 P0 CN G3 P3 G2 P2
Cntx Cnty Cntz

470
+5V
R20
3.5H

RF-N P2-16

(6A3, 9A4) SMP CLK-P

ADDR 15/7-P P1-49
ADDR14/6-P P2-6
ADDR13/5-P P2-7
ADDR12/4-P P2-8
ADDR11/3-P P2-9
ADDR 10/2-P P2-10
ADDR 9/1-P P2-11
ADDR 8/Ø-P P2-12

(18A5) ADDCNX-P
(20A5) ADDCNY-P
(20A7) ADDCNZ-P

MEMORY INDEX & MUX CONTROL

QANTEL CORPORATION
3120 BREAKWATER AVE · HAYWARD CALIF 94545

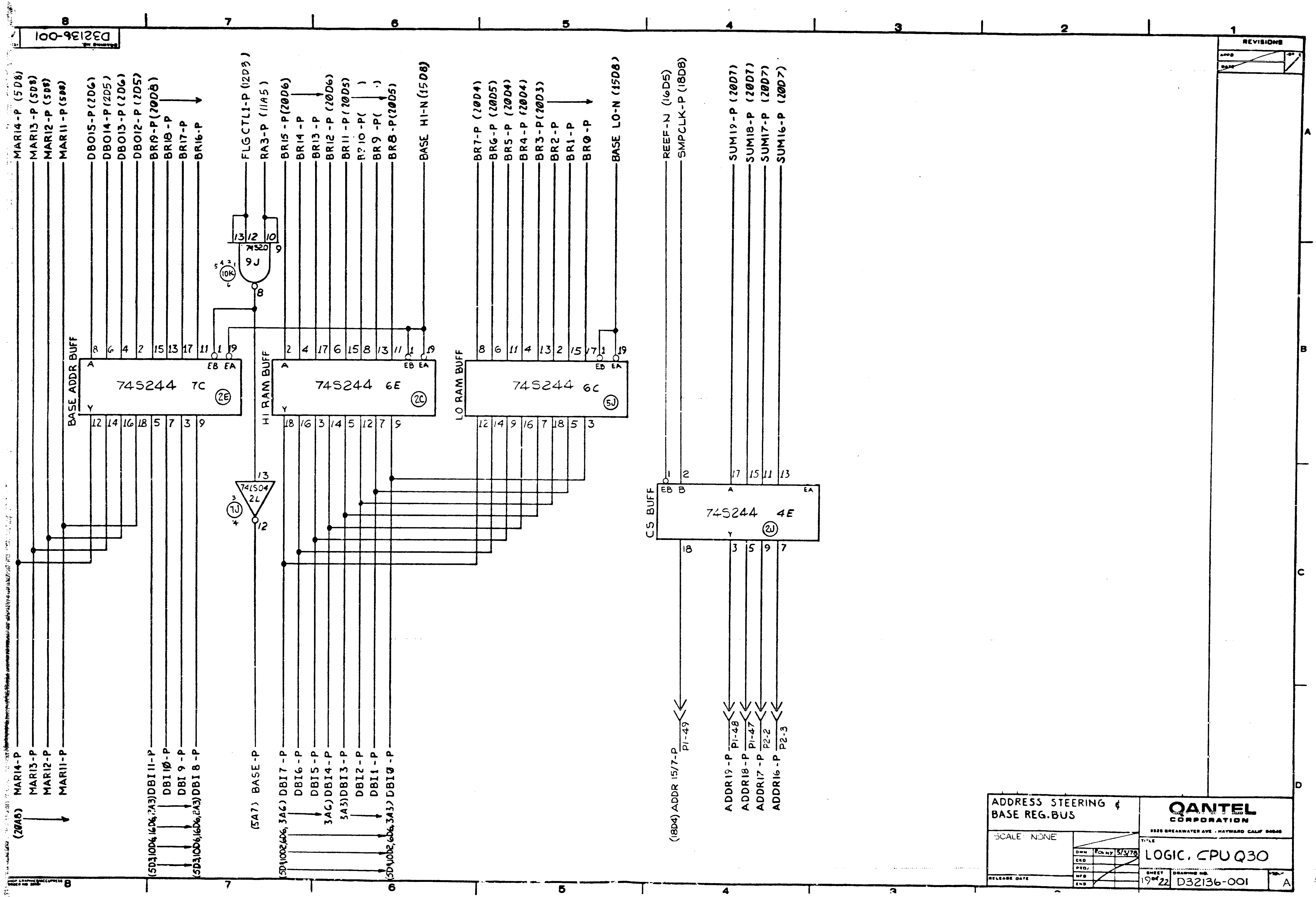
SCALE: NONE

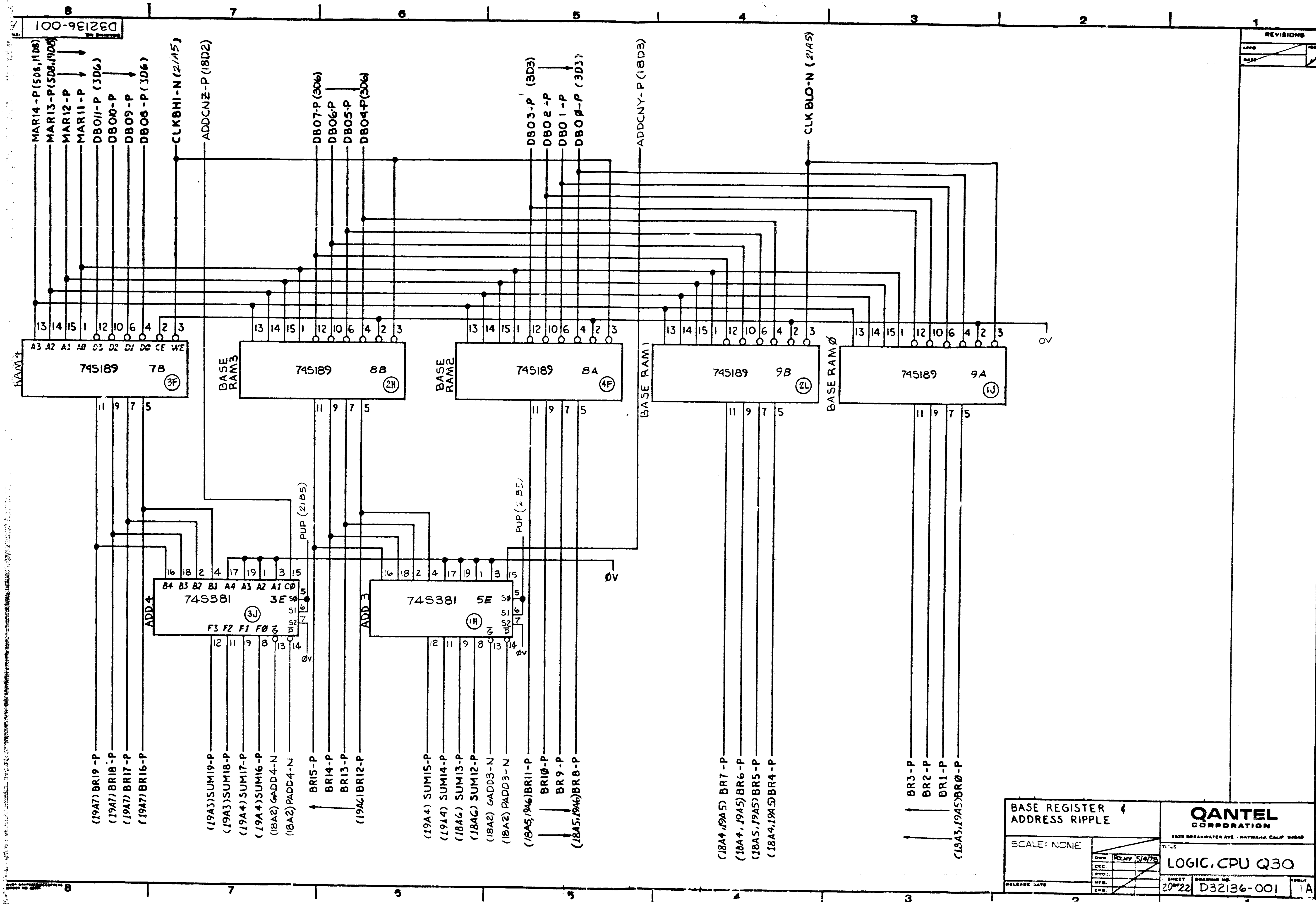
DWN ROW 6/78
CHK
PROJ
MFG
ENG

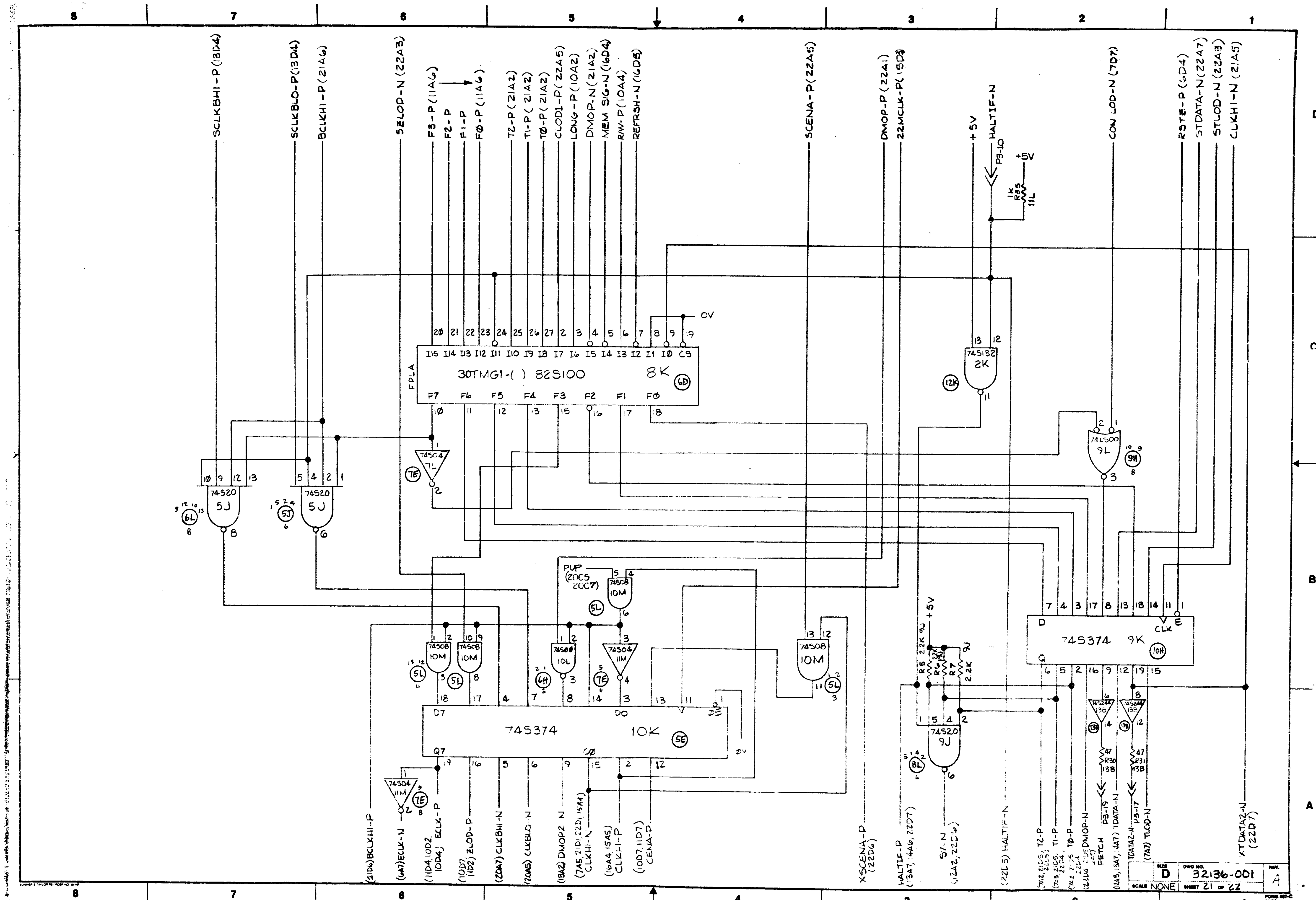
RELEASE DATE

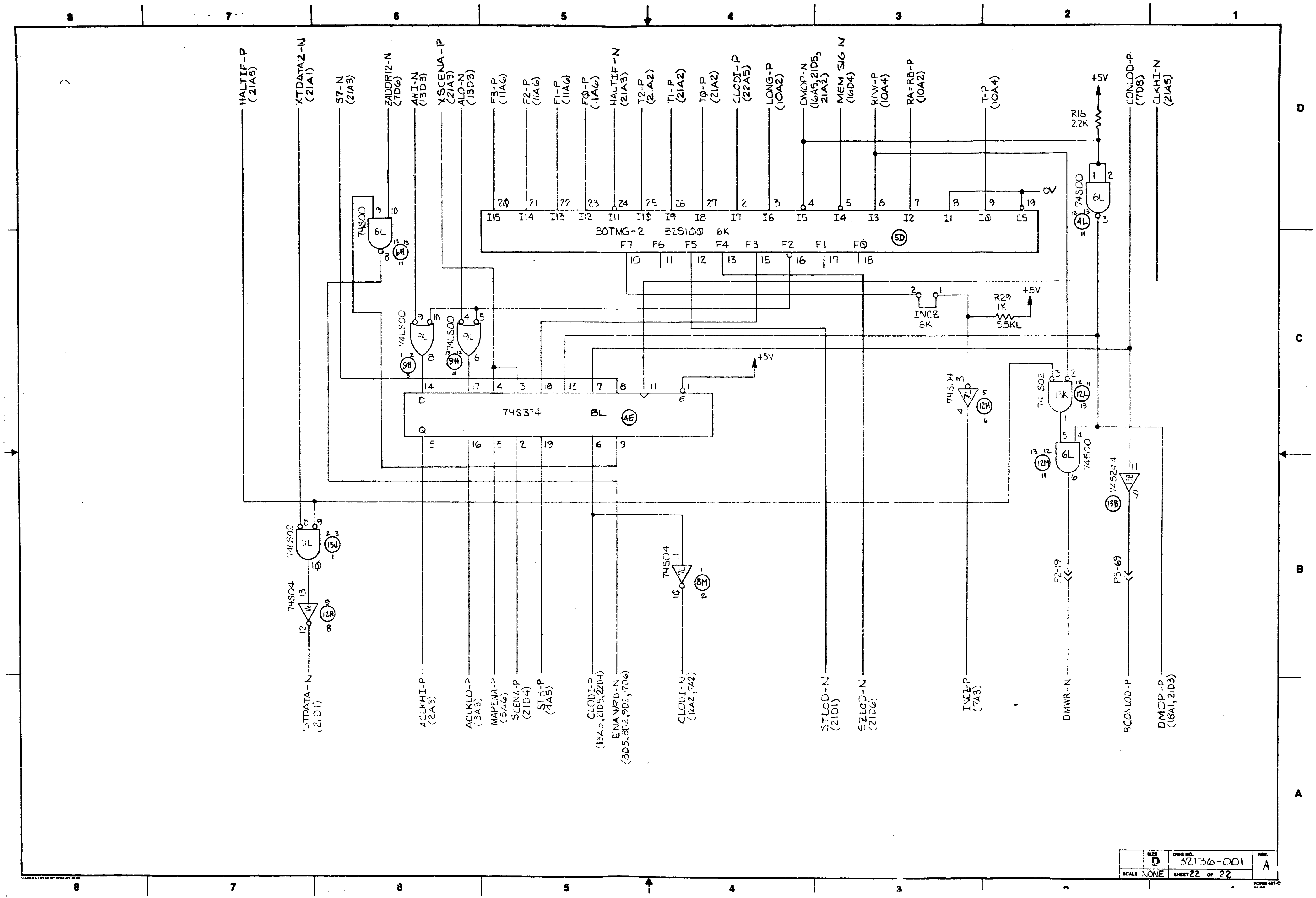
TITLE: LOGIC, CPU Q30

SHEET 18 OF 22 | DRAWING NO. D32136-001 | ISSUE A


D32136-001
REVISIONS
MAR14-P (5D8)
MAR13-P (5D8)
MAR12-P (5D8)
MAR11-P (5D8)
DBO15-P (2D6)
DBO14-P (2D5)
DBO13-P (2D6)
DBO12-P (2D5)
BR19-P (20D8)
BR18-P
BR17-P
BR16-P
FLGCTL1-P (12D3)
RA3-P (11A5)
BR15-P (20D6)
BR14-P
BR13-P
BR12-P (20D6)
BR11-P (20D5)
BR9-P
BR8-P (20D5)
BASE HI-N (15D8)
BR7-P (20D4)
BR6-P (20D5)
BR5-P (20D4)
BR4-P (20D4)
BR3-P (20D3)
BR2-P
BR1-P
BRØ-P
BASE LO-N (15D8)
REEF-N (16D5)
SMPCLK-P (18D8)
SUM19-P (20D7)
SUM18-P (20D7)
SUM17-P (20D7)
SUM16-P (20D7)
74S20
9J
10K
BASE ADDR BUFF
74S244 7C
2E
HI RAM BUFF
74S244 6E
2C
LO RAM BUFF
74S244 6C
5J
74LS04
2L
7J
CS BUFF
74S244 4E
2J
P1-49
P1-48
P1-47
P2-2
P2-3
MAR14-P
MAR13-P
MAR12-P
MAR11-P
(20A8)
(5D3,10D6,16D6,2A3) DBI 11-P
DBI 1Ø-P
DBI 9-P
(5D3,10D6,16D6,2A3) DBI 8-P
(5A7) BASE-P
(5D,10D2,6D6,3A6) DBI7-P
DBI6-P
DBI5-P
3A6) DBI4-P
3A3) DBI3-P
DBI2-P
DBI1-P
(5D,10D2,6D6,3A3) DBIØ-P
(18D4) ADDR 15/7-P
ADDR19-P
ADDR18-P
ADDR17-P
ADDR16-P
ADDRESS STEERING &
BASE REG. BUS
SCALE: NONE
QANTEL CORPORATION
LOGIC, CPU Q30
SHEET 19 of 22
D32136-001
A

 D32136-001
MAR14-P (5D8,19D8)
MAR13-P (5D8,19D8)
MAR12-P
MAR11-P
DBO11-P (3D6)
DBO10-P
DBO9-P
DBO8-P (3D6)
CLKBHI-N (21A5)
ADDCNZ-P (18D2)
DBO7-P (3D6)
DBO6-P
DBO5-P
DBO4-P (3D6)
DBO3-P (3D3)
DBO2-P
DBO1-P
DBOØ-P (3D3)
ADDCNY-P (18D3)
CLKBLO-N (21A5)
RAM 4
74S189 7B (3F)
BASE RAM3
74S189 8B (2H)
BASE RAM2
74S189 8A (4F)
BASE RAM 1
74S189 9B (2L)
BASE RAM Ø
74S189 9A (1J)
0V
PUP (21B5)
PUP (21B5)
ØV
ADD 4
74S381 3E (3J)
ADD 3
74S381 5E (1H)
(19A7) BR19-P
(19A7) BR18-P
(19A7) BR17-P
(19A7) BR16-P
(19A3) SUM19-P
(19A3) SUM18-P
(19A4) SUM17-P
(19A4) SUM16-P
(18A2) GADD4-N
(18A2) PADD4-N
BR15-P
BR14-P
BR13-P
(19A6) BR12-P
(19A4) SUM15-P
(19A4) SUM14-P
(18A6) SUM13-P
(18A6) SUM12-P
(18A2) GADD3-N
(18A2) PADD3-N
(18A5,19A6) BR11-P
BRIØ-P
BR9-P
(18A5,19A6) BR8-P
(18A4,19A5) BR7-P
(18A4,19A5) BR6-P
(18A5,19A5) BR5-P
(18A4,19A5) BR4-P
BR3-P
BR2-P
BR1-P
(19A3,19A5) BRØ-P
REVISIONS
BASE REGISTER & ADDRESS RIPPLE
SCALE: NONE
QANTEL CORPORATION
LOGIC, CPU Q30
5/4/78
SHEET 20 OF 22
D32136-001
A


SCLKBHI-P (13D4)
SCLKBLO-P (13D4)
BCLKHI-P (21A6)
5ZLOD-N (22A3)
F3-P (11A6)
F2-P
F1-P
FØ-P (11A6)
T2-P (21A2)
T1-P (21A2)
TØ-P (21A2)
CLOD1-P (22A5)
LONG-P (10A2)
DMOP-N (21A2)
MEM SIG-N (16D4)
RW-P (10A4)
REFRSH-N (16D5)
SCENA-P (22A5)
DMOP-P (22A1)
22MCLK-P (15D2)
+5V
HALTIF-N
P3-10
+5V
1K R35 11L
CON LOD-N (7D7)
RSTE-P (6D4)
STDATA-N (22A7)
STLOD-N (22A3)
CLKHI-N (21A5)
OV
FPLA
30TMG1-( ) 82S100
8K
6D
74S132
2K
12K
74LS00
9L
9H
74S04
7L
7E
74S20
5J
6L
5J
PUP
(20C5
20C7)
74S08
10M
5L
74S08
10M
74S08
10M
74S08
10L
6H
74S04
11M
7E
74S08
10M
5L
74S374
10K
5E
74S374
9K
10H
CLK
74S20
9J
8L
74S244
13B
74S244
13B
R30 13B
R31 13B
R5 R6 R7
2.2K
74S04
11M
7E
(21D6) BCLKHI-P
(6A7) ECLK-N
(11D4, 10D2, 10D4) ECLK-P
(10D7, 11D2) ZLOD-P
(20A7) CLKBHI-N
(20A5) CLKBLO-N
(18A2) DMOP2-N
(7A5, 21D1, 15A4) CLKHI-N
(16A4, 15A5) CLKHI-P
(10D7, 11D7) CENA-P
XSCENA-P (22D6)
HALTIF-P (13A7, 14A6, 22D7)
S7-N (12A2, 22C6)
(22C5) HALTIF-N
T2-P
T1-P
TØ-P
DMOP-N
FETCH
P3-19
TDATA-N
P3-17
TDATA2-N
(7A7) TLOD-N
XTDATA2-N (22D7)
SIZE D
DWG NO. 32136-001
REV. A
SCALE NONE
SHEET 21 OF 22


HALTIF-P (21A3)
XTDATA2-N (21A1)
S7-N (21A3)
ZADDR12-N (7D6)
AHI-N (13D3)
XSCENA-P (21A3)
ALO-N (13D3)
F3-P (11A6)
F2-P (11A6)
F1-P (11A6)
FØ-P (11A6)
HALTIF-N (21A3)
T2-P (21A2)
T1-P (21A2)
TØ-P (21A2)
CLODI-P (22A5)
LONG-P (10A2)
DMOP-N (16A5,21D5, 21A2)
MEM SIG N (16D4)
R/W-P (10A4)
RA=RB-P (10A2)
T-P (10A4)
+5V
R16 2.2K
CONLOD-P (7D8)
CLKHI-N (21A5)
OV
5OTMG-2 82S100 6K
74S374 8L
INC2 6K
R29 1K 5.5KL
STDATA-N (21D1)
ACLKHI-P (2A3)
ACLKLO-P (3A3)
MAPENA-P (5A6)
SCENA-P (21D4)
STB-P (4A5)
CLODI-P (13A3,21D5,22D4)
ENAWRD-N (8D5,8D2,9D2,17D6)
CLOUI-N (1A2,7A2)
STLOD-N (21D1)
SZLOD-N (21D6)
INC2-P (7A3)
P2-19
P3-69
DMWR-N
BCONLOD-P
DMOP-P (18A1,21D3)
SIZE D
DWG NO. 321316-001
REV. A
SCALE NONE
SHEET 22 OF 22