MEMORANDUM

DATE: AUGUST 8, 1985

SUBJECT: HIGH PERFORMANCE DISK DRIVES

FROM: S. BLIGHTMAN

TO: D. SMITH

CC: A. ABBOTT, J. CARROLL, T. FRANEY, C. KARZAG, S. VINELLA, H. WALLACE

With the coming of the S114, and probably future controllers supporting 3 megabytes/second, the subject of how we test these is going to become more of an issue. I don't know how expensive the new drives are going to be but I suspect the price will be substantial.

I noticed that you budgeted three new Fujitsu 2333 drives at a cost of $6,000.00 each for the testing of our 2.5 megabytes/second controllers. I suspect that you have already purchased the first one, but I suggest that we talk about a solution that may save us having to buy one or both of the other drives and also solve the 3 megabytes/second problem at the same time.

I suggest we look at designing and building a disk emulator in the vein of the Tapeworm. It would seem to me that the disk emulator would be a very simple project and could be done with no intelligence in the architecture. I imagine using a 64K or 128K byte buffer to emulate maybe two cylinders of two tracks each. The memory could be accessed byte wide and the data passed through a serializer/deserializer for conversion to the SMD interface. The high order address bits would be driven by the cylinder and head registers, and the low order bits supplied by a free running counter to simulate a rotating disk. Refresh could be performed on sector boundaries while transmitting the sector pulse. In order to test the high order bits of the SMD bus, we may have to play some games but I think that can be done too.

In order to support the ECL drivers and receivers for the enhanced SMD interface, we would have to include both a +5V and a -5V supply. However, since it would not have any intelligence, I think the cost of this device should be no more than the Tapeworm.

Providing we all agree this is a sensible thing to do, and since, as you know, Engineering resource is in high demand at the moment, I wondered whether you may have someone who might like to do this. Engineering would, of course, be willing to supply some guidance in this project.

Let me know what you think.

/rhs

1-20-87

Rework For 503 Emulator Proto Build
W/O # 5003A00-0007 (5 boards)

The following is a list of additional and replacement parts required to rework 5 boards:

P/N	Description	Qty
1400019	Res, 20KΩ	10
1800005	Cap, 6.8 μF	10
3100008	Socket, 14P, DIP	10
2000006	Header, 26P	10

SPECTRA LOGIC

ENGINEERING CHANGE ORDER

Form 4-8600003, 9/84

REWORK DELETIONS For W/O #5003A00-0007 ONLY

Page 2 of 3

ECO # N/A

No.	From ...	To	Notes
1	3J-5	cut trace	component side
2	3J-9	cut trace	solder side
3	@ R1	Remove Part	
4	@ R2	↓	
5	@ C3	↓	
6	@ C7	↓	

SPECTRA LOGIC

ENGINEERING CHANGE ORDER

Form 3-8600004, 9/84

REWORK ADDITIONS For w/o #5003A00-0007 ONLY | Page 3 of 3 | ECO # NA

No.	From	To	Notes
1	3R-7	3S-7	
2	3R-14	4R-14	
3	5R-7	5S-7	
4	5R-14	5P-16	
5	4M-6	4M-1	
6	4M-7	2K-7	
7	1D-9	6M-13	
8	7J-11	6N-1	
9	6N-2	6M-12	
10	6N-11	3J-5	
11	4N-11	CR4-2(-)	connect to feed thru directly above square pad on CR4
12	4N-9	3J-9	
13	4N-19	4P-10	
14	6M-7	6M-8	connect IC pin 7 to ground via
15	@ R1	Add component	20K (14-19)
16	@ R2		
17	@ C3		6.8 uF (18-05)
18	@ C7		
19	@ 3R		14 Pin Dip socket (31-08)
20	@ 5R		Remove pins 2-6 and 9-13
21	@ DS1-DS5		26 Pin Header (32-06)
22	@ DS9-DS16	V	cut to size — NOTE: Headers to be installed on solder side

TAPE WORM MOD (for S34)

Remove wire from 12A-11 to 4A-13

Add 1K SIP - Pin 1 to 14E-20
74LS08 + socket to location 1C

Change PROMs in 2B, 4B, 4C, 7B, 9B to revision A2.

Add wire

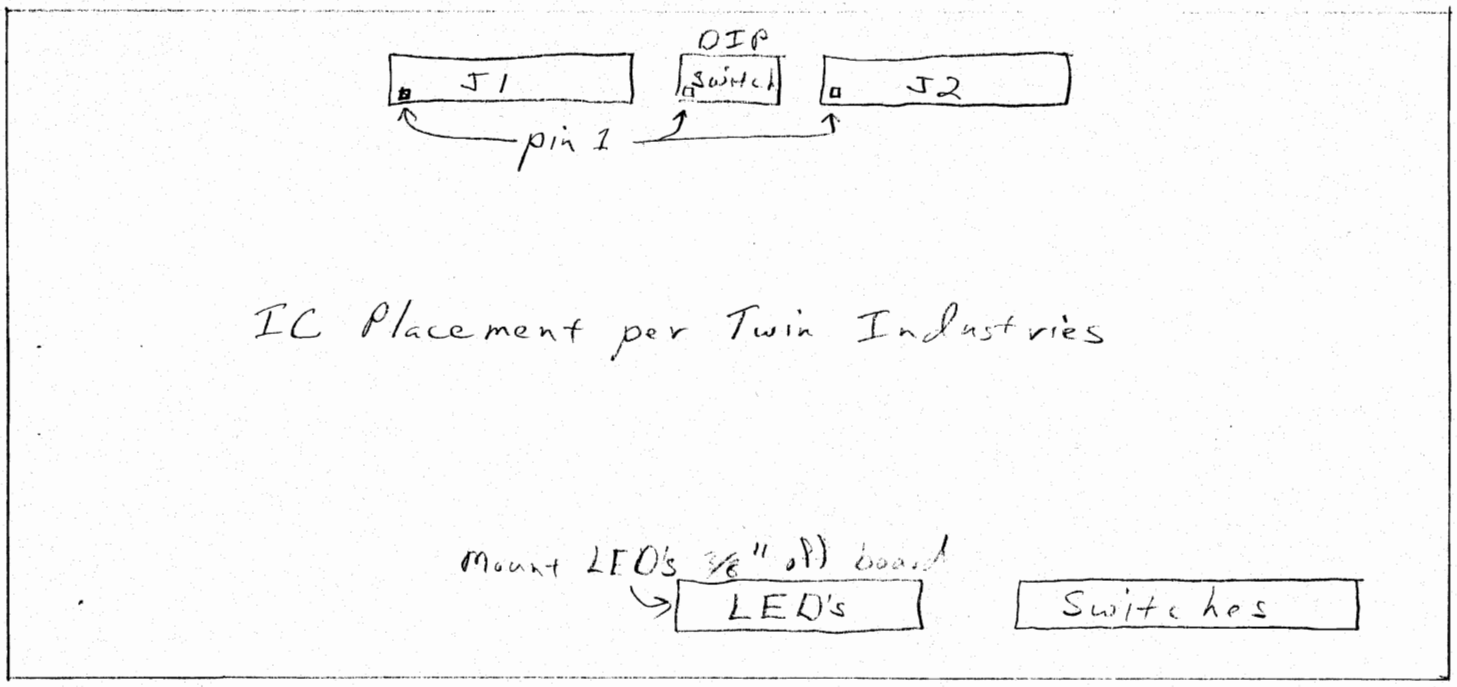
12A-11	to 1C-2
2A-6	1C-1
1C-3	4A-13
CERSW-2	GND
CERSW-3	4E-19
14E-19	16F-10
16A-9	16A-12
16A-12	10F-14
16A-8	22C-11
22C-10	J2-42
HERSW-2	GND
HERSW-3	14E-18
14E-18	16A-13
16A-11	22C-13
22C-12	7A-4
J2-26	J2-40

Switch on front panel that was Transport Address 3 is now PARITY ERR

Switch contact 2 is tied to ground, as it was.
Switch contact 3 is connected to 22C-6.

Tape worm Switch, LED & Header Placement
2-22-85 DLS

2 4
1 3



ERROR LOG

(1)
3A	pin	1
20B	↕	10
9C	↕	16
10C	↕	16
17B	pin	2
18B	pin	2
19B	↕	2
7B	↕	24
9B	↕	24
4D	pin	10
12D	pin	10
14D	pin	10
20D	pin	40
13A	↕	14
8C	↕	14
3A	pin	11

CONNECT TO 5V ↑
(Nearest)

(2).
2B	pin	12
4B	↕	12
7B	pin	12
9B	pin	12
4C	pin	12
17B	pin	8
18B	↕	8
19B	↕	8
9A	pin	1, 19
10A	pin	1, 19
2D	pin	30
4D	pin	30
14D	↕	30

↑ CONNECT TO Gnd
(Nearest)

(3). ~~3A pin 16 cut trace~~
~~CONNECT TO Gnd~~
Delete

(4) 2C pin 11 CONNECT TO 19B pin 1

(5) 2C pin 1 CONNECT TO 12A pin 6

⑥ 2A is wrong Socket (See Corrections to wire list)

⑦ 12D pin 20 is wrong should go to pin 30
pin 20 is CONNECT To G (See Corrections to wire List)

⑧ 14A pin 13 missing Wiring to 22A pin 5

ERROR Log S/B

① 3A pin 1 ✓ 3A-1 to 3A Pin 20
20B pin 1 ✓ 20B-1 to 20B-20
9C pin 16 ✓ 7C-16 → 9C-16
10C pin 16 ✓ 9C-16 → 10C-16
17B pin 2 ✓ 20B-20 → 19C-2
18B pin 2 ✓ 19B-2 → 18C-2
19B pin 2 ✓ 18C-2 → 17C-2
7B pin 24 ✓ 2B-24 → 7B-24
9B pin 24 ✓ 4B-24 9B-24 should apply 5 V

② 2B pin 12 ✓
4B pin 12 ✓
7B pin 12 ✓
9B pin 12 ✓
4C pin 12 should connect to Ground

③ 2A Wrong Socket (AND Wiring is Wrong in the back)
+ pin 8 → GND

④ Sip Socket Pwr & Gnd

SØ3 Master Diskette

The SØ3 Master Diskette contains the following files : -

SØ3P1.SCH - SØ3P1Ø.SCH
: These files are the PCAD schematic files for each of the 1Ø pages.

SØ3P1.PLT - SØ3P1Ø.PLT
: These files are the PCAD plot files for each of the 1Ø pages in HP format.

SØ3PANEL.SCH
: This file is the PCAD schematic file for the front panel.

SØ3PANEL.PLT
: This file is the PCAD plot file for the front panel in HP format.

SØ3A.REW
: This file contains the rework instructions for revision A of the artwork of the SØ3 PCB.

SØ3.BOM
: This file is the Bill of Material file generated by running the PCNETS extract program on the 1Ø schematic sheets.

SØ3.TEL
: This file is the package and net list file generated for the TELESIS system by running the PCNETS extract program on the 1Ø schematic sheets.

SØ3.MAN
: This file is the manual describing the product. It has been generated using WORDSTAR and must be printed using WORDSTAR.

SØ3_2EAØ.PAL, SØ3_2KAØ.PAL, SØ3_2VAØ.PAL, SØ3_2WAØ.PAL
: These files are the PALASM source files for the 4 PALs.

SØ3_2EAØ.PIN, SØ3_2KAØ.PIN, SØ3_2VAØ.PIN, SØ3_2WAØ.PIN
: These files are the pin files generated by PALASM for the 4 PALs.

SØ3_2EAØ.JED, SØ3_2KAØ.JED, SØ3_2VAØ.JED, SØ3_2WAØ.JED
: These files are the JEDEC files generated by PALASM for the 4 PALs. They can be downloaded directly to the DATAIO programmer to blow the fuses in the 4 PALs. If transfered to the PDP11 first, the files must be transfered using XMODEM since the files contain special control characters.

SØ3_2XAØ.PLE, SØ3_6ZAØ.PLE
: These files are the PLEASM source files for the two miscellaneous PROMs.

SØ3_2XAØ.HEX, SØ3_6ZAØ.HEX
: These files are the HEX format files generated by PLEASM for the two PROMs. They can be downloaded directly to the DATAIO programmer to blow the fuses in the two PROMs.

SØ3TAØ.MAC
: This file is the source for the firmware of the tape emulator. This source may be used by the meta-assembler on the PDP11.

SØ3TAØ.LST
: This file is the list file of the firmware of the tape emulator. It is generated by running the meta-assembler on the PDP11.

SØ3TDEF.MAC
: This file is the definition source file for the tape emulator.

SØ3TDEF.LST
: This file is the list file of the firmware definitions of the tape emulator. It is generated by running the meta-assembler on the PDP11.

SØ3TAØ.PRM
: This file is the PROM object file generated by running the meta-assembler on the PDP11. It can be used by the DATAIO program to download the PROM information for the tape emulator to the DATAIO programmer.

READ.ME
: This file.