VM-8851 Graphics Processor Manual

PRELIMINARY

VMI

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1 - Introduction

The VM-8851 Graphics Processor delivers next-generation graphics on a single MULTIBUS compatible board. The Intel 8088 CPU, operating at 8 MHz with up to 200 Mbytes local memory and up to two Mbytes image memory, provides considerable flexibilty in complex applications requiring highly independent graphics processing. For less complex applications, 8088-based applications code installed directly onto the single-board system provides the basis for stand-alone system capability. The graphics processor generates displays of up to 256 simultaneous colors chosen from a 4096 color palette. Flexible image RAM organization permits the choice of a high-resolution image (up to 1K x 1K) or multiple, image buffers. High-performance features such as 60 Hz refresh rate, pixel pan within a 1K x 1K image space, 128 independent display windows, and hardware zoom offer significant enhancements beyond previous graphics processor implementations. Output consists of RGB video with selectable sync.

The graphics processor provides flexible MULTIBUS interfaces. A 128-byte FIFO buffers MULTIBUS to graphics processor commands and data when in slave mode. Master mode capability permits DMA operation or stand-alone operation. MULTIBUS 24-bit addresses are generated and detected. The functionality of the graphics processor expands by adding expansion modules on the SBX connector.

A high-level, easy-to-use graphics language, INTERACTTM, runs on the graphics processor to provide a user accessible method for generating complex graphics images. INTERACTTM resides in a section of the graphics processor PROM space and responds to high-level commands from the MULTIBUS interface or from on-board applications code.

This manual provides a description of the graphics hardware architecture and operation and firmware design considerations. Section 2 describes the architecture of the graphics processor. Section 3 explains the theory of operation of the hardware. Section 5 covers the board hardware from the programming point of view. This information enables the user to maximize board use for any particular application. Section 5 also includes necessary hardware and software descriptions for debugging user-written 8088 software.

2 - Processor Architecture

2.1 - CPU Local Memory

An 8-MHz 8088 microprocessor running in "MAX mode" forms the basis of the CPU section. The board design of local memory allows various combinations of PROM and RAM. Jumpers supply appropriate connections to flag the board for the current configuration. (Refer to the configuration section to determine the proper jumper placement for signaling the contents of each socket.)

2.2 - Scanner Section

The scanner section supports the hardware ZOOM and PAN functions by producing the proper addresses to scan, though it does not directly address memory. Instead, the RAM address generator latch holds the scanner address during a valid period. This address remains latched until applied to memory at a later time.

Both the scanner and the CPU share the VA and VD buses (for addresses and data respectively). Using these buses the CPU can program the scanner. To achieve this goal, the CPU first gains control of the scanner so that the scanner ceases to send out its own signals. The processor then applies addresses on the VA bus and data on the VD lines to program the scanner.

The scanner and CPU also share 256 bytes of RAM (U39.U40). The scanner, accessing during horizontal retrace, can only read information stored in RAM. The CPU accesses this RAM space during vertical retrace and can perform both read and write functions.

This RAM space contains the starting address table used by the scanner during its operation. Every four raster lines in a display constitutes a group. For each group, the RAM stores a starting address in a table format. These addresses can exist anywhere within a 16-pixel boundary of display RAM. The CPU programs the starting address table to structure the memory and to determine which part of the display to scan out. At every fourth line, the scanner accesses the starting address table during horizontal retrace to determine the starting address for the next group. The scanner reads in the next value then applies the address during visible line time. Between the CPU and the scanner, U38 arbitrates access to the starting address table and the scanner. Refer to figures 2.1 and 2.2.

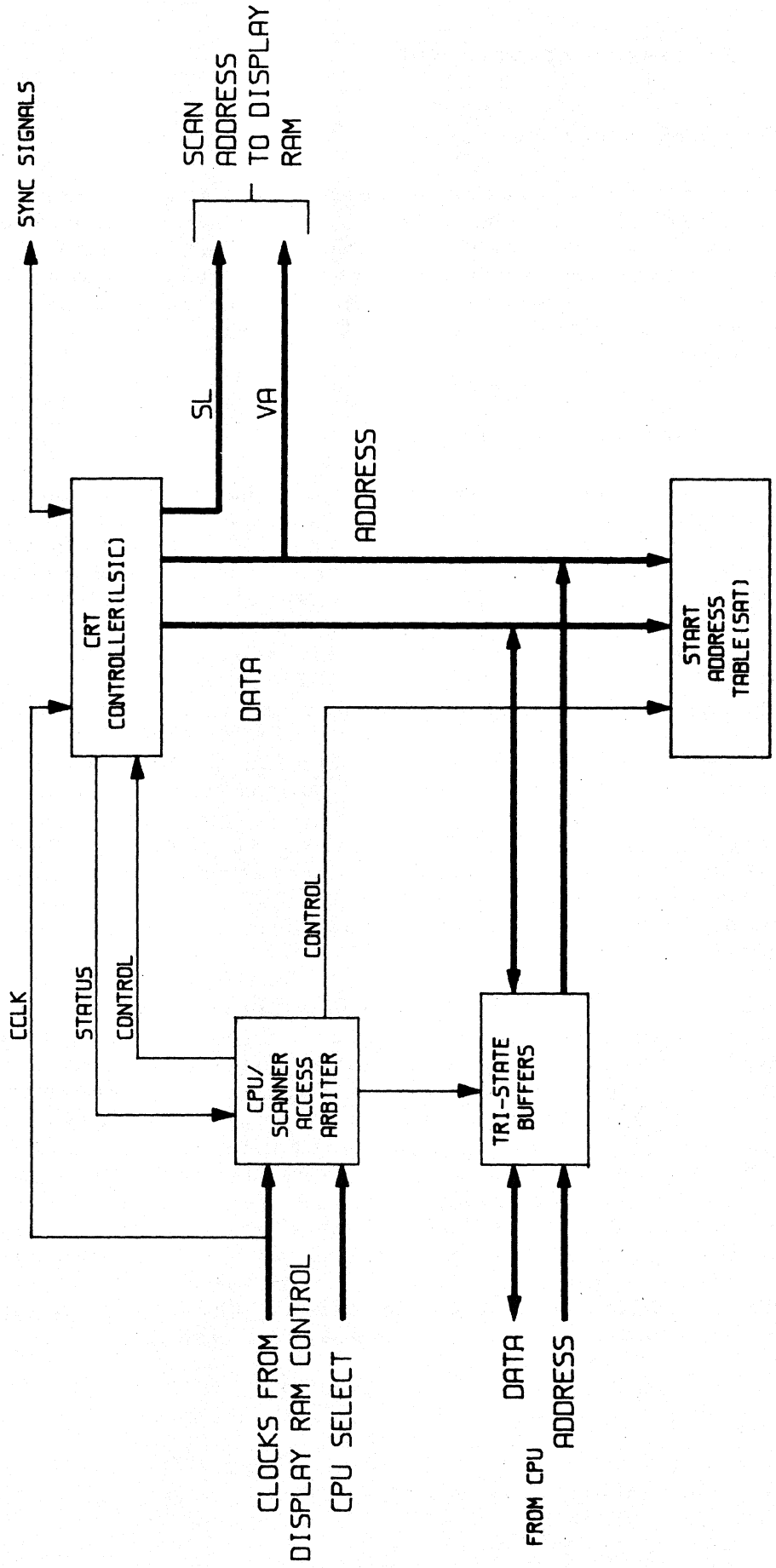


Figure 2.1 : Scanner Section

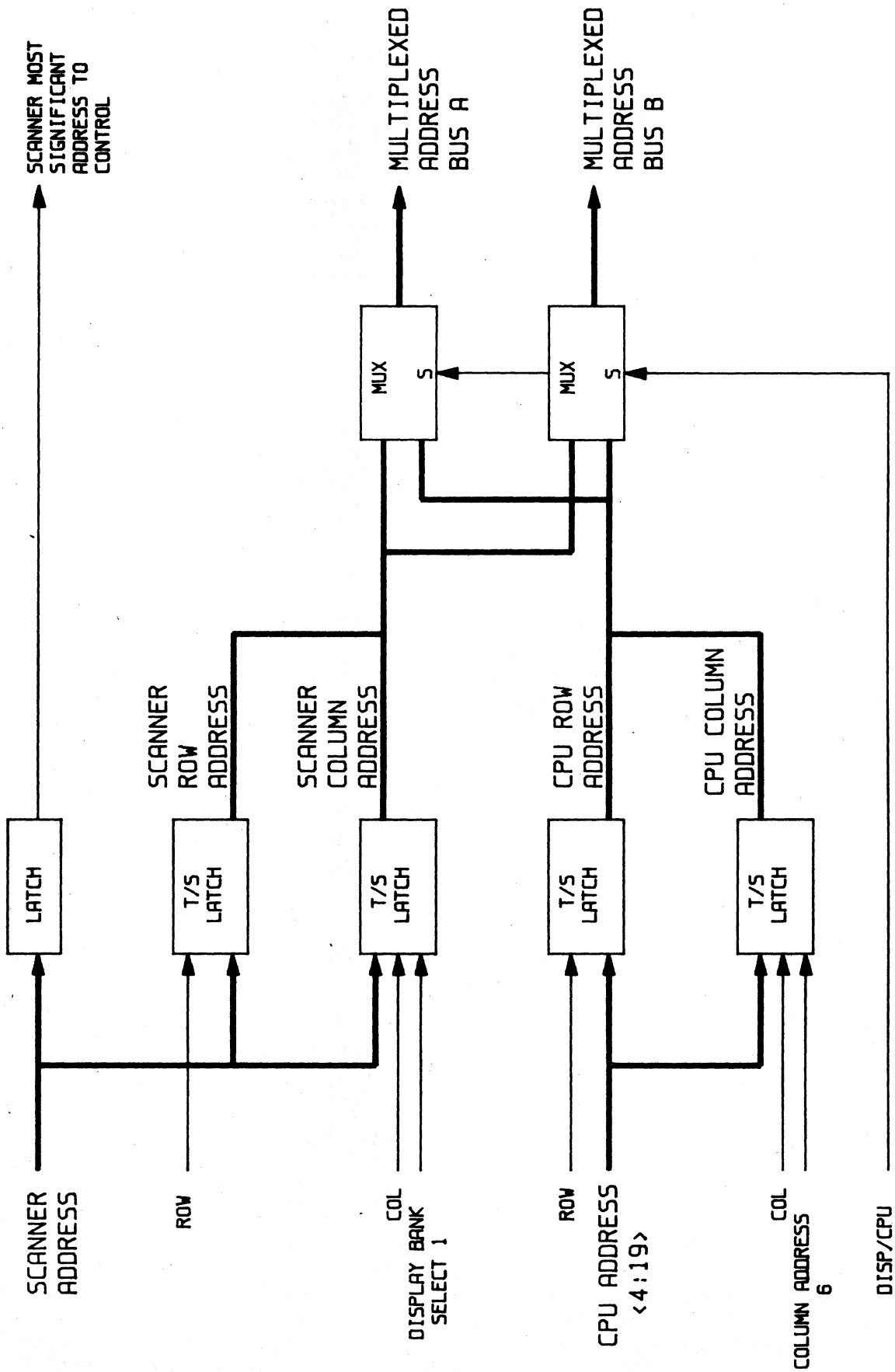


Figure 2.2 : RAM Address Generator

2.3 - MULTIBUS Interface

The VM-8851 supports two standard types of host interface simultaneously. Programmed I/O provides high-speed, bi-directional data transfer between the host and the VM-8851 with an extremely simple interface. DMA operation allows greater system throughput by freeing the host processor for other tasks while the VM-8851 fetches data from system memory. With an optional SBX serial interface, board data can also be transmitted to the VM-8851 from any RS232 compatible device. Refer to figure 2.3 for further information in reading the next sections.

2.3.1 - Programmed I/O

Using an 8-bit-wide data transfer, the programmed I/O section allows the host to communicate through the MULTIBUS to the on-board CPU, an Intel 8088. Signals coming onto the board pass first through the bus receiver, composed of four 64 x 5 FIFOs. This configuration produces a 128 x (8 + 2) bit FIFO used by the host to read status and to send data to the board. The design reserves eight bits for data. The remaining two bits function as signal bits. They identify DMA command data and distinguish those commands from INTERACTTM commands. (Refer to the INTERACTTM Command Language Manual for more information.)

The address decoder consists of a large jumper array. Two 20-pin header sockets lie offset from each other on the board. This design conserves space. These two positions can derive five commonly used addresses: 24-bit, 20-bit, 16-bit, 12-bit, and 8-bit. In all these cases, jumpers select the eight most significant bits which will feed to the address comparator (ALS520). This chip compares the data with the eight bits held in the dip switch to produce the host select signal (HSTSEL). The PAL 20L10 further decodes the signal to determine the action requested.

2.3.2 - DMA Section

The VM-8851 enacts DMA transfers using Master Mode. In the DMA section, the bus arbiter makes all requests of the bus for DMA transactions and handles the priority levels. The bus controller generates I/O signals as determined by the CPU. The CPU initiates a transfer by sending an address. The three address latches hold this value while the CPU sends data to each respective address. The host software determines the block accessed and controls the read/write operations sent to the board. Also through the host software, the latch controls access to memory pages.

When the CPU wants to access certain ranges of addresses, the DMA section interprets these inquiries as off-board requests. It then disables all local devices and converts to Master Mode on the bus. Following this transfer of control, the 8289 produces a

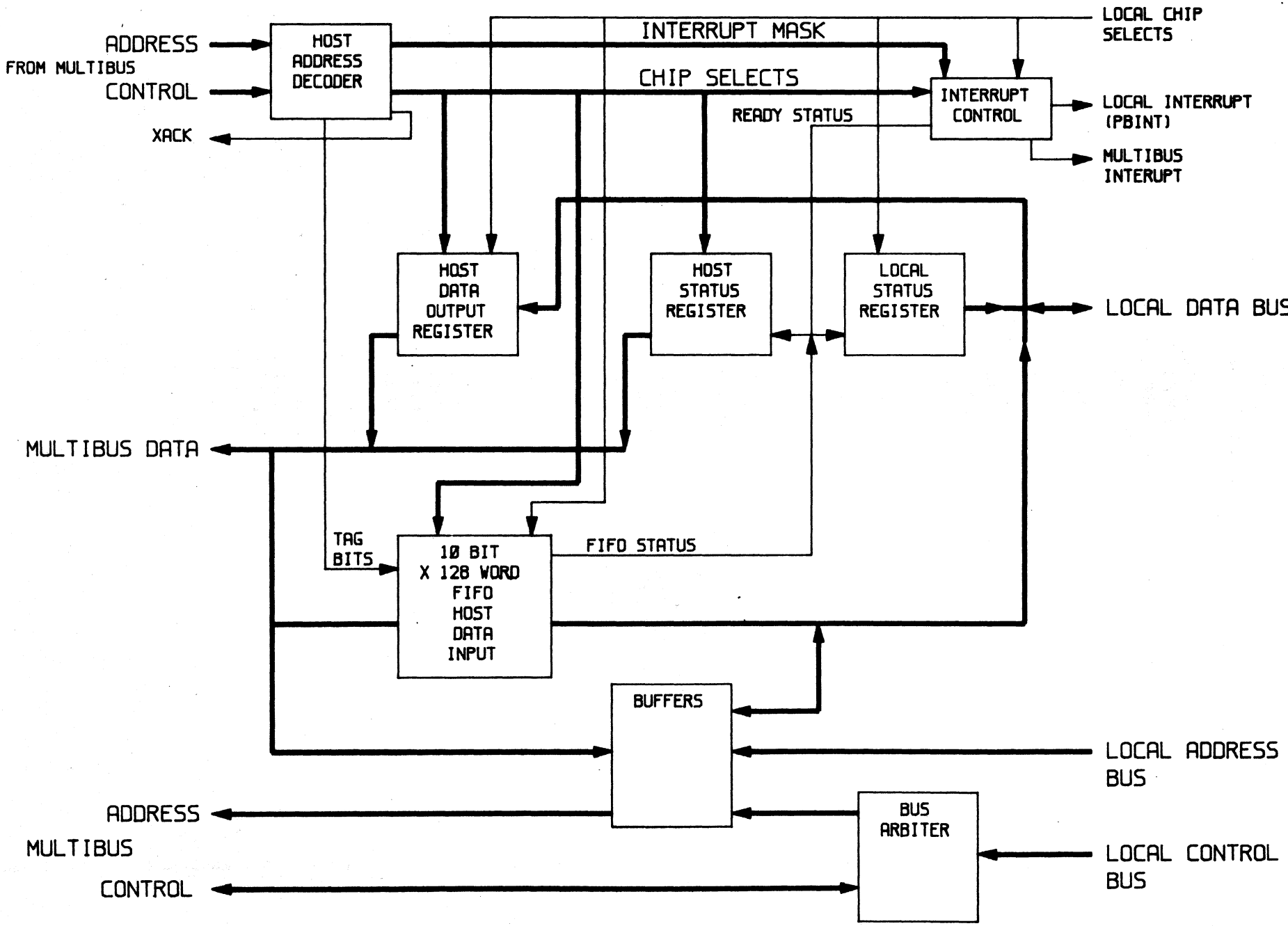


Figure 2.3 : Programmed I/O and Master Mode

bus request signal. On receiving a bus grant it drives the bus using local CPU data and control.

The upper six bits supplied on MULTIBUS drive the latch. The board can then access any of the 16K blocks available. However, to cross a 256K boundary, the CPU must reprogram the latch.

2.4 - Display RAM

This section references figure 2.3. The image is stored in an array of dynamic RAM chips which are densely packed in single-line-packages (SIPs). With standard 64K x 4 devices, the memory may be configured as one of the following:

Number of buffers	X-Dim	Y-Dim	bits/ pixel
2	512	512	8
1	1K	512	8
1	1K	1K	4
2	1K	512	4
4	512	512	4

With optional 256K x 4 devices, the options become

Number of buffers	X-Dim	Y-Dim	bits/ pixel
2	1K	1K	8
4	1K	512	8
8	512	512	8
4	1K	1K	4
8	1K	512	4
16	512	512	4

The memory is organized to produce 16 pixels in each 640 nsec cycle. These pixels are then shifted out to the video output section at a rate of 40 nsec per pixel. The CPU can access the display RAM at any time without disturbing the display output. When the CPU writes to display RAM the address and data are latched briefly to synchronize to the display cycle without making the CPU wait.

Display RAM data output is transformed through a programmable look-up table into binary values which drive video DACs. The design contains four separate look-up tables of 256 x 12 bits. These LUTs may be selected by the CPU to implement an instantaneous transformation of the displayed image. Display modes which use only four bits per pixel have only two selectable llok-up tables. In those configurations, one bit of the scan address drives the look-up table select to distinguish which nibble of the display data should be mapped to output.

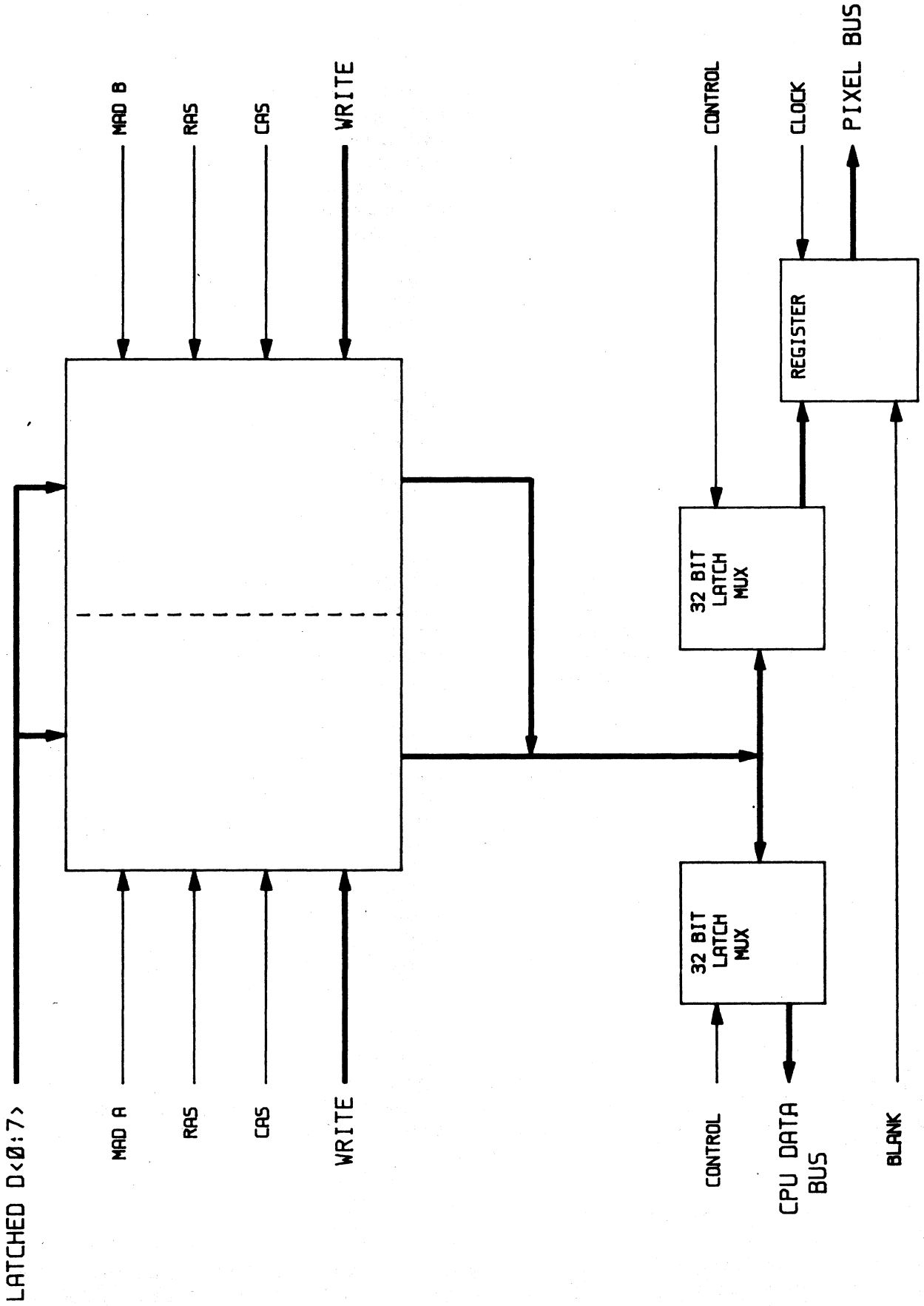


Figure 2.4 : Display RAM

2.5 - Timing and Control

The major structure of the timing and control section is depicted in figures 2.5 and 2.6. The clock generator produces various divisions and phases of the 50 MHz master clock. The dot clock has a frequency of 25 MHz, so video data output is updated every 40 nsec. Another important period is the "character" period, 640 nsec or 16 pixels. This frequency defines the resolution with which the scanner addresses display RAM.

CPU accessible latches drive the major control lines, making many operational choices software-selectable. These options include seven display RAM write modes ranging from one to 16 pixels, pan displacement. blanking, nibble write-protect. bank selection, and look-up table (LUT) selection. System mode selection is also accessible to the CPU and refers to the logical structure of display RAM and the LUT. Many dynamic control signals are directly affected by these software-defined controls.

Much of the timing and control circuitry is implemented in programmable logic (PLA or PAL) due to the complex interrelations of these signals. A programmable logic sequencer generates the display RAM control signals and arbitrates, between the CPU and the scanner, access to the the display RAM. When the CPU writes to display RAM, the address and data are latched so that the CPU can execute further instructions without waiting for the display RAM cycle to complete. This process cannot be done with read cycles, but very few common operations require reading the display RAM.

Selection of individual pixels or groups of pixels from a "character" of 16 pixels is accomplished by a combination of timing and device selection. Timing is essential, because nibble mode operation implies that different addresses are accessible at different times in the cycle.

Individual pixel panning is accomplished by selecting the appropriate phase of the clock to latch sync and blanking signals. This technique effectively skews the displayed data on the screen. Since the monitor cannot instnatly adjust to this change in sync phase, the operation is done only at the beginning of vertical blanking.

Two-power zoom operation alters the control sequences to run most parts at half-speed. Clock signals to the scanner, however, must remain at full speed and not shift in phase at the transition to zoom mode. This condition requires that the transition be synchronized to the scanner clock.

2.6 - Output Section

Storage registers contain all the output LUT information. The board provides an option of two D/A converters (DACs): monochrome or color (TO444).

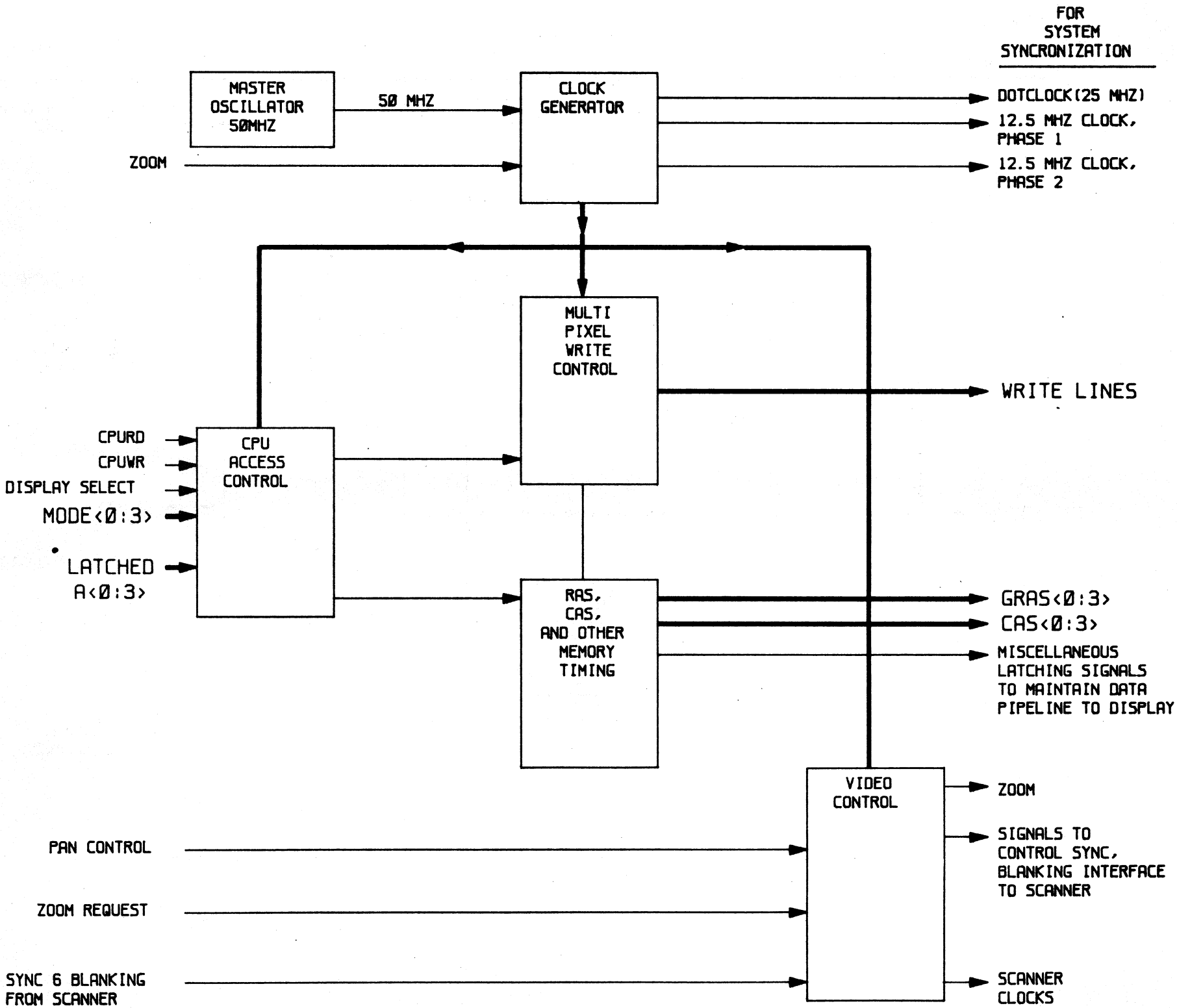


Figure 2.6 : Timing and Control

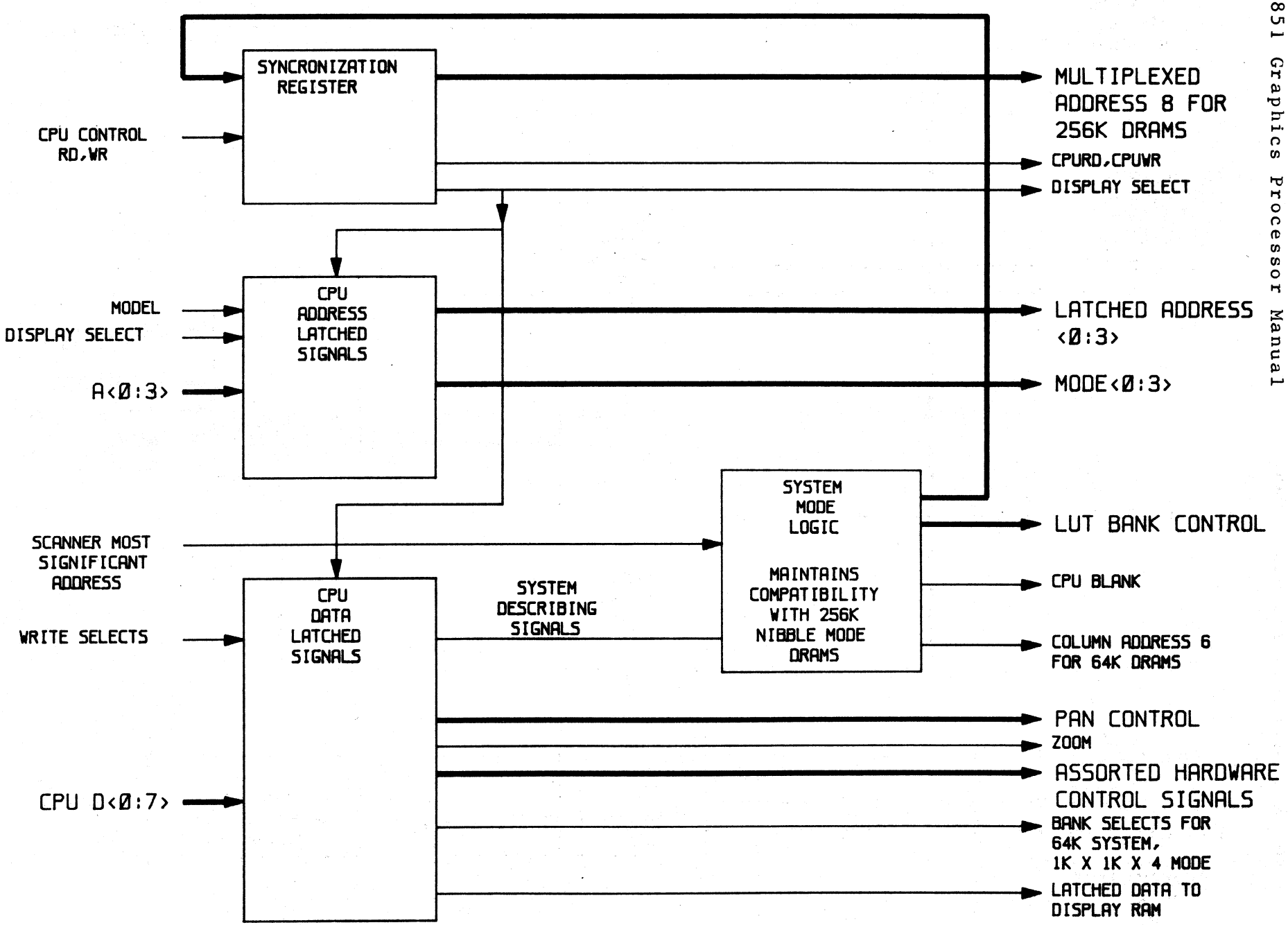


Figure 2.7 : System Control

Each look-up table (LUT) receives four bits of information. One byte contains data for the red and green LUTs, and a nibble transfers blue LUT data. In the color system all three LUTs send four bits of color information as output. The DACs convert this information into RGB signals. In the monochrome system, the red and green LUTs supply the first eight bits as input data for the DAC. The blue LUT contributes two bits which the DAC interprets as reference white and 10% overbright. These non-linear values directly affect the information defined by the other eight bits. When the CPU asserts the reference white line, the output increases to full intensity. The 10% overbright line high causes the data input to increase its intensity by 10%. The monochrome video output appears on the green output signal used for color. This method capitalizes on the sync-on-green capability.

3 - Hardware Operation

3.0 - Overview

This section describes the theory of operation of the VM-8851 graphics processor. Each subsection contains detailed descriptions of each of the major blocks in the VM-8851 architecture. Please refer to the schematics in appendix B while reading these sections as the text often refers to a specific schematic sheet. Signal names are printed in upper case, e.g. XACKL. Components are indicated by a single letter followed by a number, e.g. U62. A "U" refers to an integrated circuit, "R" to a resistor, "C" to a capacitor, "D" to a diode, "P" to a male connector, "J" to a female connector, and "W" to a jumper.

3.1 - Processor Section

With a 24 MHz crystal, Y13, the clock generator, U2, outputs an 8 MHz CLK. U2 also controls the generation of CPU wait states through the RDY output pin. The AEN1 input to U2 is held high when the CPU has to wait to access display RAM, the scanner, the start address table, or the SBX board. For SBX connector transfers requiring wait states, a low signal on MWAITL will prevent an AEN1 signal.

When display RAM is accessed, pin 13 of U9 goes low until the display RAM controller returns DISPRDYH. AEN1 is forced high causing the processor to wait. Likewise, when either the scanner or the start-address table (SAT) is accessed, pin 19 of U10 goes high. This change causes AEN1 to go high until the scanner/SAT arbiter, U38, activates SCNRDYL. U9-13 also goes low when an off board access occurs, producing a wait state until the bus arbiter, U26, activates the signal AEN2L. AEN2L acts like the select input of a multiplexor. When high, its normal state, the AEN1 input of U2 is active. When AEN2L is low the AEN1 input is ignored, but the RDY2 input driven by the bus XACKL signal, is used to produce RDY.

The resistor R1, capacitor C119, inverter U107, and open collector driver U109 combine to provide the power-on reset function. A MULTIBUS reset signal INITL will also reset the clock generator, thereby resetting the CPU, U1. The CPU, U1, operates in maximum mode (MIN/MXL=GND.) The bus controller, U3, decodes CPU status signals S0, S1, and S2 to create MRDCL, MWTCL, and AMWCL control signals. U3 also generates the address latch enable signal (ALE) and the data buffer control signals DEN and DT/RL. During an interrupt acknowledge cycle, U3 generates INTAL. The input CEN disables U3 during an off-board access cycle.

During the interrupt acknowledge cycle, the interrupt controller, U4, accepts up to seven level-sensitive interrupt inputs on IR0 through IR5 plus SINT and PBINT1 and issues a vector with

appropriate priorities to each of data bus lines D0 through D7. Jumper matrix W1 routes the incoming interrupts to the appropriate interrupt line.

Jumper matrix W2 determines the selection of one of eight MULTIBUS interrupts for input and two of eight interrupts for output. The interrupt PBINT2 or the CPU-generated interrupt MBINT route through open collector driver U109 to any of the eight MULTIBUS interrupt lines. An optionally-attached floating point processor supplies interrupt line MINT. (Refer to iSBC 377 module for details in Intel manual 142887-001.)

3.2 - Host Interface

Pages five and six of the scematics show the MULTIBUS host interface section which consists of both programmed I/O and DMA interfaces. Both of these interfaces are fully compatible with the separate interface boards used on the VM-8850A and may be used simultaneously.

The board typically uses eight bytes of MULTIBUS address space and may be configured for 8-, 16-, 20-, or 24-bit address decoding, either memory or I/O mapped. Pins 2 and 3 of W22 select the type of address while pins 4 through 9 provide six bits of address comparative data. W5 and W6 select between memory mapped and I/O mapped operation. Refer to section X.X for address selection.

FPLAs U25 and U13 act almost like multiplexors in that AM1 and AM0 select which set of six address lines to compare against the six inputs from jumper W22. The six most significant bits in each address type are thus compared with the jumpers, while the less significant bits are usually required to be zero. Any arbitrary address may be selected, however, by reprogramming U25 and U13. When the address matches, U13 produces HSTSEL. Another PLA, U24, receives HSTSEL along with ADRL0-ADRL2 and the read and write control signals. U24 decodes these to produce the following chip select signals.

Use address 0 for programmed I/O data transfer. A read at this address produces DTAENL, enabling U22 to drive the data bus, while a write produces SI, which shifts data in from U14 to the FIFO, U15-U18. TAG1 and TAG2 will equal 0 for programmed I/O transfers.

A read at address 1 produces STSENL. This signal, used in both programmed I/O and DMA operations, enables U21 onto the data bus. A write to address 1 produces CMDLCHL which clocks U33 to latch data bits 0 and 2 to form the host's interrupt enable masks. U23 also uses CMDLCHL to latch data bit 6, which constitutes the reset command.

Addresses 2 and 3 are not used. Addresses 4 through 7 are used for DMA operation and are write only. A write to any of these

addresses produces SI, to shift the data into the FIFO; DMACMDL, which signals U23 that DMA is being written; and the tag bits TAG1 and TAG2. The tag bits identify the type of data in the FIFO. This information is deduced from the address to which the data was written. As noted above, a tag value of 0 denotes programmed I/O data. Value 1 (address 4) is the low byte of a DMA control block address. Value 2 (address 5 or 6) indicates the high byte(s), and value 3 (address 7) marks the DMA reset command. An access to any of the valid addresses described above also produces XACKL immediately to signal the bus master that the transfer can proceed. U24 produces TXRDY as long as 1) the FIFO is not full, or half-full, depending on the setting of W20, and 2) a reset (warm start) is not in progress. Depending on the state of the host's interrupt enables (from U33) plus the states or TXRDY and RXRDY, U24 produces PBINT2, which may be connected through W2 to one of the eight MULTIBUS interrupt vectors.

U23 produces a variety of status information. When the host sends a reset command (CMDLCHL active and D6 equal to 1), it activates CGBRST. The CPU clears this signal by producing PBCS1 with A0 equal to 0. Similarly, RXRDY is set when the local CPU produces PBCS2 (latching data into U22) and cleared when the host produces DTAENL (reading data from U22). Activating the bus reset signal INITL also clears both RXRDY and CGBRST. DRDY is high whenever OR from U18 is high unless CGBRST is high. HFULL is active low when IRHF from U18 is low, unless CGBRST is low. HFULL low indicates a half-full condition in the FIFO.

The signals DMACMDP and DMAPRSNT are similar. They indicate the presence of DMA data in the FIFO and are set when DMACMDL is activated. DMAPRSNT serves as a status bit to the local CPU. It is cleared automatically when the DMA reset command is read out of the FIFO. DMACMDP, a status bit to the host, is cleared when the CPU produces PBCS1 with A0 equal to 1.

The two most significant bits (MSBs) latched by U28 (refer to sheet 6 of the schematics) are MASK1 and MASK2. In U23, these bits condition the generation of PBINT1 as follows. CGBRST active produces the interrupt regardless of mask bits. If MASK2 is high, RXRDY low produces the interrupt. (RXRDY low indicates that the host has read the last data sent.) If MASK1 is high, the interrupt is produced by either HFULL active or by tagged data (DMA data) available at FIFO output. The local CPU reads these status bits through U20 and FIFO data through U19.

Once DMA data is retrieved from the FIFO, the local CPU performs the DMA operation using the MULTIBUS master mode hardware on sheet 6 of the schematics. U26 arbitrates bus control, producing AEN2L when bus mastership is aquired. U27 decodes the CPU status lines S0-S2 to generate MRDCL, MWTCL, IORCL, IOWCL, the data bus enable, and the data direction control signals. U28 is a latch which is written before an off-board (master mode) access is made. This latch holds the upper six bits of the MULTIBUS address since the 8088 CPU has only 20 address lines, two of which are used to decode the off-board request. U29-U31 drive

the MULIBUS address bus with 18 bits from the CPU and six bits from U28. U32 buffers the data bus. The board supports only 8-bit data transfers. Refer to section X.X to determine the appropriate configuration of W7-W9 for a specific application.

U52 divides FCLK, the 50 MHz master clock, by five to produce a 10 MHz signal. This signal is buffered through U41 to drive TENMHZ to the SBX connector and BCLKL if W21 is closed. The other half of U41 buffers various status bits to be read by the local CPU. Bit 3 indicates the presence of an SBX module. Bit 2 connects to W23 but has no defined meaning at this time. Bit 1 reflects the state of LPENSW. Bit 0 is reserved for future expansion.

3.3 - Scanner and Start Address Table (SAT)

The CRT9007, U36, produces sync, blanking, and other control signals in addition to the addresses applied to the display RAM. This programmable LSI device is oriented to alphanumeric displays but is readily adapted to the high performance graphics in the VM-8851. The signal SCCLK, buffered by U110, clocks U36 at a 640 nsec period. Each such period produces a new address which ultimately provides 16 pixels to the display, that is, 40 nsec per pixel. The low six bits of the video address bus, VA0-5, address up to 64 such "characters", or 1024 pixels. The SL0-2 lines form the next three bits of address, the three least significant bits of the y-coordinate. These bits simply increment during each horizontal retrace. The first line at the top of the screen, however, may load SL from an internal register to effect single line scroll. VA6-12 form the remainder of the y-coordinate for a total address range of 1024 x 1024.

At the beginning of each 8-line "window", U36 produces DRB and a special address from an internal register. This process causes data from the start address table (SAT) to drive the VD bus. In this way, U36 reads the SAT to determine the address in display RAM of the next window. This address is a "character" address, that is, it has a resolution of 16 x 8 pixels. The CPU writes to the SAT to control which portion of RAM is displayed. Thus one level of panning can be effected by simply modifying entries in the SAT. As noted earlier, finer vertical pan (scroll) is done by preloading the SL address at the beginning of each frame. Finer horizontal pan is acomplished by skewing tha sync and blanking signals slightly. Refer to section X.X.

A two-power zoom operation is likewise performed at the character level. UU36 increments the memory address on every other clock, and SL increments every other line. Further manipulation of individual pixels for zoom operation is described in section X.X.

The signal LPENIN connects to U36 in order to latch the character address at the time of light pen strobe. The CPU then reads the address from U36. The sync outputs are "open drain" and may be driven with external sync signals by wiring W11 and W12 pin 2 to

4. This configuration causes U36 to synchronize to the external sync source. CKD2 and CRD3 prevent conflicts between the two sync drivers.

U38 is a programmable logic sequencer (FPLS) which arbitrates access between the CPU, the scanner (U36), and the SAT (U39 & U40). When the CPU asserts SCNRSL, U38, by leaving SCNRDYL high, causes the CPU to wait until the scanner is not using the VA and VD buses. U38 then enables the CPU to drive these buses through U34 and U35, producing SCNRDYL and the chip select for U36. Likewise, when the CPU asserts STBLSL, U38 times the transaction and produces the chip select and write enable to U39 and U40. The scanner also reads the SAT. U38 determines this information from DRB and VLT and produces the SAT chip select. Since the scanner operates in real-time mode, it generally has higher priority than the CPU.

U37 latches the sync and blanking signals in two stages. The first stage simply synchronizes them with the high-speed operation of display RAM. The second stage is clocked by a phase variable signal to effect horizontal pan. Before either stage occurs, composite blanking, CBH, is combined with CPUBLANK in U113 and then fed through U118. Refer to sheet 8 of the schematics. By setting pin 9 of U68, U118 shortens the unblanked period to either 512 or 640 pixels as selected by the CPU. This step is necessary because in panning, part of the last character scanned is not displayed. The scanner, though, cannot assert CBH before it has completed scanning a line.

U117 combines horizontal and vertical sync to produce composite sync. U105 then buffers those signals and provides both polarities to W11 and W12 for user selection.

3.4 - Display RAM Timing and Control

This section covers primarily the circuits shown on sheets 8 and 9 of the schematics.

U42 latches the CPU-generated signals AMWCL, RDL, and DISPL to synchronize them with the display RAM arbitration circuit. This synchronization avoids dynamic hazards. DISACCH also loops through U42 again, producing DDISACCH which clocks U72. This delay is needed because CAD6, which is latched by U72, is produced from LA1, which in turn is latched by DISACCH. U42 also synchronizes MADA8 and MADB8. These multiplexed address lines are used with the optional 256K x 4 RAM chips. U48 produces these lines as a function of CPU bank select, display bank select, DISP/CPU, and ROW.

U43 is a dual 4-bit latch, each half having A0-3 as inputs. The first latch is clocked on DISACCH to latch the four LSBs of address on display RAM access. These bits are called LA0-3 and determine which pixel(s) in a group (character) of 16 is desired. The same clock signal latches the other address lines in U71 and

U72 (sheet 11) and data in U44. These buses are latched so that, on write operations, the CPU need not wait for the arbiter to complete the operation.

U45 is a latch triggered by chip select PZBSML. It is used to control panning via PAN0-3, display blanking via CPUBLANK, and zoom via ZOOMH. The CPU must set these signals at the appropriate time to avoid display glitches, generally during vertical retrace.

NMBSLL clocks U46 to latch four different sets of control signals, each two bits wide. N0-1 are nibble write-protect masks applied to display RAM write operations. CPUBS0-1 select which of four possible 512K byte display RAM banks is used when the CPU accesses display RAM. With 64K x 4 RAM chips, these bits should always equal 00. DISPBS0-1 likewise select which bank is displayed and should equal 00 with 64K x 4 RAM chips. SYSMODE0-1 selects the display RAM configuration. Essentially, SYSMODE1 selects 64K x 4 or 256K x 4 (0 or 1 respectively), while SYSMODE0 selects 1K x 512 organization or 1K x 1K organization (0 or 1 respectively). These signals are decoded along with other address and timing signals by U48 to produce the multiplexed address lines mentioned above, LS8, WRITEN, and CAD6. LS8 and LS9 (from U47) select which set of look-up tables are used in the output section. In 1K x 1K x 4 organization, denoted by SYSMODE 01 or 11 and PIXDEPTH=1), LS8 is driven by VA12SYNC so that when the scanner addresses the second bank, it really receives data from the first bank. The look-up table is conditioned to use the upper nibble of data instead of the lower. In other modes, LS8 is simply a copy of LUT8. The exception occurs during blanking. In that case, LS8 copies A9 so that the CPU can directly access two sets of look-up tables. LS9 is always available to the CPU to select different sets of look-up tables.

CAD6 is column address 6 of the display RAM. With 256K x 4 chips, CAD6 is driven by CPUBS1; with 64K x 4 chips, it is driven by LA1 for read operations. It is driven low for write operations to provides multi-pixel writes with nibble mode write cycles. Column address 6 is the least significant nibble address with 64K x 4 nibble mode RAMs.

U47 and half of U68 are clocked by chip select signal ZHSRHSL. D0 maps to RSTSCNL which resets the scanner when low for greater than 2.5 usec. D1 is latched to produce PIXDPTH which controls the selection of LS8. D2 and D3 determine the LUT select signals LUT8 and LS9. LUT8 is conditioned in U48 as described above to generate LS8. D4 is latched to drive MBINT, the general purpose MULTIBUS interrupt. D5 produces signal ZZ which feeds back to address decoder U9. The hardware reset signal, INIT2L, clears U47, so ZZ is interrupted in U9 to enable selection of ROM at address FFFF:0, the 8088 reset vector. When ZZ is set high, this address is treated as an off-board access. D6 is not used with ZHSRHSL. D7 is latched by U68 to control horizontal blanking width. A value of 0 selects 512 pixel width and 1 selects 640 pixels.

U49 is an integrated 50 MHz oscillator which produces the master clock signal FCLK. U50, U51, U116, and U120 produce various divisions and phases of the master clock. These include QA-D which represent the 16-pixel periods in each scanner clock cycle.

U58 is a programmable logic sequencer (FPLS) which functions as the primary display RAM controller. Signals GRAS0-3 connect to the RAS inputs of four banks of display RAM. These signals are generated by gating four signals from U58 and two from U54 in U59. As with all the display RAM inputs, these are damped with 22 Ohm series resistors to minimize reflections. U54 then produces CAS signals CAS02 and CAS13 in a regular pattern while U58 varies the generation of RAS signals to achieve different types of cycles: scanner read, CPU read, CPU write, and refresh. Refresh is performed with CAS-before-RAS cycles during horizontal sync. U58 also produces a function enable signal, which drives U54 and U56 during CPU accesses, and DISPRDYH, which signals the CPU when a display access operation can proceed. U54 also produces, SLATCH, which loads the display output; DAVL, which loads the CPU read buffers U89-U92; ADLATCH, which synchronizes input signals in U42 and final display RAM addresses in U73-76; and SCANLATCH, which synchronizes the address coming from the scanner in U68-70.

U56 performs three functions. First, the scanner clock signals SCCLK, SBCLK< and SACLK generated by U56 are used in U38 to time various scanner operations. These clocks must be altered in zoom mode. Second, U56 synchronizes the transition of zoom mode, as signalled by ZOOMH, to the scanner clock. Pin 19 is the synchronized zoom output. Finally, U56 produces WCLK and WENL, which are used in U57 to control the timing of write operations.

Horizontal pan at the pixel level originates in U55. SYNCLATCH is generated at a fixed point in each character cycle to latch valid sync and blanking signals from the scanner. DELYLATCH then latches these signals again at a time determined by the PAN0-3 inputs. The outputs on pins 20 and 19 are decoded by U106 to produce SE0-3 which enable the display output registers U77-80 onto the pixel data bus one at a time. U55 also produces the signal DISP/CPU, to identify when CPU accesses may be performed, and ROW, which selects between row and column addresses to the display RAM by enabling U69, U70, U71, or U72.

The second half of U106 selects which data buffer of U89-92 is enabled onto the CPU data bus during a display RAM read. This operation is a function of LA0 plus the XOR of LA2 and LA3, which come from U119. The select outputs are enabled by DAVL, which also "freezes" the transparent latch data buffers.

U57 produces eight write enable signals to the display RAM, one for each nibble of each of four banks. The outputs activated for a given srite operation are a function of the mode bits M0-1, the nibble mask bits N0-1, latched address bits LA0-1, and counter bits QA and QB. The outputs are also conditioned by WENL and

WCLK. The various write modes are accomplished by a combination of RAS generation, timing, and write enables.

3.5 - Display RAM

Most of the circuitry on sheets 11-13 has been described in the previous subsection as the object of various control functions. This subsection may, therefore, appear somewhat redundant but provides some greater degree of detail.

The scanner address bus, VA0-12, is latched in U68, 69, and 70. VA12 is applied to the display RAM only when 256K x 4 chips are used. It is also applied to the output look-up table when pixel depth equals four to select which nibble is mapped to the output. SRC6 is latched from DISPBS1 which must be 0 with 64K x 4 DRAM chips, as this signal becomes the address bit incremented by nibble mode operation. With 256K x 4 chips, DISPBS1 may be varied to display different portions of the display RAM. U71 and U72 similarly latch the CPU address. A18 is inverted so that the CPU sees display RAM from 40000H to BFFFFH. The four LSBs of CPU address drive control functions to selct pixels from a group of 16. U72 latches slighty later than U71 because CAD6 is produced from signals latched at the same time as U71. CAD6 is a special address bit in the same way as DISPBS1 in U70.

The signal ROW enables the low order address bits (U69 and U71) when it is low. U113 inverts ROW to enable the high bits when ROW is high. This transformation forms the row/column multiplexor common in dynamic RAM controllers. U73-76 then select between scanner address and CPU address based on DISP/CPU. The same ICs also contain high-speed latches to minimize variations in propagation delays relative to display RAM control signals. Two memory address buses, MADA0-8 and MADB0-8, are used to allow CPU access to two banks while the scanner accesses the other. Each address bus has 22 Ohm series resistors to dampen reflections.

U77-80 latch data read out from the RAM for display. that is, data addressed by the scanner. SLATCH has a period of 80 nsec and latches 32 bits of data. Half of the data comes from the memory being addresses by the CPU. In this way, only two of the SE0-3 signals are used in one SLATCH period. The next SLATCH latches data from the same memory banks. These banks have been "CASed" to perform nibble mode access, so the same pair of SE signals are activated again. As DISP/CPU changes, the bank usage changes, and the opposite pair of SE signals are used.

In a similar manner U89-92 latch data being read by the CPU. In this case only one of the signals SC0-3 is activated for a given cycle. DISP?CPU and the accessed address determine which signal is activated.

The display RAM itself consists of U81-88 and U93-100, 16 22-pin SIPs containing 512 Kbytes of information using 64K x 4 devices

or two Mbytes using 256K x 4 devices. The chips are divided into several different groupings for various functions. U81-88 are addressed separately from U93-100 and drive a common 32-bit output bus. RAS signals further divide these groups in half so that, while on drives the lower 16 bits of the MD data bus, the other drives the upper. All the odd numbered members are low-nibble while evens are high-nibble. These members are differentiated only by the write enables. The 8-bit data input bus is common to all devices.

Both types of RAM devices are high-speed, supporting both nibble mode access and CAS-before-RAS refresh. In nibble mode operation, the CAS input is pulsed during the cycle to increment the address, allowing high-speed access of up to four locations. Unfortunately, the address bits which are effectively incremented are not the least significant bits, nor are they the same bits for the different types of devices. To minimize the impact of this difference, the VM-8851 uses only one extra CAS pulse, accessing two locations. With CAS-before-RAS refresh, an internal counter is incremented and used as the row address whenever RAS is activeated and CAS is already low.

3.6 - Output Section

Video output data appears on SR0-7 and is latched in U61 (sheet 10) on each PDOT (40 nsec) cycle. During display time BLANKH is low thus enabling U61 to drive the address inputs of the look-up table (LUT), U63-65. The upper two bits of LUT address select which of four possible mappings is used. LS9 is the output of a latch which is set by the CPU. LS8 may also come from the latch, but in some modes of operation it is derived from the scan address. This alternative allows real-time selection of a mapping which ignores part of the address data.

When BLANKL is low U61 is disabled and U62 is enabled. This configuration connects the CPU address bus to the LUT address lines. The CPU data bu is also applied to the LUT data inputs. U63 and U64 have a common write enable which is activated for even addressed writes to the LUT. The write enable from U65 is activated on odd addresses, using only four of the eight data lines. This scheme allows fast loading of LUTs by a string move command. LUTCLRL sets all LUT entries to zero so that non-programmed value will always produce black. The CPU may force activation of BLANK to ensure that long LUT programming sequences are completed before blanking ends.

BLANK is delayed by the first half of U60 to synchronize it with the dot clock (PDOTL). The second half of U60 stretches the unblanked period by one pixel. This transformation is necessary because the blanking inputs of the video DACs are asynchronous at the beginning of blanking.

Two video output options are available on the VM-8851, although both may not be used simultaneously. U67 is a video DAC hybrid

containing three 4-bit digital-to-analog converters and three buffers. Four bits from each LUT chip drive each DAC channel, thus providing 4096 possible colors. U66 is an 8-bit monochrome DAC which drives the green output, J8. The device employed here is based on ECL technology and is powered "upside-down" with the +5 Volt supply. That is, its -5 Volt supply pins are connected to ground, while the ground pins are connected to +5 Volts. RP2 pulls up the TTL level signals to ensure that they exceed the effective ECL levels. Both DACs are powered through an RC network consisting of R3, C921, and C922 to eliminate digital switching noise in the output. The data inputs of the monochrome DACs are driven by the "red" and "green" LUT outputs. The two bits which come from the "blue" LUT also drive reference white and 10% overbright inputs.

W13 is used to select sync options. The color outputs may have sync on green or not, and likewise for the monochrome output. Refer to the configuration section for configuration details.

5 - Firmware Design Considerations

5.1 - Firmware Initialization

A hardware or "power up" reset causes the CPU on the VM-8851 to perform an instruction fetch from location FFFF:0. This location in EPROM/PROM must contain a direct intersegment jump instruction to the firmware initialization routine. This routine normally includes initialization of the I/O ports and CRT scanner chip, clearing of display RAM, setting up of internal variables, and initialization of the look-up tables (LUTs).

5.2 - Address Assignment

The following memory map defines the hardware locations of the VM-8851:

ROM 1 (LMS0L)

0 0 0 0 0 x x x x x x x x x x x x x x x	0 - 7FFFH

ROM 2 (LMS1L)

0 0 0 0 1 x x x x x x x x x x x x x x x	8000H - FFFFH
or	
1 1 1 1 1 1 1 1 x x x x x x x x x x x x	FFFF0 - FFFFF (64K INTERACT only)

RAM 1 - 8K (LMS2L)

0 0 1 1 0 0 0 x x x x x x x x x x x x x	30000 - 31FFF

RAM 2 - 8K (LMS3L)

0 0 1 1 0 0 1 x x x x x x x x x x x x x	32000 - 33FFF

Display RAM (low half)

0 1 x x x x x x x x x x x x x x x x x x	40000 - 7FFFF

(high half)

1 0 x x x x x x x x x x x x x x x x x x	80000 - BFFFF

LUTs (write only)

```
0 0 1 1  1 0 0 0  0 0 x |---value code--|0/1| 38000 - 381FF
                                          ^
                                          |
                                          |
                        0 = GGGG RRRR -------
                        1 = 0000 BBBB
```

Scanner Chip

```
                                  address to
0 0 1 1  1 0 0 0  0 1 x x  |---scanner----|   38400 - 384FF
```

Start Address Table

```
0 0 1 1  1 0 0 0  1 0 x x  x x x x  x x x x   38800 - 388FF
```

MSC0

```
0 0 1 1  1 0 0 1  0 0 x x  x x x x  x x x x   39000 -
```

MSC1

```
0 0 1 1  1 0 0 1  0 1 x x  x x x x  x x x x   39400 -
```

MODEL - write only

```
0 0 1 1  1 0 0 1  1 1 x x  1 0 0 0 |-mode-|   39C8x
```

mode is address activated - write any value

Modes :		
	Single pixel	0 0 0 0
	Four pixel	0 0 0 1
	From beginning of four	0 0 1 0
	From end of four	0 0 1 1
	Sixteen pixel	1 0 0 1
	From beginning of 16	0 1 0 1
	From end of 16	1 1 0 1

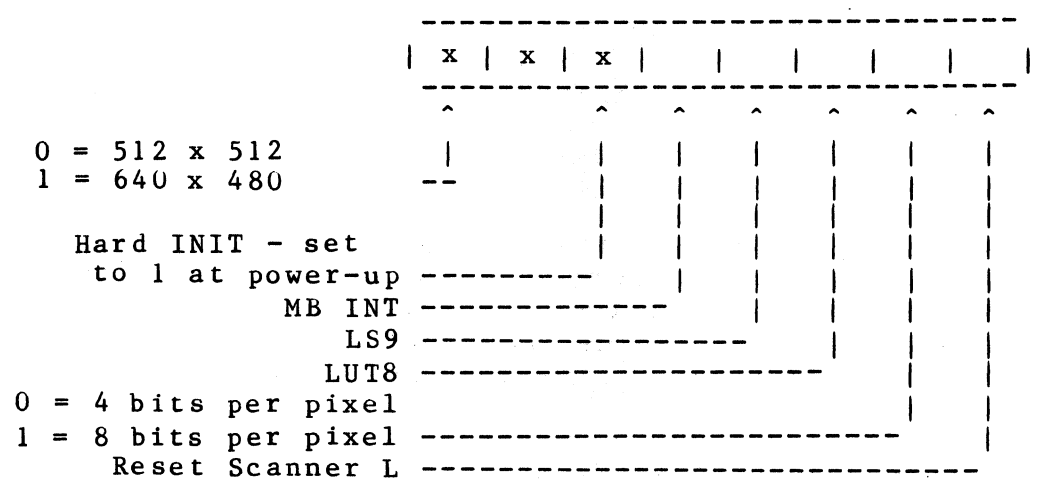
NMBSLL - write only

```
0 0 1 1  1 0 0 1  1 1 x x  1 0 0 1  x x x x   39C90
```

```
                  --------------------
                 |sys |disp|CPU |    |
                 |mode|bank|bank|N1 N0|
                  --------------------
                    ^    ^    ^    ^
                    |    |    |    |
                    |    |    |    |
    system mode ------   |    |    ----- nibble mask
   display bank ----------    ---------- CPU access bank select
```

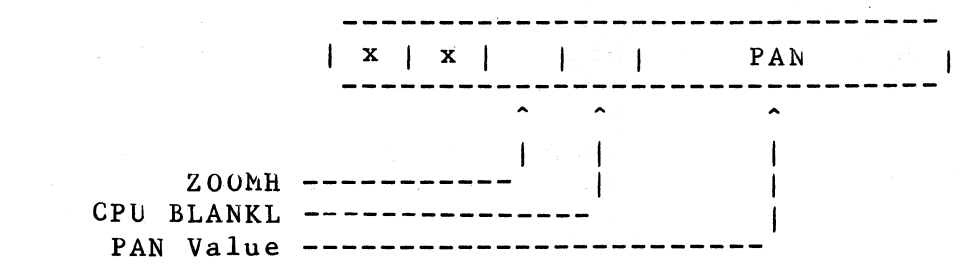
HREG1 - write only

0 0 1 1 1 0 0 1 1 1 x x 1 0 1 0 x x x x 39CA0



HREG2 - write only

0 0 1 1 1 0 0 1 1 1 x x 1 1 1 1 x x x x 39CF0



Set CPU BLANKL low to access the LUTs. The PAN value gives the number of pixels from the very first group of 16 to be displayed at the beginning of each line.

ADRLCHL - write only

0 0 1 1 1 0 0 1 1 1 x x 1 0 1 1 x x x x 39CB0

PBCS0 - read only

0 0 1 1 1 0 0 1 1 1 x x 1 0 1 0 x x x x 39CA0

PBCS1 - write only

0 0 1 1 1 0 0 1 1 1 x x 1 1 0 1 x x x x 39CD0

PBCS2 - write only

0 0 1 1 1 0 0 1 1 1 x x 1 1 0 0 x x x x 39CC0

PBCS3 - read only

0 0 1 1 1 0 0 1 1 1 x x 1 0 0 1 x x x x 39C90

5.3 - Memory Organization

Field programmable logic array (FPLA) devices decode the array space for the VM-8851. Local memory is available on four JEDEC sockets with the restriction of the first socket dedicated to PROM/EPROM only and the fourth socket dedicated to RAM. RAMs are limited to 8K x 8 static. Different configurations of local memory are jumper selectable.

The first five bytes of PROM/EPROM in the first JEDEC socket must appear at address FFFF0h to FFFF4H. Also the interrupt table requires 1024 bytes reserved at addresses 0000H to 003FFH.

5.4 - Display RAM Organization

The VM-8851 display RAM contains either 512 Kbytes or two Mbytes depending on the size of the RAM chips used. The display RAM is organized into one of four possible modes:

1 - A configuration of 1K x 512 pixels by eight bit-planes results in a single buffer with 512 Kbytes and four buffers with two Mbytes.

2 - Same hardware configuration as 1 allows two side-by-side 512 x 512 x 8 buffers with 512 Kbytes or eight buffers with two Mbytes.

3 - A configuration of 1K x 1K pixels by four bit-planes provides a single buffer with 512 Kbytes and four buffers with two Mbytes.

Note: this mode uses a different LUT accessing scheme. Refer to section 5.6 for more information about LUT programming.

4 - A configuration of 1K x 1K pixels by eight bit-planes, while illegal in the 512 Kbyte mode, provides two buffers with two Mbytes.

The SYSMODE bits in the NMBSLL hardware register enable switching between these modes of organization. The following table illustrates this method:

SYSMODE	Display RAM Organization	Number of LUTs
0 0	1K x 512 x 8, 1 buffer	4
0 1	1K x 1K x 4, 1 buffer	2
1 0	1K x 512 x 8, 4 buffers	4
1 1	1K x 1K x 8, 2 buffers	4
	or 1K x 1K x 4, 4 buffers	2

Note that the high bit of SYSMODE is only valid with two Mbytes of display RAM.

5.5 - Display RAM Access

Access to display RAM depends on display RAM organization, referenced by a SYSMODE number. Section 5.4 correlates a SYSMODE number to its appropriate display RAM organization.

In SYSMODE 00, all bank bits must equal 0 in NMBSLL. Access to all addresses require no further hardware changes.

In SYSMODE 01, all bank bits must equal zero. To both scanner and CPU, display RAM appears in a 1K x 512 x 8 organization. The low nibble of each byte is displayed in the top 512 lines of the 1K x 1K x 4 space, and the high nibble is displayed in the bottom 512 lines. Because the scanner reads a full byte of pixel data, the look-up tables must be configured to ignore either the low 4 bits (bottom half) or the high four bits (top half). Top/Bottom display information is supplied on LUT bank select 0. Refer to figure 5.1 for an illustration of this configuration.

SYSMODE 10 occurs only with two Mbytes. In this mode the CPU and display banks occupy the same locations, with up to four banks allowed. Refer to figure 5.2 for more information. Access all addresses in any bank in this mode with no further hardware modifications.

SYSMODE 11 allows either a 4-bit or 8-bit pixel. Bit 1 of hardware register HREG1 specifies the pixel depth. Bit 1 equal to 0 flags the mode as 1K x 1K x 4. Bit 1 equal to 1 specifies the mode as 1K x 1K x 8. The 1K x 1K x 4 mode mimics the organization of SYSMODE 01 but with potentially four CPU and display banks. In this configuration, the CPU and display banks are identical. Refer to figure 5.3 for this configuration.

In the 1K x 1K x 8 mode, the references for the CPU and display banks differ. Display bank 0 comprises CPU banks 0 and 1, while display bank 1 holds CPU banks 2 and 3. Refer to figure 5.4.

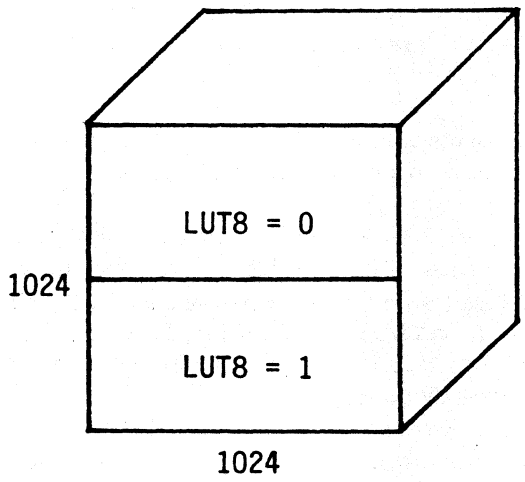


Figure 5.1 : Display RAM Map for SYSMODE 01

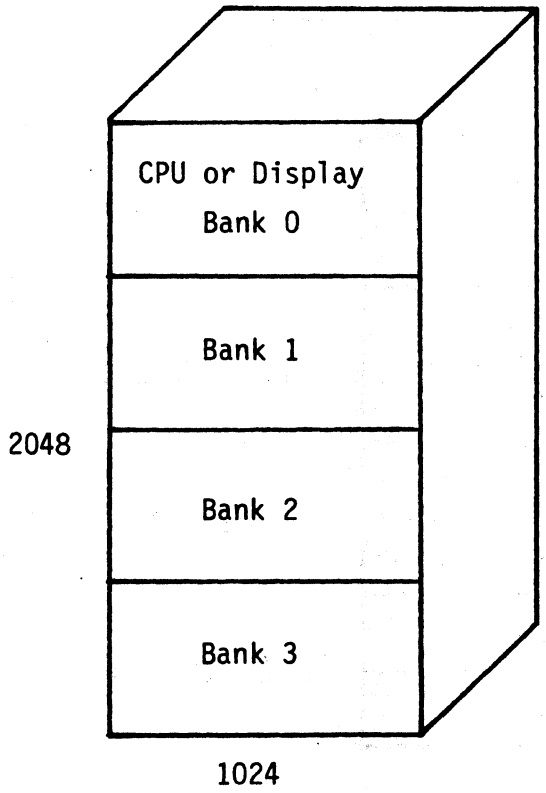


Figure 5.2 : Display RAM Map for SYSMODE 10

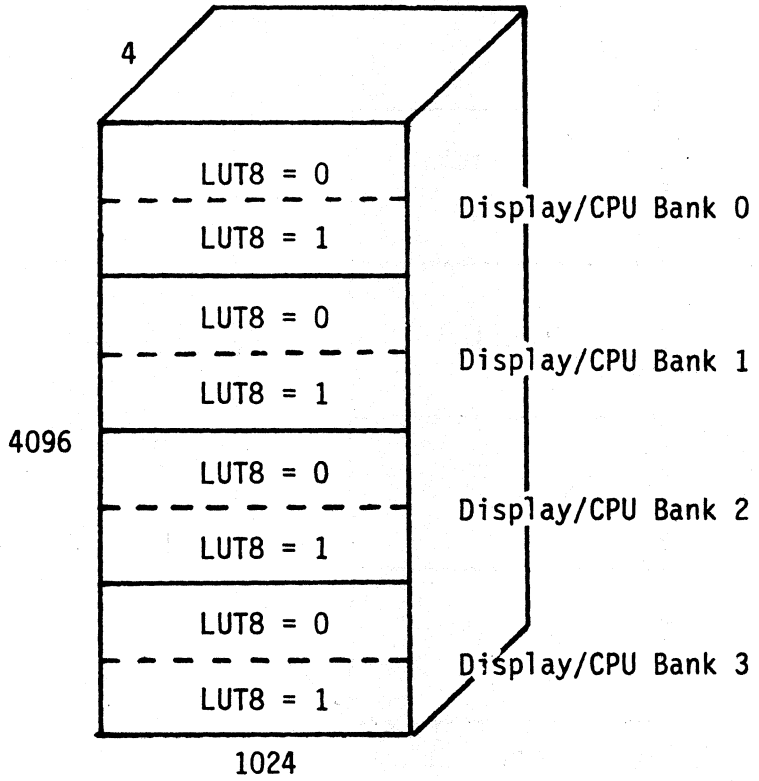


Figure 5.3 : Display RAM Map for SYSMODE 11 (1Kx1Kx4)

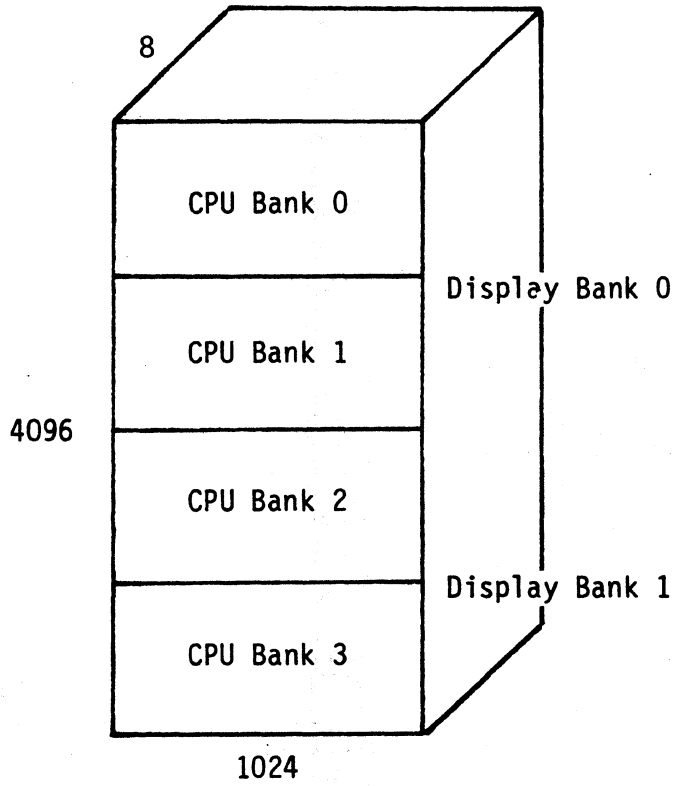


Figure 5.4 : Display RAM Map for SYSMODE 11 (1Kx1Kx8)

The VM-8851 also supports several different multiple write modes when writing to display RAM. Writing to a specific address activates the hardware registers. The following table correlates each address to its corresponding action:

Address	Action
39C80	Single pixel write.
39C81	Four pixel write.
39C82	Write from beginning of four-pixel boundary.
39C83	Write to end of four-pixel boundary.
39C85	Write to beginning of 16-pixel boundary in four-pixel groups.
39C89	16 pixel write.
39C8D	Write to end of 16-pixel boundary in four-pixel groups.

Note that multiple pixel writes do not acknowledge the four bit-plane mode. Therefore, to write in these modes, set the nibble mask appropriately as described below.

The VM-8851 has the ability to mask out one or both of the nibbles of the byte written to display RAM. Set the nibble mask bits in the hardware location NMBSLL.

5.6 - LUT Programming

The VM-8851 contains four banks of 256 word LUTs. An entry in a LUT bank appears as

x	B	G	R

where red (R) and green (G) reside in the bit whose least address bit equals zero. To access the LUTs, assert CPU_BLANK by clearing the CPU_BLANKL bit in HREG2. The LUT8 and LS9 bits in HREG1 control the bank selects of the LUTs. For all SYSMODEs except those with four pixel planes, LS9 is the high order bit and LUT8 is the low order bit for the LUT bank select.

5.7 - Interrupt Structure

The 8088 CPU has lines available as signal interrupts (INTR and NMI). On the VM-8851, the interrupt controller, U4, filters up to seven level-sensitive interrupts on IR0 to IR4, SINT, and PBINT1, placing the appropriate vector on the bus. All seven interrupts can be enabled or disabled by setting or clearing the CPUIF flag. The interrupt controller drives lines D0 to D7. The interrupt table is located between 0000H and 03FFH in the CPU local memory. Line D7 always remains high, while lines D0-D6

represent the seven interrupts. The CPU will fetch the interrupt vector from the 512-byte contiguous block in the upper half of the interrupt table. The 512-byte block must contain the seven 4-byte interrupt vectors for IR0 to IR4, SINT, and PBINT1. Place the 4-byte pointer to the NMI service routine at location 0008H. Refer to the Intel 8088 user's manual for more 8088 interrupt handling details.

Appendix A
Related Documents

Document Number	Description
VM2001-0001-06	INTERACT Graphics Language Manual
VM1018-1101-00	VM-8851 Specification Sheet
AFN-01200C-1	Intel iAPX-8088 User's Manual

Appendix B1

Schematics

NOTE:
1. ALL CAPACITORS ARE .22uf 25V CERAMIC DECOUPLING TYPE, UNLESS OTHERWISE SPECIFIED.

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ONE MAIN STREET, P.O. BOX 288 VINOOSKI, VT. 05404-0288

TITLE: 8851 GRAPHICS PROCESSOR
COMPONENTS DEFINITION

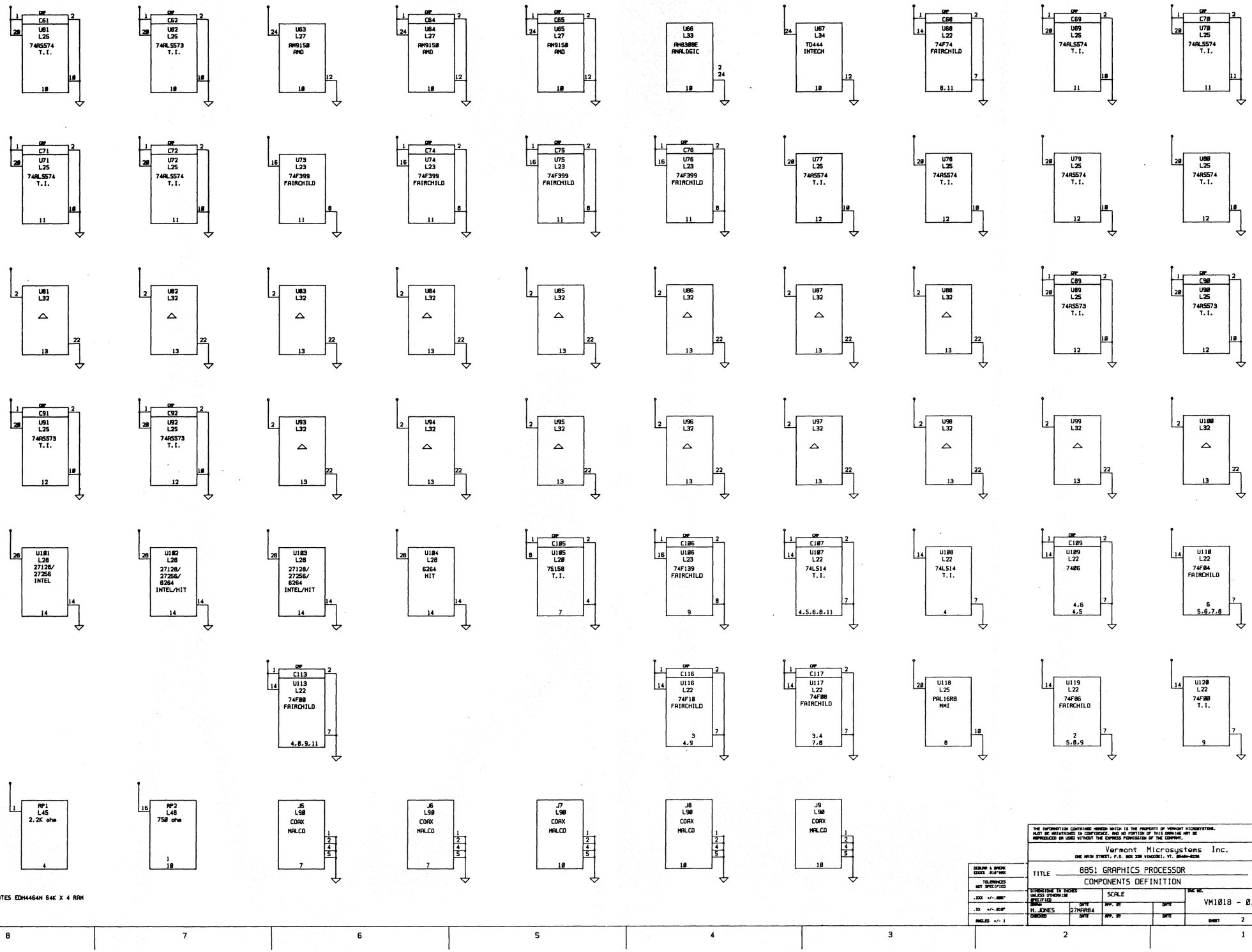
DESIGN & DRAWING EDGES .010"MAX
TOLERANCES NOT SPECIFIED
.XXX +/-.005"
.XX +/-.010"
ANGLES +/- 1

DIMENSIONS IN INCHES UNLESS OTHERWISE SPECIFIED
SCALE

DRAWN	DATE	APP. BY	DATE
M. JONES	1MAR84		
CHECKED	DATE	APP. BY	DATE

DWG NO. VM1018 - 0101 - 00

SHEET 1 OF 14



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TITLE 8851 GRAPHICS PROCESSOR
COMPONENTS DEFINITION

DRAWN & BROKE EDGES .010"MAX
TOLERANCES NOT SPECIFIED
.XXX +/-.005"
.XX +/-.010"
ANGLES +/- 1

DIMENSIONS IN INCHES UNLESS OTHERWISE SPECIFIED

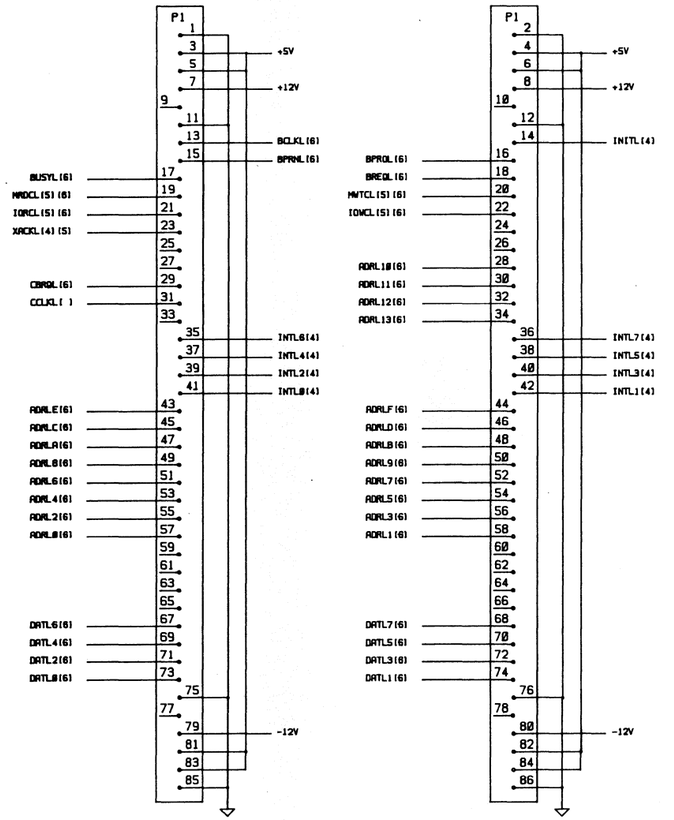
SCALE

DRAWN	DATE	APP. BY	DATE
H. JONES	27MAR84		
CHECKED	DATE	APP. BY	DATE

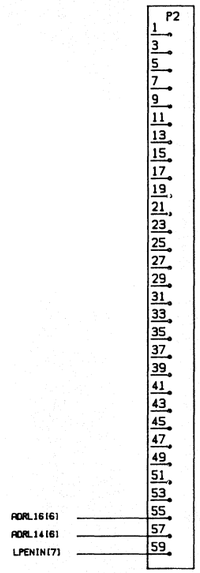
DWG NO. VM1018 - 0101 - 00

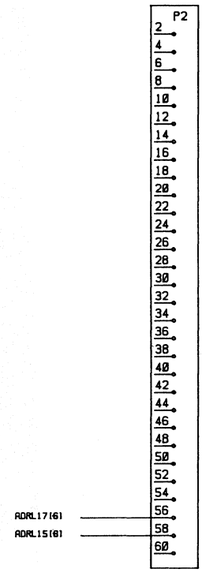
SHEET 2 OF 14

CONNECTOR P1

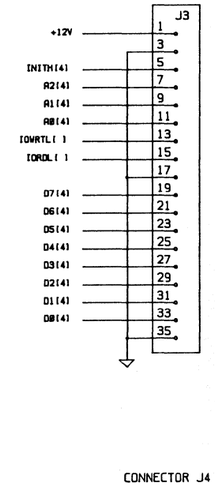


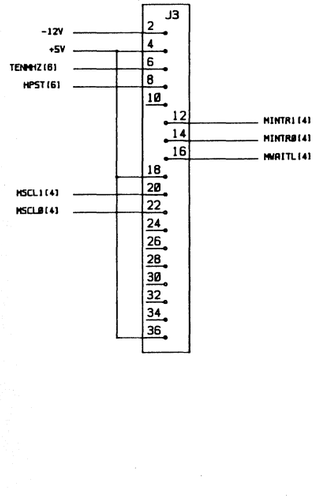
CONNECTOR P2



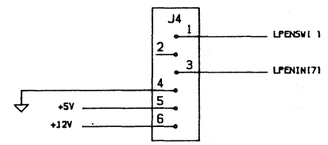


CONNECTOR J3
INTEL ISBX CONN(000-291-001)





CONNECTOR J4



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TITLE: 8851 GRAPHICS PROCESSOR
CONNECTIONS

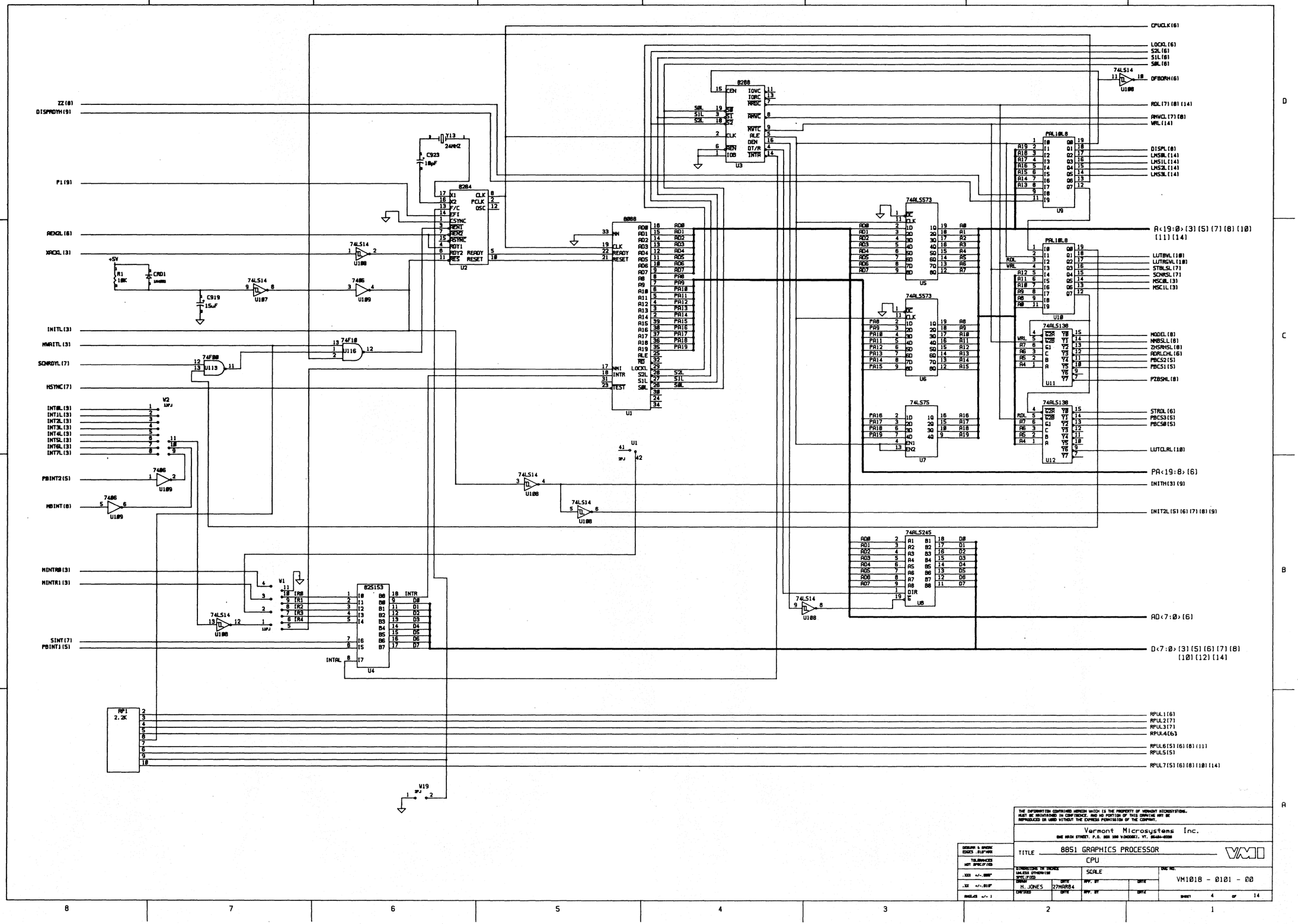
DRAWN: M. JONES DATE: 27MAR84
CHECKED: DATE:
APP. BY: DATE:
APP. BY: DATE:

SCALE:

DWG NO. VM1018 - 0101 - 00

SHEET 3 OF 14

DIMENSIONS IN INCHES UNLESS OTHERWISE SPECIFIED
DECIMALS & BREAK EDGES .010"MAX
TOLERANCES NOT SPECIFIED
.XXX +/-.005"
.XX +/-.010"
ANGLES +/- 1



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Vermont Microsystems Inc.
ONE MAIN STREET, P.O. BOX 388 WINOOSKI, VT. 05404-0388

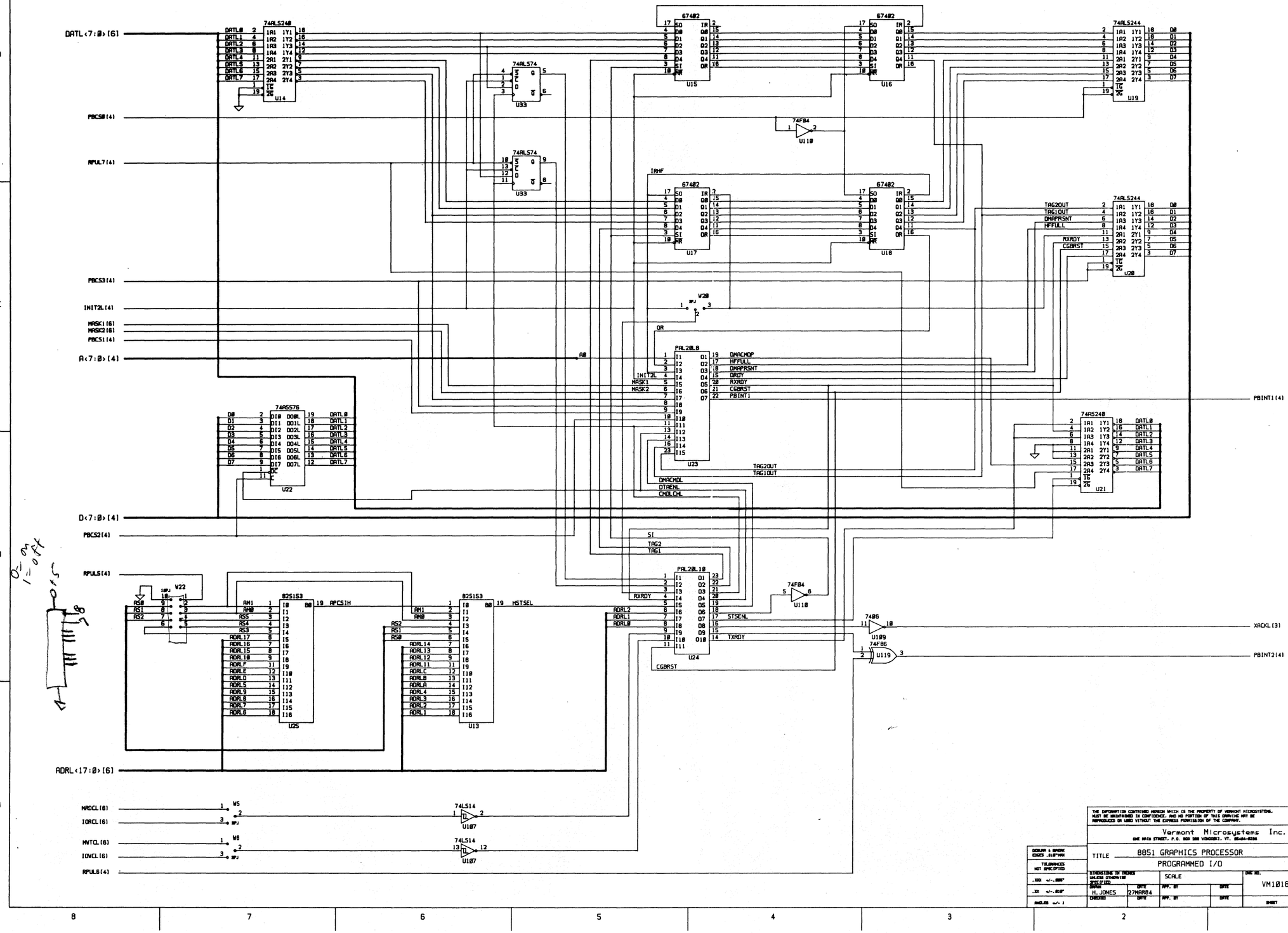
TITLE: 8851 GRAPHICS PROCESSOR CPU

DRAWN: M.JONES 27MAR84

SCALE:

DWG NO.: VM1018 - 0101 - 00

SHEET 4 OF 14



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Vermont Microsystems Inc.
ONE MAIN STREET, P.O. BOX 388 WINOOSKI, VT. 05404-0388

TITLE 8851 GRAPHICS PROCESSOR
PROGRAMMED I/O

DECIMALS & ANGULAR TOLERANCES NOT SPECIFIED
.XXX +/-.005"
.XX +/-.010"
ANGLES +/- 1

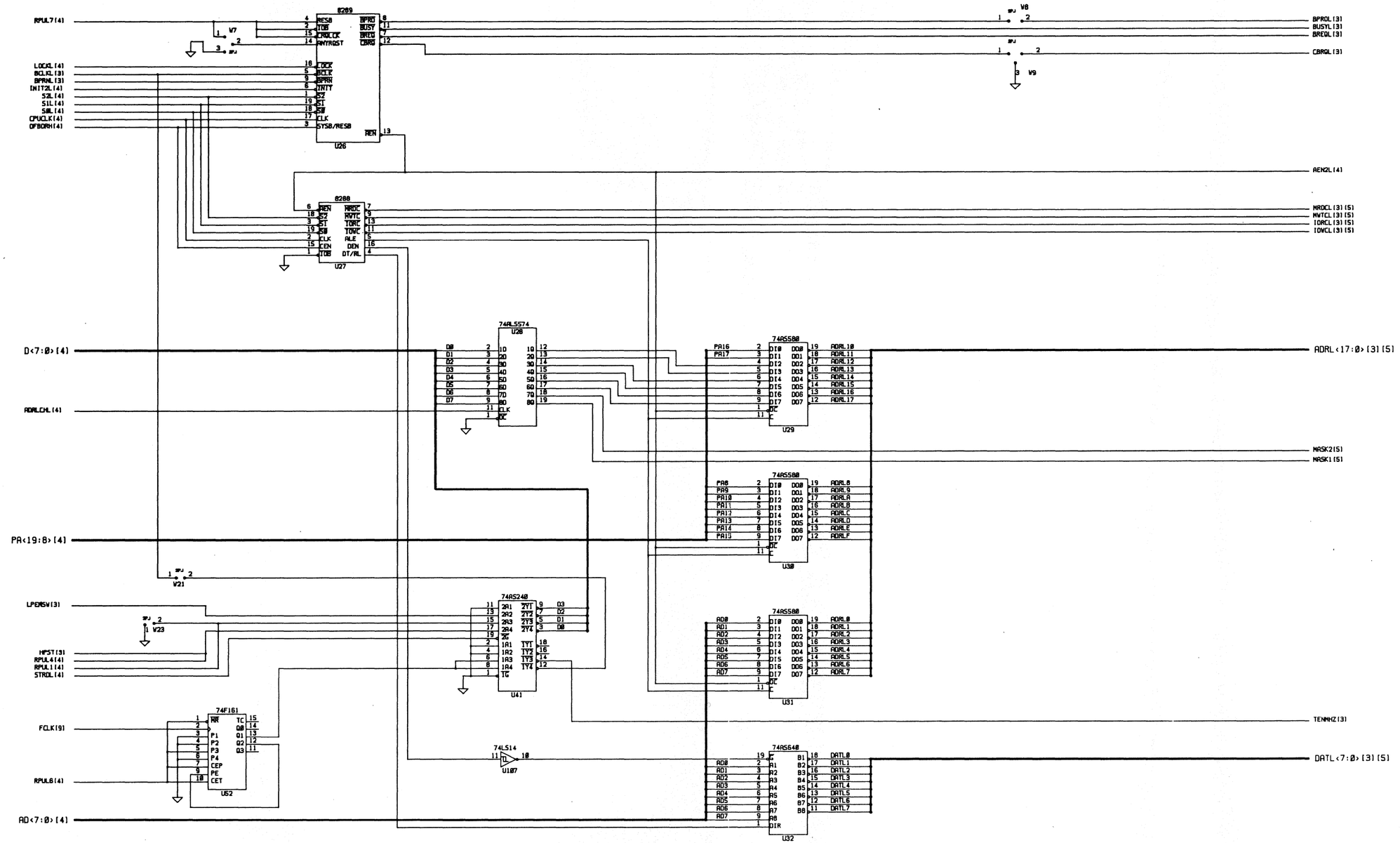
DIMENSIONS IN INCHES UNLESS OTHERWISE SPECIFIED

SCALE

DRAWN H. JONES DATE 27MAR84
CHECKED
APP. BY
DATE

DWG NO. VM1018 - 0101 - 00

SHEET 5 OF 14



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Vermont Microsystems Inc.
ONE MAIN STREET, P.O. BOX 366 WINOOSKI, VT. 05404-0366

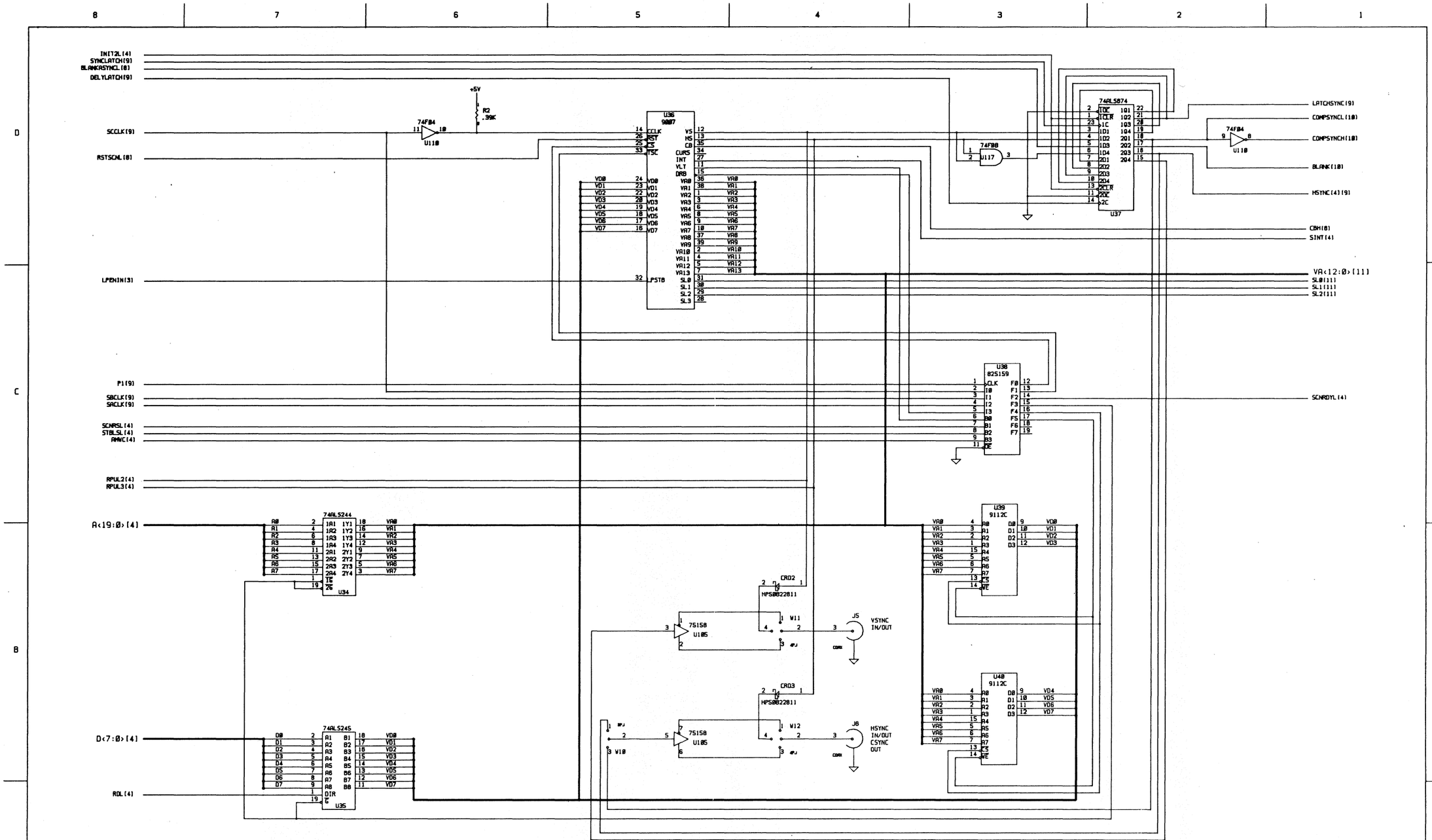
TITLE 8851 GRAPHICS PROCESSOR
MASTER MODE

DRAWN M. JONES 27MAR84
CHECKED
APP. BY
APP. BY

SCALE

DWG NO. VM1018 - 0101 - 00

SHEET 6 OF 14



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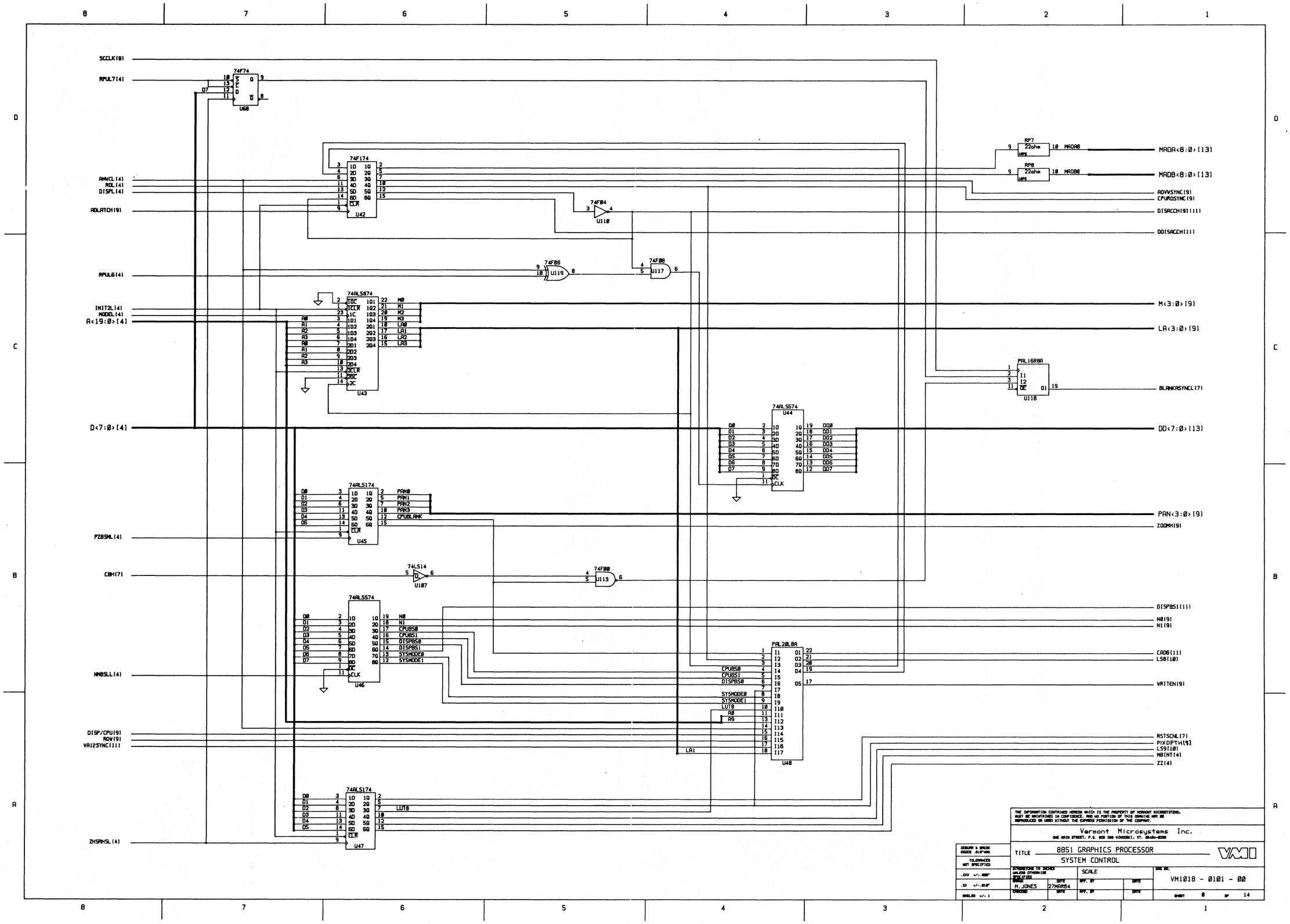
Vermont Microsystems Inc.
ONE MAIN STREET, P.O. BOX 238 WINOOSKI, VT. 05404-0238

TITLE 8851 GRAPHICS PROCESSOR

DRAWN M.JONES 27MAR84
CHECKED
SCALE
APP. BY
DATE
DWG NO. VM1018 - 0101 - 00
SHEET 7 OF 14

DEBURR & BREAK EDGES .010"MAX
TOLERANCES NOT SPECIFIED
.XXX +/-.005"
.XX +/-.010"
ANGLES +/- 1
DIMENSIONS IN INCHES UNLESS OTHERWISE SPECIFIED



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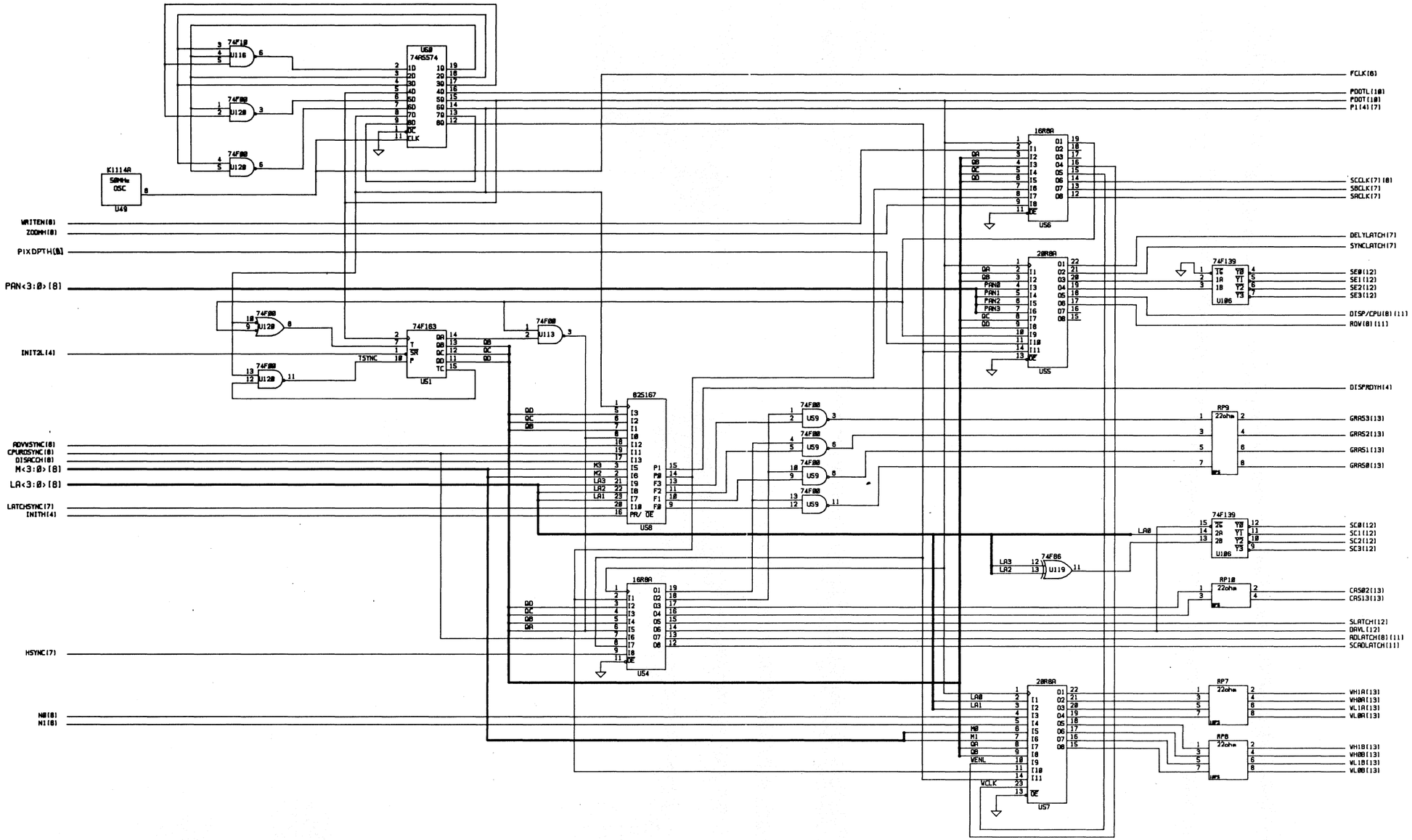
Vermont Microsystems Inc.
ONE MAIN STREET, P.O. BOX 288 WINOOSKI, VT. 05404-0288

TITLE: 8851 GRAPHICS PROCESSOR
SYSTEM CONTROL

DESIGN & DRAW: M. JONES, DATE 27MAR84
CHECKED
APP. BY
SCALE
DWG NO. VM1018 - 0101 - 00
SHEET 8 OF 14



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Vermont Microsystems Inc.
ONE MAIN STREET, P.O. BOX 288 WINOOSKI, VT. 05404-0288

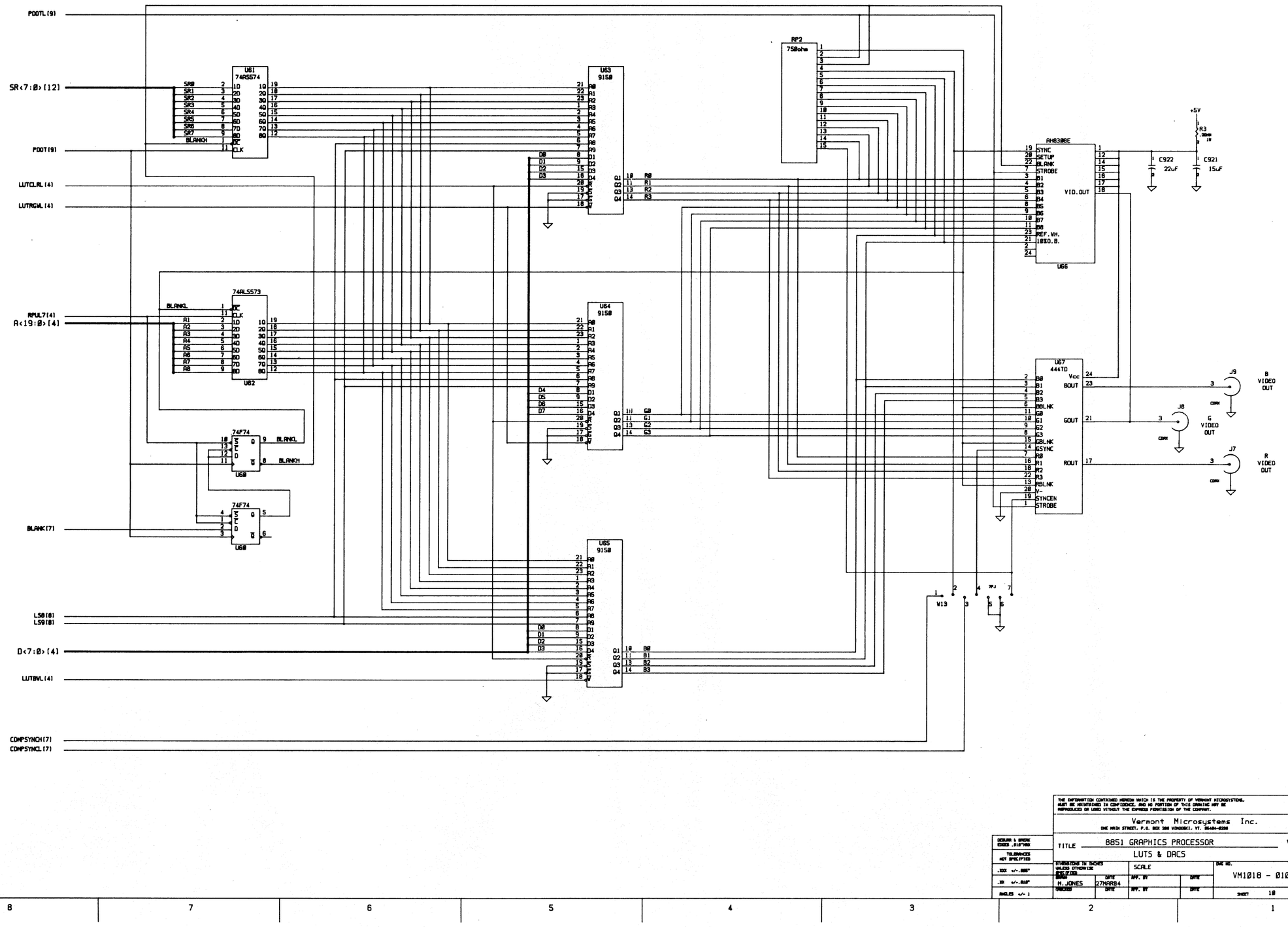
TITLE 8851 GRAPHICS PROCESSOR
TIMING AND CONTROL

DRAWN & SPACE EDGES .015" MIN
TOLERANCES NOT SPECIFIED
.XXX +/-.005"
.XX +/-.010"
ANGLES +/- 1

DIMENSIONS IN INCHES UNLESS OTHERWISE SPECIFIED
DRAWN M.JONES 27MAR84
CHECKED
APP. BY
APP. BY
DATE
DATE
DATE
SCALE

DWG NO. VM1018 - 0101 - 00

SHEET 9 OF 14



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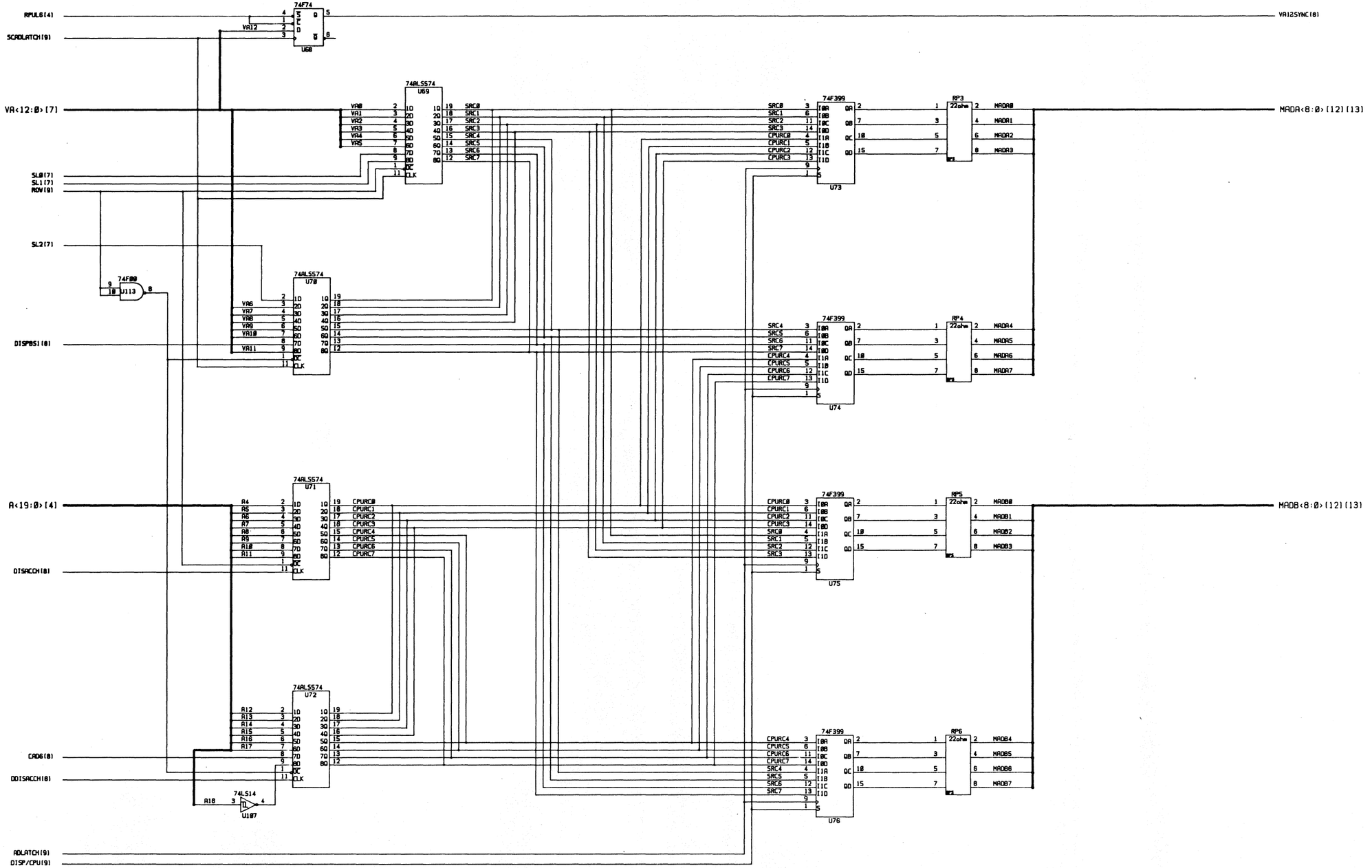
Vermont Microsystems Inc.
ONE MAIN STREET, P.O. BOX 366 WINOOSKI, VT. 05404-0366

TITLE: 8851 GRAPHICS PROCESSOR
LUTS & DACS

DRAWN: M. JONES 27MAR84
SCALE:
DWG NO.: VM1018 - 0101 - 00
SHEET 18 OF 14



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Vermont Microsystems Inc.
ONE MAIN STREET, P.O. BOX 238 WINOOSKI, VT. 05404-0238

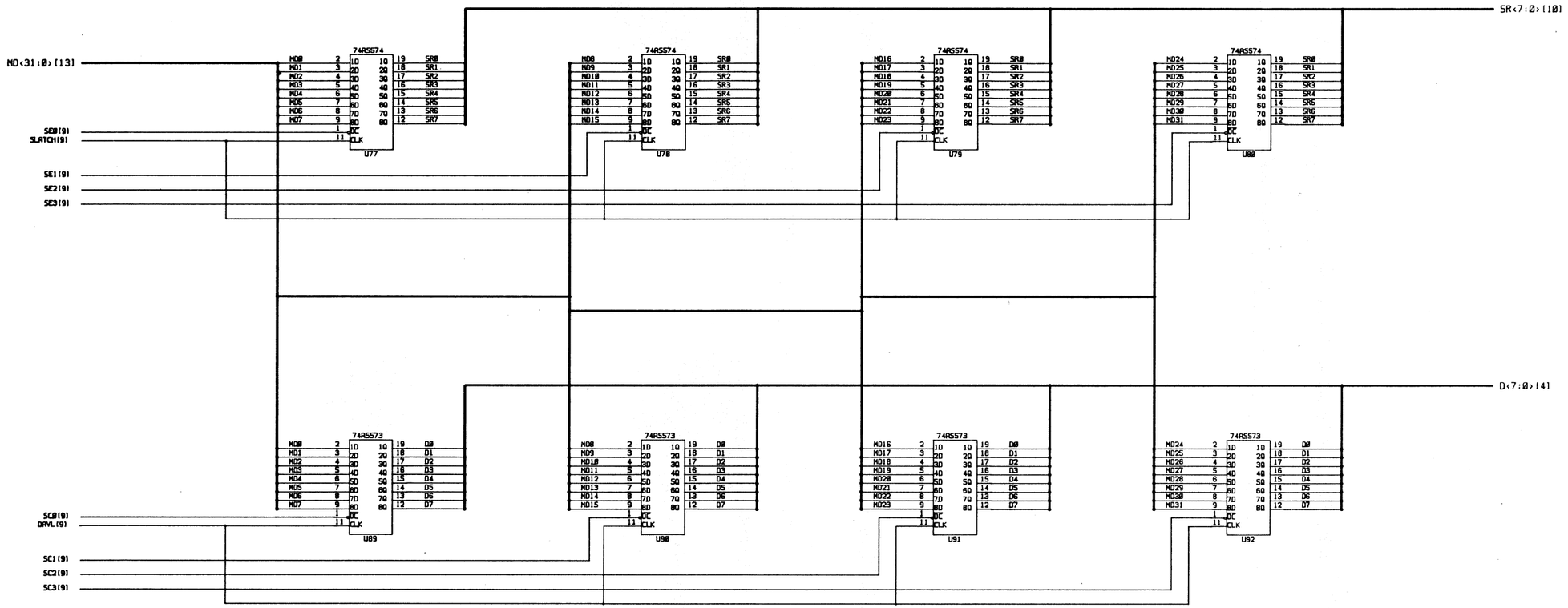
TITLE 8851 GRAPHICS PROCESSOR
RAM ADD GENERATOR

DRAWN M. JONES 27MAR84
CHECKED

SCALE

DWG NO. VM1018 - 0101 - 00

SHEET 11 OF 14



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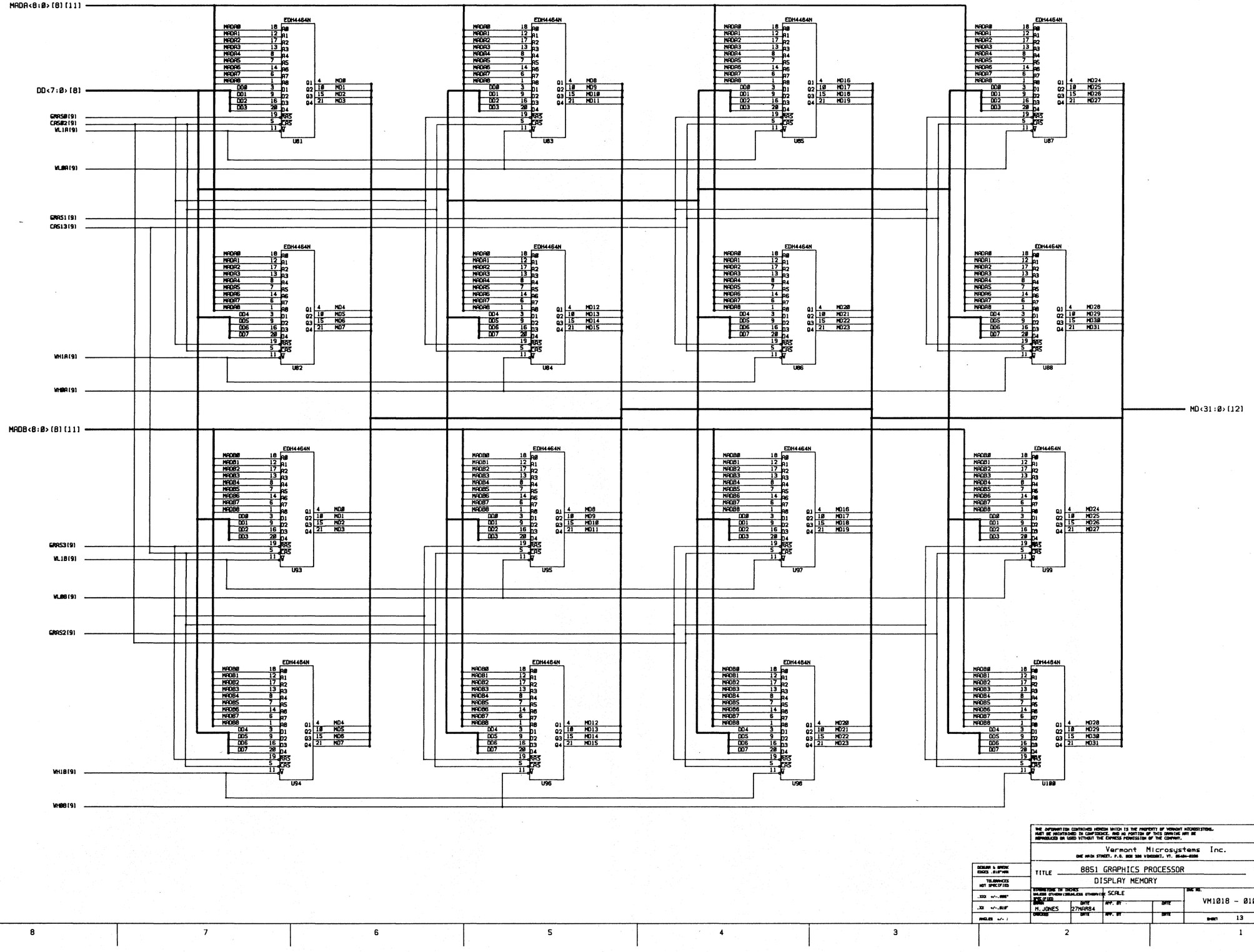
Vermont Microsystems Inc.
ONE MAIN STREET, P.O. BOX 238 VINOOSKI, VT. 05404-0238

TITLE 8851 GRAPHICS PROCESSOR
DATA SELECTION

DRAWN & BROKE EDGES .010"MAX
TOLERANCES NOT SPECIFIED
.XXX +/-.005"
.XX +/-.010"
ANGLES +/-1
DRAWN N. JONES DATE 27MAR84
CHECKED DATE
DIMENSIONS IN INCHES UNLESS OTHERWISE SPECIFIED
SCALE
APP. BY DATE
APP. BY DATE
DWG NO. VM1018 - 0101 - 00
SHEET 12 OF 14



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Vermont Microsystems Inc.

ONE MAIN STREET, P.O. BOX 338 WINOOSKI, VT. 05404-0338

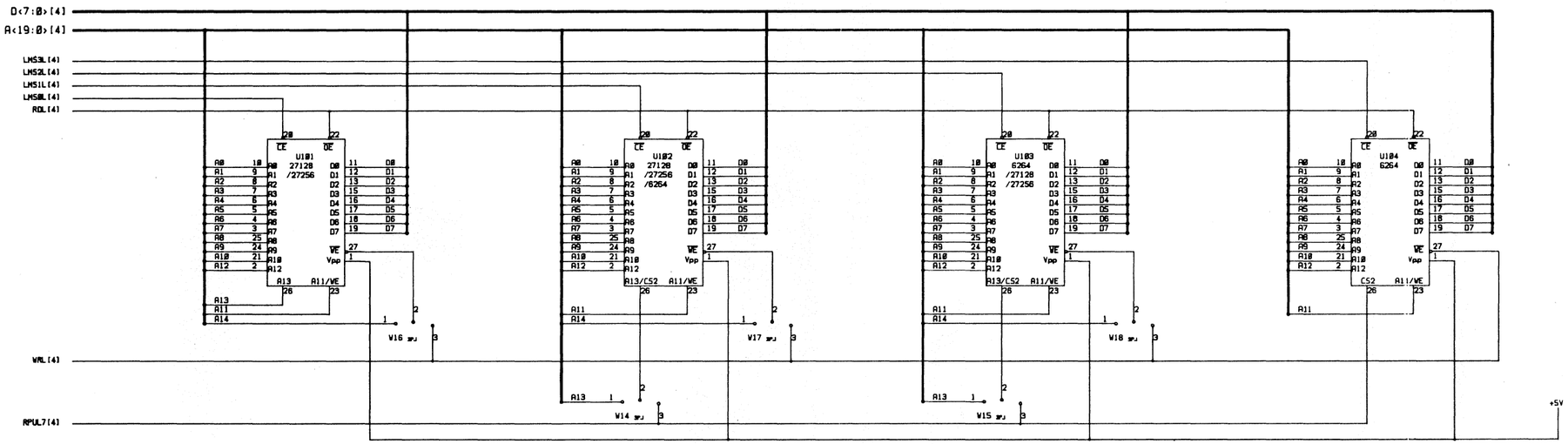
TITLE: 8851 GRAPHICS PROCESSOR
DISPLAY MEMORY

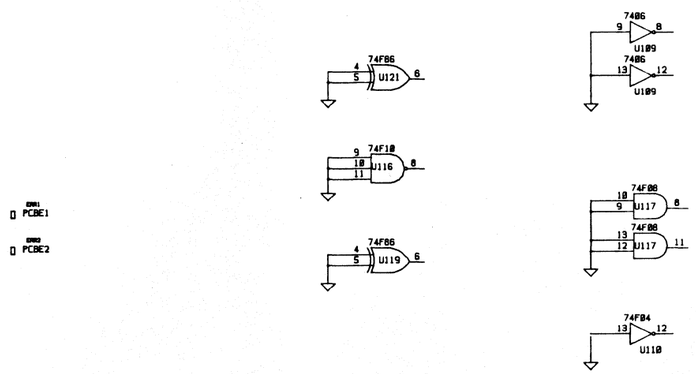
DIMENSIONS IN INCHES
SCALE

DRAWN: M. JONES — DATE: 27MAR84 — APP. BY — DATE
CHECKED — DATE — APP. BY — DATE

DWG NO. VM1018 - 0101 - 00

SHEET 13 OF 14





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Vermont Microsystems Inc.
ONE MAIN STREET, P.O. BOX 388 WINOOSKI, VT. 05404-0336

TITLE 8851 GRAPHICS PROCESSOR
CPU LOCAL MEMORY

DRAWN M. JONES DATE 27MAR84
CHECKED DATE
APP. BY DATE
APP. BY DATE

DIMENSIONS IN INCHES UNLESS OTHERWISE SPECIFIED
SCALE

DWG NO. VM1018 - 0101 - 00

SHEET 14 OF 14

Appendix C

VM-032-00 Color Graphics PCB Parts List

QTY	REFERENCE DESIGNATION	VMI PAkT NO.	MFGR	MFGR PART NO.	DESCRIPTION
3	U59,U113,U120	20500043	FAIR	74F00	QUAD 2-INP NAND
1	U110	20600009	FAIR	74F04	HEX INV.
1	U117	20500053	FAIR	74F08	QUAD2-INP AND
1	U116	20500069	FAIR	74F10	TRI 3-INP NAND
2	U60,U68	20700022	FAIR	74F74	DUAL D F/F
1	U106	20000013	FAIR	74F139	DUAL 1 OF 4 DCDR
1	U51	20500041	FAIR	74F163	SYNC PRE BIN CTR
1	U42	20700011	FAIR	74F174	6-BIT D F/F
1	U52	20900023	FAIR	74F190	UP/DOWN DEC. CTR
4	U73,U74, U75,U76	20500042	FAIR	74F399	QUAD 2 PROT REG.
1	U33	20700023	T.I.	74ALS74N	DUAL D-TYPE F/F
2	U11,U12	20900025	T.I.	74ALS138	3 TO 8 MXR
2	U45,U47	20700024	T.I.	74ALS174	HEX D F/F
2	U21,U41	20200026	T.I.	74AS240	OCT BFFR 3-STATE
1	U14	20200024	T.I.	74ALS240	OCT BFFR 3-STATE
3	U19,U20,U34	20200025	T.I.	74ALS244AN	OCT BFFR 3-STATE

2	U8,U35	20900065	T.I.	74ALS245AN	OCT XCVR 3-STATE
4	U89,U90 U91,U92	20400022	T.I.	74AS573	OCT XPRT D-LATCH
3	U5,U6,U62	20400017	T.I.	74ALS573	OCT XPRT D-LATCH
6	U50,U61,U77, U78,U79,U80	20700009	T.I.	74AS574	OCT D F/F 3-STATE
7	U28,U44,U46, U69,U70,U71, U72	20700008	T.I.	74ALS574	OCT D F/F 3-STATE
3	U29,U30,U31	20400023	T.I.	74AS580	OCT XPRT LATCH
1	U22	20400016	T.I.	74ALS580N	OCT XPRT LATCH
1	U32	20900071	T.I.	74AS640	OCT BUX XCVR
2	U37,U43	20700029	T.I.	74ALS874	DUAL 4-BIT D F/F
2	U107,U108	20200026	T.I.	74LS14	HEX SCHMITT INV
1	U7	20400015	T.I.	74LS75	QUAD LATCH
1	U109	20200001	T.I.	7406N	HEX BUFFR O.C.
16	U81-U88, U93-U100	23300018	EDI	EDH4464N-12-CC4	64K X 4 RAM
2	U101,U102	23100033	INTEL	27128/27256	128K EPROM/ 256K
2	U103,U104	23300024	HIT	6264-12	8K X 8 RAM
2	U39,U40	23300023	AMD	AM9112C	256 X 4 RAM
2	U9,U10	23200002	MMI	PAL10L8CN	PROG GATE ARRAY
1	U23	23200025	MMI	PAL20L8CN	PROG GATE ARRAY
1	U24	23200019	MMI	PAL20L10	PROG GATE ARRAY

2	U54,U56	23200009	MMI	PAL16R8ACN	PROG GATE ARRAY
2	U55,U57	23200020	MMI	PAL20R8ACNS	PROG GATE ARRAY
1	U48	23200021	MMI	PAL20L8ACN-2	PROG GATE ARRAY
3	U63-U65	23300025	AMD	AM9150	1K X 4 STATIC RAM
1	U67	27300006	INTEC	VDAC444TD	VIDEO DAC
1	U1	23000007	INTEL	8088-2	8 MHZ UP
1	U2	20900008	INTEL	8284A	CLK GENERATOR
1	U3	20900069	INTEL	8288	BUS CONTROLLER
3	U4,U13,U25	23200008	SIG	82S153	FPLA
1	U26	20900021	INTEL	8289	BUS ARBITER
1	U27	20900069	INTEL	8288	BUS CONTROLLER
1	U36	20900067	SMC	CRT9007	VIDEO CONTROLLER
1	U38	23200023	SIG	82S159	FPLS
1	U58	23200024	SIG	82S167	FPLS
4	U15-U18	20900068	MMI	67402J	64 X 5 FIFO
1	U105	21200006	T.I.	75158	DUAL LINE DRIVER
1	U49	35000020	MTRLA	K1114A	50 MHZ OSCILLATOR
1	Y13	35000010	CTS	CY24A/MP240	24 MHZ CRYSTAL
67	C1-C8,C10-C18, C20,C22-26,C28, C29,C33-35,C37-C42,C44-C48,C50, C51,C54-C59,C61, C62,C64,C65,C68-C72,C74-C76,C89-C92,C105-C107, C109,C113,C116-C118,C120	32100078	AUX	MD64K	.22uF 25V CER CP

2	U120,U121		KEMET	T330A156M010AS	15uFTANT
1	U123	32100066	PAN	ECC-D2H100KE	10PF 10V DISC
4	U124-U127	32100076	PAN	ECSF1CE226K	22uF 10V
1	CRD1	24000003	MTRLA	1N4001	RECTIFIER
2	CRD2,CRD3		HP	HP5082-2811	DIODE 1 X 6
1	R1		DALE	CCF07103G	10 KOHM 1/42 RESISTOR
1	R2		MEPCO	CR25-390OHM5%	390 OHM 1/4W RESISTOR
1	R3	34100008	DALE	EGS-1-80	.20 KOHM 1W RESISTOR
1	RP1		CTS	750-101-R2.2K	2.2 KOHM (10 PIN SIP)
1	RP2		AB	316A751	750 OHM RPACK (16 PIN DIP)
6	RP3-RP6, RP9,RP10		AB	108B220	22 OHM (8 PIN SIP)
2	RP7,RP8		BOURNS	4310R-102-220	22 OHM (10 PIN SIP)
1	J3	31210110	VIKING	000291001	SBX CONN. FEMALE 18/36 PIN
1	J4	31200122	AMP	641122-3	LIGHT PEN CONNECTOR
5	J5-J9	31300003	MALCO	031-0061-0001	COAX RECEPTACLE
2	W1,W22	39000002	BERG	76151002	JUMP 10 PIN SPCL
1	W2	39000002	BERG	76151002	JUMP 11 PIN SPCL
1	W13	39000002	BERG	76151002	JUMP 7 PIN SIP

11	W5-W7,W9,W10, W14-W18,W20	39000002	BERG	76151002	JUMP 3 PIN
2	W11,W12	39000002	BERG	76151002	JUMP 4 PIN
87	W8,W19, W21,W23	39000002	BERG	76151002	JUMP 2 PIN
2	PCBE1,PCBE2	39100001	SCANB	S-203	PCB EARS
1					CABLE SET (ASSEMBLY)
2		31500005	AUG	540AG37D	40 PIN DIP SKT
4		31500018	AUG	528AG37D	28 PIN DIP SKT
11		31500028	AUG	824AG30D	24 PIN DIP SKT
4			AUG	510-AG90D0-12	12 PIN SIP SKT
44		31500009	AUG	520AG37D	20 PIN DIP SKT
5		31500022	AUG	518AG37D	18 PIN DIP SKT
15		31500003	AUG	516AG37D	16 PIN DIP SKT
12		31500002	AUG	514AG37D	14 PIN DIP SKT
1		31500010	AUG	508AG37D	8 PIN DIP SKT

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Box 236
Winooski, VT 05404
Tel. (802) 655-3800