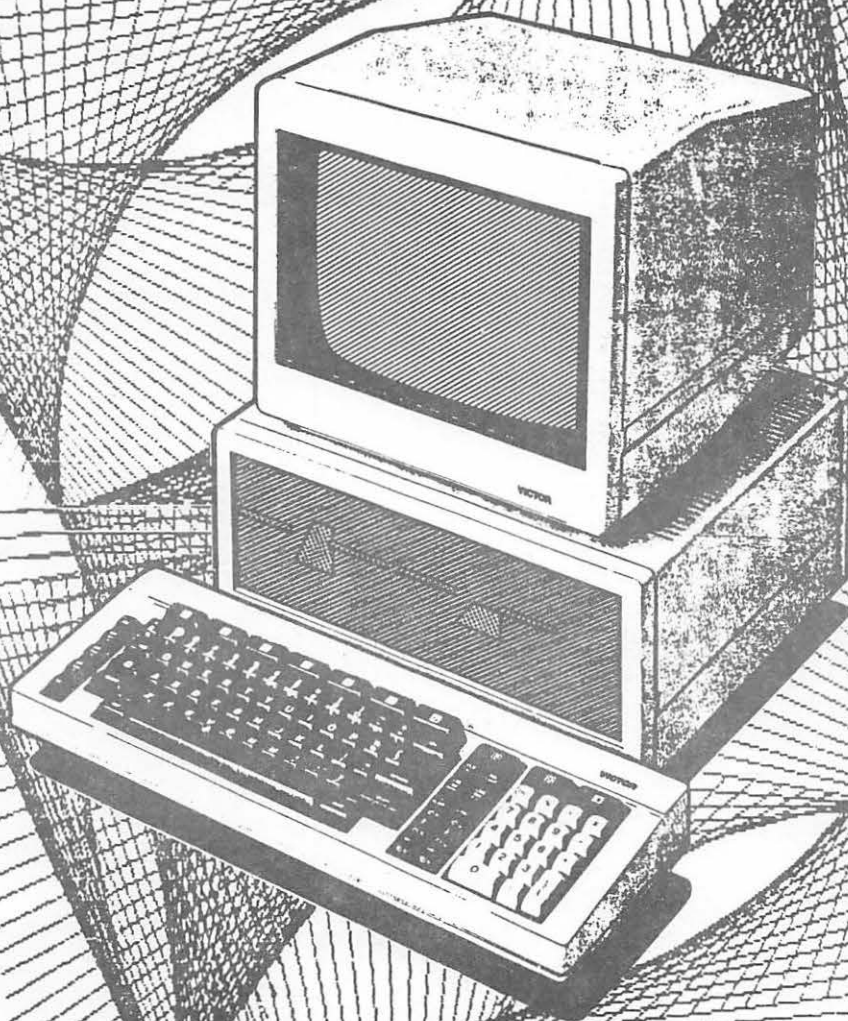# VICTOR

9000

Business Computer

SERVICE MANUAL

Form No. 581-228

READER COMMENTS

Please submit any comments you may have on the Victor 9000 field service manual. These comments will be reviewed by the computer technical support staff. Your input is needed in order to provide the service staff with the best possible reference materials.

SEND COMMENTS TO:

VICTOR BUSINESS PRODUCTS
3900 N. ROCKWELL
CHICAGO,IL. 60618
ATTN: JIM BARLOG
MANAGER
COMPUTER TECHNICAL SUPPORT

Some comments from Jens, who did this scan on February 27th, 2022

I got this service manual from my dad when I was 14 – that was in 1988. Back then, computer literature was expensive, and it was about the only tech reference that I had for the Sirius/Victor 9000.

The manual taught me a lot back then, and it surely contributed to me becoming a hardware designer today. The „Theory of operation" section goes way deeper than any of the already-scanned literature out there (specifically on bitsavers.org).

This scan is not yet complete, as section six is fold-out pages that are twice the size of what I believe is US letter format. These pages are particularly interesting, as they contain hand-written pencil notes from a German engineer/technician who either knew a lot about the machine, or had tech training from Victor (or both). I called my dad a few days ago to hear if he remembers who that might have been, but he doesn't know. His company was mostly a software company, and he rarely ever talked to the hardware guys.

My ScanSnap iX500 scanner is not big enough to eat this page size, and my A3 flat bed scanner died on me years ago (beyond repair – I tried!). The ScanSnap allows scanning A3, but it's a manual process that requires you to put the page into a special transparent envelope. However, this will only produce two A4 scans, and not a full A3 document, so there will always be a line in the middle. Tried it with bad results, stopped after an hour – it's worthless.

If you have a suggestion for a ScanSnap-type scanner that can pull in A3 pages, I'm happy to look at. I have lots of schematics in formats similar to A3 that could be scanned, so I'm willing to spend money if it's as fast as the ScanSnap product.

Contact me:

eMail: jens@icomp.de
twitter: @schoenfeld_jens

Please upload this file to common archives.

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VICTOR 9000 BUSINESS COMPUTER

SECTION THREE ..... THEORY OF OPERATION

SECTION FOUR...FAULT ISOLATION

SECTION FIVE .... CORRECTIVE MAINTENANCE

SECTION SIX .... PARTS CATALOG & SCHEMATICS

* DENOTES TO BE RELEASED

TABLE OF ILLUSTRATIONS

1.0 INTRODUCTION

The 9000 is VICTOR's answer to the markets need for a state of the art, leading edge in technology, desktop computer. Equipped standard in the unit are two 5 1/4 inch floppy disks,4 output ports,a flicker free display and 128K of memory, with the built-in capability to expand the basic unit to 896K of memory within minutes.

Field Personnel will appreciate the value of Boot routine diagnostics,components laid out in a mapped routine, and the capability of disassembly with only one phillips screwdriver.

In an effort to aid Field Personnel with troubleshooting and repair of the VICTOR 9000, this manual has been divided into six (6) basic sections:

        1.)   INTRODUCTION
        2.)   HARDWARE CONFIGURATION
        3.)   THEORY OF OPERATION
        4.)   FAULT ISOLATION
        5.)   CORRECTIVE MAINTENANCE
        6.)   PARTS CATALOG

The Theory of Operation section gives a detailed description of the operation of the unit down to the signal and component level. All information pertaining to the operation of the unit that the Field Engineer would need to troubleshoot the system has been included in a format that will greatly aid the Engineer both at the customers site and at the bench.

The Fault Isolation section gives the Field Engineer the necessary information to properly diagnose a hardware problem at any location in the system.

The Corrective Maintenance section gives proper procedures to follow in the event a component or section of the unit should malfunction.

The Parts Catalog section of the manual gives a complete illustrated view of the system with both part numbers and assembly numbers.

VICTOR 9000 TECHNICAL SPECIFICATIONS

INPUT VOLTAGE: 115V 60HZ
                                        220V 50HZ

SIZE: Mainframe   11 x 13 x 12.5
                CRT   7 x 13 x 16.5
                Keyboard   19 x 6.5 x 2

WEIGHT: 51 LBS.

MEMORY: 128KB DYNAMIC
Upgrade capacity   896KB DYNAMIC

DATA STORAGE:
5 1/4 Floppy disks   1.2 MEGABYTE
Single sided,double density   80 TRACKS

UPGRADE CAPACITY:
Double sided   2.4 MEGABYTE

An optional 10MB Winchester disk drive can be added to
the system

EXPANSION CAPABILITY: 4 Expansion slots

INPUT/OUTPUT

    TWO RS232 Communications ports with standard
    DB25 type connectors

    A. Synchronous: support-software programmable
       for internal programmable or external clock,
       1200 to 9600 bits per second, and BI-SYNC
       and SDLC line protocols supported.

    B. Asynchronous: support- software programmable
       bit rate, 75 ot 9600 bits/second.

ONE PARALLEL: I/O port-supports centronics,
    Qume,Diablo, and full IEEE-488 interface
    under software control.

1 USER PORT

CPU:

INTEL 8088 CENTRAL PROCESSING UNIT   (8/16 BIT)

DISPLAY:

80-CHARACTER BY 25-LINE STANDARD, loadable (RAM)
character generator with up to 2048 different
characters.

Graphics: 800 x 400 dot matrix
Character size: 10   X 16   dot matrix
High resolution: 16 x 16 dot matrix

KEYBOARD:

Programmers,Word processing,Standard
104 keys, 10 software definable keys,
calculator pad

2.0 HARDWARE CONFIGURATION

This section provides a technical overview to the Victor 9000 computer. An indepth explanation of each of the structures that make up the microcomputer will be presented in the theory of operation section of this manual.

The Victor 9000 computer is comprised of three modules, each connected by a cable. The CRT module, provides display; the keyboard module provides user entry; and the mainframe module provides all computation and data storage.
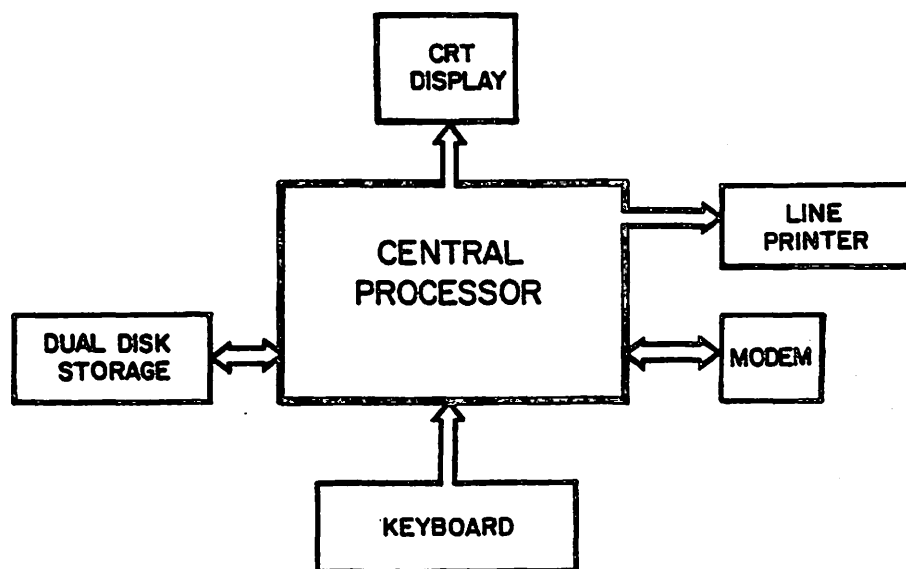
VICTOR 9000 SYSTEM BLOCK DIAGRAM

Figure 1

KEYBOARD MODULE

The keyboard module is a single printed circuit board containing 104 capacitive switches, two LSI matrix chips, and an 8021 microprocessor chip. The microprocessor scans the key switches via the matrix chips and transmits an 8 bit switch code along with a stop bit to the keyboard interface on the CPU board. 7 bits represent the actual switch code while the 8th bit determines whether the key had been pressed (closed) or released (open). The microprocessor chip also contains an 8 byte buffer which allows it to store up to 8 switch changes. The keyboard microprocessor uses a control signal to notify the interface when a key change is in its buffer.

The keyboard communicates with the CPU over a 7 wire cable connected at J6. The required +5 volts is provided by the cable.

The keyboard interface acknowledges the request by the keyboard to transfer in a character with an acknowledge control signal. When the character is received by the keyboard interface, it will generate an interrupt to the 8088 microprocessor and the 8088 will enter an interrupt service routine to transfer the character into memory.

CRT MODULE

The CRT module consists of a 12" CRT and yoke assembly, a video control board, and a video interface board. A regulated +12 volt power is provided to the display subsystem by the power supply in the mainframe unit.
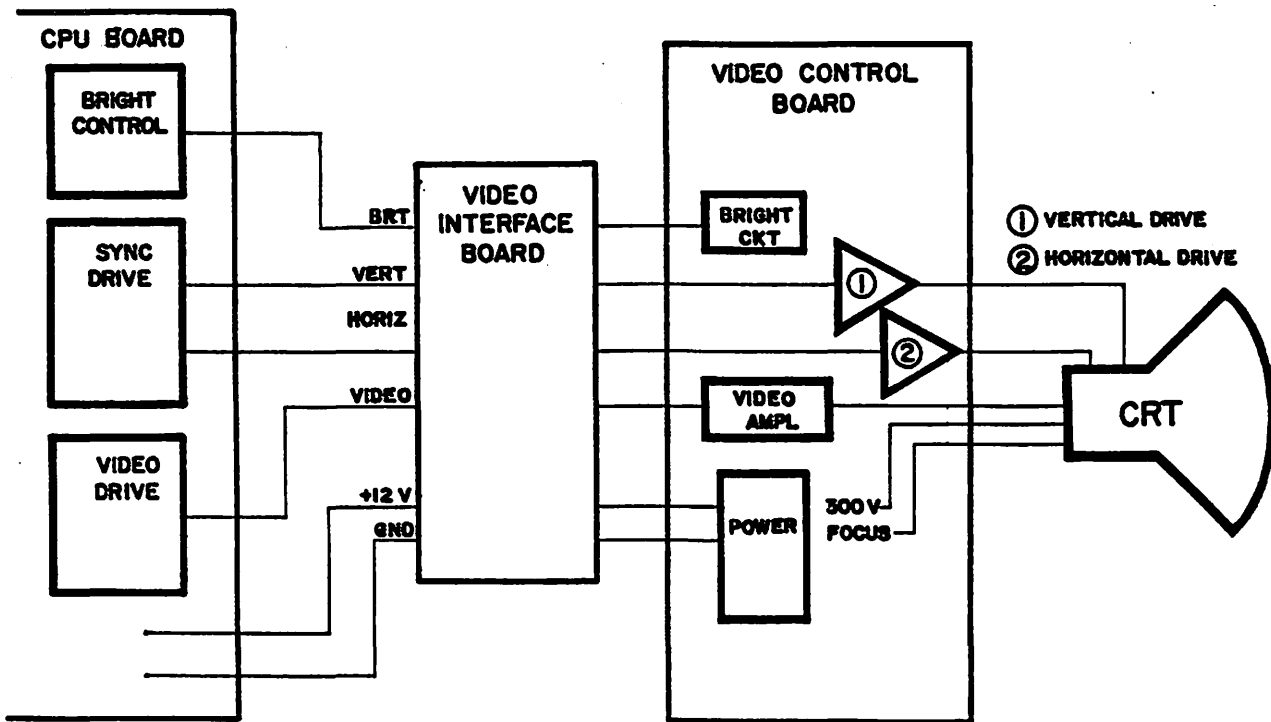
CRT DISPLAY SYSTEM BLOCK DIAGRAM

Figure 2

2-2

The video control board provides the necessary 12KV to drive the tube, horizontal and vertical synchronization, brightness control and video control. The horizontal and vertical sync originate on the CPU board and provide timing control for the video control board. The horizontal and vertical signals deflect the beam across and down the screen while the video signal turns the beam on and off. The video signal waveform is the converted digital bit pattern stored in memory for each character.

The video control board uses an integrated circuit Vertical Deflection Amplifier to control the beam. The vertical sync signal provides the input to the vertical deflection amplifier.

The display subsystem utilizes a resistor network with digital control bits to provide 8 levels of brightness and contrast from a keyboard entry. The brightness is set by the resistor network on the CPU board then routed to the video control board. The master brightness is controlled by a potentiometer on the video board. The board also contains adjustments for focus, vertical hold, vertical size, vertical linearity and horizontal size. Adjustment procedures for the video control board can be found in the fault isolation section of this manual.

The CRT display subsystem is controlled by a single HD46505 CRT controller chip located on the CPU board. This chip provides all memory address and sync timing requirements for a CRT display. The 46505 has direct access to screen memory and system memory for CRT character generation. The CRT interface circuits receive the character words from system memory and convert them into a video control waveform.

During the boot operation the CRT controller chip registers are initialized to control the CRT display. They can be altered via software to change the display mode (i.e. graphics).

MAINFRAME MODULE

The mainframe module contains: the dual disk drive subsystem, power supply and the central processor board (CPU).

Power to the Victor 9000 is provided by a high efficiency switching supply. The power supply provides: +5, +12 and -12 volts regulated, along with an unregulated +12 volt.

The power supply operates at a switching rate of 25-30 KHZ.

The power supply can be configured to operate at either 110 or 220 VAC by the placement of a jumper on the board. It also has a range of between 47 Hz to 63 Hz. The input fuse is rated at 5 amps.

Power cabling consists of one cable to the CPU board and another cable to the disk drive controller board.
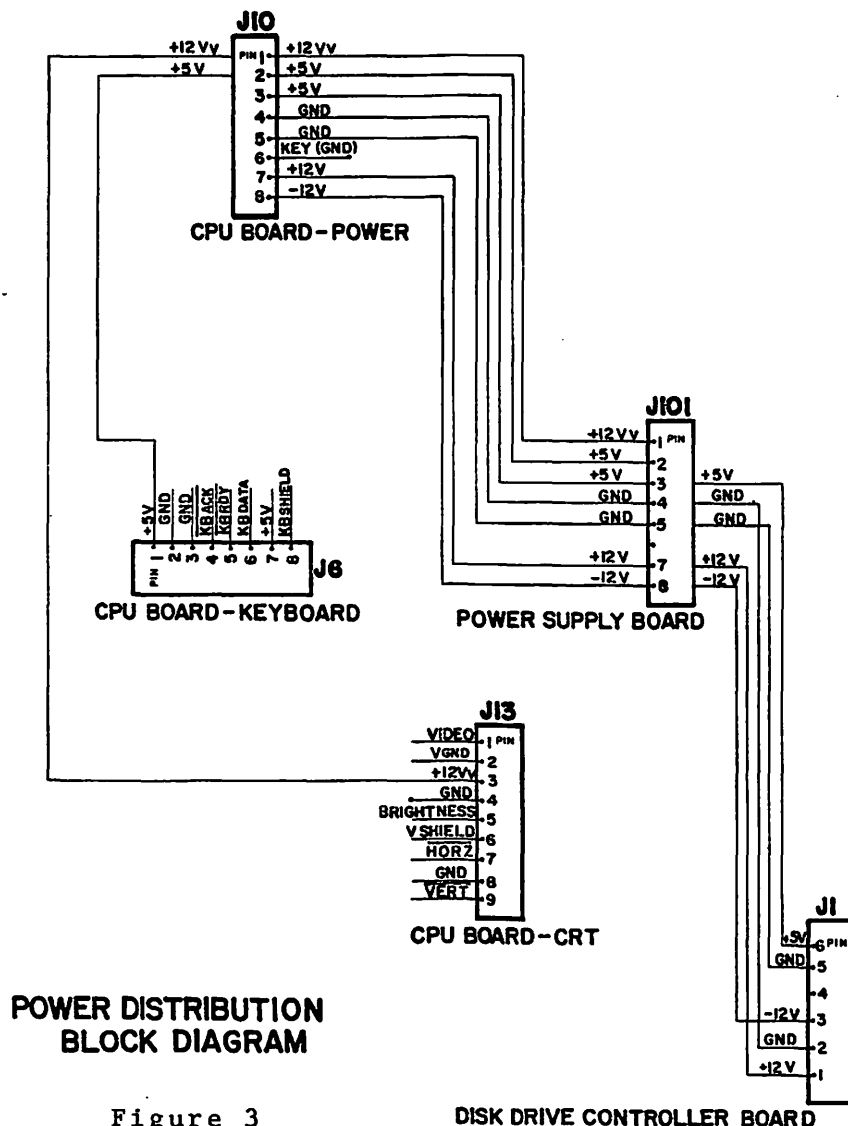
POWER DISTRIBUTION BLOCK DIAGRAM

Figure 3

DUAL DISK DRIVE SUBSYSTEM

The dual disk drive subsystem provides either 1.2 Mbytes on single-sided or 2.4 Mbytes on double-sided double density 5.25 inch floppy diskettes. The subsystem is composed of two identical disk drive units, and a disk drive controller board. All electronic functions are accomplished on the controller board.

The disk drive subsystem requires four functions to accomplish data storage and retrievel. They are seek, write, read and speed control.

The seek logic positions the read/write head over the desired track. Once in position a read or write sequence can be performed. This function is accomplished by use of a Versatile Interface Adapter chip (VIA), a set of driver chips, and a four phase stepper motor located on the drive assembly. During a format operation the sector header will be written with the track and sector number. A header search is performed before a read/write operation can occur. The headers will be read by the system to determine when the desired sector passes under the head.
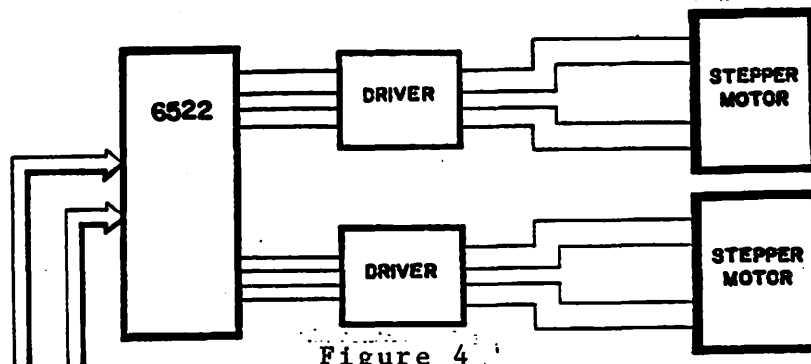
Figure 4
SEEK CONTROL

Motorspeed control is accomplished by an 8748 microprocessor chip, a digital to analog converter chip, a motorspeed driver chip and a DC motor on the drive assembly. The diskette is divided into 8 speed zones, each having a speed calculated to maintain a constant linear velocity for the media as it passes under the head. This design allows for constant bit density throughout the entire surface of the diskette.

6522   8748   DAC   DAC   SPINDLE MOTOR   SPINDLE MOTOR

A∅-A3
ID∅-ID7

MOTOR SPEED CONTROL
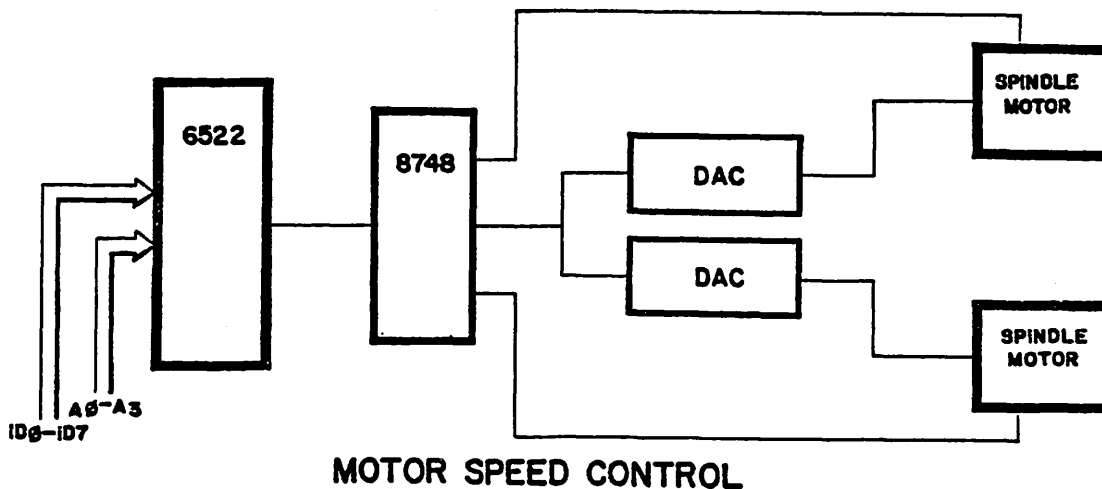
Figure 5

The DC motor contains a tachometer that provides a speed feedback to the 8748. The microprocessor chip will monitor the incoming tach pulses and increase or decrease its speed byte output to maintain the desired speed.

The number of sectors per track increases as the physical size of the track increases. The tracks are organized with track zero at the outer edge and track 80 at the inner edge. Track zero will contain 19 sectors while track 80 will contain 12 sectors. The sectors per track will increase by one as the head moves from one speed zone to the next, going from the inner tracks to the outer tracks.

The write function is accomplished by use of the Group Code Recording (GCR) method of data storage and retreivel. In a GCR system the data byte is converted into a code and the code is stored on the media. When the data is to be retreived, the code is read from the disk, converted back to the data byte, then transferred to the computer. These functions are accomplished in the controller logic for the disk drives. The use of GCR allows the data to be retreived in a self clocking mode which maximizes use of media space. The table 1 on page 2-7 defines the GCR code for each nibble in a data byte.

The GCR codes are contained in a ROM on the controller board. Each time a byte of data is to be written it will first be converted by the logic to the GCR code. The code is then serially written onto the media as it passes under the head.

GROUP CODE RECORDING

BINARY		GCR
0000	0	01010
0001	1	01011
0010	2	10010
0011	3	10011
0100	4	01110
0101	5	01111
0110	6	10110
0111	7	10111
1000	8	01001
1001	9	11001
1010	10	11010
1011	11	11011
1100	12	01101
1101	13	11101
1110	14	11110
1111	15	10101
SYNC		11111

Table 1

The controller board contains a write current source that records a magnetic flux onto the diskette when data is written. The diskette can be protected by a write protect switch in the drive assembly that removes the write current from the heads when a diskette is write protected.

A door open switch in the drive signals the system when a diskette has been inserted into the drive.
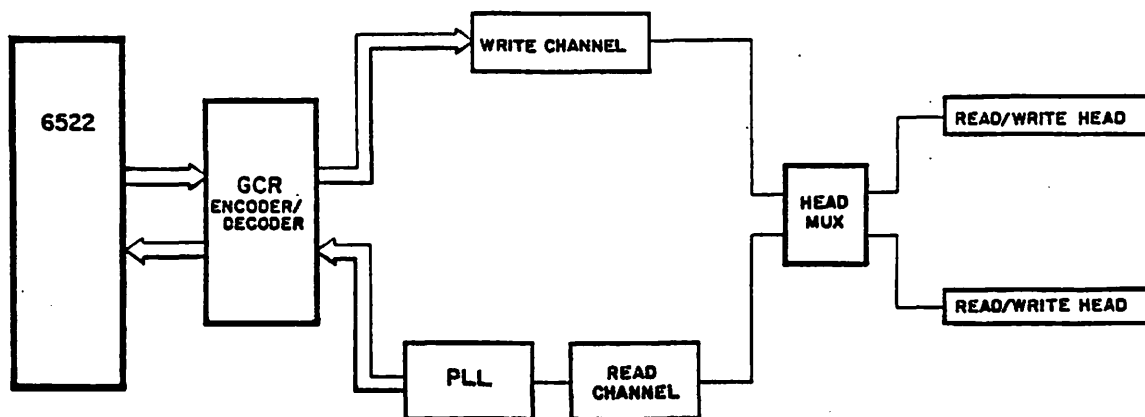
DISK DRIVE READ/WRITE SYSTEM

Figure 6

The read recovery logic on the controller board provides a self-clocking method for the retrievel of stored information. The read logic is composed of a read preamplifier, a phase lock loop and a GCR decoder.

The read preamplifier senses the 10 millivolt signal generated by the flux reversals stored on the media. When the read head is selected it will pass the changes into an amplifier circuit that filters, amplifies, then digitizes the signals. These signals enter a phase lock loop where they are clocked by a Voltage Controlled Oscillator (VCO). The phase lock loop samples the rate at which the pulses are read from the disk and generates a clock at the same rate as the data to insure synchronization during read recovery. The clock and data pulses are then routed through the GCR decoder where they are converted back into the data byte. This byte can then be transferred to the computer.

A sync code is written at the beginning of a sector header and again at the beginning of a data block. This provides the necessary read signal to lock the phase lock loop in and allow the processor to identify whether the information to be read will be sector identification or data.

CENTRAL PROCESSOR BOARD

The central processor unit is composed of the 8088 microprocessor, memory (system, screen and boot) and the Input/Output structure. All input/output for the system is controlled by the 8088.

The internal architecture of the 8088 is divided into two units: the Execution Unit, where all data manipulation takes place; and the Bus Interface Unit, which controls all transfer of data or instructions between the system and the 8088. The execution unit has 16 registers which may be byte or word addressed. The 20 bit address bus allows the 8088 to address 1 MByte of memory. A 4 instruction "Instruction Queue" allows the 8088 to prefetch instructions and minimize memory access wait time. The memory addressing structure utilizes a segment register, which combined with an address displacement in the instruction, provides a 20 bit memory reference address. The 8088 utilizes 6 different modes for memory addressing.

Data is transferred to and from the 8088 over a multiplexed 8 bit data bus. This bus is shared by 8 bits of the 20 bit address bus. Word transfer is accomplished by accessing two consecutive memory bytes.
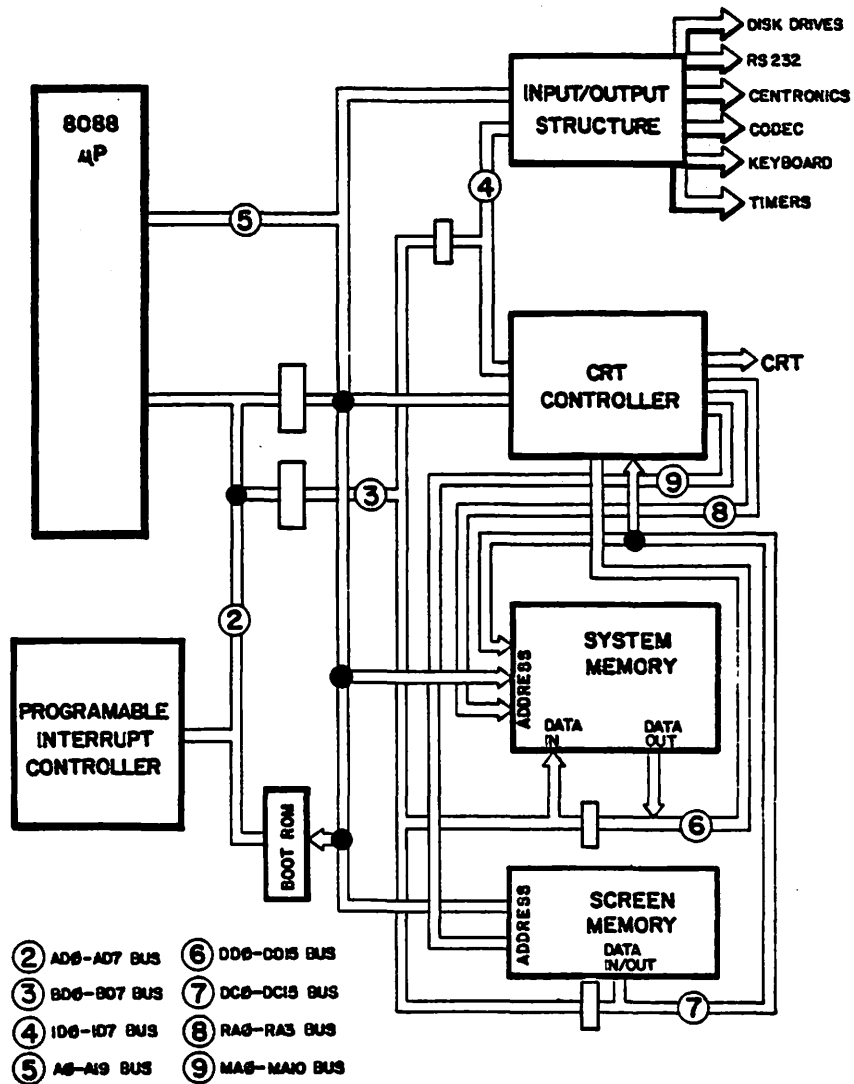
Figure 7

Timing for the 8088 is provided by a 5 MHZ clock generated by a divider network for a 15 MHZ master clock. The MPU clock uses a 40% on and 60% off duty cycle.

MEMORY

The memory section of the CPU board is divided into three sections: System memory, Screen memory, and Boot memory.

System memory is a dual port memory composed of 128K bytes of storage capability. It can be upgraded with memory expansion boards to 896K of memory. Both the 8088 and the CRT controller have direct access to system memory. All input/output device controllers access memory through the 8088. The memory arbitration circuit controls processor and CRT access to memory. It will hold the processor in waiting while a CRT memory access is in progress and likewise, hold the CRT in waiting when a processor memory cycle is in progress.

System memory utilizes the 64K x 1 dynamic RAM chips which require periodic refreshing. The refresh circuitry guarantees that all memory locations will be refreshed within the 2 msec requirement.

System memory contains user programs, data blocks, the fundamental modules of the operating system and the character fonts for CRT character generation. The CRT accesses memory to address the character dot patterns for character generation on the display.

Screen memory is 2K words of static RAM used specifically for storing the character pointer for the CRT display subsystem. The CRT ciontroller chip accesses a screen memory location for each character cell on the display. In the memory location will be an address pointer for the dot pattern in system memory of the character to be generated. The dot pattern is composed of 16 consecutive words in system memory. The screen memory data word will be the address for the first dot pattern location. The character pointers are loaded into screen memory by the 8088 and are systematically read from the memory by the CRT controller chip.

The screen memory also contains the character attributes. A character attribute identifies the type of character generation to be processed. The character attributes are: Reverse Video, Underline, Secret,and Low Intensity. One bit of the character attribute is uncommitted.

Boot memory is composed of 8K byte of Read Only Memory (ROM). This memory contains CRT, keyboard, and disk drive initialization software; self test routines; and the bootstrap loader to bring the operating system in off the diskette. The bootstrap will boot the system from either the A or B drive.

Boot memory is accessed by the 8088 only. When power is applied or the reset signal on the 8088 goes active, the 8088 will address the boot memory. At this time all previous memory contents will be lost and the entire microcomputer logic will be set to an initialized state.

When a failure is detected by the self test routines in the Boot memory an error code will be displayed on the screen. This error message will aid in isolating faults in a system where the diagnostic diskette fails to load into the system.

Bootrom error codes

01- No sync pulse detected
02- No header track
03- Checksum error in header
04- Not right track
05- Not right sector

06- Not a data block
07- Data checksum error
08- Sync too long
99- Not a system disk

INPUT/OUTPUT ORGANIZATION

The input/output structure is composed of programmable peripheral controller chips, a memory-mapped I/O structure and a Programmable Interrupt Controller (PIC). The I/O contains a parallel port, two serial ports, programmable User port, Codec, disk drive interface, keyboard interface, and CRT controller interface.

The parallel port consists of a 6522 Versatile Interface Adapter chip and two driver chips. It can be configured as a standard Centronics parallel or an IEEE-488 interface. The VIA is programmed by the 8088 for data transfers.

The two serial ports are controlled by a single Multi-Protocol Serial Communications Controller chip. This chip can handle async, bisync, SDLC and HDLC communications protocols. It is programmed by the 8088 for data transfers. It uses a variable baud rate from 110 bps to 19.2K bps which is set up through a Programmable Interval Timer chip. The clocks generated by the timer chip provide the transfer clocks for the baud rates.

The programmable User port is a 6522 that is connected directly to an I/O connector. It can be programmed by the 8088 to handle 8 bit parallel transfers.

The Codec, voice digitizer, provides for voice input through a microphone and preamplifier. The digitized voice can be stored on a diskette and played back through the internal speaker. The circuitry for the codec, with the exception of the microphone and preamplifier, is contained on the CPU board.

The disk drive interface, CRT interface, and keyboard interface are programmed by the 8088 via the I/O bus.

In order to free the 8088 from device polling software routines a Programmable Interrupt Controller is employed. The PIC allows the 8088 to deviate from its program only when a peripheral device requests service. When a device needs service it will send an interrupt request to the PIC. The PIC will then relay the request to the 8088. At the end of each instruction the 8088 will examine the interrupt request line for the presence of an interrupt request. If present, it will read in an interrupt pointer from the PIC which will direct it to the memory location of the interrupt service routine. The interrupt service routine will handle the demand for peripheral service (i.e. keyboard character entry).

The PIC is initialized by the 8088 during the initialization sequence. At that time the interrupt byte pointers are loaded into the control registers of the PIC.

The memory mapped I/O structure allows greater flexibility in addressing peripheral devices. In a memory mapped I/O each device is assigned a dedicated block of memory. Whenever that memory space is accessed information will be transferred to or from the device. In an I/O mapped system each device is assigned a device code. To access a device the processor utilizes the code in conjunction with an IN or OUT instruction. In the memory mapped system a device is accessed whenever its memory address space is placed on the bus. Effective transfers take place whenever a LOAD,MOVE,STORE, OR, AND instruction is executed with the appropriate memory address space.

SECTION THREE....THEORY OF OPERATION

Top section (rectifier / regulator):

F101 · D101 IN4004 · D102 IN4004 · THR101 · D103 IN4004 · D104 IN4004 · 3 (CUT FOR 220V)

C101 100 200V · C102 100 200V · C105 100 200V · C106 100 200V · C109 .0047, 3KV.

R101 240K 1/2W · R102 39K 1/2W · R108 240K 1/2W · R109 100K · D108 IN988 130V · D109 IN988 130V

R104 75 1/2W · R103 62 1/2W · D105 IN914 · C103 33, 10V. · A101 1/2 · R110 2K · D107 IN914 · R111 100 · R113 100 · C110 .01 100V

Q101 SU374 · C107 .1 25V · R112 100 · Q102 2N2219

R106 1 · R105 470K 1/2W · Q103 SJ6942 · D110 IN4004 · R114 1.3 1/2W · C111 4.7 10V

R107 33 5W · D106 IN4936 · C108 .0033 600V · C104 .1 400V

Lower section (output regulators):

L101 065 · D112 MR2400F/2401F · C112 1000 10V · C113 1000 10V · C114 1000 10V. · C115 2200 10-16V · R115 1K

D111 IN4733 · R116 100 · R117 1K · R118 1K · 1/2 A101 · +5

L102 155-5601 · D115 80SQ035 · C116 470 25V · C118 220 25V · R119 240 · Q105 2N3904 · Q106 2N3904 · Q104 2N3906 · R125 82

L103 155-5601 · D118 80SQ035 · C119 330 16V · C120 220 25V · R127 1K · D120 IN4743 · R122 680 · R123 150 · R124 150 · R126 3K

R121 10 · D116 IN4004 · R133 10 2W · +12

R129 15 · A103 C122F · A102 · A104 · D117 IN4004 · C121 2.2 16V · +12 REG

L104 155-5601 · D121 MR851 · C122 220 25V · C123 220 25V · R132 1K · C124 2.2 16V · D119 IN4004 · -12

Notes:

4 REF COMPOWER CORP. CP-5102 SCHEMATIC. DWG NO 90017.
3 CUT FOR 220V OPERATION
2. ALL RESISTORS ARE ±5%, 1/4W.
1. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS AND MICROHENRIES.

3.1 POWER SUPPLY

The power supply for the VICTOR 9000 is a switching type supply. It develops four DC outputs: +5 volts, two +12 volt outputs and a -12 volt output. Over-all feedback is used to regulate all outputs by sensing the +5 volts. One of the +12 volt outputs (+12vv) also has an independent series regulator, as does the -12 volt output.

1. RECTIFIER/VOLTAGE DOUBLER

The input voltage (115 VAC) is fullwave bridge rectified by diodes D101-D104 developing, through the voltage doubler circuit C101,C102,C105,and C106, a filtered 330 VDC (Unregulated). R101 and R108 are load resistors for the circuit. THR101 is a thermo resistor used as a current limiter to protect C101,C102,C105 and C106 from surge charges. The circuit is protected by a 5 amp fuse, F101.
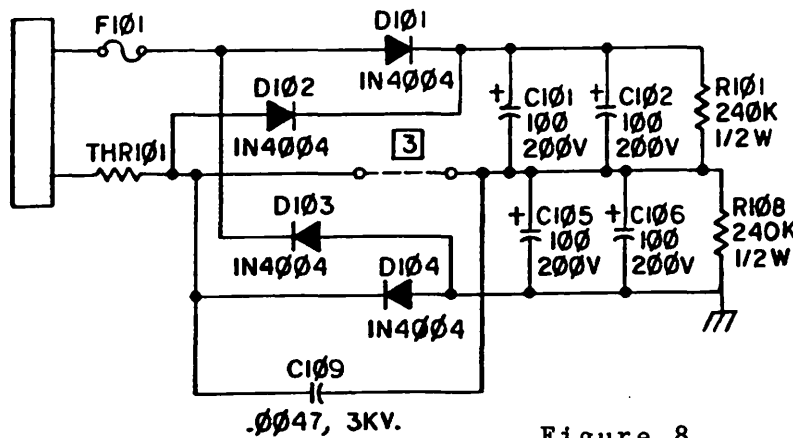
Figure 8

2. OSCILLATOR CIRCUIT

As the source voltage, 330VDC (Unregulated), is applied to the circuit C103 charges through R104, R103 and R105 turning Q103 on. With Q103 on, a current is passed through R114, Q103, and T1 pins 9 and 10. This current induces a voltage across T1 pins 9 and 10, which serve as the primary coil for the four secondary coils: T1 pins 1 and 2, 3 and 4, 5 and 6, 11 and 12, respectively. The bases of Q101 are labeled as B1 and B2. B1 is the base connected to D105, B2 is the base connected to R112. C107 charges through D105, R103, C103,and R105, keeping B2 of Q101 at the proper potential.

3-1
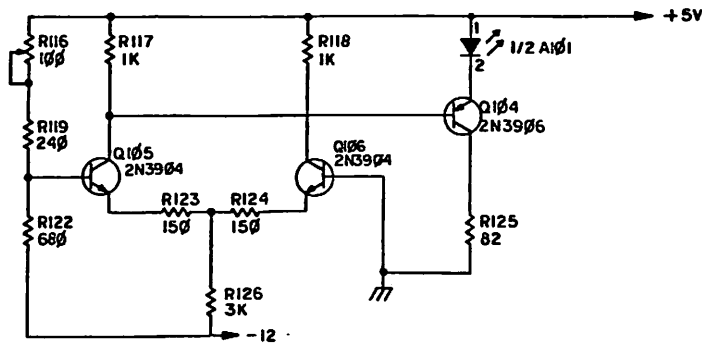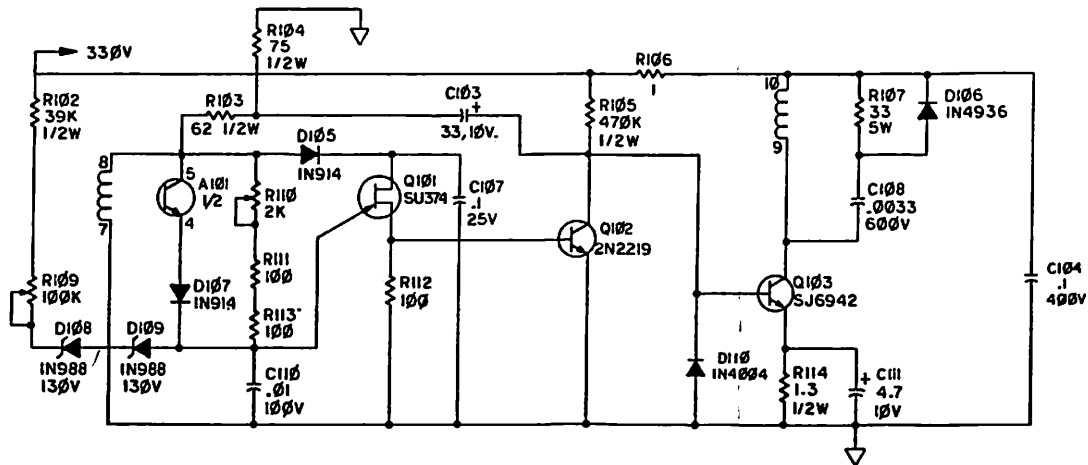
Figure 9

As C110 charges through R113, R111, R110, R103, C103 and R105 it developes the voltage potential to turn Q101 on. With Q101 being on, E-B1 and R112 provide a discharge path for C110. A voltage drop is then developed across R112 providing the necessary voltage potential to turn Q102 on. By turning Q102 on, Q103 is turned off. With Q103 turned off, the current flow through T1 pins 9 and 10 is stopped. D106 is used as a protection against back EMF. As C110 is discharging, the voltage potential on the emitter of Q101 becomes less. When that voltage potential can no longer sustain the bias required for the conduction of Q101, the E-B1 discharge path is broken and the charging cycle repeats.

When C103 is fully charged, the polarity of T1 pins 7 and 8 is reversed, turning off D105. With D105 being opened B2 of Q101 is not affected by this polarity shift, keeping the proper voltage potential upon B2. A101 acts like a variable resistor controlling the charge time of C110 through D107, which in turn controls the frequency of oscillation between 25 - 30KHZ. D110 prevents the base of Q103 from going beyond a -.7 VDC. C111 is used to shunt any unwanted AC to ground 1 (AC grd).

R114 prevents Q103 from turning on to saturation. R106 is a "fuseable" Resistor serving as part of the over voltage protection circuit. R109 and R110 are current limiting resistors to set the wattage for A101 and Q101 respectively. These resistors are not field adjustable.
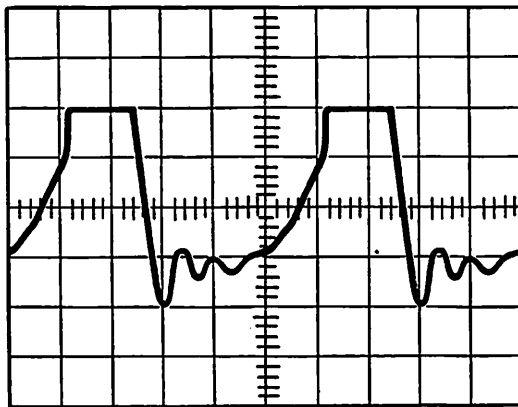
IO-A ANODE OF D105

5 V/Cm
5 μsec/Cm
20 V P-P

IO-B CATHODE OF D105
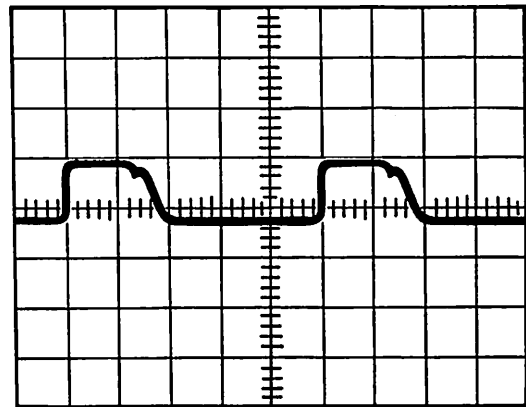
1 V/Cm
5 μsec/Cm
1.2 V P-P

IO-C JUNCTION OF R103-C103
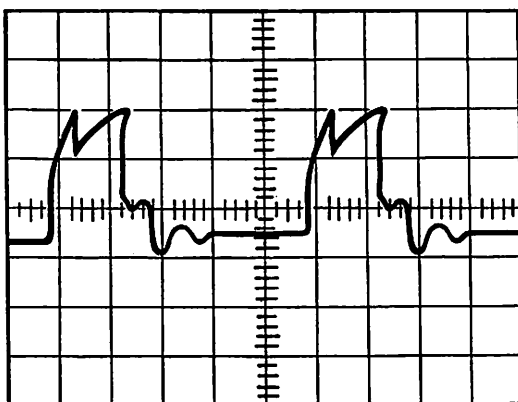
1 V/Cm
5 μsec/Cm
3 V P-P

IO-D EMITTER OF Q101
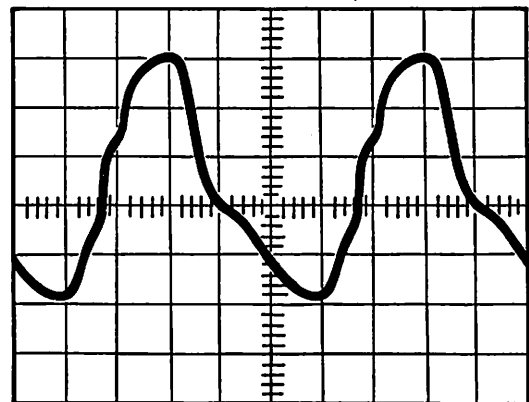
5 V/Cm
5 μsec/Cm
20 V P-P

Figure 10

3-3

10-E   BASE OF Q102
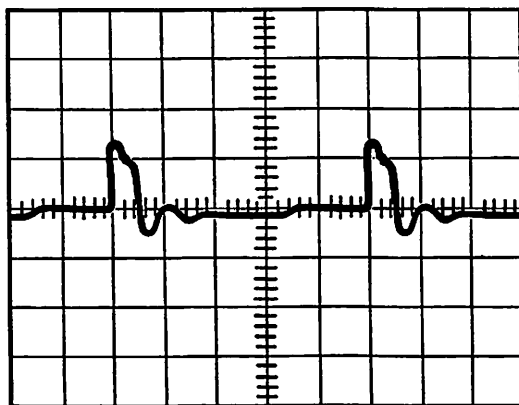
I V/Cm
5 µsec/Cm

10-F COLLECTOR OF Q103
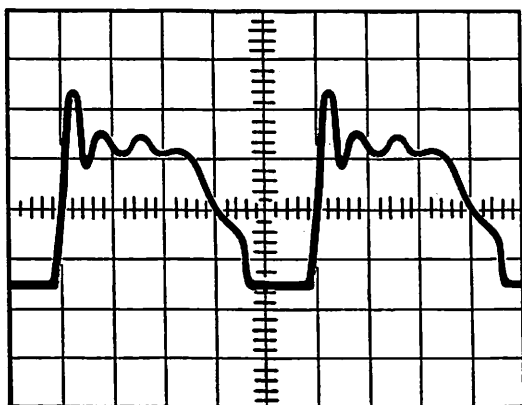
20 V/Cm
5µsec/Cm
78V P-P

10-G ANODE OF D106
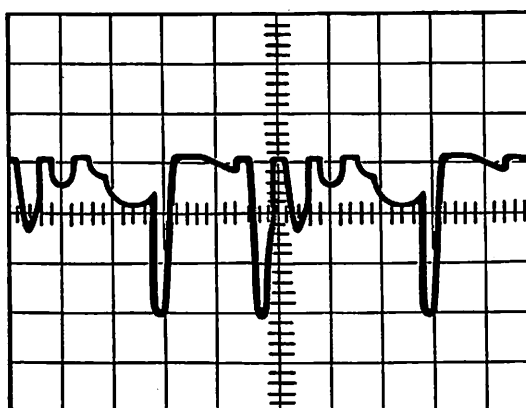
IO V/Cm
5µsec/Cm
32V P-P

3. +5VDC REGULATED

Transformer T1 supplies approximately 3.6 VAC to the secondary winding pins 3 and 4. This secondary voltage is half-wave rectified by D112 resulting in a 5.1 VDC (Unregulated). This voltage is filtered by C112-C115 and L101. R115 is a load resistor. D111, R121, R129, and SCR (A103) serve as a over voltage protection circuit. If the +5.1VDC line rises enough to turn D111 on, a current is passed through D111, R121, and R129. A voltage drop is

3-4

developed across R121 and R129 providing the necessary voltage potential to turn A103 on. With A103 on, a short is developed between the +12VDC (Unregulated) line and ground 2 (chassis grd). The accompanying increase in current should be enough to blow the "fuseable" Resistor, R106.
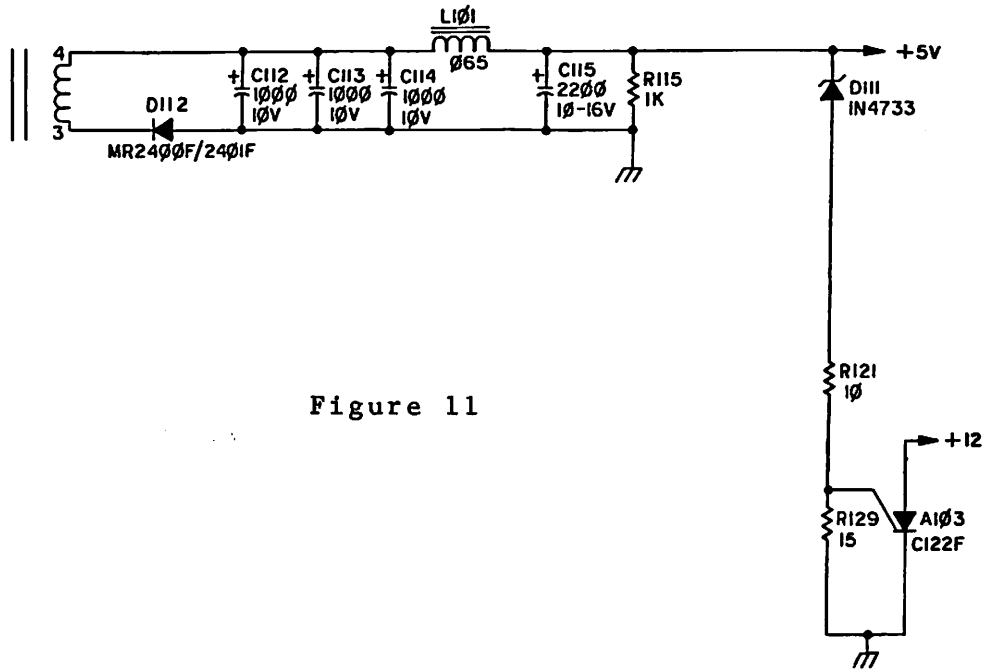
Figure 11

4. +12VDC UNREGULATED

Transformer T1 supplies approximately 8.6VAC to the secondary windings pins 1 and 2. This secondary voltage is half-wave rectified by D115 resulting in a 12.2 VDC (Unregulated). The 12.2 VDC (Unregulated) is filtered by C116, C118, and L102.
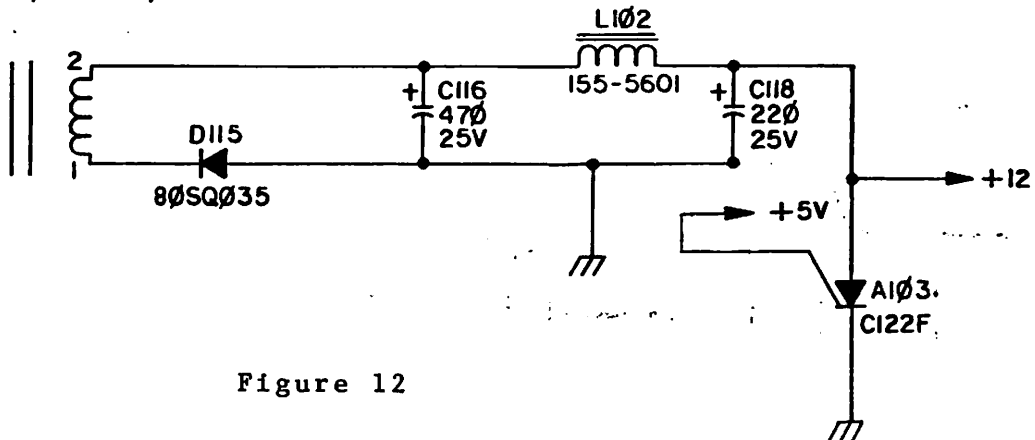
Figure 12

5. +12VDC-Regulated

Transformer T1 supplies approximately 11 VAC to the secondary windings pins 5 and 6. This secondary voltage is halfwave rectified by D118, resulting in a 15.2 VDC (Unregulated). This voltage is filtered by C119, C120, and L103. R127 is a load resistor. The 15.2 VDC (Unregulated) is put through a 12V Regulator (A102) whose output is +12 VDC (Regulated). D117 prevents the +12 VDC from going beyond -.7 VDC. The Regulated +12 VDC is filtered by C121. The resulting voltage is used to power the CRT module.
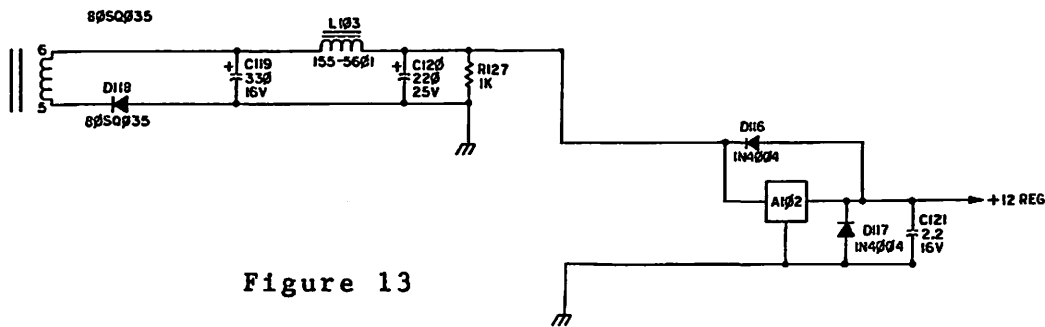
Figure 13

6. -12VDC-Regulated

Transformer T1 supplies approximately 11.5 VAC to the secondary windings pins 11 and 12. This secondary voltage is half-wave rectified by D121, resulting in a -16.3 VDC (Unregulated). This secondary voltage is filtered by C122, C123 and L104. R132 is a load resistor. The -16.3 VDC (Unregulated) is put through a 12V Regulator (A104) whose output is -12 VDC (Regulated). This voltage is filtered by C124. D119 prevents the -12 VDC from going beyond +.7 VDC.
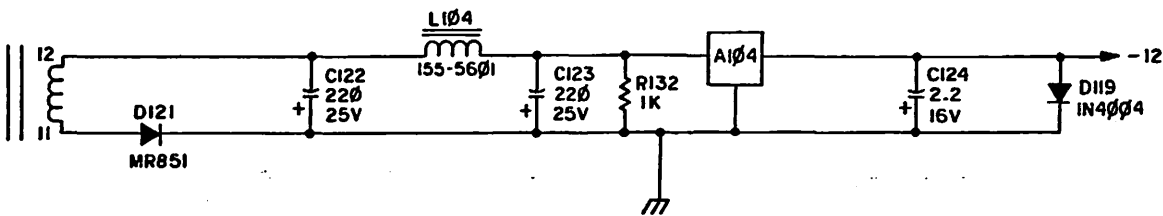
Figure 14

7. The OP AMP/REGULATOR

The base of Q106 is held constant by being tied to ground 2 (chassis grd). The emitter of Q106 is held constant by going to a regulated voltage (-12 VDC). Thus the current flow through R126, R124, Q106, and R118 is held constant. The current flow through A101 is controlled by Q104. Q104 is controlled by Q105. If the +5 VDC tries to go up, Q105 is turned on harder, turning Q104 on harder, increasing the current flow through A101, which increases the brightness of the LED. The brightness of the LED serves as the bias for the other half of A101. If the +5 VDC tries to go low, Q105 is turned on less, turning Q104 on less, decreasing the current flow through A101. This circuit controls the oscillation of the primary through the other half of A101.
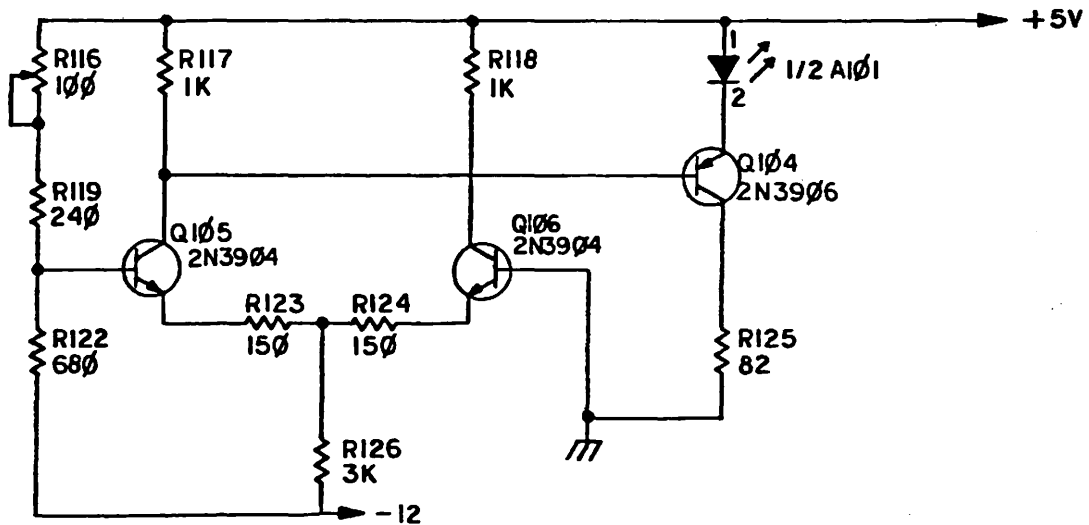
Figure 15

3.2 VIDEO CONTROL BOARD

The video control board can be functionally broken down into five units. These units are:
1. Power
2. Brightness control
3. Horizontal drive
4. Vertical drive
5. Video amplifier

1. POWER

The reg +12v for the video control board is input on pin 1 of J1. This +12v supplies the voltage necessary to drive the various circuits. The +12v is also applied to the primary of transformer T702. The secondary of T702, through diode D752, supplies -180v to the brightness control circuit. The -180v is applied to resistor R51. The +50 volts for the video drive circuit is developed through resistors R51,R758,R759 and ZD751 (33.8v zener), and applied to resistor R209.

The secondary, through diode D751, supplies +300v for the control grid on the CRT. The +300v is output to the CRT through pin 6 of P1. The 300v circuit is protected from over-voltage by spark gap SG751. The +300v is also applied through R751 to pot R754. R754 is used to adjust the voltage level to the focus grid on the CRT (0 - 150v). The focus circuit is over-voltage protected by spark gap SG752.

The focus voltage through R755 is transmitted to the CRT through pin 7 of P1. The focus controls the sharpness of the characters on the screen. Part of the secondary of T702 is tied to the primary (pin 1). Pin 3 of the secondary (primary side) supplies a +200v output for the horizontal drive circuit. The +200v is applied to the collector of Q704. The secondary also supplies the 12K volts for the anode of the CRT through pin 1 of P2.

2. BRIGHTNESS CONTROL

The brightness control circuit is used to adjust the voltage for the brightness grid on the CRT. The -180v from the secondary is applied through resistor R51, pot R758, resistor R759 and zener diode ZD751. R759 is used to adjust the voltage level to the brightness control grid on the CRT. This voltage level is the reference point for the circuit, the brightness will be controlled through the keyboard. The brightness output voltage is applied to resistor R756 and output to the brightness grid of the CRT on pin 1 of P1.
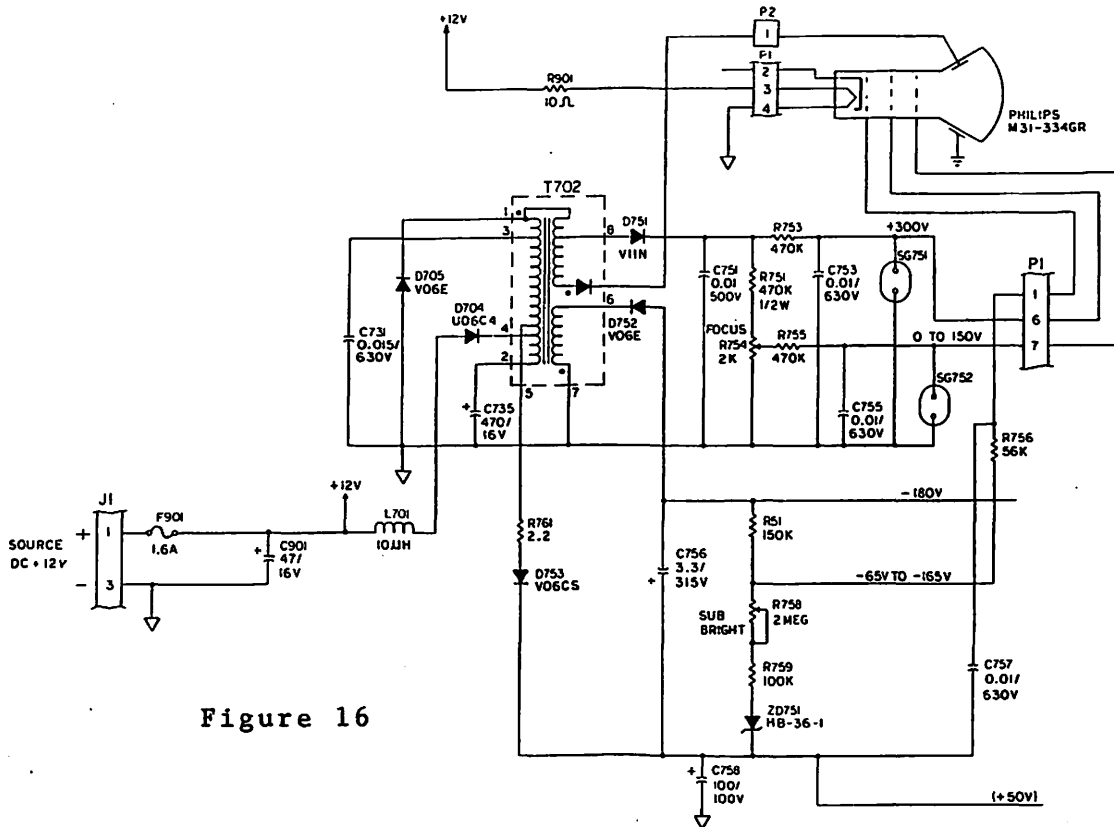
Figure 16

3. HORIZONTAL DRIVE

The horizontal drive signal is used to control the amount of horizontal deflection on the CRT. The horizontal drive signal from the CPU is input to the video control board on pin 4 of J1. The horizontal drive signal is applied to capacitor C701, resistor R703 and diode D701, and is the trigger input to the multivibrator circuit. The multivibrator circuit consists of transistors Q701, Q702, R704, R705, R709, R710, R711, R718, R719, C702 & C711.

Each time a positive trigger is applied to the base of
Q701, Q701 will conduct. When Q701 is conducting, Q702 will
be off. The circuit will remain in this condition as long
as the base of Q702 is at a negative potential, determined
by C711 and R711. When capacitor C711 discharges, a
positive potential will be applied to the base of Q702,
this will turn Q702 on.
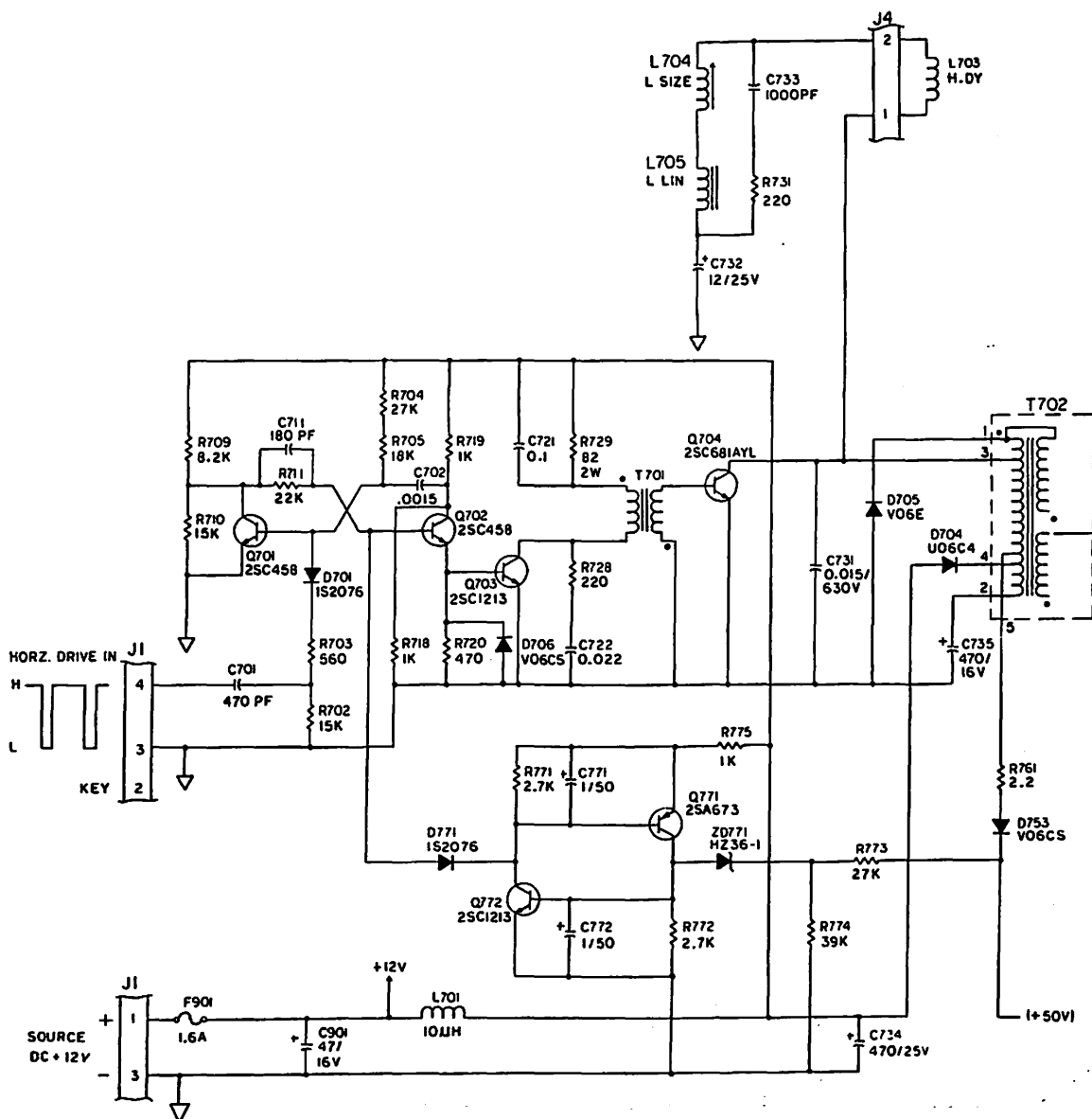
Figure 17

With Q702 on, Q701 will be off. With Q702 on, a positive potential will be applied to the base of Q703. This will turn on Q703. Q703 conducting will allow current flow through the primary of transformer T701. The secondary of T701 is connected to the base of Q704. Q704 will produce a 225v pulse, switching from 0 to +225, with a 7 usec pulse width and a 16khz rate. The output of Q704 is applied to the horizontal yoke on the CRT through pin 1 of J4.
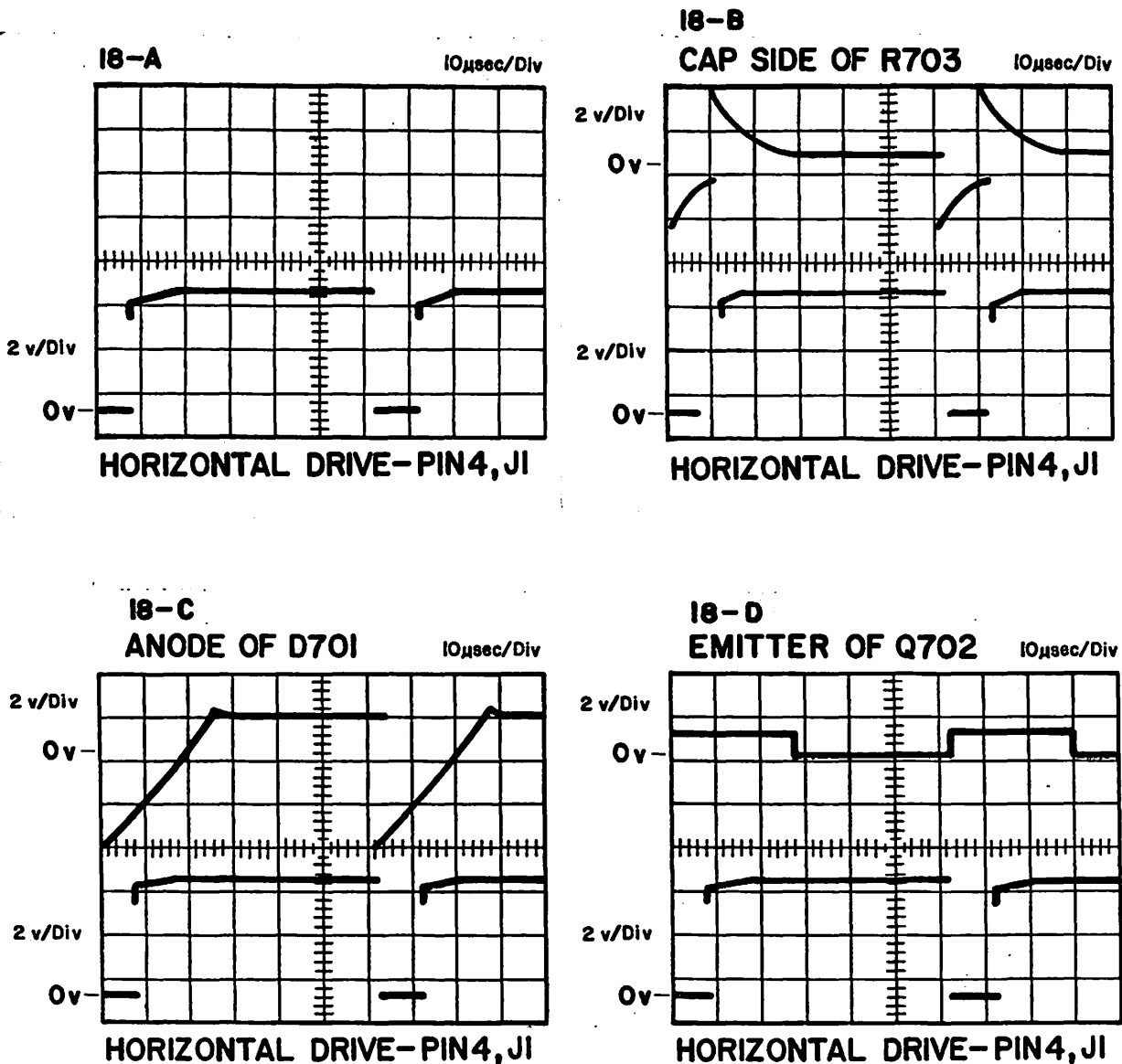
18-A
10μsec/Div

HORIZONTAL DRIVE-PIN4,JI

18-B
CAP SIDE OF R703
10μsec/Div

HORIZONTAL DRIVE-PIN4,JI

18-C
ANODE OF D701
10μsec/Div

HORIZONTAL DRIVE-PIN4,JI

18-D
EMITTER OF Q702
10μsec/Div

HORIZONTAL DRIVE-PIN4,JI

Figure 18

I8-E
COLLECTOR OF Q703 IOµsec/Div

5v/Div
Ov
2 v/Div
Ov

I8-F
BASE OF Q704 IOµsec/Div

Ov
5v/Div
2 v/Div
Ov
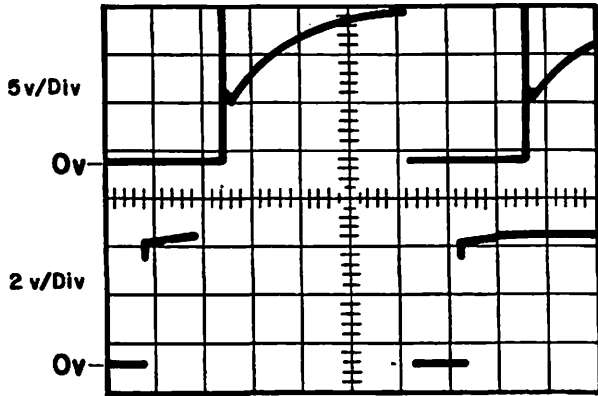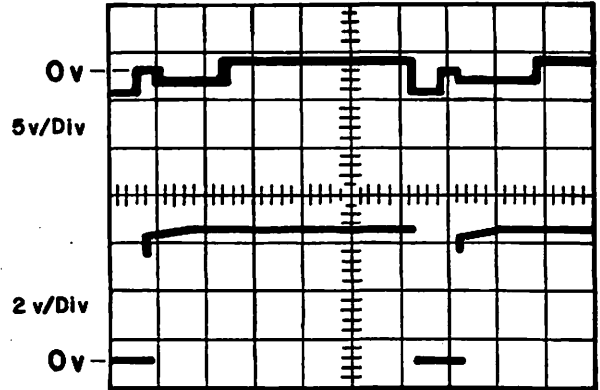
I8-G
COLLECTOR OF Q704 IOµsec/Div

50v/Div
Ov
2 v/Div
Ov
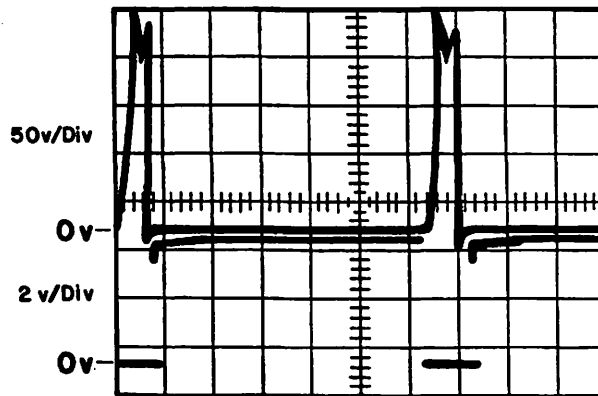
HORIZONTAL DRIVE-PIN4,JI

4. VERTICAL DRIVE

The vertical drive signal is used to control the amount of vertical deflection on the CRT. The vertical drive signal from the CPU is input to the video control board on pin 5 of J1. The vertical drive signal is applied through resistor R601 to the base of transistor Q601. Q601 will amplify and invert the vertical drive signal. The output of Q601 is then applied to pin 6 of IC601.

IC601 will sync on the vertical drive signal and produce a saw-tooth output to drive the vertical yoke. Pin 5 of IC601 is the internal vertical sync oscillator output. This output is applied to pin 6 with the vertical drive signal for synchronization. Pot R611 is used to adjust the input to stop vertical roll. Pin 4 is the output of the internal saw-tooth generator. This saw-tooth is applied through R623 and C622 to pin 7.

The input to pin 7, Vertical Size, is adjusted by pot R622. This adjustment sets the number of characters on the screen. Pot R624 through C621 will also affect this circuit. R624 is used to adjust the Vertical Linearity, the vertical height of the characters. IC601 will produce a 10v pulse, switching from +5v to +15v, with a 850 usec pulse width and a 76hz rate. The output of IC601 (pin 1) is applied to the vertical yoke on the CRT through pin 1 of J3.

Figure 19

20-A

2msec

2v/Div

Ov —

VERTICAL DRIVE-PIN5,JI

20-B
COLLECTOR Q601   2msec

2v/Div

Ov —

2v/Div

Ov —

VERTICAL DRIVE-PIN5,JI

20-C
IC 601, PIN 5   2msec

2v/Div

Ov —

2v/Div

Ov—

VERTICAL DRIVE-PIN5,JI

20-D
IC 601, PIN 6   2msec

2v/Div

Ov —

2v/Div

Ov —

VERTICAL DRIVE-PIN5,JI

20-E
IC 601, PIN 4   2 msec

5v/Div

Ov —

2v/Div

Ov—

VERTICAL DRIVE-PIN5,JI

Figure 20

3-15

20-F
IC 601, PIN 7

2 msec

2v/Div

0v

2v/Div

0v

VERTICAL DRIVE-PIN5,J1

20-G
IC 601, PIN 9

2 msec

2v/Div

0v

2v/Div

0v

VERTICAL DRIVE-PIN5,J1

20-H
IC 601, PIN 1

2 msec

5v/Div

0v

2v/Div

0v

VERTICAL DRIVE-PIN5,J1

20-I
PIN 1, J3

2 msec

10v/Div

0v

2v/Div

0v

VERTICAL DRIVE-PIN5,J1

5. VIDEO AMPLIFIER

The video amplifier is used to boost the video signal
to drive the CRT. The video signal from the CPU is input to
the video control board on pin 6 of J1. The video signal is
applied through resistor R201 to the base of transistor
Q201. When Q201 turns on, Q202 will turn on. Q202 will
produce a 20v signal, switching from +60v to +40v, with a
.1 usec pulse width and a 17.5mhz rate.

The video output from the collector of Q202 , through
resistor R232, is applied to the cathode on the CRT through
pin 2 of P1. The neon tube, NE201, is used for over-voltage
protection. The circuit is also protected through the +12
volt supply and by Zener Diode ZD771. If the voltage rises,
ZD771 will conduct. With ZD771 conducting, Q772 and Q771
will turn on. With Q772 and Q771 on, the +12v will be
removed from the primary of T702, thus shutting down the
transformer. D771 will also conduct keeping Q702 off in the
multivibrator circuit.

Figure 21

22—A
VIDEO IN — PIN 6,JI   .1μsec/Div

22—B
COLLECTOR OF Q202   .1μsec/Div

Figure 22

3-17
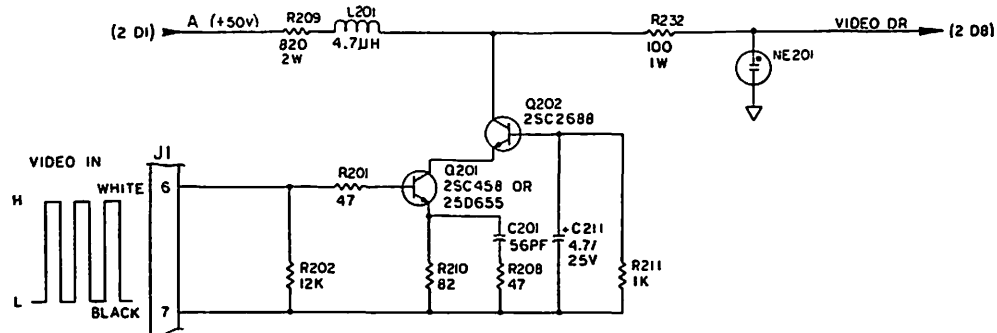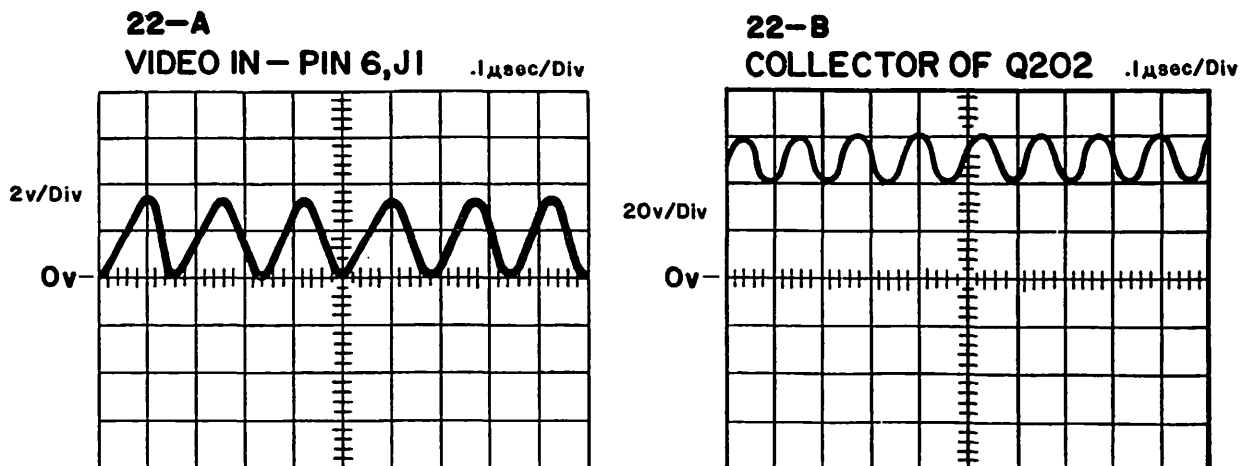
3.3 DISK DRIVE CONTROL BOARD

The disk drive control board performs the operations necessary for data transferrs to and from the CPU board and the disk drives. The following sections explain the theory of operation for the Seek, Write, Read and Motor Speed functions of the disk drive control board.

3.3.1 SEEK LOGIC

The disk drive subsystem will position the read/write head over the desired track by use of a four phase stepper motor. The stepper motor is controlled by the VIA (Versitile Interface Adapter) 6522 at location 1F on sheet 2 of schematic 100671.

The four phase signals are controlled by the Peripheral Port A (PA4-PA7) of 1F for the A disk drive and Peripheral Port B (PB4-PB7) for the B disk drive.

The computer program will determine the direction and number of steps needed to move the head from the present track to the desired track. It will then transfer the 4 bits necessary to step the head to the selected track.

Sheet 4 of CPU schematic 100471 illustrates the Chip Select ($\overline{CS5}$) required to address the 6522 for the seek control logic. The memory mapped I/O space for seek and motorspeed is E80A0.

When A19,A18,and A17 are all high (sheet 4 of 100471) and the IO/$\overline{M}$ signal is low, the Y7 output of decoder 9F will go low. This enables decoder 9H. When A16 is low and A15 is high the Y1 output of 9H will go low enabling the G2A input to 10H. Decoder 10H is used to chip select each of the 6522's used in the microcomputer. When A8 is low, A5 is high, A6 is low and A7 is high, the Y5 output will go low enabling $\overline{CS5}$ for the seek logic 6522 on the disk controller board. When $\overline{CS5}$ is low data may be written or read from the VIA.

The 6522 at 1F (sheet 2 of 100671) is register selected by address bits A0-A3 of the address bus. These bits will select one of sixteen internal registers.

The seek logic for the A drive is controlled in the Output Register A (ORA) for the peripheral A port. This register is initialized by the Data Direction Register A (DDRA). The DDRA determines whether a peripheral port bit will be used as an input or an output. For seek logic the PA4-PA7 bits will be programmed as output pins. The ORA register is accessed for data transfer when address E80A1 is placed on the address bus. The four bits then placed on the ID4-ID7 bit positions of the ID bus will be placed into the ORA register when the $\overline{WR}$ signal goes low.

When the drive is selected, the STP0 or STP1 control lines on 6522 1H will go low. This low will be inverted by 4G to enable the stepper motor driver chips. These control lines are loaded in the same fashion as the four phase stepper signals at 1F.

The four phase stepper control lines will be sequenced by the microprocessor to cause the stepper motors to step either in or out as referenced by the following table.

STEPPER MOTOR PHASE SEQUENCE

	STEP IN					STEP OUT			
STOA	0	1	1	0		0	0	1	1
STOB	1	0	0	1		1	1	0	0
STOC	0	0	1	1		0	1	1	0
STOD	1	1	0	0		1	0	0	1
STP0	1	1	1	1		1	1	1	1

The step in sequence will step the head toward the center hub (increasing track number) while the step out sequence will step the head toward the outer perimeter of the diskette (decreasing track number). Each time the sequence changes the head will step one track.

The four phase signals are fed to driver chip 3D on sheet 7 after going through the enable nand gate 4D. STP0 will be high during the A disk select sequence allowing the four phases to pass to the drivers. The outputs of 4D are fed to the driver and are pulled to a +12v level by the in-line resistors. The voltage swing out of 4D will be from 0 to 12v. The two diodes on each input line to the driver are used for spike elimination.

The resultant output waveform from 3D will drive the stepper motor one track position.

The stepper motor will remain in a stable position until it receives another step command from the 6522 at 1F.

The seek logic is identical for the B drive except the B drive uses PB4-PB7 of 6522 1F. These lines are initialized by the Data Direction Register B (DDRB) and the four phase control signals are loaded into Output Register B (ORB). The ORB register is accessed when address E80A0 is placed on the address bus. The same bits ID4-ID7 of the Input/Output bus are transferred to bits 4-7 of the ORB. When the B drive is selected the STP1 line on 6522 at 1H will go low.

The STP0 and STP1 control lines are initialized by the DDRB of 6522 1H at address E80C2 and PB6 and 7 are loaded when address E80C0 is selected.

3.3.2 MOTOR SPEED CONTROL

The disk drive subsystem uses a technique in disk speed variation to allow the data to be stored onto the media in a near constant bit density. The media allows up to 8000 bits per inch data density. In a standard disk drive the 8000 bpi is maintained on the inner tracks while the bit density drops to near 4000 bpi on the outer tracks. Consequently much storage space is wasted in the outer track area. By varying the speed at which the diskette rotates the microcomputer stores data at a constant density of 8000 bpi on all tracks of the media.

This process is accomplished through the use of a microprocessor chip, a digital to analog converter, and a DC motor with tachometer feedback.

Refer to sheet 2 of schematic 100671. A four bit speed zone value is loaded into 6522 at 1F. This VIA not only controls speed but also controls the seek logic. Peripheral port A (PA0-PA3) control the A drive as LOMS0-LOMS3 and are directed to the 8748 microprocessor chip. This chip controls the speed by issuing an 8 bit digital value for the desired speed. On boot up it is downloaded with a speed table and control instructions to allow it to monitor the speed of each drive.

As with the seek logic, the PA0-PA3 pins are programmed by the DDRA register as outputs. When memory address E80A1 is placed on the address bus, $\overline{CS5}$ will go low, chip selecting the 6522 (refer to seek logic for a full description of the chip select sequence). The A0-A3 bits of the address will select the ORA register and the data bits in position ID0-ID3 of the Input/Output bus will be transferred to the PA0-PA3 output pins.

Drive B is controlled in the same manner except the four bit value is output on PB0-PB3 of 1F. This port is programmed by the DDRB and the data on the ID0-ID3 is transferred into the ORB register.
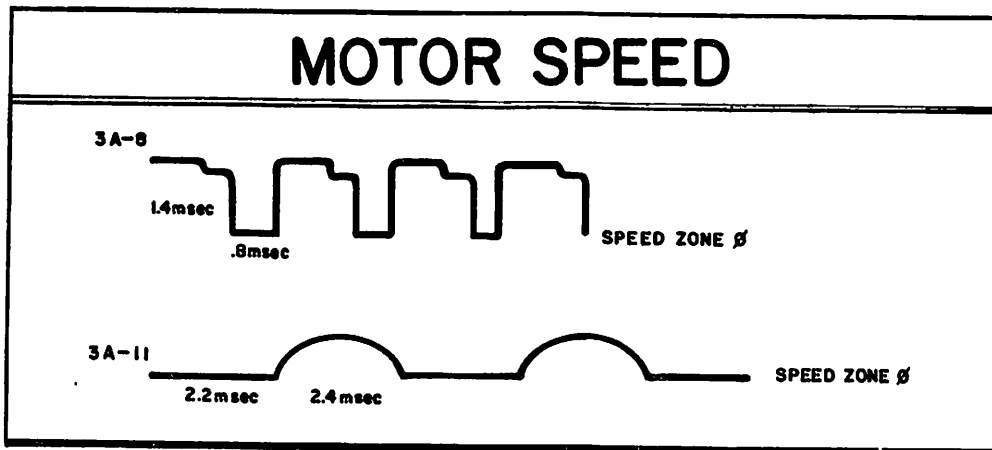
Figure 23

The 4 bit speed zone enters the 8748 microprocessor chip on either P10-P13 for the A drive or P14-P17 for the B drive. The microprocessor is 5D on sheet 3.

The 8748 uses CLK5 from the cpu board for basic timing. CLK5 is used in both the normal and inverted states. A speed control reset (SCRESET) is generated from 6522 1H-PB2 to allow the microprocessor to be reset. When SCRESET is high, the inverted output of 6F will reset the 8748, clearing the internal registers.

An 8 bit speed value is output from the 8748 on DB0-DB7. This represents a digital value for the desired speed. When either SEL0 or SEL1 goes low the speed byte will be latched into either 6B or 6C, respectively. The output of the latches are used as inputs to the digital to analog converters 5B or 5C. The D/A chips use a + and - 12 volt reference and provide an analog output to drive the dc motors. The normal driving range for the D/A chips will be between 2.2v and 3.6v.

In an idle state the output of the D/A converter will be approximately .7v. The analog output provides the drive input to driver chips 3A or 3C. The outputs on pin 8 of the driver chips biases the Q1 or Q2 bases to provide the voltage waveform necessary to control the speed of the motor. The motor speed waveform is represented in figure 23. The duration of the high pulse will decrease as motor speed increases.
A tachometer feedback provides a square wave input to the 8748 to allow it to calculate the motor speed. As it monitors the incoming tach pulses it can increase or decrease it's digital output to maintain the desired speed.

Once the 8748 has determined that the drive has achieved the proper speed, through tachometer pulse monitoring, it will put a high on the RDY0 or RDY1 line. These ready signals are routed back to the microcomputer via the 6522's 1H and 1K to acknowledge that the drive is ready for a read or write operation.

The final control signals in the motor speed logic are the start and stop bits. START0 will drop low momentarily to allow the drive circuit to start the motor. At the same time the STOP0 line will go low and remain low. When the disk operation is complete the STOP line will go high, removing the drive voltage from the motor circuit.

3.3.3 WRITE LOGIC

Data is written onto the media in the form of a 10 bit GCR code. During the write sequence an 8 bit data byte is received by the controller, converted to a 10 bit GCR code, then serially written onto the diskette.

The data byte is received over the ID0-ID7 bus by 6522 at 1K on sheet 2 of schematic 100671. This 6522 is chip selected by the $\overline{CS7}$ control signal from the CPU board.

On sheet 4 of 100471 when A19, A18, and A17 are all high at 9F and IO/$\overline{M}$ is low, the Y7 output will go low. This low will enable the decoder at 9H. When A16 is low and A15 is high the Y1 output will go low enabling the G2A input to decoder 10H. At the same time A8 will be low, enabling G2B of 10H. A7,A6, and A5 will all be high resulting in the Y7 output ($\overline{CS7}$) going low. This low chip selects the 6522 at 1K on the disk controller board.

The DDRB register will be initialized to set the peripheral port B to an output port. The byte to be written will then be transferred into the ORB register. The byte will enter the write sequence as WD0-WD7. The ORB (output register B) is addressed when memory address E80E0 is placed on the address bus.

WD0-WD7 are inputs to multiplexer chips, 5H,5J,& 5K on sheet 7. When DRW is low (Data Read/Write) signifying a write operation,it is inverted at 4G and the resultant high selects the B inputs on the multiplexer chips.

DISK WRITE CONTROL

```
5H-4
WRT CLOCK

110110
4F-12
GCR

4F-11
GCR
DATA

5N-5
WR +
```
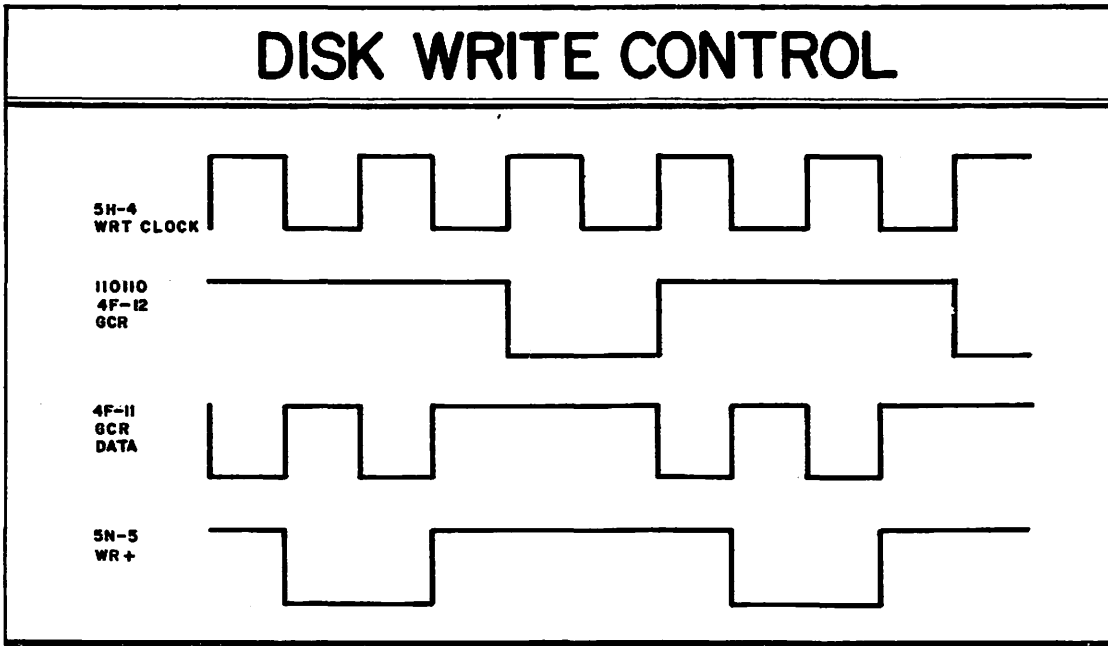
DISK WRITE CONTROL

Figure 24

The WD0-WD7 bits are placed on the I0-I9 bus in bit positions I0-I8 with the exception of I4. I4 is used for the WRSYNC signal which will be discussed in the section on writing the sync code onto the disk. During the write sequence the I9 bit is held high. The I0-I9 bus addresses the GCR ROM at 4K.

The GCR Rom will then output an 8 bit code representative of the data byte. Table 1 on page 2-7 shows the GCR conversion. The translation process allows the I2 and I7 bits of the address bus to pass directly to the parallel to serial converter at 4J and 4L.

The DRW low signal is also routed as address bit 10 to the GCR Rom. This forces the GCR Rom to be addressed in the lower 1K addresses. During a read operation the high on the DRW line will force the GCR Rom to address the upper 1K addresses.

The E0-E7 data output of the GCR Rom is coupled with the I2 and I7 bits and fed into the parallel to serial converter.

The parallel to serial converters clock the parallel input out in a serial data string by use of the WRTCLK clock generated on the CPU board.

The WRTCLK pulse train originates on sheet 5 of 100471. The counter at 11H is clocked by every CLK15A pulse. The 1QD output is tied to the CLK2 input of the chip. The WRTCLK output is taken from the 2QA internal flip- flop. The resultant waveform is a 1 usec clock. (figure 24)

The R input clears the counters on power up to insure they begin at an all zero state. The WRTCLK signal is a continuous clock present when power is applied to the unit.

The WRTCLK signal is multiplexed through 5H on sheet 7 of schematic 100671 then inverted by 4G to provide the necessary clock to transfer the serial pulses out of the parallel to serial converter. The serial data string is "nanded" with the WRTCLK at 4F to provide GCR DATA. Figure 24 shows the relationship of WRTCLK and the serial data string.

The GCR DATA pulses are used to clock the write flip- flop at 5N on sheet 6. On the rising edge of the GCR data pulse the write flip- flop will toggle. This will alternate the high from $\overline{WR+}$ to $\overline{WR-}$. Each time the flip- flop toggles a flux reversal will be recorded on the media.

The write flip- flop is disabled by a low on both the PR and CLR inputs. Both PR and CLR will be low when either the WPS goes high (a diskette is write protected) or the DRW signal is high. When both PR and CLR are low the $\overline{WR+}$ and $\overline{WR-}$ outputs will be high. These high signals are inverted at 2N on sheet 5 and disable the write circuits.

In the write sequence the $\overline{WR+}$ and $\overline{WR-}$ will toggle low, being inverted by 2M with the resultant high selecting a current source for the write head. When $\overline{WR+}$ is low, current will flow in one direction through the head coil. When $\overline{WR-}$ is low, current will flow in the opposite direction.

The $\overline{WR+}$ and $\overline{WR-}$ enable the write current drivers composed of 3N. The four transistors provide the current source for writing onto the disk. The circuit composed of the 5th transistor in 3N, Q3, and CR7 act to disable the write current in the event of low voltage.

The head select logic HS00 through HS11 selects the desired head for writing. The head select control signals originate on sheet 6 at decoder 3M. Head 0 will be selected (HS00 low) when both SIDE SELECT and DRIVE SELECT are low. The SIDE SELECT and DRIVE SELECT are controlled by the 6522 at 1H on sheet 2 (PA4 and PA5).

The processor will load the proper bit configuration into the ORA register when a drive is selected. The low output for head select (HS00) is inverted at 2M and the resultant high enables the digital relay at either 1M or 1N. The table on page 3-27 defines each head select bit.

The head select allows the write current to pass through the write coil thereby recording a flux reversal onto the media. The write sequence can either write a data byte (10 bit GCR Code or a 10 bit sync code. The sync code is composed of an all one's GCR Code.

To write a sync code the WRSYNC control line on 6522 at 1F on sheet 2 will be directed high by the processor. This high is gated through multiplexer 5K on sheet 7 and places a high on the I4 bit. At the same time the processor will put a one in WD2 and WD6. This bit configuration will address a GCR Rom address that contains all ones for E0 through E7. The resultant "all ones" pattern will be serially clocked through the write circuit and be recorded on the disk.

The sync bytes will be used by the controller to detect the beginning of a sector header and the beginning of a data block. Their significance will be apparent during the read/recovery sequence.

3.3.4 READ RECOVERY CIRCUIT

Data is recovered from the media by the use of a Read Amplifier, a Phase Lock Loop circuit and a GCR decoder. Refer to schematic 100671 for the read recovery theory of operation.

READ AMPLIFIER

The Read Amplifier circuitry (sheet 5) senses the flux reversals created during the write operation.

Each head is selected for reading by its respective head select control line.

HS00	Drive A	Head 0
HS01	Drive A	Head 1
HS10	Drive B	Head 0
HS11	Drive B	Head 1

When HS00 on sheet 6 goes low, drive A head 0 is selected for either a read or a write operation. The low output of 3M is inverted at 2M and the resultant high engages the digital relay at 1M.

As the media passes under the head, the flux reversals induce a 10 mvolt signal through the read coil. This signal is directed into the read pre-amplifier at 1P. 1P amplifies the signal to approximately .6 volts and passes it through a linear phase filter network of R62, R63, L3, L4, C21 and C56.

The analog input is amplified and differentiated by 3P, then routed to a digitizer at 4P. The LM311 at 4P takes the positive and negative peaks and generates a digital pulse representing the zero crossings of the differentiated analog inputs. Figure 25 (4P-7) represents the read data (RDATA) output of the flux reversals sensed by the head coil.

PHASE LOCK LOOP

The digital pulse train (RDATA) enters the Phase Lock Loop (PLL) circuit on pin 13 of 5P (sheet 4). This Exclusive OR gate will generate a high pulse at each transition of the RDATA pulse.

DISK READ CONTROL
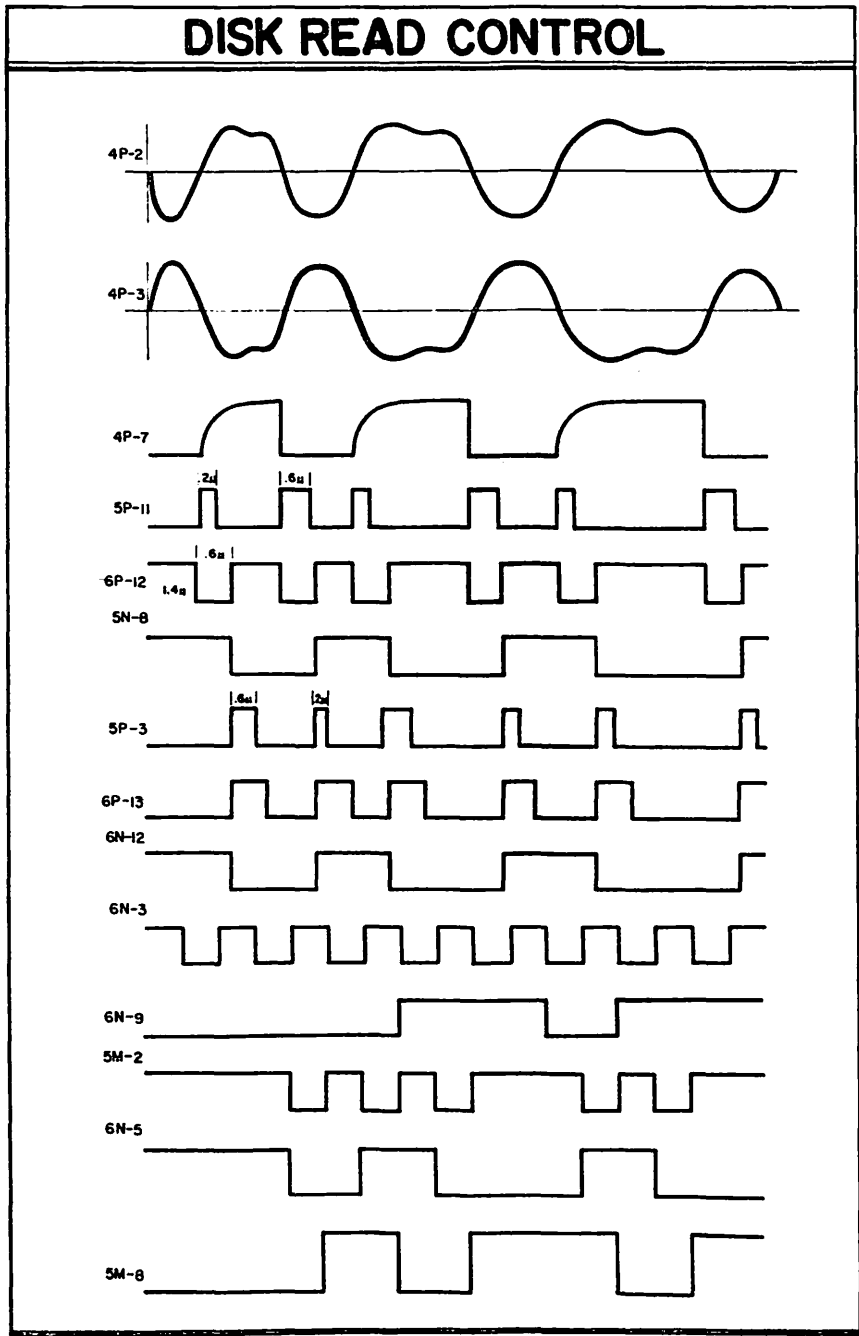
Figure 25

Pin 11 of 5P will go high for approximately 200 nanosec on the leading edge of RDATA and will go high for approximately 400 nanosec at the trailing edge of RDATA. Figure 25 (5P-11) illustrates the relationship between RDATA and the output of 5P.

Each time 5P pin 11 goes high (on the leading or trailing edge), it will trigger one-shot 6P. At that time 6P Q output (pin 5) will go high for 1 usec and the $\overline{Q}$ output (pin 8) will go low for 1 usec. At the end of the 1 usec one-shot time frame, the rising edge of 6P pin 12 will clock the D input (pin 12) of 5N onto the Q output. Figure 25 illustrates the output of 5N pin 8. This output will be the inverse of the D input when the flip-flop is clocked.

The output of 5N pin 8 is directed to "Exclusive OR" gate 5P (pin 1). This circuit functions the same as the initial "Exclusive OR" gate. Figure 25 (5P-3) represents the output of 5P pin 3, using the input of 5N-8. Each time 5P pin 3 goes high, it will fire the second one-shot. This one-shot will also put out a 1 usec high on the Q output (6P pin 13). 6P pin 13 is routed to the clock input of 6N (pin 11).

The rising edge of 6P pin 13 will toggle flip-flop 6N. The $\overline{Q}$ output of 6N (pin 8) is routed to the D input (pin 12) to cause the flip-flop to toggle each time a positive going pulse is received. Figure 25 (6P-13) illustrates the clock input while Figure 25 (6N-5) illustrates the Q output of 6N.

The VCO (Voltage Controlled Oscillator) output of the 4046 chip, 6L pin 4 , is used to clock the data pulse into 6N pin 2. On the leading edge of READ CLOCK (VCO output pin 4), the Q output of 6N (pin 9) is triggered onto the Q output of 6N (pin 5).

The VCO output is "Exclusive OR'd" with a high at 5P (pins 9 & 10) which results in inverting the VCO input at 5P pin 8. This inverted output is again inverted at 3L to generate READ CLOCK.

The Q output of 6N pin 5 is clocked onto the Q output of 5M on the rising edge of the inverted clock signal of 5P pin 8. This results in clocking the data bit into 5M on the falling edge of the VCO output. Figure 25 shows the relationship of the $\overline{Q}$ output (pin 8) of 5M to the Q output of 6N (pin 5).

The outputs of 6N pin 5 and 5M pin 8 are "Exclusive OR'd" at 5P pins 4 and 5. Figure 25 (5M-2) is the resultant output waveform of 5P pin 6. The output of "Exclusive OR" gate 5P pin 6 is used to set the output of 5M pin 5 on the rising edge of the inverted VCO output. The READ DATA output is represented on the $\overline{Q}$ output of 5M at pin 6. When READ CLOCK goes high, the $\overline{Q}$ output of 5M will represent the data bit read from the media.

The output of 5P pin 6 is also inverted at 6F and routed to the comparator input of the PLL chip. The PLL will compare the rate at which the signal pulses from 6P pin 4 and the VCO output pulses from 6F are arriving. It then adjusts the VCO output rate at pin 4 to equal the rate at which the signal pulses are coming in.

The PLL uses the 'all ones' that are read from the sync code to capture on the signal input frequency.

4046 PHASE LOCK LOOP CHIP

The Phase Lock Loop (PLL), IC 6L on sheet 4 of schematic 100671, consists of a voltage controlled oscillator (VCO) and 2 different phase comparators having a common signal-input amplifier and a common comparator-input.

VCO SECTION

R27 (IC 6L, pin 11) and C17 (IC 6L, pins 6 & 7) determine the frequency range of the VCO. R28 (pin 12) enables the VCO to have a frequency offset.

PHASE COMPARATORS

The PLL has 2 different phase comparators (1 & 2). Comparator 1 may lock onto harmonics close to the center frequency. It will also have a varying phase angle between the signal-input and the comparator-input signals. These situations do not exist in phase comparator 2. Phase comparator 2 is used in the 9000.

PHASE COMPARATOR 2

Phase comparator 2 is an edge controlled digital memory network. It consists of 4 flip-flop stages, control gating and a 3-state output circuit. The 3-state output circuit is composed of P-type and N-type drivers having a common output node. When the P-MOS drivers are on, they pull the output up to VDD. When the N-MOS drivers are on, they pull the output down to VSS. When both are off, the output will be an open circuit.

Since this type phase comparator acts only on the positive edges of input signals, the duty cycle is unimportant. The phase comparator output, 6L pin 13, is used to adjust the VCO input voltage, 6L pin 9.

PHASE COMPARATOR 2 OPERATION

If the signal-input frequency, 6L pin 14, is higher than the comparator-input frequency, 6L pin 3, the P-MOS driver will be on most of the time, placing VDD on the phase comparator output (6L pin 13). The remainder of the time, the P-MOS and the N-MOS drivers will both be off (open circuit out, 6L pin 13).

If the signal-input frequency, 6L pin 14, is lower than the comparator-input frequency, 6L pin 3, the N-MOS driver will be on most of the time, placing VSS on the phase comparator output (6L pin 13). The remainder of the time the N-MOS and the P-MOS drivers will be off (open circuit out, 6L pin 13).

If the signal-input and the comparator-input frequencies are the same, but the signal-input lags the comparator-input in phase, the N-MOS driver is turned on for the time corresponding to the phase difference, VSS out on 6L pin 13. If the frequencies are the same, but the comparator-input lags the signal-input in phase, the P-MOS driver is turned on for the time corresponding to the phase difference, VDD out on 6L pin 13.

In this way, the N-MOS and the P-MOS drivers will adjust the low-pass filter capacitor voltage (C18) on the comparator output until the signal-input and the comparator-input signals are equal in both frequency and phase.

At this stable point, the P-MOS and the N-MOS drivers will remain off, open circuit out, holding the voltage on C18 at a constant level. This frequency and phase relation will be maintained over the full VCO range.

The power dissipation of the PLL is reduced due to the low-pass filter keeping the N-MOS and the P-MOS drivers off for most of the signal-input cycle. With no signal-input applied, the VCO is adjusted to its lowest frequency. The VCO output, 6L pin 4, is used to generate the READ CLOCK through 5P and 3L. It is also used as the clock input for 6N (pin 3). the output of 6N, pin 5, through 5P and 6F is the comparator-input signal.

GCR DECODER

The read data pulses generated by the PLL are clocked into flip-flop 6K on sheet 7 by the read clock. On the rising edge of READ CLOCK, the READ DATA input is set to the Q output of 6K. The next READ CLOCK will set the second flip-flop (6K pin 5) to the output of the first flip-flop. The serial bit string will be shifted into the serial to parallel converter chip at 6G. The 10 bit GCR code for the data byte will then go to the multiplexer chips 5H, 5K, and 5J. If the 10 bits are "all one's" " nand" gate 6J will go low signifying that a sync code has been read.

When the sync detect gate goes low it will be inverted by 4G and allow BCD counter at 5G to count up to ten. When the counter overflows the ripple clock (RC) output will go low clocking the binary up counter at 5F. This counter will be preset to a count of 9 when the inverted sync line is low.

When the binary counter at 5F overflows, the resultant ripple clock output (RC) will generate an interrupt to the Programmable Interrupt Controller (PIC). The rising edge of the low will be captured by the PIC as an interrupt request. The counters at 5G and 5F are counting sync pulses to identify whether the information will be a header block or a data block. If more than five sync codes are read the sync interrupt will go low signifying that a header block is being read.

The sync pulse is also gated through the 2A input to multiplexer 5H which will be passed to the LD input of BCD counter at 4H. This low will load the counter with the preset of all zeroes. Each rising edge of read clock on the CLK input to 4H will clock the counter. When the counter overflows the ripple clock output will go low, signifying that a 10 bit GCR code has been read in. The $\overline{BRDY}$ signal is routed to the CA1 input of 6522 at 1K. This low controls the latching of the byte read from the disk into the PA0-PA7 port of the 6522.

The low $\overline{BRDY}$ signal also sets the $\overline{LBRDY}$ latch which is sent back to the cpu on pin 39 of J14. This control signal is routed to the $\overline{TEST}$ input on the 8088 microprocessor chip. This input is examined by the " wait for test " instruction. If the $\overline{TEST}$ input is low, execution continues, otherwise the processor waits in an idle state.

The 10 bit GCR data code is converted to parallel and placed on the SR0-SR9 bus where it is multiplexed onto the I0-I9 bus for the GCR Rom. It will act as a address to the GCR Rom where it will be converted back to an 8 bit data byte on E0-E7. The DRW control will be high forcing the A10 address bit high which will address the upper 1K addresses of the GCR Rom.

The 8 bit data byte on E0-E7 is latched into the 6522 at 1K on the peripheral A port and from there will be placed on the ID0-ID7 bus to be transferred into the computer.

3.4 CENTRAL PROCESSOR BOARD

The central processor board contains an 8088 CPU,128k RAM memory,communications ports,codec,boot ROM,and timing circuits. The theory of operation of each subsystem is described independent of each other system.

3.4.1 THEORY OF OPERATION - 8088 MICROPROCESSOR CHIP

The 8088 microprocessor contains a 16-bit internal register structure utilizing an 8-bit data bus. The 8088 has a 20-bit address range providing the capability to directly address 1 megabyte of memory. The 8088 is compatible with and utilizes the 8086 instruction set.

Internally the 8088 is divided into 2 functional units, the Bus Interface Unit (BIU) and the Execution Unit (EU). The BIU fetches instructions from memory and passes data to and from the EU and the data bus. The EU decodes and executes the instructions. The BIU will pre-fetch instructions and fill an "instruction Queue" with instructions waiting to be processed. By filling the "Queue" with instructions, the EU seldom has to wait for the BIU to fetch instructions. This seperate fetching and executing of instructions gives the 8088 almost as much performance as a "pure" 16-bit microprocessor such as the 8086.

The 8088 contains 8 16-bit general registers, 2 16-bit control registers and 4 16-bit segment registers.

REGISTERS

General purpose registers:

Data group registers:

AX   accumulator register
BX   base register
CX   count register
DX   data register

These 16-bit registers may be split for use as 8 8-bit registers as follows:

AH	AL
BH	BL
CH	CL
DH	DL

Pointer and index registers:

BP   base pointer
SP   stack pointer
SI   source index
DI   destination index

Control registers

IP   instruction pointer
FLAGS

Segment registers

CS   code segment register
SS   stack segment register
DS   data segment register
ES   extra segment register

Address generation

An operand is data to be processed. Operand-addressing modes are the facilities available for designating operand locations. Utilizing a 20-bit address bus, the 8088 can access 1,048,576 operand address locations stored sequentially from 0 - FFFFF(h). There are 3 uses for addresses; programs, data and stack. Each of the 4 memory spaces have a segment base register which points to the base address of the area. They are:

CS - points to the base of program currently running
SS - points to the base of the stack
DS - points to the base of one data area
ES - points to the base of an extra data area

The 8088 uses one of these segment registers for the generation of all addresses. For the address to become a 20-bit address, the segment register is shifted left by 4 binary bits before it is added to a logical address in the instruction.

For the generation of an instruction address, the CS register is added to the IP register contents. A stack address location is generated by adding the SS register to the SP register. Data addresses are generated by adding the DS register or the ES register to logical address of many types. These operand-addressing modes for the data address are selected by encoding in the instructions. The operand addressing modes are:

Immediate: The data is contained within the instruction.

Register: The data location is contained within a register.

Direct: The data is at a location pointed to by an address contained within the instruction.

Register Indirect: The data is at a location pointed to by an address contained in a register.

Indexed or Based: The data is at a location pointed to by the sum of an index or base register contents and immediate data contained within the instruction.

Based and Indexed with displacement: The data is at a location pointed to by the sum of a base register contents, an index register contents and the immediate data contained within the instruction.

The pin description for the 8088 is as follows:

Pin	Signal	Type	Definition
19	CLK	I	Clock - provides basic timing for the processor - 5MHZ.
23	TEST	I	Test input. When high places processor in a idle state. Examined by the "wait for test" instruction.

3-36

21	RESET	I	Reset causes processor to terminate present activity. Must be active high for the 4 clock cycles.
22	READY	I	Active high acts as acknowledgement from the addressed memory or I/O device that it will complete the data transfer.
17	NMI	I	Non-Maskable Interrupt - positive edge triggered interrupt. Not maskable by software.
31	HOLD	I	Active high signal to suspend operation and relinquish control of the bus lines.
40	VCC	I	+5VDC supply voltage + or - 10%.
33	MN/MX	I	Tied to +5VDC forcing the minimum mode of processor operation.
1,20	GND	I	Ground pins.
18	INTR	I	Interrupt Request - an active high level triggered input requesting an interrupt service subroutine. It can be internally masked by software.
24	INTA	O	Interrupt Acknowledge is used as a read strobe for interrupt acknowledge cycles. Active low signal.
34	SSO	O	Status line - used in conjunction with IO/M & DT/R.

26	DEN	O	Data Enable - active low during each memory and I/O access and for INTA cycles.
27	DT/R	O	Data Transmit/Receive - It is used to control the direction of data flow to the system. High for transmit, low for receive.
29	$\overline{WR}$	O	Write - strobe indicates that the processor is performing a write memory or a write I/O cycle. Active low signal.
32	$\overline{RD}$	O	Read - strobe indicates that the processor is performing a memory or I/O read cycle. Active low signal.
28	IO/M	O	Status line - it is used to distinguish a memory access from an I/O access. (I/O=HIGH, M=LOW).
25	ALE	O	Address Latch Enable - used to latch the processor address onto the address bus.
30	HLDA	O	Acknowledgement of a hold request.
9-16	AD0-AD7	I/O	Address/data bus - time multiplexed memory / I/O address and data bus.
2-8,29	A8-A15	O	Address bus
35-38	A16-A19	O	Address bus

8088 OPERATION

Refer to CPU schematic 100471 sheet 2 for the theory of operation. When power is applied the reset signal will go high causing the microprocessor to enter the reset mode. The CPU clk (generated on sheet 3) provides master timing for the 8088. It is a 5 Mhz clock signal. The reset signal must remain high for at least four clock cycles. The high to low transition triggers the 8088 to clear the registers and begin executing the instruction at absolute address FFFF0(H). The MIN/$\overline{\text{MX}}$ (minimum/maximum) mode input is connected to +5v forcing the 8088 into the minimum mode of operation.

The NMI (non-maskable interrupt) has a higher priority that the maskable interrupts (INTR). The NMI is edge triggered on a low to high transition. It is pulled to +5v and is routed to the expansion slots on the CPU board.

Timing and Status

The basic machine cycle for the 8088 is 4 clock periods T1, T2, T3 and T4 (See figure 26 page 3-46).

During T1, the 8088 places an address on the address bus (AD0-AD7,A8-A19). IO/$\overline{\text{M}}$, $\overline{\text{SSO}}$ and DT/$\overline{\text{R}}$ are valid. ALE will go to a low level.

During T2, AD0-AD7 will go to a high impedance state in preparation for a data transfer. $\overline{\text{DEN}}$ and $\overline{\text{RD}}$ or $\overline{\text{WR}}$ become valid to enable data onto the bus for transfer. AD0-AD7 will switch to the data bus (D0-D7).

During T3, the data is held valid on the data bus to allow it to stabilize and be read by either the 8088 or a selected peripheral device.

During T4, RD or WR becomes inactive and the data is latched into the 8088 or the selected device. $\overline{\text{DEN}}$ and DT/$\overline{\text{R}}$ go high and the peripheral device is deselected from the data bus.

Wait States

If a peripheral device has not completed a data transfer, it must inform the 8088 to enable the machine cycle to be extended. This is performed by bringing the READY line low before the beginning of T3. This will force the 8088 to insert additional clock periods (TW or wait states). The bus activity for a TW cycle is the same as a T3 cycle. So in effect, the 8088 simply inserts additional T3 periods. When the device has completed the data transfer, it brings the READY line high. This will allow the 8088 to terminate the TW cycles and continue on to the T4 cycle.

Idle Cycles

The 8088 will only execute a machine cycle when a data transfer is needed. When the 8088 is not executing a machine cycle, it executes idle cycles (T1). During these idle cycles, the 8088 continues to place data on the bus from the previous instruction.

Interrupt Acknowledge Cycle

INTR (interrupt request) is sampled during T4 to see if INTA cycles are to be entered. If an INTA cycle is to be entered, the PIC will drive the INTR line high. When the 8088 senses this high, it will issue 2 INTA cycles. During T2, if the IF (interrupt flag) is set (1), the 8088 will issue an INTA pulse. If the IF is reset (0), the 8088 ignores the INTR. When the 8088 issues the first INTA pulse, the address/data bus is set to a high impedance state from T2-T4. INTA will be active low during T2,T3 and T4 of each INTA cycle. In the second consecutive INTA cycle, a data byte is read from the PIC. This byte identifies the type of interrupt. It is used as a pointer into the table of interrupt routines in memory.

3.4.2 MASTER BUS CONTROL

The microcomputer utilizes a number of bus structures to control the flow of data through the microcomputer. These are both address buses and data buses. The block diagram below illustrates and identifies each of the major buses used in the computer.

The address bus, which allows the 8088 to address both memory and the I/O structure is divided into two parts. The AD0-AD7 bus and the A8-A19 bus. The 20 bit address bus allows the 8088 to address a maximum of 1 megabyte of memory. The A8-A19 bus will always contain address information and will be latched by the 8088 to allow it to address system memory, screen memory, boot memory,or any I/O device.

The AD0-AD7 bus is the multiplexed address and data bus used by the 8088. During the T1 cycle it will contain address bits and during the T3 cycle it will contain data bits. The design of the system allows for information to pass from or to the 8088 on this bus. Data placed on the AD0-AD7 bus will be transferred into one of the internal registers or from one of the internal registers. Address information on the AD0-AD7 bus will always be generated by the 8088.

The Boot ROM and the programmable interrupt controller (PIC), which provide data to only the 8088, are connected directly to the AD0-AD7 bus.

The BD0-BD7 data bus will carry the data byte from the AD0-AD7 bus to either memory (system or screen),or the Input/Output bus (ID0-ID7). Data is transferred from system memory to the 8088 by way of the BD0-BD7 bus to the AD0-AD7 bus.

The IDO-ID7 bus is the input/output bus for the microcomputer. In order for the 8088 to address a peripheral device (i.e. crt, parallel port, serial port) it must transfer the data byte onto the IDO-ID7 bus. Consequently all data transfers from the disk drive subsystem to the microcomputer will take place over the IDO-ID7 bus.

The DD0-DD15 data bus is the output bus for system memory. It will contain a data byte read from memory for the 8088 or it will contain a 16 bit dot pattern to be directed to the video output interface. The DD0-DD15 bus feeds directly into the video interface for character generation. When the 8088 is reading from memory it will transfer the data from either the DD0-DD7 byte or the DD8-DD15 byte onto the BD0-BD7 bus. The byte will then be placed on the AD0-AD7 bus where the 8088 can read it into one of it's registers.

The DC0-DC15 is the data output bus for the screen memory. The 8088 can write into screen memory by transferring a data byte from the BD0-BD7 bus onto either the DC0-DC7 bus or the DC8-DC15 bus. The CRT controller will access screen memory and read out address and attribute data onto the DC0-DC15 bus. The DC0-DC15 bus is divided into two parts: DC0-DC10, which is input to the system memory address bus; and DC11-DC15 which contain attribute data directed to the CRT interface circuit.

The MA0-MA10 bus is an address bus output from the CRT Controller Chip to address screen memory. Each address will represent a character position on the CRT. The address it will select in the screen memory will be the starting address for the dot pattern of the character to be displayed in that character position. Each character pattern in system memory will occupy 16 consecutive words.

The RA0-RA3 address bus addresses the 16 consecutive addresses that make up the character dot pattern in system memory.

ADDRESS/DATA BUS

The Address bus (sheet 2 of 100471 schematic) is broken down into 3 sections, AD0-AD7, A8-A15 and A16-A19. AD0-AD7 is the 8-bit data bus and the lower 8 bits of address. A8-A15 is the middle 8 bits of address. A16-A19 are the upper 4 bits of address.

Address bits A16-A19 are placed onto the A0-A19 bus by address latch 6M. 6M is chip selected by a low HLDA on pin 1. Pin 1 will be high only when another device brings HOLD high (pin 31) to request control of the bus. The address bits will be latched onto the bus during T1 when ALE makes a high to low transition. ALE is at a high level at the beginning of T1. It will go low at the end of T1, and remain low during T2,T3 and T4. ALE is connected to 6M pin 11, the E (enable) input. The output of 6M will follow the input when E is high. When E makes a high to low transition, the output will be latched at the level set up by the input.

Address bits A8-A15 will be placed on the A0-A19 bus by driver 7M. 7M is enabled by a low HLDA on pins 1 and 19 (G1 & G2 inputs). Address bits A8-A15 will be placed on the bus for the entire bus cycle.

Address/data bits AD0-AD7 will be placed on the A0-A19 bus by address latch 8K. The chip select for 8K (OC pin 1) is tied to ground, so it will always be selected. The address bits will be latched onto the bus during T1 by the high to low transition of ALE. The AD0-AD7 bus will be at a high impedance state during T2 of a bus cycle in preparation for a data transfer, and then become the data bus D0-D7.

Read Cycle

A read cycle begins at T1 with ALE, 7K (8088) PIN 25, going high. The memory location is placed on the AD0-AD7, A8-A19 bus (sheet 2 of 100471 schematic) by the 8088. IO/$\overline{\text{M}}$ and $\overline{\text{SS0}}$ become active. DT/$\overline{\text{R}}$ is low for a receive operation. ALE goes low and latches the address onto the A0-A19 bus.

At the beginning of T2 the 8088 will set the AD0-AD7 bus to a high impedance state. T2 is used mainly to change the direction of the AD0-AD7 bus during a read cycle. $\overline{RD}$ and $\overline{DEN}$ will go low.

$\overline{RD}$ from 7K pin 32, is routed to line driver 8L pin 2. 8L will be enabled by a low HLDA on pins 1 and 19 (G1 & G2). $\overline{RD}$ is output from 8L on pin 18, and routed to pin 6 of 8J. $\overline{DEN}$ is output from 7K pin 26 to input pin 15 of 8L. DEN is output from 8L pin 5, to pin 5 of 8J. With pins 5 and 6 of 8J both low, the output (pin 4) will be high.

This high is routed to 9J pin 10. 9J pin 12 is the output of 11L, pin 3. Pin 3 of 11L will be high when HLDA (pins 1 & 2) is low. 9J pin 13 will be high when the PIC is not selected. 9J pin 9 will be high when the BOOTROM is not selected. With all the inputs to 9J high, the output (pin 8) will be low. This low is routed to 10K pin 1 (OC), and will select 10K. ALE on pin 25 of 7K is routed to pin 8 of 8L. The output of 8L, pin 12, is routed through inverter 10D to pin 4 of 12D.

This inversion of ALE will be high from T2-T4. Pin 5 of 12D is from pin 6 of "NAND" gate 9D. Pin 5 of 9D is the output of 12D (pin 6). Pin 4 of 9D is $\overline{MLAT}$ (memory latch), which will be low from T3-T4 during a memory operation and high for an I/O operation. Pin 3 of 9D is $\overline{IOLAT}$ (I/O latch), which will be high for a memory operation and low from T3-T4 for an I/O operation. When either of these signals go low, 9D will produce a high out on pin 6. The high on pin 5 of 12D and $\overline{ALE}$ on pin 4, will produce a low output on pin 6 from T3-T4. 12D pin 6 is routed to 10K pin 11 (enable). The high to low transition on pin 11 will latch the data from the BD0-BD7 bus onto the AD0-AD7 bus to be read into the 8088.

Memory data enters directly on the BD0-BD7 bus. I/O data will enter on the ID0-ID7 bus and be passed on to the BD0-BD7 bus.

Data will be passed from the ID0-ID7 bus to the BD0-BD7 bus by transceiver 11K. The G input (pin 19) is the $\overline{IOBUF}$ signal from sheet 4 of 100471 schematic.

Decoder 9F will produce a low output on pin 7 (Y7) when IO/$\overline{M}$ is low and A17-A19 are high. IO/$\overline{M}$ will be low for I/O operations because the 9000 uses a memory mapped I/O structure, which means that the 8088 addresses I/O devices as memory spaces.

This low is routed to pin 1 (1G) of decoder 9H. With pin 1 low and A16 low, A15 will cause 9H to produce a low output on either pin 5 (Y1) or pin 4 (Y0). If A15 is high, pin 5 will be low. If A15 is low, pin 4 will also be low. 9H pins 4 and 5 are routed to 11J pins 10 and 11 respectively. If either is low, 11J pin 8 will be low. 11J pin 8 is routed to 11D pins 4 and 5. With a low on pins 4 and 5, 11D pin 6 will be high. This high is routed to 11D pin 10. $\overline{\text{EXTIO}}$ on pin 9 of 11D will be high. With pins 9 and 10 high, 11D pin 8 will be low. This low ($\overline{\text{IOBUF}}$) will enable 11K on sheet 2. I/O BUF goes low whenever an I/O device is addressed (6522 or INTEL DEVICE). The EXT I/O signal goes low (active) whenever external I/O occurs.

11K Pin 1 (DIR) is the direction input. If DIR is high, data flow is from A to B (BD bus to ID bus). If DIR is low, data flow is from B to A (ID bus to BD bus). ALE from 8L Pin 12 is routed to "NOR" gate 8J Pin 3. DT/$\overline{\text{R}}$ (low for receive) from 8L Pin 14 is routed to "NOR" gate 8J Pin 2. The ALE and DT/$\overline{\text{R}}$ signal will produce an output on Pin 1 of 8J that is low at T1 and high from T2-T4. 8J Pin 1 is routed through inverter 9L as a high at T1 and low from T2-T4. This low from 9L Pin 2 is routed to 11K Pin 1 to transfer the ID bus onto the BD bus at T2. The data on the BD bus is routed to 10K where it will be passed on to the AD bus as before by 12D Pin 6 at T3.

During T4, 8088 will take $\overline{\text{RD}}$ high and read the data into its input registers. $\overline{\text{RD}}$ going high will deselect 10K by disabling 8J (Pin 6). This will disable the BD bus. DT/$\overline{\text{R}}$ and DEN will go high.

WRITE CYCLE

A write cycle starts at T1 with ALE going high. The Memory address is placed on the AD0-7, A8-A19 bus by 8K. IO/$\overline{\text{M}}$ and $\overline{\text{SSO}}$ become active. DT/$\overline{\text{R}}$ is high for a transmit operation. ALE goes low and latches the address on the A0-A19 bus.

At T2 8K will again float the AD0-AD7 bus. $\overline{\text{WR}}$ and $\overline{\text{DEN}}$ will go low. DT/$\overline{\text{R}}$, high for transmit, from 8L Pin 14 is routed to "NOR" gate 8J Pin 2. The high on Pin 2 will produce a low out on Pin 1. This low on Pin 1 is routed to Pin 19 (G input) transceiver 9K. This low will select 9K. 9K Pin 1 (DIR) is HLDA which is low. This low on Pin 1 will transfer data from the B to A. (AD bus to BD bus).

BASIC SYSTEM TIMING
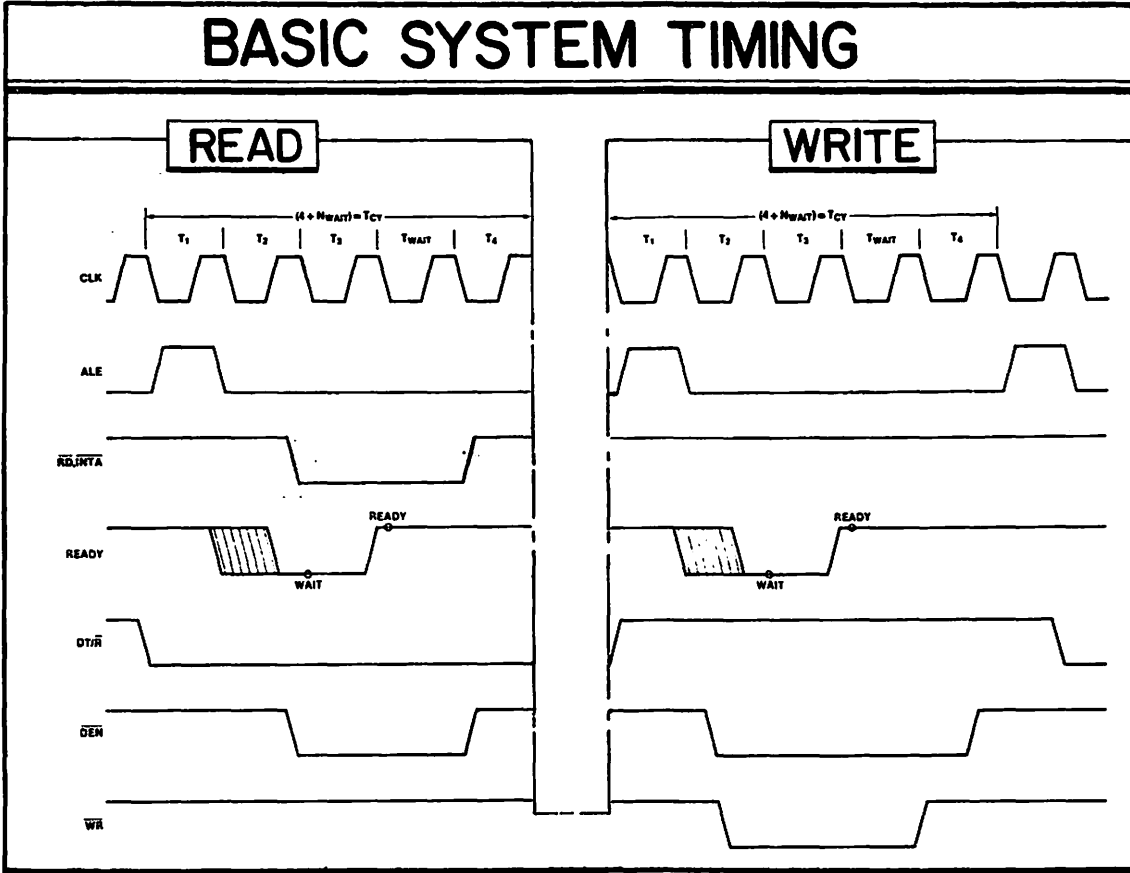
Figure 26

Memory data will exist on the BD0-BD7 bus. I/O data will be passed from the BD0-BD7 bus to the ID0-ID7 bus, then exit on the ID0-ID7 bus.

Data will be passed from the BD0-BD7 bus to the ID0-ID7 bus by transceiver 11K. DT/R from 8 L Pin 14 will be routed to NOR gate 8J Pin 2. This will produce a low out (Pin 1) which is routed to 9L Pin 1. 9L will produce a high out (Pin 2) and be routed to 11K Pin 1 (DIR). With a high on Pin 1, data will be transferred from A to B (BD bus to ID bus). 11K will be enabled by $\overline{IOBUF}$ low on Pin 19. The data will then be transferred to the I/O device.

9K will remain enabled until DT/R̅ goes low at a read cycle. 11K will remain enabled until $\overline{IOBUF}$ goes high. At T4, 8K will take $\overline{WR}$ and $\overline{DEN}$ high. The data will remain on the bus until another cycle is initiated.

3.4.3 MASTER CLOCK AND RESET CIRCUITS

MASTER CLOCK CIRCUIT

The Master Clock circuit is comprised of Crystal Y1, Transistors Q1 and Q2, Inverter 2K and J-K Flip-Flop 2L. These components combined with various discrete components produce 8 clock outputs which are used throughout the system. These clock outputs are as follows:

1) CLK 15
2) CLK 15A
3) CLK 15B
4) MPU CLK
5) CLK 5
6) $\overline{\text{CLK 5}}$
7) PHASE 2
8) $\overline{\text{PHASE 2}}$

The 15 MHZ Crystal (Y1) has its power supplied by the +12 volt supply. The output of the crystal is applied to the emitters of transistors Q1 and Q2. With transistor Q1 being on, the clock output is used to control the on-off condition and output of transistor Q2. This output, which is 180° out of phase with the crystal, is applied to inverter 2K at Pin 1. The output is inverted again by inverter 2K Pin 13 producing a $\overline{\text{CLK15}}$ output at Pin 12 which is supplied to the system.

The output at Pin 12 is also applied to inverter 2K at Pins 11 and 9 producing a CLK15A and CLK15B. The CLK15A signal is applied to the system and the CLK15B signal is used to develop the MPUCLK and the CLK5 and $\overline{\text{CLK5}}$ signals.

The CLK15B signal is applied to Pins 1 and 13 of the J-K Flip-Flop 2L. These two Flip-Flops, working in conjunction with each other and contained within the same package produce the MPUCLK at Pin 9 of 2L, and the $\overline{\text{CLK5}}$ signal at Pin 7 of 2L. The CLK5 signal is produced by simply inverting the $\overline{\text{CLK5}}$ signal at Pin 7 with inverter 2K, Pins 5 and 6.

The CLK15, CLK15A and B have a 50% duty cycle and the MPUCLK and $\overline{\text{CLK5}}$ clocks have a 60-40 and 40-60% duty cycles respectively.

The Phase 2 and Phase 2 signals are developed by using the $\overline{CLK5}$ signal as a clocking input to a divide by 5 counter (10 E). This produces an output signal which is off for 600 nanoseconds and on for 400 nanoseconds. The output, Phase 2, is inverted by inverter 10 D producing the Phase 2 signal. Both signals are then transferred and use'd by various circuits in the system.

RESET CIRCUIT

The Reset Circuit is comprised of one (1) Reset Switch, one (1) Timer Chip (NE 555) located at 12N, a inverter device (Located at 9L) and various discrete components. With the depression and release of the Reset Switch (located on the rear mainframe panel) the input signal to Pin 2 of the Timer Chip will go low, (0 volts). The Timer Chip is incorporated into the circuit to insure that the incoming reset signal is of sufficient duration and not an unwanted glitch. This input to the Timer produces a low output on Pin 3 of the device which is then passed to various circuits within the system as a RESET signal. The low (0 volt) reset signal is also inverted by component 9L and sent to system circuits as a RESET signal. The timer is also incorporated in the circuit to insure that the duration of the reset signal is 800 nanoseconds longer than the leading edge of the release of the reset switch.

3.4.4 BOOT ROM (READ ONLY MEMORY)

The Read Only Memory contains the self test routines and the initialization software for the CRT, the disk drive subsystem, and the bootstrap routine. The bootstrap routine loads the operating system from the diskette into memory. The physical location of the Boot Roms are in two (2) locations:5H and 7H. Both Boot Roms contain 4K of information each for a total of 8K. The Boot Roms are accessed when the 8088 microprocessor enters a reset condition or when the address bus consisting of address lines AD0 thru AD7 and A8 thru A19 contains FFFF0(H).

When the correct address (FFFF0(H)) is present on the address bus, the Boot Roms will be selected by the I/O state circuits consisting of latches 6M, 7M, 8K, Decoders 9F,9H and various discrete components.(Refer to sheets 2 and 4 of schematic 100471.) When IO/$\overline{M}$ is low, and address A19, A18, and A17 are all high, gate 9F will generate a low output on Y2(Pin 7). This low output will enable gate 9H. With 9H enabled addresses A16 and A15 (both high) will force the output at Pin 7 to be low. This low output ($\overline{RST}$) is used in conjunction with the $\overline{RD}$ signal to select the Boot Roms.

The process used to enable the chip select on each of the Boot Roms is accomplished through gates 8J, 8H, address line A12 and a jumper wire across E5 to E6. With $\overline{RST}$ and $\overline{RD}$ both low, a high output is produced at Pin 10 of 8J. This high output is applied to Pins 5 and 9 of gate 8H. This makes the accessing of each individual Boot Rom dependent upon the address A12 signal through jumper E5-E6 and gate 8H. Because of the configuration of gate 8H only one Boot Rom can be accessed at a time.

At address location FFFF0(H) the Boot Rom in 7H is selected and will contain the instructions to direct the 8088 to execute the programs contained entirely in the two (2) Boot Roms. The 8088 addresses the Roms directly using address lines A0-A12 on Pins 1-8 and 19-23 of the Boot Roms. The output of the Roms is placed on the AD0-AD7 bus where it is directed into the 8088 microprocessor.

3.4.5 SCREEN MEMORY

Screen Memory for the 9000 is contained in 4K Bytes of static memory which hold the addresses for the dot patterns which are stored in system memory. The screen memory is formatted in such a way as to hold 2048/16 bit words. These 2048 words each represent a character cell on the CRT display. The system memory contains the dot pattern necessary to generate a character on the screen. Each character will contain 16 consecutive addresses of dot information. In order to display the letter "A" on the CRT in the 1st character position on the screen, the starting address of the letter "A" dot pattern is placed in the 1st character position in screen memory.

When the HD46505 CRT Controller Chip addresses the 1st character position in screen memory, it will be directed to the starting address of the letter "A". The 16 consecutive words will be sent out to the video output control where they will be used to generate the letter "A" on the screen. (The output will be on lines DC0-DC15 of the 4K RAMS.) Should another letter be generated (Example "M") then the character address will go to the screen location for the particular character and output that information to the screen.

The address bus for screen memory is on lines AA0-AA10, and all data is either input or output on the DC0-DC15 data bus. The 8088 accesses the screen memory over lines A1-A11 (Refer to sheet 8 of 100471) and is controlled by the $\overline{RSO}$ signal which is generated by the I/O state circuitry. The CRT Controller Chip (9A) accesses the screen memory with lines MA0-MA10 through selectors 7A ,8A and 8B (Input pins 3,6,10 and 13).

To initialize the screen memory the 8088 must clear all screen memory addresses, then place the address of the dot pattern in the screen address corresponding to the character position on the display. To do this the 8088 begins by addressing screen memory space.(Refer to sheet 4 of 100471.) Whenever the IO/$\overline{M}$ signal into decoder 9F is low, and address A19,A18 and A17 are high, the output at Y7 (Pin 7) will be low. This low output enables decoder 9H. When the address A16 signal is high and the A15 signal is low, decoder 9H will produce a low output at Y2, (Pin 6) which is the $\overline{RSO}$ signal.

The low $\overline{RSO}$ signal (Refer to Sheet 8) is used in conjunction with the $\overline{EBLCA}$ signal and the AO signal to produce the proper $\overline{WE}$ signal for accessing screen RAM. When the $\overline{EBLCA}$ signal is high, meaning the CPU is accessing screen memory,the $\overline{RSO}$ signal and the AO signal are low, the Y2 output is low and the Y3 output is high (8C). The low Y2 signal is applied to gate 8D Pin 5. This in combination with a low $\overline{RAMWRT}$ signal will produce a low output on Pin 6 of 8D. This low output of 8D will write enable RAM 4A. To write enable RAM 6A $\overline{RSO}$ would be low and $\overline{EBLCA}$ and AO would have to be high. This would force a low output on 8D Pin 3 and would enable 6A and disable 4A. To transmit data into the Rams the DT/$\overline{R}$ signal must be high and the ALE signal must be low. This in combination with the low output of 8C Pin 6 will produce a low output at Pin 3 of gate 2C and set up the proper configuration for transfer of data from the BDO-BD7 bus to RAM.

The screen address is selected by selectors 7A,8A and 8B. When the EBLCA signal is low the selectors will select the "A" input. When EBLCA is high the selectors will select the "B" inputs. The screen memory is under 8088 control when the EBLCA signal is low. The screen address will originate on address lines A1-A11. When EBLCA is high the screen memory will be under CRT control and the screen address will originate on the MAO-MA10 bus lines. Further explaination and operation of the EBLCA signal will be presented in the section on Memory Timing.

The output of screen memory on lines DCO-DC15 is broken down into two segments: (1) DCO-DC10 are sent as address inputs to system memory and (2) DC11-DC15 are character attributes that are processed by the video output controller. (Refer to sheet 10 of 100471). These attributes are used to select the underlining, reverse video,or secret mode of character generation. The DT/$\overline{R}$ signal (in conjunction with the $\overline{EBLCA}$,$\overline{RSO}$ and AO signals) is used to determine the direction of data on transceivers 4C and 6C. With DT/$\overline{R}$ low the signals are passed from the DCO-DC15 bus to the BDO-BD7 bus and when high the direction is from the BDO-BD7 bus to the DCO-DC15 bus.

For transfer of data from the Rams to the DC0-DC15 bus the $\overline{EBLCA}$ signal will go low. This forces the output on 8C (Pins 6 and 7) to go high. With high outputs on Pins 6 and 7 the $\overline{WE}$ signal on Pin 21 of 4A and 6A will force the Rams into a read format. With $\overline{EBLCA}$ low transceivers 4C and 6C are shut off,and the output of gate 4M is also low. This sets the output enable ($\overline{OE}$) of the Rams and allows for transfer of data onto the DC0-DC15 bus.

3.4.6 SYSTEM MEMORY

System Memory is composed of 128K bytes of Dynamic Ram. The memory is expandable up to 896K bytes of memory with the addition of expansion boards. This section will deal with the 128K of memory located on the CPU board. For an explaination of the operation of the expanded memory refer to the section dealing with the expansion slots.

The 8088 and the CRT controller chip can access memory directly through the AB0-AB7 memory bus. Multiplexers 8F,8E,3A and 2A will determine whether the CRT or the 8088 accesses the memory.(Refer to sheet 9 of 100471.) On multiplexers 8F and 8E, when EBLCA is high, the outputs are at a high impedance state and the CRT controller is accessing system memory on the AB0-AB7 bus. When EBLCA is low the 8088 will access the system memory through the multiplexers. When the MUX signal is low the "A" inputs will be passed onto the bus. When the MUX signal is high the "B" inputs will be passed onto the memory address bus.

When the MUX signal is low and the EBLCA signal is also low the A1-A8 signals are placed on the AB0-AB7 bus. When MUX is high and EBLCA is low, the A9-A16 signals are placed on the AB0-AB7 bus.

When the EBLCA signal is low and $\overline{\text{LOWRAM}}$ is low,gate 8D goes low and the signal enables decoder 8C. Decoder 8C is used in conjunction with the A0 and $\overline{\text{RAMWRT}}$ signals to select either the odd or even byte in memory. When $\overline{\text{RAMWRT}}$ and A0 are low, the odd byte of memory is write enabled. When $\overline{\text{RAMWRT}}$ is low and A0 is high the even byte of memory is write enabled. When $\overline{\text{RAMWRT}}$ is high, the A0 signal is used to enable either the even or odd byte for read enable through gate 2C and latches 5C and 7C.

To enable the even byte for read enable the A0 signal must go low. This low forces the output at Pin 10 (Y2) to go low. This low output combined with a low INEBL signal will produce a low output at Pin 8 of gate 2C. This low output at Pin 8 will enable buffer 8C and allow the transfer of the even byte through buffer 5C. For the transfer of the odd byte of information, the A0 signal must go high. This high produces a low output on Pin 9 of 8C (Y3). This will enable and produce a low output at Pin 11 of gate 2C, enabling buffer 7C and allow the transfer of the odd byte.

When 5C or 7C are enabled the data bits on either DDO-DD7 or DD8-DD15 will be latched onto the BDO-BD7 bus. When MUX is low the memory timing circuits also generate a RAS signal (Row address select). This RAS signal will strobe the row address into the RAM. The row address will be composed of A1-A8 of the 8088 memory address. One memory clock cycle later MUX will be triggered high and a CAS (column address select) signal will be generated. This high signal will strobe the column address into the RAM. At this time the A9-A16 addresses will be on the memory bus.

Data bus BDO-BD7 is the input data bus for the system memory, and will be controlled by the 8088. For accessing of the system memory by the CRT, the EBLCA signal must be high. This will access the system memory through the octal edge triggered flip-flops 3A and 2A.

When CRAS ADDR is low (CRT strobe address) and CRT LATCH goes high, the ABO-AB7 bus will be composed of information from the RAO-RA3 and DCO-DC3 bus. When $\overline{CCAS}$ $\overline{ADDR}$ (CRT column strobe address) is low and CRT LATCH goes high, the ABO-AB7 bus will be composed of information from the DC4-DC10 bus. $\overline{CCAS}$ $\overline{ADDR}$ will occur one memory timing cycle after the $\overline{CRAS}$ $\overline{ADDR}$ signal.

The CRT controller can only read memory so the DDO-DD15 outputs from the memory will be directed to the video output control. This is accomplished by having the EBLCA signal forcing a high input to decoder 8C. This will produce a high output on Pins 9-12 and will shut off 5C and 7C through gate 2C.

The 128K byte of system memory, being composed of 64K x 1 dynamic ram chips, must be refreshed within 2 msec to prevent loss of data. To accomplish this the $\overline{REFRESH}$ will go low on sheet 9. When $\overline{REFRESH}$ is low 3D will be enabled and the refresh address from counter 2D will be placed on the ABO-AB7 bus. she refresh address generator at 2D is incremented when $\overline{REFRESH}$ and $\overline{MB}$ are low. At the same time $\overline{RAS}$ will be taken low by MA being set. When $\overline{REFRESH}$ is low the $\overline{CAS}$ signal will be disabled at 4H pin 1 on sheet 7. When $\overline{RAS}$ goes low a ROW ADDRESS REFRESH will take place.

The $\overline{REFRESH}$ signal is taken low on sheet 10 when EBLCA is low and DISP is low. At this time the processor will not be accessing memory and the CRT will have completed it memory access cycle. The DISP signal is generated by the CRT controller chip on sheet 8.

3.4.7 SYSTEM MEMORY TIMING

8088 Memory Access
(Schematic 100471 Sheet 7)

The 8088 will request access to system memory whenever both ALE and IO/$\overline{\text{M}}$ are low. Both low input signals at gate 8J will force a high out and set processor request flip-flop (3M) at the trailing edge of the next $\overline{\text{CLK5}}$ signal. Either $\overline{\text{LOWRAM}}$ or $\overline{\text{RSO}}$ will also be low to force a low out of gate 4M to complete the K input to flip-flop 3M. A low on the clear (CLR) input will reset the flip-flop when MA and $\overline{\text{EBLCA}}$ are high.

The PRQ high signal is routed as an input to "NOR" gate 3K. The one input forces a low output from 3K. This low is coupled with MA low, and MC low to set the MA cycle flip-flop (4K) .

Flip-flops 4K and 4J compose the memory cycle counter and generate the necessary timing signals to access system memory. All three flip-flops are controlled by CLK15A.

The next CLK15A signal following "NAND" gate (3L) going high sets the MA cycle flip-flop (4K). The high (Q) output of 4K for MA will set the MUX flip-flop at (3J) at the next clock 15B signal.

When MA is high it will also force a low out of "Nand" gate (4H) generating the $\overline{\text{RAS}}$ signal. $\overline{\text{RAS}}$ low will generate the Row address strobe for the memory chips when the MUX flip-flop is in the reset state. This selects the A inputs for output. The address bits A1-A8 will be placed on the AB memory address bus. On the next CLK15B the MUX flip-flop will set with the resultant high causing the B inputs to be selected when $\overline{\text{CAS}}$ goes low. This places address bits A9-A16 on the AB bus.

When PRQ is high it will lock out CRT request for memory by placing a high at "AND" gate (3L PIN 11). This high prevents a CRT request from being honored.

MEMORY TIMING

CLK I5B
CLK 5
ALE
PRQ
MA
MB
MC
$\overline{RAS}$
$\overline{CAS}$
MUX
CARRY
$\overline{CRQX}$
EBLCA

Figure 27

3-56
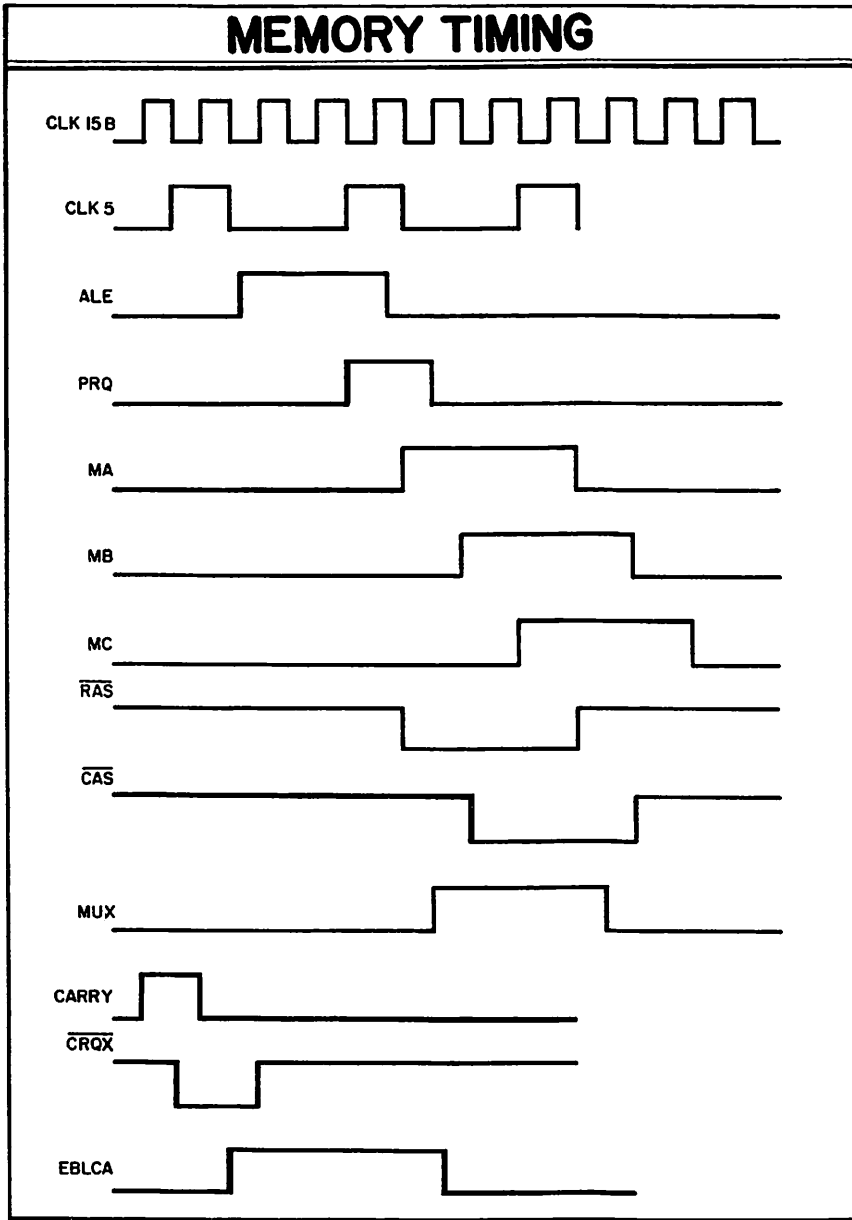
The PRQ flip-flop (3M) will be reset when MA and $\overline{\text{EBLCA}}$ are both high. $\overline{\text{EBLCA}}$ is the enable CRT access control signal. It will be high when the CRT does not have access to system memory. At the next CLK15A the MA high will set the MB flip-flop at (4K).

When MB is high it will couple with $\overline{\text{REFRESH}}$ at (4H) to generate the $\overline{\text{CAS}}$. $\overline{\text{CAS}}$ is the column address strobe for the system memory chips. On the next CLK15A clock pulse the MB high will trigger the MC flip-flop high. This flip-flop will remain high for three clock cycles before being reset by the low on the MB flip-flop.

The MUX flip-flop will remain set until the MA flip-flop is reset during the MC cycle. With MUX set, DT/$\overline{\text{R}}$ high and the MC cycle high the $\overline{\text{RAMWRT}}$ "AND" gate at 3H will go low allowing the memory chips to be written into.

The $\overline{\text{MLAT}}$ control signal will go low when $\overline{\text{MUX}}$ is high and $\overline{\text{MC}}$ is low with either $\overline{\text{LOWRAM}}$ or $\overline{\text{RSO}}$ low and EBLCA low. The resultant low for $\overline{\text{MLAT}}$ is "Nanded" with IOLAT at 9D of sheet 2. When $\overline{\text{MLAT}}$ goes low a high is forced out of 9D. This high is anded with ALE high at 12D and the resultant low transition will latch the octal latches at 10K, placing the data onto the AD0-AD7 bus. For a memory write sequence the data on BD0-BD7 will be written into the addressed memory location. For a read sequence the data byte on either DD0-DD7 or DD8-DD15 will be transferred onto the BD0-BD7 bus.

CRT MEMORY ACCESS

The CRT will request access to system memory whenever the carry output of counter 3N is high and EBLCA is low. The carry output of the counter will go high whenever the count reaches fifteen in HIRES or ten in standard character generation. The next clock will cause the carry output to go high. At CLK15B flip-flop 3M will set with the resultant low on the $\overline{\text{Q}}$ output being "Anded" with PRQ low and MA low.

If all three inputs are low the high out of 3L will set CRT access flip-flop 4J on the next CLK15B provided $\overline{\text{MC}}$ is high at the input to 3K pin 8. The high output on Q (EBLCA) enables CRT access and sets the MA flip-flop through "Nor" gate 3K. When MA goes high it will set the MUX flip-flop at 3J. The resultant high is "Anded" with EBLCA at 4L and the low output generates CRT LATCH.

With $\overline{MUX}$ high, EBLCA high, and DISPOFF high, gate 3H goes low to generate a low on $\overline{CRAS\ ADDR}$. The low $\overline{CRAS\ ADDR}$ enables the octal latch at 3A on sheet 9. When CRT LATCH goes high the DC0-DC3 along with RA0-RA3 bits will be latched onto the AB0-AB7 bus.

When the MUX flip-flop is set by MA high and CLK15B the $\overline{CCAS\ ADDR}$ signal will go low at 3H pin 6. The $\overline{CCAS\ ADDR}$ low will enable octal latch 2A on sheet 9. This will place the DC4-DC10 address bits on the AB0-AB7 bus.

The CRT LATCH signal will also latch the DD0-DD15 data output from system memory into the video output control latches on sheet 10. The CRT will access memory for read sequences only.

The data word DD0-DD15 will be latched into the parallel to serial converters 4D and 6D when the $\overline{SRLD}$ signal goes low. $\overline{SRLD}$ will go low when flip-flop 3J sets on sheet 7. Flip-flop 3J will set when the carry output of counter 3N goes high and CLK15A is active. The carry output will go high at every ten counts for standard character generation and every sixteen counts for high resolution graphics.

3.4.8 INTERRUPT PROCESSING

The real-time interrupt structure utilized in the Victor 9000 computer is controlled by an 8259 Programmable Interrupt Controller chip (PIC).

A real-time interrupt structure allows the microcomputer to execute its main program, and only deviate when a peripheral device requests service. Contrary to a polling interrupt structure, the real-time interrupt allows the microcomputer to operate in the most efficient manner.

When a device requires service, (i.e. keyboard entry, Disk Access) it will send an interrupt request to the microprocessor. At a breakpoint, predetermined in the chip design, the microprocessor will check for the interrupt request and if present, alter its execution. The microprocessor will determine the source of the interrupt, save the present contents of its registers, then execute the service routine to satisfy the demand of the device generating the interrupt request.

The 8259 PIC generates the interrupt request to the microprocessor, prioritizes interrupting devices, and directs the processor to the interrupt service routine via the interrupt byte.

A specific block of memory, called the Interrupt Pointer Table, is dedicated to interrupt processing. It is absolute memory addresses 0-255. During the system initialization process the 8259 is programmed with control words and interrupt bytes to be utilized during program execution.

Refer to schematic 100471 sheet 2. The 8259 PIC is located at 5K. The boot sequence initializes the 8259 PIC. At this time control data bytes are loaded into the device over the AD0-AD7 data bus.

In order to write to the PIC the microprocessor must generate the CS low on Pin 1. When $\overline{\text{IOD0}}$ goes low the PIC will be chip selected. (Sheet 4) The $\overline{\text{IOD0}}$ signal goes low when IO/$\overline{\text{M}}$ is low on Pin 4 of (9F) and A19, A18, A17 are all high. This forces the Y7 output of (9F) low. This low enables the decoder chip at (9H). When A16, and A15 are both low they will force a low output at Y0. This Y0 low will enable the decoder at (9H) labeled "Intel I/O".

With (9H) enabled by the Y0 low and A6 and A5 both low, the Y0 output will be forced low. This Y0 output at Pin 12 of (9H) generates the $\overline{\text{IODO}}$ signal to chip select the 8259 PIC. In the memory mapped I/O structure the PIC occupies address space E0000-E0001.

The IWR input (pin 2) to the PIC is used in conjunction with the CS and the A0 control lines to write data into the registers of the interrupt controller. (Refer to sheet 4 of 100471).

IWR will go low when the 8088 $\overline{\text{WR}}$ signal is low and flip-flop (9E) is set. The flip-flop will be set at the trailing edge of ALE when either the Y0 or Y1 output of (9H) is low. Either signal going low will force a high out of "Nand" gate (12D). The high output is routed to the set side of the flip-flop at (9E).

The set output of flip-flop at (9E) and the 8088 $\overline{\text{WR}}$ (inverted at 10J) are "Anded" at Pins 4 and 5 of (10J) to produce a low $\overline{\text{IWR}}$. The A0 address bit is latched at (8K) and routed to the A0 input of the 8259. When A0 is low during a write operation it is interpreted as an Initialization Command Word.

Refer to sheet 4. During the Initialization sequence, when (9E Pin 5) is set, the set output will set flip-flop (9E Pin 9) on the next Phase 2 clock. With the set output high, Phase 2 high, and QB high from 10E, a low output will be generated from 9D (Pin 12). This IOLAT low is "Or'd" at 9D (sheet 2) . The low IOLAT forces a high out of Pin 6 of 9D. That high is "Anded" with $\overline{\text{ALE}}$ to generate $\overline{\text{DLATCH}}$. The $\overline{\text{DLATCH}}$ low signal latches the 8 bits of data from the BD0-BD7 bus onto the AD0-AD7 bus at 10K. The PIC can then strobe the data byte into its internal registers.

The IRD signal will go low when the flip-flop at 9E is set, same as in a write sequence, and the 8088 read signal ($\overline{\text{RD}}$) is low. The 8088 $\overline{\text{RD}}$ is inverted at 10J Pin 11 and the two high inputs at 9 and 10 of 10J force a low output for $\overline{\text{IRD}}$.

The memory mapped address space for the 8529 PIC is E0000-E0001. All control words to be written are located in these addresses. Likewise, all register status bits will be read into these memory addresses.

The SP/EN signal on the 8259 is tied to +5V forcing
the PIC to operate in the master mode of operation. The
CAS0-CAS2 inputs are only used when the 8259 is placed in a
multiple 8259 PIC structure. For the Victor 9000 the
CAS0-CAS2 inputs are not connected to the system.

The Interrupt Request inputs (IR) are generated by the
various peripheral devices to signal the microprocessor
when they require data transfers in or out of the system.
All interrupt requests are edge triggered on the positive
edge of the interrupt request pulse. The following table
defines the IR inputs and their origins:

INTERRUPT LEVEL	SIGNAL	ORIGIN
IR0	SYN	DISK
IR1	COMM	7201
IR3	TIMER	8253
IR3	PARALLEL	6522 (ALL)
IR4		EXPANSION
IR5		EXPANSION
IR6	KBINIT	KEYBOARD
IR7	VINT	CRTC

INTERRUPT PROCESSING

When a peripheral device wishes to request an
interrupt it will pull its IR line high. Or as in the case
of the disk SYN line, it will drop it low then return to a
high state.

(Refer to schematic 100471 sheet 5). When the keyboard
interface chip 6522 (12L) requests service it will place a
low out on Pin 21 ($\overline{\text{IRQ}}$). This low is inverted at 14N
generating a high for KBINT.

The high KBINT for IR6 is an asynchronous input to the
PIC. The PIC will receive the interrupt request, insure
that no higher priorty interrupt is requesting service
(i.e. IR5, IR4) then generate a (high) INT signal to the
8088. The INT signal from the PIC is coupled directly to
the INTR input for the 8088. The INTR input is checked
during the last clock cycle of each instruction. The
Interrupt Enable flag must be set to allow the 8088 to
service an interrupt request for a peripheral device.

When the 8088 accepts the INTR (high) signal it will execute 2 INTA cycles. These active low signals are directed to the 8259. The first INTA signal notifies the PIC that the Interrupt request has been honored and the second Interrupt acknowledge (INTA) gates the Interrupt byte containing the interrupt type (0-255) onto the AD0-AD7 bus. The 8088 uses this type code to call the indicated interrupt service routine.

It is possible for more than one device to request an interrupt at the same time. At the same time the keyboard interrupt request went high, the parallel (IR3) interrupt request also went high. In this case the interrupt requests would be placed in the Interrupt Request Register (IRR). The PIC would prioritize the requests then generate its interrupt to the 8088 (Refer to sheet 6). When the 8088 responded to the interrupt from the PIC, the PIC would automatically place the interrupt byte of the higher priority interrupt request on the bus. When the Interrupt enable flag is returned to a set condition the 8088 will respond to the second interrupt signal from the PIC for the next priority interrupt request.

The Parallel Interrupt Request (IR3) is wire "Or'd" with all the IRQ of the 6522's used in the microcomputer. That includes the 3 disk 6522's, the User Port, the Codec, the expansion bus, and the parallel output port. Whenever any of these devices requests any interrupt the IR3 line will go high. The 8088 will then poll the devices individually to determine the source of the interrupt request.

The INTA signal resets flip-flop 9E (Pin9) on sheet 4. The low on the set side of 9E pin 9 will disable the CS decoder during an interrupt byte transfer between the PIC and the 8088.

3.4.9 KEYBOARD INTERFACE

The keyboard interface for the 9000 is located on sheet 5 of schematic 100471. The keyboard is connected to to the 9000 by J6.

Data transmission between the keyboard (KB) and the 9000 is in serial format. Data transmission is in 9-bit form. The first 8 bits are a byte of data. The last bit is a stop bit. The least significant 7 bits of the data byte are the code for the key number. The most significant bit (MSB) is a status bit which indicates an open or closed key switch condition. If the MSB is high, a closed key is indicated. If the MSB is low, an open key is indicated.

During a data transfer, the KB interface will operate in 3 different states or modes. These 3 states will control the operation of the 6522 (Versatile Interface Adapter) through software. The states will be programmed into the 6522 (12L) by the 8088. State 0 is for data transfers. States 1 and 2 are for the transfer of the stop bit. 3 interrupts will be generated each time a data byte and a stop bit are transferred. One for the data byte, one when the stop bit is at a low level, and another when the stop bit is at a high level.

In state 0, the 6522 will be programmed to operate in the shift register mode. In this mode, CB1 (pin 18) is an external clock pulse input which shifts the data received on CB2 (pin 19) into its shift register. When the shift register is full (8 bits shifted in) the 6522 will issue an interrupt to the processor.

In state 1, the 6522 will be programmed for PA6 (pin 8) to be a low input pin and CB1 (pin 18) to detect a negative edge. The 6522 will issue an interrupt when a low is sensed on CB1 (pin 18) and PA6 (pin 8).

In state 2, the 6522 will be programmed for PA6 to be a high input pin and CB1 to detect a positive edge. The 6522 will issue an interrupt when a high is sensed on CB1 and PA6.

DATA BITS

When the KB has a byte of data to send, it will send the first data bit (KBDATA). The KBDATA is routed to pin 6 of J6. From J6 it is routed to VIA 6522 (12L) pins 8 (PA6) and 19 (CB2). After sending the data bit, the KB will take KBRDY (key board ready) low. $\overline{\text{KBRDY}}$ is routed to pin 5 of J6. The low on pin 5 is routed to inverter 14N (Pin 5). The high output of 14N (pin 6) is routed to D-type flip-flop 17N (Pin 12).

With a high on pin 12, 17N will set at the next positive transition of the PHASE 2 clock (pin 11). The low out on the $\overline{\text{Q}}$ (pin 8) is routed to "NAND" gate 11L pin 9 and to 12L pin 18 (CB1). (12L pin 21) IRQ (Interrupt Request), will be high until a byte of data is received, it will then go low to interrupt the 8088. Pin 21 of 12L is routed to 11L pin 10 and through inverter 14N to 11L pin 13.

By routing IRQ as an input to 2 "NAND" gates in 11L, of which one input is inverted, one gate will be maintained off when IRQ is low and the other will be maintained off when IRQ is high. For the gate not maintained off, IRQ will be an enabling input. The status of the other input pin will determine if the $\overline{\text{KBACK}}$ (Keyboard Acknowledge) is generated. In this configuration, the "NAND" gate with the non-inverted IRQ input will generate $\overline{\text{KBACK}}$ for the data bits. The "NAND" gate with the inverted IRQ input will generate the $\overline{\text{KBACK}}$ for the stop bit. The output of the "NAND" gates are high (gate off) to generate a $\overline{\text{KBACK}}$.

When IRQ is high, pin 10 of 11L will be high and pin 13 of 11L will be low. The low on 11L pin 13 will produce a high output on pin 11. With the low from the $\overline{\text{Q}}$ output of 17N on pin 9 of 11L, 11L will have a high output on pin 8. The high on pins 8 and 11 is routed to pins 5 and 4 of "OR" gate 11L, producing a low out on pin 6. 11L pin 6 is routed to pin 4 of J6 ($\overline{\text{KBACK}}$). $\overline{\text{KBACK}}$ is routed to the KB to acknowledge the transitions of $\overline{\text{KBRDY}}$. After receipt of the $\overline{\text{KBACK}}$, the KB will drive the $\overline{\text{KBRDY}}$ high. $\overline{\text{KBRDY}}$ high will clear 17N at the next positive transition of PHASE 2 clock.

KEYBOARD INTERFACE
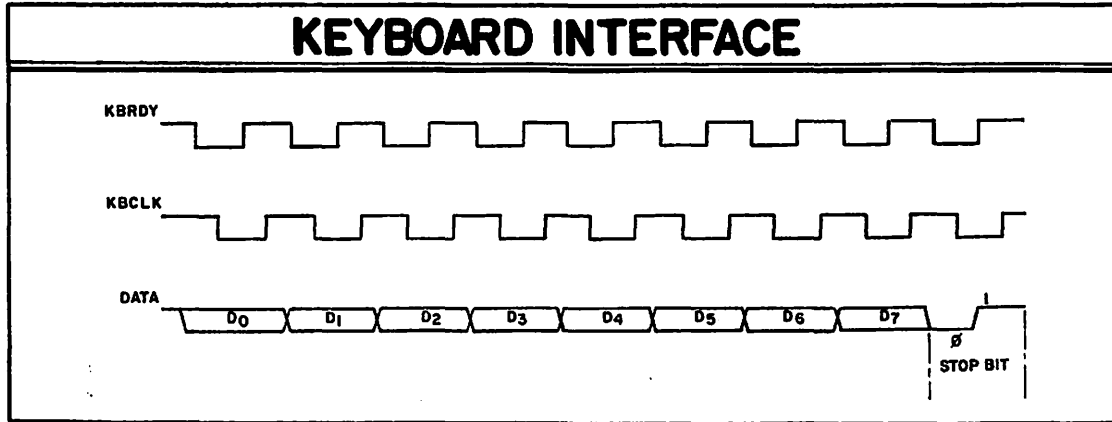
Figure 28

The high from the Q output (pin 8) is routed to 12L pin 18 and to 11L pin 9. The low to high transition at 12L pin 18 will shift the data bit into the Shift Register input at pin 19 (CB2). The high on 11L pin 9 will produce a low output on pin 8. The low on pin 8 is routed to 11L pin 4 producing a high $\overline{KBACK}$ output on pin 6. After receipt of the positive transition of $\overline{KBACK}$, the KB will send the next data bit and again take $\overline{KBRDY}$ low.

The changing states of $\overline{KBRDY}$ on the D input of 17N, will produce a keyboard clock (KBCLK) on the $\overline{Q}$ output. KBCLK is routed to pin 9 of 11L and to pin 18 of 12L. Each time KBCLK goes low, the low on pin 9 of 11L will produce a high output. The high output of 11L (pin 8) is routed to 11L pin 5. The high on pin 5 will produce a low output on pin 6 ($\overline{KBACK}$). When KBCLK is high, pin 8 of 11L will be low. This low on pin 5 of 11L will produce a high $\overline{KBACK}$. Each positive transition of KBCLK on pin 18 of 12L will shift the KBDATA (pin 19) into the shift register of 12L.

When 8 bits have been shifted in, 12L will take IRQ (pin 21) low. This low is routed to 11L pin 10 to maintain the output (pin 8) at a high level. It is also routed to inverter 14N pin 1. The low to high transition on pin 2 of 14N is routed to the 8088 as KBINT (keyboard interrupt). The 6522 at 12L will then place the data from the shift register onto the ID0-ID7 bus to be processed by the 8088.Pin 2 of 14N is also routed to pin 13 of 11L.

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STOP BIT

The stop bit for the data stream is low when $\overline{KBRDY}$ is low, and goes high when $\overline{KBRDY}$ goes high. Following the transmission of the data byte, the KB will drive KBDATA low. This low will be routed to 12L pin 8 (PA6). The KB will then drive $\overline{KBRDY}$ low. The low will set 17N at the next positive transition of $\overline{PHASE\ 2}$ clock. The low from $\overline{Q}$ of 17N is routed to pin 18 (CB1) of 12L. If both inputs are low, 12L will generate an interrupt (low on pin 21). This low is routed through inverter 14N to pin 13 of 11L. If pin 12 of 11L is low, 11L will produce a high output on pin 11. Pin 12 of 11L is the output of 12L pin 11 (PB1). The high from 11L pin 11 is routed to pin 4 of 11L. A high on pin 4 of 11L will produce a low $\overline{KBACK}$ to inform the KB of the low stop bit being received. If the $\overline{KBRDY}$ and the KBDATA are not low, no interrupt will be sent and no $\overline{KBACK}$ will be generated.

After receipt of the $\overline{KBACK}$, the KB will drive KBDATA and $\overline{KBRDY}$ high. The high KBDATA is routed to 12L pin 8 (PA6). The high $\overline{KBRDY}$ will clear 17N at the next positive transition of $\overline{PHASE\ 2}$ clock. The high from the Q of 17N is routed to pin 18 (CB1) of 12L. If both inputs are high, 12L will generate an interrupt (low on pin 21). This low is routed through inverter 14N to pin 13 of 11L. If pin 12 of 11L is low, 11L will produce a high output on pin 11. Pin 12 of 11L is the output of 12L pin 11 (PB1).

The high from 11L pin 11 is routed to pin 4 of 11L. A high on pin 4 of 11L will produce a low $\overline{KBACK}$ to inform the KB of the high stop bit being received. If the $\overline{KBRDY}$ and the KBDATA are not low, no interrupt will be sent and no $\overline{KBACK}$ will be generated

When 12L takes IRQ high, the high will be routed to pin 9 of 11L. 11L pins 9 and 10 will both be high. With both inputs high, 11L pin 8 will be low. This low is routed to pin 5 of 11L. A low on pin 5 will produce a high output on pin 6 ($\overline{KBACK}$). When $\overline{KBACK}$ goes high, the KB will enter the idle state until another data byte is to be transferred.

3.4.10 HD46505 CRT Controller Chip

The HD46505 CRT Controller Chip is used to interface the master processor to a CRT raster display. The programmable features of the chip allow its application to a wide range of display types.

The CRT Controller Chip handles all timing requirements for the CRT unit, the cursor(both for position and blinking) and the refresh requirements. The chip contains 17 control registers that are programmed by the CPU (8088) to handle CRT interfacing.

CRT Chip Description

The HD46505 CRTC chip is located on sheet 8 of 100471. All interface chips for the CRT display are located with the HD46505 on the CPU board. The CRTC can be broken down into two (2) groups of signals. The 8088 control side and the CRT control side.

8088 Interface Signals

The CS signal, which is active low, enables the CRTC for read/write operations to the internal registers. The pin is controlled by $\overline{CS0}$ from the I/O state circuits. The $\overline{CS0}$ signal will be low when the 8088 addresses memory address space E8000-E8001.

When IO/$\overline{M}$ is low (Refer to sheet 4 of 100471) and A19, A18 and A17 are high, Pin 7 on 9F will go low. This low enables 9H (Pin 1). When A16 is low and A15 is high, a low output is developed on Pin 5 of 9H (Y1 output). This low output (E8000) enables decoder chip 10H at Pin 4 (G2A input). The low output at Pin 5 (Y1) of 9H also forces a high output at Pin 3 of gate 12D. The high output of gate 12D will set flip-flop 9E at the trailing edge of the ALE signal which comes in at Pin 1.

The next phase 2 clock pulse (which is developed by the CLK5 and devices 10E and 10D (Pin 2)) will cause the second flip-flop (9E) at Pin 9 to set. The set output of 9E is routed as an enable (high) for CSEN. The A8 bit (low) will enable 10H at the G2B input allowing the A7,A6 and A5 address bits to be decoded at 10H. When A7,A6 and A5 are all low, the Y0 output (Pin 15) of 10H will go low, generating the chip select ($\overline{CS0}$) for the CRTC chip.

Listed below are the input requirements for the selection of the $\overline{CSO}$ signal:

```
A19 A18 A17 A16 A15 ......  A8 A7 A6 A5
 1   1   1   0   1           0  0  0  0
```

The R/W signal controls the direction of data transfer between the CRTC and the 8088. When R/W is high (Pin 22 of the HD46505),data is read from the CRTC. When R/W is low, data is written into the CRTC. The R/W signal to the CRTC is controlled by the 8088 $\overline{WR}$ signal (Pin 29). This $\overline{WR}$ signal coupled with the CS signal will write information into the CRTC. The timing base is the Phase 2 clock for transfer operations between the CRTC and the 8088.

The RES input at Pin 2 of the CRTC is the reset signal from sheet 3 of 100471.(Developed by the depression of the reset switch located on the rear panel of the unit). During a reset operation all counters in the CRTC are cleared, all outputs go low, and the control registers in the chip are not affected.

The D0-D7 data bus is connected to the microcomputer ID0-ID7 data bus. All control bytes are loaded into the CRTC via the ID0-ID7 bus lines (Pins 26 thru 33). The RS input (Pin 24) is controlled by the A0 address bus of the 8088. This is the register select input for the CRTC. When RS is low,the address register is selected; when RS is high, the control registers are selected. While the RS signal is low, the address register is used to determine which of the control registers are selected.

CRT Display Interface Signals

The CLK input (Pin 21) is a character clock signal which defines the character timing for the CRTC display operation. The CLK input is controlled by CRTCLK (from sheet 7,3N Pin 11).CRTCLK is generated each time the QD output (Pin 11) goes high. The counter is loaded with a count generated by the HIRES signal (From Pin 17 of the CRTC). When HIRES is low, the counter input will be 0110. At each CLK15 the counter will be incremented. The CARRY output of the counter is routed back through inverter 4N to reload the base count (0110) each time the counter generates a carry.

The LPSTB signal (Pin 3) is the light pen strobe signal to mark the position of the light pen on the screen. MA0-MA10 provide addressing for periodically refreshing the CRT display. These signals are routed as address inputs to screen memory through latches 7A,8A and 8B. The MA12 signal is used to determine the location of the font cell memory. When MA12 is low, the font cells are located in the lower 64K of system memory. When MA12 is high, the font cells are located in the upper 64K of system memory.

The MA13 signal is used to enter the HIRES (High Resolution) mode of CRT display. This determines the base count of counter 3N (0110). When in the standard character mode the character cell is 10 dots wide. The count change for high resolution (0000) will cause the cell to be 16 dots wide. The standard character cell of 10x16 dots is changed to 16x16 when MA13 is high.

The RA0-RA3 signal lines are the raster address bits for the system memory (Pins 35-38 of the CRTC). These bits are latched during CRT access to system memory to provide bits AB0-AB3. They will represent each of the consecutive sixteen memory addresses that make up a character or graphics cell on the screen.

The CUDISP output will display the cursor on the screen. It is an active high signal that is inhibited while the DISPTMG signal (Display Time) is at a low level. Both signals are routed to the video output control circuits.

The HSYNC and VSYNC provide horizontal and vertical synchronization for the screen. They are passed directly to the video control board from Pins 39 and 40 of the CRTC. The VSYNC also generates the VINT signal which can be used as an interrupt to the 8088 via the Programmable Interrupt Controller (5K Pin 25).

The DISPTMG signal is active high and defines the display period in horizontal and vertical raster scanning. The DISP output (Pin 18) when high, will enable the video output signal to the video control board.

3.4.11 CRT INTERFACE

The CRT Interface receives the 10 or 16 bit word from system memory for character generation, converts it to a serial pulse string then converts the pulses to a video signal compatible with the video control board in the CRT module. The Character Attributes are intergrated into the video control for low intensity, reverse video, secret, or underline.

The CRT interface is contained on sheet 10 of schematic 100471.

The DD0-DD15 data bus bits from system memory are latched onto the LD0-LD15 bus by the rising edge of CRT LATCH at 5D and 7D. At the same time the DC11-DC15 attribute bits, read from screen memory, are latched into 9C. The DISP and CURSOR control signals are received from the CRTC chip and latched at 9C along with the attribute bits.

The LD0-LD15 bus feeds the parallel to serial converter chips 4D and 6D. When SRLD goes low the parallel inputs will be latched into the converters on the next clock pulse. The CLK15A input will clock the serial pulse string out on its rising edge.

On the rising edge of SRLD the attribute bits , cursor and DISP are latched into 10C and the previous word's attribute bits are latched into 11C. The DISP bit is inverted by 11D then latched into 11C. The underline attribute bit, DC13, is "Anded" with LD15 and the inverted output will be latched into 11C. When the Underline bit is set and the LD15 bit is set the scan line will be white, otherwise the lower ten bits of the word will be displayed.

When the underline attribute is not set it will force a one to be latched into 11C. The SECRET attribute, when set, will disable the video circuit and the character will not be displayed. When SECRET is set, the one is latched into 11C. This high is inverted at 13B "Nor" gate and provides a low input to 4H. This low disables 4H, blocking the serial data string from being processed by the interface circuits.

The DISP signal (low) provides the enable for the data selector at 12C. The CURSOR signal provides the A input, the UNDLN signal provides the B input, and the RVS provides the C input.

The serial data string is "Nanded" with the SECRET attribute at 4H then routed to the inputs, in both inverted and non-inverted form, of the data selector at 12C. When CURSOR is low, UNDLN is high (underlining not active) and RVS is low, the data selector will select the D2 input and direct it to the W output. The W output is the complemented D inputs. The data string will be inverted by 4H then inverted again by 11A and inverted a third time by the data selector.

When the data is to be displayed in reverse video mode, the RVS bit will be high, UNDLN will be high and CURSOR will be low. This configuration will select the D6 input for output on W. The D6 input is the data string inverted by 4H only. To display the CURSOR the CURSOR bit will go high selecting the D1 input which will force a constant high out of W.

The LOWINT attribute is routed from 11C to the D input of flip-flop 13C. On CLK15A the flip-flop will set and the reset output will go low. This low is inverted by 13D and provides a bias for transistor Q4.

The set output of 13C, which is the W output of the data selector clocked by CLK15A, is inverted at 13B, pins 8 and 6. The outputs of 13B are routed to the emitter of Q5. Transistor Q5 drives the video signal to the video control board in the CRT module.

The Horizontal Sync (HORIZ) and Vertical Sync (VERT) are routed directly from the CRTC chip to the CRT connector.

BRIGHTNESS AND CONTRAST CONTROL

The brightness and the contrast are controlled by the operator through the keyboard. This is accomplished by programming a 6522 with three bits and processing the three bits through a resistor network to influence either the brightness control signal or the video control signal.

The eight levels of either brightness or contrast are programmed into 6522 at 12L,(Sheet 5 of 100471). PB2, PB3, and PB4 control the brightness while PB5, PB6, and PB7 control the contrast. The bits are programmed into the ORB register at memory address E8040. Setting all "zero's" for either brightness or contrast will provide the level at it's minimum and all "one's" set the levels to their maximum.

The three bits for brightness pass through resistor network R23, R25, R26, R24 to provide a voltage level to the emitter of Q3. At maximum brightness the level is approximately 1.2v and is at .5v level for minimum brightness. The collector of Q3 will be at a -150v for minimum brightness and a -100v for maximum brightness.

The three contrast bits are inverted by 13D and pass through resistor network R27, R28, R29 where they provide a voltage level to the emitter of Q4.
The CRT connector configuration is contained in the following table.

CRT CONNECTOR

PIN	SIGNAL
1	VIDEO
2	VIDEO GND
3	+12VV (REGULATED 12 VOLT)
4	GND
5	BRIGHTNESS
6	VSHIELD
7	VERTICAL SYNC
8	GND
9	HORIZONTAL SYNC

Table 3

3.4.12 REAL TIME CLOCK

The real time clock circuit provides for a programmable interrupt interval. The interrupt would allow the processor to update and maintain a real time clock program in the system. The entire clock circuit requires a single 8253 programmable interval timer chip.

The real time clock circuit is contained on sheet 11 of schematic 100471. The 8253 counter is addressed when its chip select is low ($\overline{CS}$) which is controlled by the $\overline{IOD1}$ signal from sheet 4.

The memory mapped I/O space for the timer is E0020-E0023.(Refer for sheet 4). When the timer is addressed IO/$\overline{M}$ will be low and A19, A18, and A17 will be high forcing the Y7 output of 9F low. This low enables decoder 9H. A16 and A15 will both be low, forcing the Y0 output low on 9H. This output enables the second 9H decoder. On the input to the decoder A6 will be high and A5 will be low forcing the Y1 (IOD1) output low. When $\overline{IOD1}$ goes low the 8253 timer is selected for either a read or write operation.

The RD line to the 8253 is tied to +5v and the WR line is controlled by the IWR control signal. IWR goes low on sheet 4 when the 8088 WR signal is low and the flip-flop at 9E pin 5 is set. The flip-flop at 9E will set on the falling edge of ALE when either the Y0 (E0000) or Y1 (E8000) output of 9H is low.

The 8253 contains three internal counter circuits and each is addressed by the A0 and A1 address bits. The selection is determined by the following table:

WR	A0	A1	SELECTION
0	0	0	Load counter no. 0
0	0	1	Load counter no. 1
0	1	0	Load counter no. 2
0	1	1	Write Mode Word

When WR and RD are both high the 8253 is in a no-operation 3 state mode. The real time clock circuit is addressed at memory address E0022 and the control word register is addressed at E0023.

Each counter consists of a single, 16 bit, pre-settable down counter. The count register is loaded with either a byte or word over the ID0-ID7 bus.

The counter will decrement on each clock input for its counter (CLK0, CLK1,CLK2). The CLK2 input is a phase 2 clock divided down by the LS90 counter chip at 11E. The QD output of 11E provides a 2 usec pulse every 8 usec to clock the real time clock counter.

The GATE2 input is tied to +5v and is not used. The OUT2 line will go high when terminal count is reached and will remain high until the counter is re-written by the CPU. The TIMER output is an interrupt input to the 8259 PIC on sheet 2.

3.4.13 PARALLEL PORT

The parallel port is designed specifically for 8 bit data transfers to a peripheral device. The port can be programmed to operate in a standard Centronics parallel configuration or an IEEE-488 configuration.

The port consists of a 6522 Versatile Interface Adapter chip and a pair of Octal Bus Transceivers (75160 & 75161),(located on sheet 6 of 100471). The 6522 for the parallel port is chip selected when address space E8020-E802F is addressed by the 8088.

Refer to sheet 4. When the IO/M signal is low and A19, A18, and A17 are all high decoder 9F will be enabled and will force a low out of the Y7 output. This low enables decoder 9H. The A16 line will be low and the A15 line will be high which will force the Y1 (E8000) output low enabling the G2A input to decoder 10H. When 9E pin 9 is set G1 will be enabled. A8 will be low enabling the G2B input to 10H. A7 will be low, A6 will be low and A5 will be high generating a low at the Y1 output. This low, $\overline{CS1}$ will chip select the 6522 for the parallel port.

When $\overline{CS}$ is low the 6522 will be accessed by the 8088 for either a read or write operation. When the $\overline{WR}$ signal is low the 8088 will write data into one of 16 internal registers. The A0-A3 address bits select the internal registers for reading or writing. The data byte is placed on the ID0-ID7 bus for transfer into the 6522 register.

The 8 bit data output is programmed into the Peripheral Port A (PA0-PA7) while the control signals are programmed into the Peripheral Port B (PB0-PB7).

The chip will be initialized by addressing the Data Direction Register A (DDRA) and setting the 8 bits to outputs. The Data Direction Register B (DDRB) will be initialized to configure the control signals to either inputs or outputs dependent upon the protocol of the port configuration desired.

The control signals can then be loaded into the Output Register B (ORB) and the data byte loaded into Output Register A (ORA).

The following table defines the memory addresses used
to address each of the above registers.

REGISTER	MEMORY ADDRESS
ORB/IRB	E8020
ORA/IRA	E8021
DDRB	E8022
DDRA	E8023

The CA1, CA2 lines (Peripheral Port A control Lines)
are used as interrupt inputs to the 6522. The CA1 interrupt
indicates the device is ready for data. The DAC line
controls the CA2 line to generate an interrupt when the
data was accepted by the device.

The Interrupt Request (IRQ) line will go low whenever
the internal interrupt flag is set and the corresponding
interrupt enable bit is a logic 1. The interrupt enable
register is address E802E.

The 75160 and 75161 Octal General Purpose Interface
Bus Transceivers control the transfer of data out of the
port. The 75160 handles the 8 line data bus while the 75161
handles data transfer and bus management.

The PE signal on the 75160, tied low, causes the
outputs to have the characteristics of open collector
outputs. The TE signal will be high for the transfer of the
data byte out to the peripheral device. The TE signal is
controlled by the 6522 at 12L on sheet 5. It is programmed
as the Talk/Listen signal out of the PB0 bit.

The 75161 controls the flow of control signals between
the 6522 and the peripheral device. The Direction Control
(DC) is tied to ground. When TE is high the 75161 is
configured as in Table 4. When TE is low the 75161 is
configured as in Table 5.

SIGNAL	DIRECTION
ATN	TRANSMIT
EOI	TRANSMIT
REN	TRANSMIT
IFC	TRANSMIT
SRQ	RECEIVE
NRFD	RECEIVE
NDAC	RECEIVE
DAV	TRANSMIT

TABLE 4

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```
ATN                    TRANSMIT
EOI                    TRANSMIT/RECEIVE*
REN                    TRANSMIT
IFC                    TRANSMIT
SRQ                    RECEIVE
NRFD                   TRANSMIT
NDAC                   TRANSMIT
DAV                    RECEIVE
```

TABLE 5

* EOI will receive when ATN is high and transmit when
ATN is low whenever DC and TE are in the same state.

The SRQ/BUSY signal from the peripheral device is
routed to the CA2 input of 6522 at 12L on sheet 5. It will
be used to set the interrupt flag when the peripheral
device is busy.

The pin configuration for the parallel port is listed
in the following table.

PARALLEL PORT INTERFACE J14   (GENERAL SPECIFICATIONS)

```
 1   Strobe                        19 return
 2   Data 1                        20 return
 3   Data 2                        21 return
 4   Data 3                        22 return
 5   Data 4                        23 return
 6   Data 5                        24 return
 7   Data 6                        25 return
 8   Data 7                        26 return
 9   Data 8                        27 return
10   NRFD/ACK                      28 return
11   SRQ/BUSY                      29 return
12   NC
13   SEL/DAC
14   GND
15   PI/EOI
16   GND
17   SHIELD GND
18   NC
30   NC
31   NC
32   SEL/DAC
33   GND
34   REN
35   ATN
36   IFC
```

3.4.14 SERIAL PORTS

The Serial Ports are designed specifically for data transfer to or from a peripheral device. The circuit consists of a 7201 Multiprotocol Serial Communications Controller (MPSC), a 6522 Versatile Interface Adapter (VIA), a 8253 Programmable Interval Timer and various discrete components.

The 7201 for the serial ports is chip selected when address space E0000 is addressed by the 8088. The chip select input is on Pin 23, and is selected through addresses A5 thru A8, A15 thru A19 and the IO/$\overline{\text{M}}$ signal. (refer to sheet 4 of 100471.) When the IO/$\overline{\text{M}}$ signal is low and A19, A18 and A17 are high, decoder 9F will produce a low output at Pin 7 ($\overline{\text{Y7}}$). This low output combined with a low input from A16 and A15 will produce the E0000 output at Pin 4 ($\overline{\text{Y0}}$) of decoder 9H. The E0000 output of decoder 9H is combined with a high input from address bit A6 and a low from A5 to produce the $\overline{\text{IOD2}}$ output (low) at Pin 10 of decoder 9H. It is this low output of the decoder ($\overline{\text{IOD2}}$) that is used as the chip select for the 7201 at Pin 23. (Refer to page 11 of 100471.)

With Pin 23 low, the MPSC is selected for transfer of data or commands during a read or write cycle. The 7201 also has two channels for transferring data. For accessing these channels the proper input must be applied at Pin 25 (Channel Select). With a high input applied at Pin 25, the B channel is selected for transfer of data or commands. A low input will select the A channel for transfer of data or commands. The input for channel selection is the A0 input from the 8088.

For reading or writing information in or out of the 7201, the $\overline{\text{WR}}$ or $\overline{\text{RD}}$ inputs at Pins 21 or 22 respectively, combined with the $\overline{\text{CS}}$ signal must be low. This is accomplished by producing a $\overline{\text{IRW}}$ and $\overline{\text{IRD}}$ signals. (Refer to Page 4 of 100471.)

To produce the $\overline{\text{IRW}}$ and $\overline{\text{IRD}}$ signals, the $\overline{\text{WR}}$ and $\overline{\text{RD}}$ signals from the 8088 must be clocked through gate 10J. Refer to sheet 4 of 100471. As previously discussed, decoder 9H produces a low output at Pin 4 ($\overline{\text{Y0}}$). This low output produces a high output at Pin 3 of gate 12D. The high output of gate 12D is supplied to flip-flop 9E, producing a high output at the trailing edge of the clocked ALE input. This high input will produce the necessary low $\overline{\text{IRW}}$ or $\overline{\text{IRD}}$ output at Pin 6 or 8 of gate 10J which is then transfered to the 7201 at Pins 22 and 21.

The clock input for the 7201 is developed by the CLK5 signal which is produced by flip-flop 2L. (Refer to sheet 3 of 100471.) The output of the CLK5 signal from flip-flop 2L is applied to counter 12E, producing a divide by two clock which is then applied to the 7201 as the input clock. The divide by two clock is also applied to flip-flop 10E which again divides the clock by two, and applies it's output to the clock 0 and 1 inputs of the Interval Timer 11F (8253).This input is used to develop the real time clock output at Pin 17.

The Reset input at Pin 2 of the 7201 (active low) is used to initialize the 7201 to the following conditions: receivers and transmitters disabled,TXDA and TXDB set high,outputs $\overline{DTRA}$,$\overline{DTRB}$,$\overline{RTSA}$ and $\overline{RTSB}$ set high, and all interrupts disabled. After a reset, all control registers must be rewritten before restarting operation.

Pins 12 thru 19 are the Data Bus lines which are connected to the system data bus. Data or status from the 7201 is output on these lines when $\overline{CS}$ and $\overline{RD}$ are high, and data or commands are latched into the 7201 on the rising edge of $\overline{WR}$ when $\overline{CS}$ is high.

$\overline{RXCA}$ (Pin 35) is the receiver clock input which is used to clock in the serial data at Pin 34 (RXDA). The $\overline{RXCA}$ input is dependent upon the Data Selector 15F. Data Selector 15F is enabled by the INT/EXT A and INT/EXT B signals from 6522 at location 12L. (refer to sheet 5 of 100471, Pins 2 and 3.)

DATA TRANSFER (INPUT) PORT A & B

For transfer of data (input) on Port A,Pins 3,5,8 and 17 are used. The input clock signal is applied from Pin 17, through 14D, to Pins 3 and 5 of Data Selector 15F. Timer 11F (8253) produces an output at Pin 10 which is applied to Pins 6 and 4 of Data Selector 15F. This combined with the INT/EXT A and INT/EXT B inputs from the 6522 will produce a output at Pin 7 (1Y).

With the INT/EXT A signal low, the output at Pin 7 (1Y) will follow the IC0 input.(Which is a internal clock from the 8253.) With the INT/EXT A high, the output at Pin 7 will follow the IC3 input. (Which is a external clock from the serial port.) This provides the proper input clock for transfer of data to the 7201 over the RXDA line.

Pin 6 and 39 of the Serial Port Controller Chip is used for the CTS (Clear to Send) signal. The Clear to Send signal is used to inform the 7201 that the peripheral(printer) is ready to receive data from the 7201. Pin 5 and 3 of the Serial Port are used for the $\overline{DCD}$ (Data Carrier Detect) signal. The $\overline{DCD}$ signal is used to indicate valid serial data on the RXDA line. Both the $\overline{DCD}$ and the CTS signals are active low. Both Serial Ports A and B work in the same manner.

DATA TRANSFER (OUTPUT) PORT A & B

Data transfer out of the 7201 and the system is accomplished over Pins 8 and 37 (TXD) of the 7201. This information is sent to Pin 2 of driver chips 15D and 15E for both the A and B ports respectively. Information can only be transmitted after the receipt of the $\overline{CTS}$ signal from the peripheral device. With the receipt of the $\overline{CTS}$ signal data is transmitted basically in the same manner as incoming data is clocked in. This is accomplished using the $\overline{TXCA}$ and $\overline{TXCB}$ signals which control the rate in which the data is clocked out of the 7201 to the Ports.

This is accomplished by using a sample of the output data, which is fed back into the system, and through the same type of circuitry as incoming data is sampled. As with the input side of the Port the $\overline{DCD}$ (Data Carrier Detect) signal is used to inform the peripheral device of the output of valid data on the TXDA and TXDB lines.

Pin 28 of the 7201 is used as an interrupt acknowledge signal to the Peripheral Interface Controller. This input to the PIC will inform the 8088 of the type of interrupt that is being generated. The 8088 will determine that the Serial Ports need servicing and will generate the appropriate commands to gather the data that is present on the Ports. The $\overline{INTA}$ signal at Pin 28 of the 7201 is active low.

SERIAL PORTS INTERFACE (J8 & J9) GENERAL SPECIFICATIONS.

1.	Chassis Ground (A & B)	14.	Not Used
2.	TXDA & B	15.	TXCA & B
3.	RXDA & B	16.	Not Used
4.	RTSA & B	17.	RXCA & B
5.	CTSA & B	18.	Not Used
6.	DSRA & B	19.	Not Used
7.	Signal Ground (A & B)	20.	DTRA & B
8.	DCDA & B	21.	Not Used
9.	Not Used	22.	RIA & B
10.	Not Used	23.	Not Used
11.	Not Used	24.	TTXCA & B
12.	Not Used	25.	Not Used
13.	Not Used		

3.4.15 USER PORT

The User Port circuit is comprised of a 50 Pin connector, physically located inside the system mainframe, and a 6522 Versatile Interface Adapter chip. Control and accessing of the User Port is under the direction of the 8088 microproccessor thru the ID0-ID7 bus, the A0-A3 address lines, a read/write (WR) signal and the Chip Select (CS4) signal. Timing for the 6522 is provided by the Phase 2 clock. Initialization and clearing of the device and port is accomplished through the RESET signal.

The RESET signal for the 6522 and the User Port (Refer to sheet 13 of 100471) is supplied from the Reset switch located on the rear panel of the system. This signal (active low) will reset all internal registers to a logic 0. (Except for latches T1,T2, counters, and the shift Registers.) With a low reset input all peripheral interface lines are set to the input state, and the chip interrupt is disabled.

Pins 35 through 38 on the 6522 are inputs of the A0-A3 address lines. These inputs allow the 8088 to select one of 16 internal registers of the 6522. For accessing the A or B register of the 6522, the following inputs are necessary on Pins 35-38.

R0	R1	R2	R3
0	0	0	0

The input of all 0's selects Input or Output register B (Pins 10-17)

R0	R1	R2	R3
0	0	0	1

The input of Pins 36-38 low and 35 high selects Input or Output register A .

R0	R1	R2	R3
0	0	1	0

The input of Pins 35,37 and 38 low, and Pin 36 high selects the data direction B register.

R0	R1	R2	R3
0	0	1	1

The input of Pins 37 and 38 low, and 35 and 36 high selects the data direction A register.

For selection of the 6522 and the User Port the proper inputs from the 8088 must be present on the A5-A8 and A15-A19 address lines. The proper addresses will provide the correct Chip Enable (CS4) signal to the 6522 at Pin 23.

USER PORT ENABLE

The $\overline{CS}$ signal, which is active low, enables the user port for read/write operations.The Chip Select input is controlled by $\overline{CS4}$ from the I/O state circuits. The $\overline{CS4}$ signal will be low when the 8088 addresses memory address space E8080 through E808F.

When IO/$\overline{M}$ is low (Refer to sheet 4 of 100471) and A19,A18 and A17 are high, Y7 on 9F will go low. This low enables 9H (Pin 1). When A16 is low and A15 is high, a low output is developed on Pin 5 of 9H (Y1 output). This low output (E8000) enables decoder chip 10H at Pin 4 (G2A input). The low output at Pin 5 (Y1) of 9H also forces a high output at Pin 3 of gate 12D. The high output of gate 12D will set flip-flop 9E at the trailing edge of the ALE signal which comes in at Pin 1.

The next Phase 2 clock pulse (which is developed by the CLK5 and devices 10E and 10D (PIN 2) will cause the second flip-flop 9E at Pin 9 to set. The set output of 9E is routed as an enable (high) for CSEN. The A8 bit (low) will enable 10H at the G2B input allowing the A7,A6 and A5 address bits to be decoded at 10H.When A7 is high and A6 and A5 are low, the Y4 output (Pin 11) of 10H will go low, generating the chip select (CS4) for the User Port.

Listed below are the input requirements for the selection of the $\overline{CS4}$ enable.

A19	A18	A17	A16	A15	......	A8	A7	A6	A5
1	1	1	0	1		0	1	0	0

The Phase 2 clock input (Pin 25) is the system clock, and is used to trigger all data transfers between the 8088 and the 6522.

The direction of the data transfers between the system and the 6522 is controlled by the R/W signal (Pin 22). If R/W is low, data will be transferred out of the 8088 and into the 6522 for the User Port. If R/W is high, and the chip is selected,(CS4), data will be transferred out of the 6522 and onto the ID0-ID7 bus.

The eight bi-directional bus lines are used for transfer of data between the 8088 and the 6522. During read cycles, the contents of the registers are placed on the bus lines and transferred to the 8088. During a write cycle, the lines are input lines and information is transferred from the 8088 to the proper register within the 6522.

Pins 2-9 and 10-17 serve as the output and input Pins of the 6522 to the User Port. Pins 39,40,19 and 18 act as interrupt inputs or as handshake outputs. Each line controls an internal interrupt flag with a corresponding interrupt bit which is used in conjunction with Pin 21 (IRQ) to signal the 8088 that a interrupt is being requested by the User Port. The IRQ signal is directed to the Processor Interrupt Controller (PIC) for interrupt priority. The IRQ signal is hard "wire-ored" with the other 6522's used in the system.

PIN CONFIGURATION--USER PORT--J5

Pin 1.	-12 volts	Pin 18.	PA1	Pin 35.	Ground
Pin 2.	-12 volts	Pin 19.	Ground	Pin 36.	PB2
Pin 3.	Not Used	Pin 20.	PA2	Pin 37.	Ground
Pin 4.	Not Used	Pin 21.	Ground	Pin 38.	PB3
Pin 5.	+12 volts	Pin 22.	PA3	Pin 39.	Ground
Pin 6.	+12 volts	Pin 23.	Ground	Pin 40.	PB4
Pin 7.	+5 volts	Pin 24.	PA4	Pin 41.	Ground
Pin 8.	+5 volts	Pin 25.	Ground	Pin 42.	PB5
Pin 9.	Not used	Pin 26.	PA5	Pin 43.	Ground
Pin 10.	Lite Pen(CRT)	Pin 27.	Ground	Pin 44.	PB6
Pin 11.	Ground	Pin 28.	PA6	Pin 45.	Ground
Pin 12.	CA1	Pin 29.	Ground	Pin 46.	PB7
Pin 13.	Ground	Pin 30.	PA7	Pin 47.	Ground
Pin 14.	CA2	Pin 31.	Ground	Pin 48.	CB1
Pin 15.	Ground	Pin 32.	PB0	Pin 49.	Ground
Pin 16.	PA0	Pin 33.	Ground	Pin 50.	CB2
Pin 17.	Ground	Pin 34.	PB1		

3.4.16 CODEC CODER/DECODER

The Victor 9000 digitizes voice through the use of a codec. The codec (HV 55516) uses the CVSD (CONTINUOUSLY VARIABLE SLOPE DELTA MODULATION) method for digitizing analog signals and for converting digital information into audio signals.

CVSD is a simple way to digitize analog signals. The analog signal is input to the CVSD device. The signal is then applied to a comparator and an integrator. The output of the integrator is applied as the second input to the comparator to form a feedback loop. The output of the comparator is the sign difference between the audio input and the integrator output. The sign bit is also used to control the gain of the integrator by varing the direction of the ramp of the integrator.

The codec and its associated elements can be broken down into four basic sections:

1. THE CODEC
2. DATA SERIALIZATION SECTION
3. VOLUME CONTROL SECTION
4. AMPLIFICATION AND ACTIVE FILTERING SECTION

THE CODEC

The codec is a CVSD device (HV 55516). It can be operated in two basic modes, record and playback. In the record mode, audio data is fed into the codec and digitized into a synchronous serial bit stream. In the playback mode, a synchronous serial bit stream is clocked into the codec. The signal is converted into an analog signal by the CVSD method. The analog signal is then actively filtered and applied to the volume control section. Once the volume level has been established the signal is fed through a four watt (MAX) audio amplifier section and applied to the system speaker that is located in the system chassis.

RECORD MODE

(NOT USED AT THIS TIME)

PLAYBACK MODE

Digitally encoded audio information is sent across the ID0-ID7 data bus to the 6852 (SYNCHRONOUS SERIAL DATA ADAPTER) at location 11B. The 6852 is reset by the reset signal pin 9 going low. The reset signal is generated on power on or whenever the system reset switch is activated. The 6852 uses an interrupt to gain access to the microprocessor . The interrupt is generated from the 6852 from pin 7 and sent to the 6522 at location 15L for interrupt processing.

The RS signal pin 11 is used to determine whether the incoming data will be read into data registers or status registers. When RS is low the status registers are selected,when RS is high data registers are selected in the 6852 SSDA. When $\overline{CS}$ (PIN 10),$\overline{WR}$ (PIN 13) are low and E (1 MHZ CLOCK) (PIN 14) is high, the parallel data is gated into the 6852 SSDA at location 11B.

The 6852 SSDA is enabled when address E8060 is placed on the address bus. The $\overline{CS}$ (PIN 10) is controlled by the $\overline{CS3}$ signal. The $\overline{CS3}$ signal is generated by decoder chip 10H (Y3 output). Decoder chip 10H is enabled when the G1 input pin 6 is high and the G2A and G2B inputs are low. The G1 input is controlled by the CSEN signal from flip flop 9E. The G2A signal is controlled by decoder 9H. When A15 is high and A16 is low,address E8000 will be selected. The E8000 line from decoder 9H activates the G2A input. The G2B input is controlled by address bit A8. When A8 is low, the G2B input is activated.

The 6852 serializes the data and gates the information to the 55516 CODEC (DIG IN PIN 12). The 6852 issues the DTR signal (PIN 5) when it has serial data to transmit. The signal is gated through inverter 15B, setting DTR low causing the codec to go into a decoding mode by setting the status of ENC/DEC (PIN 10) high. The information is gated synchronously with the codec clock signal.

BUTTERWORTH FILTER SECTION

17C, PIN 3

17C, PIN 7
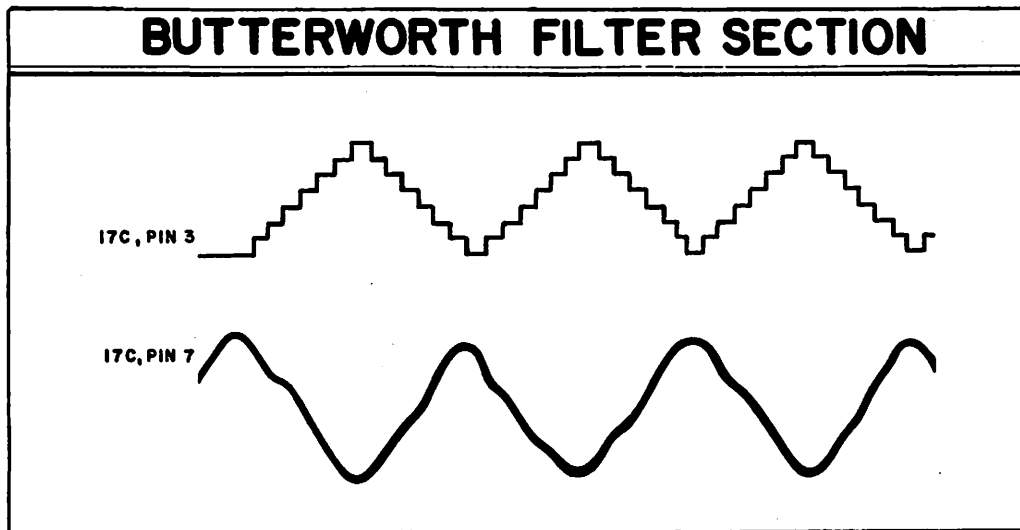
Figure 29

The codec clock signal is generated by the 6522 VERSATILE INTERFACE ADAPTER (VIA) at location 14L (PB7 PIN 17). The codec clk is applied to pin 13 of inverter 15B. The codec clk signal is output from pin 12 of inverter 15B and applied to the RXCLK (PIN 3),TXCLK (PIN 4) on the 6852 and the codec clk input (PIN 9) on the codec. The frequency of the codec is 16 KHZ. The codec through the use of the CVSD method, decodes the digital information into an analog audio signal.

The audio signal exits the codec at pin 3 AUDIO OUT . The signal is passively filtered by capacitor C41. The audio signal is then applied to the 3KHZ cutoff low pass active butterworth filter which consists of half a LM324 (17C) and its associated circuitry. The audio signal is applied to the operational amplifier 17C (PINS 2 AND 3). The signal is then applied to op amp 17C (PINS 5 AND 6).

These two op amps form the active filter section. After the filter section,the audio signal is applied to a 4066 bilateral switch 17B. The 4066 is used to form an electronic volume switch. The 4066 is controlled by the 6522 VIA at location 15L. The codec vol signal is issued from the 6522 at CB2 (PIN 19). The codec vol signal is applied to inverter 14N (PIN 13). The inverted codec vol signal exits 14N (PIN 12) and is applied to inverter 15B (PIN 9) and also (PIN 3).

The codec vol signal and the inverted codec vol signal
are used to control the duty cycle of the audio signal. By
controlling the duty cycle of the audio signal ,the volume
control section can generate seven (7) different audio
levels. The 4066 is divided into two functional sections in
the volume control section. The first section inputs the
audio signal through pins 1 and 4 on the 4066 at location
17B. The second section inputs the dc bias voltage through
pins 8 and 11 of the 4066 at location 17B.

When full volume is desired the codec vol signal is
kept at a constant high, turning on the first section of
the 4066 only,thus applying the full (100 PERCENT) duty
cycle of the audio signal to the final amplification stage.
By toggling the codec vol signal the duty cycle of the
audio signal is decreased thus decreasing the volume level.
The cycle time for the full audio signal is approx. 48 us.
The different volume levels are separated by about 6 ms
between levels (i.e. level 6 codec vol high 42 ms,low 6
ms).

The audio signal is then applied through resistor R53
and filter capacitor C32 to the final amplification stage
which consists of a LM383 operational amplifier and its
associated circuitry. The audio signal is then amplified
(FOUR WATT MAX) and applied to the system speaker through
connector J16 (PINS 1 AND 2).

3.4.17 EXPANSION BUS

The expansion bus for the Victor 9000 is composed of 4
female 50 pin edge connectors. These connectors allow
for the addition of memory expansion boards, interface
boards, or special purpose control boards.

The table below indicates the pin configuration for the
expansion slots.

PIN	SIGNAL	DEFINITION
1	A18	Address bit 18
2	A16	Address bit 16
3	A14	Address bit 14
4	A12	Address bit 12
5	A10	Address bit 10
6	A8	Address bit 8
7	SSO	Status
8	DEN	Data enable
9	ALE	Address latch enable
10	IO/M	I/O or memory
11	RD	Read
12	DT/R	Data transmit/Receive
13	RESET	Reset
14	WR	Write
15	NMI	Non-Maskable interrupt
16	IRQ	Interrupt request
17	HOLD	Hold
18	HLDA	Hold acknowledge
19	CSEN	Chip select enable
20	PHASE 2	I/O clock
21	XACK	External bus acknowledge
22	BD6	Buffered data bus, bit 6
23	BD4	Buffered data bus, bit 4
24	BD2	Buffered data bus, bit 2
25	BD0	Buffered data bus, bit 0
26	BD1	Buffered data bus, bit 1
27	BD3	Buffered data bus, bit 3
28	BD5	Buffered data bus, bit 5
29	BD7	Buffered data bus, bit 7
30	EXTIO	External I/O
31	GRD	Ground
32	-12V	-12V DC
33	DLATCH	Data latch
34	+12V	+12V DC

PIN	SIGNAL	DEFINITION
35	GRD	Ground
36	+5V	+5V DC
37	+5V	+5V DC
38	CLK5	200 Nanosecond clock
39	GRD	Ground
40	CLK15B	67 Nanosecond clock
41	READY	Ready
42	IR5	Interrupt request bit
43	IR4	Interrupt request bit
44	GRD	Ground
45	A9	Address bit 9
46	A11	Address bit 11
47	A13	Address bit 13
48	A15	Address bit 15
49	A17	Address bit 17
50	A19	Address 19

Refer to the Intel 8088 Reference Manual for a full description of the 8088 microprocessor signals.

A8-A19 are 8088 memory address bits latchable at the trailing edge of ALE.

BD0-BD7 is the Buffered data bus for the transfer of the data to/from the expansion bus.

RD & WR are the read or write control signals generated by the 8088 during a read or write cycle.

IO/M determines whether a data transfer is to/from memory versus to/from an I/O device.

IR4, IR5 are external interrupt request bits input to the 8259 programmable interrupt controller.

IRQ is the parallel interrupt request line for perpherial devices.

Hold generates a hold request to the processor.

HLDA is the processor response to a hold request.

DEN controls the transfers of data from the Buffered data bus (BD0-BD7) to the multiplexed address/data bus (AD0-AD7).

3.5 KEYBOARD MODULE

The keyboard (KB) module for the 9000 is located on schematic 100379. The KB switch matrix is arranged in 13 columns X 8 rows, for a total of 104 switch positions. The switches used are the capacitive-type switches which produce a change in capacitive coupling between the contacts when depressed. The KB utilizes an Intel 8021 microprocessor chip (Z3) for the generation of KB strobes and for data transfers to the logic board.

Z3 produces 5 KB scan outputs, 4 on P10 - P13 (pins 18-21) and 1 on P22 (pin 1). The P10 - P13 outputs are routed to Z2 on the A-D input lines (pins 6-9). Z2 will generate 12 scan output pulses on the 0-B outputs (pins 1-4 & 12-19) from the 4 inputs. The column lines in the matrix will be scanned sequentially from 0 to B. The P22 output is routed through inverter Z4 to produce scan line number 13.
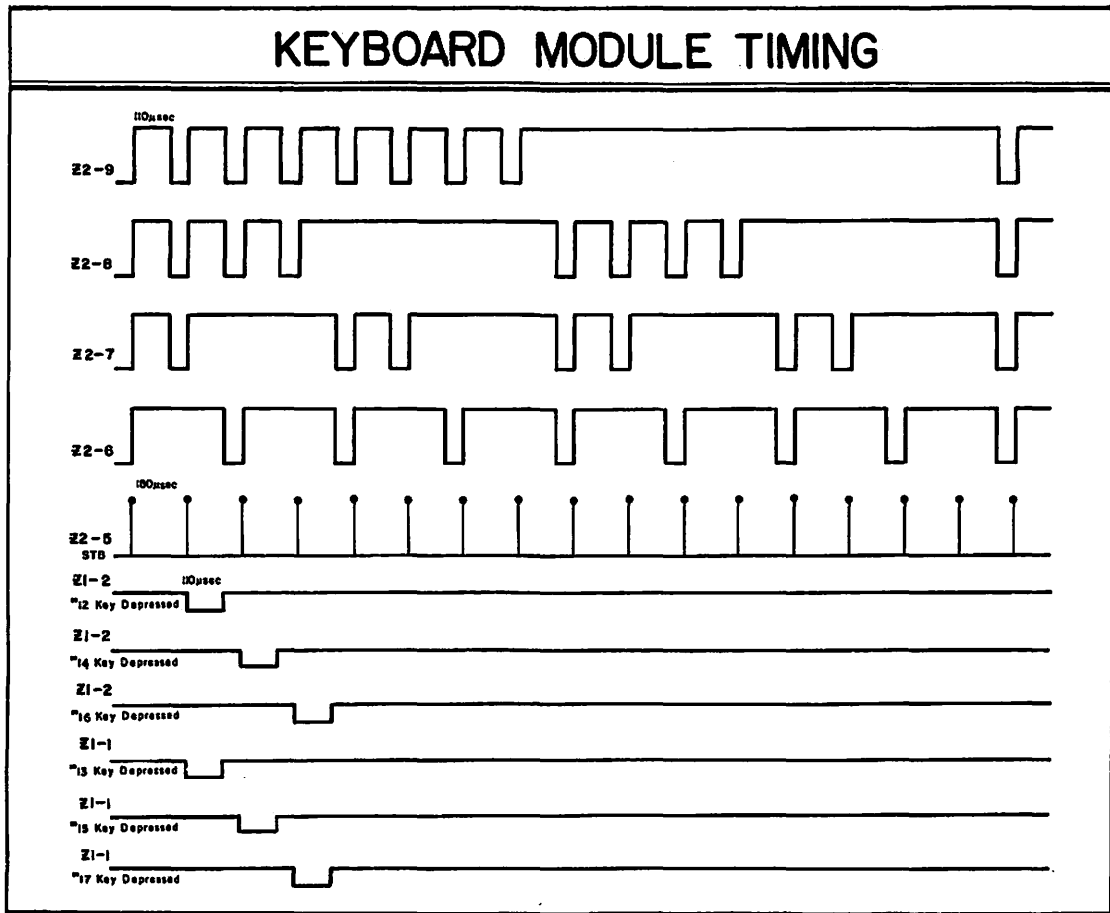
Figure 30

When a switch is depressed the column line will be connected to a row line. If switch number 44 is depressed, column line 5 (Z2 pin 17) will be connected to row line number 3 (Z1 pin 4). The scan pulse from column 5 will be input to Z1. Z1 will produce a 4-bit output on pins 11 - 14 to tell Z3 which switch position in the matrix was depressed. The code from Z1 will be an address pointer into the ROM matrix of Z3 to determine the logical number for the key. Z3 will output the logical number for the key depression to the logic board. The logical number will be transferred to the logic board serially on the KBDATA line. The 8088 on the logic board will decode the meaning of the key number as defined by software.

For a detailed data transfer sequence to the logic board, refer to section KEYBOARD INTERFACE.
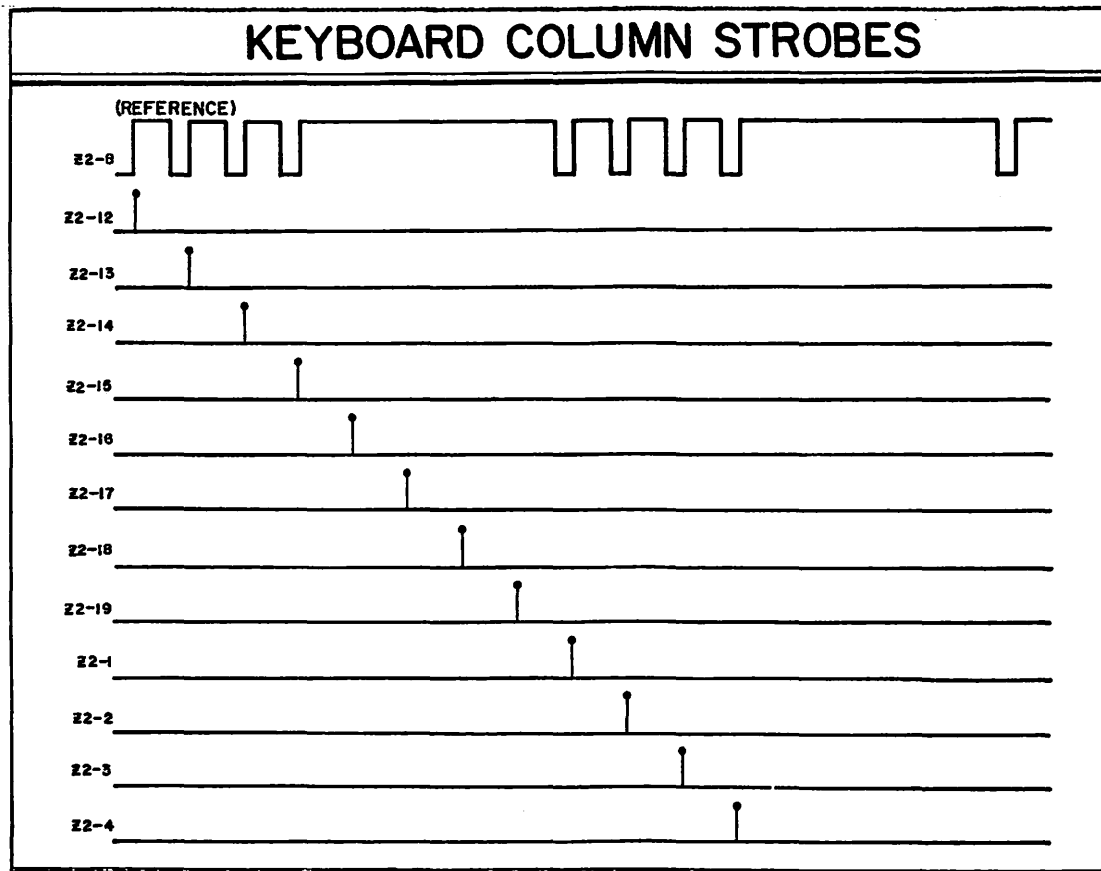
Figure 31

3.6 128K MEMORY EXPANSION BOARD

System memory can be expanded with the addition of either 128K or 384K memory boards. The Victor 9000 can access a maximum of 896K bytes of memory.

The dip switches on the 128K board allow for the addition of multiple memory boards in a system. Each switch from 1-6 allows for the selection of a 128K block of memory. The memory board is contained on 4 sheets of schematic 100901.

The memory board is accessed by address bits A0-A19. The A8-A19 address bits enter the board directly over the expansion bus while the A0-A7 bits are latched onto the BD0-BD7 bus then latched into the memory board as A0-A7.

When ALE is high (sheet 2 of 100471) from the 8088 microprocessor it is inverted at "Nor" gate 8J. The resultant low enables transceiver chip 9K. The HLDA being low configures the chip to pass the 8 address bits from the AD0-AD7 bus to the BD0-BD7 bus.

The address bits on the BD0-BD7 bus are latched into 1E on sheet 4 of schematic 100901 on the trailing edge of ALE. At this time the address bus, A0-A19, will have valid address data on it.

While ALE is high flip-flop 4E on sheet 3 will set on the next CLK5. The set side of PRQ is routed to the set side of flip-flop counter chip 4P. At the rising edge of the next CLK15 the P1 flip flop will set. The set output provides the D input to the next flip-flop P2. The next CLK15 will set flip-flop P2. The set output of P2 will cause P3 to set on the next CLK15. When P3 sets the high output is "Nor'ed" at 2B resulting in a low $\overline{RAS}$ being generated. At this time the MUX flip-flop will still be reset waiting for the next CLK5. On the rising edge of CLK5 MUX will be set.

At the next CLK15 the P3 high will set the P4 flip-flop. The high out of P4 will be "Nor'ed" at 2B pin 10 generating $\overline{CAS}$ low. The low $\overline{CAS}$ will enable the $\overline{CAS}$ decoder on sheet 4. P1 will be reset on this CLK15 by the PRQ flip-flop being reset.

128K MEMORY BOARD

CLK15

CLK5   T1   T2   T3   T4

ALE

PRQ

MUX

P1

P2

P3

P4

P5

$\overline{RAS}$

$\overline{CAS}$

RAD

4C

WINDOW
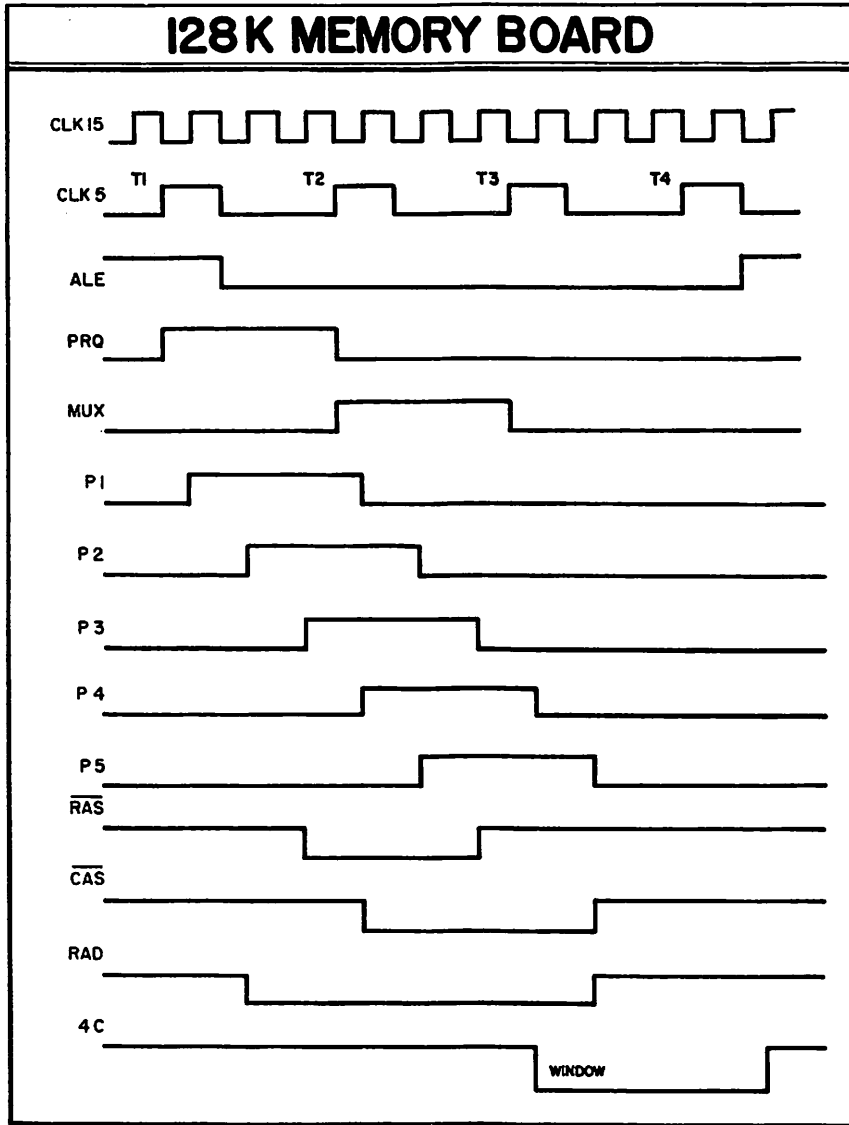
Figure 32

During a write operation the $\overline{WR}$ control signal will go low. This low is inverted at 1B pin 1. The resultant high is "Nanded" with the MUX high at 4C and the low output generates the $\overline{WE}$ for the memory chips (sheet 2). When $\overline{WR}$ is low $\overline{RD}$ is high configuring the transceiver at 1F to transfer the data byte from the BD0-BD7 bus to the D0-D7 bus. The transceiver will be enabled when $\overline{EN}$ goes low on pin 19. $\overline{EN}$ will go low when decoder 3B is enabled by a low on IO/$\overline{M}$ and the input address configuration A19, A18, A17 forces a low out of the decoder (Y0-Y7) which is coincident with the switch closures of dip switch 4B.

The dip switch module at 4B selects the 128K block of memory in which the memory board will reside. The following table defines the memory blocks to switch settings.

MEMORY SPACE	SWITCH NUMBER
0-128K	
128K-256K	1
256K-384K	2
384K-512K	3
512K-640K	4
640K-768K	5
768K-896K	6

Dip switches 7 and 8 are used to establish the time base for the memory refresh cycle. Dip switch 7 is set to off and dip switch 8 is set to on.

The low $\overline{EN}$ is also routed to the data selector at 3C. This enable is selected on the 4Y output and enables the $\overline{RAS}$ and $\overline{CAS}$ selector at 3F.

When $\overline{EN}$ is low, $\overline{RAS}$ is low, and A16 is low, the $\overline{RAS0}$ low is generated to provide the row address strobe for the lower 64K of the board. When $\overline{EN}$ is low, $\overline{RAS}$ is low, and A16 is high, $\overline{RAS1}$ will go low generating the Row Address Strobe for the upper 64K of the board. $\overline{CAS0}$ and $\overline{CAS1}$ are generated the same as $\overline{RAS}$ except the $\overline{CAS}$ control signal is low.

When $\overline{RAS}$ is low, MUX will be low and RAD will be low selecting the 0 input for the output of selectors 2D, 2C, 1C, and 1D. This will place A0-A7 on the AB0-AB7 bus. When $\overline{CAS}$ is low, MUX will be high and RAD will be low selecting the 1 input for output. At this time A8-A15 will be on the AB0-AB7 bus. When RAD goes high (during a refresh cycle) the RFA0-RFA6 and RFA10 will be on the AB0-AB7 bus.

MEMORY REFRESH CYCLES

When ALE goes high it will be inverted at 1B pin 8 and the low will force a high out of "Nand" gate 4C. This high will cause the flip-flop at 4E to set on the next CLK5. The reset side will go low allowing counter 3E to begin counting up. When the count reaches 8, QD will go high enabling 4C to go low at the end of a memory access cycle. QD will remain high for 7 CLK5 cycles.

When ALE is low, PRQ is reset, MUX is reset, and the count is 8 or above (QD high) 4C will go low. The low output will cause 4E to be reset on the next CLK5 generating RRGL. On the leading edge of the low to high transition $\overline{RAS}$ will go low out of 2B pin 1 and the refresh address generator (3D & 3E) will be incremented. The high level on the Q output of the 4E flip flop will clear the counter at 3E and hold it in a zero state until the flip-flop is again set on the next CLK5. The end result will be a RAS only refresh cycle being performed.

3.7 384K MEMORY EXPANSION BOARD

The 384K memory board allows system memory to be expanded to either 512K or 896K bytes.

The memory board is structured in 3 blocks of 128K bytes of dynamic RAM (Random Access Memory). The circuit design for each block is identical and is also identical to the 128K memory expansion board.

The 384K memory board circuits are contained on 6 sheets of schematic 101071.

The addressing for the memory board enters via the expansion bus on BD0-BD7 and A8-A19. The address bits on BD0-BD7 are latched into 2M on sheet 3 on the trailing edge of ALE. The address bits A0-A18 are inputs to address selector chips 2T, 2R, 2P, and 2S. The output of the address selectors, AB0-AB7 provide address selection for the 4164 Dynamic Rams. The A19 address bit is used only in the generation of the enable ($\overline{EN}$) for the memory board.

The $\overline{EN}$ signal, generated on sheet 2, is dependent upon the position of jumper E4/E5 with E6, E1,E3 with E2, and the output of decoder chip 1B. The table below defines the jumper positions for memory selection.

JUMPER	MEMORY SPACE
E2-E3 & E4-E6	128K-512K
E1-E2 & E5-E6	512K-896K

Any low input to the "And" gates 1D will cause the output to go low, enabling the board. When A17 is high, A18 is low, and A19 is low the Y1 output will go low selecting the memory if it is jumpered E4-E6. If the board is jumpered E5-E6 and A19 is high, A18 is low, and A17 is high, the Y5 output will go low selecting the memory board for upper memory. When A19, A18, and A17 are all high the Y7 output is selected and neither memory board will be selected for access. This memory space is reserved for memory-mapped I/O operations.

The A17 and A18 address bits are buffered by "Exclusive Or" gates at 2B. When the address bit is high, its buffered address bit will also be high. The BA17 and BA18 bits are inputs to selector 1P for the $\overline{RAS}$ and $\overline{CAS}$ signals.

The data byte to be written is passed from the BD0-BD7 bus to the D0-D7 memory data bus by transceiver 2L. When $\overline{EN}$ is low the transceiver is enabled and the state of the $\overline{RD}$ control signal determines the direction of data transfer. When $\overline{RD}$ is high, data is transferred from the BD0-BD7 bus to the D0-D7 bus. When $\overline{RD}$ goes low, indicating a read operation, data is passed from the D0-D7 bus onto the BD0-BD7 bus.

A memory access cycle begins when ALE goes high. This high will steer the PRQ flip-flop set on the next CLK5 signal. The high out of PRQ steers the counter flip-flops at 1E to begin their count sequence. The next CLK15 will set the P1 flip-flop which will set the P2 flip-flop on the following CLK15. When P2 goes high it will force RAD low at 1F. The low RAD signal will steer the address selectors to select address bits rather than refresh bits. The next CLK15 will set the P3 flip-flop. P3 will generate $\overline{RAS}$ low at 1F. This low $\overline{RAS}$ signal enables the $\overline{RAS}$ decoder at 2J on sheet 3.

When any $\overline{RAS0}$-$\overline{RAS5}$ signal goes low the AB0-AB7 address bits will be strobed into the row address latches in the selected ram chips. At this time MUX will be low placing the A0-A7 address bits on the AB0-AB7 bus. On the next CLK5 MUX will be set. The next CLK15 will set the P4 flip-flop which will generate the $\overline{CAS}$ signal. When $\overline{CAS}$ is low the CAS decoder at 1K will be enabled. When any $\overline{CAS0}$-$\overline{CAS5}$ signal goes low Column Address bits will be strobed into the latches of the selected ram chips. At this time MUX will be high, placing the A8-A15 address bits on the AB0-AB7 bus. When P5 is set on the next $\overline{CLK15}$ $\overline{CAS}$ will be held low forcing RAD to remain low.

When the $\overline{WR}$ signal from the 8088 goes low it will be inverted at 2F, "Anded" with MUX at 1D and the resultant high output will be inverted by 2F generating the write enable for the ram chips in three signals; $\overline{WE0}$, $\overline{WE1}$, and $\overline{WE2}$. Each $\overline{WE}$ is for a 128K block of memory.

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals are used as enables for the decoders on sheet 3, 2J and 1K. The inputs to the decoders, from data selector 1P, determine which $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ will be generated. The following table defines the address bit configuration used to generate each of the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals to the ram chips.

ADDRESS BIT			RAS OR CAS
A18	A17	A16	
0	1	0	0
0	1	1	1
1	0	0	2
1	0	1	3
1	1	0	4
1	1	1	5
RFA9	RFA8	RFA7	RAS
0	1	0	0
0	1	1	1
1	0	0	2
1	0	1	3
1	1	0	4
1	1	1	5

The G2A enable for the RAS decoder is tied to ground to keep it enabled at all times. The G2A enable for decoder 1K is tied to data selector 1P. When RAD is high at pin 1 of 1P the B inputs are selected for output. The high RAD out of 4B on 1P will disable the CAS decoder during a refresh cycle. When RAD is low, the $\overline{\text{EN}}$ low is applied at the 4B output, enabling the $\overline{\text{CAS}}$ decoder.

MEMORY REFRESH

The dynamic ram chips are refreshed at a 2msec rate to prevent loss of data. The refresh cycle begins at 2E when ALE is low, PRQ is reset, MUX is reset, and counter chip 1S has reached a count of 4 or above. The all ones input to "Nand" gate 2E will force a low out and on the next CLK5 flip-flop 2D will be reset. The rising edge of the reset output of 2D will force "Nor" gate 1F to go low, generating $\overline{\text{RAS}}$. When $\overline{\text{RAS}}$ goes low decoder 2J on sheet 3 will be enabled. The rising edge of RRGL will also increment counters 1R and 1S on sheet 3. These counters provide the memory refresh address during a refresh cycle.

At the same time both inputs to "Nor" gate 1F pin 13 will be low. This will generate a RAD high selecting the RFA address bits to be placed on the AB0-AB7 address bus. The RFA7, RFA8, and RFA9 bits will be placed on the input to decoder 2J by the data selector 1P. These signals will determine which $\overline{RAS}$ will be strobed. The low going $\overline{RAS}$ signal will perform a Row Address Refresh on the selected memory chip.

3.8 DISK DRIVE ASSEMBLY

The disk drive assembly comprises the electro-mechanical segment of the disk drive subsystem. It is used in conjunction with the disk drive controller board, which provides the electronic control functions.

The disk drive assembly is composed of the following functional subassemblies:

1. Spindle Drive System

2. Head Positioning system

3. Read/Write/Erase system

4. Track Zero Sensor

5. Activity LED, Write Protect Sensor, Door Open Switch

The Spindle Drive System is composed of a DC motor, belt drive, and spindle assembly. When a diskette is inserted into the drive the cone/clamp system centers the media on the spindle and clamps it to the spindle hub. The motor controls the speed of the media under the head. The Victor 9000 uses a varying speed technique to increase storage capacity on the diskette, thereby making the strobe marks on the spindle wheel unusable. The speed is controlled by a microprocessor on the controller that monitors the feedback from the tachometer connected to the motor.

The diskette is accurately positioned in the drive unit by plastic guides and by the front latch inhibitor. The in/out location is ensured by the backstop.

The magnetic head is positioned over the desired track by use of a stepper motor/band assembly. The positioner employs a one step rotation to cause a one track linear movement. The stepper positioning system provides no feedback to the electronics during head positioning. The feedback is created by reading the sector header on the diskette to confirm track position.The four phase stepper signals are generated on the controller board. The head is secured to the frame by use of two metal rails. A head pad on the opposite side of the media provides the required amount of media pressure against the head.

The Read/Write/Erase head is a glass bonded ferrite/ceramic structure that provides the means by which data is stored and retreived from the diskette. It is composed of a read coil, write coil and erase coil. During a write operation, a 0.1650 mm data track is recorded. Then, this track is tunnel erased to 0.1524 mm. The disks have double density capacity with 96 TPI (tracks per inch). During a read operation the read coil senses the flux reversals stored on the media during the write sequence.

The Track Zero sensor provides an electronic signal when the head is physically positioned at track zero. It is composed of an LED light source and a light sensor. When the light beam is broken by the presence of a metal finger attached to the head positioner the system is signalled that the head is at track zero.

The activity LED is illuminated whenever the drive is selected for a read, write, or seek operation. It is generated on the drive controller board.

The Write Protect sensor disables the write electronics whenever a write protected disk is placed in the drive. Each diskette has a notch removed on the left side of the case. When the notch is uncovered the write protect switch is allowed to remain in the open position. When the notch is covered by a silver write protect tab the switch is closed, disabling the write electronics.

The door open switch is physically attached to the door mechanism. When the door is closed the switch contacts are closed.

SCHEMATICS
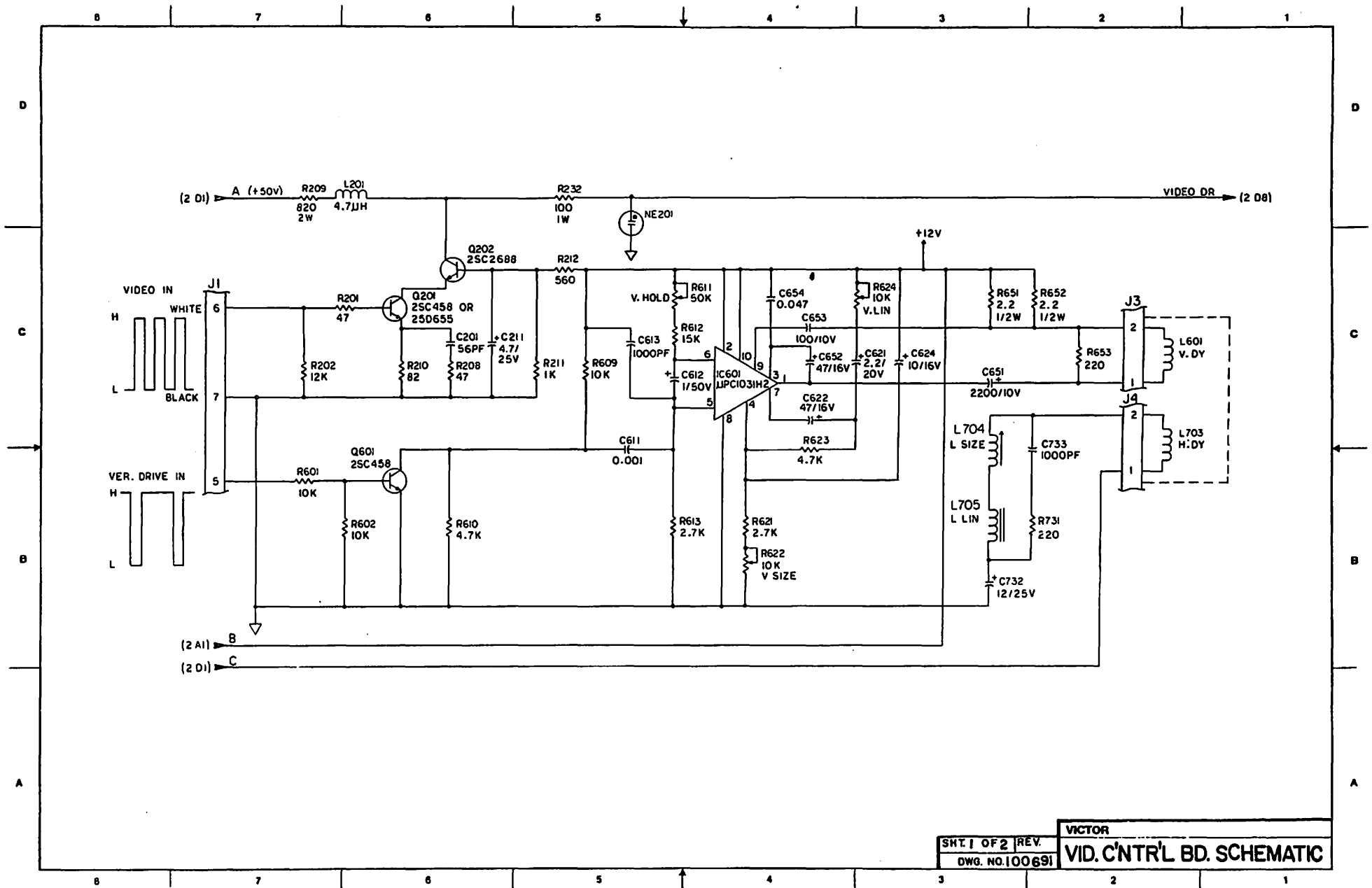
VICTOR

SHT. 1 OF 2 | REV.
DWG. NO. 100691

VID. C'NTR'L BD. SCHEMATIC
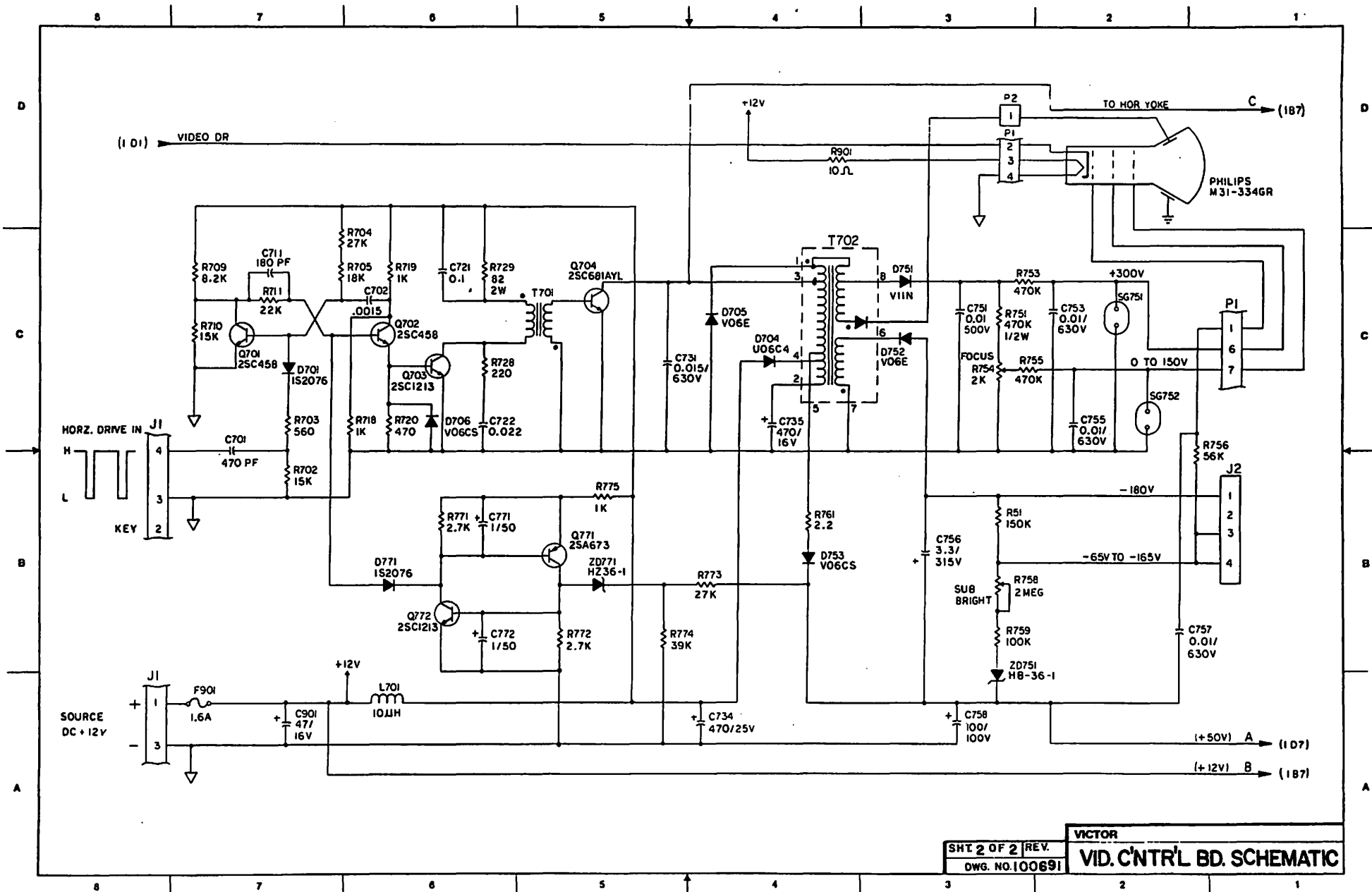
SHT 2 OF 2 | REV.
DWG. NO. 100691

VICTOR
VID. CNTR'L BD. SCHEMATIC

KEYBOARD MODULE

R4
1M

Y1
356 MHZ

+5V
R3
3.3K

Z4
LS14

A B C D   ST8
Z2

B A 9 8 7 6 5 4 3 2 1 0

R1
6.8K

R2
806
1%

T14 RESET

P22

VCC +5V

Z3

P20

P10
P11
P12
P13
P14
P15
P16
P17

+5V
C3
10

RESET

GND

+5V
R5
1.5K

T1

Z4
LS14

R6
100

C7
.0047

J1

4 KBACK

P21
Z4
LS14
Z4
LS14
L1
22 UH
C8
.0047
5 KBRDY

P23
Z4
LS14
Z4
LS14
L2
22 UH
C9
.0047
6 KBDATA

+5V

C1
.033
C2
.033
C4
.033
C6
.033
C10
.033
C5
10

7 +5VDC
1
3
2 GND
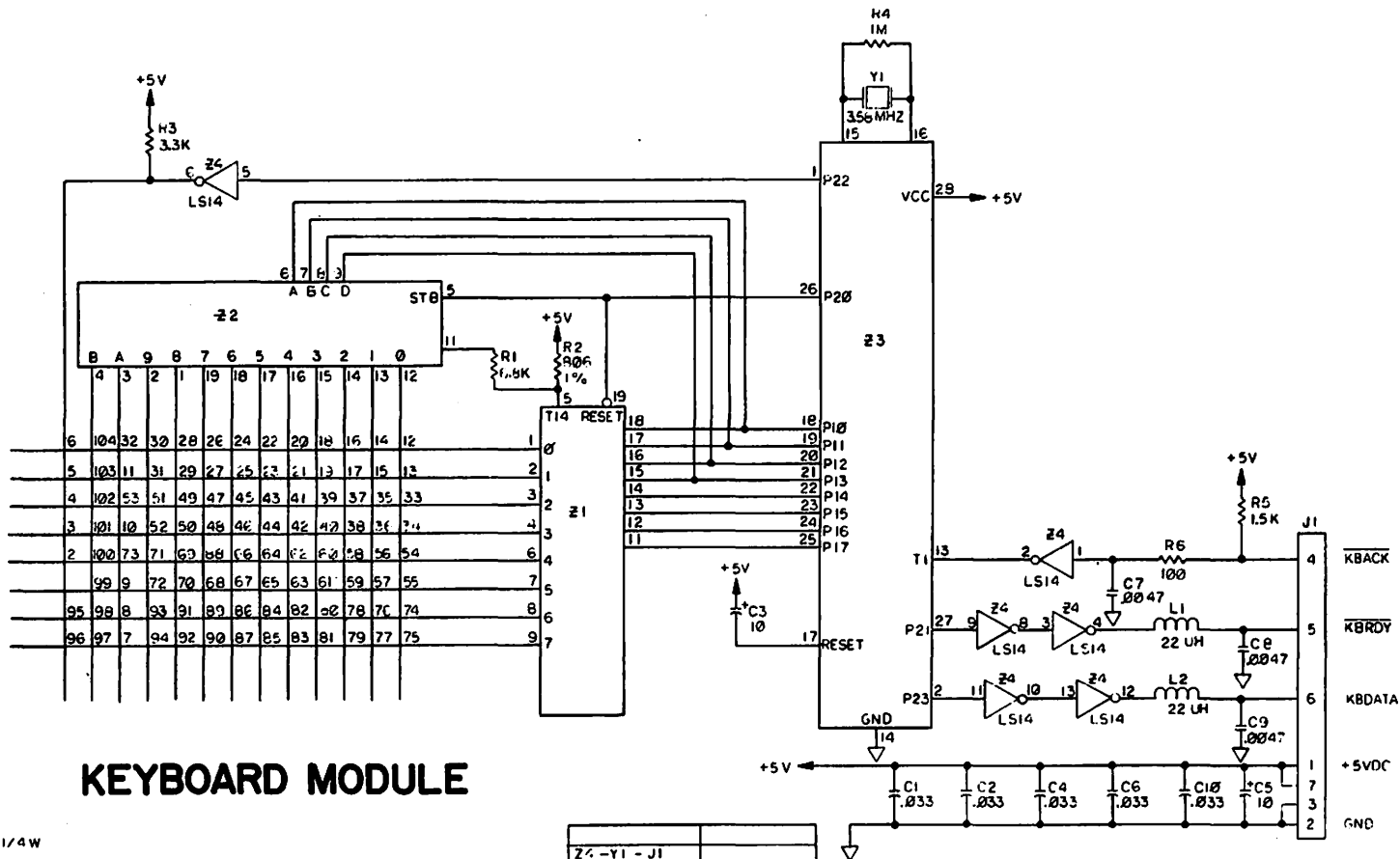
3. ALL RESISTORS ARE ±5%, 1/4 W

2. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS
& MICROHENRIES

1. MADE SCHEMATIC FROM KEY TRONIC CORPORATION,
SPOKANE, WASH. PART NUMBER 35-02307-XXX

NOTE: UNLESS OTHERWISE SPECIFIED

Z4 - Y1 - J1	
R6 - C10 - L2	
LAST USED	NOT USED
REF. DES.	
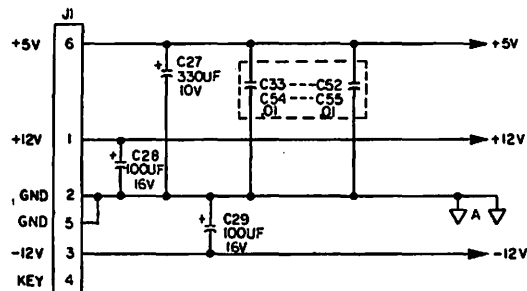
POWER & SPARES

J1

+5V	6
+12V	1
GND	2
GND	5
-12V	3
KEY	4

C27 330UF 10V
C28 100UF 16V
C29 100UF 16V

C33 — C52
C54 — C55
.01 .01

→ +5V
→ +12V
→ -12V

NOTES: UNLESS OTHERWISE SPECIFIED.

1. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS AND MICROHENRIES.
2. ALL RESISTERS ARE ±5%, 1/4W.
3. F.S. IS FACTORY SELECT COMPONENTS.
4. Q1, Q2 ARE MOUNTED ON HEATSINK.
5. ALL INTEGRATED CIRCUITS ARE SN74 SERIES.
6. I.C. PINS ARE GND = 7, +5V = 14 EXCEPT FOR:

TYPE	GND	+5V
74LS123	8	16
74LS133	8	16
74LS139	8	16
74LS157	8	16
74LS165	8	16
74LS190	8	16
74LS191	8	16
74LS373	10	20
2316	12	24
75462	4	8

7. ALL DIODE ARE 1N4148.
8. SEE TABULATION TABLE THIS PAGE.
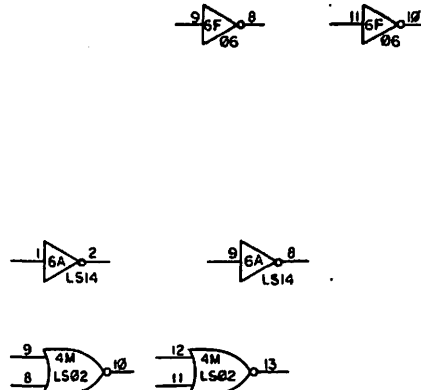
SHEET	DESCRIPTION
1	POWER & SPARES
2	CPU INTERFACE (6522)
3	MOTOR SPEED (8748 & DAC)
4	PLL
5	RD/WR HEAD INTERFACE
6	DRIVE SELECT, LED, DECODE
7	GCR EN/DE-CODER
8	DISK CONNECTORS (REF)
9	STEPPER CONTROL

SPARE GATES

6F 06, 6F 06, 6A LS14, 6A LS14, 4M LS02, 4M LS02

VICTOR
DISK DRIVE SCHEMATIC
SHT. 1 OF 9 REV. C
DWG. NO. 100671

CPU INTERFACE (6522)

VICTOR

DISK DRIVE SCHEMATIC

MOTOR SPEED (8748 & DAC)

VICTOR

DISK DRIVE SCHEMATIC

SHT. 3 OF 9 REV. C

DWG. NO. 100671

PHASE LOCKED LOOP

| SHT. 4 OF 9 | REV. C | VICTOR |
| DWG. NO 100671 | | DISK DRIVE SCHEMATIC |

RD/WR HEAD INTERFACE

DRIVE SELECT, LED,
DECODE

| SHT. 6 OF 9 | REV. C | VICTOR |
| DWG. NO. 100671 | | DISK DRIVE SCHEMATIC |

GCR EN/DE-CODER

VICTOR
DISK DRIVE SCHEMATIC
SHT. 7 OF 9 REV. C
DWG. NO. 100671

DISK CONNECTORS (REF)

STEPPER A (SHT 9)

MOTOR A (8748, DAC, DISCRETE) (SHT 3)

ACTIVITY LED A (SHT 6)

WRITE PROTECT A (SHT 6)

STEPPER B (SHT 9)

MOTOR B (SHT 3)

ACTIVITY LED B (SHT 6)

WRITE PROTECT B (SHT 6)

CPU INTERFACE (6522) (SHT 2)

POWER CONNECTOR (SHT 1)

DRIVE A HEAD Ø (SHT 5)

DRIVE A HEAD I (SHT 5)

DRIVE B HEAD Ø (SHT 5)

DRIVE B HEAD I (SHT 5)

MOTOR START SWITCH A (SHT 6)

DISK A (SHT 2)

MOTOR START SWITCH B (SHT 6)

DISK B (SHT 2)

STEPPER CONTROL

(2B5) ST0A
(2B5) ST0B
(2B5) ST0C
(2B5) ST0D
(2C1) STP0

(2B5) ST1A
(2B5) ST1B
(2B5) ST1C
(2B5) ST1D
(2C1) STP1

4D-2 75462
4D-2 75462
4D-1 75462
4D-1 75462

4E-2 75462
4E-2 75462
4E-1 75462
4E-1 75462

CR11 IN4003   R65 3.3K
CR12 IN4003   R66 3.3K
CR13 IN4003   R67 3.3K
CR14 IN4003   R69 3.3K
CR15 IN4003   R71 3.3K
CR16 IN4003   R72 3.3K
CR17 IN4003   R74 3.3K
CR18 IN4003   R75 3.3K

CR19 IN4003
CR20 IN4003
CR21 IN4003
CR22 IN4003
CR23 IN4003
CR24 IN4003
CR25 IN4003
CR26 IN4003

C58 3.3/15V

3D 2074B
3D 2074B
3D 2074B
3D 2074B
3E 2074B
3E 2074B
3E 2074B
3E 2074B

R68 10Ω,2W
R70 10Ω,2W
R73 10Ω,2W
R76 10Ω,2W

+12V

J2
4 S0A
3 S0B
2 S0C
1 S0D
5 S0CT

J13
4 S1A
3 S1B
2 S1C
1 S1D
5 S1CT

1/2 STEPPER MOTOR
1/2 STEPPER MOTOR
1/2 STEPPER MOTOR
1/2 STEPPER MOTOR

NOTES: UNLESS OTHERWISE SPECIFIED:

1. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS AND MICROHENRIES
2. ALL RESISTORS ARE ± 5%, 1/4 W
3. ALL INTEGRATED CIRCUITS ARE SN74 SERIES.
4. I.C. PINS ARE GND = 7, +5V = 14 EXCEPT FOR:

TYPE	GND	+5V	+12V
74LS112	8	16	—
74LS138	8	16	—
74LS139	8	16	—
74LS151	8	16	—
74LS153	8	16	—
74LS157	8	16	—
74S163	8	16	—
74LS166	8	16	—
74LS257	8	16	—
74LS244	10	20	—
74LS245	10	20	—
74S374	10	20	—
74LS373	10	20	—
74LS374	10	20	4
LM324	11	—	4
4066	7	—	14
2732	12	24	—
75160	10	20	—
75161	10	20	—
6116	12	24	—
4164	8	16	—
8259A	14	28	—
74LS90	10	5	—

5. NOT USED : J15, RESISTORS: R18,30, 31, 39,40,41,42, 44, 45,46,47,48,49,50, 63,68 69,43,66,67, CAPS:1,13, 19,20,21,22,23,24,27,136 28,76,39, E19,20,21,22,13,14,15,16,17,18

6. FOR JUMPER CONFIGURATION FOR USE WITH EITHER PROMS IN LOCATIONS 5H & 7H OR 64K ROM IN LOCATION 7H SEE NOTE IN AREA B1 ON SHEET 2.

POWER & SPARES

SPARE GATES

CPU & BUS CONTROL

NOTE:

FOR 64K ROM
AT 7H
JUMPER: E3-4
        E7-8
        E11-12
CUT: E1-2
        E5-6
        E9-10

FOR EPROM'S
(2732'S)AT 5H&7H
JUMPER: E1-2
        E5-6
        E9-10
CUT: E3-4
        E7-8
        E11-12

MASTER CLOCK

CLK 15   (7B8)
CLK 15A   (5B8)(7D8)(1ØB8)
CLK 15B   (12C8)(7C8)
MPUCLK   (2D8)
CLK5   (12B8)(12C3)(11C8)
CLK5   (7D8)(4B8)
RESET   (5B8)(8C8)(6B8)(12C3)(11B8)(13B8)(14C8)
RESET   (2D8)(12B8)

DECODER CHIP SELECT

KEYBOARD INTERFACE

IEEE CENTRONICS INTERFACE

VICTOR

CPU SCHEMATIC

CONTROL SIGNALS

MEMORY CYCLE

	0	1	2	3	4
MA	0	1	1	1	0
MB	0	0	1	1	1
MC	0	0	0	1	1

CRT CYCLE HIRES

	3	4	5	6	7	8	9	0	1	2
CA	0	1	0	1	0	1	0	1	0	1
CB	0	0	1	1	0	0	1	1	1	1
CC	0	0	0	0	1	1	1	1	1	1
CD	1	1	1	1	1	1	1	0	0	0

CRT CYCLE HIRES

	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8
CA	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
CB	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
CC	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
CD	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
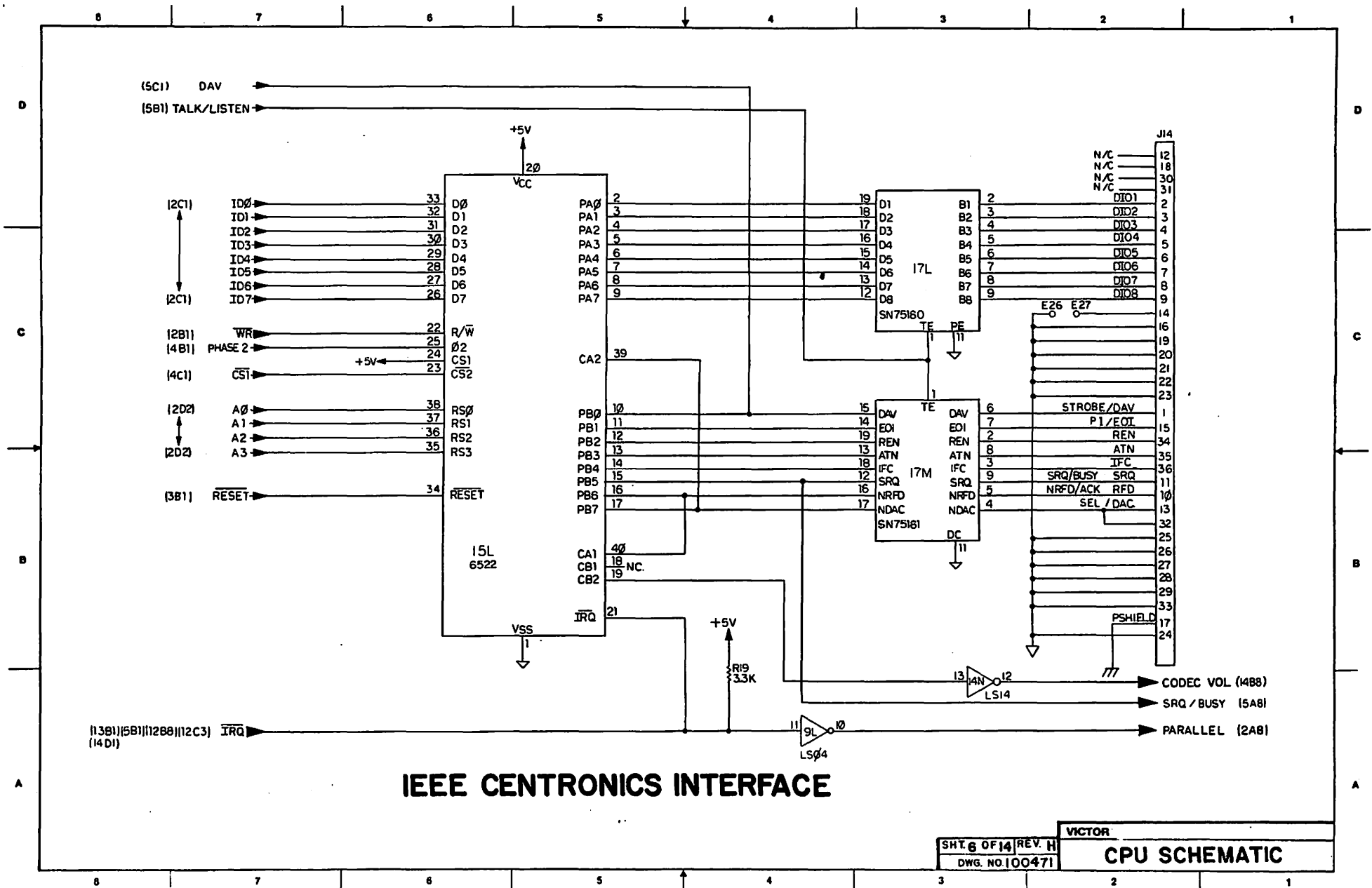
SHT. 7 OF 14 REV. H
DWG. NO. 100471
VICTOR
CPU SCHEMATIC

SCREEN MEMORY

SYSTEM MEMORY

CRT INTERFACE

VICTOR

CPU SCHEMATIC

SHT. 100F14 REV. H
DWG. NO. 100471

SERIAL COMM INTERFACE

(4B1) R̄
(4B1) PHASE 2
(2C1) ID0
ID1
ID2
ID3
ID4
ID5
ID6
(2C1) ID7
(4D2) IRD̄
(4D2) IWR̄
(2D2) A0·A1
(4C1) IOD1
(3B1) CLK5

(5C1) INT/EXT A
(5C1) INT/EXT B

(3B1) RESET

(4C1) IOD2

8253
D0 CLK2 18
D1 GATE2 16
D2 OUT2 17
D3   11F
D4 CLK1 15
D5 GATE1 14
D6 OUT1 13
D7
RD̄
WR̄
A0 CLK0 9
A1 GATE0 11
C̄S̄ OUT0 10
VSS VCC 24

+5V
¼LS90
CKA QA
12E

+5V
LS90 11E
R0 VCC QD
R1 QC N/C
LS90QB N/C
CLKA QA
CLKB

+5V
QA 12
10E
A
LS90

TIMER (2A8)

+5V

RIA (5D8)
DSR A
RIB
DSR B (5D8)

IC0
IC1 15F
IC2 1Y
IC3
1G
LS153

D0 RXCA 35
D1 TXCA 36
D2 RXDA 34
D3 TXDA 37
D4
D5 CTSA 39
D6 RTSA 38
D7 DCDA 3
RESET DTRA 31
CLK
WR̄ RXCB 4
RD̄ TXCB 7
RXDB 9
13E TXDB 8
INTA 27
CTSB 6
RTSB 10
DCDB 5
C/D DTRB 26
B/A INT 28
C̄S̄
VSS PD7201
SERIAL CONTROL

A 14 D RXDA 1
B
C
D MC1489
2 A 15 D TXDA 3
B RTSA
C DTRA
D TTXCA
MC1488

A 14 E RXDB 1
B CTSB
C DCDB
D RXCB
MC1489
A 15 E TXDB 3
B RTSB
C DTRB
D TTXCB
MC1488

+12V
-12V

R76
1K +5V

16E
MC1489

IC0
IC1 16F
IC2 1Y
IC3
1G
LS153

2C0 16F
2C1 2Y
2C2
2C3
2G
LS153

S04
COMM (2A8)

J8
RXDA 3
CTSA 5
DCDA 8
RXCA 17
TXDA 24
RTSA 2
DTRA 4
TXCA 20
RIA 15
DSRA 22
CHS GND A 6
SIG GND A 1/7
COMM PORT A

J9
RXDB 3
CTSB 5
DCDB 8
RXCB 17
TXDB 24
RTSB 2
DTRB 4
TXCB 20
RIB 15
DSRB 22
CHS GND B 6
SIG GND B 1/7
COMM PORT B

LITE PEN (8C8)

+5V

20
VCC

J5
+ 12V 5
+ 12V 6
- 12V 1
- 12V 2
10

(2C1)
ID0 33 D0 PA0 2 16
ID1 32 D1 PA1 3 18
ID2 31 D2 PA2 4 20
ID3 30 D3 PA3 5 22
ID4 29 D4 PA4 6 24
ID5 28 D5 PA5 7 26
ID6 27 D6 PA6 8 28
(2C1) ID7 26 D7 PA7 9 30

+5V 7
+5V 8

(2B1) WR 22 R/W CA1 40 12
(4B1) PHASE 2 25 Ø2 CA2 39 14
24 CS1
(4C1) CS4 +5V 23 CS2

PB0 10 32
PB1 11 34
(2D1) A0 38 R0 PB2 12 36
A1 37 R1 PB3 13 38
A2 36 R2 PB4 14 40
(2D1) A3 35 R3 PB5 15 42
PB6 16 44
(3B1) RESET 34 RESET PB7 17 46

CB1 18 48
CB2 19 50

14 L
6522

11
13
15
17
19
21
23
25
27
29
IRQ 21 31 IRQ (6A8)
33 CODEC CLOCK (14D8)
35
37
39
41
43
45
47
49

USER
PORT

GND
1

USER PORT

CPU CONNECTORS (REF)

J1   J2   J3   J4   J10

POWER SUPPLY

Signal	(ref)	J1	J2	J3	J4
BD0	[2C1]	25	25	25	25
BD1		26	26	26	26
BD2		24	24	24	24
BD3		27	27	27	27
BD4		23	23	23	23
BD5		28	28	28	28
BD6	[2C1]	22	22	22	22
BD7		29	29	29	29
A8	[2D2]	6	6	6	6
A9		45	45	45	45
A10	[2D2]	5	5	5	5
A11	[2D1]	46	46	46	46
A12		4	4	4	4
A13		47	47	47	47
A14		3	3	3	3
A15		48	48	48	48
A16		2	2	2	2
A17		49	49	49	49
A18	[2D1]	1	1	1	1
A19	[2D1]	50	50	50	50
XACK	[2D6]	21	21	21	21
CLK15B	[3C1]	40	40	40	40
HLDA	[2C1]	18	18	18	18
HOLD	[2C8]	17	17	17	17
ALE	[2C1]	9	9	9	9
IO/M	[2C1]	10	10	10	10
RD	[2B1]	11	11	11	11
WR	[2B1]	14	14	14	14
DT/R	[2B1]	12	12	12	12
DEN	[2B1]	8	8	8	8
PHASE 2	[4B1]	20	20	20	20
CSEN	[4A1]	19	19	19	19
NMI	[2C8]	15	15	15	15
RESET	[3A1]	13	13	13	13
CLK5	[3B1]	38	38	38	38
+5V		36	36	36	36
+5V		37	37	37	37
+12V		34	34	34	34
-12V		32	32	32	32
		31	31	31	31
DLATCH	(2B5)	33	33	33	33
		35	35	35	35
		39	39	39	39
		44	44	44	44
EXTIO	(4B8)	30	30	30	30
IR4	(2A6)	43	43	43	43
IR5	(2A8)	42	42	42	42
SS0	(2B1)	7	7	7	7
IRQ	(6A8)	16	16	16	16
READY	(2D3)	41	41	41	41

EXPANSION BUS

J10 POWER SUPPLY

- 8 → -12V
- 7 → +12V
- 1, 2, 3 → +12VV
- → +5V
- 6, 4 → KEY (GND)
- 5

J12 DISC POWER

	J12
+ 5V	6
+ 12V	1
KEY	5
- 12V	3
GND	2
GND	4

J7 DISK DRIVE

Signal	(ref)	J7
ID0	[2C1]	1
ID1		3
ID2		5
ID3		7
ID4		9
ID5		11
ID6		13
ID7	[2C1]	15
WR	[2B1]	33
PHASE 2	[4B1]	37
CS5	[4C1]	19
CS6		17
CS7	[4C1]	35
A0	[2D2]	41
A1		43
A2		45
A3	[2D2]	47
RESET	[3B1]	49
WRTCLK	[5A1]	25
CLK5	[3C1]	27
IRQ	[6A8]	21
SYN	[2A8]	23
LBRDY	[2D8]	39

2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 44, 46, 48, 50

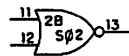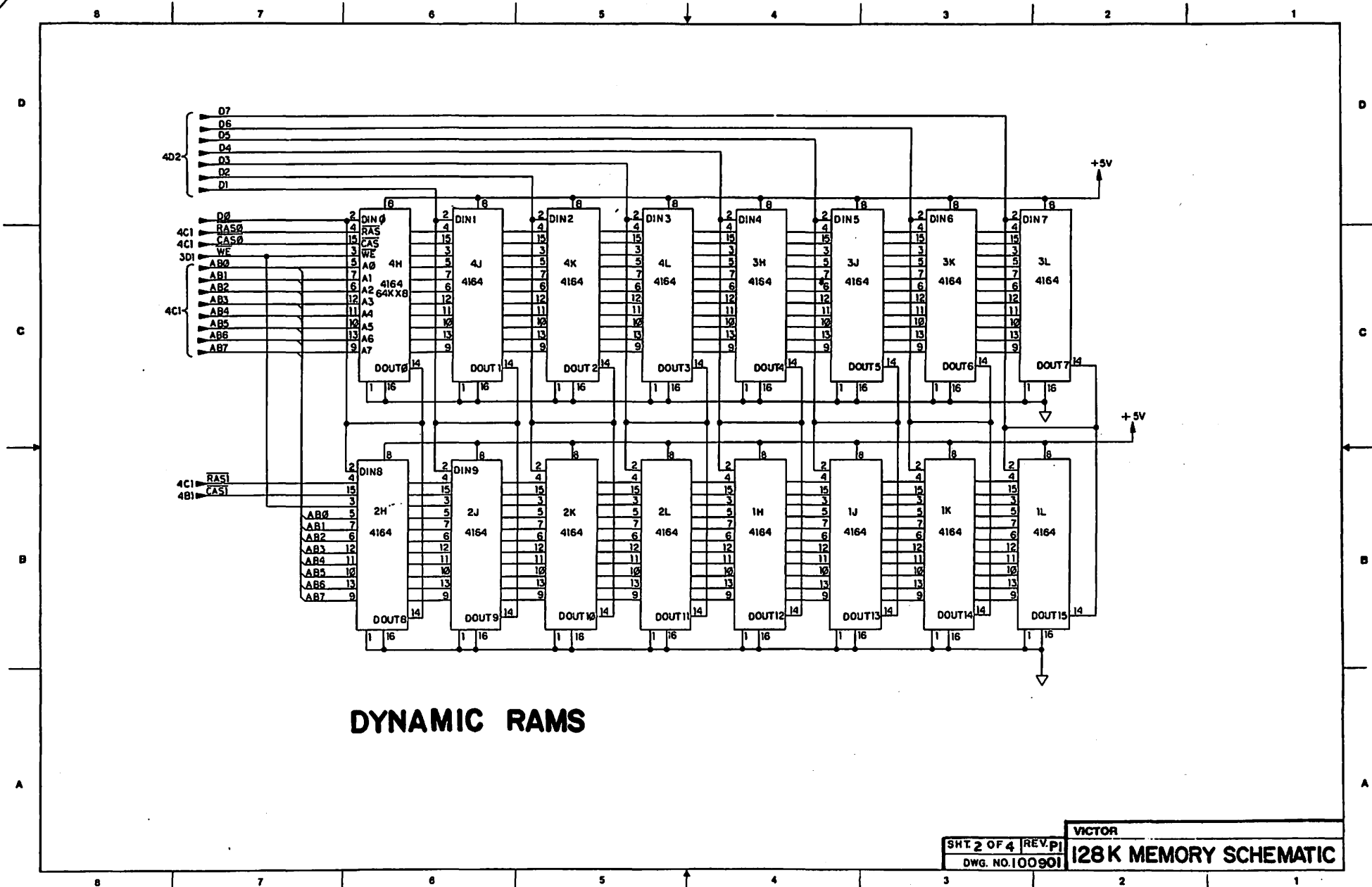**AUDIO INTERFACE**

POWER & SPARES

NOTES: UNLESS OTHERWISE SPECIFIED

1. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS, AND MICROHENRIES.
2. ALL RESISTORS ARE ±5%, 1/4W
3. ALL INTEGRATED CIRCUITS ARE SN74 SERIES.
4. IC PINS ARE, GND = 7, +5V = 14

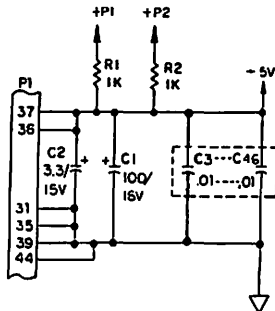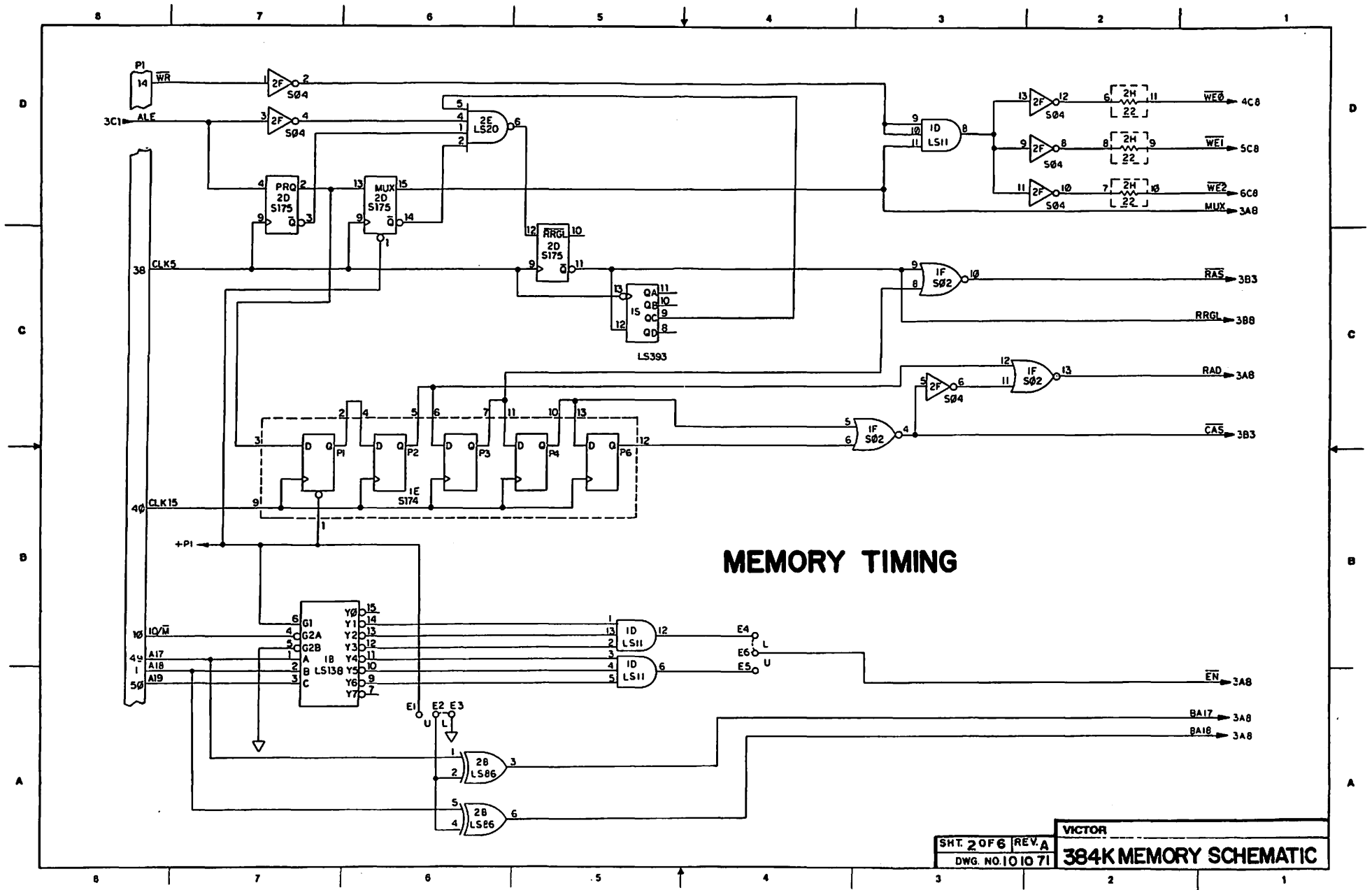| IC TYPE	GND	+ 5V
74LS138	8	16
74LS139	8	16
74LS153	8	16
74LS157	8	16
74LS174	8	16
74LS175	8	16
74LS245	10	20
74LS373	10	20
4164	16	8

SPARE GATES

MEMORY TIMING

VICTOR

128K MEMORY SCHEMATIC

MEMORY ADDR/
DATA CONTR'L

SHT. 4 OF 4 | REV. P1
DWG. NO 100901

VICTOR
128 K MEMORY SCHEMATIC

DYNAMIC RAMS

+PI +P2

R1 R2
1K 1K

−5V

P1
37
36

C2
3.3/
15V

+ C1
100/
16V

C3---C46
.01---.01

31
35
39
44

NOTES: UNLESS OTHERWISE SPECIFIED

1. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS, AND MICROHENRIES.
2. ALL RESISTORS ARE ±5%, 1/4W
3. ALL INTEGRATED CIRCUITS ARE SN74 SERIES.
4. IC PINS ARE , GND = 7, +5V = 14

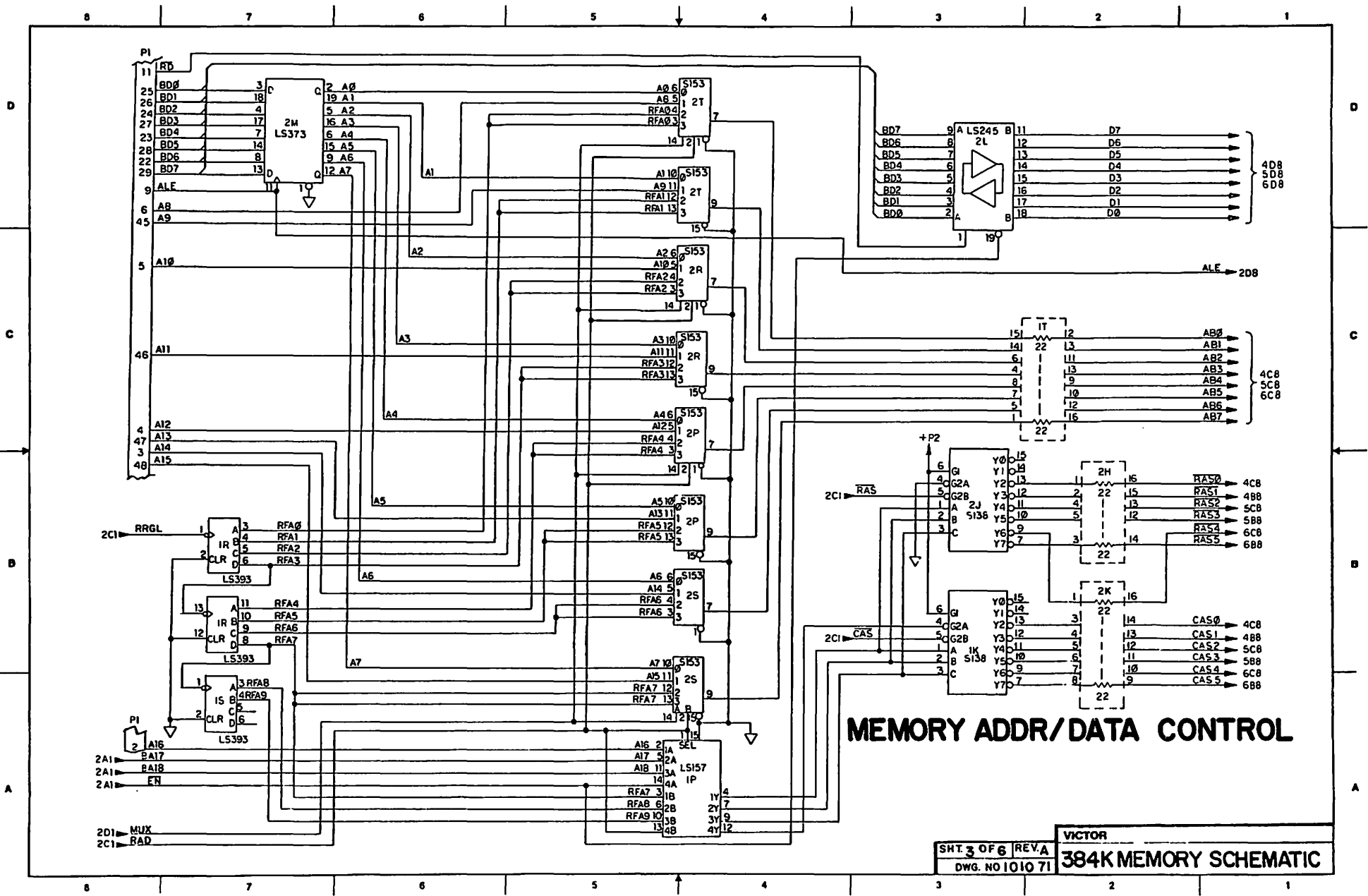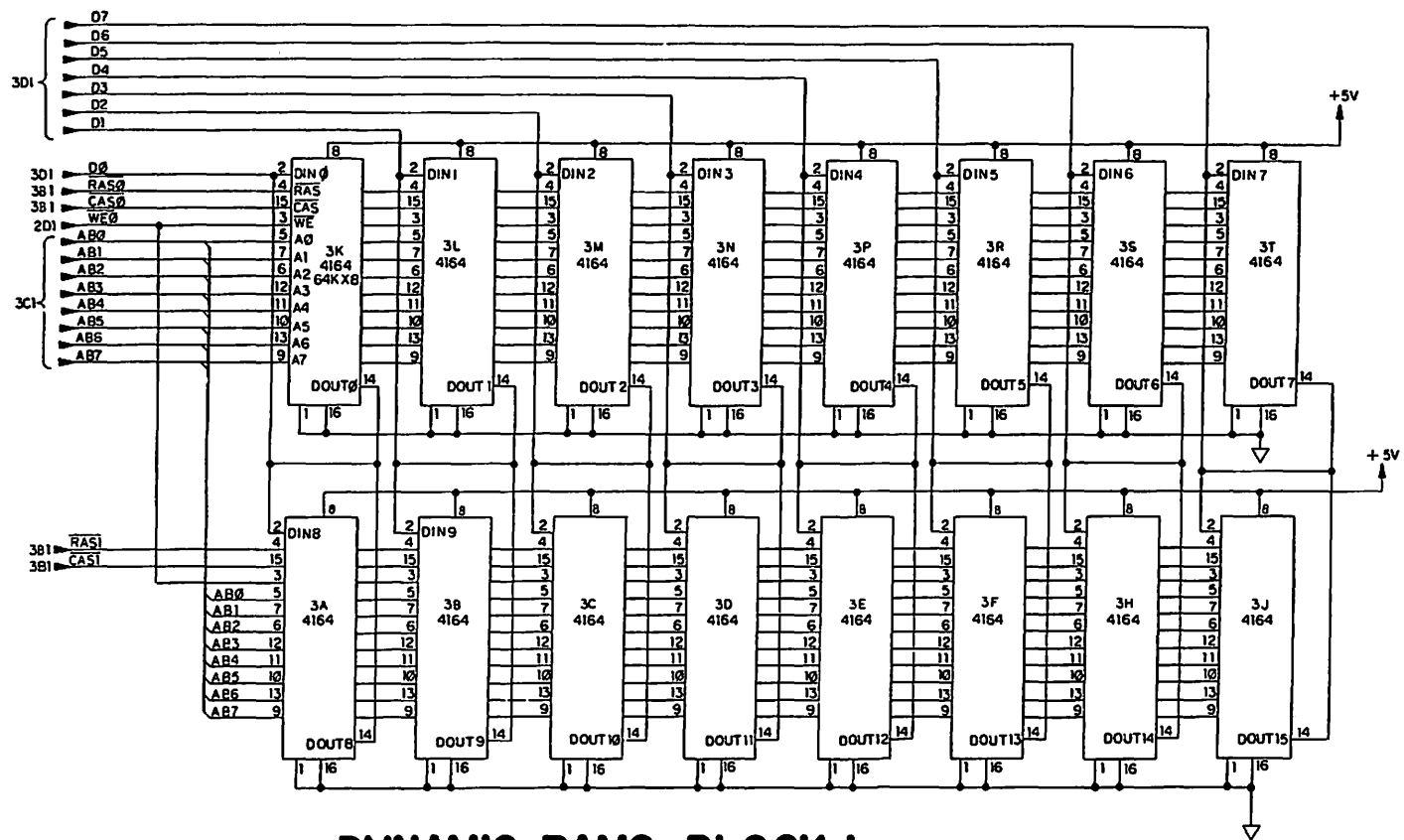| IC TYPE	GND	+ 5V	
74LS138	8	16	
74 S153	8	16	
74LS157	8	16	
74 S174	8	16	
74 S175	8	16	
74LS245	10	20	
74LS373	10	20	
4164	16	8	(REF)

POWER & SPARES

2 2K 15
22

13
12
10
9

2E
LS20

8

2
3

1F
S02

1

9
10

2B
LS86

8

12
13

2B
LS86

11
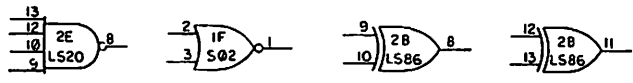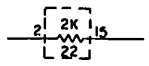
SPARE GATES

VICTOR

384K MEMORY SCHEMATIC

MEMORY TIMING

MEMORY ADDR/DATA CONTROL

VICTOR

384K MEMORY SCHEMATIC

SHT. 3 OF 6 REV. A

DWG. NO 1010 71

DYNAMIC RAMS, BLOCK I
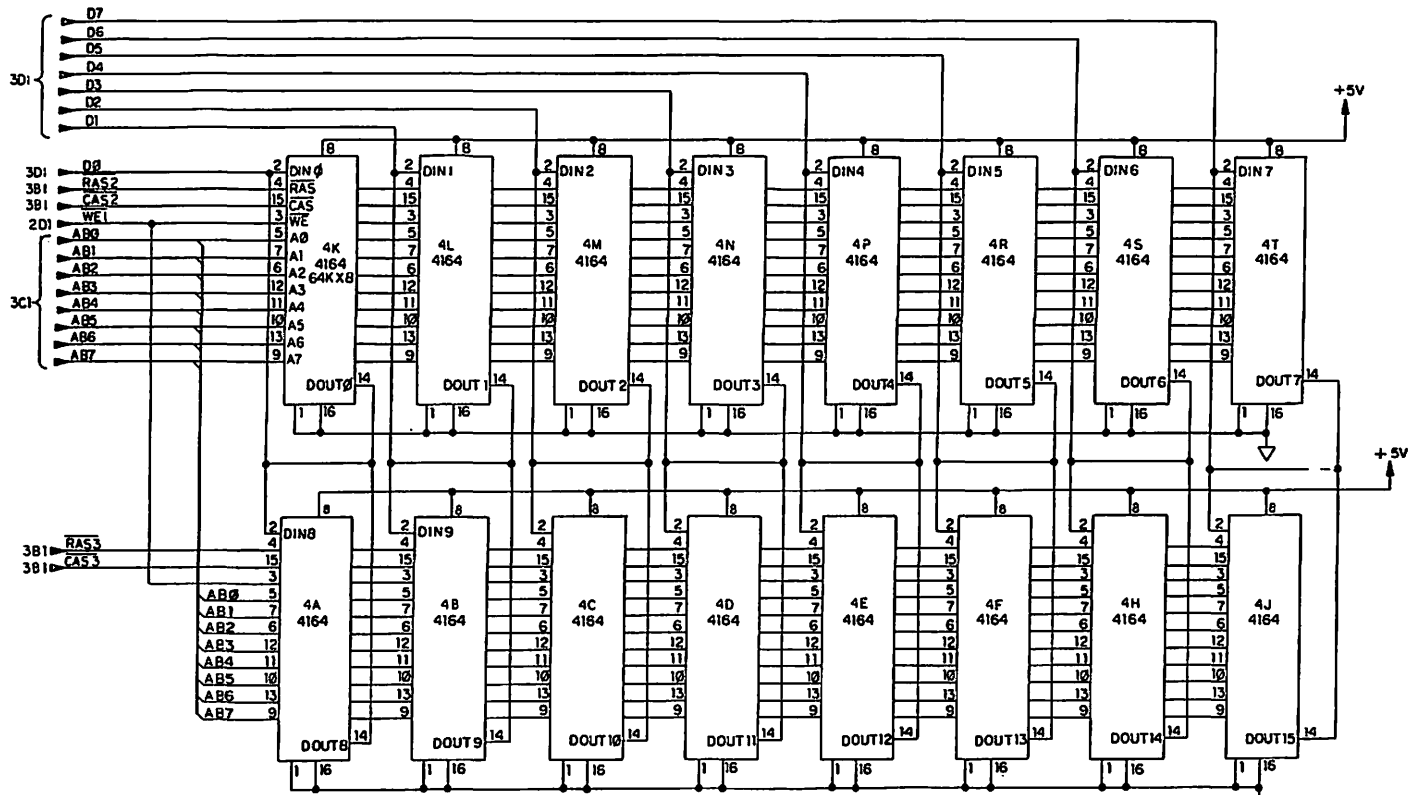
DYNAMIC RAMS, BLOCK 2

DYNAMIC RAMS, BLOCK 3

SHT. 6 OF 6 | REV. A
DWG. NO. 10 10 71

VICTOR
384K MEMORY SCHEMATIC
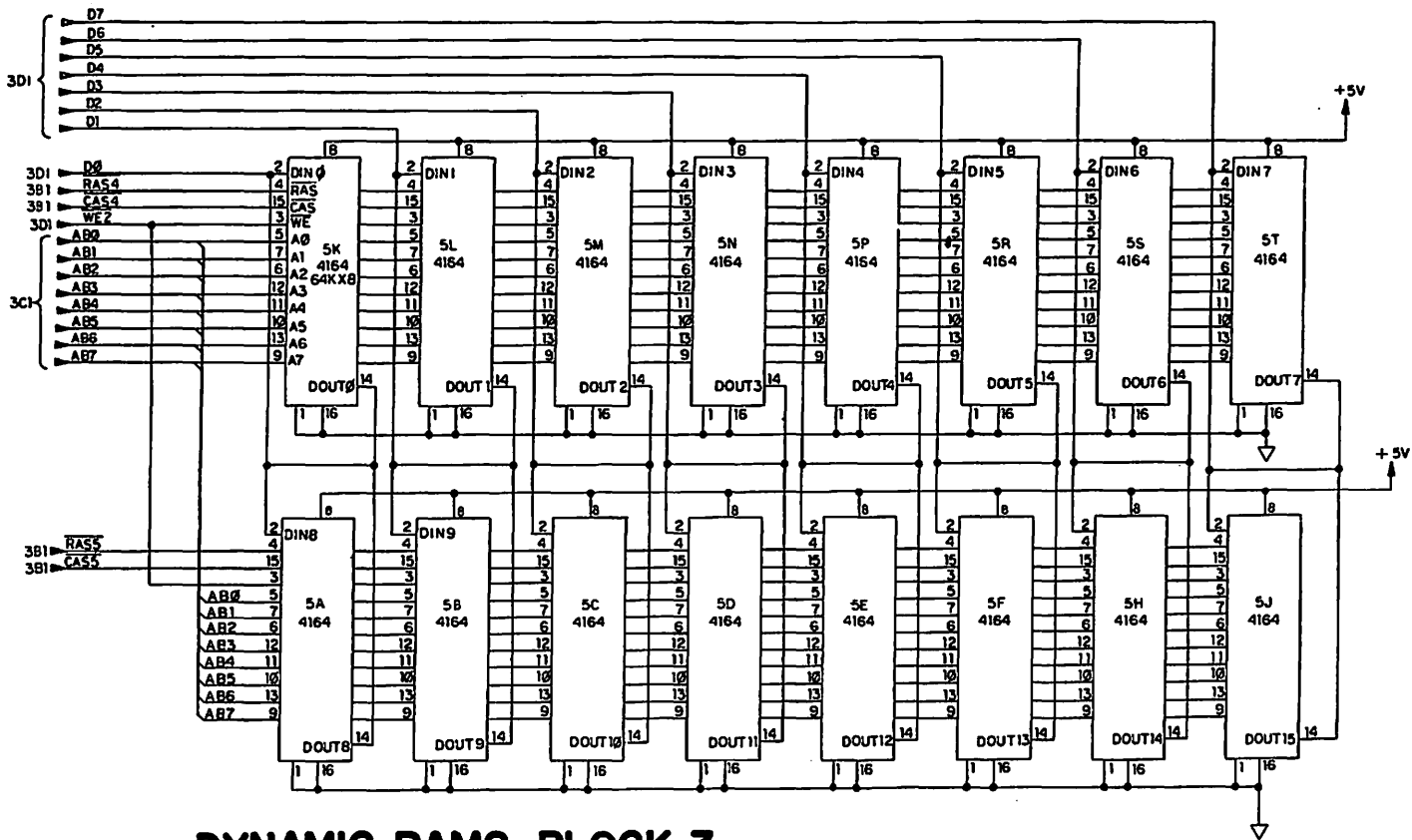
SECTION FOUR............FAULT ISOLATION

4.1   POWER SUPPLY FAULT ISOLATION

SECTION A
MISSING ALL VOLTAGES

************************WARNING********************

1. SCOPE SHOULD BE PLUGGED INTO A UNGROUNDED POWER SOURCE.

2. WHEN CHECKING COMPONENTS ON THE PRIMARY SIDE, USE ANODE SIDE OF D110 AS PRIMARY GROUND.

3. **DISCHARGE CAPACITORS C101,102,105, AND 106**
        THESE CAPACITORS CHARGE UP TO APPROX. 160VDC.
BAD POWER SUPPLY BOARDS RETAIN CHARGE LONGER THAN FUNCTIONAL POWER SUPPLY BOARDS.

****

1. Check F101 fuse for open, if bad replace component
   check voltage at fuse with respect to primary ground
   (NORMAL OPERATING APPROX. 330V P-P 116.65 EFF.)

2. Check thermal resistor THR101 for open
   (NORMAL OPERATING .080VAC ACROSS THERMISTOR)

3. Remove power from board, **DISCHARGE CAPACITORS**
   Check diodes D101,102,103,104 for open
   If bad replace component(s)

4. Check R101 for APPROX. 300VDC (NORMAL OPERATING VOLTAGE)
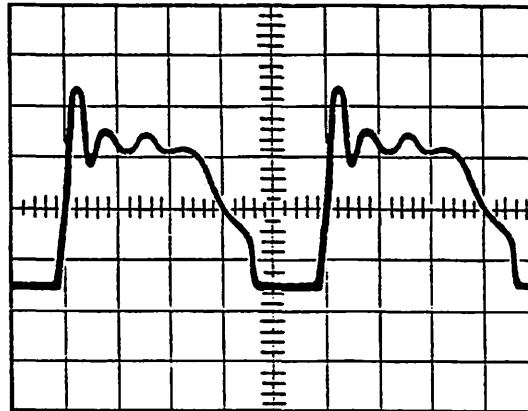   If no voltage, go back to step 1

5. Check fuseable resistor R106 for open if bad replace component
(NORMAL OPERATING VOLTAGE APPROX. 330VDC)

6. Check Q103 case voltage with respect to primary ground
(NORMAL OPERATING APPROX. 225-300VDC)

   ***************CAUTION*********************************
                    sonde
      DO NOT TOUCH SCOPE PROBE TO HEATSINK WHILE CHECKING
      CASE VOLTAGE.

   ****
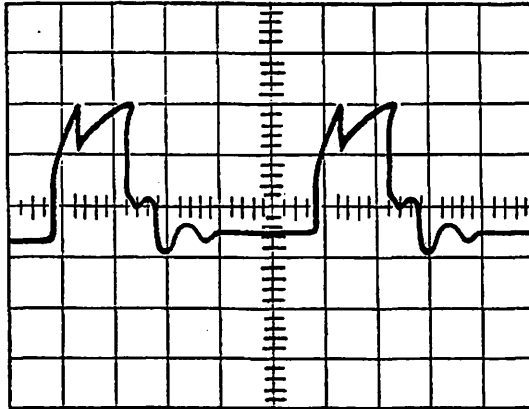

COLLECTOR OF Q103

20 V/Cm
5μsec/Cm
78V P-P

7. Check R103 and C103 for open or short
   If bad replace component

   R103-C103 JUNCTION WAVEFORM

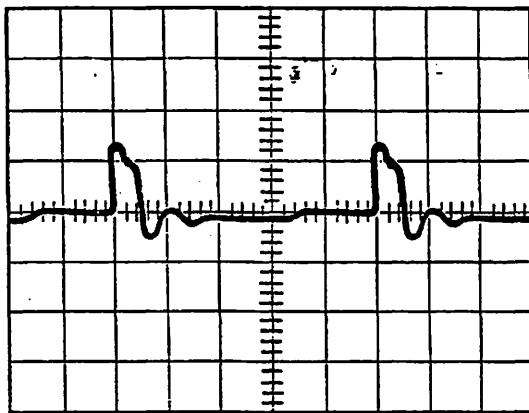### JUNCTION OF R103-C103

I V/Cm
5µsec/Cm
3V P-P

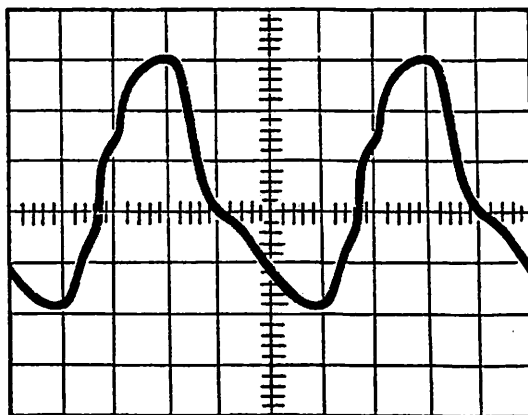8. Check Q102 for open, If bad replace component
   Base of Q102 WAVEFORM

BASE OF Q102

I V/Cm
5µsec/Cm

9. Check Q101 for open, If bad replace component
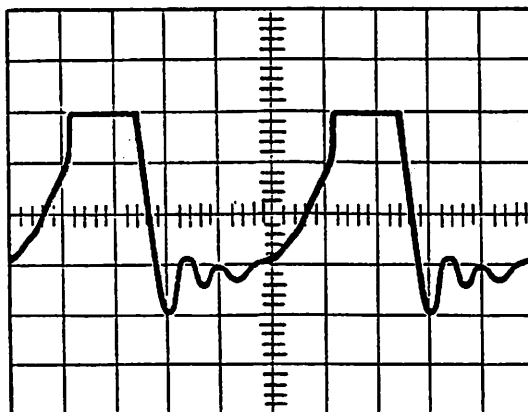   emitter of Q101 waveform

EMITTER OF QI0I

5 V/Cm
5 μsec/Cm
20V P-P

10. Check D105 for open (POWER OFF), If bad replace component
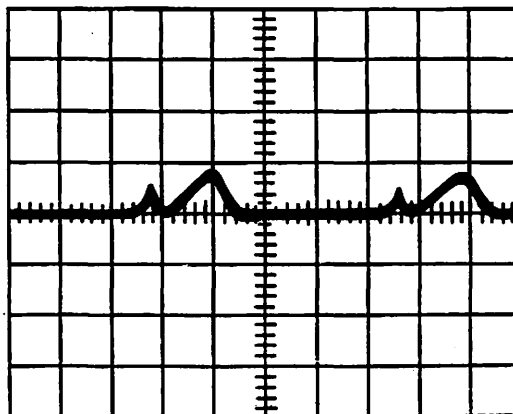   CATHODE OF D105 WAVEFORM

ANODE OF DI05

5 V/Cm
5 μsec/Cm
20V P-P

11. Check C111 for open, If bad replace component
    POS. SIDE OF C111 WAVEFORM

POS. (+) SIDE OF CIII

I V/Cm
5 μsec/Cm
I V P-P

**********************WARNING*********************************

WHEN ON THE SECONDARY SIDE OF TRANSFORMER, USE SECONDARY
GROUND.   USE BASE OF Q106 FOR SECONDARY GROUND.
****

SECTION B
NO +12V (UNREG)

1. Check T1 pins 1 and 2 for approx. 8.6VAC
     If no voltage, go to section A

2. Check D115 for open or short
     Normal operating level 12.2 VDC
     If bad, replace component

SECTION C
NO +12VV (REG)

1. Check T1 pins 11 and 12 for 11.5VAC
   If no voltage, go to section A

2. Check D118 for open or short
   Normal operating level 15.2VDC
   If bad, replace component

3. Check regulator A102 for approx.15.3vdc input
   and approx. 12vdc output
   If no output, replace A102

4. Check protection diodes D116 and D117 for open
   If bad replace component

SECTION D
NO -12 VDC

1. Check T1 pins 11 and 12 for approx. 11.5VAC
   If no voltage, go to section A

2. Check diode D121 for open or short
   Normal voltage -16.3 VDC

3. Check A104 for approx. -16.3v input
   and -12v output
   If no output or wrong output,replace A104

4. Check D119 for open or short
   If bad, replace component

SECTION E
NO +5 VDC

1. Check T1 pins 3 and 4 for approx. 3.6VAC

IF NO VOLTAGE, GO TO SECTION A

2. Check diode D112 for open or short
   Normal voltage level 5.1 VDC
   If bad, replace component

   NOTE: DIODE D111 IS FOR OVER VOLTAGE PROTECTION OF THE
         +5 VOLT SUPPLY. IF D111 IS CONDUCTING, THE +5 VOLT
         SUPPLY WILL NOT FUNCTION.

SECTION F
BLOWING FUSES

1. SCR A103 and diode D111 are used for overvoltage protection
   Check A103 for open
   If bad, replace

2. Check D112,D115,D121, and D118 operating voltages
   If wrong voltage, go to appropriate trouble shooting section

3. Check diodes D118 and D119 for open or short
   If bad, replace component

SECTION G
NO REGULATION

1. Short A101 pins 4 and 5 together
   If the power supply shuts down, the problem is in the
   OP AMP regulator section

2. If no shut down occurs,then check Q101 for open.
   check C110 for open
   Replace component(s)

SECTION H
OP AMP REGULATION

1. Check -12v supply for proper operation
   If bad go to section D

2. Check +5v supply for proper operation
   If bad, go to section E

3. Check Q104,Q105,Q106 FOR OPEN
   If bad, replace component(s)

4. Check R116 potentiometer
   If bad, replace component

4.2 VIDEO CONTROL BOARD

Fault Isolation on the Video Control Board is divided into two sections: (1) Component failure and (2) adjustments.

1. COMPONENT FAILURES

A. Supply Voltages:

1. Is the +12 Volts Present at Pin 1 of Connector J1? Check connector J1 (Pin 1), the Power Supply Assembly and Fuse F901.

2. Is the +12 Volts present at Pin 3 of Connector P1 ? Check connector P1 resistor R901 and +12 Volt Supply from Power Supply Assembly.

3. Is the -180 Volts Present at Pin 1 of Connector J2 ? Check transformer T702 (Pin 6),Diode D752 or connector J2.

4. Is the +300 Volts Present at Pin 6 of connector P1 ? Check Transformer T702 (Pin 8),Diode D751,resistor R753 Spark Gap SG751 or connector P1.

5. Is -65 to -165 Volts Present at Pins 3 and 4 of connector J2 ? Check resistor R51,R758,R759 or Zener Diode ZD751.Check connector J2, Pins 3 and 4.

6. Is +50 Volts Present at the Cathode of Zener Diode ZD751 ? Check Zener ZD751.

7. Is 0 to 150 Volts Present at Pin 7 of connector P1 ? Check resistor R754,R755, capacitor C755 Spark Gap SG752 or connector P1.

8. Is 12K Volts present at Pin 1 of connector P2 ? Check connector P2 or replace Transformer T702.*WARNING High voltage equiptment is required to test **12,000V line***

9. Is +200 Volts Present at Collector of transistor Q704 ? Replace Transformer T702.

B. BRIGHTNESS CIRCUITS

1. Dim Display. Check -180 Volt Supply, Resistor R758 or Keyboard Brightness Control Switches.

2. Display Too Bright. Check -180 Volt Supply,
Resistor R758 or Zener Diode ZD751.

C. HORIZONTAL CIRCUITS

1. No Input Horizontal signal to base of transistor
Q701. Check Diode D701, Resistor R703, Capacitor C701 or
the Input Horizontal Signal from the CPU Board (Pin 4 of
connector J1)

2. Proper Input Signal from CPU, no Horizontal signal
on Pin 1 of connector J4. Check to insure transistor Q701
is turning on and off. Check to insure transistor Q702 is
turning on and off opposite of transistor Q701.(If not,
replace Q701,Q702, R711 or C711) With Q702 on does Q703
turn on ? Replace Q703. With Q703 on does Transformer T701
produce an output which turns transistor Q704 on ? Replace
Q704 or Transformer T701 or both.(Output Signal should be
switching between 0 and +225 Volts.)

D. VERTICAL CIRCUITS

1. No Vertical Drive signal at Pin 6 of IC601. Check
transistor Q601,Connector J1, Pin 5 or the Vertical Drive
Signal from the CPU Board.

2.Vertical Roll. Check resistor R611 or IC601. Replace
if necessary.(No Effect on Vertical Roll.)

3. Vertical Size. Check resistor R622, R624 or IC601.
Replace if necessary. (No Effect on Vertical Size.)(Number
of Characters on the Screen.)

4. Vertical Linearity.(Height of Characters on Screen)
Check resistor R624 and/or IC601. Replace if necessary.

5. No Vertical Output Signal at Pin 1 of IC601. Check
IC601 for a +5 to +15 Signal at a 850 usec pulse width and
a 76hz. rate.Replace if necessary. Check connector J3 Pin
1.

E. **VIDEO CIRCUITS**

1. No Video Signal (Switching from +60 volts to +40 volts with a .1usec pulse width and a 17.5 mhz. rate) at the base of transistor Q202. Check transistor Q202 and Q201. Replace if necessary. Check connector J1 Pin 6. Check output of CPU board. Ensure that overvoltage protector tube NE201 is good. Replace if necessary.

2. No Video Signal due to overvoltage.Check if Zener Diode ZD771 is conducting. Is +12 Volts gone.(If in a overvoltage situation the +12 volts will not be present, indicating the Zener should be operating.)

3. Overvoltage Circuit does not work when in an overvoltage condition. Check Transistors Q771 and Q772, Zener Diode ZD771, Video Signal and Horizontal Signal.

2. **VIDEO ADJUSTMENTS**

1. R611 is used to adjust the vertical hold.

2. R624 is used to adjust the vertical linearity.

3. R622 is used to adjust the height.

4. R754 is used to adjust the focus.

5. R758 is used to adjust the brightness.

6. L704 is used to adjust the width.

4.3.1 SEEK LOGIC FAILURE

The seek circuit is composed of 2 6522 Versatile Interface Adaptors (VIA), 2 quad "NAND" gate IC's and 2 quad driver IC's.

When a seek operation is to take place, the 8088 will send the data to a VIA. The VIA will output the STP0 signal for the A drive and STP1 for the B drive to select the proper stepper motor. These signals are routed to the "NAND" gate IC as one enable to all 4 gates. Through another VIA, the 4 phase stepper signals will be generated as ST0 A-D for the A drive and ST1 A-D for the B drive. These signals, going high, will be the other enabling input to the "NAND" gates. The "NAND" gate outputs are routed to the stepper motor driver IC, which will cause the motor to step in or out one track at a time. The ST signal wave forms are shown in Section 3.3.1.

Seek failures can be either a total failure or a partial failure. The failures can also be on one drive. By running the Seek Test all the associated stepper signals can be traced on the oscilloscope.

1. If both drives are failing, suspect a missing control signal from the VIA.

Check to see that the STP0 or the STP1 are high to select the drive. Also check for the presence of the PHASE 2 clock. Check to see if the chip is selected by a low on the $\overline{CS2}$ input. Check to see if the data is input to the VIA.

2. When one drive is failing, the control signals for the failing drive should be checked.

The seek circuits for the two drives are for the most part independent of each other. The drives are controlled by different ports on the VIA. The PA port controls the stepper signals for the A drive by the ST0A-D pulses. The PB port controls the B drive by the ST1A-D pulses. The ST pulses should be switching each time the motor is to step (refer to 3.3.1 for the stepper phase pulse sequence). The STP and the ST pulses together control the stepping through the "NAND" gates to the driver IC's.

3. If the seek circuits are stepping incorrectly, the ST pulses are probably not switching correctly.

4.3.2 MOTORSPEED FAILURE

The motorspeed circuit is composed of a 6522 Versatile Interface Adaptor (VIA), an 8748 microprocessor, 2 74LS373 Data Latches (one for each drive), 2 DAC0808 Digital to Analog Converters (one for each drive), 2 CS2917 motor speed regulators (one for each drive) and 2 driver transistors (one for each drive).

When the spindle motor is to be turned on, a data byte with the desired speed value is transferred from the 8088 to the VIA on the ID0 - ID7 bus. The VIA transfers the speed value to the 8748 (LOMS0-3 & LOMS0-3). The 8748 transfers the speed value to the DAC through the data latches. The DAC will convert the digital speed value to an analog signal to drive the motors. This signal is routed to the motor speed regulators which use the tach signals as a feed back input. The speed regulator output controls the bias for the motor drive transistors. The 8748 controls the A and B drives by the select signals (SEL 0 & 1), the start signals (START 0 & 1), the stop signals (STOP 0 & 1). The 8748 also monitors the speed of the motors by the tach signals (TACH 0 & 1). When the motor is running at the correct speed, the 8748 informs the VIA of this by the ready signals (READY 0 & 1).

Motorspeed failures can be either a total failure or a partial failure. The failure can also be on one drive. When a total failure occurs, the enabling signals should be checked. The following list gives points to check and the inputs required to enable the various devices at the check points. A mid-point of the checks should be chosen to facilitate fault isolation.

Total Speed Failure

1. Check to see that the VIA is selected by a low on the CS2 input. Also check to see if the PHASE 2 clock is present (1 Mhz signal).

2. Check to see if the motorspeed data is being transferred to the 8748. These outputs are LOMS0 - 3 for A drive and L1MS0 - 3 for the B drive.

3. Check the START 0 and 1 signals to see if they go low momentarily then high when a motor is selected.

4. Check to see if the STOP signal goes low when the motor is selected.

5. Check to see if the SEL 0 and 1 signals go high when a motor is selected. These signals enable the data latches when high and latch the data on the output when they go low.

Speed Failure On One Drive

1. Check to see if the byte is being output from the data latch to the DAC.

2. Check to see if the data is being output from the DAC (analog level at 2.2v zone 0 to 3.6v at zone 8).

3. Check to see if the signal is input to the speed regulator. Also check the TACH signal, as it is a feed-back input to the speed regulator.

4. Check to see if the data is being output from the speed regulator to the base of the motor drive transistor (A 1.4 msec pulse occurring at .8 msec rate at zone 0 to a .6 msec pulse occurring at .8 msec rate at zone 8).

5. Check to see if the motor driver transistor is providing the output to drive the motor.

Partial Speed Failure

1. If the motorspeed is experiencing partial failure, check the TACH input to see if it is at proper frequency (a 2.4 msec pulse occurring at 2.2 msec rate at zone 0 to a 1.4 msec pulse occurring at 1.4 msec rate at zone 8).

2. Check to see if the RDY signal goes high to inform the 8748 that the motor is at the proper speed.

3. Check the latching of the data to the DAC. When SEL is high, the speed byte will be input to the data latch. When SEL makes a positive to negative transition, the speed byte will be latched onto the output. If the data is not being latched, erroneous speed data may be entering the DAC.

4. Check to see if speed regular output is at correct frequency (see 4. above).

4.3.3 WRITE LOGIC FAILURE

The write circuit is composed of a 6522 Versatile Interface Adaptor (VIA), 3 74LS157 Data Selectors, 2 74LS165 Parallel to Serial converters, a D2716 GCR Rom, a D-type flip-flop, 2 electronic switch IC's and several logic gates. Another VIA produces the side and drive select signals and a 74LS139 2-4 decoder selects the proper head.

When data is to be written to the disk, the 8088 will transfer a byte of data to the VIA on the ID0-ID7 bus. The VIA will output the data on the WD0-WD7 bus to the data selectors. The data selectors route the data to the GCR Rom. The GCR Rom will then output a code so that no more than 2 0's in a row are written. This coded data is routed to the parallel to serial converters.

From the parallel to serial converter, the serial data is shifted out by the write clock and passed through a "NAND" gate to the write flip-flop. The Q and the $\overline{Q}$ output of the write flip-flop control the turning on of the write current to the read/write head. The outputs of the write flip-flop are routed through inverters to an electronic switch which turns on the write current. This inverter also enables the proper read/write head through another electronic switch.

A write failure can be a total failure or a partial failure. The failure can also be on one drive. For a total failure, an IC is either not being enabled or is defective and will not operate. Both the disk drives use most of the same circuitry to write on the disk, so if the failure is on one drive the control signals for that drive should be checked.

As an aid to fault isolation, install Write Test 1 or Write Test 2 diagnostics. Test 1 will write a sync pattern of all "ones" on track zero of a disk. Test 2 will write an alternating high and low pattern (1010) on track 0 of a disk. These tests will provide a continuous, distinctive data pattern which can be easily traced on an oscilloscope. The following list gives points to check and the inputs required to enable the various devices at the check points. A mid-point of the checks should be chosen to facilitate fault isolation.

Total Write Failure

For a total failure where the unit will not write to either disk at all, certain signals can be checked prior to running the diagnostics. Check the write clock and the phase 2 clock which should be present any time power is on.

If the clocks are good, run Write Test 2. While running, the unit will try to write the alternating 1 and 0 pattern. The high order nibble should be all 1's and the low order nibble should be all 0's.

1. Check to see if the VIA at 1F is selected by a low on the CS2 input. Also check to see that PHASE 2 clock is present at the VIA.

2. Check the data to the VIA on the ID0-ID7 bus. Also check the data out on the WD0-WD7 bus.

3. Check to see if the VIA at 1H is selected by a low on the CS2 input. Also check to see if the PHASE 2 clock is present. This VIA produces the SIDE SELECT and the DRIVE SELECT signals. Head 0 will be selected when these are low (refer to 3.3.3 for the head selection chart).

4. Check to see if the decoder at 3M is enabled by a low on G2. Also check the outputs to see if the proper heads are being selected.

5. Check to see if the data selectors are selected by a high on the SEL input. Also check the WD0-WD7 inputs and the I0-I9 outputs. Check for the presence of the write clock input and output at the data selectors.

6. Check for the presence of data into and out of the GCR Rom.

7. Check to see if the parallel to serial converters are enabled by a low on the LD input. Check to see if the output of the parallel to serial converter is a changing pattern (1010).

8. Check to see if the GCR data is present at pin 11 of the "NAND" gate. check for the presence of write clock write clock and GCR data at the inputs.

9. Check the write flip-flop for a changing state at the Q and the Q̄ outputs. Check to see if the PR and CLR inputs are at a high level. If the PR and CLR pins are held low, both the Q and the Q̄ outputs will remain at a high level. Check for the presence of the GCR data at the clock input.

10. Check to see if the inverter outputs at 2M are switching to a high level to enable the electronic switch at 2N.

11. Check to see if 2N is turning on to apply the write current to the head.

13. Check for a high on the inputs to the electronic switches at 1M & 1N.

Write Failure On One Drive

A write failure on one drive will be caused by a missing signal for that drive.

1. Check the SIDE SELECT and DRIVE SELECT signals at the VIA and at the 2-4 decoder.

2. Check the inverter output at 2M.

3. Check the electronic switch at 1M.

Partial Write Failure

If the controller is writing on the disk, but the data is incorrect, suspect a timing related problem or a component breaking down. The data can be checked to some extent during a write test 2. During a write test 2, a FO(H) character will be written. This will make the high order nibble all ones and the low order nibble all zeros going into the data selectors. The outputs of the data selectors will be a 10 bit code. The 2 extra bits are formed by the WRSYNC input for I5 and +5v input for I9. This will make I9 always high and I5 high only when writing sync. The output of the GCR Rom will be alternating high and low data lines. The output of the parallel to serial converter will be the 1010 pattern. The data flow can be checked for missing data bits.

4.3.4 READ CIRCUIT ANALYSIS

The read circuit consist of 3 linear amplifiers, 2 one-shot circuits, a 4046 Phase Lock Loop (PLL), a 74LS164 serial to parallel converter, 3 74LS157 data selectors, a D2716 GCR Rom, various flip-flops, Exclusive "OR" gates and a 6522 Versatile Interface Adaptor (VIA). Another VIA and a 74LS139 2 to 4 decoder are used for the drive and the read/write head selection.

The read recovery circuitry is self clocking, and requires no control signals other than a drive and side select to enable the proper head. At any time the disk is rotating, the read circuits will be functioning. The PLL generates the clock for recovery of the read data. The internal oscillator (VCO) in the PLL will operate at it's lowest frequency with no data input.

Read data from the disk is routed through a pre-amplifier filter network, a differentiator and a digitizer to the one-shot circuits. The Exclusive "OR" gates function as an edge detector. They will output a .2 usec pulse on the leading edge and a .6 usec pulse on the trailing edge. The one-shots will output a 1 usec pulse when triggered. The output of the last one-shot is the data input signal to the PLL and is also used as the clock for the bit comparing flip-flops (6N). The VCO signal is used to clock the bits through the first flip-flop stage (6N), inverted, then used as the clock for the second flip-flop stage (6M). The VCO is inverted one more time and used as read clock. The data and clock are routed through flip-flop 6K to the serial to parallel converter. From the S/P converter the data is input to the data selectors. The data selectors route the data to the GCR Rom. From the GCR Rom the data goes to the VIA and is output to the 8088.

Read failures can be a total failure or a partial failure. The failure can also be on one drive.If the controller will not read at all, suspect a timing problem, a defective component or a missing control signal. The read test has an alternating 1 and 0 (1010) pattern written on track zero. This test will provide a continuous, distinctive data pattern that can be traced through the circuitry. The following list gives points to check and basically what the signals should be. A mid-point of the checks should be chosen to facilitate fault isolation.

Total Read Failure

1. Check the output of the PLL. The PLL will generate a clock at it's lowest frequency with no data input. The signal may not appear as a stable signal, but should be checked for a changing state to insure the PLL is operating. If the PLL is working, run the read test.

2. The read test will input a 1010 pattern from the disk to the read circuitry with drive A and head 0 selected.

3. Check the input and output of the first amplifier stage. The input signal should look like an AC sign wave of appx 2-8 millivolts. If the signal is present, go to the next step. If no signal is present at the input, check for a high at pin 10 of inverter IC 2M. If this signal is not present, check for a low on pin 11 of 2M. If the signal is not present, check the SIDE SELECT and the DRIVE SELECT inputs to decoder at 3M. These inputs should both be low for drive 0 head 0. If these signals are not present, check the VIA to see if it is selected by a low on the $\overline{CS2}$ input. Also check for the presence of the input data and the PHASE 2 clock.

4. Check the input and the output of the second amplifier stage. An AC sign wave appx volts at the output.

5. Check the input and the output of the digitizer. A digital signal which looks like a 2 usec pulse at the output.

6. Check the output of the first edge detector for a .2 usec pulse on the leading edge of the signal and a .6 usec pulse at the trailing edge.

7. Check the output of the one-shot for a 1 usec low pulse at the $\overline{Q}$ output.

8. Check the flip-flop at 5N for the data .

9. Check the second edge detector for a.2 usec pulse on the leading edge of the signal and a .6 usec pulse on the trailing edge.

10. Check the second one-shot for a 1 usec pulse at the Q output.

11. Check to see if the data is being clocked through the flip-flop stages at 6N and 5M. If not, check the VCO and $\overline{VCO}$ signals at 5P pins 9 and 8. Also connect the scope to data input and to the clock input at the same time to see if the VCO is in the right time frame to clock the data through.

12. Check to see if the read clock is present at inverter 3L.

13. Check to see if the data is be clocked through 6K.

14. Check to see if the data is being output from the S/P converter.

15. Check to see if the data selectors are selected by a low on pin 1. Check the outputs of the data selectors.

16. Check the input and the output of the GCR Rom.

17. Check to if the data is present at the A port of the VIA and is output to the 8088 on the IDO-ID7 bus. If at the A port but not being output, check to see if the VIA is selected by a low on the $\overline{CS2}$ input. Also check for the presence of the PHASE 2 clock.

Read Failure On One Drive

A read failure on one drive will be caused by a missing signal at the VIA, the decoder, the inverter IC or the the electronic switch. The SIDE SELECT and the DRIVE SELECT signals produce the proper head through the 2 to 4 decoder. The 2 to 4 decoder outputs are routed through the inverter IC to the electronic switch. Refer to step 3 above for the required signals for drive 0 head 0. The other heads will be selected by the following SIDE SELECT and DRIVE SELECT configuration; DS low and SS high selects drive 0 head 1, DS high and SS low selects drive 1 head 0, DS high and SS high selects drive 1 head 1.

4-20

Partial Read Failure

A partial read failure will be caused by a bit being dropped or a component breaking down. The bit patterns can be traced through the circuitry following the steps for a total failure will running the read test. The read test will generate the 1010 pattern from the disk through the circuitry up to the GCR Rom. The output of the GCR Rom will be the upper nibble all 1's and the lower nibble all 0's. The data input to the flip-flop stages and the VCO should be looked at on the scope at the same time to insure that the VCO does not drift out of phase.

4.5 MEMORY EXPANSION BOARD FAILURE

Expansion memory board failures can be categorized into three classes. Each class maintains characteristic that will aid in identification. Once the class is identified a logical sequence of troubleshooting steps will allow the technician to repair the defective board.

The classes of failures are: 1) Control signal failure, 2) Refresh failure, and 3) RAM failure.

Each class can be identified by analyzing the error data recorded during diagnostic testing. The diagnostic will display an address and a data byte when a memory error is detected by software. The accumulation of memory errors will point to one of the three classes of failures.

The following table defines memory address space for each of the various blocks of memory.

MEMORY ADDRESS	LOCATION
00000-1FFFF	0-128K ON BOARD MEM
20000-3FFFF	128K-256K
40000-5FFFF	256K-384K
60000-7FFFF	384K-512K
80000-9FFFF	512K-640K
A0000-BFFFF	640K-768K
C0000-DFFFF	768K-896K
20000-7FFFF	1ST. 384K BOARD
80000-DFFFF	2ND. 384K BOARD

The failing address or addresses will point to either the on board memory, a 128K memory expansion board, or a 384K memory board.

A control signal memory failure will inhibit proper operation of the entire range of the memory board. If a critical control signal is lost (i.e. RAS,MUX,EN) the entire range of addresses on the board will fail. If the first address for the memory space of the board fails in a diagnostic mode, and each consecutive address to follow the failure is most likely in the control signal area of the board.

The following steps outline an efficient method of isolating and repairing a failing board with a Control Signal Failure.

1. Check for the presence of RAS, CAS, and MUX.
2. Check for the EN low when the memory board is accessed.
3. Check for the presence of RD and WR from the 8088 when a memory access is performed.

To evaluate step one above, place the board on the test bed in one of the expansion slots, or place the board on an extender in the mainframe. Once the system is booted, RAS, CAS and MUX will be active. As they are generated as a result of ALE, CLK5, and CLK15, they will be present even when the board is not being accessed.

If RAS is missing, check for the PRQ flip-flop set condition. Then check the counter flip-flops at 4D. Each one should be clocked set by CLK15. If CAS is missing, insure either P4 or P5 flip flop is setting. MUX is a direct result of the set condition of PRQ.

Execute a memory diagnostic selecting the proper configuration of memory to insure access to the failing board. Check for EN going low when the memory board is addressed by the 8088. Next insure that decoder chip 3F is outputting low signals when the memory address is addressed on the board.

Finally insure that RAD is low during a processor memory access cycle. If RAD is high the refresh address will be gated onto the bus rather than the processor address.

In the final step monitor the WR and RD signals through the board to insure that the memory chips are write enabled (WE) during the write cycle and the transceiver is directed to control the direction of data transfer.

A Refresh Failure will exhibit erratic data loss throughout the entire memory space of the board. The failure will most likely be visible in multiple addresses and multiple bit patterns.

A memory refresh failure may resemble a control signal failure, except if one address is selected and continually written into and then read, it will exhibit memory integrity. The best test then for a refresh failure is to select a small block of addresses and test them continuous within a small time span for memory integrity. Then write a pattern into them, delay long enough to exceed the 2 msec refresh requirement , and read the memory space. If the program demonstrates a memory error the problem lies in the refresh circuitry.

First, check that the RRGL flip-flop is being reset by "And" gate 4C and CLK5. Check that $\overline{RAS}$ goes low while RAD is high. Insure that the refresh address generator is incrementing with each RRGL transition. Finally insure that $\overline{RAS0}$ and $\overline{RAS1}$ go low to perform the RAS only refresh on the memory chips.

The third class of failure on the memory boards is a RAM Chip Failure. The symptom here would be a specific bit failing in one or more addresses on the board. The failing bit will remain within a 64K pattern of memory addresses. Analysis of the memory diagnostic error report will point to the failing RAM. Each RAM Chip represents a single bit in the byte for a 64K block of memory. The error data byte will point to one of two RAM Chips. The error address will isolate which of the two RAMs is failing. On the 384K board the error byte points to one of six, while the address will identify the failing RAM of the six.

A bad bus bit will exhibit the same symptom as a failing RAM with one exception; the failing bit pattern will transcend the bounds of a 64K block of memory.

The procedure for isolating faults in a 384K memory board is the same as with the 128K board. Remember the circuitry is designed the same, only there are three blocks of 128K of memory on each board. The same procedures would be used to determine if all 3 blocks are bad, one of the three blocks is bad, or one bit within a 64k block is bad.

Refer to the timing diagrams for the control signals in the memory board theory of operation to insure that signals are generated in the proper time sequence.

SECTION FIVE........CORRECTIVE MAINTENANCE

5.1 DISK DRIVE ASSEMBLY REPAIR

POWER REQUIREMENTS

D.C. POWER SEQUENCING

One second maximum from the time power is applied to
the time in which the unit will accept commands.

PRIMARY POWER

+12 VDC + or - 0.6 VDC @ 900 MA. (Average Max.)
+5 VDC + or - 0.25 VDC @ 600 MA. (Average Max.with
100 MV P/P Ripple.)

Connector J1

PERFORMANCE CHARACTERS

HEAD

Wear guaranteed 20,000 hours in media contact.

TRACKS

80 Tracks Side 0.
.264 mm (10.4 milli inch) Spacing
36.25 mm Track Radius (inside) Side 0.

MEDIA

133.4 mm (5.25 Inch) Industry Standard Diskette
3.6 X 10(6) Passes per track Minimum wear guarantee

ACCESS TIME

3.0 Millisec - Track to Track
15 Millisec - Head Settle Time

SCOPE

The Tandon Magnetics Corporation Flexible Disk Drive is a compact Data Storage device utilizing an industry Standard 5.25 inch Diskette (133.4 mm)
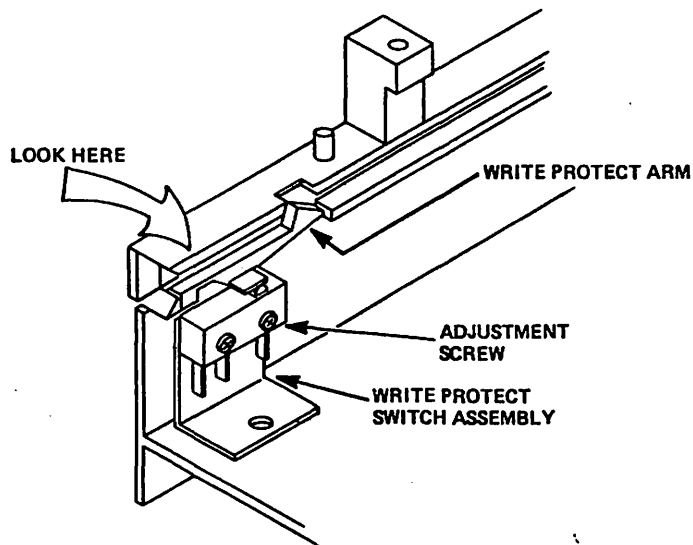
WRITE PROTECT (STANDARD)

When a Write Protected Diskette is inserted in the Flexible Disk Drive, the Write Electronics are disabled.

LED INDICATOR (STANDARD)

A Busy Indicator located on the Front Panel will become illuminated when the Flexible Disk Drive is selected.

WRITE PROTECT SWITCH ASSEMBLY

1. Visually ensure that the arm on the Write Protect Switch Assembly moves the switch and makes a clicking noise when the arm is pushed down.

Write Protect Switch Assembly Arm and Adjustment Screw

Figure 33

2. Remove the Defective Drive.

3. With a Phillips screwdriver, remove the mounting screw that attaches the Write Protect Switch Assembly to the side of the chassis.

4. Cut the harness that attaches the Write Protect Switch Assembly and the Activity LED Assembly cables to the bottom of the chassis.

5. Cut the harness that attaches the Write Protect Switch Assembly and the Activity LED Assembly cables to the bundle of wires that go to the Logic Board.

6. Remove the Write Protect Switch Assembly from the Disk Drive.

7. Place the new Write Protect Switch Assembly in position on the left-hand side of the chassis near the front.
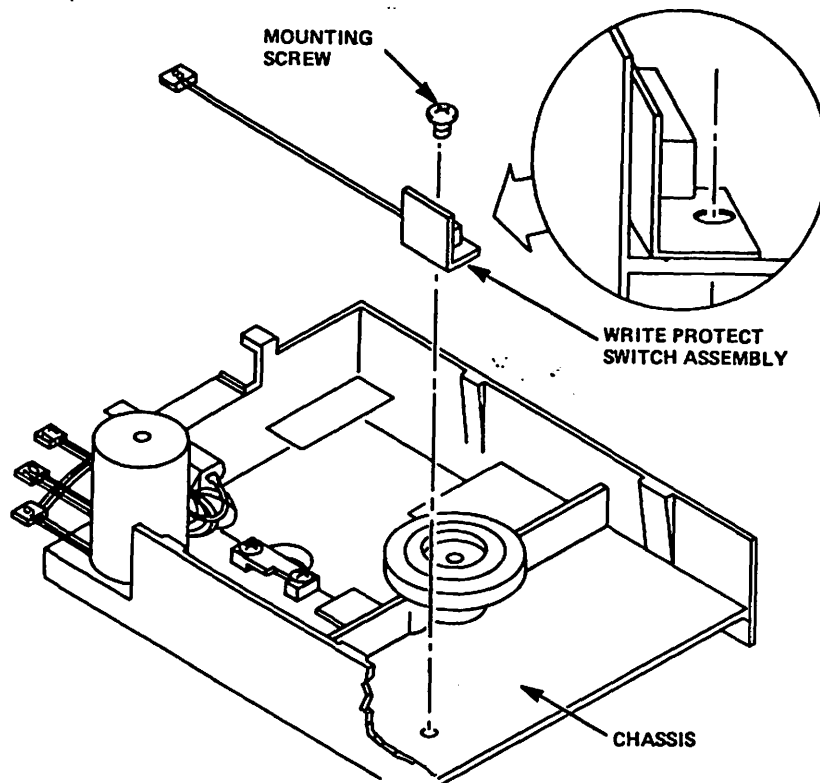
Write Protect Switch Assembly Mounting Screw and Connector P8

Figure 34

5-3

8. Using a Phillips screwdriver, mount the new Write Protect Switch Assembly with its mounting screw.

9. After smoothing out the Write Protect Switch Assembly cables and the Activity LED Assembly cables, harness them to the bottom of the chassis, routing the wires between the Drive Motor Assembly and the Track 00 Switch Assembly.

10. Harness the bundle of wires at the back of the disk drive, including the new Write Protect Switch Assembly cables in the bundle.

11. Reinstall the Drive.

12. Verify the output of the Write Protect Switch Assembly by inserting a diskette.

13. Reverify the output of the Write Protect Switch Assembly.

14. Adjust the Write Protect Switch if necessary.

15. Reinstall the Drive.

GUIDE RAIL

1. Remove the defective drive.

2. With needlenose pliers, remove the bushing from the front panel locating tab on the guide rail that is to be replaced.

3. With a Phillips screwdriver, remove the two (2) mounting screws located near the front of the disk drive, underneath the chassis. These two screws attach the front panel to the chassis.

4. Pull up the front panel slightly from the guide rail that is to be replaced.

** NOTE **

If the right-hand guide rail is to be replaced, detach the head cables from the two (2) posts.
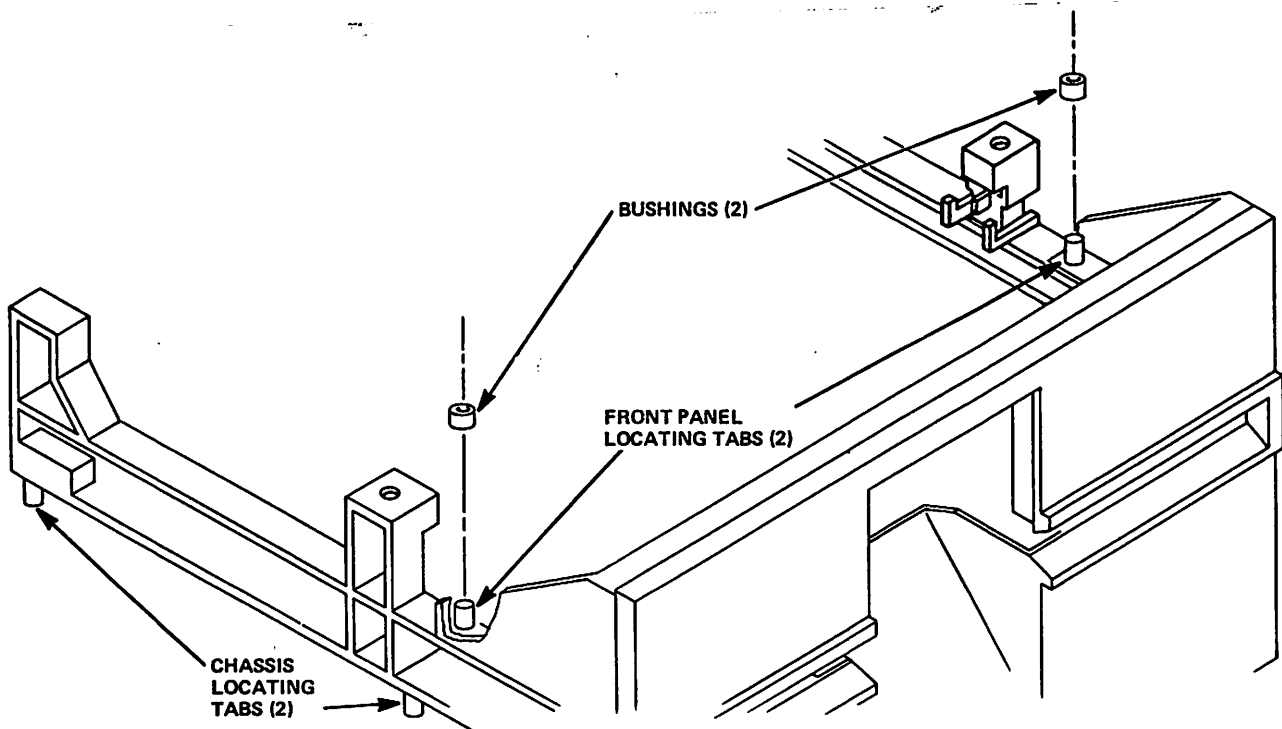
Front Panel Bushings, and Locating Tabs

Figure 35

5. With a flat blade screwdriver inserted between the guide rail and the chassis, pry up, from both of its ends, the guide rail that is to be replaced, and remove it.

6. If one of the two (2) chassis locating tabs, located underneath the guide rail that has been removed, has broken off inside the chassis, clean out the hole completely, using a one-eighth (1/8) inch drill or soldering iron to melt the plastic, then remove the debris.

** NOTE **

Take care not to enlarge the hole in the chassis.

7. Press in the new guide rail evenly.

8. Push down on the front panel until it is back in place.

9. After turning the disk drive upside down, reinstall the two (2) mounting screws located near the front of the chassis with a Phillips screwdriver.

10. After turning the disk drive right-side up, put the bushing over the front panel locating tab.

11. Put a small drop of glue (Permabond, Superglue, or other cyanoacrylic adhesive) on the top of the front panel locating tab.

12. If the left-hand guide rail has been replaced, verify the Write Protect Switch and its adjustment.
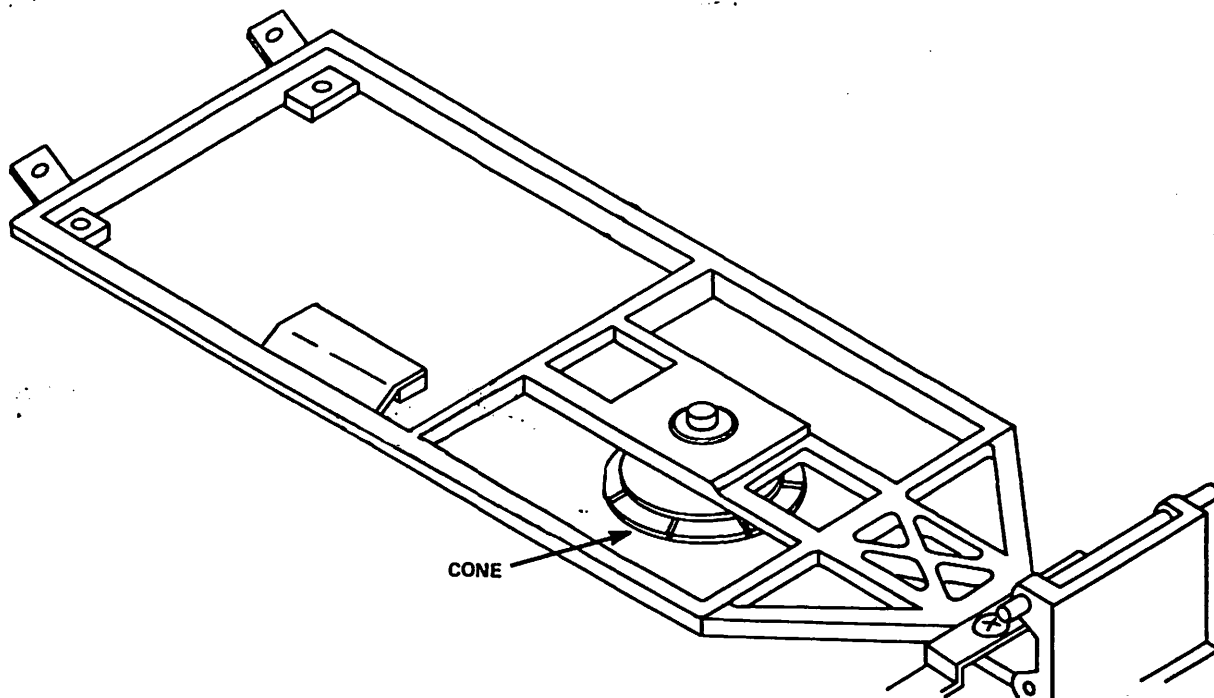
13. Reinstall the drive.

CONE LEVER ASSEMBLY

1. Remove the defective disk drive.

2. Open the front door, located in the front panel of the disk drive.

3. Cut the tie wrap from the Head Assembly.

CONE

Cone Lever Assembly Harnessing and Mounting

Figure 36

4. With a Phillips screwdriver, remove the (2) mounting screws that attach the Cone Lever Assembly to the chassis.

5. Gently slide the head carriage to the front of the disk drive.

6. Slide the Cone Lever Assembly rearward to release the upper arm finger.

7. Remove the Cone Lever Assembly by lifting it up and toward the rear of the disk drive, and sliding the front door out of its tracks.

8. Holding the new Cone Lever Assembly, put the front door into its tracks, and move it as far as it will go toward the front of the disk drive. Then, carefully lower the cone lever, lifting the upper arm finger over the cone lever.

9. With a Phillips screwdriver, install but do not tighten the two (2) mounting screws that attach the rear of the Cone Lever Assembly to the chassis.
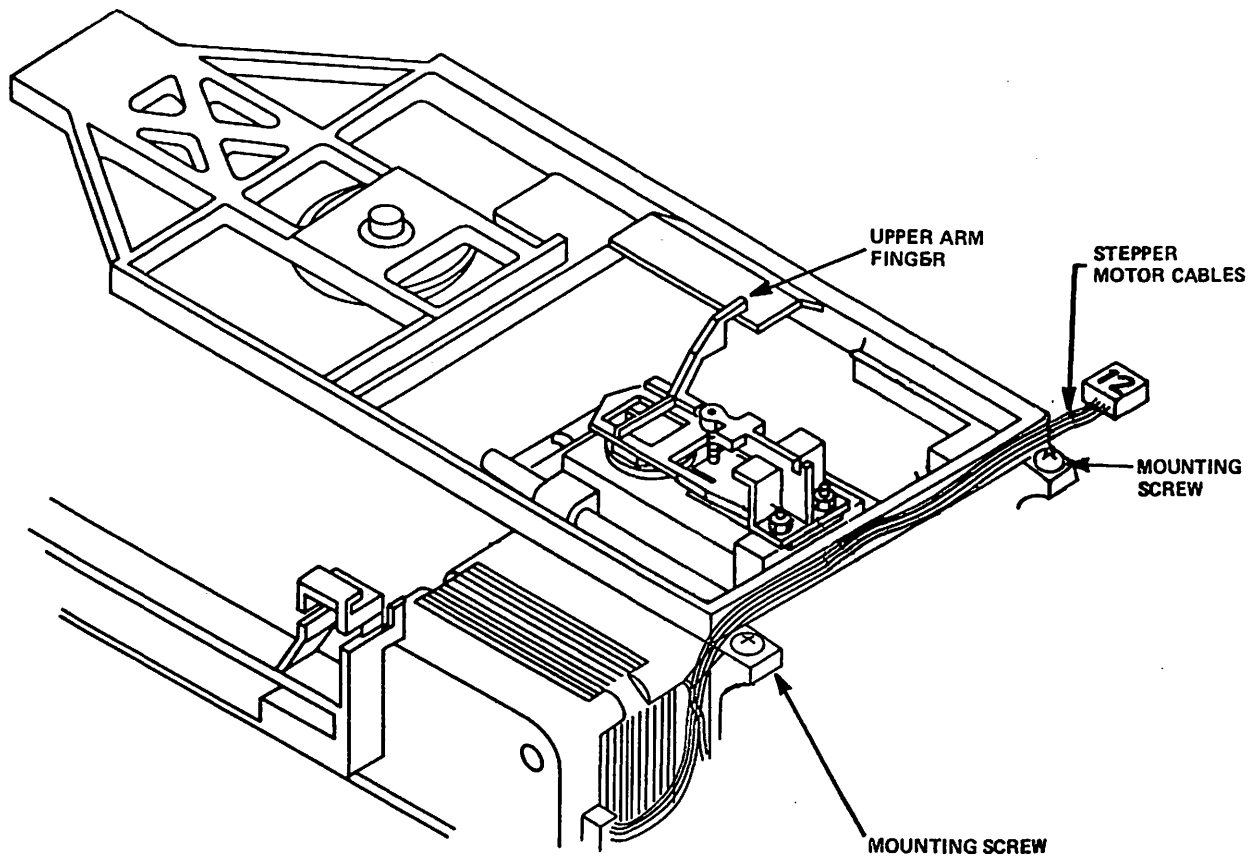
Cone Lever Assembly Harnessing, Mounting, and Stepper Motor Cables

Figure 37

10. Rewrap the Head Cable.

11. Close the front door of the disk drive to engage the cone and the hub.

12. Ensure that the cone is centered in the lever (shaft) hole.

13. With a Phillips screwdriver, tighten the two (2) mounting screws that attach the Cone Lever Assembly to the chassis.

CONE LEVER ASSEMBLY
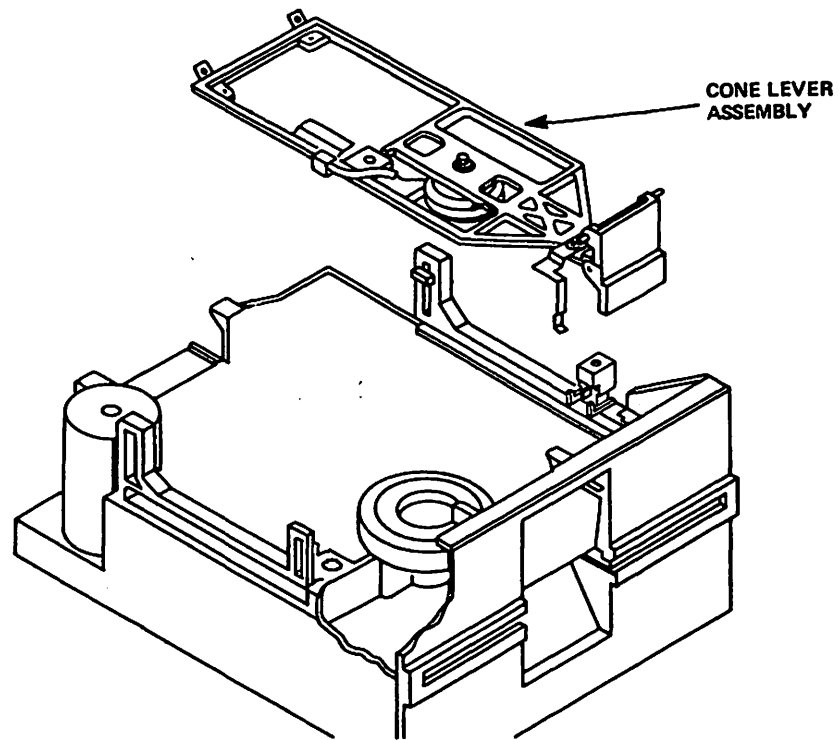
Cone Lever Assembly Cable Harness

Figure 38

14. Check to ensure there is a 0.010" + or - 0.001" clearance between the E-ring and the washer when the cone is clamped; the result of the front door being closed.

15. If necessary, adjust the clearance by adding or deleting a washer located under the E-ring.

16. Reinstall the Drive.
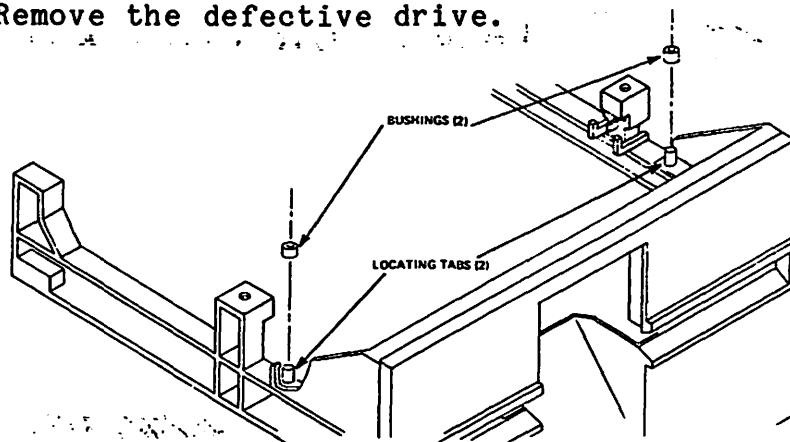
MOUNTING
SCREWS (2)

DEPRESS THE CONE
LEVER ASSEMBLY INTO
THE LATCHED POSITION.

LIFT
FINGER
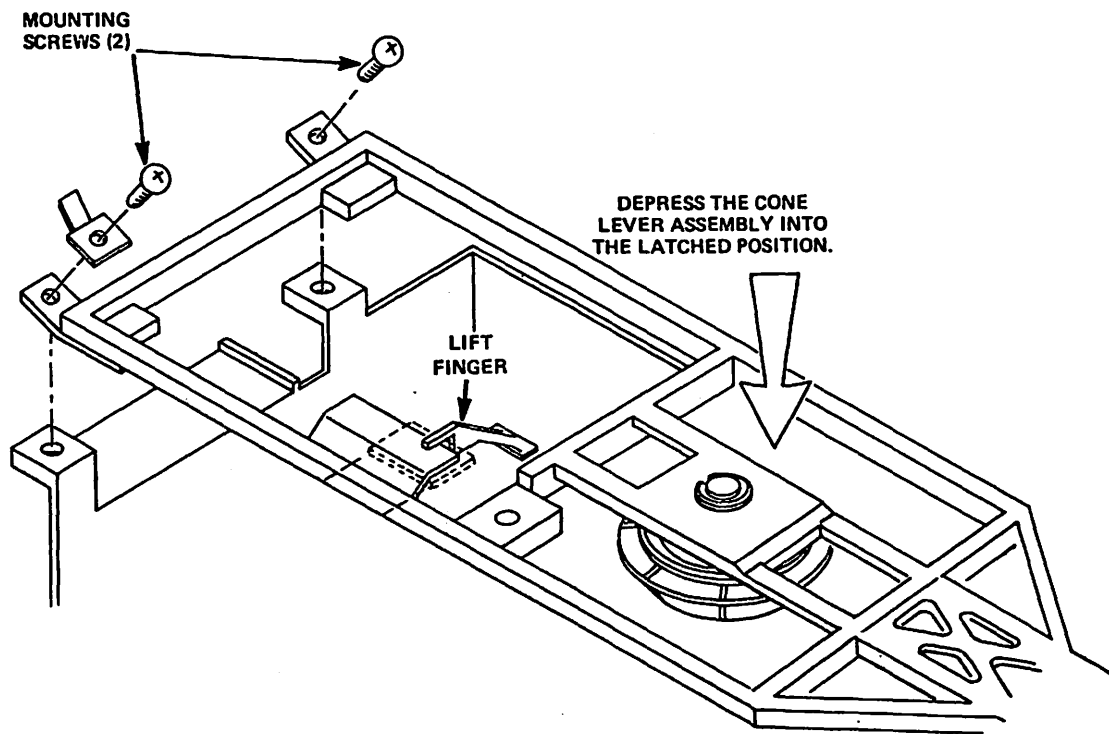
Cone Shaft and E-Ring

Figure 39

FRONT PANEL

1. Remove the defective drive.

BUSHINGS (2)

LOCATING TABS (2)

Front Panel Bushings

Figure 40

5-10

2. Using a pair of needle nose pliers, remove the two(2) bushings located on the right hand and the left hand top sides of the front panel by pulling up on them while using a twisting motion.

3. Remove the retaining collar that attaches the Activity LED Assembly to the front panel by taking a pair of needle nose pliers and gently pulling the retaining collar away from the front panel.

** NOTE **

Slide the retaining collar over the Activity LED assembly.

4. Snap out the Activity LED Assembly from its grommet.

5. With a Phillips screwdriver, remove the two (2) mounting screws that attach the front panel to the chassis.

** NOTE **

These two mounting screws are located underneath the front end of the disk drive.

6. Lift up the front panel, and remove it from the chassis.

Activity LED Assembly Retaining Collar and Grommet
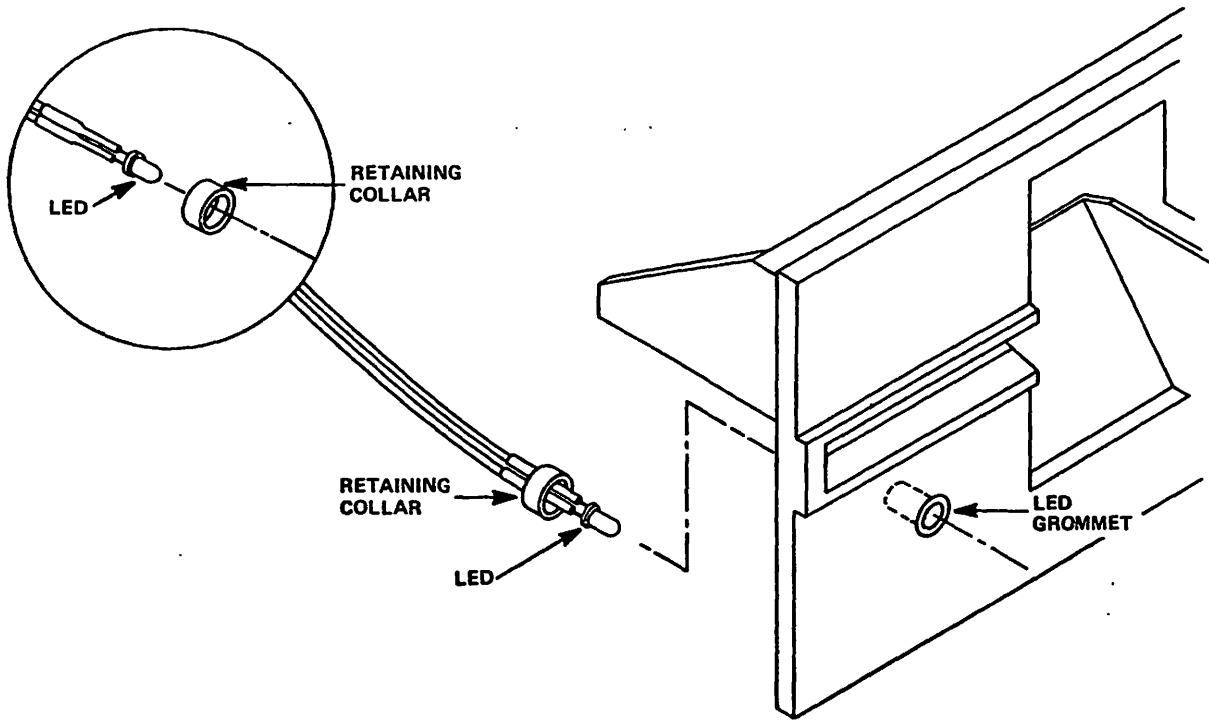
Front Panel Mounting Screws

7. Taking the new front panel, place the front door in its tracks on the front panel, and place the new front panel on the rail pins.

8. After upending the disk drive, using a Phillips screwdriver, reinstall the two (2) mounting screws that attach the front panel to the chassis.

9. Push the Activity LED Assembly into its grommet.

** NOTE **

The Activity LED Assembly usually makes a clicking noise when it is firmly pushed into the LED grommet.

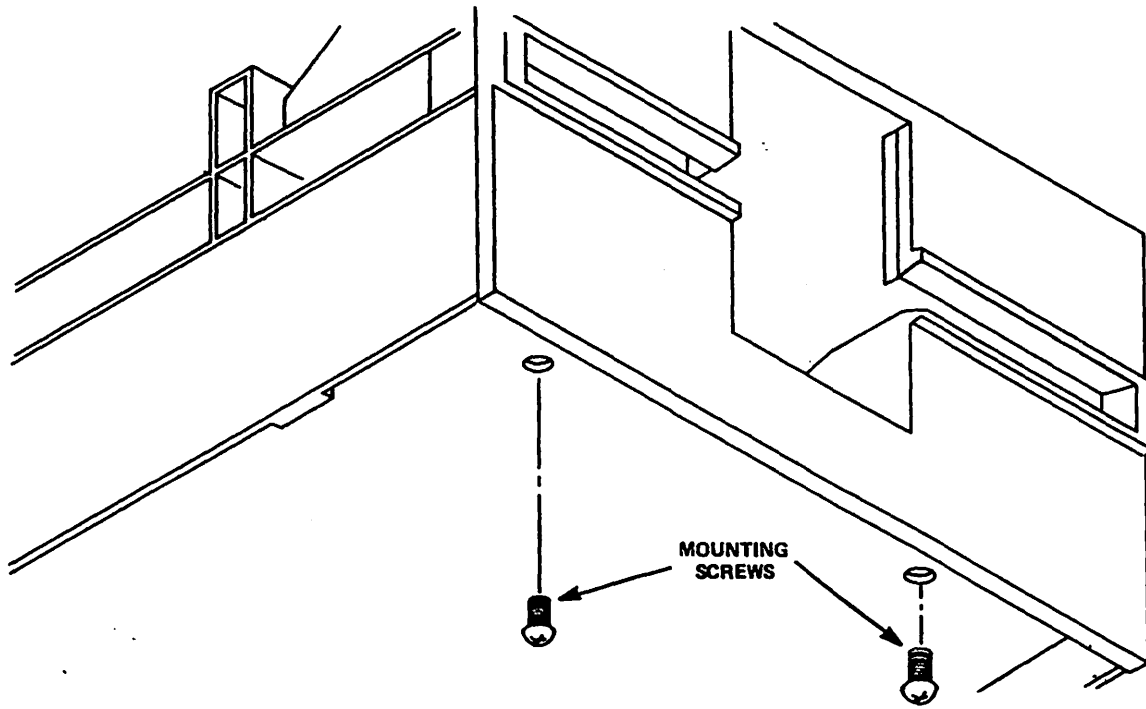Activity LED Assembly Retaining Collar and Grommet

Figure 41

Figure 42

Front Panel Mounting Screws

5-12

10. Push the Activity LED Assembly retaining collar over the back of the LED grommet.

11. Install two (2) new bushings on the right hand and left hand sides of the front panel.

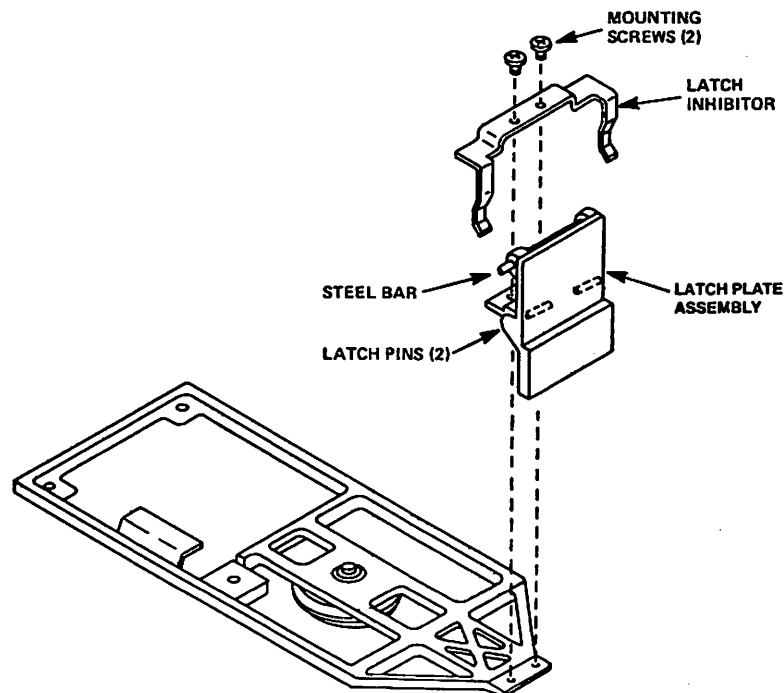12. Put a small drop of glue (Permabond, Superglue, or other cyanoacrylic adhesive) on the top of each bushing.

13. Reinstall the drive.

LATCH PLATE ASSEMBLY

1. Remove the defective drive.

2. With a Phillips screwdriver, loosen the two (2) mounting screws that attach the Latch Plate Assembly to the cone Lever Assembly.

Latch Plate Assembly Mounting Screws and Latch Inhibitor

Figure 43

3. Remove the two (2) mounting screws from the Latch Plate Assembly.

4. Remove the latch inhibitor and the Latch Plate Assembly from the disk drive.

5. While holding the Cone Lever Assembly down, insert the new Latch Plate Assembly into its tracks.

6. Close the front door of the disk drive.

7. Still holding the Cone Lever Assembly down, place the latch inhibitor on the top of the Latch Plate Asssembly.

8. With a Phillips screwdriver, install but do not tighten the two(2) mounting screws that attach the latch inhibitor and the Latch Plate assembly to the Cone Lever Assembly .

9. Open the front door located in the front panel.

10. Insert a diskette into the disk drive.

11. Close the front door.

12. Adjusting the latch inhibitor, align it so that it just touches the diskette as the front door is closed.

13. While holding the latch inhibitor in place, tighten the two (2) mounting screws with a Phillips screwdriver.

14. Reinstall the drive.

CONE KIT

1. Remove the Cone Assembly.

2. Remove the E-ring that holds the cone shaft on.

** NOTE **

The cone's Parts are now loose from the Cone Lever.
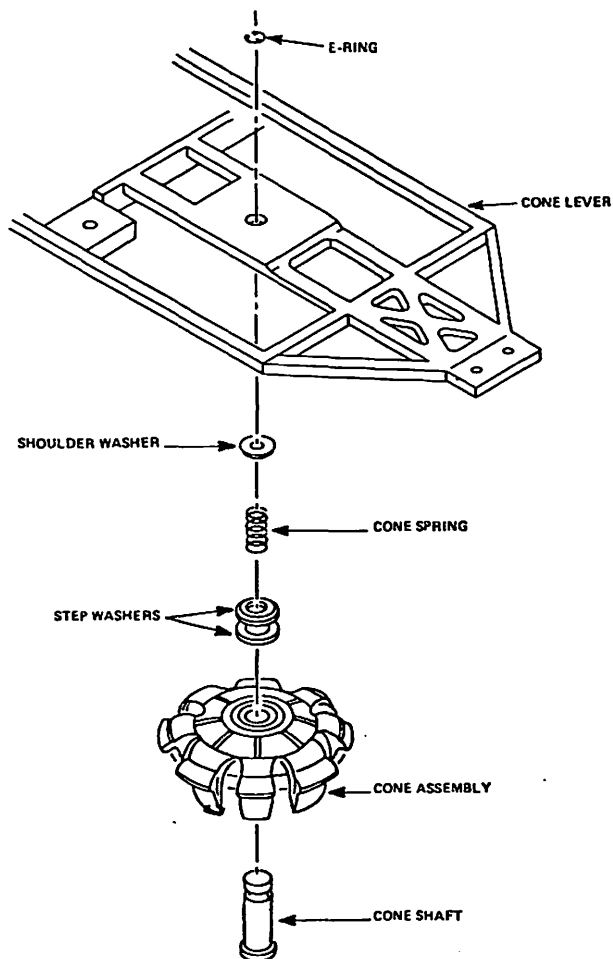
Cone's Component Parts

Figure 44

3. Put the Cone Shaft through the cone.

4. Slip on the step washer, the cone spring, and the shoulder washer.

5. Compress the spring, and put the cone shaft through the hole in the Cone Lever Assembly.

6. Install the E-ring in order to retain the Cone Lever Assembly.

7. Reinstall the Cone Lever Assembly.

DRIVE BELT

1. Remove the old drive belt from the pulleys.
See figure below

Drive Belt and Pulleys

Figure 45

2. Taking care not to stretch the new drive belt,
install it with the dark, shiny side facing the pulleys.

** NOTE **

Put the drive belt on the small pulley first, then on
the large one.

DRIVE MOTOR ASSEMBLY

1. After turning the disk drive upside down, remove the drive belt.

2. With a Phillips screwdriver, remove the two (2)
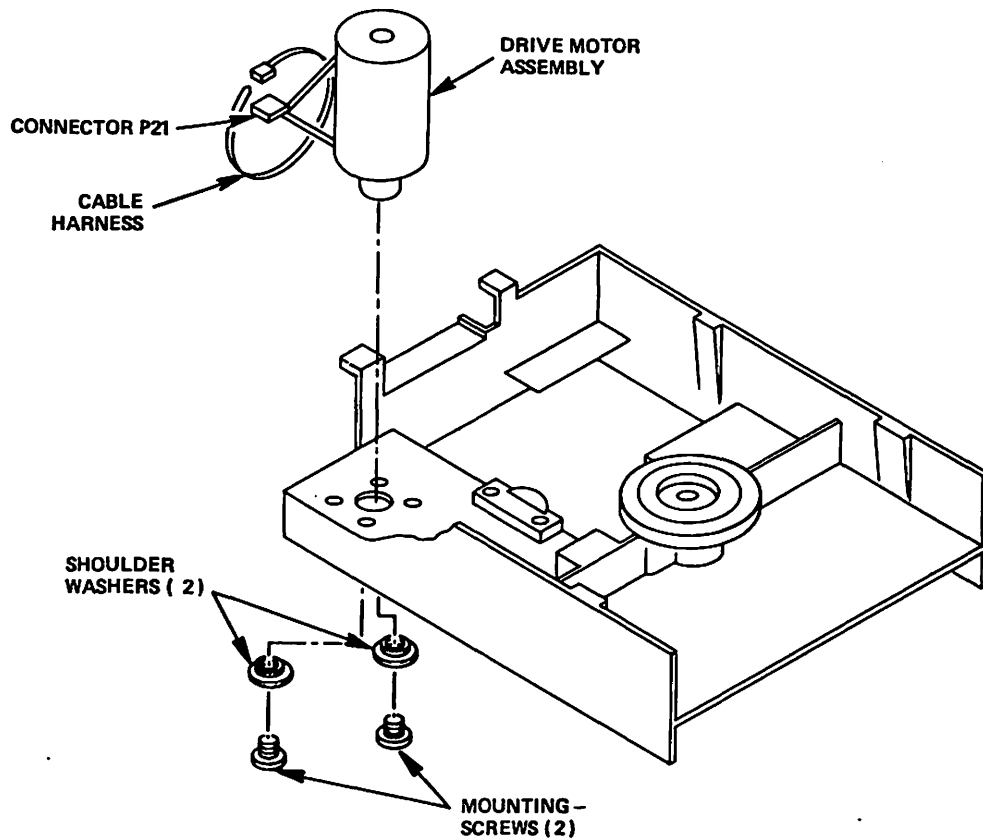
Drive Motor Assembly Harnessing and Mounting

Figure 46

mounting screws and the two (2) Shoulder washers that attach the drive motor assembly to the chassis.

** NOTE **

Save the mounting screws and the shoulder washers.

3. Remove the Drive Motor Assembly from the chassis.

4. Insert the pulley of the new drive motor assembly through the bottom of the chassis.

5. Rotate the Drive Motor Assembly until its two tapped holes are aligned with the two holes in the chassis.

6. With a Phillips screwdriver, mount the drive motor assembly to the chassis, using the two mounting screws and the two shoulder washers previously set aside.

7. Reinstall the Drive Belt.

8. Reinstall the drive in unit and reconnect all connectors.

TRACK 00 SENSOR ASSEMBLY

1. With a flat blade screwdriver, remove the E-ring from the Track 00 Sensor Assembly's adjustment screw located on the inside of the disk drive between the switch and its bracket (see figure 47)
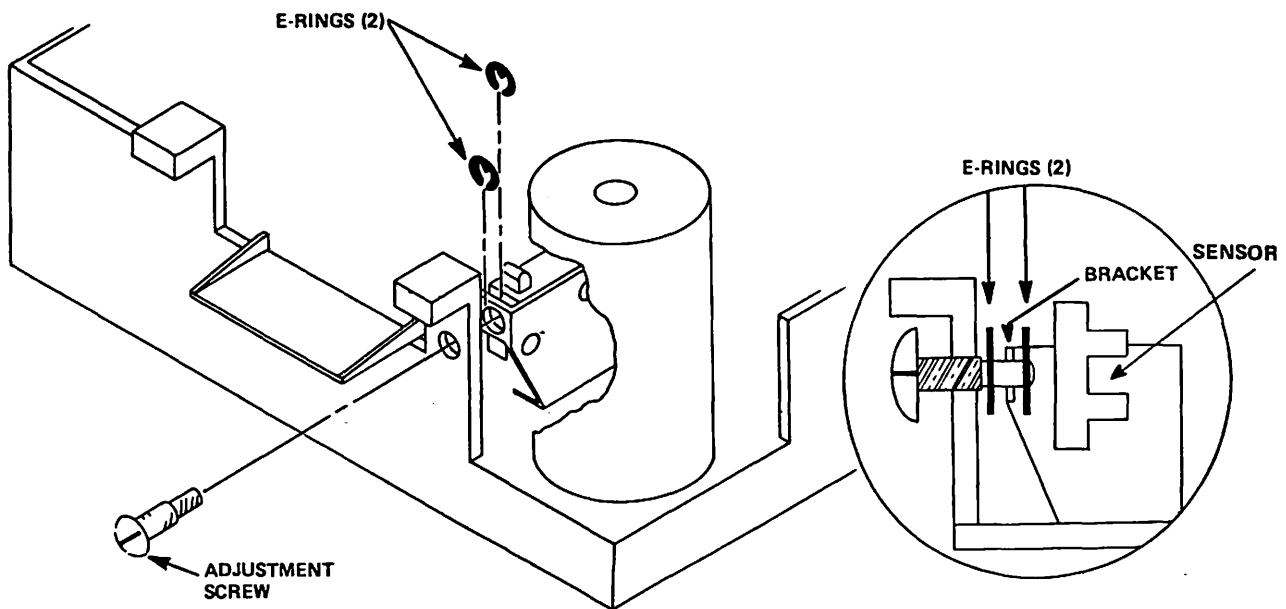
Track 00 Sensor Assembly E-Rings and Adjustment Screw

Figure 47

2. Move the head carriage toward the front of the disk drive, i.e. away from the Track 00 Sensor assembly.

3. With a Phillips screwdriver, remove the mounting screw that attaches the Track 00 Sensor Assembly to the chassis. (see figure 48).

4. Remove the Track 00 sensor assembly by pulling it toward the front of the disk drive.

5. Put the new Track 00 Sensor assembly into the disk drive near the left hand rear of the chassis.

6. Push the new Track 00 Sensor Assembly toward the rear of the disk drive until its mounting hole is aligned with the mounting hole in the chassis.
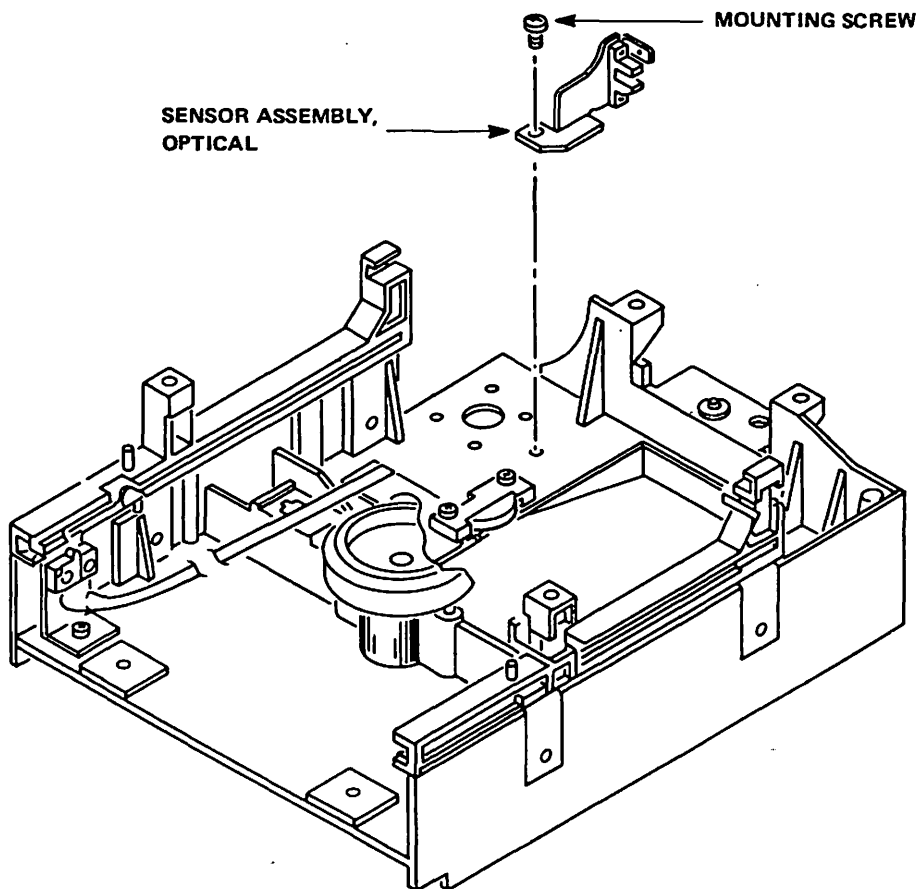
Track 00 Sensor Assembly and Mounting Screw

Figure 48

5-19

7. Make sure there are no cables underneath the Track 00 Sensor Assembly.

8. With a Phillips screwdriver, install and tighten the mounting screw that attaches the Track 00 Sensor aassembly to the bottom of the chassis (see figure 48).

9. Reinstall the E-ring with an E-ring insertion tool.

10. To adjust the Track 00 Sensor Assembly, loosen the mounting screw, and move the switch in or out by turning the adjustment screw.

11. The drive can be adjusted for track 00 by inserting the drive in the B position. Enter the Format program, select B and hit the space bar. When the drive homes the B head assembly hit ALT C to stop the program. The head is now positioned at track 00. Monitor the ouptut of 1E PIN 10 with an oscilloscope. It will be between 2.5 and 5 volts when the track 00 is sensed. Moving the head away from track 00 will cause the output to drop to 0.

APPENDIX A

MEMORY MAPPED I/O ADDRESS ASSIGNMENTS

I/O DEVICE		MEMORY ADDRESSES
8259	PIC	E0000-E0001
8253	TIMER	E0020-E0023
7201	SERIAL PORT CONTROLLER	E0040-E0043
46505	CRT CONTROLLER	E8000-E8001
6522	PARALLEL PORT	E8020-E802F
6522	KEYBOARD	E8040-E804F
6852	SSDA	E8060-E806F
6522	USER PORT	E8080-E808F
6522	DISK DRIVE CONTROLLER	E80A0-E80AF
6522	DISK DRIVE CONTROLLER	E80C0-E80CF
6522	DISK DRIVE CONTROLLER	E80E0-E80EF

VICTOR 9000 PHYSICAL MEMORY MAP

Spec. No. 8014

0:0

0-2000
128K
Dynamic RAM

2000:0

2000-E000
768K
Memory Expansion Space

E000:0 — PIC 8259
E002:0 — Timer 8253
E004:0 — USART 7201
E006:0 — Not Used Intel I/O
E008:0
E00A:0 — PIC ─┐
E00C:0 — TIMER │ These 4 devices can be addressed through-
E00E:0 — USART │ out this space since
       — NC ──┘ A4-A14 are not decoded

E000 - E800
32K
Intel Devices

32 Addresses
per device
4 Devices

E7FC:0 — TIMER
E7FE:0 — USART
E800:0 — NC
E802:0 — CRT CNTRL 46505
E804:0 — Centronics/488 6522
E806:0 — Keyboard 6522
E808:0 — Codec 6852
E80A:0 — User Port 6522
E80C:0 — Disk Motors 6522
E80E:0 — Head Select etc. 6522
E810:0 — Disk Data 6522

E800 - F000
32 K
Phase 2 Devices

Additional Phase 2
Drive Devices
Bus Signals
CSEN, IRQ, XACK, Phase 2, etc.
support these

E83E:0
E840:0 — 46505 (again)

32 Addresses
per device
32 Devices

E8FE:0
F000:0

F000-F100
4K
Screen Ram
First Image
A12-A14 Not Decoded

F000 - F8000
32 K
Screen Ram

F100:0 — Second

4K Used

F800:0 — Second Image of Rom

F800 - FFFF:F
32K
ROM/PROM

FC00:0 — 2732 Mode Not conn. — 2364 Mode 5H

FD00:0

FE00:0

FF00:0 — 5H — 7H

FFFF:F — 7H

16 or 8K used

SECTION SIX ... PARTS CATALOG AND SYSTEM SCHEMATICS