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PDP-10 INTERFACE MANUAL

PDP-10

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PDP-10 INTERFACE MANUAL
DEC-10-HIFB-D
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CHAPTER 1
INTRODUCTION

This manual presents implementation guidelines and requirements for the PDP-10 I/O bus, memory bus, and data channel bus. Specifications for the FLIP CHIP modules recommended for these interfaces are included with examples of interfaces and a description of the GP10 General Purpose I/O Interface.

Also included is information for interfacing user terminals (Teletypes, alphanumeric displays, etc.) to the PDP-10 system.

Details are supplied throughout to enable the engineer or experimenter to construct even a large peripheral unit with a minimum of difficulty.

REFERENCE MATERIAL

This manual complements other DIGITAL publications of particular interest to the interface designer. Some of these manuals are listed below.

DIGITAL Logic Handbook (C-105)
DIGITAL Industrial Handbook (C-110)
PDP-10 System Reference Manual (DEC-10-HGAA-D)
PDP-10 Maintenance Manual Vol. III (Special Modules) (DEC-10-I6CA-D)
PDP-10 Installation Manual

The DIGITAL Logic Handbook and the DIGITAL Industrial Handbook provide complete specifications of DIGITAL's line of FLIP CHIP logic modules with basic instruction in digital logic usage and general reference material.

The PDP-10 System Reference Manual describes the PDP-10 instruction set and hardware organization and contains descriptions of the I/O instructions and memory organization. Also included in the System Reference Manual are descriptions of all standard PDP-10 I/O devices.

The PDP-10 Maintenance Manual Volume III is primarily intended for use by maintenance personnel but is also useful to designers of large or high-speed peripheral devices which require the use of B-, G-, R-, H-, and W-series modules not described in this manual.

SYMBOLS

DIGITAL often uses logic symbols and design conventions which are unfamiliar to many designers. A brief explanation of DIGITAL's logic conventions is provided in Chapter 3 with a comparison with MIL-STD-806B symbology.

CHAPTER 2
PDP-10 I/O BUS DESCRIPTION

The PDP-10 I/O Bus is a set of cables which connects all PDP-10 I/O devices to the central processor. Both data and control information flow through the bus. Rules for designing peripheral equipment, helpful suggestions, and a design example are given below.

The following description of the PDP-10 I/O Bus has sufficient detail to enable a user to design an interface between the PDP-10 I/O Bus and special peripheral hardware. Loading and interfacing rules are specified in terms of DIGITAL FLIP CHIP modules which may be used to implement an interface.

COMPATIBILITY

The PDP-10 I/O Bus is compatible with the PDP-6 I/O Bus and PDP-10 devices can be used with a PDP-6 or vice versa. The PDP-10 I/O Bus includes control lines for the hardware read-in feature of the PDP-10 which is not available on the PDP-6. The -15 V turn-on feature of the PDP-6 is available in the PDP-10 Margin Check Bus System and is not included in the PDP-10 I/O Bus.

GENERAL DESCRIPTION

PDP-10 I/O Bus Information Flow

The PDP-10 I/O Bus is a cable system which connects all I/O device interfaces in parallel. Due to the high-speed signals involved, the parallel connection is implemented as a transmission line with one end at the central processor. The bus is chained through each successive I/O device in no particular order. Figure 2-1 shows the information flow in the I/O bus. References to the DATAO instruction include by implication the appropriate functions of the BLKO instruction. Similarly, references to DATAI include BLKI, and references to CONI include CONSO and CONSZ. The 36 data lines (IOB 0 through IOB 35) carry data to or from the device during DATAI and DATAO instructions. The same 36 data lines carry control to and status from the device control during CONO and CONI instructions.

Device Selection

All PDP-10 I/O devices share the I/O bus; therefore, part of the information carried by the bus indicates which device is to respond. The device-number portion of a PDP-10 input or output instruction is a 7-bit field but, for convenience in decoding, a pair of complementary signals for each bit appear

on the I/O bus as IOS 3 (1), IOS 3 (0) through IOS 9 (1), IOS 9 (0). These 14 levels must be decoded in each device so that only one device at a time responds to the command signals and data on the bus. A physical device may use more than one device number if a large amount of control or status information must be carried to or from the PDP-10. The decoded IOS signals should not be used to cause any action by themselves. These signals are derived directly from the instruction register of the PDP-10. During a non-I/O instruction, a device may be selected due to the bit configuration of the instruction register, but no I/O command signals are given by the PDP-10. The IOS signals are DIGITAL standard levels, -3 V when asserted and ground when not asserted.

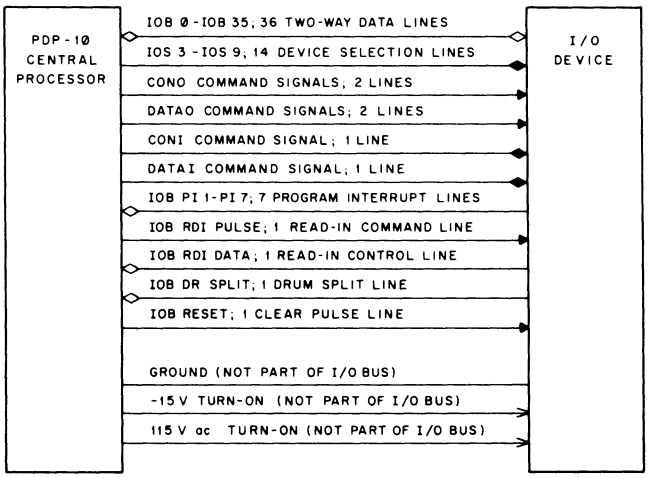


Figure 2-1 I/O Bus Information Flow

Data Lines

All data transmitted between an I/O device and the central processor in either direction is carried by the 36 data lines. These lines serve a quadruple function: (1) They carry control information from the computer to the device. (2) They carry data from input devices to the computer. (3) They carry status information from the device to the computer. (4) They carry data from the computer to output devices. Because of the two-way nature of these lines, the interface design must conform to the specifications that follow. Failure to conform to the specifications may result in overloading or mismatching of the lines, either of which will make the operation of all devices connected to the I/O bus unreliable.

I/O Command Signals

For each of the four functions of the data lines there is a corresponding command signal or pair of command signals If the function of the data lines is to transmit control information from the computer to the device (CONO), a pair of command pulses is issued. The first pulse prepares the device to receive control information and the second pulse commands the device to read the control information off of the data lines into the device's control register. Similarly, another pair of command pulses is issued when the function is to transmit data from the computer to the device (DATAO). If the function is to send status information from the device to the computer (CONI), a level is provided which determines when and for how long the device places its status on the data lines. Another level is issued if the function is to transmit data from the device to the computer (DATAI). This level determines when and for how long the device places its data on the data lines.

Priority Interrupt Requests

Part of the control information normally sent from the computer to a device is a 3-bit interrupt channel number. The device must store and decode this number so that, when the conditions for initiating an interrupt request are met in an I/O device, the device can apply a signal to the PI request line designated by the computer. If the channel number previously supplied by the computer is zero, no interrupt request should be transmitted. If a non-zero channel number has been supplied by the computer, an interrupt request should be transmitted on the designated line when the interrupt request condition in the I/O device occurs. (See the PDP-10 System Reference Manual for details of the computer's interrupt system operation and appropriate programming.)

Read-In Signals

The read-in feature on the PDP-10 consists of hardware in the central processor and in each I/O device designed to operate in the read-in mode. The operator first sets switches on the processor to the device number to be used for reading in the bootstrap program. When the operator presses the READ-IN Switch, the processor sends an I/O bus reset pulse to initialize all I/O devices, followed by the IOB RDI pulse with the IOS lines set according to the number placed in the manual switches. The IOB RDI pulse must initiate the read-in action that is appropriate for the particular device (e.g., a DEC-tape control would select DTA0, backspace into the end zone, and then proceed to read data starting in block 0). When the read-in device has a word of data ready for the central processor, it signals the

computer with the IOB RDI DATA level. This signal causes the computer to execute the instruction in the instruction register which for the first word read in is DATAI DEV, 0 and for succeeding words read in is BLKI DEV, 0 which reads data in according to the pointer read in as the first word. The data read in must have the format shown in Figure 2-2.

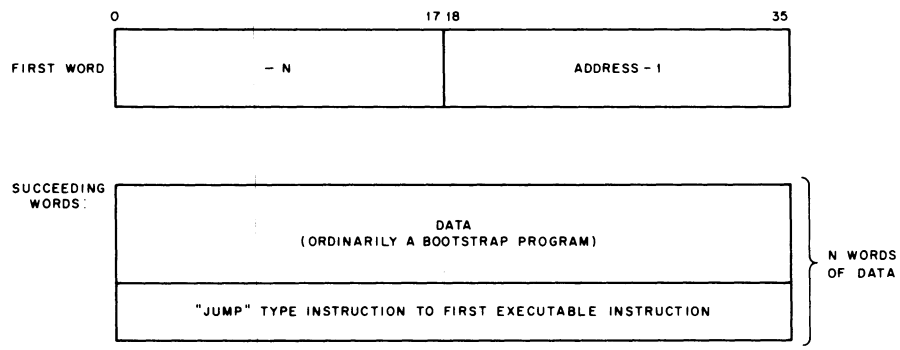


Figure 2-2 Read-In Mode Data Format

The data will be read into the memory starting at location ADDRESS. The last data word is executed as if by an XCT instruction. The read-in device must supply full-word data (36 bits) to the computer.

Miscellaneous Signals

The IOB RESET pulse is a signal which should be used to clear all peripheral device control registers so that the device is in a "null" state in which it will accept any normal sequence of commands. It must stop physical motion. It specifically should clear any conditions which cause interrupts. No device may request an interrupt following an IOB RESET without being given an I/O instruction directed to it. The central processor sends the IOB RESET pulse under four conditions:

1. Power was just turned on (a series of pulses is actually generated in this case).
2. The processor console's READ-IN button is pushed.
3. The processor console's RESET button is pushed (to clear the I/O system before restarting a program, for example).
4. The program executes a CONO to the arithmetic processor (Device 0 Mnemonic APR) with bit 19 a 1.

A DR SPLIT signal line is provided in the I/O bus to allow a high-speed direct memory accesing device to inhibit the central processor from requesting memory read-modify-write cycles in order to minimize memory tie-ups.

A Remote Turn-On signal is present in the margin check cable when the central processor has power applied. This signal or its ac equivalent which is supplied through a separate remote-on cable should be used to turn on the power supplies in each I/O device. A ground connection (in addition to the safety wire in the power cord) should be provided between the central processor and each I/O device. This connection should be through #4 gage copper wire or equivalent and may be chained through other I/O devices. (See Chapter 10 of this manual or the PDP-10 Installation Manual for further details.)

Programming Considerations

The designer should give consideration to the programming aspects of the design of special-purpose peripheral devices for the PDP-10. By designing with the PDP-10's instruction set in mind, an efficient hardware-software interaction can be accomplished, thus reducing programming effort and increasing program running speed. For example, to use the BLKO or BLKI instructions it is usually necessary to provide separate DONE (data) and ERROR PI channels (decoders) in a device.

INTERFACE SPECIFICATIONS

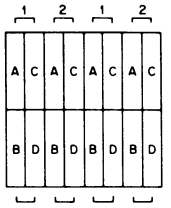
Cables

The I/O bus physically consists of two coaxial cable sets which terminate in two W851 FLIP CHIP Connector Assemblies. (W850's may be used after evaluation.) These connectors fit into a single, augmented FLIP CHIP connector block (H801 with an H003 or H004 retaining block). All I/O bus interfaces must have two sets of I/O bus connectors: one set to receive the incoming cables from the central processor or previous I/O device and the other set to plug-in outgoing cables for the next device on the I/O bus. On all 16 FLIP CHIP positions occupied by the I/O bus cables, pins C, F, J, L, N, R, and U must be grounded. The normal power connection to pin B (-15 V) must be made for all 16 positions; power connections to pin A (+10 V) are optional and do not affect the operation of the I/O bus. Even though some I/O bus signals may not be used by a particular I/O device, all signals (including spares) must be strapped across from the input connector positions to the output connector positions in order to feed all signals to each subsequent device. See Chapter 4 for further cable information. No terminating resistors are required at the end of the I/O bus. Table 2-1 shows the pin assignments for the I/O cable system and the wiring-side layout of a typical I/O bus cable connection plan. Various cable adapters are available for connecting PDP-6 I/O equipment to PDP-10 systems. The pin assignments for these adapters are also shown in Table 2-1. (PDP-6 I/O bus details are available in DEC permanent memo M-1174.)

Table 2-1
PDP-10 I/O Bus Signals

PDP-6 PIN	PIN	I/O BUS CABLE #1				I/O BUS CABLE #2			
(B)	D	IOB 0		IOB 18		IOB RESET	→	DATAO CLEAR	→
(C)	E	IOB 1		IOB 19		RESERVED		DATAO SET	→
(D)	H	IOB 2		IOB 20		SPARE		CONO CLEAR	→
(E)	K	IOB 3		IOB 21		IOB DR SPLIT	◇—	CONO SET	→
(F)	M	IOB 4		IOB 22		IOS 3 (1)	→	IOB DATAI	→
(H)	P	IOB 5		IOB 23		IOS 3 (0)	→	IOB CONI	→
(K)	S	IOB 6		IOB 24		IOS 4 (1)	→	IOB RDI PULSE	→
(L)	T	IOB 7		IOB 25		IOS 4 (0)	→	IOB RDI DATA	◇—
(M)	V	IOB 8		IOB 26		IOS 5 (1)	→	SPARE	
		A ↑	B ↓	C ↑	D ↓	A ↑	B ↓	C ↑	D ↓
(N)	D	IOB 9		IOB 27		IOS 5 (0)	→	SPARE	
(P)	E	IOB 10		IOB 28		IOS 6 (1)	→	SPARE	
(R)	H	IOB 11		IOB 29		IOS 6 (0)	→	IOB PI 1	◇—
(T)	K	IOB 12		IOB 30		IOS 7 (1)	→	IOB PI 2	◇—
(U)	M	IOB 13		IOB 31		IOS 7 (0)	→	IOB PI 3	◇—
(V)	P	IOB 14		IOB 32		IOS 8 (1)	→	IOB PI 4	◇—
(W)	S	IOB 15		IOB 33		IOS 8 (0)	→	IOB PI 5	◇—
(X)	T	IOB 16		IOB 34		IOS 9 (1)	→	IOB PI 6	◇—
(Y)	V	IOB 17		IOB 35		IOS 9 (0)	→	IOB PI 7	◇—

ARRANGEMENT OF I/O BUS CONNECTORS



AS SEEN FROM WIRING SIDE

NOTE:
—◇ FROM PROCESSOR
◇— TO PROCESSOR
PINS:
C,F,J,L,N,R,U ARE GROUNDED
CABLES MUST BE LOCATED:
EACH SET (1 & 2) ON SINGLE FLIP CHIP BLOCK

DIGITAL FLIP CHIP Module types are specified for I/O bus interface requirements. However, a non-DIGITAL module having specifications within those of the specified module may be used if care is exercised. Module specifications are listed in the Module section of this manual (Chapter 4). A list of transmitting and receiving modules is given in Table 2-2.

Table 2-2
Transmitting and Receiving Modules

Signal	Transmitting Module Type	Receiving Module Type
IOB n (36)	B163, B141	W107
IOB RESET	-	R107
IOB DR SPLIT	B165	
IOS n (m) (14)	-	R111 + R001, R002
DATAO CLEAR	-	R111 Note 1; R107 Note 2

Note 1: Use when only one device number is used in a "box".

Note 2: Use when two or more device numbers are used in a "box".

Table 2-2 (Cont)
Transmitting and Receiving Modules

Signal	Transmitting Module Type	Receiving Module Type
DATAO SET	-	R111 Note 1; R107 Note 2
CONO CLEAR	-	R111 Note 1; R107 Note 2
CONO SET	-	R111 Note 1; R107 Note 2
IOB DATAI	-	R111 Note 1; R107 Note 2
IOB CONI	-	R111 Note 1; R107 Note 2
IOB RDI PULSE	-	R111
IOB RDI DATA	B133	-
IOB PI n (7)	B152 or B156	-

Note 1: Use when only one device number is used in a "box".

Note 2: Use when two or more device numbers are used in a "box".

Device Number Decoding

The I/O device number is transmitted from the processor as seven pairs of complementary signals: IOS 3 (0), IOS 3 (1) through IOS 9 (0), IOS 9 (1). By applying the proper 1 and 0 signals to a 7-input AND gate each device number may be decoded. This AND gate is required to be a 1 mA diode gate such as the R111 with R001 or R002 gate expanders. Use of this type of gate allows the use of all 123 available device numbers (5 numbers are used by the central processor). The device number signals are asserted at least 200 ns before IOT T0. (See timing chart, Figure 2-4.) No use should be made of the I/O bus control pulses or levels unless the device is selected. In general, device numbers from 000_8 to 374_8 are reserved for standard DIGITAL peripheral devices, device numbers from 400_8 to 774_8 are for use on DIGITAL special systems and for user built peripheral devices. Figure 2-3 shows the device number assignments for PDP-6/PDP-10 peripherals and the software mnemonics assigned.

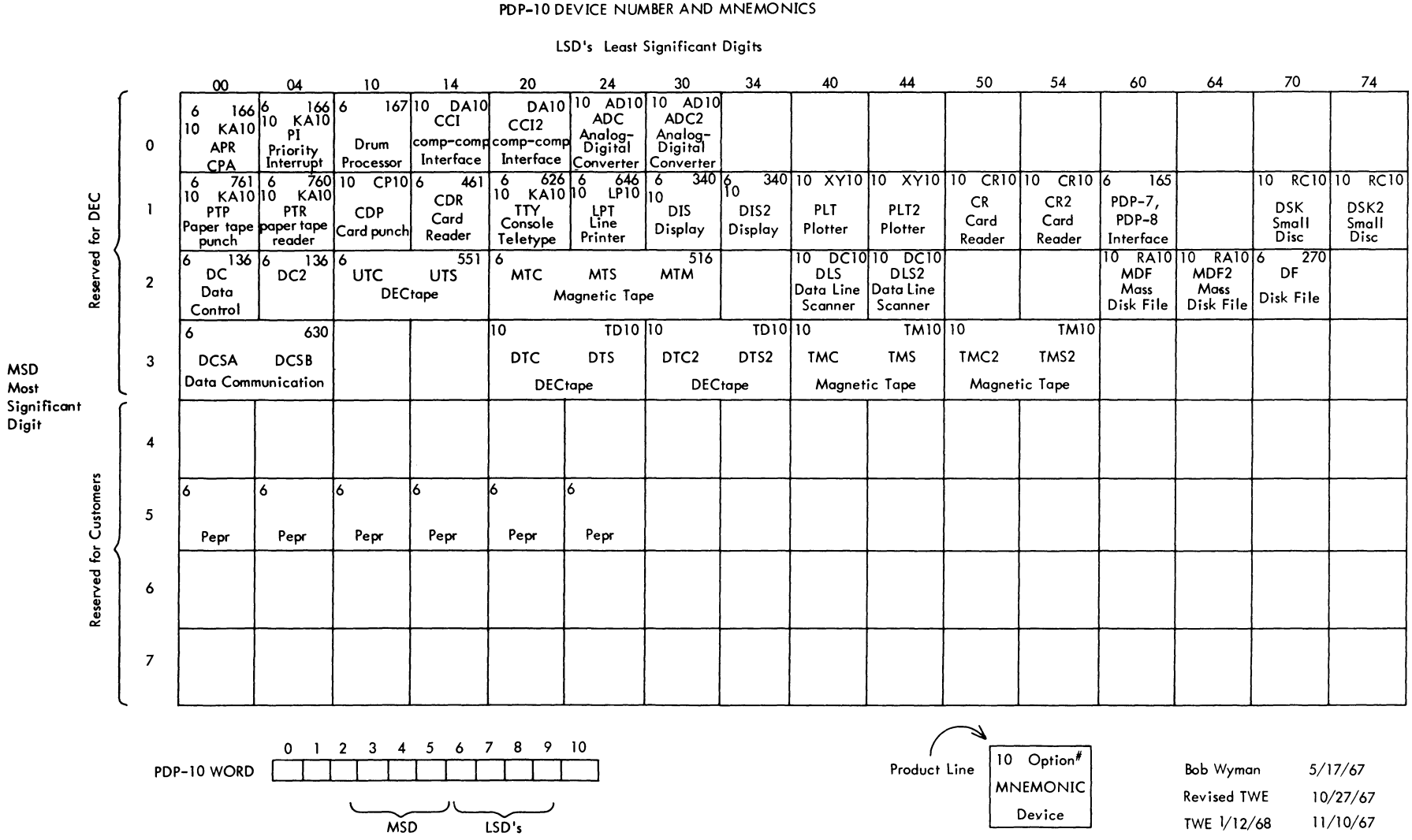


Figure 2-3 Device Number Assignments and Software Mnemonics, PDP-6/10 Peripherals

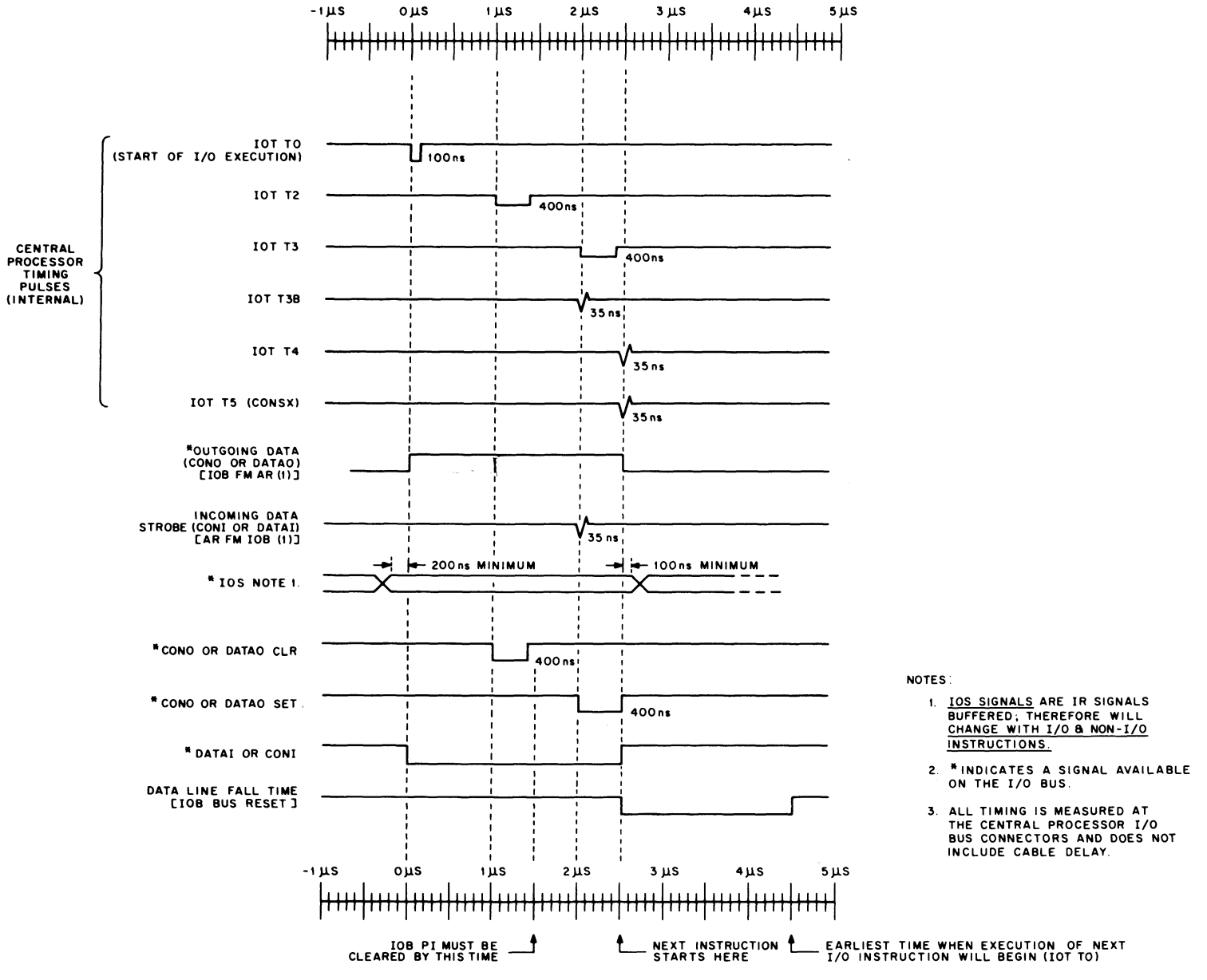


Figure 2-4 I/O Bus Timing

Control Pulses and Levels

For each device, there are four standard commands from the central processor: accept control information (CONO); send status information (CONI); accept data information (DATAO); and send data information (DATAI). These have direct mnemonics, namely, CONditions Out, CONditions In, DATA Out, and DATA In. The fifth command, enter read-in mode (RDI pulse), is explained later. All information is transmitted over the 36 data lines. When the command is to accept control information, two negative pulses are sent from the central processor, IOB CONO CLEAR and IOB CONO SET in sequence; the first pulse is usually used to clear the control register; the second pulse is usually used to sample the data lines into the control register. It is permissible to sample data with the CONO CLEAR or DATAO CLEAR pulse. These negative pulses are used by ANDing the pulse on the bus with the device selected level and regenerating the pulse with a pulse amplifier. Each pulse may be received from the I/O bus in one of two ways. If the device ("box") uses only one device number, the I/O bus pulse (e.g., IOB CONO CLEAR) should be ANDed with the device select level in a R- or S-series 1 mA diode gate such as the R111. The resultant ANDed pulse should be regenerated with a pulse amplifier such as the R613. If the device "box" uses two or more device numbers, the I/O bus pulse should be buffered and inverted with a R- or S-series 1 mA diode inverter such as the R107. The resultant pulse should be ANDed with the device selected levels for the various device numbers used (e.g., with the DCD gate of a pulse amplifier) and the resulting pulses regenerated with a pulse amplifier such as the R613. See the examples in Figures 2-5 and 2-6.

The command to accept data information operates similarly to the commands to accept control information. There is a negative IOB DATAO CLEAR pulse and a negative IOB DATAO SET pulse which must be applied to circuitry identical to the CONO pulse circuitry. These pulses may be used for control functions as well as for controlling data transfer. For example, the DATAO CLEAR pulse usually sets the BUSY flag and clears the DONE flag of an output device and may initiate other actions as well.

When the central processor gives the command to send status information to the central processor, a 2.5 μs negative IOB CONI level is sent out by the central processor. This level determines when and for how long the device should present its status information to the I/O bus. This level may be received off of the I/O bus in one of two ways. If the device "box" uses only one device number for CONI, the I/O bus level IOB CONI should be ANDed with the device select level in a R- or S-series 1 mA diode gate such as the R111. The resulting level may be inverted and buffered as necessary to drive the I/O bus CONI data gates. If the device "box" uses two or more device numbers for CONI, the I/O bus level IOB CONI should be inverted with a R- or S-series 1 mA diode inverter such as the R107. The resultant level should be ANDed with the device selected levels for the various device numbers used with any convenient AND gate and outputs applied to the I/O bus CONI data gates. See Figures 2-5 and 2-6 for examples.

The command to send data information to the central processor operates identically to the command to send status information. There is a 2.5 μs negative IOB DATAI level which must be applied to circuitry identical to the IOB CONI circuitry. This level may be used for control functions in addition to controlling data transfer. For example, the DATAI command usually sets the BUSY flag and clears the DONE flag of an input device and may initiate other actions.

Data Line Sampling

Since the data lines transmit information both to and from the processor, great care must be taken in the selection of circuits to sample or drive these lines. The data lines must be sampled with the W107 Buffer which places a minimum load on the data lines. No other dc load may be connected to the data lines.

Only 18 bits of control information are sent from the computer by a CONO instruction (since it is immediate mode). A copy of the control information is sent in both halves of the data word. If a device requires more than 18 bits of control information, it must be assigned two or more device numbers.

The control or information data are allowed to settle 1 μs before the CONO CLEAR or DATAO CLEAR pulses occur (see timing diagram, Figure 2-4) and may be sampled by these pulses.

Driving the Data Lines

All data sent to the central processor must be applied to the I/O bus with a saturated-transistor collector supplying at least 26 mA to the I/O bus, ordinarily a B-series 2 mA or 3 mA gate. The B163 is recommended for this use. Alternatively, the B141 can be used where many registers must be placed on the I/O bus. No clamped load may be attached to the data lines at any device. Typically, one input of the B163 is the DATAI or CONI level suitably ANDed with the device selected level and the other input of the gate is the information or status data to be sent to the central processor. The device shall not drive the data lines except when it is being addressed.

The CONI instruction reads all 36 data lines into memory. However, the CONSZ and CONSO instructions (being immediate mode) test only the right half of the status word (bits 18 through 35). Thus any status data which may be tested with a CONSZ or CONSO instruction must appear in the right half of the device's status word. Simple devices usually do not use the left half of the status word.

Priority Interrupt Circuits

Three flip-flops in the control register of each device (which causes a priority interrupt) must be used to store the interrupt channel number of the device. These flip-flops are usually loaded from

bits 33 through 35 of the CONO data word. The outputs of these flip-flops form the binary input to a binary to octal decoder. A signal which is the inclusive OR of all conditions causing an interrupt is applied to the enable input of the decoder. The recommended binary-to-octal decoder is the B152. The seven decoder outputs representing channel numbers 1 through 7 are applied to the corresponding IOB PI lines. The 0 output of the decoder is not used. The B152 outputs may be tied directly to the appropriate IOB PI lines. Otherwise any B-series 2 mA diode gates may be used to drive these PI lines. No clamped load may be connected to the IOB PI lines at any I/O device. Each interrupt condition should be cleared when it is serviced, e.g., by DATAO CLEAR or DATAI commands. The PI must be cleared before the time indicated in Figure 2-4 during the I/O cycle in which it is cleared. The status register should contain a flag for each condition which causes an interrupt (ordinarily in the right half of the status word) so that the program can determine the cause of the interrupt. An interrupt must be clearable by some I/O instructions (CONO, DATAO, or DATAI). The PI channel flip-flops must be set to the number 0 by the IOB RESET pulse. Complex devices may have more than one PI channel assignment; for example a channel for "done" and a channel for device errors. If two or more channel assignments are required, a set of flip-flops and decoders must be provided for each assignment.

It is a common practice to start output data transfers by setting the DONE flag of the I/O device and allowing the PI thus caused to transfer to the device's interrupt service subroutine. To allow this type of programming, CONO should be able to clear and set the DONE flag of each device. This also facilitates maintenance programming.

Any device which uses the BLKI or BLKO instructions for data transfer should either provide separate PI circuitry for data interrupts and all other interrupts or else disable all other interrupts during data transfer. The latter is not always possible as the device may use an end-of-record mark or have a non-recoverable error stop feature which inhibits further data transfer, leaving the BLKI or BLKO waiting for additional data.

A PI request may remain raised after a data transfer, if more data is immediately available for transfer. If the PI request is not lowered, a PI cycle will occur after every instruction (for details of PI operations see the PDP-10 System Reference Manual). A BLKI or BLKO instruction will then transfer data on every possible I/O cycle until the PI is lowered (or a PI with higher priority occurs). The PI should be lowered when the desired data transfer is finished (determined by a counter, end of sector, etc). The processor will be completely occupied with the BLKI or BLKO instruction during the transfer.

Read-In Signals

Read-in mode control is accomplished by the IOB RDI PULSE from the central processor and IOB RDI DATA level to the central processor. The IOB RDI PULSE must be taken from the I/O bus using circuits identical to those used for the CONO and DATAO pulses. The read-in pulse must initiate

appropriate actions for each device intended to be used in the read-in mode. (For example, see the description in the Introduction above.) When the read-in device has a word of data information ready for the central processor, it should apply a ground to the IOB RDI DATA line using a B163 or other 2 mA or 3 mA diode gate. No clamped load may be placed on this line by any device. The ground on the IOB RDI DATA line initiates action similar to a PI request during normal processor operation. The IOB RDI DATA level is usually made up of the device DONE flip-flop (1) ANDed with the device select level. The IOB RDI DATA level must be removed by the DATAI level, usually by clearing the DONE flip-flop. The IOB RDI DATA line has no effect except when the central processor is in read-in mode. The IOB RDI pulse is a 400 ns negative pulse on the I/O bus.

Drum Split Signal

The IOB DR SPLIT line is provided for the use of high-speed devices whose data path is through the memory bus system. When this line is made high (ground) by a device, central processor read-modify-write memory cycle requests are inhibited by forcing instructions which ordinarily request read-modify-write cycles to split requests into separate read and write cycles instead. Thus the maximum time from the time that the high-speed device requests a memory cycle until its requested memory cycle is initiated is one memory cycle time (assuming the high-speed device has the highest priority of the requested memory references).

The maximum time required if the IOB DR SPLIT line is not used is one memory cycle time, plus 1000 ns, plus the round trip cable delay between the memory module addressed and the central processor. The standard PDP-10 memory system is sufficiently fast that very few devices require the use of the IOB DR SPLIT signal.

A high-speed device should make the IOB DR SPLIT line high as soon as it realizes it will be doing a high-speed data transfer to or from memory, in order to assure that it does not request its first memory cycle during a read-modify-write cycle which the processor has already initiated. For details of memory bus timing and rules refer to the PDP-10 Memory Bus section. The IOB DR SPLIT line must be driven by a 2 mA or 3 mA diode gate without a clamped load such as a B165. No dc load is allowed on this line.

IOB RESET

The IOB RESET pulse is provided by the central processor to stop and clear all I/O devices. This cleared state should not allow the device to cause any PI requests until the processor has done a CONO to the device to specify which channel the device is to use. The IOB RESET pulse should clear any locked-up states (although few, if any, devices should have such states). It should clear all sources

of interrupts and may perform other resetting functions. The IOB RESET pulse must be taken off of the I/O bus with a 1 mA diode gate such as the R107 and the pulse should be regenerated by a B613 pulse amplifier. During the power turn-on sequence, the central processor generates a burst of IOB RESET pulses to ensure the presence of a pulse after all power supplies are up to the proper voltage. The IOB RESET pulse is a 400 ns negative pulse on the I/O bus. This pulse should not be gated with the device select level.

Power Up and Power Down

In order to make it possible to maintain a particular I/O device (or I/O box), an I/O device should clear itself when it is turned on (dc power on) and should inhibit any PI requests when it is turned off (dc power off). In addition, it should have no effect on the I/O bus which would interfere with other devices when it is off. To clear an I/O device as it comes on, the R303 integrating one-shot is recommended. This module comes on in the 1 state when power comes on and will go to the 0 state after approximately its normal delay time. This 1 to 0 transition should initiate the power clear signal which is also produced by the IOB RESET pulse. See the examples.

To inhibit interference with the I/O bus while a device is turned off, a contact is provided on the 844 Power Control which provides a ground signal at turn-off prior to the shutting down of power. This ground signal must be applied to an input of every gate driving the I/O bus data lines and every gate driving the IOB PI lines, the IOB DR SPLIT line, and the IOB RDI DATA line. This turn-off signal may be applied directly to a gate input or through a R001 or R002 diode.

Wiring

The wiring from the I/O bus connectors to the transmitting or receiving modules in the I/O device should be as short as possible. In general wire lengths less than six inches can and should be achieved. The I/O bus connectors may be located in the middle of a FLIP CHIP connector row (locations 13 through 20 in a 32 slot wide row) in order to minimize wire lengths. PDP-10 wiring rules for loading, terminating and length of wires should be followed when building on I/O device to achieve high reliability with margins. See Chapter 11 for details.

Example

Figure 2-5 shows a typical simple I/O device, in this case, a CalComp Plotter Control for a CalComp Model 563 Plotter. Figure 2-5a shows the required interfacing modules for device decoding and control level and pulse gating as well as the PI decoders. Figure 2-5b shows the data interface, which for the plotter is only six bits wide. Figure 2-5c shows the plotter control proper. The power off

signal from the 844 Power Control is driven into the data line gates by tying a R002 diode to the PLOT CONI negative signal (Figure 2-5a). The power off signal is driven into the PI decoder by tying a R002 diode to the DONE flip-flop line which drives the B152 decoder; that is the (1) negative or (0) positive line. As a side effect this will clear the DONE flip-flop, which is not objectionable.

Two examples of I/O bus usage in process control and experimental research applications are shown in Figure 2-6 and 2-7. The example in Figure 2-6 shows the use of the CONSO and CONSZ instructions with a small amount of hardware to skip in the computer program on the presence or absence of some external signal generated by a switch closure, by other logic, or by experimental or control apparatus. The signal is applied (say) to the line marked SKP 34 in Figure 2-6. If the signal is high (ground), executing the instruction CONSZ SKP, 4 will not skip the next instruction, whereas, if the signal is low (-3 V), CONSZ SKP, 4 will skip the next instruction. CONSO, of course, skips under just the opposite conditions. (See the PDP-10 System Reference Manual for complete details of the operation of CONSZ and CONSO.)

Figure 2-7 shows the hardware required to provide the control pulses and control levels to external equipment. In this case, the CONO instruction is used in the program to set flip-flops or to trigger pulse amplifiers. Executing CONO PLS, 10 will cause the line labeled PLS 32 in Figure 2-7 to be pulsed, CONO PLS, 2 will reset the flip-flop to 0. CONO PLS, 3 which appears to both set and reset the flip-flop, actually causes the flip-flop to be complemented due to the nature of the R202 flip-flop. Extensions to both of the devices shown in Figures 2-6 and 2-7 are obvious.

Larger Devices

Figures 2-8 and 2-9 are examples of interface logic for larger devices (having two or more device numbers for example). Not all bits of the status register need to be flip-flops. They may also be the output of a logic network or an external signal. However, all bits of the status register which cause a PI must be capable of being either cleared or disabled.

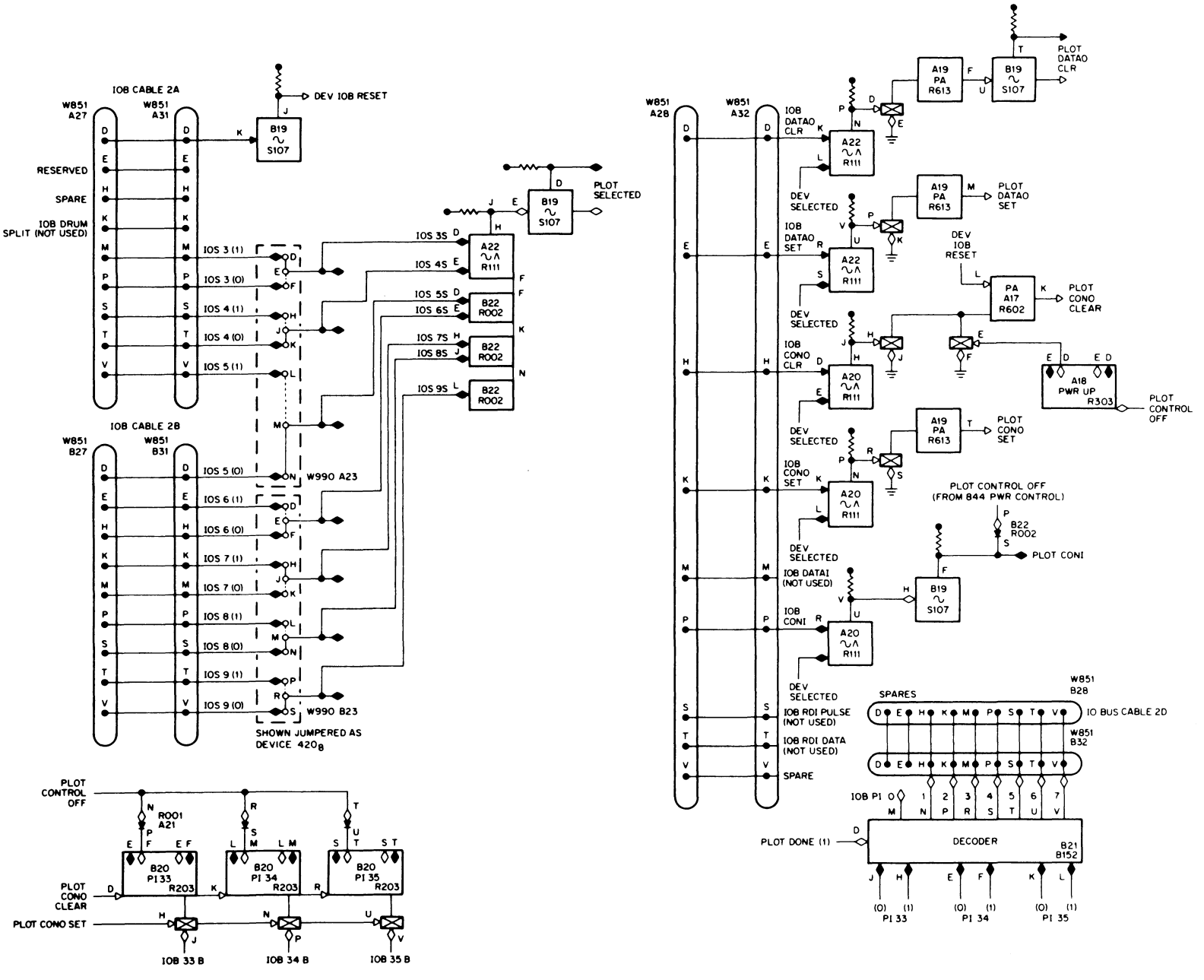


Figure 2-5(a) Control Interface

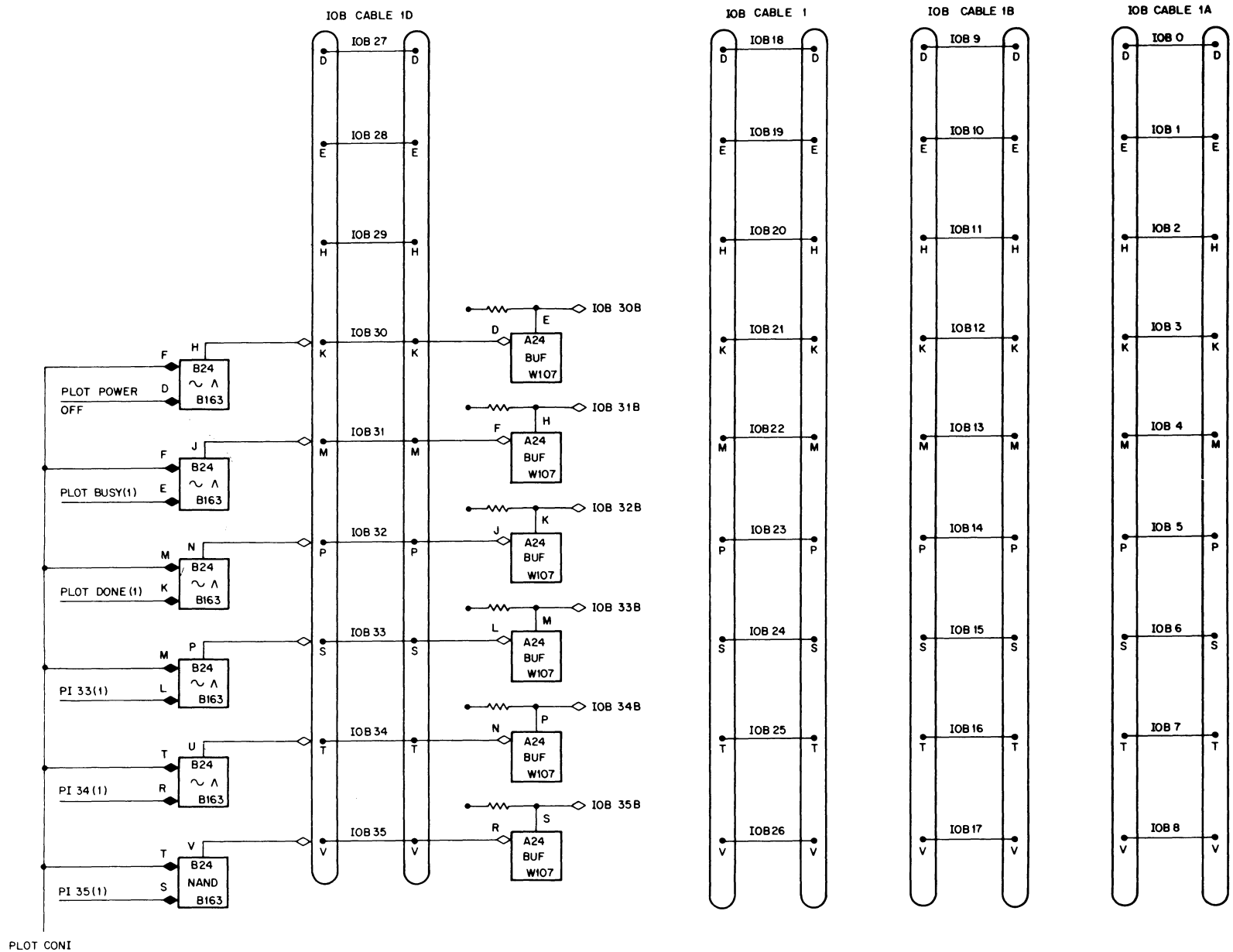


Figure 2-5(b) Data Interface

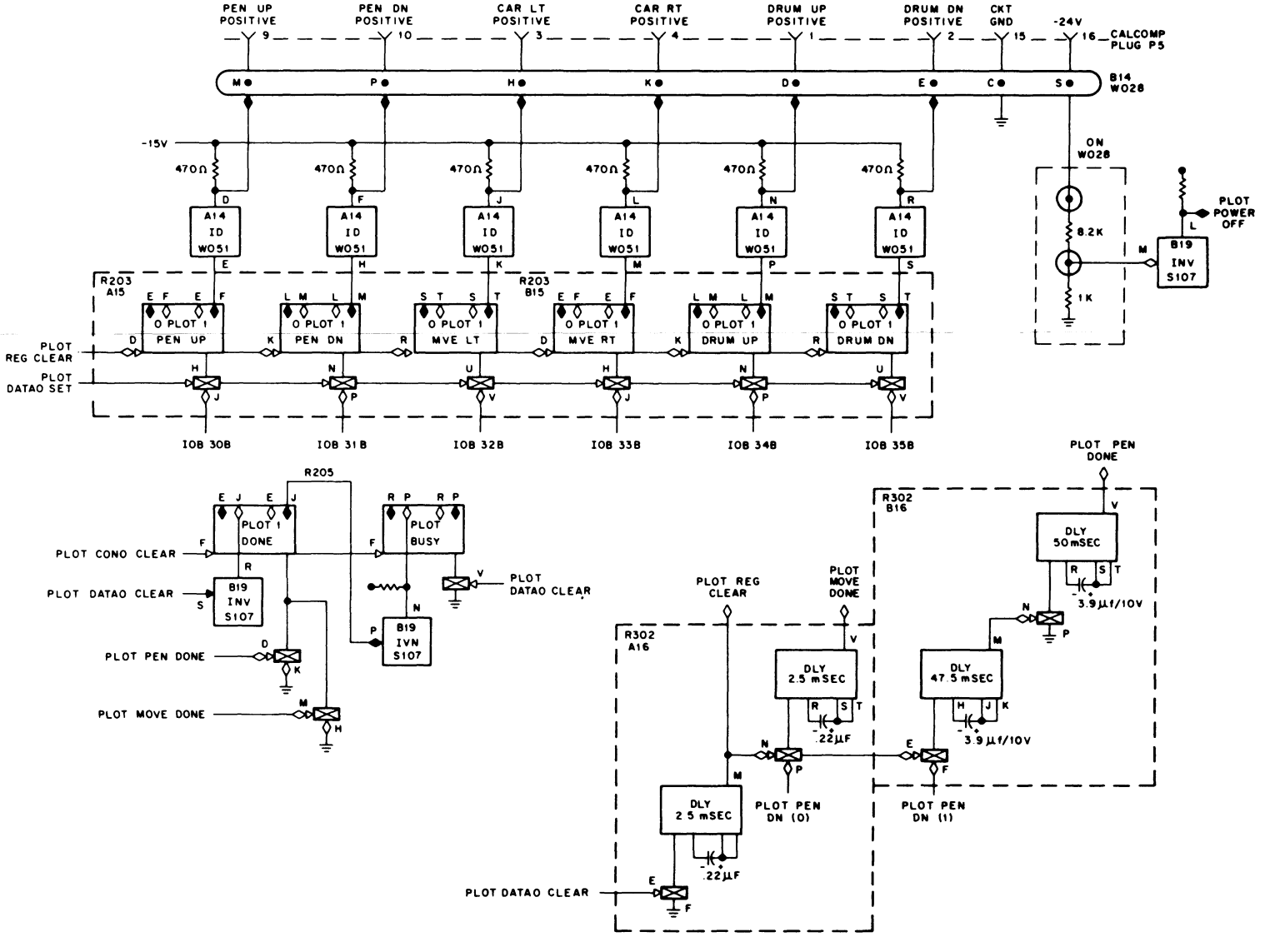


Figure 2-5(c) CalComp Plotter Control

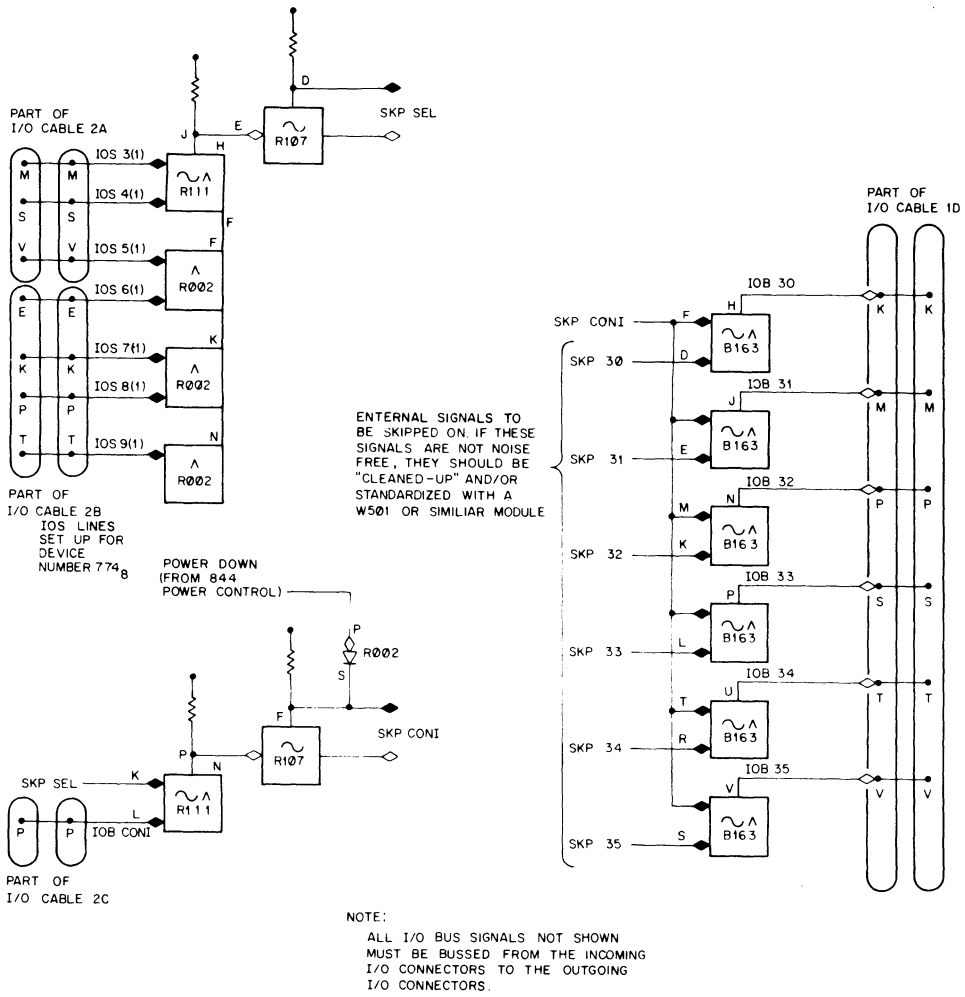


Figure 2-6 SKIP Device (for CONSO and CONSZ)

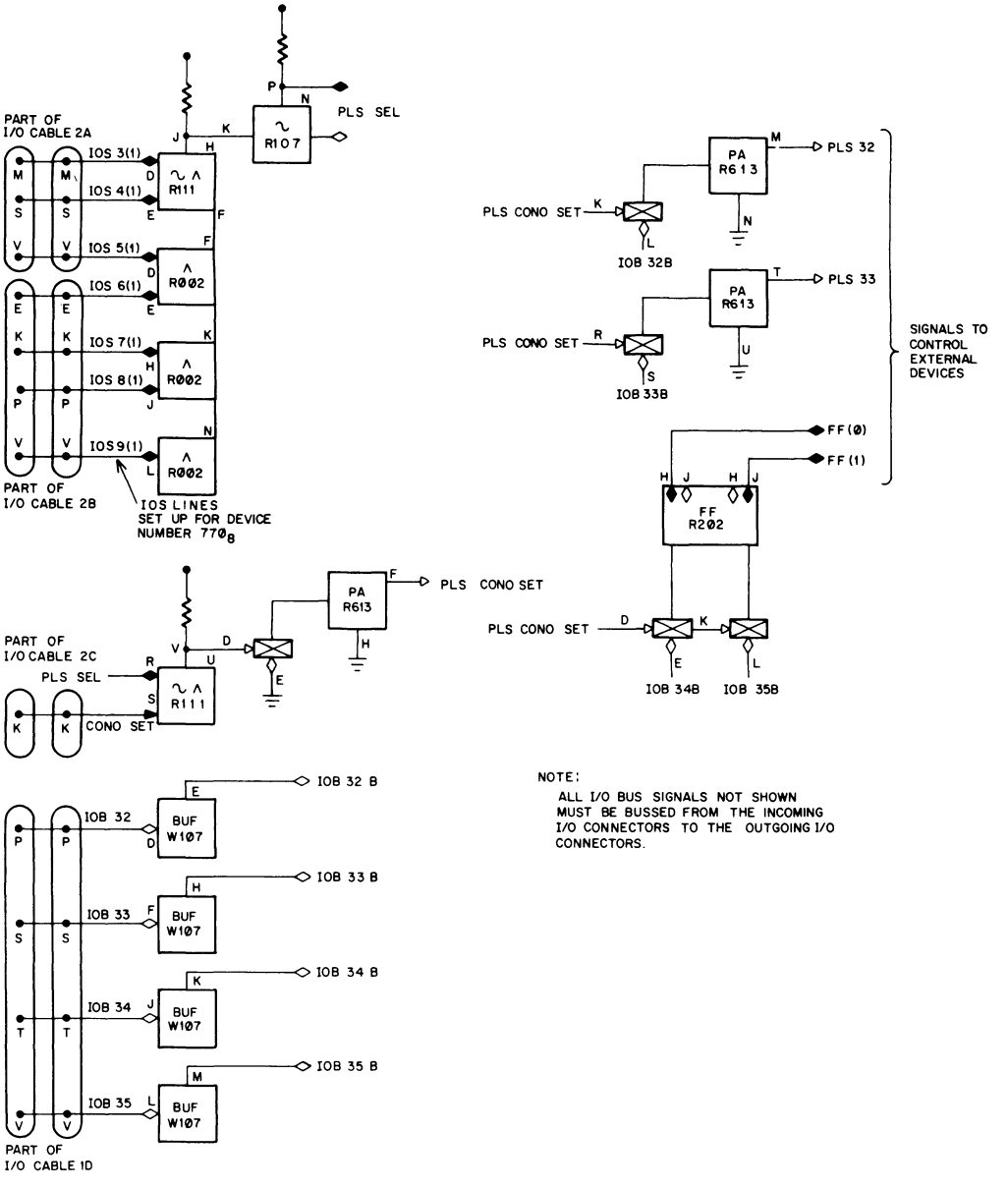


Figure 2-7 Control Device

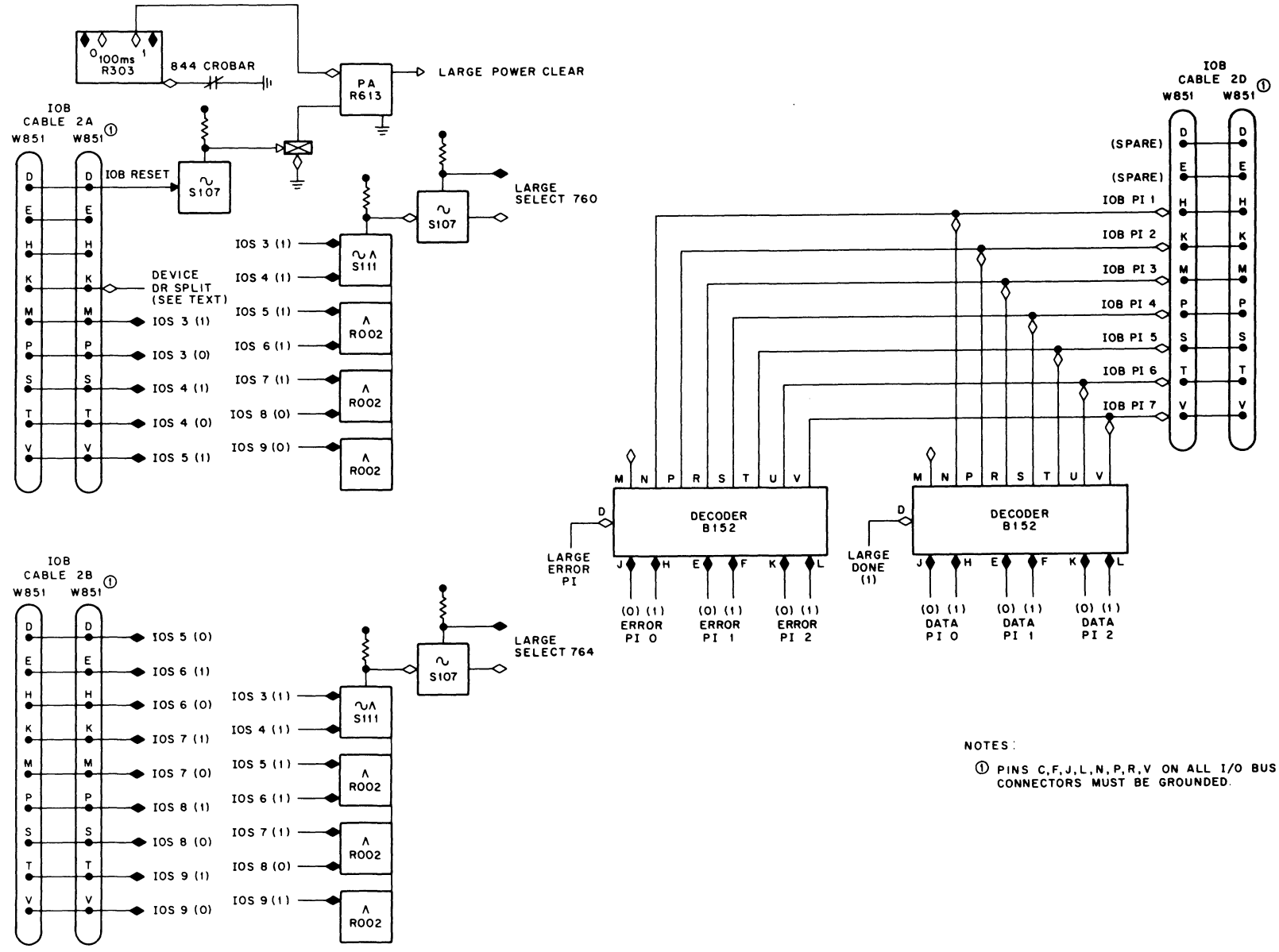


Figure 2-8 Interface Logic for Larger Devices

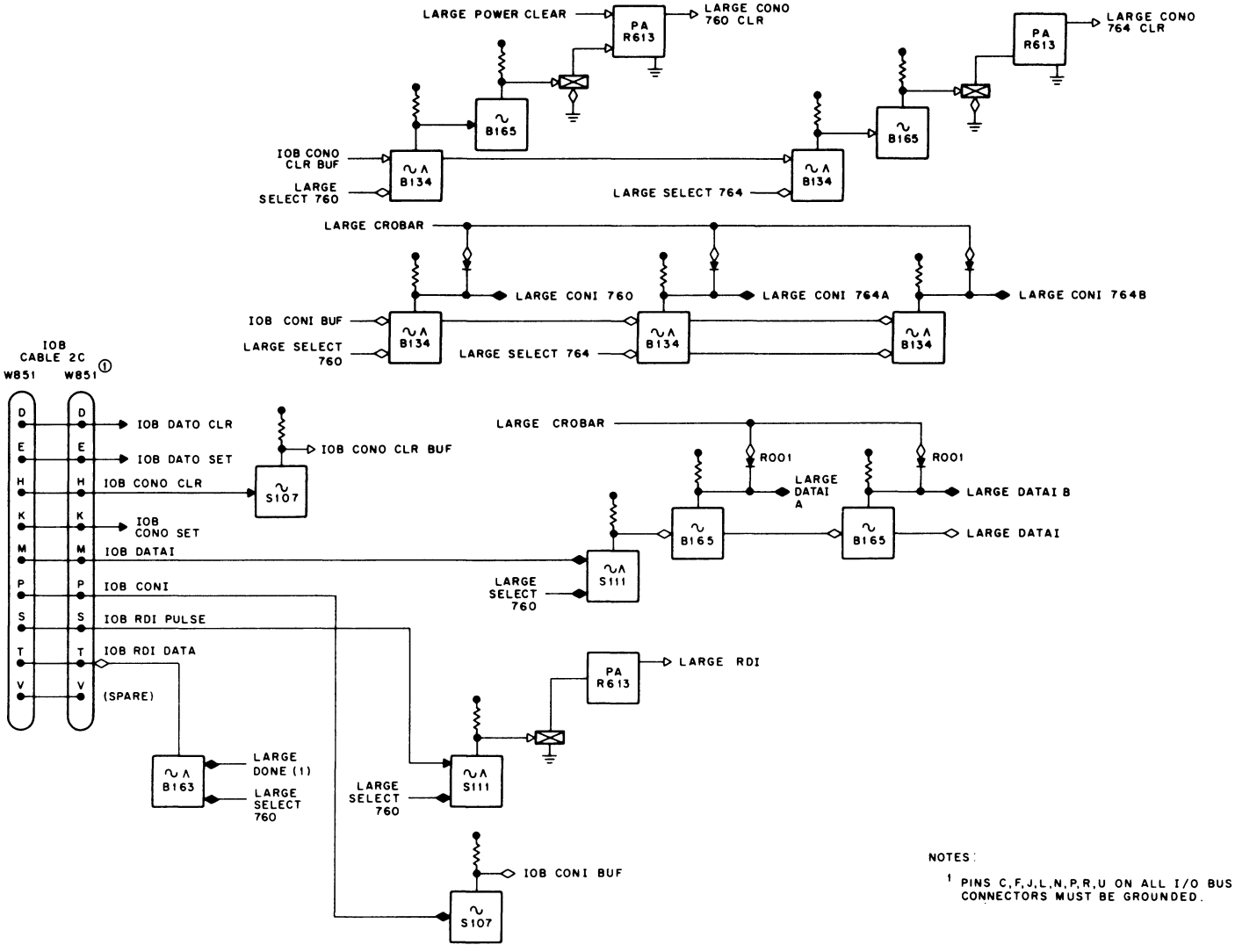


Figure 2-8 Interface Logic For Larger Devices (Cont)

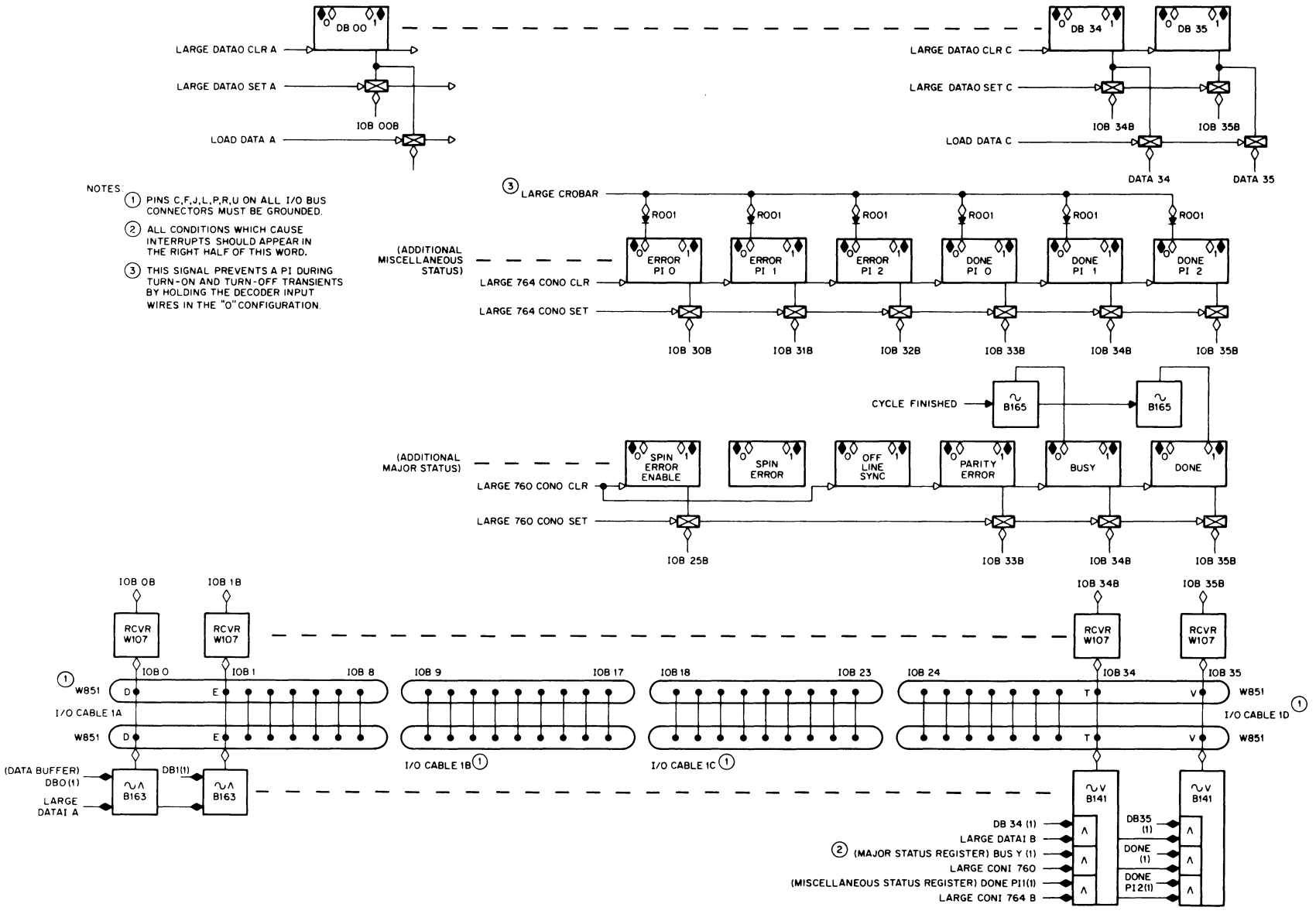


Figure 2-9 Data Interface for Larger Devices

Maximum Loading Rules

The I/O bus must be less than 150 ft (46 m) long. The I/O bus connectors should be located low in the cabinet to minimize the cable length used up in any given device. A compromise between short cables and convenient access is best.

A maximum of 40 I/O "boxes" is allowed; that is, a maximum of 40 taps on the I/O bus data lines with W107 modules. No other dc load is allowed on the IOB data lines. The output of a W107 may supply I/O bus data to more than one device; for example, the standard PDP-10 peripheral cabinet containing the line printer control, the card reader control, and the plotter control uses only one set of W107's and counts as only one I/O "box."

A maximum of 40 taps on the I/O bus pulse and level control lines (such as IOB DATAO CLEAR) with 1 mA diode gates such as the R107 or R113 is allowed. If more than one device number is used in an I/O "box," the control pulses and levels must be buffered by an inverter such as the R107 and then distributed to the various devices or device numbers.

A maximum of ten 2 mA diode gate collectors may be tied to the I/O bus data lines per I/O "box"; for example, ten B163 outputs, or ten B133 outputs, or one B141 output and three B165 outputs. The B141's output counts as seven collectors, the B134's counts as two collectors. No clamped loads may be tied to the I/O bus data lines. Any number of device number decoders may be used in an I/O "box" up to a maximum of 123 device numbers on the I/O bus (five device numbers are already used in the central processor).

A maximum of 20 PDP-10 I/O "boxes" may be used on the I/O bus with up to five PDP-6 I/O devices. A maximum of ten PDP-6 I/O devices may be used alone on the PDP-10 I/O bus.

Conversion of PDP-6 I/O Devices for PDP-10 Use

To convert a PDP-6 I/O device for use on the PDP-10 I/O bus system it is only necessary to remove the -15 V turn-on lead from pin C of I/O cable 3 (System modules) or pin E of I/O cable 3A (FLIP CHIP modules) and attach it to pin 6 of the margin check cable. If the I/O device does not use -15 V turn-on, this change is not required. The PDP-6 margin check cable bracket should be reworked as indicated in the PDP-10 margin check section (Chapter 8) in order to carry PDP-10 margin voltages across the PDP-6 I/O device. The 100 ohm resistors on 4230's and 4657's should be shorted out if they have not already been. No other changes are required.

Operation of PDP-10 Devices in PDP-6 Systems

PDP-10 I/O devices may be connected to PDP-6 systems without alteration. However, the BC10A (W851) bus cables cannot be used as the clamping terminating features of the bus cable interfere

with the recovery of the 4606 Pulse Amplifiers used in the PDP-6. Special unclamped bus cables must be used such as can be constructed from W021 or W852 FLIP CHIP connector cards.

List of Modules for Use in PDP-10 I/O Bus Interfaces

2 mA B-series Gates	1 mA R- and S-series Gates	
B133	R001	S107
B134	R002	S111
B135	R107	S202
B137	R111	S203
B141	R113	
B152	R121	
B163	R123	
B165	R613	
Used to drive I/O Bus Data Lines IOB DR SPLIT, IOB RDI DATA, and IOB PI Lines	Used for device decoding and receiving control pulses and levels.	
Hardware	W-series Modules	
H003 Connector Retaining Kit H004 Connector Retaining Kit H351 I/O Bus Connector Kit BS10A I/O Bus Cable Set	W107 Receiving I/O bus data	

Other DIGITAL modules may be used for constructing I/O devices, although preference should be given to modules already in use in the PDP-10 central processor as these have been thoroughly checked for compatibility and performance and their use will reduce the number of module types stocked for repair and replacement purposes.

CHAPTER 3
INTRODUCTION TO DIGITAL LOGIC

Most of the PDP-10 system is put together with DIGITAL's discrete component FLIP CHIP modules (B-, R-, S-, and W-series modules). Logic schematics (called block schematics at DEC) using these modules are usually drawn with DIGITAL'S pre-MIL-STD-806 logic symbols. With the exception of shape representation, however, these logic symbols conform to MIL-STD-806 with one additional feature added for clarity. Both of these logic symbol standards are elaborated briefly below.

The most striking feature of DIGITAL logic (and most puzzling to those not accustomed to it) is that a logic signal may be true (asserted, logical 1) either when it is high or when it is low depending on the choice of the logic designer. In any given logic network, both signals which are high-when-true and signals which are low-when-true will ordinarily exist. Not infrequently, the same logic signal will have two electrical representations, one high-when-true and the other low-when-true. In addition, the logic designer has the freedom of using the logical negation of a logic signal. This usage is indicated by a not sign (~) or a minus sign preceding the signal name. The indication of whether a signal is true-when-high or true-when-low is the type of diamond or arrow (open or solid) in DIGITAL logic symbols or the presence or absence of a small circle in MIL-STD-806 logic. This convention allows the logic designer to design the logic without regard to the inversion properties of most DIGITAL logic, and then to assign logic packages to the realization of the design without undue redesign to account for gate inversions.

The electrical equivalance of the negated-low signal and the un-negated-high signal and of the negated-high and un-negated-low signal is recognized and freely used.

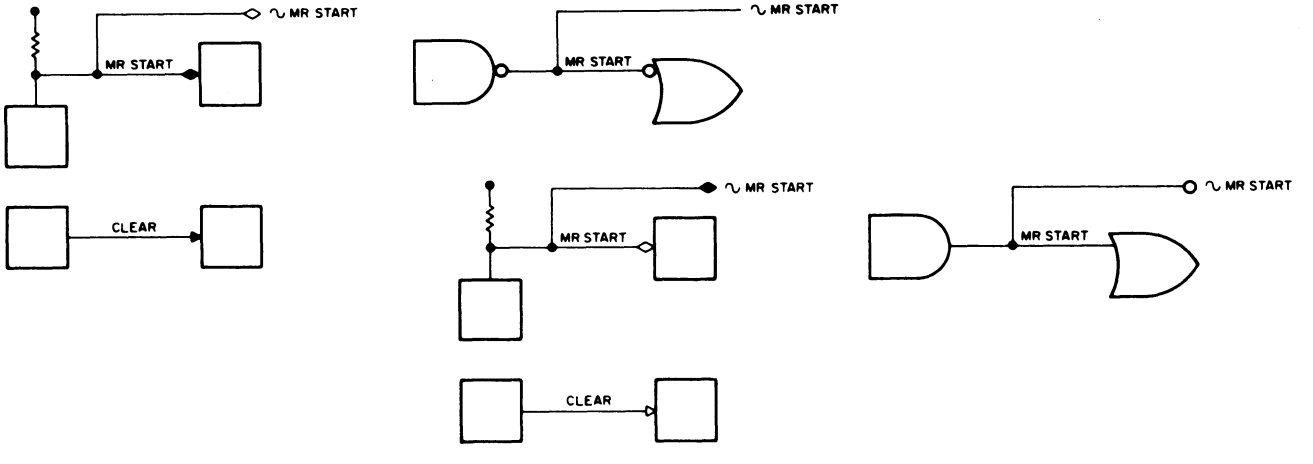


Figure 3-1 DIGITAL Logic Signals

Frequently in larger logic networks, it is convenient to show a named signal's source without a connection to its load which is elsewhere. To facilitate this, a small circle may be drawn at the end of the source line when using MIL-STD-806 logic symbols in order to show that the signal is true-when-low. This is the only deviation from MIL-STD-806 used by DIGITAL.

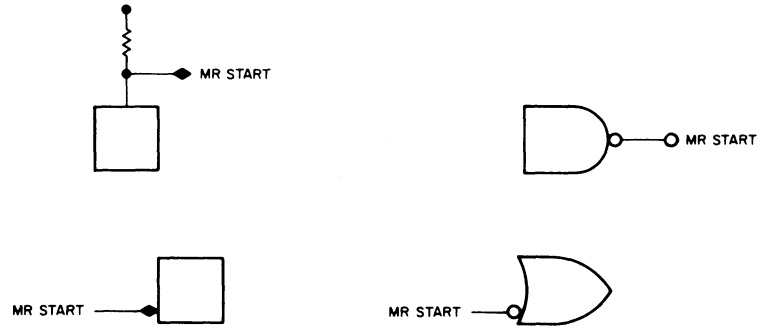


Figure 3-2 Sources and Loads Shown Without Connections

In DIGITAL logic symbols, wired ANDs and wired ORs are not explicitly marked. They must be recognized. Due to the electrical properties of DIGITAL's below ground logic (ground and -3 V logic levels), a wired OR will usually occur at ground (high) and a wired AND at -3 V (low). The B683 and W102 are exceptions.

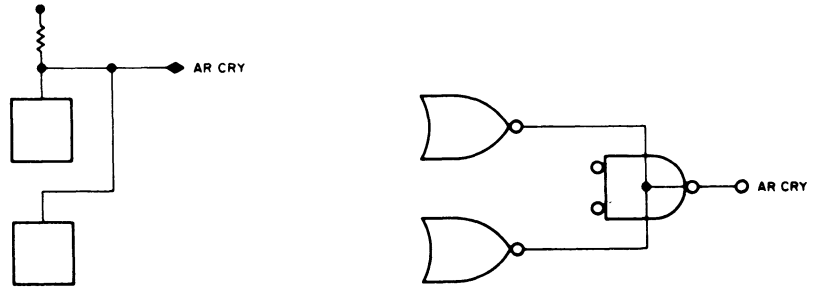


Figure 3-3(a) Wired AND

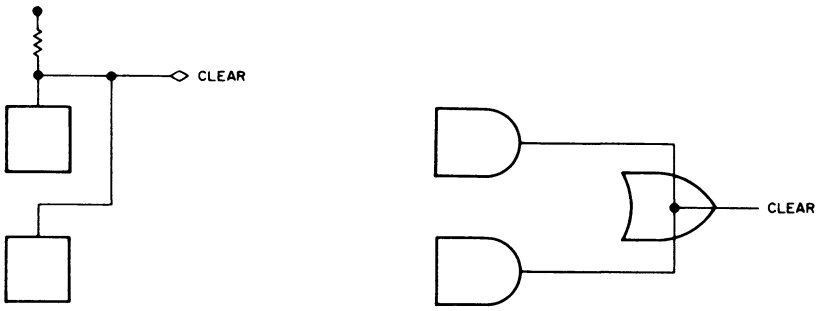


Figure 3-3(b) Wired OR

In DIGITAL logic, most flip-flops are drawn with four outputs: one which is high when the flip-flop is in the 1 state, one which is low when the flip-flop is in the 1 state, one which is high when the flip-flop is in the 0 state, and one which is low when the flip-flop is in the 0 state. This convention allows the condition "the flip-flop is in the 1 (0) state" to be used with gates that require either high or low inputs without juggling highs, lows, 1s and 0s. Although a flip-flop has four logical outputs as noted above, it has only two electrical output connections, as the 1-high and 0-low connections are electrically equivalent, as are the 1-low and 0-high connections. Except when the lines are quite short, connections to flip-flop outputs are not usually shown explicitly.

Figure 3-4 Flip-Flop Representation

In MIL-STD-806 logic drawings DIGITAL shows only the 1-high and 0-high output of a flip-flop, although all outputs are considered present for the purpose of logic design.

Special mention should be made of DIGITAL's DCD (diode-capacitor-diode) gate which is both an AND gate and a logic delay. This gate allows the output of a flip-flop to be sampled (with a DCD gate) at the same time the flip-flop state is changed (by any means). The flip-flop state seen by the DCD gate is the state prior to the change. The DCD gate generates an output pulse when the "level" input has been true (high) for approximately 400 ns and the "pulse" input has a 100 ns positive pulse or a positive-going (ground-going) level change with a risetime of less than 60 ns applied to it.

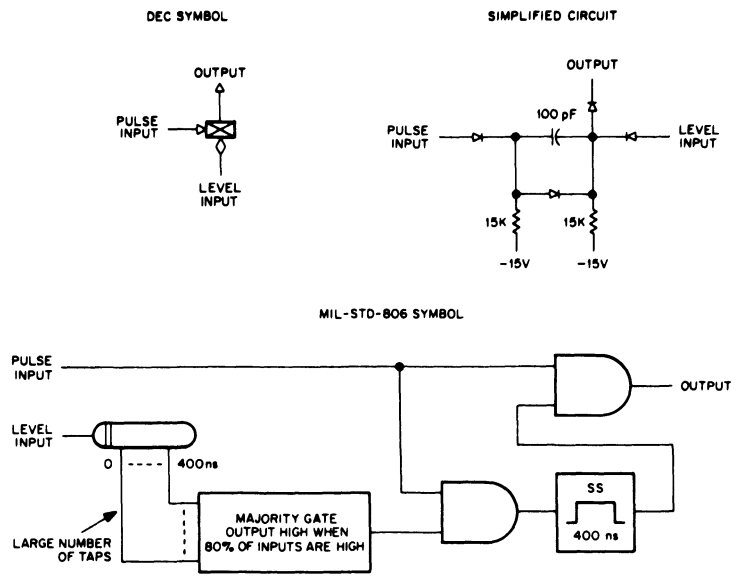


Figure 3-5 DCD Gate

It is recommended that the DIGITAL rectangular symbol for the DCD gate be used with either the older DIGITAL logic symbols or with the MIL-STD-806 logic symbols in order to distinguish the quite different properties of the two inputs and to indicate the logic delay properties of the DCD gate.

DIGITAL logic symbols are all rectangular in shape. The function of the symbol is indicated by a notation in it describing its function. Examples of the more common symbols are shown below.

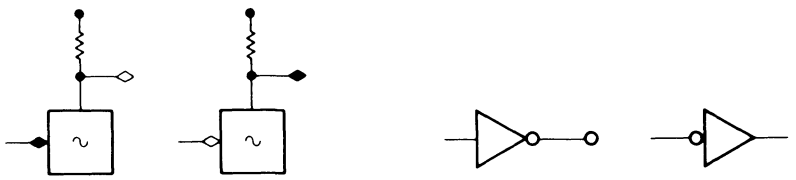


Figure 3-6 (a) Inverter (NOT Gate)

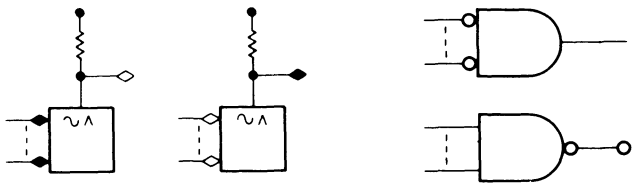


Figure 3-6 (b) AND Gate

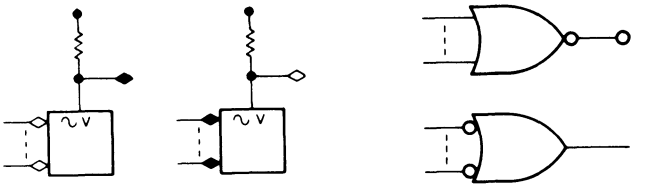


Figure 3-6 (c) OR Gate

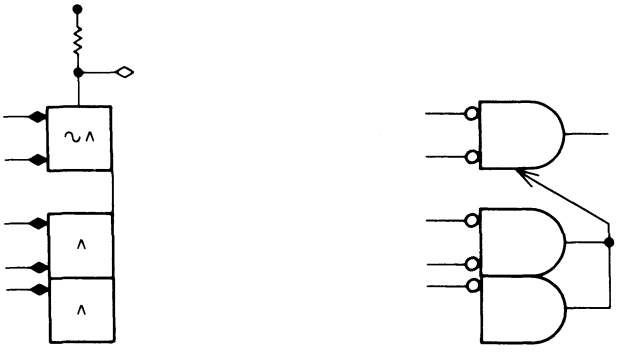


Figure 3-6 (d) Expanded Gate

Figure 3-6 (e) Pulse Amplifier

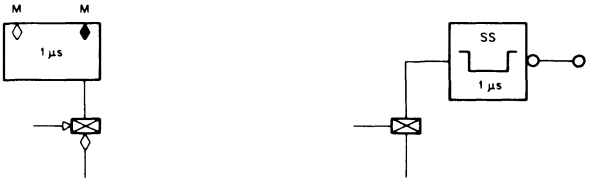


Figure 3-6 (f) Monostable Multivibrator (Single Shot)

Figure 3-6 (g) Monostable Multivibrator (Delay)

Figure 3-6 (h) Delay

Figure 3-6 (i) Clamped Load

DIGITAL makes free usage of the electrical equivalence of various logic configurations. As an aid to understanding, symbols are drawn to represent the logic function intended by the designer rather than as a single standard symbol for each module type. Thus, a particular module type may appear as several different symbols.

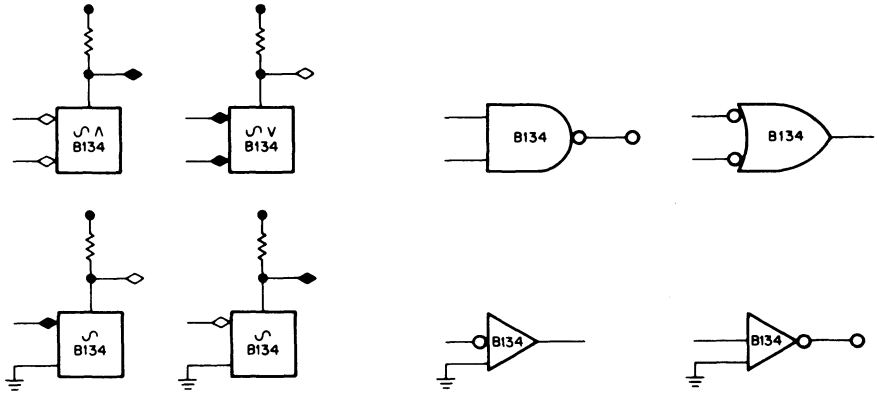


Figure 3-7 Different Uses of a Particular Module

Occasionally, the trailing edge of a signal will be used to cause some action, usually by triggering a DCD gate. This usage is noted below.

Figure 3-8 Trailing Edge Triggering

For additional details on the types of logic modules available see the DIGITAL Logic Handbook, C105 and the module descriptions in Chapter 4.

CHAPTER 4
PDP-10 MODULE INFORMATION

This chapter provides descriptions of many of the DIGITAL FLIP CHIP modules useful for building special hardware for PDP-10 systems. PDP-10 wiring rules are provided in Chapter 11 to aid the designer in producing reliable high-speed logic designs.

DIGITAL builds three series of compatible below-ground logic (the B-, R- and S-series), two series of compatible above-ground logic (K- and M-series), an extensive line of modules to interface different types of logic (W-series), a line of special purpose modules (G-series), and a line of support hardware for its module line (H-series).

With few exceptions, the DIGITAL compatible below-ground logic operates with logic levels of ground (±0.3 V) (upper level) and -3 V (-3.3 V to -3.9 V) (lower level) using diode gates which draw input current at ground and supply output current at ground.

The DIGITAL compatible above-ground logic generally operates with levels of ground (±0.4 V) (lower level) and +2.4 to +3.6 V (upper level) using TTL or TTL-compatible circuits whose inputs supply current at ground and whose outputs sink current at ground.

The DIGITAL Logic Handbook, C-105, is recommended reading for those not already familiar with the basic principles of digital logic and the type of circuits used in DIGITAL's logic modules. Updated repair schematics for all modules used in the PDP-10 are furnished with each system.

ABBREVIATIONS

S. I. (Systeme International) abbreviations are used where applicable. The most common of these and some special abbreviations are listed below. The units used are consistent with the MKSA system of units.

Basic Units		Multipliers		
A	Ampere	G	10^{+9}	Giga
V	Volt	M	10^{+6}	Mega
Ω	Ohm	k	10^{+3}	kilo
s	second	c	10^{-2}	centi
H	Henry	m	10^{-3}	milli
F	Farad	μ	10^{-6}	micro
m	Meter	n	10^{-9}	nano
Hz	Hertz (cycle per second)	p	10^{-12}	pico
		f	10^{-15}	femto

Usual Usage

Hz	Hertz	
kHz	10^{+3}	Hertz
MHz	10^{+6}	Hertz
s	second	
ms	10^{-3}	second
μs	10^{-6}	second
ns	10^{-9}	second
A	Ampere	
mA	10^{-3}	Ampere
μA	10^{-6}	Ampere
nA	10^{-9}	Ampere
μF	10^{-6}	Farad
nF	10^{-9}	Farad
pF	10^{-12}	Farad
H	Henry	
mH	10^{-3}	Henry
μH	10^{-6}	Henry
V	Volt	
mV	10^{-3}	Volt
μV	10^{-6}	Volt
Ω	Ohm	
kΩ	10^{+3}	Ohm
MΩ	10^{+6}	Ohm
mΩ	10^{-3}	Ohm

ac	alternating current
dc	direct current
DCD	diode-capacitor-diode
DEC	Digital Equipment Corporation
FF	flip-flop
min	minimum
max	maximum
PA	pulse amplifier
p-p	peak to peak
TTT	Total transition time

MEASUREMENT DEFINITIONS

Timing is measured with input driven by a gate or pulse amplifier of the series under test and with output loaded with gates of same series, unless otherwise specified. Percentages are assigned as follows: 0% is the initial steady-state level, 100% is the final steady-state level regardless of the direction of change.

Delay is the time difference between input change and output change, measured from 50% input change to 50% output change. Rise and fall delays for the same module usually are specified separately.

Risetime and falltime are measured from 10% to 90% of waveform change, either rising or falling.

Total transition time (TTT) is the time difference between 10% input change and 90% output change. Output rise and fall TTT are usually specified separately.

Typical propagation delay is the average delay per stage for many similar circuits connected in cascade and should be independent of the level (10%, 50%) at which it is measured.

Set-up time is the time during which an input must be held stable (e.g., the level input of a DCD gate) before another input is asserted (e.g., the pulse input of the DCD gate).

Input current is defined as positive when it is flowing into the input terminal.

Output current is defined as positive when it is flowing out of the output terminal.

All specifications are nominal or typical unless noted as Min or Max or with a tolerance.

B-SERIES MODULE INTERCONNECTIONS

Due to the high operating speed of B-series modules, the effects of wiring on logic operation should be considered. However, the use of diode-transistor circuitry similar to that used in the R-series modules provides good noise margins. Detailed guidelines for wiring systems including B-series modules are provided in Chapter 11.

Occasionally, a logic design will require a minimum delay along a particular path. Logic elements which provide a guaranteed minimum delay such as the B212 flip-flop or the B311 delay should be used to provide such a delay as regular decreases in delay are obtained in other modules due to continued improvements in technology.

Slow fall times of logic levels may limit the speed of systems built with B-series modules to less than 10 MHz. In most cases, an estimate of fall time can be made by considering the total capacitance on the logic line and the current available to drive the line negative. Figure 4-1 shows the equivalent circuit.

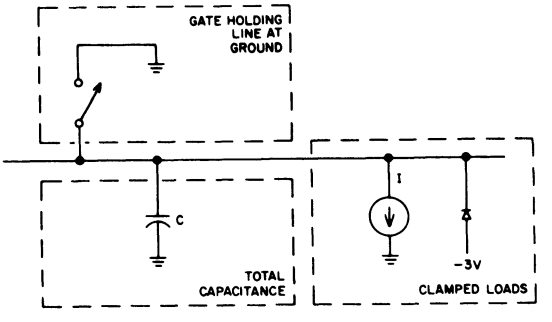


Figure 4-1 Circuit to Estimate Fall Time

The fall time is then given by

$$t_f\ (ns) = \frac{C\ (pF)}{I\ (mA)}\ \Delta V\ (V).$$

For B-, R-, S-series logic, as well as the "DEC" (below ground) portions of W-series modules, ΔV is around -3.5 V. To be conservative, I should be taken as the current that can be sinked by the clamped

loads at -3 V. Thus a "10 mA" clamped load provides -7 mA of current to discharge capacitance at -3 V. Inputs which require current at -3 V must be deducted from the available current before calculating fall time (e.g., B684 inputs, indicator drivers). Input and output capacitances are typically as follows: input capacity 10 pF for each diode input, output capacity 8 pF for each collector output, a clamped load with a separate pin represents 8 pF of capacity, and wiring represents 1 to 1.5 pF per in. (.04 to .06 pF per mm).

Fall time calculations become inaccurate as the delay inherent in the wiring (1.5 ns per ft, 4.5 ns per m) approximates 1/10 the estimated fall time due to overshoots, reflections and ringing.

When wire lengths become relatively long, the distributed capacitance and inductance of the wiring will produce overshoots and "ringing" of the logic signal. The DEC level terminator circuit has been designed to control the amplitude of these effects to eliminate false operation of the logic. A simplified circuit of the level terminator is shown in Figure 4-2.

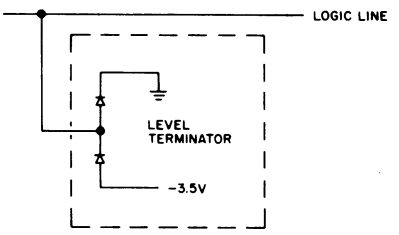


Figure 4-2 Level Terminator, Simplified Circuit

The level terminator operates by clamping the signal excursions at ground and -3.5 V. By applying level terminators as outlined in Chapter 11, these transmission-line-like problems should not cause trouble. Occasionally, a clamped load is incorporated into the level terminator to improve fall time (e.g., G796, G704). A theoretical analysis of the level terminator operation when terminating a transmission line is provided in Appendix A.

Module Margining

The PDP-10 is provided with a system for checking the margin of power supply which will still allow a module to operate. A module should work properly within a prescribed range of supply voltage variation. Failure to do so may be due to a faulty module or to timing or loading problems in the logic design. To avoid permanent damage to the modules, the supply voltage should not exceed the range 0 V to +20 V (+10 V supply) or 0 V to -20 V (-15 V supply). Exceeding these limits (or tighter limits where specified) may cause permanent damage to the module. Typical power supply margins which allow proper operation are shown with each module.

Inter-series Pulse Conversion

A question which frequently arises is how to integrate DIGITAL's various series of logic modules. Table 4-1 provides a helpful aid in the selection of module to convert pulses from series to another. For complete specifications refer to the appropriate module catalog.

DIGITAL's Module Applications Group can supply numerous application notes and advice on unusual problems in this area.

Table 4-1
Inter-Series Pulse Conversion

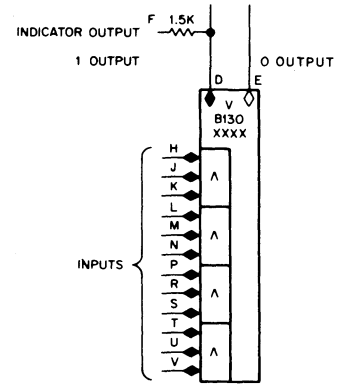
FROM \ TO		FLIP CHIP K 100/5 kHz 4/50 µs	FLIP CHIP M 6MHz 30 ns	Conversion To Below Ground → M652[1] W512 W510 1501	FLIP CHIP B 10 MHz 25 ns	FLIP CHIP R (& S) 2 MHz 40 ns	LAB 100 5 MHz 50 ns	SYSTEM 1000 5 MHz 50 ns	LAB 3000 500 kHz 300 ns	SYSTEM 4000 500 kHz 60 ns	LAB 5000 10 MHz 25 ns	SYSTEM 6000 10 MHz 25 ns
FLIP CHIP K[2]			M602**		B611**	R601,** etc.	602**	1607**	3602**	4604**	5602**	6603**
FLIP CHIP M	50 ns	M302 K303[3]			DIRECT	R601,* etc.	DIRECT	DIRECT	Convert To 100 Series First	Convert To 1000 Series First	DIRECT	DIRECT
Conversion To Above GND ↑ M502[1], W603, W601, 668, 4686												
FLIP CHIP B	40 ns	Convert To R or M Series First	M602			R601,* etc.	W607 602 with Feedback	W607 1609	Convert To R or 100 Series First	Convert To R or 1000 Series First	DIRECT	DIRECT
FLIP CHIP R (& S)	100 ns 400 ns	K303[4] R302 R303	M602** †		B611**		W607** 602**	W607** 1607**	W640	W640	B611** 5602**	B611** 6603**
LAB 100	70 ns	302	M602 †		5602 B611 †	R601,* etc.		DIRECT	3602 with Feedback	4604 3602 with Feedback	5602 †	5602 6603 †
SYSTEM 1000	70 ns	1304	M602 †		6603 B611 †	R601,* etc.	DIRECT		4604 3602 with Feedback	4604 4606	6603 5602 †	6603 †
LAB 3000	400 ns	3301 K303	M602** †		Convert To R or 100 Series First	R601,* etc. †*	602 †	1609 602 †		DIRECT	Convert To 100 Series First	Convert To 100 or 1000 Series First
SYSTEM 4000	400 ns	4301 4303 K303	M602** †		Convert To R or 1000 Series First	R601,* etc. †*	1609 602 †	1608 1609 etc. †	DIRECT		Convert To 100 or 1000 Series First	Convert To 1000 Series First
LAB 5000	40 ns	Convert To 100 Series First	M602		DIRECT	R601,* etc.	602 with Feedback	1609 602 with Feedback	Convert To 100 Series First	Convert To 100 or 1000 Series First		DIRECT
SYSTEM 6000	40 ns	6304	M602		DIRECT	R601,* etc.	1609 602 with Feedback	1609 1608 with Feedback	Convert To 100 or 1000 Series First	Convert To 1000 Series First	DIRECT	

[1] M502 and M652 must be used for 40 ns pulses
[2] Convert to unslowed K-series first
[3] See Application note AP-K-016
[4] Use 400 ns Pulse

*Invert with higher speed inverter to obtain correct polarity
**Invert twice with higher speed series to obtain adequate risetime
†Direct except where pulse overlap or recovery problems occur

B130 THREE-BIT PARITY CIRCUIT

Standard Size FLIP CHIP Module, 18 Pins



This special module has two levels of high speed logic and complementary outputs. It is designed to compute the parity (odd or even) of the contents of a flip-flop register with a minimum of delay, but it can be used wherever there is a need for four 3-input negative diode AND gates feeding a 4-input OR gate.

Delay is typically 15 ns from 50% of the input transition to 50% of the output transition when output capacitive loading is very small.

INPUTS: The input load is 2 mA shared among the inputs of each AND gate which are at ground. Input load at -3 V is less than 1 μA. When the inputs are connected to compute parity, the total load on each of the input lines is 2.67 mA or less. Pin D is at -3 V whenever all three inputs to one or more of the AND gates are negative.

OUTPUTS: Each of the complementary outputs (pins D and E) can drive 10 mA at ground -7 mA at -3 V (-6 mA at pin D when pin F is used). The output is a special emitter follower circuit.

An indicator output (pin F) is provided to drive an indicator driver circuit such as the W012-W250 indicator driver or the W020-4902 indicator driver with lamp.

POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	+4 V to +16 V	49 mA
B	-15 V	-12 V to -18 V	92 mA
C	ground		

APPLICATION: The B130 can be connected to compute either even or odd parity by ORing the appropriate four of the eight possible 3-bit configurations together.

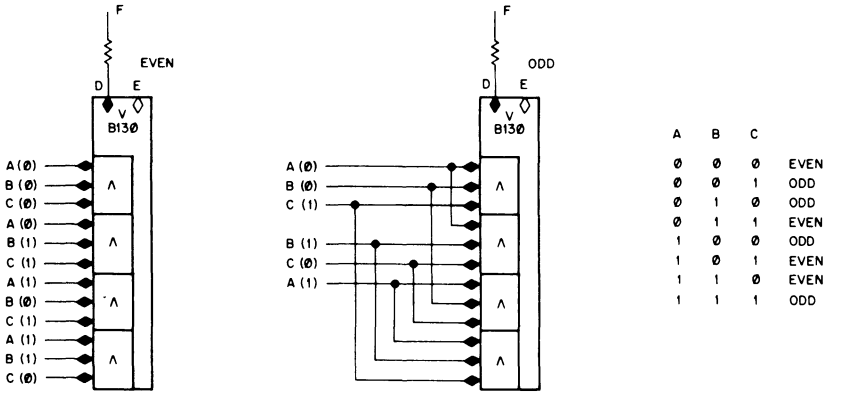
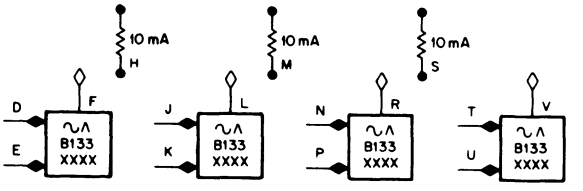


Figure 4-3 B130 Connections, Odd and Even Parity

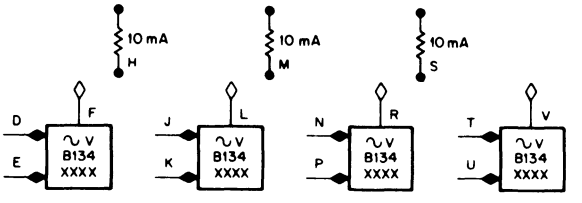
B133, B134, B135, B137, B163, B165, B167, B168 DIODE GATES

Standard Size FLIP CHIP Modules, 18 Pins

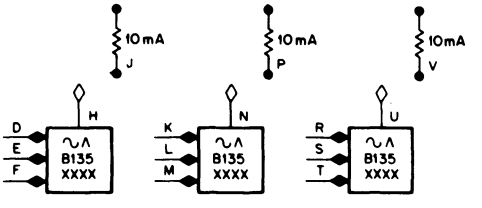
B133



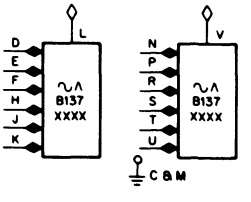
B134



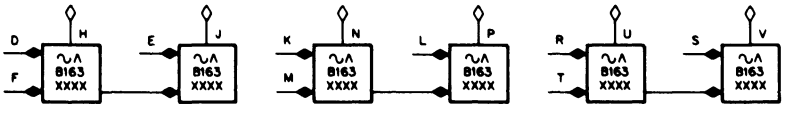
B135



B137

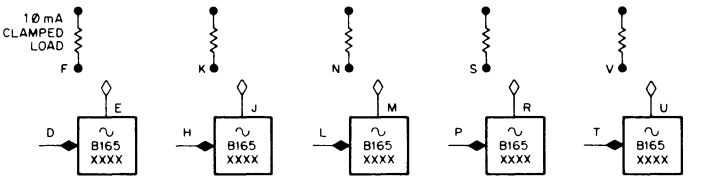


B163

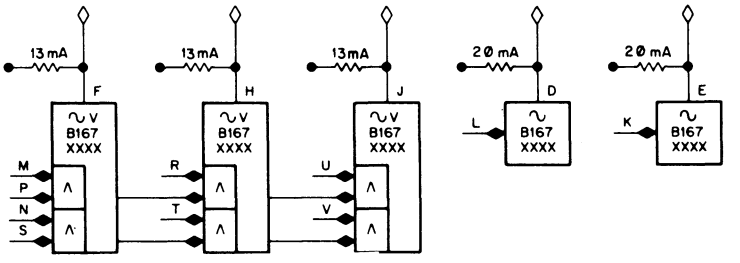


Note: Pins D, E, K, L, R, S include level terminator at input

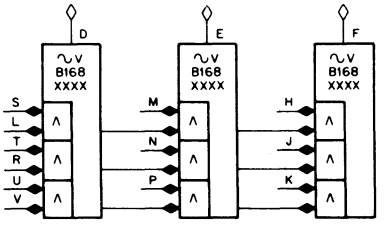
B165



B167



B168



The B-series 2 mA diode gates are used for performing high speed AND/OR gating, register input gating, and general logic use. These gates operate from standard DEC 35 ns or 40 ns negative pulses (0 V to -3 V), provided that adequate fall times are maintained. (See technical notes below). These gates will also operate with standard DEC levels of ground and -3 V. (Pulses 70 ns or wider are considered levels.) Collector outputs are provided in order to allow wired ORing at ground by paralleling outputs of gates. Simultaneous switching of outputs in decoding applications is not guaranteed; ORed outputs may contain spikes.

INPUTS: Each diode gate input is a 2 mA or greater load at ground, shared among the input diodes which are at ground. The loading at ground for all the diode gate inputs is given in Table 4-2. The load at -3 V is less than 1 μA for each diode input.

Table 4-2

Input Loading (at ground)

Module	2 mA	2.7 mA	3.2 mA	4 mA	6 mA	8.1 mA
B133	D and E, J and K, N and P T and U					
B134[1]	D,E,J,K,N,P,T,U					
B135	D and E and F, K and L and M, R and S and T					
B137	D and E and F and H and J and K, N and P and R and S and T and U					
B163	D,E,K,L,R,S[2]			F,M,T		
B165	D,H,L,P,T					
B167	N,M,T,R,V,U		K,L		S,P	
B168		H,J, K, N,M,P, T,U,S				L,R,V

[1]Each input to the B134 is a 2 mA load at ground; there is no load sharing between inputs.

[2]These inputs include a level terminator circuit and should only be used for signals which go from -3 V to ground. Signals which attempt to go above ground (such as B611 outputs) are clamped at ground, and signals which attempt to go below -3 V are clamped at -3 V.

OUTPUTS: Each output of this series of gates can supply up to 26 mA at ground less that required by internal clamped loads. Rise and fall times are listed in Table 4-3.

Fall times for logic levels may increase the effective width of standard pulse inputs, thus limiting the system repetition rate to less than 10 MHz. To calculate fall times, follow the procedure detailed at the beginning of this chapter. The 10 mA clamped loads are adequate to maintain reasonable pulse width and pulse shape through several stages of gating, provided that capacitive loading is small and wire lengths are short. For other conditions, the 35 ns or 40 ns pulses should be regenerated with a pulse amplifier (B602, B611, etc.) after three stages of gating at most. Although these gates will not drive resistive terminators to ground at dc, satisfactory operation over long wires (65 ft, 20 m) can be obtained by terminating the far end of the driven line with a G796 or G704 level terminator.

Table 4-3

Technical Data

Type	Typical Propagation Delay* (ns)	Output Rise TTT Max.* (ns)	Output Fall TTT Max.* (ns)	+10 V (pin A)		-15 V (pin B)	
				Current Required (mA)	Margin Range	Current Required (mA)	Margin Range
B133	13	30	45	0.6	0 V, 20 V	48	-10 V, -20 V
B134	13	30	45	1.2	0 V, 20 V	54	-10 V, -20 V
B135	13	30	45	0.45	0 V, 20 V	44	-10 V, -20 V
B137	13	30	45	0.30	0 V, 20 V	4	-10 V, -20 V
B163	13	30	45	0.90	0 V, 20 V	30	-10 V, -20 V
B165	13	30	45	0.75	0 V, 20 V	68	-10 V, -20 V
B167	13	30	45	1.2	0 V, 20 V	107	-10 V, -20 V
B168	13	30	45	1.3	0 V, 20 V	24	-10 V, -20 V

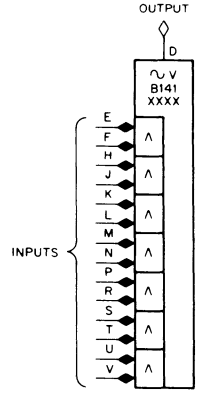
*Test Conditions: Five 2-mA diode gates as load, 10 mA clamped load total, 3 in. of connecting wire, gate under test driven by and driving standard 2 mA diode gates.

Pin C is ground on all modules. Both Pins C and M of the B137 must be grounded.

POWER: Power and margins are listed in Table 4-3. Margins assume 40 ns input pulses from a 2 mA diode gate with a 10 mA clamped load only. Operating margins are broader with wide pulses or with levels. With heavier loads, rise and fall times are longer when the -15 V supply is adjusted toward -10 V due to decreased transistor drive and decreased clamped load current, causing narrower margins.

B141 DIODE GATE

Standard Size FLIP CHIP Module, 18 Pins



The B141 is a 2 mA diode gate used for performing AND/OR functions and register comparisons. It is typically used for register loading and driving I/O bus data lines. The B141 will operate from standard DEC 35 ns or 40 ns negative pulses, provided that adequate fall times are maintained. It will also operate with standard DEC levels of ground and -3 V. (Pulses 70 ns or wider are considered levels.) Repetition rate may be limited to less than 10 MHz by slow fall times.

INPUTS: Input load is 2 mA per input pair shared by the grounded inputs. When any pair is not being used, at least one of the two inputs must be grounded.

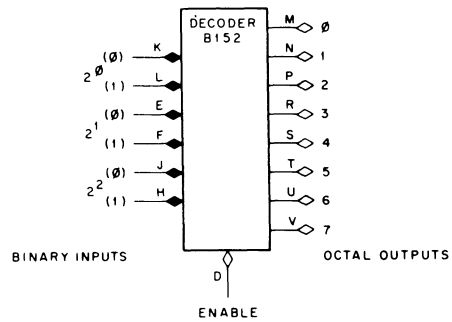
OUTPUT: Standard levels of -3 V and ground. The output can drive 26 mA at ground (30 mA if slower rise and fall is adequate). Rise TTT is 15 ns or less; fall TTT is 50 ns or less. Fall delay is 20 ns or less. No clamped load is provided.

POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	0 V to 20 V	1.3 mA
B	-15 V	-10 V to -20 V	19 mA
C	ground		

B152 BINARY TO OCTAL DECODER

Standard Size FLIP CHIP Module, 18 Pins



This circuit decodes binary information from three flip-flops into octal form. The internal gates, including the enable gate, are high speed B-series 2 mA diode gates. Maximum repetition rate is slightly less than 10 MHz.

INPUTS: Standard levels of -3 V and ground, with pulse widths 40 ns or greater. Each diode gate within the decoder draws 2 mA at ground which is shared among the input diodes which are at ground. The load at -3 V is less than -1 μA for each diode input.

Binary: 4.7 mA or less when used as a decoder.

Enable: 2 mA when at ground. When the enable input is at ground, the selected output line is at ground and the deselected outputs are at -3 V. When the enable input is at -3 V, all outputs are at -3 V.

OUTPUTS: Standard levels of -3 V and ground. Each output can supply 26 mA at ground. A 5 mA or heavier clamped load must be used at each output. Output TTT with respect to binary inputs is 20 ns for rise and 35 ns for fall. With respect to the enable input, output TTT is 40 ns for both rise and fall (with 10 mA clamped loads). Simultaneous switching of outputs is not assured. If outputs are ORed together, the resultant output may contain spikes.

POWER:

Pin	Voltage	Margin Range	Current
A	+ 10 V	0 V to 20 V	1.3 mA
B	-15 V	-10 V to -20 V	19 mA
C	ground		

APPLICATION: In addition to a binary-to-octal decoder, the B152 may be used in any application where the internal gating structure is appropriate. The internal structure is shown below. The B152 is most often used as the PI decoder which drives the PDP-10 I/O bus.

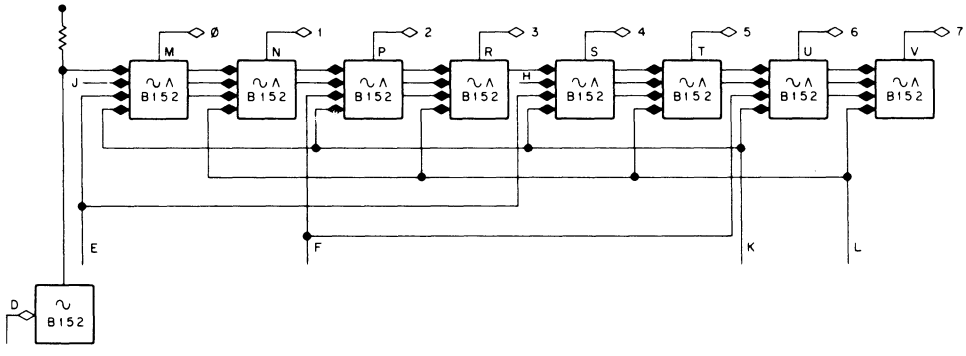
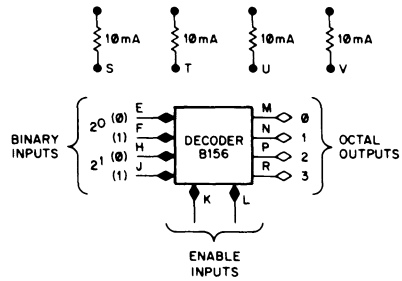


Figure 4-4 Internal Gating Structure, B152 Module

B156 HALF BINARY-TO-OCTAL DECODER

Standard Size FLIP CHIP Module, 18 Pins



The B156 module is used alone as a 2-bit decoder with two enable inputs, or it is used with another B156 to form a full 3-bit (binary-to-octal) decoder, with one combined enable line. Either way, each binary input combination results in one selected output held at ground if the decoder is enabled. No output will be selected if an enable input is held at ground. The decoder consists of four 4-input 2 mA diode gates with appropriate input connections. The B156 is often used as a high-speed decoder for unit-select or instruction-decoding applications.

INPUTS: Standard levels of -3 V and ground, with pulse widths of 40 ns or greater. Each diode gate within the decoder draws 2 mA at ground which is shared among the input diodes which are at ground. When used as a decoder, the binary inputs draw 3 mA or less. When two B156s are used as a full binary-to-octal decoder, the binary inputs draw 4.7 mA or less. The load at -3 V is less than -1 μA for each diode input.

OUTPUTS: Standard levels of -3 V and ground. Each output can supply 26 mA at ground. Output TTT is 30 ns max. for rise and 45 ns max. for fall when driving five 2 mA diode gates, a 10 mA clamped load, and 3 in. of connecting wire. Typical propagation time is 13 ns.

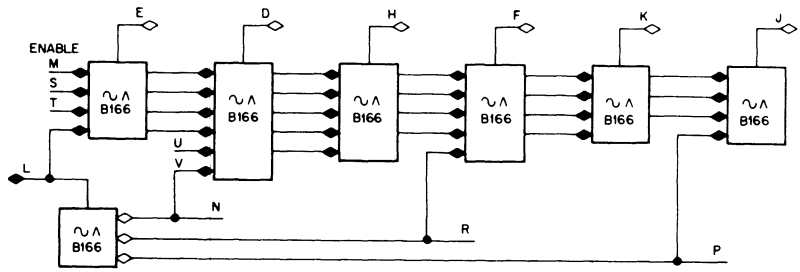
Simultaneous switching of B156 outputs is not assured. It outputs are ORed together, the resultant output may contain spikes.

POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	0 V to 20 V	.6 mA
B	-15 V	-10 V to - 20V	56 mA
C	ground		

B166 COUNTING GATE

Standard Size FLIP CHIP Module, 18 Pins



The B166 provides compact gating to implement an up counter or down counter using delayed flip-flops such as the B212. It is constructed out of 2 mA diode gates and will operate using standard DEC 35 ns or 40 ns negative pulses, provided adequate fall times are maintained. This circuit will also operate with DEC standard levels of -3 V and ground. (Pulses 70 ns or wider are considered levels.)

INPUTS: Each diode gate input is a 2 mA load at ground, shared among the input diodes which are at ground. The inputs to the positive NAND (whose output is pin L) each draw 2 mA at ground independent of the state of the other inputs. The load at -3 V is less than 1 μA for each diode input.

OUTPUTS: Each diode gate output can supply up to 26 mA at ground. Output TTT of each diode gate is 30 ns max. for rise and 45 ns max. for fall. When driving five 2 mA diode gates, a 10 mA clamped load, and 3 in. of connecting wire. Typical propagation time is 13 ns. No internal clamped loads are supplied; external clamped loads must be supplied when necessary (usually for pin L at least).

POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	0 V to 20 V	1.3 mA
B	-15 V	-10 V to - 20 V	18 mA
C	ground		

APPLICATION: Part of a typical up counter arrangement is shown in Figure 4-5. The three-bit section shown includes carry conditions from lower order stages and generates part of the carry condition for succeeding higher order stages. Notice that three input pins (N,R,P) are used for both the 1-high and 0-low states of a flip-flop. This is valid as these two signals are electrically equivalent.

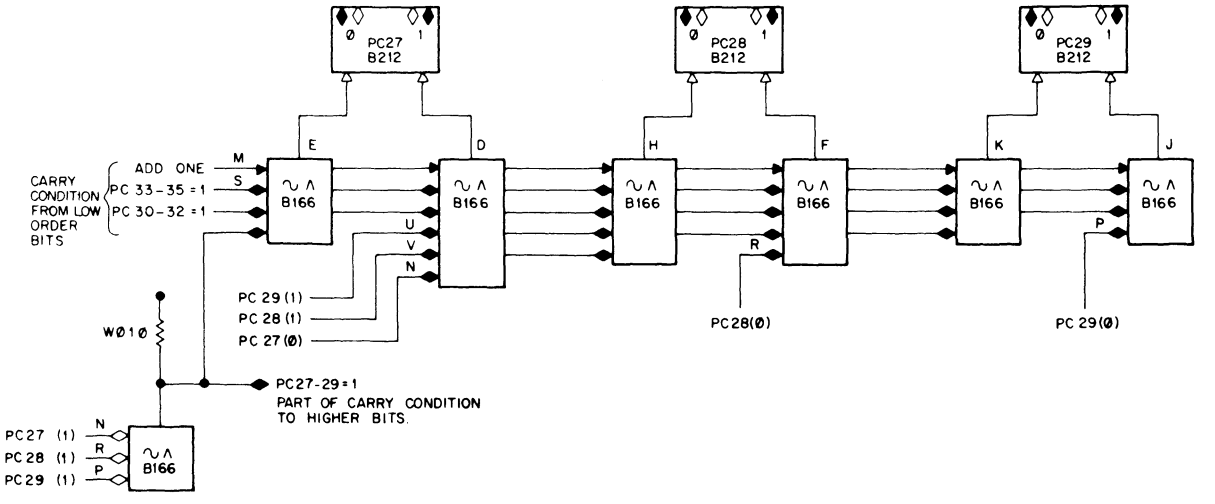
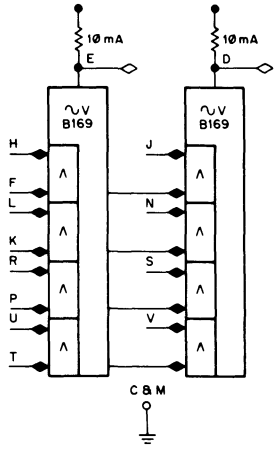


Figure 4-5 Up Counter Arrangement of B166 Module

B169 DIODE GATE

Standard Size FLIP CHIP Module, 18 Pins



The B169 is a 2 mA diode gate used for performing AND/OR functions such as register input gating. The B169 will operate from standard DEC 35 ns or 40 ns negative pulses, provided that adequate fall times are maintained. It will also operate with standard DEC levels of ground and -3 V. (Pulses 70 ns or wider are considered levels.) Repetition rate may be limited to less than 10 MHz by slow fall times.

INPUTS: Input load is 2 mA per input-AND pair shared by the grounded inputs. When any pair is not being used, at least one of the two inputs must be grounded.

OUTPUTS: Standard levels of -3 V and ground. The output can drive 16 mA at ground (26 mA output minus 10 mA clamped load). 22 mA can be driven if slower rise and fall is adequate. The internal clamped load will supply -7 mA at -3 V. Typical TTT is 25 ns for output rise and 30 ns for output fall.

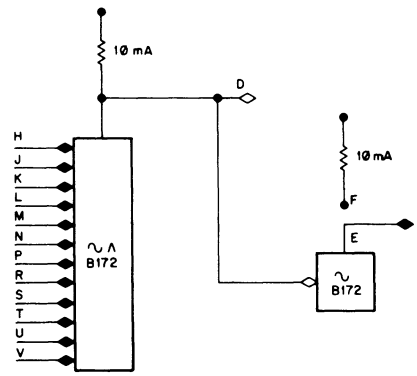
POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	+5 V to +15 V	.8 mA
B	-15 V	-12 V to -18 V	42 mA
C,M	ground		

Both pins C and M must be grounded.

B172 DIODE GATE

Standard Size FLIP CHIP Module, 18 Pins



The B172 provides a 12-input 2 mA diode gate with 2 mA diode inverter permanently connected to the output of the first gate. It is often used for memory module selection on the PDP-10 memory bus.

INPUTS: The input load of the diode gates is 2 mA shared among the inputs which are at ground. Each diode input at ground represents 12 pF of capacitance. The input load at -3 V is less than 1 μA plus 5 pF of capacitance at each input provided at least one input is at ground.

OUTPUTS: Pin D - This output can drive up to seven other 2 mA diode gates (14 mA at ground). The internal clamped load will supply -7 mA at -3 V.

Pin E - This output can supply 26 mA at ground. The output capacitance is 3 pF. A 10 mA clamped load is available at pin F.

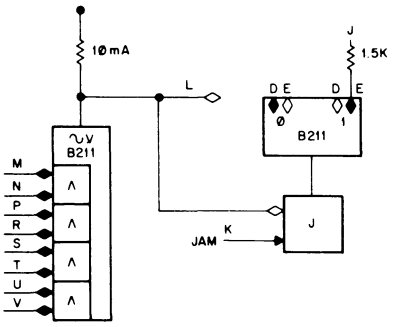
Typical propagation time through the first gate is 15 ns; through both gates, 25 ns. Rise TTT from input is 25 ns to pin D, 40 ns to pin E. Fall TTT from input is 40 ns to pin D, 35 ns to pin E. The output load for pin E is the clamped load at pin F for these measurements.

POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	0 V to 20 V	.3 mA
B	-15 V	-10 V to -20 V	24 mA
C	ground		

B211 JAM FLIP-FLOP

Standard Size FLIP CHIP Module, 18 Pins



The B211 provides a 2 mA diode gate AND/OR circuit driving a jam flip-flop similar to one half of a B213. It is useful as the memory address register of a PDP-10 memory module.

INPUTS: Diode gate - Standard DEC levels of -3 V and ground. Input load is 2 mA per input pair shared by the grounded inputs. When any pair is not being used, at least one of its inputs must be grounded.

Jam - A standard DEC 40 ns or longer negative pulse or a level change greater than -1 V in 12 ns will set or clear the flip-flop. Input load is -5 mA at -3 V and 31 pF. Maximum repetition rate is 10 MHz. Rise and fall TTT from the jam input to the output is less than 40 ns.

Pin L - Standard DEC levels of -3 V and ground. This pin may be used to expand the input capability of the flip-flop. Load at ground is 12 mA (10 mA clamped load plus 2 mA input load). The clamped load will supply -7 mA at -3 V. The input must be settled at -3 V or ground 20 ns before the jam input is pulsed. If pin L is at ground when the jam input is pulsed, pin E will go negative (the flip-flop will be set).

OUTPUTS: Flip-Flop - Standard levels of -3 V and ground. Each output can drive 36 mA at ground. The internally connected clamped load will supply -7 mA at -3 V (-6 mA at pin E when the indicator output is used).

Indicator - A resistor output is provided to drive an indicator driver circuit such as the W012-W250 indicator driver or the W020-4902 indicator driver with lamp.

Pin L - The output of the diode gate may be used to perform additional logic provided that the set up time required above is met. The diode gate will drive 14 mA in addition to the internally connected loads.

POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	+5 V to +15 V	17 mA
B	-15 V	-12 V to -18 V	82 mA
C	ground		

NOTE

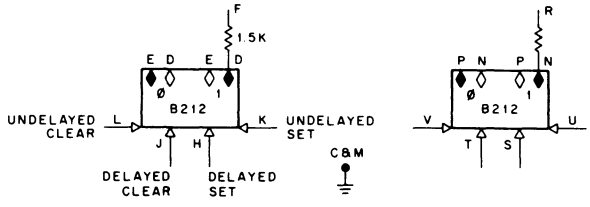
This description applies to B211 flip-flops revision E or later.

CAUTION

The B211 flip-flop may be damaged if its output is grounded when one or more of its inputs is active.

B212 DELAYED FLIP-FLOP

Standard Size FLIP CHIP Module, 18 Pins



The B212 standard size FLIP CHIP module contains two clear-set flip-flops with buffered outputs and individual delayed and undelayed set and clear inputs.

INPUTS: Undelayed - Undelayed inputs must be driven from the collector of a diode gate and require an external clamped load. A total of five B212 undelayed inputs may be driven from one 2 mA diode gate collector if a 5 mA clamped load is used. For driving four or less B212 direct inputs a 10 mA clamped load may be used. Undelayed inputs require 5.5 mA at ground and 0 mA at -3 V. The B212 will operate at 10 MHz; therefore, undelayed input pulses may occur at a 5 MHz repetition rate. The input to the 2 mA diode gate driving the B212 undelayed input should be a standard 40 ns or longer negative pulse. The state of the flip-flop after the simultaneous application of set and clear pulses is undefined.

Delayed - Delayed inputs contain an internal 2 mA clamped load and must be driven from the collector of a diode gate. Two delayed inputs may be driven from the collector of one 2-mA diode gate. The B212 delayed input requires 14 mA at ground for a 35 ns or 40 ns pulse and 2 mA at -3 V. A longer pulse or level is loaded with 22 mA at ground. Maximum repetition rate for any delayed input is 5 MHz. The input to the diode gate driving the delayed input of the B212 must be a standard 35 ns or longer pulse. Output delay time is 40 ns minimum and 60 ns maximum measured from the input of the diode gate driving the delayed input.

OUTPUTS: Logic - Standard ground and -3 V levels. Each output can drive 40 mA of external load at ground and -7 mA at -3V (-6 mA at pin D, N when the indicator output is used). A total of twenty 2-mA diode gates may be driven at 10 MHz provided that the wiring is kept very short.

Indicator Drive - Pins F and R apply the "1-low" output through a 1.5 KΩ resistor to an indicator driver such as the W012-W250 or W020-4902.

POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	2.5 V to 17.5 V	50 mA
B	-15 V	-10 V to -20 V	120 mA
C, M	ground		

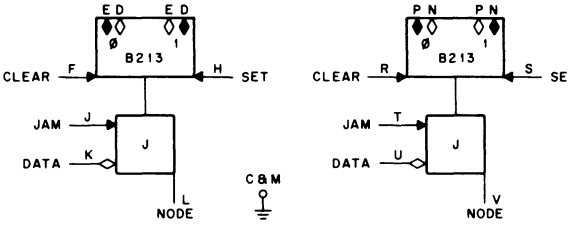
Pins C and M must both be grounded.

CAUTION

The B212 flip-flop may be damaged if its outputs are grounded when one or more of its inputs is at ground. To manually set or clear the flip-flop ground the input.

B213 JAM FLIP-FLOP

Standard Size FLIP CHIP Module, 18 Pins



The B213 provides two jam transfer (C-D) flip-flops. It is often used in combination with the B169 diode gate to form a general purpose register. It is also useful as a complementary bus driver.

INPUTS: Data - Standard DEC levels of -3 V and ground. Input load is 2 mA shared among those inputs (pin K or U and expansion inputs) which are at ground. The inputs must be settled at -3 V or ground 20 ns before the jam input is pulsed.

Node - The node can be used to expand the data input using R001 or R002 diode networks. Short wires must be used between the node and diode networks. If any data input is at ground when the jam input is pulsed, pin D,N will go negative (the flip-flop will be set). If all data inputs are at -3 V, pin E,P will go negative (the flip-flop will be cleared).

Jam - A standard DEC 40 ns negative pulse or a level change greater than -1 V in 12 ns will set or clear the flip-flop. Input load is -5 mA at -3 V and 31 pF. Maximum repetition rate is 10 MHz. Rise and fall TTT from the jam input to the output is less than 40 ns.

Direct Set or Clear - Standard DEC 40 ns negative pulses. Input load is -10 mA at -3 V. The result of pulsing both the set and clear inputs is not defined. The set and clear inputs may be left open when not in use.

OUTPUTS: Standard DEC levels of -3 V and ground. All outputs can drive 36 mA at ground or 2 base loads at 10 MHz. (A base load is -1 mA and 60 pF.) The internally connected clamped loads will supply -7 mA at -3 V.

POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	+8 V to +12 V	32 mA
B	-15 V	-12 V to -18 V	80 mA
C, M	ground		

Both pins C and M must be grounded.

CAUTION

The B213 flip-flop may be damaged if its outputs are grounded when one or more of its inputs is active.

APPLICATIONS: Redefining the B213 output pins provides a jam (C-D) flip-flop with a negative data input. (See Figure 4-6.)

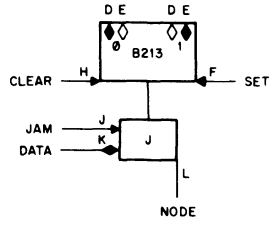


Figure 4-6 B213 With Negative Data Input

The B213 can also be used as a dual complementary bus driver by connecting the jam input to a source of -3 V such as a free clamped load. (See Figure 4-7.)

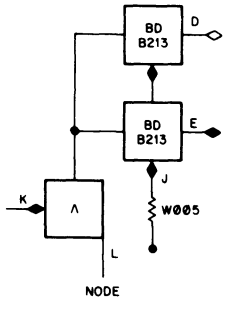
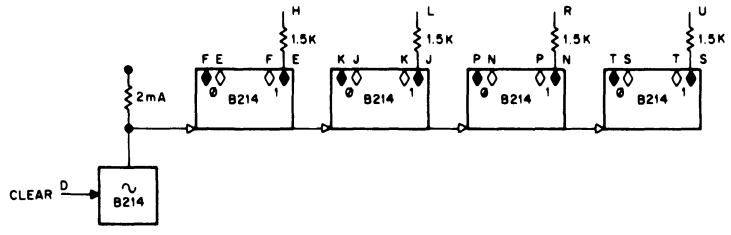


Figure 4-7 B213 As Bus Driver

B214 FLIP-FLOPS

Standard Size FLIP CHIP Module, 18 Pins



The B214 contains four unbuffered flip-flops. The module is pin-compatible with the B204, but has improved noise rejection and a 2 mA diode inverter clear input.

INPUTS: Each flip-flop may be individually set or cleared by grounding the "1-high" or "0-high" output. The collector of a 2 mA diode gate driven by a 35 ns or longer pulse may be used to ground a flip-flop output. Diode gates such as B113, B115, B117, etc., may also be used, but due to their slower operation they must be conditioned "on" for at least 70 ns to provide adequate drive. When switching, the output of the negative-going side must reach -1.4 V to latch the flip-flop. The driving signal must be present until this occurs. A negative level at least 35 ns wide applied to the input of the inverter clears all four flip-flops. Clear input loading is 2 mA at ground. If the clear input of the B214 is allowed to fall, all flip-flops clear. Then if one stage is driven to the 1 state, it holds that state as long as the driving signal is present. However, when the driving signal is removed the flip-flop falls back to the 0 state if the clear signal is still present. If the clear input is not used, it must be grounded.

OUTPUTS: Each flip-flop output can drive 20 mA of external load at ground or -6 mA at -3 V (-5 mA when the indicator output is used). For flip-flops driven by 2 mA diode gates with 35 ns pulse inputs, each side of the flip-flop can be loaded with five 2-mA diode gates and 100 pF.

The 1500 Ω resistor outputs allow an indicator driver circuit such as the W012-W250 or W020-4902 to be used. The wire to the W012 or W020 should be short.

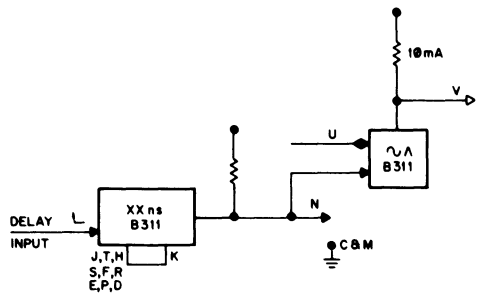
POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	0 V to 20 V	0.6 mA
B	-15 V	-8 V to -20 V	50 mA
C,M,V	ground		

Pinc C,M, and V must all be grounded.

B311 TAPPED DELAY LINE

Standard Size FLIP CHIP Module, 18 Pins



The B311 consists of a tapped delay line with suitable buffering and a connected 2 mA diode gate. Delay time is selected by connecting pin K to a delay line tap. (See delay control below.) This module has the same pin connections and can be used in the same slot as the B312 variable delay line module.

INPUTS: Delay Input - The standard input to pin L is a negative 35 ns pulse from a B611 PA. Loading is equivalent to a 75-Ω resistance in series with a 68 pF capacitance. For levels, the static input load is -7 mA at -3 V, 0 mA at ground, dynamic load is negligible. The input may be driven by a clamped load drawing 10 mA at ground. The B311 may be driven by a 2-mA diode gate with clamped load, but pulses will tend to become wider than normal.

Gate Input - Standard levels of -3 V and ground. Loading is 2 mA shared by the gate inputs at ground, 0 mA at -3 V. The gate is a 2 mA diode gate.

OUTPUTS: When the delay input is driven with 35 ns negative pulses, output N delivers negative pulses with no overshoot (ground to -3 V) from 50 to 70 ns wide at the -1.0 V points. If pin U is at -3 V, pin V delivers positive pulses (-3 V to ground) of the same width.

Pins N and V each drive 22 mA at ground in addition to the clamped loads and other gates tied internally. Each clamped load drives -7 mA at -3 V.

DELAY CONTROL: The delay time is selected by connecting pin K to delay tap pins D, E, F, H, J, P,R, S, T of the same B311 card. No other use for pin K is intended. The wire from pin K to the tap should be as short as possible.

The delay from pin L to pin N measured at the -1 V point on the waveforms can be predicted by the formula:

$$\text{L to N delay} = \text{tap delay} + 16 \pm 3 \text{ ns}$$

where the tap delay is from the table below.

Pin K connected to Pin	Tap Delay
J	50 ns
T	75 ns
H	100 ns
S	125 ns
F	150 ns
R	175 ns
E	200 ns
P	225 ns
D	250 ns

The delay from pin N to pin V at the -1 V point depends on the loads at pin N and pin V, but for a fanout of 2 or less from pins N and V and wire runs less than 3 in., 9 to 12 ns delay is typical.

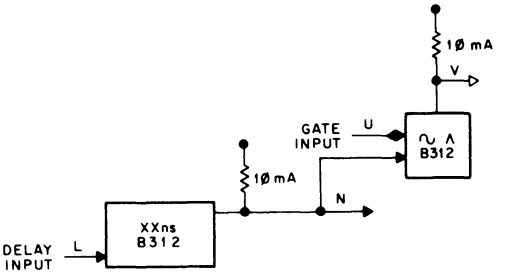
POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	+2.5 V to +20 V	10 mA
B	-15 V	-10 V to -20 V	56 mA
C, M	ground		

Pins C and M must both be grounded.

B312 ADJUSTABLE DELAY LINE

Standard Size FLIP CHIP Module, 18 Pins



The B312 is an adjustable delay line with suitable buffering driving a standard 2 mA diode gate. The delay is set by a screwdriver adjustment accessible from the handle end. This module has the same pin connections and can be used in the same slot as the B311 tapped delay line module.

INPUTS: Delay Input - The standard input is a negative 35 ns pulse from a B611 PA. Loading is equivalent to a 250-Ω resistance to ground. For levels, the static input load is -12.5 mA at -3 V, 0 mA at ground; dynamic load is negligible. The input may be driven by a clamped load drawing 15 mA at ground. The B312 may be driven by the output of a 2 mA diode gate with clamped load, but pulses will tend to become wider than normal.

Gate Input - Standard levels of -3 V and ground. Loading is shared by the gate inputs at ground, 0 mA at -3 V. The gate is a 2 mA diode gate.

OUTPUTS: When the delay input is driven with 35 ns negative pulses, output N delivers negative pulses with no overshoot (ground to -3 V) from 40 to 80 ns wide at the -1 V points. If pin U is at -3 V, pin V delivers a positive pulse (-3 V to ground) of the same width.

Pins N and V each drive 22 mA at ground in addition to the clamped loads and other gates tied internally. Each clamped load drives -7 mA at -3 V.

DELAY CONTROL: The delay from pin L to pin N, measured at the -1 V on the waveforms, can be adjusted from 20 ns to 215 ns. The delay from pin N to pin V at the -1 V point depends on the loads at pin N and pin V, but for a fanout of 2 or less from pins N and V and wire runs less than 3 in., 9 to 12 ns delay is typical.

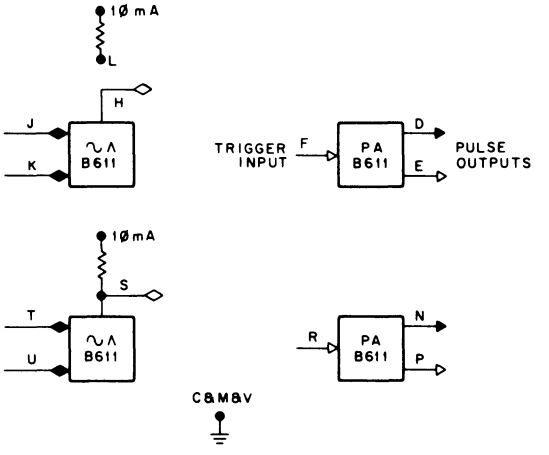
POWER

Pin	Voltage	Margin Range	Current
A	+10 V	+2.5 V to +20 V	4.7 mA
B	-15 V	-10 V to -20 V	34.4 mA
C, M	ground		

Pins C and M must both be grounded.

B611 PULSE AMPLIFIER

Standard Size FLIP CHIP Module, 18 Pins



The B611 contains two independent 10 MHz 35 ns pulse amplifiers for power gain and pulse standardization. Two 2-input diode gates increase the logic flexibility.

INPUTS: Gate Inputs - Input load is 2 mA shared by the grounded inputs of each gate. Load at -3 V is less than 1 μA.

Trigger Inputs - The input to each pulse amplifier is a diode gate which is a 1 mA load at ground and no load at -3 V. The PA is triggered by positive-going pulses or level transitions (-3 V to ground) which are 25 ns or wider at the -1.5 V point at the PA input. The PA produces output pulses for any spacing of input pulses above a minimum of 100 ns provided that the input is at -3 V for at least 50 ns before going to ground. The PA may be driven by any circuit which meets the above requirements. Gates may be collector ORed at the PA input provided that the wiring is kept short, stray capacitance is minimized and the above rules are followed. Up to four PA inputs may be driven from one diode gate collector.

OUTPUTS: Gate Outputs - The diode gate output at pin S has a 10 mA clamped load connected internally and therefore can supply 16 mA drive at ground and -8 mA at -3 V. The diode gate output at pin H has no internal clamped load and therefore can supply 26 mA at ground and no current at -3 V. A 10 mA clamped load is available at pin L. These diode gates are suitable for driving the B611 PA input.

Pulse Outputs - The PA output is from the secondary of a transformer so that positive or negative pulses are available by grounding the appropriate pin. The PA output is capable of driving eighteen 2-mA diode gate loads if careful consideration is given to the wiring and termination. In general, a 100-Ω termination at the last gate in the line provides the proper termination but each case should be examined to see if that is adequate. See the wiring guidelines in Chapter 11 for details. For a negative pulse output (pin E or P grounded), the pulse width is 30 to 40 ns measured at the -1.5 V point, the output amplitude is -3 V, delay from PA input to output is 20 ns or less, and the transformer backswing is +4 V, all of which are measured at the PA output. Corresponding values apply to a positive pulse output. There is approximately 1 ns additional delay through the PA for each diode gate collector that is ORed at the PA input.

NOTE

Transistors with low BV_{cbo} should not be driven by negative pulses from the B611. The +4 V backswing from a negative pulse may cause breakdown.

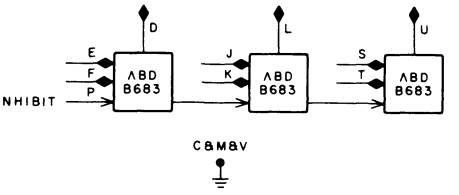
POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	0 V to 20 V	0.66 mA
B	-15 V	-10 V to -20 V	134 mA
C,M,V	ground		

Pins C, M, and V must all be grounded. One side of each pulse transformer output used must be grounded (D or E, N or P).

B683 BUS DRIVER

Standard Size FLIP CHIP Module, 18 Pins



The B683 is the level counterpart of the W102 pulsed bus transceiver. It is designed to drive two 100 Ω transmission lines terminated to ground in their characteristic impedance. A single, terminated 50 Ω transmission can be driven instead. The output impedance of the B683 is zero when the output is low (-3 V) and infinite when high (ground) or when the power is off. Thus, two or more of these drivers may be attached to the same line in a "wired OR" fashion.

INPUTS: The input is that of a two input 2 mA diode AND gate. When both inputs are low, the output is also low. The input load is 2 mA shared by those inputs at ground, 0 for those inputs at -3 V.

An inhibit input is provided on pin P. If this input is held at ground (for example, by the CROBAR relay contact on the 844 Power Control possibly through an isolating diode) power-on, power-off transients are prevented from causing the outputs to go negative. This input normally is at -5.3 V and must not be tied to any other potential if normal operation is expected. Load is 30 mA at ground.

OUTPUTS: The outputs will supply -60 mA to a 50 Ω load at -3 V. The output circuit will tolerate short circuit operation for a short time (tens of seconds) but this type of operation is not recommended. Typical TTT is 30 ns.

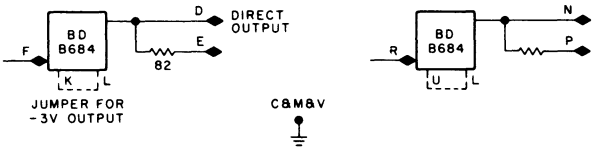
POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	0 V to 20 V	.4 mA
B	-15 V	-12 V to -18 V	350 mA
C,M,V	ground		

Pins C, M, and V must all be grounded.

B684 BUS DRIVER

Standard Size FLIP CHIP Module, 18 Pins



The B684 contains two dual-purpose, non-inverting bus drivers. Each bus driver provides standard DEC levels of -3 V and ground to a large number of diode gates and "inverter base loads" (an inverter base load is a load of -1 mA at -3 V and 60 pF). Alternatively, the bus driver will drive a terminated cable of 90 Ω characteristic impedance.

INPUTS: Standard levels of -3 V and ground. Load is -1 mA at -3 V, 0 mA at ground. Input wiring must be kept relatively short (less than 3 ft).

OUTPUTS: Direct - Standard levels of -3 V and ground. The direct output will drive +40 mA at ground and -80 mA at -3 V. A 100 Ω cable terminated at each end by 100 Ω resistors to ground can be driven by this output. The level control pins must be jumpered when the direct output is used.

Resistor - Levels of ground and -6 V at the resistor output provide standard ground and -3 V levels at the end of a 93 Ω cable terminated with 100 Ω to ground. The terminated cable will drive ±10 mA at 10 MHz. The level control pins must be left open when driving terminated cable from the resistor output.

For driving 5 mA loads or less, an unterminated cable or open wire may be driven from the resistor output using ground and -3 V levels. This connection allows heavy local load and light distant loads on one circuit.

Typical delay through the bus driver is 30 ns.

The output can be held at approximately ground, independent of the input and of power-on, power-off transients, by bringing the level control pin (K,U) to ground with the CROBAR relay contacts of an 844 Power Control (possibly through an isolating diode). Approximately 50 mA is required.

POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	+6 V to +20 V	80 mA [1]
B	-15 V	-12 V to -18 V	120 mA [2]
C,M,V			

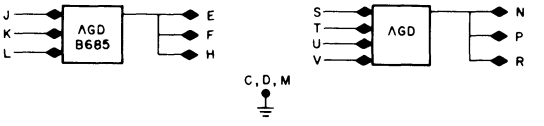
Pins C, M, and V must all be grounded.

[1] Plus the current required to bring the loads to ground.

[2] Plus the current required to bring the loads negative.

B685 DIODE GATE DRIVER

Standard Size FLIP CHIP Module, 18 Pins



The diode gate driver circuit consists of a diode AND gate controlling a current-mode switch, the output of which is buffered with a complementary emitter follower of asymmetric drive capability. Both circuits are identical except one diode AND gate has four inputs while the other has three. Both circuits are non-inverting.

INPUTS: The input load shared by the diode inputs is 2.5 mA at ground and 0 mA at -3 V. The capacitive load of each input is 11 pF at ground and 4.5 pF at -3 V. Propagation delay is about 20 ns.

OUTPUTS: Each output circuit drives up to 36 2-mA diode gates (or 80 mA) at ground, and sinks up to 8 mA at -3 V. There are three pins per output. The output load should be split among the three pins to allow adequate signal transmission. See the wiring guidelines in Chapter 11 for details. Each output has a separate pin brought out for grounding.

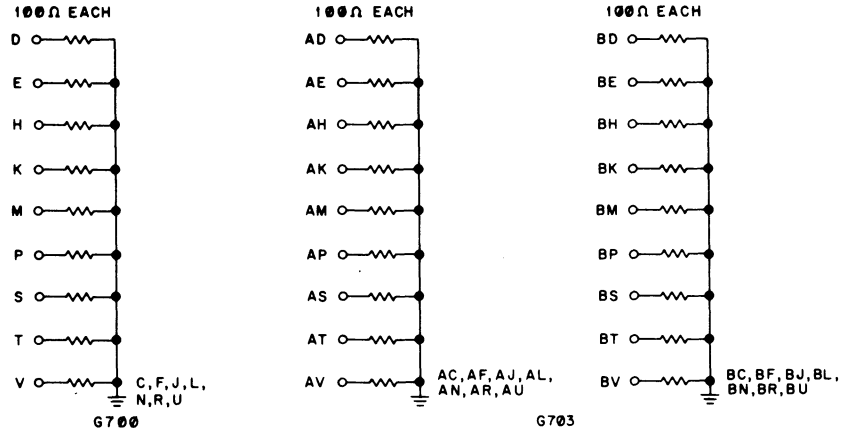
POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	+6 to +16 V	65 mA
B	-15 V	-10 V to -20 V	100 mA
C,D,M	ground		

Pins C,D, and M must all be grounded.

G700, G703 100 Ω TERMINATORS

Standard Size FLIP CHIP Module, 18 Pins.



The G700 provides nine 100 Ω resistive terminators for use in terminating standard 9-circuit cables such as W021 cable assemblies. It is designed to plug into the same module locations as the cable assembly facilitating future extension of the cable. A typical application is the termination of the PDP-10 memory bus in the MB10 memory. The G700 is also useful for terminating transformer-coupled pulse-amplifier outputs such as are found on the B611. Details of pulse amplifier termination are provided in Chapter 11.

The G703 is a double width FLIP CHIP module with 36 pins. It provides 18 100-Ω resistive terminators for use in terminating standard dual 9-circuit cables such as W851 cable assemblies. The G703 is notched to fit in a module location which has been provided with nylon cable retaining blocks such as the H003 or H004, which hold BC09A and BC10A FLIP CHIP cables to module blocks. Thus, the G703 can be used to terminate a bus by plugging it into the same location that future bus extension cables plug into.

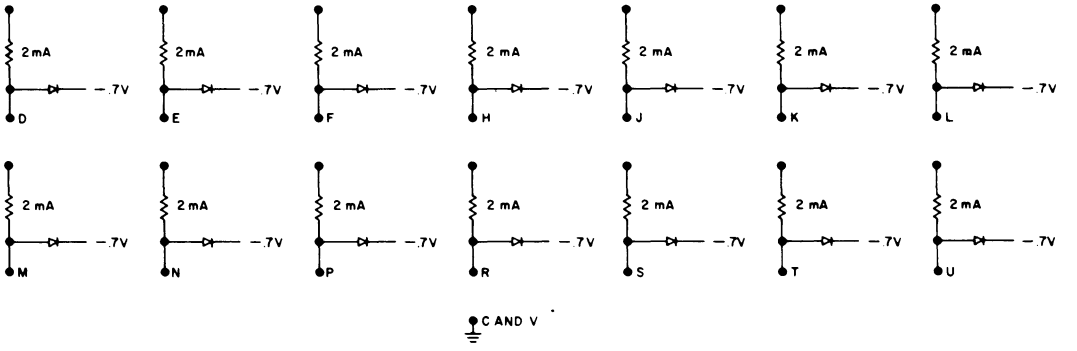
INPUTS: Each input pin has a 100 Ω ±10% 1/4 W carbon resistor to ground.

GROUNDS: All ground pins must be grounded. The "A" and "B" ground buses of the G703 are not internally connected.

POWER: No power is required. Power connections to pins A and B (G700) or AA, AB, BA and BB (G703) are optional. These pins are not connected to anything internally.

G704 2 mA LEVEL TERMINATOR

Standard Size FLIP CHIP Module, 18 Pins



The G704 provides fourteen 2-mA level terminator circuits; that is, level terminator circuits combined with 2 mA clamped loads. It is used to control overshoots and ringing on long or heavily loaded level lines as described in the wiring guidelines (Chapter 11).

INPUTS: Each circuit will prevent the signal to which it is connected from going below -3 V (-3.5 V) and from going above approximately ground. Thus, it can be used only on signal lines which have standard DEC levels of -3 V and ground. The clamped load draws 2 mA at ground and will supply -1.6 mA at -3 V.

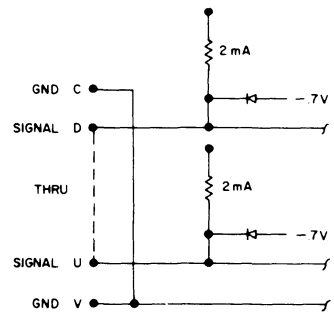
POWER:

Pin	Voltage	Margin Range	Current
A	not used - connection optional		
B	-15 V	-7.5 V to -20 V	60 mA
C,V	ground		

Pins C and V must both be grounded.

G796 LEVEL TERMINATING CABLE CONNECTOR

Standard Size FLIP CHIP Module Without Handle, 18 Pins



The G796 cable connector provides an end for 14 circuit cables formed from 2 flat, flexible cables made of Flex Print or Tape Cable. A 2 mA level terminator (level terminator plus 2 mA clamped load) is connected to each signal line to control overshoot and ringing as described in Chapter 11. Only signals using DEC standard levels of -3 V and ground can be transmitted through this cable. All signal lines are separated by at least one grounded line in the cable to reduce cross-talk.

SIGNAL CIRCUITS: Circuits suitable for transmission of DEC standard levels of -3 V and ground are available at pins D, E, F, H, J, K, L, M, N, P, R, S, T, and U. Load is 4 mA at ground (2 mA at each end). -3.2 mA is supplied at -3 V to discharge capacitance.

POWER: (at each end of the cable)

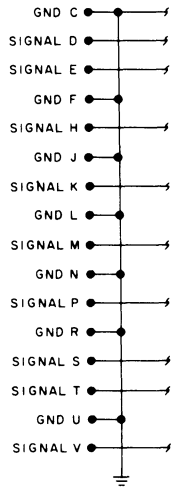
Pin	Voltage	Margin Range	Current
A	not used - connection optional		
B	-15 V	-7.5 V to -20 V	60 mA
C,V	ground		

Pins C and V must both be grounded.

CABLE: The G796-G796 Tape Cable assembly is available as DEC part number 7005469. The length must be specified. Length is measured from the back end (handle end) of each cable connector.

G799 30 Ω CABLE CONNECTOR

Short (3.25 in.) FLIP CHIP Module Without Handle, 18 Pins



The G799 cable connector provides an end for standard 9-circuit cables made with 3 tape cables cemented together. The 30 Ω impedance achieved by paralleling these 100 Ω tape cables allows full utilization of the output capabilities of the B611 Pulse Amplifier and similar high output deive circuits. See the wiring guidelines in Chapter 11 for details of usage.

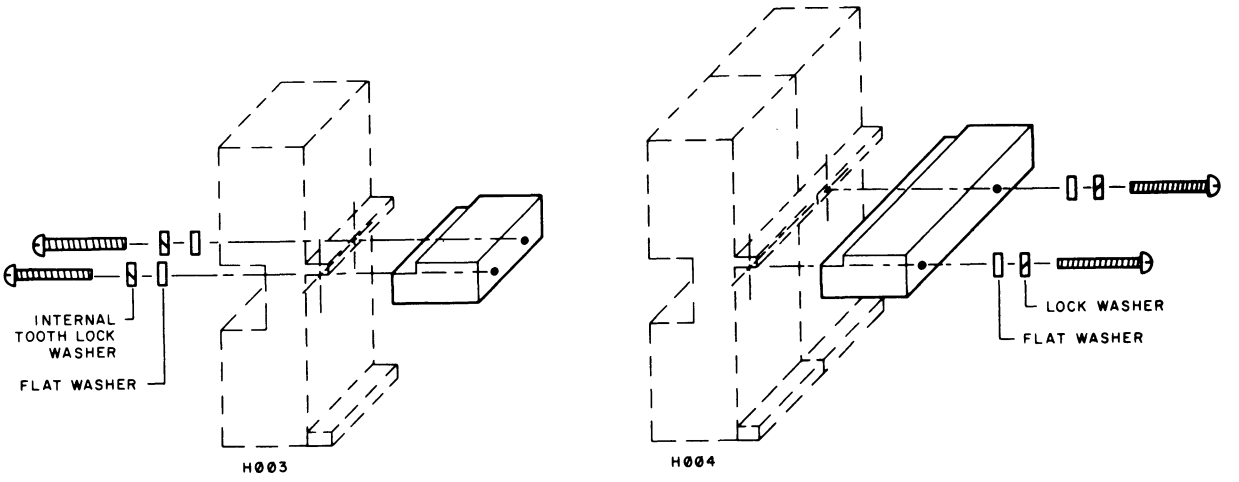
SIGNAL CIRCUITS: Circuits suitable for transmission of 35 ns or longer pulses or levels are available at pins D, E, H, K, M, P, S, T, and V.

POWER: No power is required. Connections to pins A and B are optional.

Pins C, F, J, L, N, R, and U are connected together internally and must all be grounded externally.

CABLE: The G799-G799 Cable Assembly is available as DEC part number 7005463. The length must be specified. Length is measured from the back (handle end) of each cable connector. The bend radius of the cable should not be less than 2 in.

H003, H004 CONNECTOR RETAINING BLOCK KITS

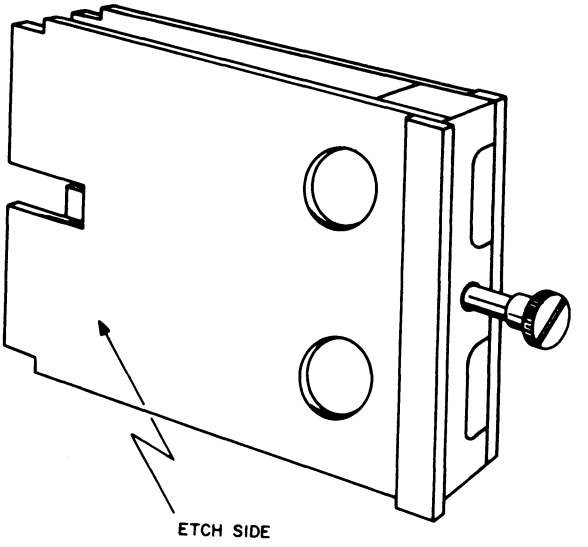


The H003 and H004 Connector Retaining Block kits are hardware kits which provide a connector retaining block to hold H350 series cable connectors and BC09A, BC10A and other compatible cable assemblies to H800 connector block (shown in phantom) such as are used in the H900 and 1943 mounting panels.

The H003 spans one H800 connector block and allows two cables to be plugged in.

The H004 spans two H800 connector blocks and allows four cables to be plugged in.

All necessary hardware and installation instructions are furnished with each kit.



The H351 and H352 are cable connector assemblies suitable for plugging into a H800 connector block equipped with H003 or H004 retaining blocks. They may also be plugged into H800 connector blocks but this will not take advantage of the hold-down screw provided.

The H351 consists of two W851 level terminating connector modules together with appropriate cable clamping and joining hardware. The signals transmitted must be DEC standard levels of -3 V and ground.

The H352 consists of two W852 non-terminating connector modules together with appropriate cable clamping and joining hardware. Any signal levels may be transmitted through this connector.

Either connector assembly will accommodate either four 9-conductor coaxial cables as used in the BC10A, or any cable of a similar diameter. Split lugs are provided on the connector module boards for soldering on signal conductors and their associated ground conductors.

SIGNAL CIRCUITS: Signal circuits are arranged as four standard 9-circuit configurations. Signal pins are D, E, H, K, M, P, S, T, and V of each of the four module locations occupied. The connector occupies the left or right half of a single H800 module connector block.

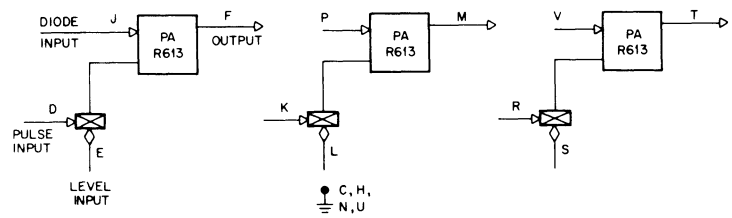
POWER: The H352 requires no power. Connections to pins A and B of any module location occupied is optional.

The H351 requires -15 V at 37 mA on pin B of each module location occupied. Margin range is -7.5 V to -20 V. No +10 V power is used and connections to pin A are optional. The H351 will not adversely affect signal transmission when its power source is turned off but it will not provide level termination in that condition.

Pins C, F, J, L, N, R, and U of every module location occupied must be grounded for either the H351 or H352.

R613 PULSE AMPLIFIER

Standard Size FLIP CHIP Module, 18 Pins



The R613 is pin compatible with and functionally similar to the R603.

Each pulse amplifier produces a 200 ns R-series (positive) pulse. A DCD gate and a diode input permit considerable flexibility. Input pulses can occur at any rate up to 2 MHz. Delay through the pulse amplifier is typically 50 ns.

INPUTS: DCD Gate Level - DEC standard levels of -3 V and ground. The DCD gate is enabled by a ground level and disabled by a -3 V level. The conditioning level must be present for at least 200 ns before the gate is pulsed. The level input represents 2.5 mA of load at ground and 0 mA at -3 V. The level input is prevented from going above ground by a diode clamp.

DCD Gate Pulse - 40 ns or longer pulses going from -3 V to ground at any repetition rate up to 2 MHz. It can also be driven by positive going level changes (-3 V to ground) with rise times of 60 ns maximum and durations of 40 ns minimum. The input must have been at -3 V for at least 200 ns prior to operation of any input. The pulse input represents 5 mA of load at ground, 0 mA at -3 V. The pulse input is prevented from going above ground by a diode clamp.

Diode - DEC standard levels of -3 V and ground. 40 ns or longer pulses or positive going level changes (-3 V to ground) with a rise time of 60 ns maximum will trigger the PA. The input must be returned to -3 V for at least 400 ns before another input is allowed to trigger the PA from either the DCD gate or diode input. The output produced by a ground level at the diode input will be at ground for 200 ns or as long as the input is at ground, whichever is longer. This feature can be used to apply a dc clear to flip-flops during an initial power-up period and also to apply clear pulses during normal operation. The diode input represents a 1 mA load at ground.

OUTPUTS: Outputs are positive pulses (-3 V to ground) of from 190 ns to 350 ns duration or levels (see diode input above). Each output can supply 65 mA at ground. The internal clamped load supplies -3.5 mA at -3 V. Output pulses may be ORed by paralleling PA outputs. The outputs are buffered so that the PA cannot be triggered by noise on the output line (or by another gate or PA). Pulse lines and grounds should be kept as short as possible.

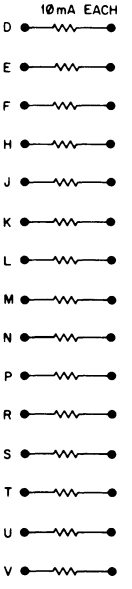
POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	+8 V to +12 V	3.3 mA
B	-15 V	-12 V to -18 V	77 mA
C,H,N,U	ground		

Pins C,H,N, and U must all be grounded.

W010 CLAMPED LOADS

Standard Size FLIP CHIP Module, 18 Pins



The W010 is pin compatible with the W002 and W005 clamped loads. It contains fifteen 10 mA clamped loads.

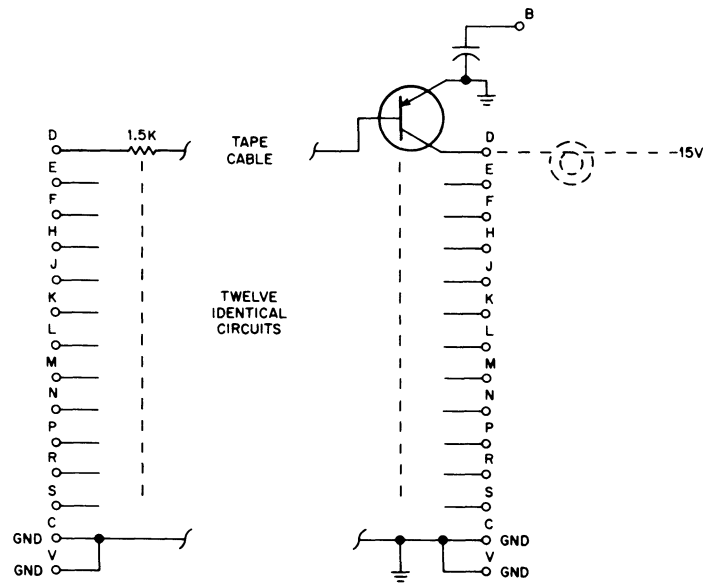
OUTPUTS: Each clamped load draws 10 mA at ground and can supply -7 mA at -3 V.

POWER:

Pin	Voltage	Margin Range	Current
A	Not Used	Connections are optional	
B	-15 V	-7.5 V to -20 V	180 mA
C	ground		

W012 - W250 INDICATOR DRIVER WITH CABLE

Short (3.25 in.) FLIP CHIP Module, Without Handle, 18 Pins (W012)
Standard Size FLIP CHIP Module, 18 Pins (W250)



The W012 - W250 indicator driver consists of a W012 indicator connector and a W250 connector lamp driver connected with Flex Print or Tape Cable. The W012 serves to isolate cable capacity from the logic signals. The W250 will drive 12 lamps returned to -15 V as found on the PDP-10 indicator assemblies provided in the GP10. Locating the lamp driver at the indicator assembly keeps the large indicator currents away from the logic wiring.

INPUTS: DEC standard levels of -3 V and ground or the indicator outputs of modules such as the flip-flop in the 1 state turns on the indicator drive. Input load at -3 V is less than 1/40th of the lamp current. No input current is required at ground. For the 40 mA lamps usually used, the input load is less than 1 mA. The circuit will function with either 1.5 kΩ or 3 kΩ indicator outputs of flip-flops and similar circuits.

OUTPUTS: Each circuit will drive a 40 mA lamp returned to a negative voltage not to exceed -20 V. If an input is driven from -3 V directly (rather than an indicator output) the corresponding output will drive an 80 mA lamp.

POWER: No power is required by the W012 or W250. However, the lamp current (up to 960 mA steady state, 2 A transient) must be supported by the ground connections to the W250. Pins C and V of the W250 must be grounded. Connections to pins A and B of either module are optional. Pin B of the W250 should be connected to -15 V to take advantage of the filter provided. The ground

connection carried from pin C and V of the W012 to the W250 is not meant to carry the lamp current and should not be used for this purpose. Grounding pins C and V of the W012 is optional.

The lamp current is drawn from the -15 V supply by the indicator assembly itself.

CABLE: The W012 - W250 Tape Cable assembly is available as DEC part number 7005459. The length must be specified. Length is measured from the back end (handle end) of each connector module.

W020 INDICATOR CABLE CONNECTOR

Standard Size FLIP CHIP Module, 18 Pins

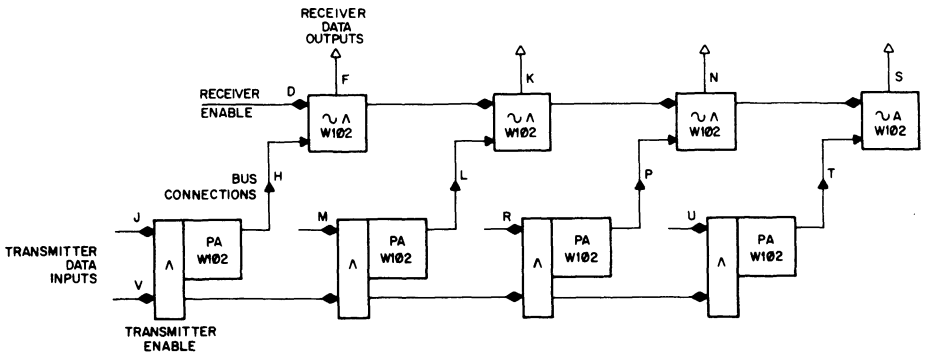
The W020 provides 18-line ribbon cable connections to FLIP CHIP mounting panels. Each connection is through a 1.5 kΩ resistor. The W020 is normally used with an indicator with an amplifer such as the 4902 or 4903 to provide indication of flip-flop states or other logic conditions. When used in this manner, the indicator cable capacity is isolated from the logic signal. When connected to the indicator output of a B130, B211, B212, B214 or similar module, -1 mA of base drive is supplied to the indicator amplifier when the logic signal is at -3 V. There is no load on the logic signal when it is at ground. When the W020 is driven directly from a logic signal (not an indicator output), -2 mA of base drive is available to the indicator amplifier.

POWER: No power and no grounds are required by the W020. Pins A, B, and C are available for use as signal connections.

CABLE: The W020 is available with or without ribbon cable attached. With ribbon cables it is ordered as W020-XXR where XX is the number of inches of ribbon cable attached. When ribbon cable is not desired, order W020U.

W102 PULSED BUS TRANSCEIVER

Standard Size FLIP CHIP Module, 18 Pins



The W102 module is a pulsed bus transceiver capable of communicating with the PDP-1-D, PDP-6 and the PDP-10 memory bus system.

INPUTS: Transmitter Inputs - 2 mA per circuit shared between the grounded inputs; 2 mA maximum for data inputs; 8 mA maximum for the enable input. No load at these inputs at -3 V.

Receiver Inputs - 2 mA per circuit shared between the grounded input. No load at -3 V. The receiver pulse input is tied to the transmitter output, hence internally the pulsed bus. The bus is loaded by 2 mA at ground when the enable input is negative. The enable input draws 8 mA maximum at ground. The receiver gate is a modified diode gate with additional noise rejection at ground.

OUTPUTS: Transmitter Outputs - This module is designed to drive a single 50 Ω cable or two 100 Ω cables. Cables must be terminated in their characteristic impedance so that the load at the transmitter output is 50 Ω. The output pulse is 100 ns nominal width (100 to 125 ns at nominal supply voltage) and -3 V in amplitude, with no positive overshoot. A pulse is produced whenever both inputs to a transmitter circuit are negative. Either the transmitter inputs or the enable input may be pulsed. The input pulse must be at least 30 ns wide and should not occur more often than 400 ns (2.5 MHz maximum repetition rate). Input pulses or levels that are longer than 100 ns make the output pulse up to 15% longer than for a minimum width input pulse.

Receiver Outputs - The receiver outputs are pulled to ground whenever the receiver enable is at -3 V and the bus is pulsed (whether by the same module or by some other source). The outputs should be used with a clamped load to drive additional diode logic or to set unbuffered flip-flops via their collectors. The receiver outputs should not be used to gate emitters as the upper level is too negative to insure adequate noise rejection. ORing of the receiver with other collectors at ground is allowable. The receiver output will suppy 29 mA at ground.

TECHNICAL NOTES: The W102 does not adversely affect the pulsed bus operation even though its power supplies are turned off.

When connecting a large number of transceivers (10 or more) to a bus, the upper (ground) level of the bus is pulled down by the receiver idle current (approximately 2 mA per enabled receiver). To compensate for this effect, the 100 Ω (or 50 Ω) terminating resistors can be returned to a slightly positive voltage (not more than +1.5 V) to make the bus rest at ground. A diode should be connected so that the bus itself will not go above +0.7 V. The bias supply should be thoroughly bypassed to ground. When only one or two receivers are enabled at a time, this scheme is not necessary.

The wires connecting the W102 to the transmission line should be as short as possible; these lines carry large signals at high impedances and are subject to cross-talk. The transmission line is defined as the path of wire from the "left end" terminator (through many cabinets and much cable) to the "right end" terminator.

POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	0 V to +20 V	0.6 mA
B	-15 V	-8.5 V to -23 V	85 mA (26 mA at low duty factor)
C	ground		

NOTE

This description applies to modules revision F or later.
For information on earlier modules contact DEC.

APPLICATION: Typical connections of the W012 are shown in the Figure 4-8.

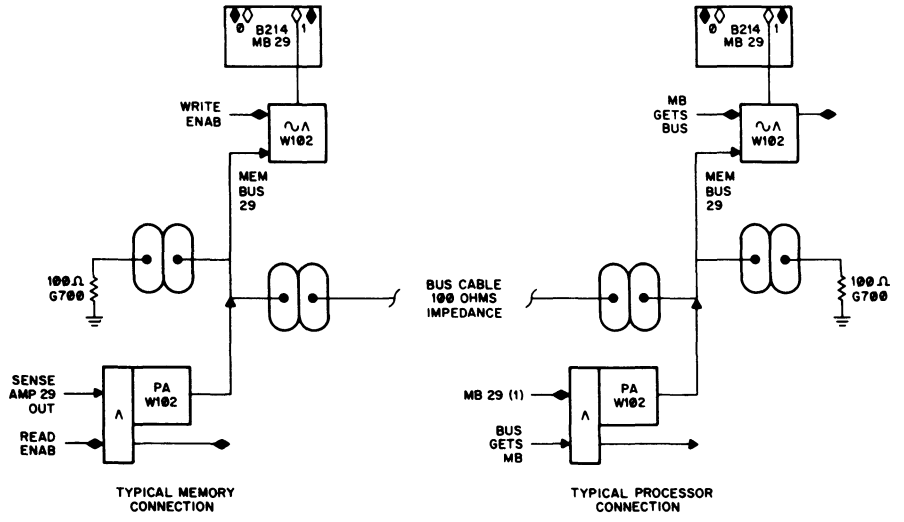
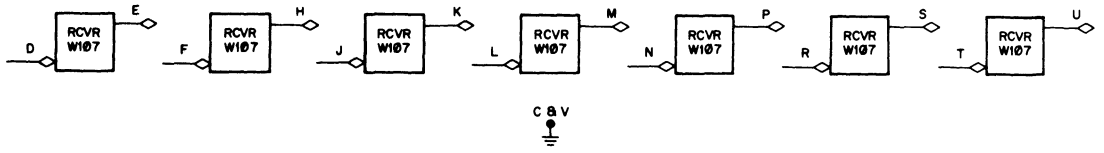


Figure 4-8 Typical Connections, W102

W107 I/O BUS RECEIVER

Standard Size FLIP CHIP Module, 18 Pins



The W107 contains seven identical non-inverting receiver circuits with high-impedance input for buffering signals from the PDP-10 I/O Bus. The W107 is pin compatible with the W500 emitter follower.

INPUTS: Standard DEC levels of -3 V and ground. Each input draws 0.22 mA at ground and less than 1 μA at -3 V.

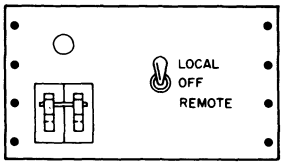
OUTPUTS: Standard DEC levels of -3 V and ground. Each output can supply -7 mA at -3 V and 36 mA at ground, in addition to the internal clamp load. The TTT is less than 150 ns for both rise and fall.

POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	2.5 V to 17.5 V	.14 ma
B	-15 V	-10 V to -20 V	100 mA
C,V	ground		

Both pins C and V must be grounded.

Type 844 POWER CONTROL Panel



The 844 Power Control provides remote and local on-off control, noise filtering, and power-on, power-off logic transient control.

The 844 requires 8 in. of space on a 16 in. plenum door. All connections are on the inside of the plenum door. All operating controls are on the outside of the door.

INPUTS: Line - The 844 will accommodate 115 V or 230 V ac 50-60 Hz power lines. A three conductor cord containing a safety ground wire should be connected to the pressure type terminal strip provided. The input supply need not have one side grounded as both sides of the line are switched throughout.

Remote Control, ac - Power to the load is applied when the ac remote control input is energized. It must be of the same voltage as the line input. Male and female parallel-blade, U ground connectors are provided to facilitate connection of the ac remote control bus to all successive power controls.

Remote Control, dc - Power to the load is also applied when any of the four dc remote control inputs are at -15 V. Load is approximately 1 W. The dc remote control inputs are Heyman tabs suitable for AMP Faston solderless connectors.

If either of the ac or dc remote control inputs are energized and the local-remote switch is in the remote position, power will be applied to the load.

CONTROLS: Circuit Breaker - A 30 A double-pole toggle-switch type circuit breaker controls all power to the load. The circuit breaker can be used as a master power switch.

Local-Off-Remote Switch - This three-position toggle switch controls the power control mode. In local, the switched load is energized. In off, the switched load is de-energized. In remote, the switched load is energized under the control of the remote control inputs.

Console Switch - A single-pole switch can be inserted between the pair of Heyman tabs provided. When the switch is closed the switched load may be energized. The switch must break the line voltage and carry approximately 500 mA rms. If a console switch is not used, a jumper must be substituted.

Orange Jumpers - Two orange Faston jumpers must be supplied between the pairs of orange Heyman tabs to operate the power control from 115 Vac. The jumpers should be removed for 230 Vac operation.

White Indicator - A white neon indicator is lit whenever line voltage is present at the line input terminals.

OUTPUTS: Unswitched - The two unswitched convenience outlets and unswitched Heyman tabs are energized whenever the circuit breaker is on.

Switched - The two switched convenience outlets and switched Heyman tabs are energized when the console switch is on, and the local-off-remote switch is in local or remote. (See the block diagram Figure 4-9.) The switched power comes on immediately and goes off with a 4 s delay.

Frame Ground - These Heyman tabs are connected to the chassis of the power control and the safety ground wire of the line cord.

Crobar - These Heyman tabs are connected to a time delayed relay contact. The contact is closed when power is off. They open 4 s after power-on and close immediately at power off. The contacts are rated at 115 V ac 5 A.

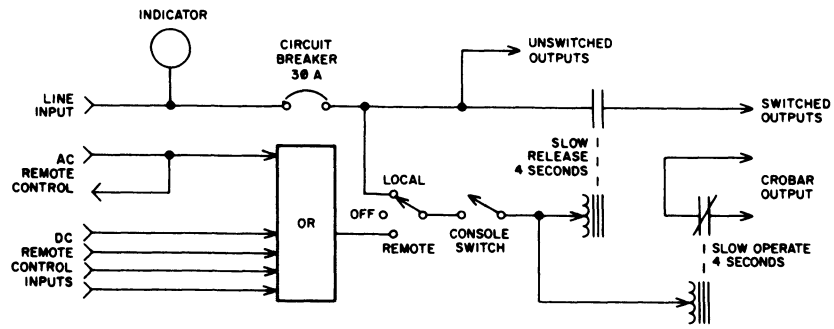
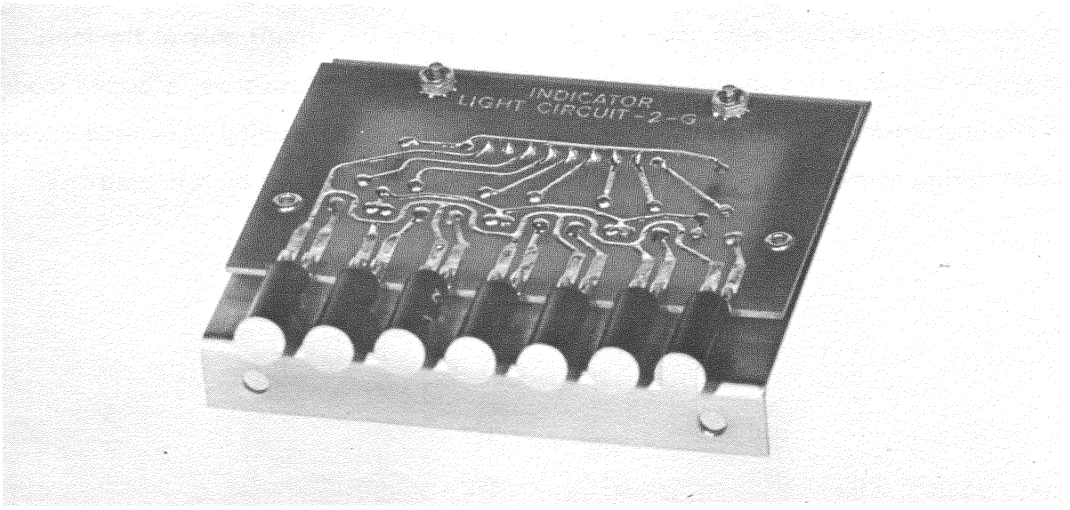


Figure 4-9 844 Power Control Block Diagram

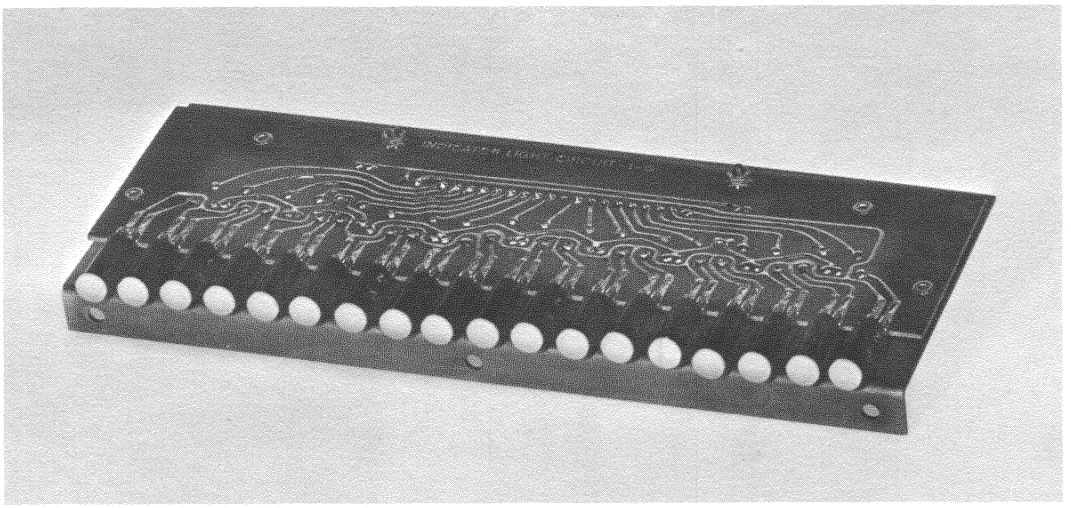
The term "crobar" is an extension of a concept originally used in radar power supply technology and more recently used in integrated circuit power supplies. A crobar circuit (often spelled crowbar) was originally used to rapidly discharge a radar's high voltage power supply after a detected malfunction to avoid damaging (expensive) output components. In more recent integrated circuit power supplies, the term is used to describe a circuit which detects excessive output voltage and shorts it to ground to avoid damaging integrated circuit components. The crobar function of the 844 provides a means which the logic designer may use to attempt to eliminate improper operation (glitches) in logic when power is being applied or removed.

The use of the word crobar (crowbar) for this function apparently comes from the "violent" means used to accomplish the function. (The operation of the crowbar circuits of a high power radar can be quite spectacular.) In semi-slang, the crobar is said to gronk the logic, in order to prevent false operation.

APPLICATION: To obtain maximum benefit from the crobar feature of the 844 in the large transient electric and magnetic field environment associated with turn-on and turn-off, it is advisable to connect the crobar contacts to the logic with coaxial cable, grounding the circuit only at the logic. In addition, noise energy on the crobar line should be absorbed by the use of load resistors, clamped loads, or diode clamps on the ungrounded side of the crobar circuit. The particular loading to be used depends on the voltage level during normal operation and the amount of noise which can be tolerated.



4902 Indicator With Amplifier



4903 Indicator With Amplifier

The 4902 provides seven indicators with amplifiers mounted on a bracket designed to mount from the rear of a blank panel. The 4903 is similar but provides 18 indicators with amplifiers.

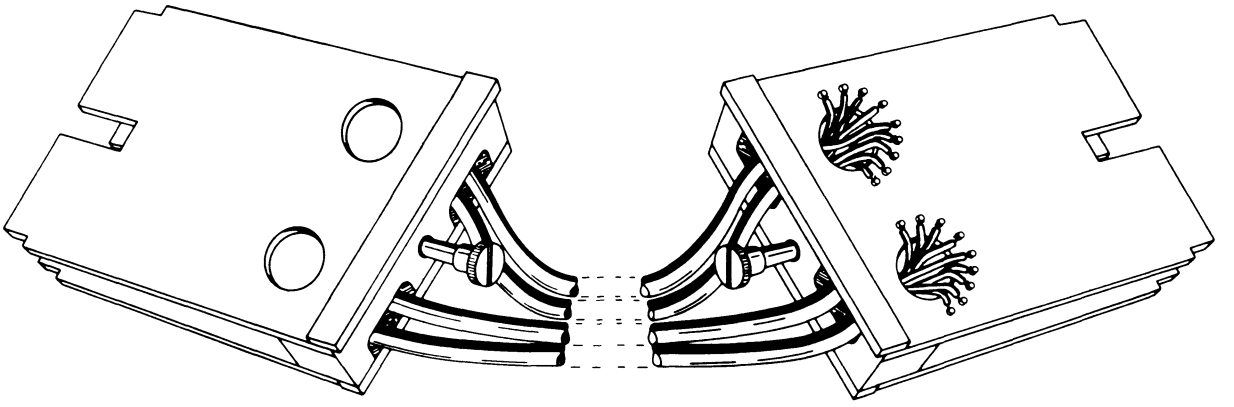
Both units use 28 V lamps operated at 15 V providing a pleasant indication over an extended life. Indicators are located on 1/2 in. centers and require a clearance hole for their 5/16 in. diameter.

INPUTS: Each indicator with amplifier requires -1 mA at -3 V which may be provided by the W020 indicator connector. The indicator is on when the input to the W020 is at -3 V and off when the input is grounded.

POWER:

	4902	4903
	-15 V 210 mA	-15 V 540 mA
Mating Connector	Amphenol 143-010	143-022
Overall Dimensions	4 x 3.75 x 15/16 in.	9.5 x 3.75 x 15/16 in.

BC10A BUS CABLE ASSEMBLY



The BC10A Bus Cable Assembly is the standard PDP-10 I/O bus, memory and multiplexer bus, and channel bus cable. It consists of an H351 type connector assembly at each end of a quadruple 9-conductor coaxial cable assembly. The connectors at each end screw into H003 or H004 connector retaining blocks so that they will not loosen under vibration. Each connector occupies four module locations on the left or right half of a single H800 module connector block.

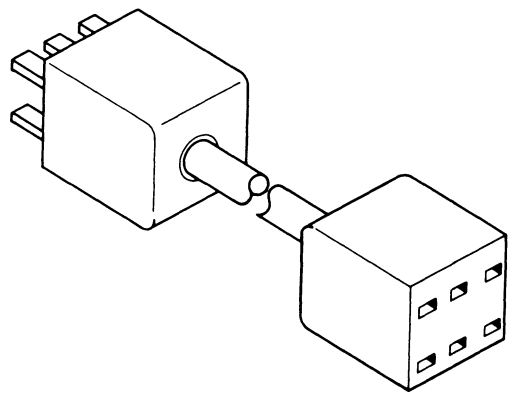
See the H351 description for connection and power details.

The BC10A cable assembly is ordered by specifying BC10A-XX where XX is the number of feet of cable measured from the back end (handle end) of each connector.

Standard lengths are 5, 7, 10, 15, 25 and 35 ft.

Two BC10A cable assemblies are required for each of the PDP-10 buses.

BC10B MARGIN CHECK CABLE ASSEMBLY



The BC10B Margin Check Cable Assembly is the standard PDP-10 margin check bus cable. It consists of a Cinch-Jones P-306-CCT male plug at one end and Cinch-Jones S-306-CCT female plug at the other end. The cable is arranged as an extension cord; that is, all six pins at one end are connected to the corresponding pins at the other end.

The BC10B cable assembly is ordered by specifying BC10B-XX where XX is the length of the cable in feet. Standard lengths are 5, 7, 10, 15, 25 and 35 ft.

Also available is a similar cable with male plugs at both ends to facilitate conversion of equipment arranged for the PDP-6 margin check bus to PDP-10 margin check bus operation. This cable assembly is DEC part number 7005256.

BS10A BUS CABLE SET

The BS10A cable set provides the cables usually needed for the PDP-10 I/O memory, or multiplexor bus. It consists of two BC10A bus cable assemblies, one BC10B margin check cable assembly, and an ac remote turn-on cord.

The BS10A cable set is ordered by specifying BS10A-XX where XX is the length of the cable set in feet. Standard lengths are 5, 7, 10, 15, 25 and 35 ft.

CHAPTER 5
GP10 GENERAL PURPOSE INTERFACE FOR THE PDP-10

The GP10 provides much of the hardware needed for an I/O bus interface to the PDP-10. Three versions are available. The GP10M provides a standard DEC 19 in. cabinet fitted with the hardware accessories most often required when building a special logic assembly. The GP10L provides a general-purpose logic interface to the I/O bus, including a control and status register and buffering for 36 bits of data. The GP10B provides the GP10L logic mounted with the GP10M hardware accessories in a 19 in. cabinet.

GP10M

The GP10M consists of a CAB-9B drilled for the indicator panel and power distribution/margin bus bracket with an indicator panel (three rows of 36 lights), an 844 Power Control, two 728 Power Supplies (728A's for 50 Hz areas), doors, side panels, and one set of logic cooling fans, and an intake fan mounted in it. The GP10M also provides nine W012 - W250 indicator driver cable assemblies, and a 15 ft set of I/O bus cables. Fifty-two and a half inches of space is provided for mounting the logic.

GP10L

The GP10L contains an I/O bus interface and status logic usable for almost any device which is to communicate with the PDP-10 through its I/O bus. It contains bus receivers and gating such that an unchecked-out I/O device may be connected to the I/O bus through the GP10L with no possibility of interferring with I/O bus operation. The GP10L provides one program assignable program interrupt (PI) channel, six bits of device control information, and nine bits of device status in its status register. It provides facilities for the transfer of 36 bits of data into or out of the PDP-10. It occupies 5-1/4 in. of space in the GP10M.

PROGRAMMING

GP10 programming will vary widely depending on what type of device the user constructs using the GP10 and how he wires the various "option-jumper" cards. The device number which the GP10 responds to is set by an option jumper card. It should be in the range 400_8 to 774_8 . The mnemonic DEV is assumed below for the device number assigned to the GP10.

The instruction DATAO DEV will transfer 36 bits (or less if all bits are not used) to the user's device from the contents of the effective address. In addition, it may clear one or more of the status flip-flops (bits 27 through 32 of the status register), depending on the option jumpers provided by the user.

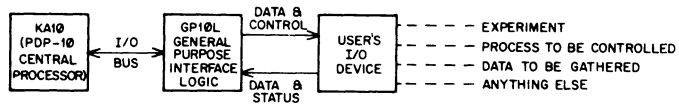


Figure 5-1 GP10 General Purpose I/O Bus Interface Configuration

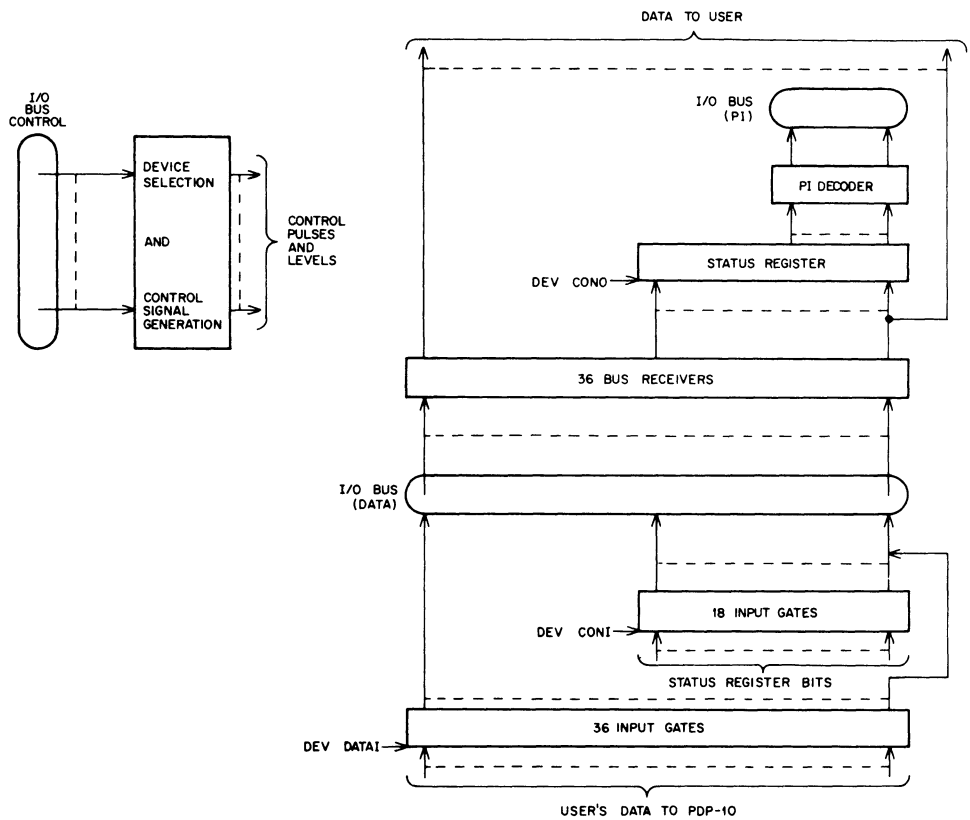


Figure 5-2 GP10L Block Diagram

The instruction DATAI DEV will transfer 36 bits (or less if all bits are not used) from the user's device to memory. In addition it may clear one or more of the status flip-flops depending on the option jumpers provided.

If a data word of less than 36 bits is transferred to or from the user's device, it is conventional to transfer the data in the least significant bits of the 36-bit data word (i.e., at the right end of the word) although cases may arise where it is more convenient to locate it elsewhere in the word.

The GP10 status register is shown in Figure 5-3.

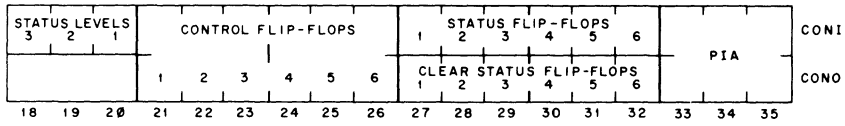


Figure 5-3 GP10 Status Register

The instruction CONI DEV will transfer the status register shown into memory. Bits 33 to 35 of the word transferred indicate the current setting of the PI channel. When a program interrupt occurs it will be on this channel. Bits 27 to 32 indicate the state of the status flip-flops. These flip-flops may be set by the user's device and may be cleared by a DATAO or DATAI depending on option jumper wiring and may be selectively cleared by the corresponding bit in a CONO instruction. One or more of these flip-flops depending on option jumper wiring cause a PI when it is in the 1 state. Bits 21 to 26 indicate the state of the control flip-flops. Bits 18 to 20 indicate conditions in the user's device.

The instruction CONO DEV will load or clear flip-flops in the status register according to bits of the effective address which are 1s. (CONO is an "immediate mode" instruction; i.e., the effective address itself is used as data rather than the contents of memory.) Bits 33 to 35 load the PI channel flip-flops. Bits 27 to 32 clear the status flip-flops. Bits 21 to 26 load the control flip-flops. In addition, any of bits 18 to 35 may be used to cause additional actions in the user's device.

The control flip-flops, status flip-flops, and PI channel flip-flops are cleared at power on and are cleared by IOB RESET.

OPTION JUMPER WIRING

The logic structure of the GP10L is very flexible as the operations of most functions can be varied by the installation of jumpers on three plug-in modules. The variations possible using these jumpers are described below. Further variation is possible if the user modifies the wiring of the logic. To this end a complete set of logic diagrams is provided with each GP10L.

Device Number

The GP10L can be made to respond to any of the 128 possible device numbers. A sketch of the W991 module at location AB28 showing which jumpers to use is shown in Figure 5-4. One jumper of each pair (IOS 3(1), IOS 3(0)) must be provided in order that the device will respond to only one device number.

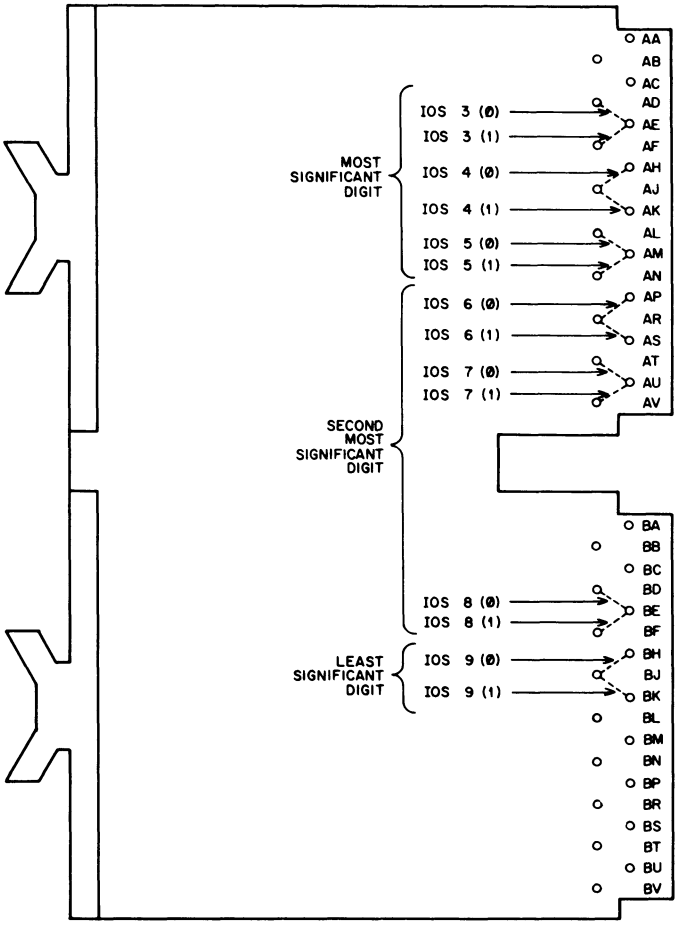


Figure 5-4 W991 Module, Location AB28

Status Flip-Flops

Each status flip-flop may be cleared by DATAI, DATAO, or both (in addition to CONO) by suitable jumpering on the W990 module at location B06. These jumpers are shown in Figure 5-5.

Any status flip-flop which should be cleared by both DATAI and DATAO should have its clear input (shown above) connected to pin L (DATAI OR DATAO). Any status flip-flop which should be cleared by DATAI only should have its clear input connected to pin M (DATAI). Any status flip-flop which should be cleared by DATAO only should have its clear input connected to pin N (DATAO). Any status flip-flop which should not be cleared by either DATAI or DATAO should have its clear input connected to pin C (ground). If a clear input is left unconnected the status flip-flop will always be cleared.

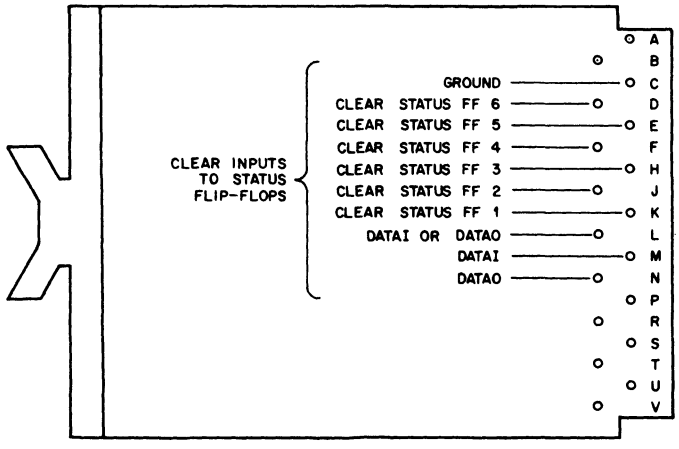


Figure 5-5 W990 Module, Location B06

Program Interrupts

Any of the status flip-flops may cause a program interrupt PI when it is in the 1 state (i.e., set). To select which status flip-flops will cause program interrupts, wire the W990 module at location B05 as shown in Figure 5-6.

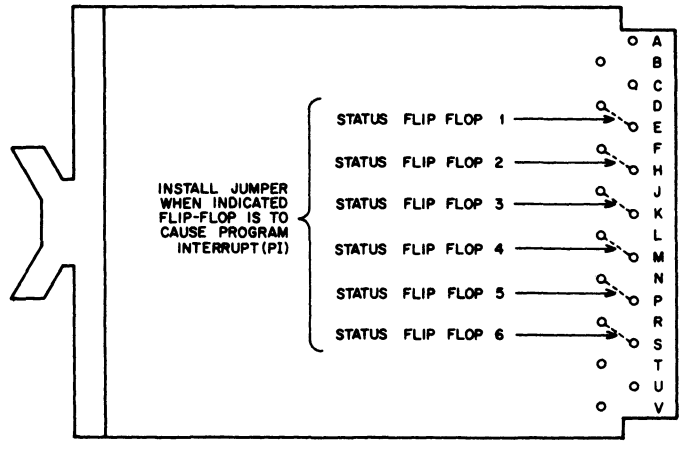
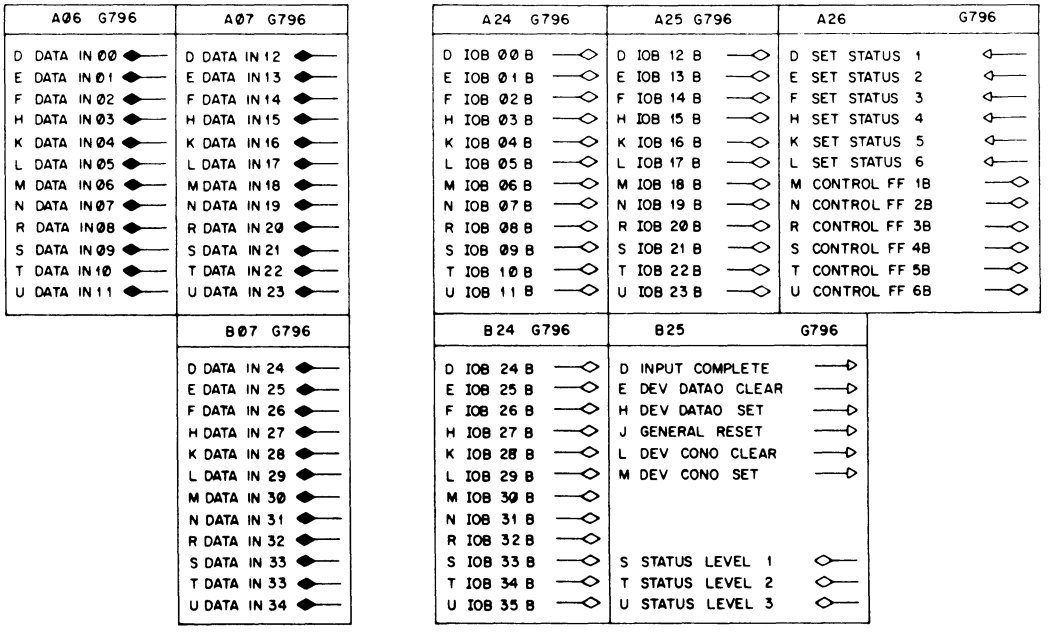


Figure 5-6 W990 Module, Location B05

INTERFACE

The GP10L provides data and control connections between itself and the user's logic with eight G796-G796 cable assemblies. The user may chose instead to locate his logic immediately adjacent to the GP10L and wire the connections between them instead. The cable connections are shown in Figure 5-7.



Pin B of all connectors used must be supplied with -15 V.
Pins C, J, N, and V must be grounded on all connectors used except B25.
Pins C, F, K, N, P, R and V must be grounded on B25 connector if used.

Figure 5-7 Cable Connections to GP10L

All lines into and out of the user's device are DEC standard levels of -3 V and ground. The G796 cable connectors contain level terminators which prevent signals from going above ground or below -3.5 V and facilitate "clean" signal transmission.

The Data In nn lines supply the user's data to the I/O bus interface. -3 V represents a 1, ground represents a 0. The user's logic must drive 6 mA at ground on these lines. These lines are strobed into the PDP-10 by a DEV DATAI instruction. Any line not used, should be grounded, otherwise a 1 will be sent to the PDP-10 by the DEV DATAI instruction.

The IOB nn B lines supply PDP-10 data to the user. Ground represents a 1, -3 V represents a 0. These lines are the I/O bus data lines buffered by W107 bus receivers. Both DEV CONO and DEV DATAO instructions make use of these lines. These lines are correct at least 400 ns before DEV CONO CLR, DEV CONO SET, DEV DATAO CLR, and DEV DATAO SET pulses and are often used to drive the level inputs of R-series DCD gates. (See the DIGITAL Logic Handbook for module descriptions of these gates.) These lines will supply up to 30 mA at ground or -7 mA at -3 V.

The Set Status n lines allow the user to set the status flip-flops in the status register. The flip-flop is set by a negative 100 ns or longer pulse or by a negative going transition with a fall time of less than 60 ns and a duration of 100 ns or longer. The line must be at ground at least 400 ns before going negative. The user's logic must drive 5 mA at ground on these lines. These lines may be left unconnected when not used.

The Control FF n lines provide the user with an indication of the state of the control flip-flops. The line is ground when the flip-flop is in the 1 state (set) and -3 V when the flip-flop is in the 0 state (cleared). Each line will drive 10 mA at ground and supply -3.5 mA at -3 V.

The input complete pulse signals the user that a DATAI DEV instruction has just been executed. This signal is a 100 ns positive (-3 V to ground) pulse which will drive 30 mA at ground or -3.5 mA at -3 V.

The DEV DATAO CLEAR and DEV DATAO SET pulses are regenerated versions of the two pulses caused by a DATAO DEV instruction. Ordinarily, the DEV DATAO CLEAR pulse is used to clear a data register and the DEV DATAO SET pulse is used to load it from the IOB n B lines. Each pulse is a 100 ns positive (-3 V to ground) pulse which can drive 30 mA at ground or -3.5 mA at -3 V. The pulses are 1 μs apart.

The GENERAL RESET pulse occurs at power-up and when the PDP-10 generates an IOB RESET pulse. It should be used to reset the user's device to a "starting" or "cleared" state. The pulse is a 100 ns positive (-3 V to ground) pulse which will drive 30 mA at ground or -3.5 mA at -3 V.

The DEV CONO CLEAR and DEV CONO SET pulses are regenerated versions of the two pulses caused by a CONO DEV instruction. The DEV CONO CLR pulse is used to clear the control and PI flip-flops in the GP10L, whereas the DEV CONO SET pulse is used to load them from the IOB n B lines. These pulses may also be used for control purposes in the user's logic. Each pulse is a 100 ns positive (-3 V to ground) pulse which can drive 20 mA at ground or -3.5 mA at -3 V. The pulses are 1 μs apart. The DEV CONO CLEAR pulse also occurs whenever the GENERAL RESET pulse occurs to allow the GENERAL RESET pulse to clear single clear input flip-flops by means of the CONO CLEAR pulse.

The Status Level n lines provide the user with direct status bits into the PDP-10. These lines are read into the PDP-10 by a CONI DEV instruction along with the rest of the status register. Ground represents a 1, -3 V represents a 0. The user's logic must drive 6 mA at ground on these lines. If a line is left unconnected, it represents a 0.

CHAPTER 6
USER TERMINALS

FUNCTIONAL REQUIREMENTS

Teletypes and other user terminals need to meet only a minimum number of requirements to be used with the standard PDP-10 hardware-software system. (Violation of any particular requirement will require the use of some hardware option or special interface, or a modification of the standard software. In many cases, the change is quite simple,such as supplying extra NUL characters to allow a slow carriage to return.) PDP-10 software is designed around an ordinary (essentially unmodified) Teletype machine using the ASCII (USASCII) character codes.

a. The terminal must have a 20 mA, neutral, full-duplex or an EIA interface. Details of these standard interfaces are supplied below.

b. The terminal must use self-synchronizing, asynchronous, serial-by-bit, serial-by-character data transmission. (That is, ordinary, start-stop, teletype-style data transmission.)

c. The printer or display part of the terminal must respond to the control characters CR (carriage return, 015_8) and LF (line feed, 012_8) in the ordinary way. Response to other control characters is not required

d. The printer or display must have "continous paper"-like characteristics. That is, a special control should not be required to "advance-to-the-next page" (erase the present display).

e. No waiting time beyond that provided by a CR LF sequence (carriage return, line feed) should be required to return the printing carriage to the beginning of the line.

f. The printer or display should respond to at least the first 64 graphics of ASCII. (USASCII "figures" 040_8 to 077_8, and "upper case" 100_8 to 137_8). Any version of ASCII can be used with the user doing translation among equivalent graphics as necessary. All 95 graphics of USASCII can be used when available.

g. The keyboard must be able to generate at least one of the ALTMODE or ESC (PREFIX) codes (033_8, 175_8, 176_8).

h. The keyboard must be able to generate the "control" characters (000_8 to 037_8).

i. The keyboard must be able to generate at least the first 64 graphics of ASCII.

j. The terminal should not have any "funny" or "strange" features; i.e., features not predictable from some reasonable interpretation of some revision of the ASCII standard.

Any terminal which meets the above requirements should be a usable terminal. It may not be as convenient to use as an ordinary Teletype with the PDP-10 modifications, but it will be adequate for many uses.

Teletypes supplied by DIGITAL for PDP-10 systems will have the following as standard: local (off-line) mode; slashed zero (Ø), upward arrow, and left arrow characters; a separate ALTMODE, ESC, or PREFIX key; and standard plug connector. When considered necessary by DIGITAL engineering, various mechanical modifications will also be incorporated to provide improved reliability and user convenience.

INTERFACE

Connections for 20 mA, neutral, full-duplex terminals (most Model 33 and 35 Teletypes and similar equipment):

Arrange (modify) the machine for 20 mA line current and full-duplex operation as indicated on the drawings furnished with the machine by the manufacturer. Connect a 283B plug as shown in Figure 6-1. Polarity must be as indicated.

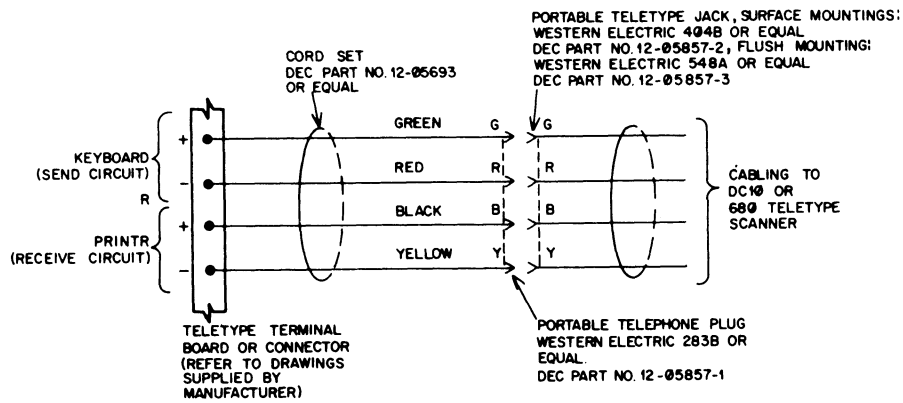


Figure 6-1 20 mA, Full Duplex Terminal Interface

Connections for EIA Interface terminals (EIA Standard RS-232-B) (Model 37 Teletypes and many other terminals):

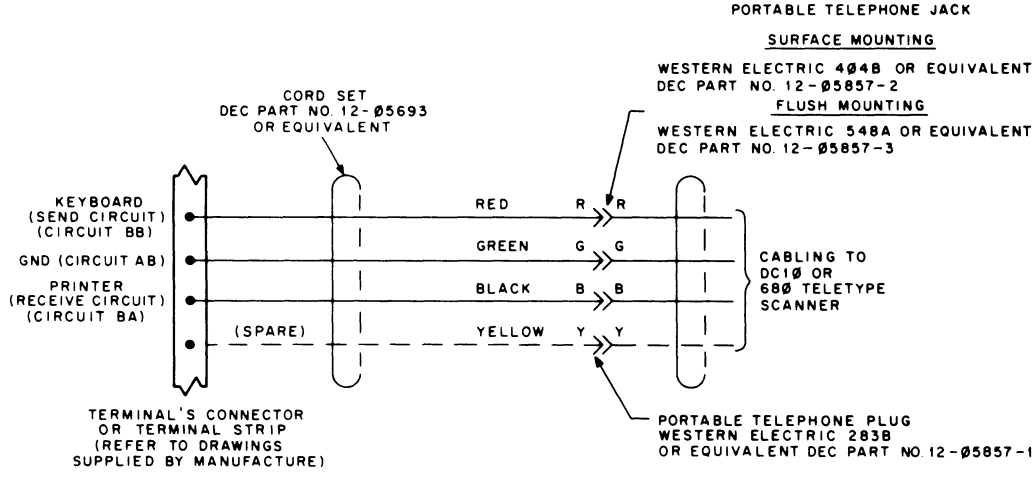


Figure 6-2 EIA Interface

CHAPTER 7
PDP-10 MEMORY BUS AND MULTIPLEXOR BUS DESCRIPTION

INTRODUCTION

The PDP-10 memory bus is a set of cables which connect PDP-10 memory modules to the KA10 Central Processor, to the MX10 Memory Multiplexor, or to a suitable peripheral processor (channel) such as the DF10 Data Channel. The multiplexor bus is a simple extension of the memory bus and is also included in this description. Timing and loading rules for the memory and multiplexor buses are spelled out, along with design guide lines.

This chapter describes the PDP-10 memory bus and memory multiplexor bus in sufficient detail to enable a user to design special peripheral processors and memory modules compatible with the PDP-10 system. Loading and interfacing rules are specified in terms of DIGITAL FLIP CHIP modules which may be used to implement an interface. All statements about the memory bus apply to the multiplexor bus unless otherwise noted.

COMPATIBILITY WITH PDP-6 SYSTEMS

The PDP-10 memory bus is compatible with the PDP-6 memory bus: PDP-6 memory modules may be used on the PDP-10 memory bus or vice versa (except the 162 Fast Memory which is inapplicable to the PDP-10). Also, PDP-10 peripheral processors can operate on the PDP-6 memory bus.

BUS OPERATION

Memory Bus Information Flow

The PDP-10 memory bus is a cable system which connects a processor and one or more memory modules together. The processor interface and memory module interfaces are all in parallel across the memory bus. Due to the high-speed signals involved, the parallel connection is realized as a transmission line passing through each memory module and through the central processor, and terminated at each end. All standard PDP-10 memory modules are equipped with one to four access ports (that is, four independent memory bus interfaces). Figure 7-1 shows a possible arrangement of memory modules and processors. Notice that there is only one processor on each memory bus. Figure 7-2 shows the information flow in the memory bus.

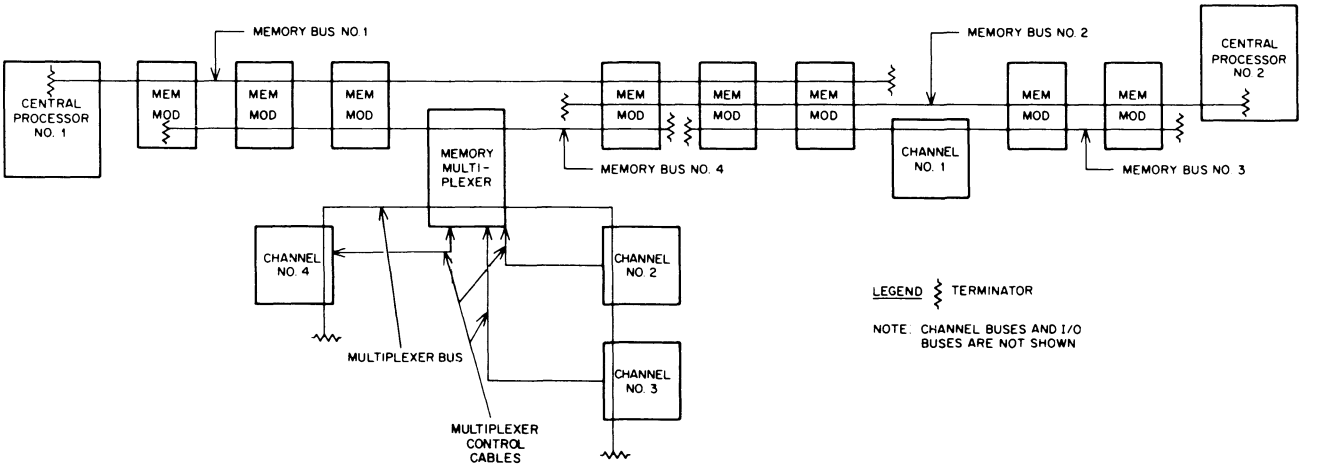


Figure 7-1 Possible Memory Bus Arrangement

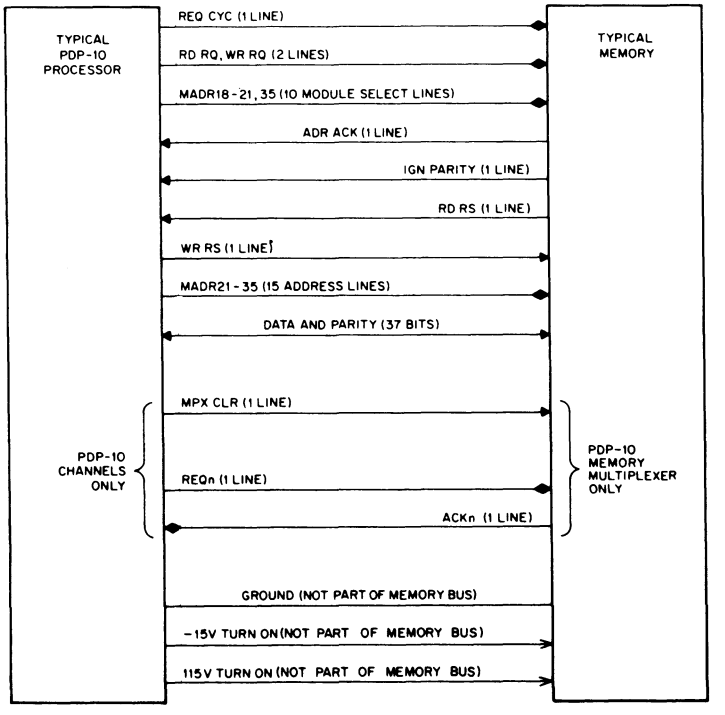


Figure 7-2 Memory Bus Information Flow

Memory Bus Operation

Because both the PDP-10 processors and the PDP-10 memory modules are asynchronous, the use of the memory bus is controlled by "Request-Response" operation; that is, the processor (typically) makes a request and waits for a response from a memory module. Another feature to consider is that each memory module may be addressed by up to four different processors (or memory multiplexors). The memory bus operates in the following manner. When the processor on a memory bus requires a memory reference, it places the memory address and information as to whether it will read out of memory or write into memory or both on the appropriate lines. Then it asserts the REQ CYC (request cycle) signal. When the memory module addressed has no higher priority requests and is ready to start another cycle, it sends the ADR ACK (address acknowledge) pulse to the processor signifying its acceptance of the request.

If the cycle requested is a read only cycle, the memory proceeds to read out the data at the requested address onto the memory data lines and parity onto the parity line if the memory module has parity provided. If parity is not provided, the memory sends the IGN PARITY (ignore parity) pulse to the processor concurrent with the ADR ACK pulse. After the memory module sends the requested data to the processor, it sends the RD RS (read restart) pulse signifying it has finished the request. It then disconnects itself from the bus and finishes its read cycle.

If the processor requests a write only cycle, the memory clears its data buffer register, and the transmits the ADR ACK pulse. After ADR ACK is received, the processor must send the data to be written and parity to the memory module and then transmit the WR RS (write restart) pulse to the memory module signifying that the data has been sent. The memory module disconnects itself from the bus while writing the data into memory. Thus, the processor may obtain another memory cycle from a different memory module while the one previously referenced is finishing its cycle.

If both a read and write cycle are requested by the processor (a read-modify-write cycle), the memory module proceeds through a read cycle, sending the data, parity, and RD RS to the processor. However, instead of disconnecting itself from the memory bus and completing a normal read cycle, the memory module clears its data register and waits. The processor may then send new data to the memory module (with parity) and restart the memory with the WR RS pulse. After receiving the WR RS pulse, the memory disconnects from the memory bus and writes the new data into the location from which it read the old data. This mode of operation is used by the KA10 Central Processors in such instructions as AOS MEM which reads the location MEM into the central processor, adds 1 to the number read in, and writes the incremented number back into location MEM. Read-modify-write cycles of this type, of course, tie up the memory module for a longer time than if memory modification instructions are split into separate read cycles and write cycles. Both the 166 and KA10* Central Processors have a signal (the DR SPLIT line in their I/O bus systems) for inhibiting read-modify-write cycle requests (splitting

*The KA10 is the PDP-10's Central Processor; the 166 is the PDP-6's.

them into separated read and write cycles), thereby providing memory access in one memory cycle maximum, instead of one memory cycle plus processing time. This time saving is valuable when operating high-speed peripheral processors.

Multiplexor Bus Operation

The multiplexor bus operates in a manner similar to the memory bus operation. However, a preliminary "Request-Response" must occur - when a processor (such as the DF10 Channel) accesses memory through the MX10 Memory Multiplexor, it must request a path through the multiplexor by asserting the REQn signal. If the processor has the highest priority of all processors sending REQn signals, the multiplexor returns an ACKn signal to the processor. The processor now has control of the multiplexor bus and proceeds exactly as if it were communicating directly with memory. The preliminary REQn, ACKn exchange is necessary to establish non-interference among the processors (eight maximum) which may be accessing memory through the memory multiplexor since all multiplexed processors use the same lines for communication.

Memory Module Selection

In general, one processor (or multiplexor) and several memory modules share a single memory bus, therefore, part of the information carried by the bus indicates which memory module is to respond to the memory request. The bus also allows memory interleaving on the least significant bit of the memory address so that odd addresses are located in one set of memory modules and even addresses in another set. The four most-significant bits of the memory address (MADR 18 through 21) and the least significant (MADR 35) appear on the memory bus as complementary pairs of signals. Thus for 16K or larger memory modules, interleaved or not, all module selection decoding can be done directly off of the bus. For 8K memory modules, the MADR 22 line is also available as a complementary pair for use as an input to the module selection decoding gate. A memory module must respond only when its range of memory addresses is selected and a REQ CYC signal is present. (The KA10 Central Processor uses the memory bus for data transfer from the AR to the IR without requesting any memory cycle.)

Memory Address

The memory address lines MADR 21 through 35 designate the specific address to be referenced in the selected memory module. These lines are usually loaded into a memory address register and then used to control the selection matrix in the memory. MADR 21 replaces MADR 35 when a memory is used with other memories for interleaved operation.

Data Lines

Data passes between the memory module and the processor as pulses. The 36 MBD (memory bus data) lines and the PARITY PULSE line carry these data pulses in both directions. Further, these data lines (like the other lines in the memory bus) are shared by all memory modules. Because of the two-way, shared nature of these pulse lines, the memory module and processor interfaces must conform to the specifications below. Failure to conform may result in marginal operation which will make the entire bus system unreliable.

Miscellaneous Signals

If a processor transmits a non-existent address to the multiplexor, the multiplexor waits indefinitely for a response from the memory system. In such an event, the MPX CLR (multiplexor clear) signal in the multiplexor bus allows a processor to relinquish control of the memory multiplexor to which it is attached.

A POWER ON signal is present in the margin check cable when the central processor has power applied. The memory's power should turn on if any of the four possible processors to which it is attached are on. An alternate ac power-on signal is also supplied from the processor. A ground connection (in addition to the safety wire in the power cord) should be provided between each central processor and its memory modules. This connection should be made with #4 gage copper wire or equivalent and may be chained through other memory modules. (See the PDP-10 Installation Manual or Chapter 10 for further details.)

Programming Considerations

Although the memory bus itself need not be considered by programmers, the design of peripheral processors using memory locations for control information should take into account the fixed core allocations defined by both the central processors and the software monitors. Further, address translations must be considered (e.g., if a memory module is interleaved from port 0 (P0) and noninterleaved from port 1 (P1), the relationship between port 0 and port 1 addresses is somewhat unwieldy).

INTERFACE SPECIFICATIONS

The memory bus physically consists of two 100 Ω coaxial cable assemblies which terminate in H351 FLIP CHIP connector assemblies.* These connectors fit into a single, augmented FLIP CHIP connector block (H800 with a H003 or H004 retaining block). All memory bus interfaces must have two sets

*W850-type connectors may be used after evaluation.

of memory bus connectors; one set to receive the incoming cables from the processor or previous memory module and the other set to plug-in outgoing cables for the next memory module on the bus. If no cable is plugged into the outgoing cable connectors, the bus must be terminated by plugging in terminating cards. Thus the memory bus must thread through each memory module and through the processor and have terminators at each extreme end. Each memory bus signal line must be wired with twisted pair from the incoming bus connector, to the sources or loads, and then to the outgoing memory bus connector. The designer may violate this rule (at his own risk) if very short wires are used. Even though some memory bus signal lines are not used by a particular memory module (e.g., MADR 22 (0)), all signals including spares must be strapped across from the input connector positions to the output connector positions with twisted pair in order to feed all signals to subsequent memory modules. The length of this twisted pair must be included when checking the maximum memory bus length specification of 150 ns from the processor to the farthest memory module, one way (see below), and care must be taken that the differential lengths do not exceed 1 ns (200 mm or 8 in.). On all 16 FLIP CHIP connector slots occupied by the memory bus cables, pins C, F, J, L, N, R, and U must be grounded. The normal power connection to pin B (-15 V) must be made for all 16 positions; power connections to pin A (+10 V) are optional and do not affect the operation of the memory bus. 100 Ω ± 10% terminating resistors are required at both ends of each line of the memory bus. These terminating resistors may be provided by G703 modules plugged into the empty cable connectors at the end of the bus (G700s cannot be used because of the retaining block for the W851s). Eight G700 modules should be used in the 164 and MB10 memories. Table 7-1 shows the pin assignments for the memory bus cable system and a typical wiring-side layout of the memory cable connectors. Various cable adaptors are available for connecting older memories to operate with PDP-10 processors. The pin assignments of these adaptors are also shown in Table 7-1.

Multiplexor Interface

The multiplexor bus consists of two coaxial cable sets identical to the memory bus plus a separate cable between each peripheral processor and the multiplexor which carries signals to determine which processor has control of the multiplexor. Table 7-2 shows the pin assignments for these eight additional cables. Like the memory bus, the multiplexor bus must be wired through each peripheral processor using twisted pair from the incoming connector, to sources or loads, to the outgoing connector. All lines in the multiplexor memory cable must be wired through from incoming connector to outgoing connector, and must be terminated with 100 Ω ± 10% resistors at each extreme end. Each multiplexor control cable connects between a particular peripheral processor and the multiplexor and must terminate in 100 Ω ± 10% resistors at the peripheral processor and at the multiplexor.

Table 7-1
Memory Bus Signals

SYSTEM MODULE PIN	PIN	MEMORY CABLE #1		MEMORY CABLE #2	
(B)	D	ADR ACK ←	MADR 22 (1) →	MBD 0 ↔	MBD 18 ↔
(C)	E	RDRS ←	MADR 23 (1) →	MBD 1 ↔	MBD 19 ↔
(D)	H	WRRS →	MADR 24 (1) →	MBD 2 ↔	MBD 20 ↔
(E)	K	PARITY ↔	MADR 25 (1) →	MBD 3 ↔	MBD 21 ↔
(F)	M	REQ CYC →	MADR 26 (1) →	MBD 4 ↔	MBD 22 ↔
(H)	P	MADR 22 (0) →	MADR 27 (1) →	MBD 5 ↔	MBD 23 ↔
(K)	S	MADR 18 (0) →	MADR 28 (1) →	MBD 6 ↔	MBD 24 ↔
(L)	T	MADR 18 (1) →	MADR 29 (1) →	MBD 7 ↔	MBD 25 ↔
(M)	V	MADR 19 (0) →	MADR 30 (1) →	MBD 8 ↔	MBD 26 ↔
		A↑ B↓	C↑ D↓	A↑ B↓	C↑ D↓
(N)	D	MADR 19 (1) →	MADR 31 (1) →	MBD 9 ↔	MBD 27 ↔
(P)	E	MADR 20 (0) →	MADR 32 (1) →	MBD 10 ↔	MBD 28 ↔
(R)	H	MADR 20 (1) →	MADR 33 (1) →	MBD 11 ↔	MBD 29 ↔
(T)	K	MADR 21 (0) →	MADR 34 (1) →	MBD 12 ↔	MBD 30 ↔
(U)	M	MADR 21 (1) A →	MADR 35 (1) B →	MBD 13 ↔	MBD 31 ↔
(V)	P	MADR 35 (0) →	RD RQ →	MBD 14 ↔	MBD 32 ↔
(W)	S	MADR 35 (1) A →	WR RQ →	MBD 15 ↔	MBD 33 ↔
(X)	T	FMC SELECT ◇	IGN PARITY ←	MBD 16 ↔	MBD 34 ↔
(Y)	V	FMC SELECT →	MADR 21 (1) B →	MBD 17 ↔	MBD 35 ↔

CABLES MUST BE LOCATED ON THE LEFT OR RIGHT HALF OF A MOUNTING BLOCK

CABLE SLOTS (4) DEVOTED TO EACH CONNECTOR AS SEEN FROM WIRING SIDE

NOTE

→ FROM PROCESSOR

← TO PROCESSOR

PINS:
C,F,J,L,N,R,U ARE GROUNDED

THE FMC SELECT LINES ARE PERMANENTLY FALSE IN PDP-10 MEMORY SYSTEMS.

Table 7-2
Pin Assignments

PIN	MPX CONTROL CABLE	W990 PROCESSOR CARD USED WHEN MULTIPLEXOR NOT USED
B	−15V ①	470Ω 1/4W
E	REQ N →	
H	ACK N ←	
K	MPX CLR →	
M	~ ①	

DIRECTION:

→ TO MULTIPLEXOR

← TO PROCESSOR

NOTES: PINS C,F,J,L,N,R, AND V MUST BE GROUNDED

① THE −15V CONNECTION AND THE CLAMPED LOAD AT PIN M SHOULD BE SUPPLIED AT THE PROCESSOR END TO FACILITATE OPERATION OF THE PROCESSOR WITHOUT THE MULTIPLEXOR

Interface Modules

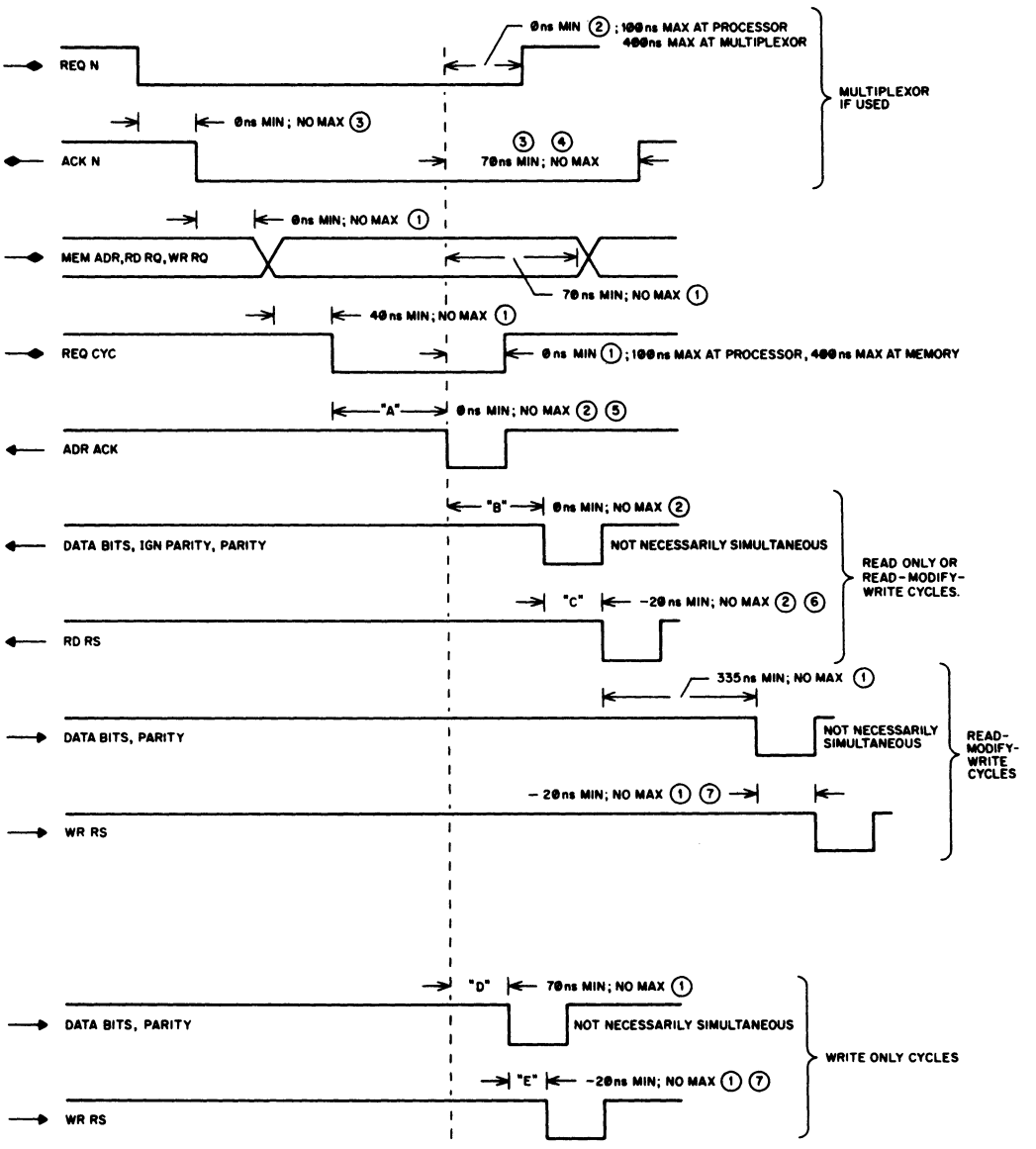
The recommended DIGITAL FLIP CHIP module types satisfy memory bus and multiplexor bus interface requirements. However, a non-DIGITAL module having specifications within those of the specified module may be used if care is exercised. Interface construction is greatly simplified by the use of DIGITAL FLIP CHIP modules. Module specifications are listed in Chapter 4 and in the DIGITAL Logic Handbook or will be supplied upon request. All memory bus and multiplexor bus signals are DEC standard levels of -3 V and ground.

Memory Address Lines

Each processor must drive the memory address lines with B683 or B684 bus drivers. The B683 is required in any processor which may be connected to the MX10 Memory Multiplexor because the memory address lines must be "ORed" together on the multiplexor bus. The lines to be driven by these bus drivers are MADR 18 (1) through MADR 21 (1), MADR 18 (0) through MADR 22 (0), MADR 35 (1), MADR 35 (0), and MADR 21 (1) through MADR 35 (1). Typical connections for these lines are shown in Figure 7-4. Timing requirements for the memory address lines are shown in Figure 7-3. A processor designed for use with the MX10 Memory Multiplexor must not drive any lines unless its ACKn line is true.

Memory Module Selection

The most significant lines of the memory address group (and the least significant line in the case of odd-even interleaving) select a memory module. This selection is decoded as shown in Figure 7-4 by ANDing the selected lines together with REQ CYC in a B172 diode NAND gate. It is frequently convenient to AND in a term from the memory control logic signifying that the memory is ready to start another cycle (AWAIT RQ (1) in Figure 7-4). To maintain compatibility with the PDP-6, ~FMC SELECT should also be ANDed into the B172. Maintenance of the memory system is greatly simplified by running the module selection bits through switches, thus allowing the rapid change of a memory module's address. The wires from the twisted-pair bus to these switches must be as short as possible (less than 6 in.). The wires from the switches to the B172 must also be short. Figure 7-4 also shows the connections necessary to do even-odd interleaving for a 16 K memory module. The "complementary" memory address lines MADR 18 through MADR 21 (0) and (1), from the MX10 Memory Multiplexor are not complementary at all times. However, they are truly complementary whenever the REQ CYC line is true. Timing for these lines is shown in Figure 7-3.



NOTES:
(1) CONTROLLED BY AND MEASURED AT THE PROCESSOR (CONNECTOR).
(2) CONTROLLED BY AND MEASURED AT THE MEMORY MODULE (CONNECTOR).
(3) CONTROLLED BY AND MEASURED AT THE MEMORY MULTIPLEXOR (PROCESSOR CONNECTOR).
(4) ACK N WILL BE TRUE UNTIL THE END OF BUS OPERATION (RD RS IF READ ONLY OR WR RS IF READ-MODIFY-WRITE OR WRITE ONLY).
(5) CENTRAL PROCESSOR WILL DECIDE IT IS ADDRESSING NON-EXISTANT MEMORY AFTER 100 µs.
(6) RD RS MUST OCCUR NO EARLIER THAN 20ns BEFORE THE LATEST DATA, PARITY OR IGNORE PARITY PULSE.
(7) WR RS MUST OCCUR NO EARLIER THAN 20 ns BEFORE THE LATEST DATA OR PARITY PULSE.

MAXIMUM CABLE LENGTH IS 150 ns ONE WAY (30 m OR 98 FT @ 67% PROPAGATION FACTOR).

READ ACCESS IS "A"+"B"+"C".
WRITE ACCESS IS "A"+"D"+"E".

"NO MAX" IMPLIES THAT THE MEMORY BUS, MEMORY, AND PROCESSOR ARE TIED UP UNTIL EVENT OCCURS.

Figure 7-3 Memory Bus Timing

Memory Address Usage

The memory address bits which are not used for module selection must be used for memory addressing to insure that each of the 262,144 (2^{18}) possible memory locations is reached by at most one memory address. These bits are ordinarily loaded into a memory address register in the memory module. To load these bits into a register, the B169 module is recommended. This module provides gating for four access ports to the memory module. The memory address bits to be loaded into the memory address register must be taken off of the memory bus with a B-series 2 mA diode gate (such as the B169) which has two-input AND for negative inputs. The second input must disable the gate unless the memory module has been selected. Figure 7-4 shows an example of this requirement. A convenient way to build the memory address register is to use B213 flip-flops which have a "jam" input suitable for use with the B169 output. The B211 is a suitable alternate which provides the gating and flip-flop functions in one module. The multiplexor regenerates all of the memory address signals. Timing requirements for the MA lines are shown in Figure 7-3. The MADR lines as named (MADR 22 (0)) are true when negative (-3 V).

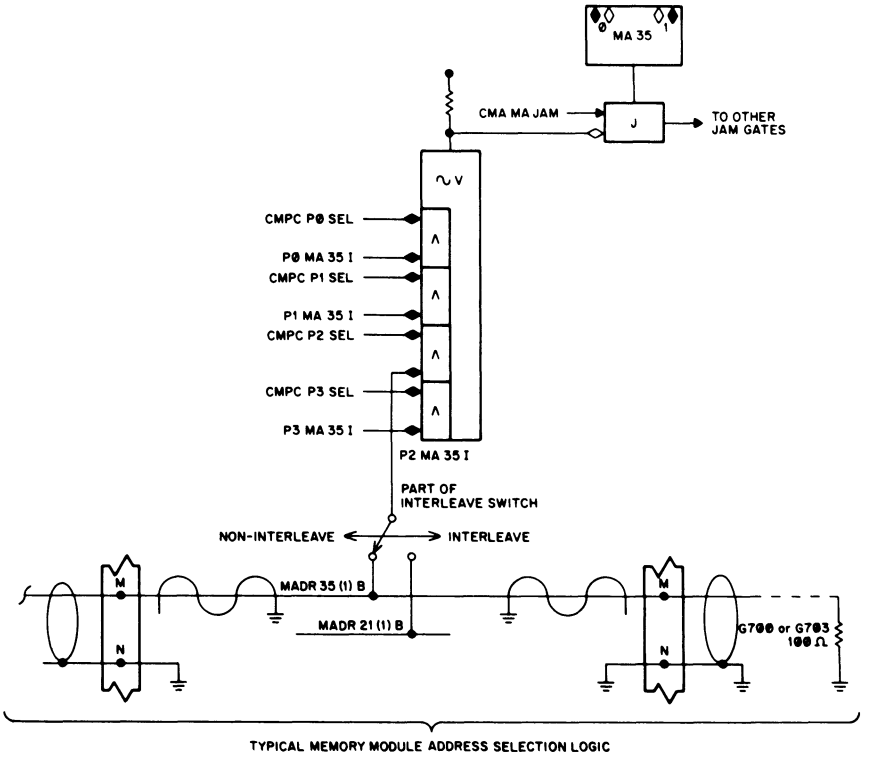


Figure 7-4 Memory Module Selection Decoding

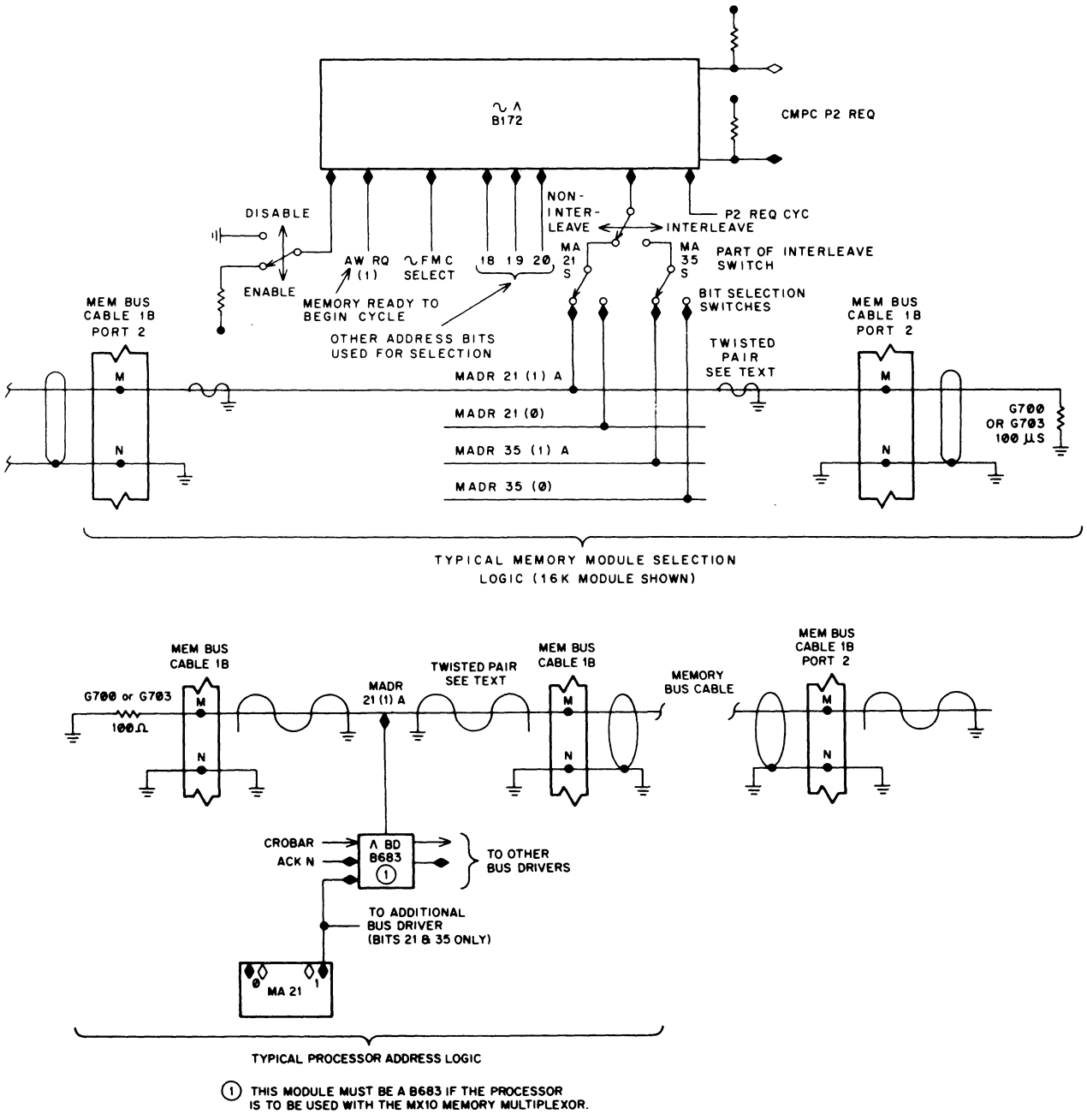


Figure 7-4 Memory Module Selection Decoding (Cont)

Read-Write Control

The RD RQ and WR RQ lines (read and write request respectively) are electrically similar to the memory address lines. They must be driven by B683s or B684s as shown in Figure 7-4. The B683 must be used if use of the MX10 Memory Multiplexor is contemplated. They must be received in the memory module (and usually jammed into flip-flops) in the same fashion as the least significant memory address lines, as shown in Figure 7-4, using a diode gate such as the B169. The other input of the re-

ceiving AND gate should be selected only when the particular memory module is selected. The RD RQ and WR RQ lines are true when negative. The RD RQ and WR RQ timing requirements are identical to the MADR lines and are shown in Figure 7-3. If the RD RQ line is true, a memory read cycle will be performed; if the WR RQ line is true, a memory write cycle will be performed; if both are true, a read-modify-write cycle will be performed; if neither is true, the memory operation is undefined, and a particular type of memory might, for example, destroy (zero) the contents of the location addressed.

Cycle Request

The REQ CYC (request cycle) line is electrically similar to the memory address lines. It must be driven by a B683 or B684 bus driver at the processor (the B683 must be used with the memory multiplexor). REQ CYC must be received in the memory module with one input of a B172 as shown in Figure 7-4. It is recommended that a disable switch also be included for ease of maintenance. The REQ CYC signal is usually the buffered output of a memory request flip-flop in the processor. As shown in Figure 7-3 this flip-flop must be reset by the ADR ACK pulse with a minimum of delay. Otherwise, an additional memory cycle will be requested after the one being requested is completed. The memory address (MADR) lines and RD RQ and WR RQ must carry correct information whenever the REQ CYC line is true (negative). This requires that the REQ CYC line be false whenever the MADR or RD RQ or WR RQ lines are changing, even though another memory cycle is requested immediately.

Fast Memory Select

The complementary FMC SELECT ——◇ and ——◆ lines are for use with the Type 162 Fast Memory which is connected through the memory bus in PDP-6 systems. Only the PDP-6 Type 166 Central Processor makes use of these lines. Any processor which does not use a 162 Fast Memory should have these lines permanently wired false (pin T at -3 V; pin V at ground). The operation of processors with the 162 Fast Memory is beyond the scope of this description.* A memory system which makes use of both the 162 Fast Memory and the MX10 Memory Multiplexor should have processors which gate the FMC SELECT signals with ACK N in the same manner as all other address lines even if the particular processor does not use the 162 Fast Memory.

MEMORY BUS PULSES

All memory bus pulses, data, parity, and control, must be sent and received with W102 Pulse Transceivers. This module type is specifically designed for this application. It will not interfere with proper operation of the bus when its power is off. This feature allows the turning off of either a processor or a memory module without destroying any memory information or inhibiting other use of the bus. All

*For additional information contact DIGITAL.

pulses are negative (ground to -3 V) and of 100 ns duration nominal. Details of the operation of the W102 are contained in its write-up. In the case of a multiport memory module, a pulse must not be sent out through any port other than the one whose cycle is being performed. Similarly, no pulse should be accepted except from the port whose cycle is being performed.

Address Acknowledge

The address acknowledge (ADR ACK) pulse is sent from the selected memory module to the processor when the memory module has decided to accept a memory request as previously described. It must not be sent at any other time. Required timing is shown in Figure 7-3.

Ignore Parity

The IGN PARITY (ignore parity) pulse is sent from the selected memory module to the processor to indicate that the particular memory module does not have provision for storing and transferring parity signals with its data. This pulse should be used by the processor to inhibit parity check alarms (halts, flags, etc.). The IGN PARITY pulse is usually coincident with the ADR ACK pulse, see Figure 7-3 for exact timing specifications.

Read Restart

The RD RS (read restart) pulse generated by the memory module signals the processor that the memory has sent out the memory data and parity. This pulse occurs only during read or read-modify-write cycles. Its timing is shown in Figure 7-3. It usually causes the processor to proceed with its operation.

Write Restart

The WR RS (write restart) pulse is sent by the processor to the memory module to indicate that the processor has sent out the data and parity to be written. This pulse is used only during read-modify-write and write cycles. If no pulse is sent during such cycles, the memories will usually "hang" and must be cleared by the operator. The required timing for the WR RS pulse is shown in Figure 7-3. Note that the timing is different for read-modify-write cycles and for write cycles.

Data and Parity

The data and parity lines are two-way (see Figure 7-5). They are used for data transfer to the processor during read operations and to the memory modules during write operations. The MBD 0 through MBD 35 lines (memory bus data lines) carry the information as pulses with the presence of a pulse

representing a 1 and the absence of a pulse representing a 0. This type of operation requires that the register used to "catch" or receive the data be cleared before the data pulses arrive. The data pulse timing is shown in Figure 7-3 for both read and write operations. The PARITY pulse line is used to transmit odd parity computed over the data to the memory module. It need not be simultaneous with the data. The PARITY pulse timing is shown in Figure 7-3. The processor should compute odd parity and send it to the memory with the data. Though not required, memory parity is helpful for isolating system failures and should be provided if possible. The memory module is not required to check parity, only to store it with the data and send it back to the processor when the data is read out. If a memory module is not equipped to store parity, it must send the processor the IGN PARITY pulse as described above. At most, two receivers may be enabled in the active memory module. No receiver may be enabled in an inactive memory module.

As specified previously, the data pulses must be transmitted with W102 pulsed bus transceivers. However, in the processor, it is often convenient to load the MBD data directly into more than one register (for example, the memory buffer and parity buffer). For this purpose, the MBD and PARITY lines may be received by either a W102 or by a B-series 2 mA diode gate such as the B133. The diode gate must be an AND for negative inputs and one input must be used to inhibit the gate. (The use of 2 mA diode gates such as the B133 as receivers is discouraged as their noise margins are not as good as the W102 receiver for this service.) At most four receivers may be used on any MBD line in a processor and at most two of them may be enabled at one time. (In order to meet bus loading requirements, no receiver in the processor may be enabled when the processor is transferring information to the memory.)

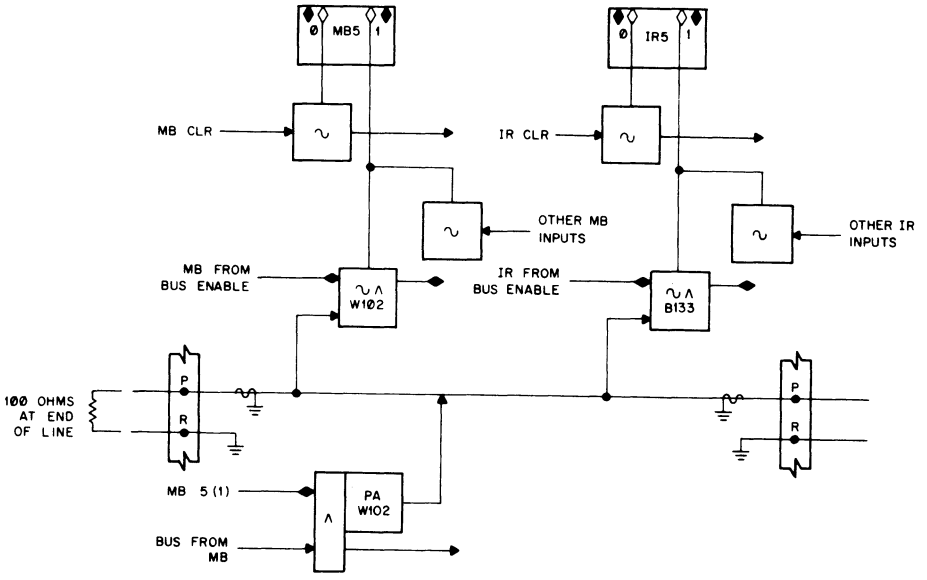
Multiplexor Control: REQn

The REQn (request) signal is a negative level sent by a peripheral processor requesting control of the memory multiplexor. Use a B683 or B684 bus driver to generate this level. The timing for REQn is shown in Figure 7-3. This line must be terminated by a 100 Ω resistor in the peripheral processor (and in the multiplexor).

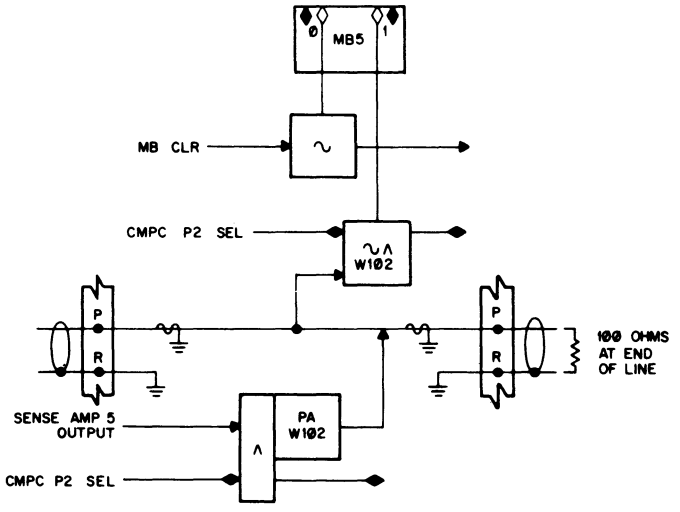
ACKn

The ACKn (acknowledge) signal is a negative level sent from the memory multiplexor to a peripheral processor signifying that the processor has control of the multiplexor. Unless this line is true (negative), a peripheral processor must disable all of its interface lines (both the B683 and W102 have provisions for this). Once the ACKn level is received, the processor may treat the multiplexor bus as though it went directly to the memory modules. If a peripheral processor is designed to work through the memory multiplexor, but is actually interfaced to the memory bus, the ACKn line should be held negative by connecting it to a source of -3 V with a W990 card (see Table 7-2). The peripheral proces-

sor may load the ACKn line with 6 mA maximum at ground or -3 V. 2 mA B-series modules are recommended for receiving the ACKn signal. The ACKn line must be terminated with 100 Ω in the peripheral processor and in the memory multiplexor.



Processor Data (or Parity) Connections



Memory Data (or Parity) Connections

Figure 7-5 Data and Parity Lines

Multiplexor Clear

The multiplexor clear pulse (MPX CLR) allows a peripheral processor to clear the memory multiplexor, if the processor should decide that the multiplexor is "hung." The processor should send this signal whenever a non-existent memory condition is detected. This pulse, like all pulses in the memory bus and multiplexor bus, must be interfaced with a W102 pulsed bus transceiver. This line must be terminated with 100 Ω in the peripheral processor.

Nonexistent Memory

A processor should determine whether the memory it has addressed exists by waiting 100 μs from the time it makes its REQ CYC line true. If no ADR ACK pulse is returned within that time, no memory with the given address exists. The processor may halt or trap to an error subroutine under this condition.

Faulty Requests

A memory module intended for multiprocessor applications should also recover from faulty requests (such as a write request with no WR RS following) by waiting 100 μs and restarting itself. To aid in processor maintenance, this feature should be capable of being disabled by a switch when desired.

System Integrity During Power Off

The PDP-10 memory bus design allows an idle processor or memory to be shut off without affecting memory bus operation. Conversely, turning on a memory or processor should not disturb bus operation either. To accomplish these goals, several requirements must be met. The REQ CYC line must not be true (even briefly) as a processor is turned off. This is accomplished by "crobarring" the REQ CYC driver with a signal which is grounded before the power supply voltage starts to fall, and which remains grounded until the power supplies have risen at the next turn-on. This type of signal is furnished by the 844 Power Control or may be derived by other means. A special input is provided on the B683 for the purpose of crobarring the driver; the B684 can be crobarred by using the voltage setting connection (pins K and U). A processor which is designed for use with the MX10 Memory Multiplexor must also have all of its MA lines crobarred before its power supplies fall to prevent interference with some other processor which may be active. Neither a memory nor a processor may transmit spurious pulses during turn-on or turn-off. To prevent this, it is adequate to insure that at least one input of every W102 transmitter remains at ground during turn-on and turn-off. In a processor which will not

work with a memory multiplexor (such as the KA10), this requirement is waived as no other data can be on the bus lines and therefore subject to interference from spurious pulses. Both B683s and W102s are designed so as not to interfere with the operation of a shared bus even though their own power supplies are off.* The presence of a B684 as a bus driver precludes the sharing of a bus.

Maximum Loading

A memory bus may have at most 16 memory modules on it. A memory bus always has one processor or memory multiplexor on it. The smallest memory module size which lends itself to easy decoding of selection bits is 8 K (8192) memory locations. Any size memory module (up to 262,144) is allowed.

Maximum Bus Length

The maximum propagation delay of a memory bus is 150 ns one-way from the processor to the furthest memory module. For 67% propagation factor transmission line (as supplied with the standard bus cable assemblies) this means 30 m maximum length (98 ft) including wire runs through each memory module. By locating the processor in the middle of the bus (not possible with the KA10 processor), the maximum physical bus length can be as long as 60 m (196 ft).

The maximum length of a multiplexor bus is determined by the following rule: when the MX10 Memory Multiplexor is used, the maximum propagation delay from the furthest processor on the multiplexor bus through the memory multiplexor to the furthest memory module on the associated memory bus is 150 ns one-way. With 67% propagation factor transmission line, this means 30 m maximum length (98 ft) including wire runs through each memory and processor and including 30 ns delay (6 m, 20 ft) through the memory multiplexor. If the memory multiplexor is adjacent to the only memory module on its memory bus and in the center of its multiplexor bus, the maximum multiplexor bus length is 48 m (~~136~~ 156 ft). See Figure 7-1.

CONTROL FUNCTIONS OF AN I/O PROCESSOR ATTACHED TO A MEMORY BUS

The memory control functions imposed upon any I/O processor on the memory bus have been explained previously and are quite simple in concept. It is frequently useful to consider the memory control functions as a hardware subroutine which is "called" by other functions of the processor and "returns" to the calling function after reading or writing memory. See Figure 7-6.

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*This applies only to W102s with board revision F or later revisions.

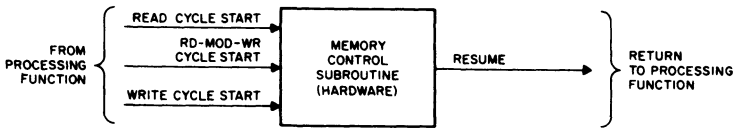


Figure 7-6 Memory Control Functions

A hypothetical implementation of such a hardware subroutine is shown in Figures 7-7 through 7-12. The example is similar to the memory control in the KA10 Central Processor. It has not been designed to minimize data destruction in the event of module failures (a design philosophy worth implementing in many applications). The example also assumes that the "modify" process involved in a read-modify-write cycle is a single simple process. Extensions and modifications of the design are straightforward, however.

Figure 7-8 illustrates how the various enable levels generated within the I/O processor might be gated with the I/O processor's timing chain if desired and then converted to standard 40 ns negative pulses. The resulting pulses are used to select the desired type of memory cycle by means of the flip-flop register in Figure 7-9.

When the addressed memory responds with ADR ACK (address acknowledged), REQ CYC (request cycle) is lowered. If the requested cycle was read only, the data is sent to the I/O processor together with parity. The I/O processor should check the received parity and restart itself upon receipt of the RD RS (read restart) pulse from memory. Conversely, during a write only cycle request upon receipt of ADR ACK, data is sent to memory together with generated parity and WR RS (write restart). A read-modify-write cycle combines the operations cited above.

There are several features which a processor should have. For example, should an error occur, the processor ought to recover without "hanging" the memory. A manual power clear or reset might also be provided.

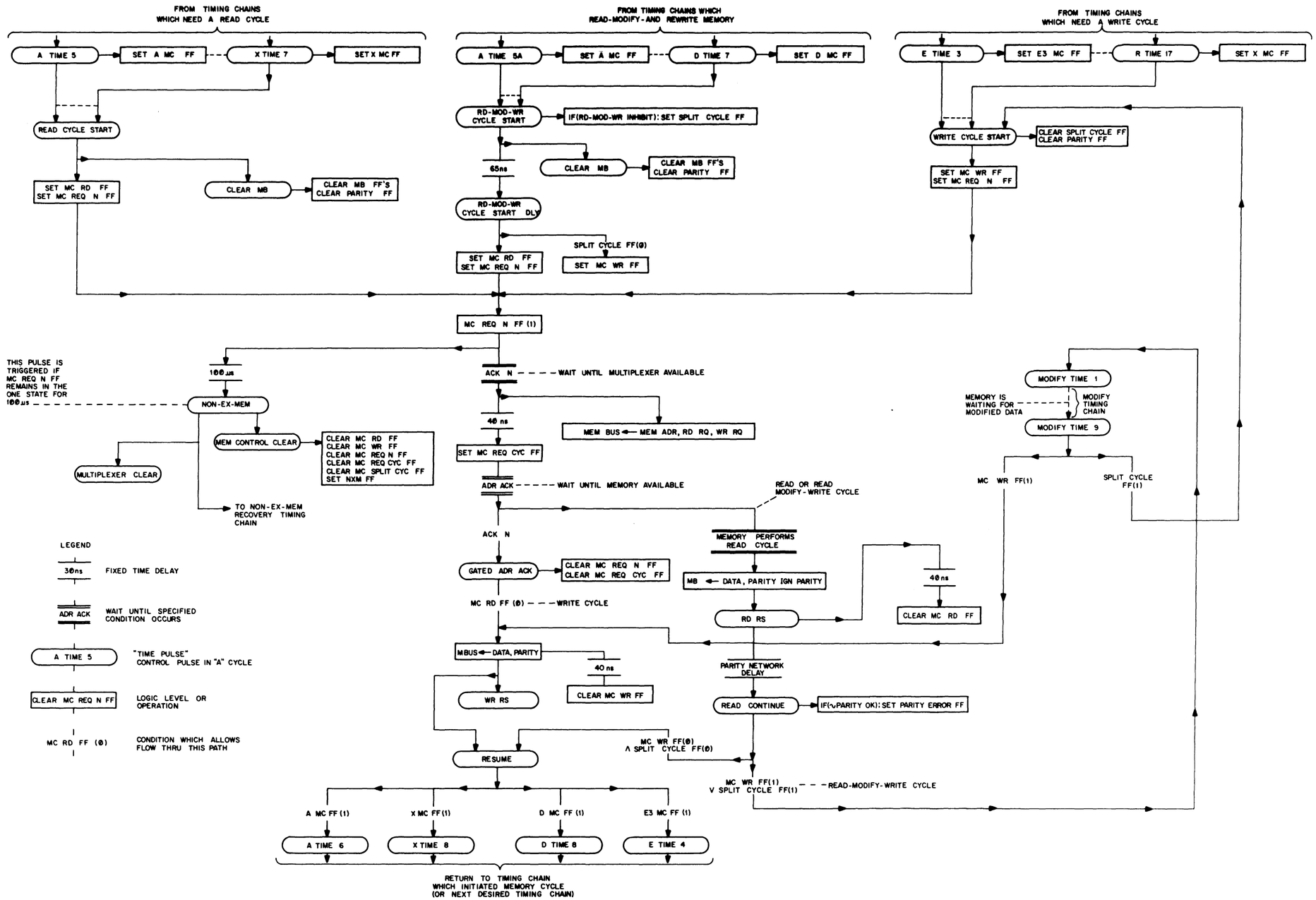


Figure 7-7 Hypothetical Memory Control Flow Diagram

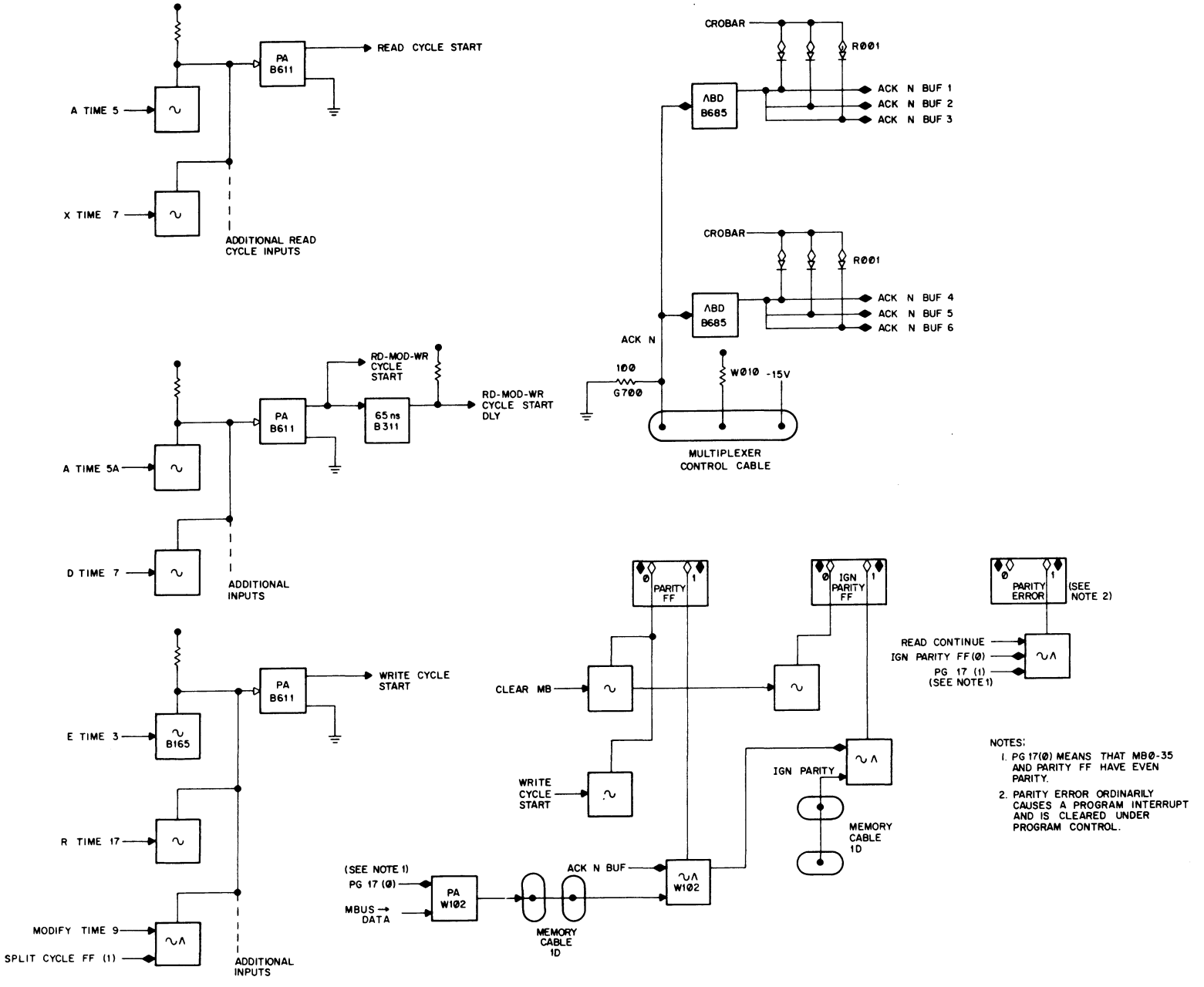


Figure 7-8 Enable Level Generator

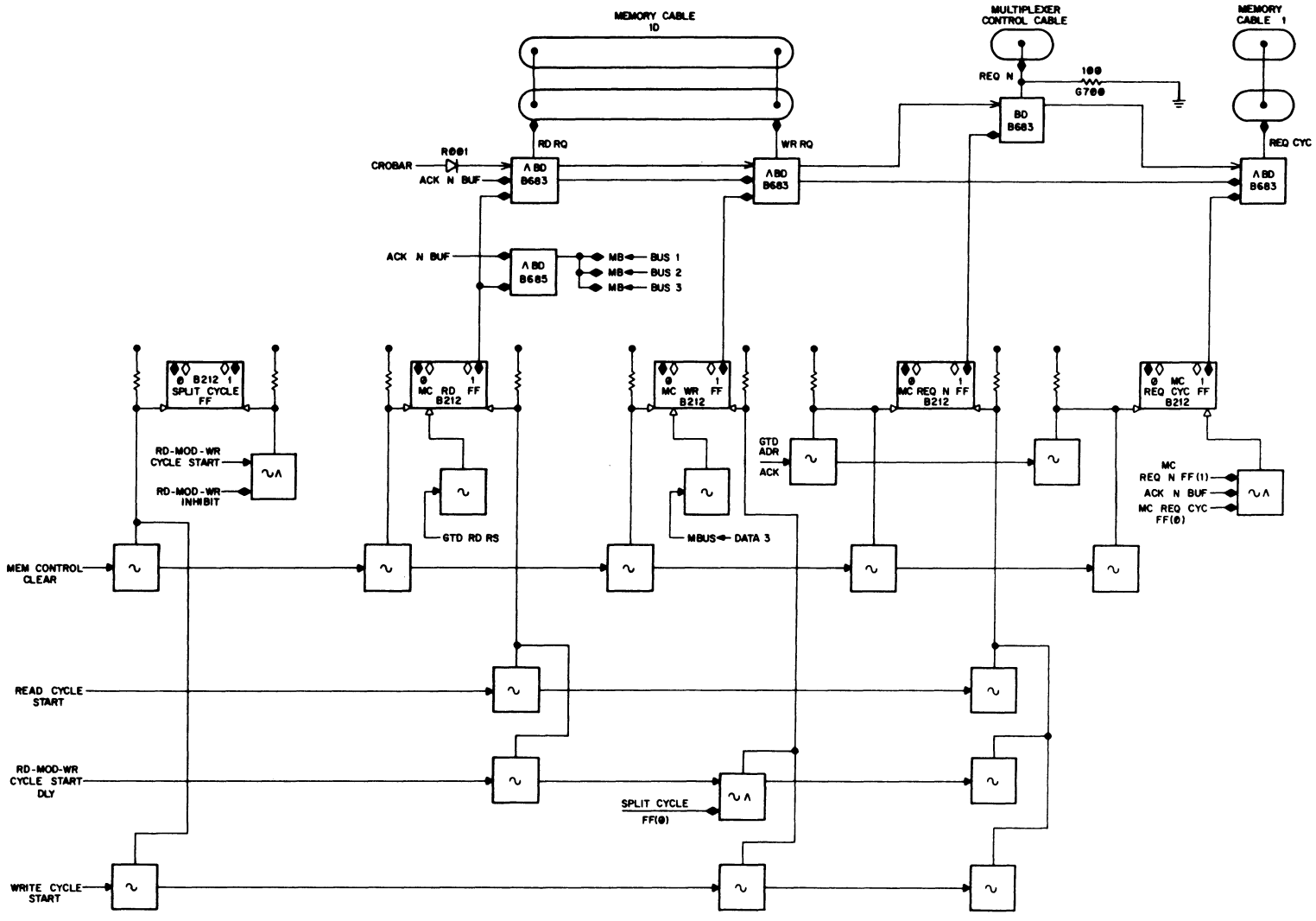


Figure 7-9 Memory Cycle Flip-Flop Register

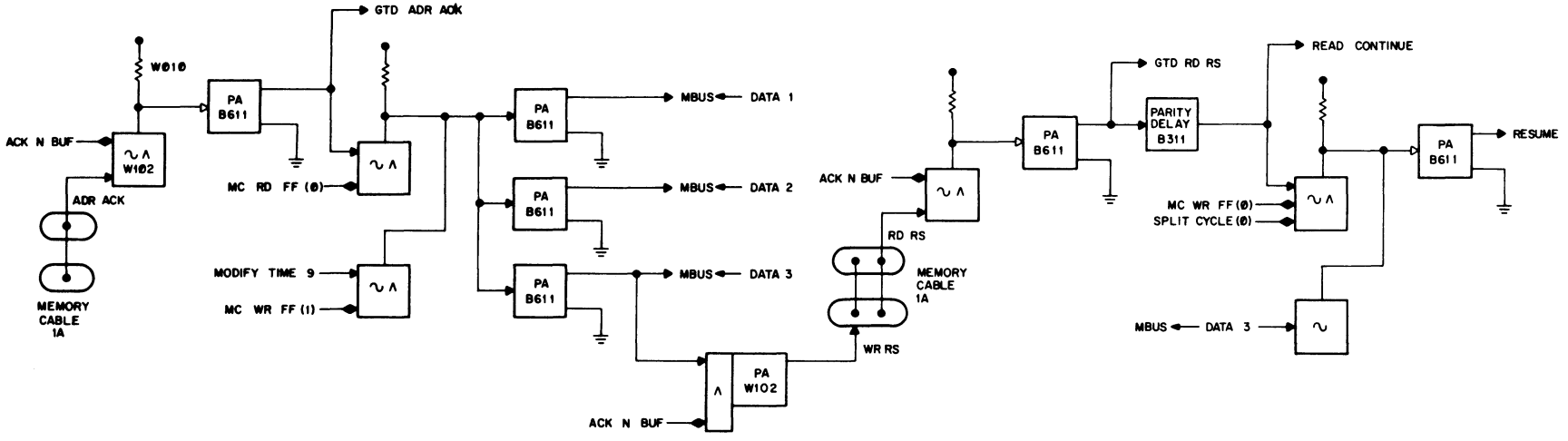


Figure 7-10 Memory Cycle Timing Chain

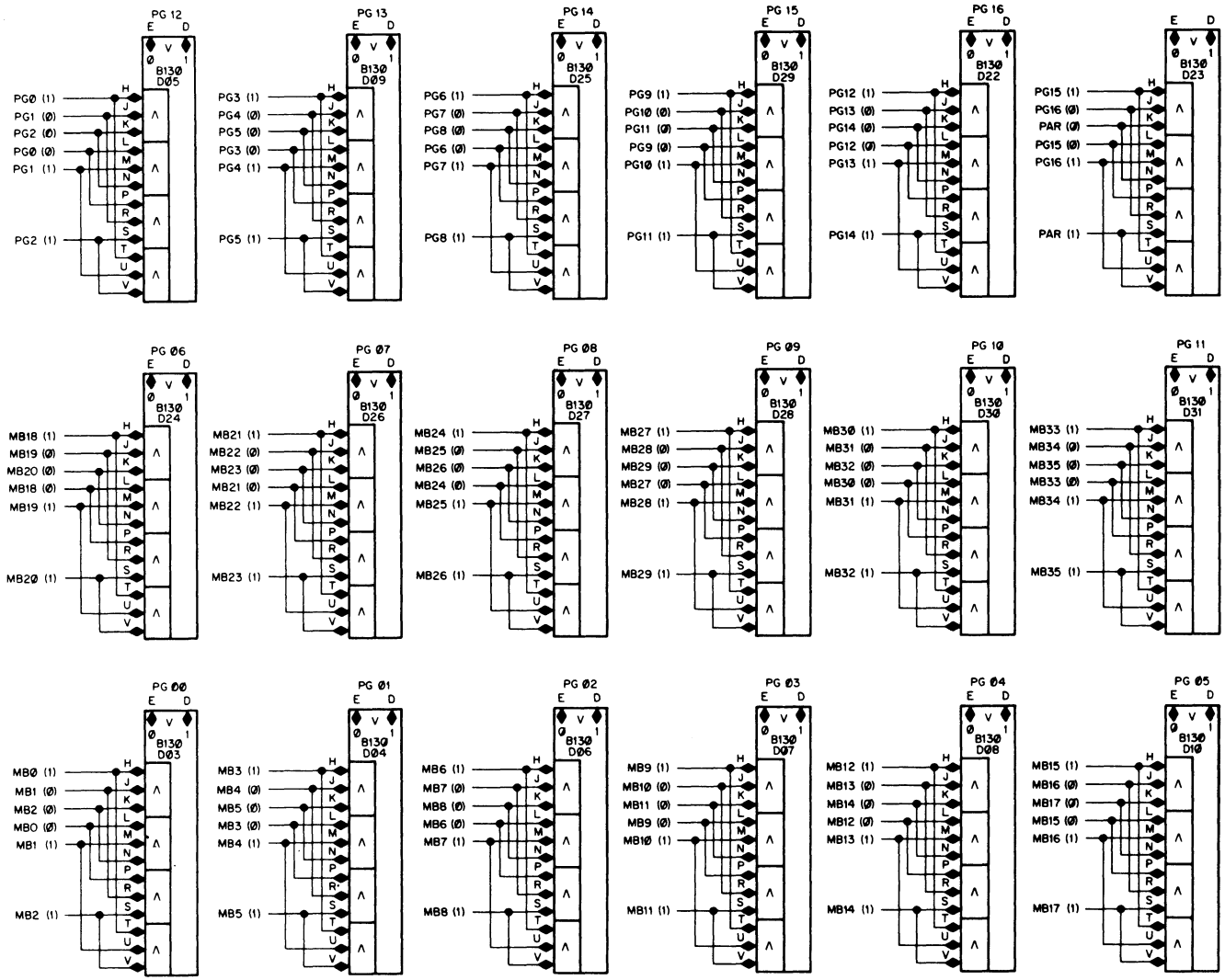


Figure 7-11 Data Parity Generation

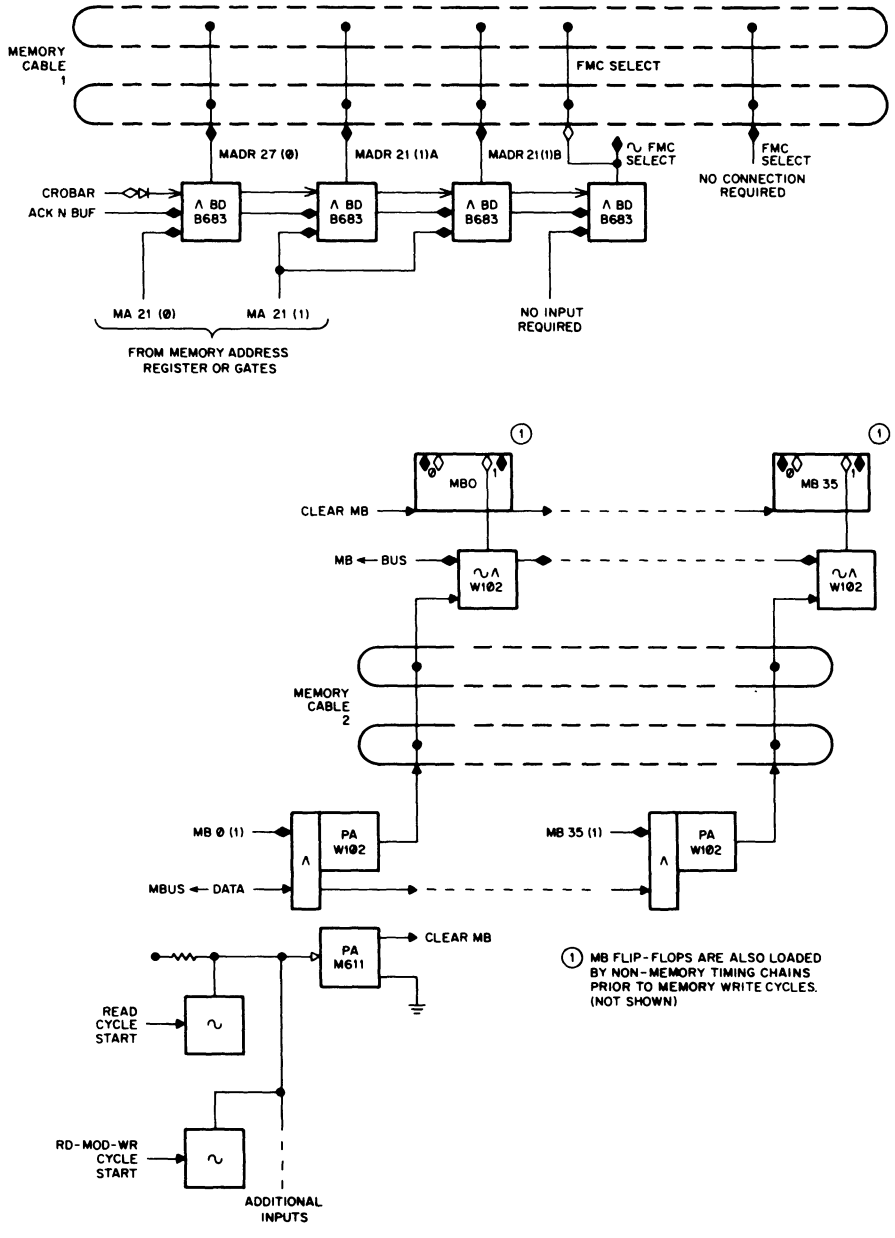


Figure 7-12 Memory Bus Address and Data Interface

CHAPTER 8
CHANNEL AND CHANNEL BUS DESCRIPTION

The channel (see Figure 8-1) is a device which communicates directly with the PDP-10 memory system (either directly on a memory port or through the multiplexor) and allows transfers of blocks of data between the memory and the channel bus. The channel bus, which is normally used by high transfer rate I/O devices, contains a 36-bit data register, an 18-bit data address register and an 18-bit word counter. Additionally, to facilitate scatter-write gather-read operations, the channel contains an 18-bit control word address register (program counter) which specifies the memory address in which the next initial data address and word count are located.

Channel Bus

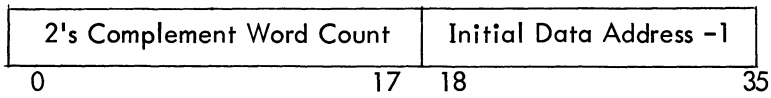
The channel bus (see Figure 8-2), which is seen by the user, consists of the following signals:

36 bidirectional data pulse lines	These signals are 100 ns negative pulses (ground to -3 V) with no overshoot.
CHANNEL PULSE	This 100 ns negative pulse is sent from the channel. It accompanies the data pulses when the channel is sending data to the device. It signifies the channel is ready to receive data when data flow is away from the device.
DEVICE PULSE	This 100 ns negative pulse is similar in function to the CHANNEL PULSE signal. It accompanies the data when the device is sending, and signifies the device is ready to receive when data flow is toward the device.
CHANNEL START	This is a level (-3 V for true) which is sent from the device to the channel. It will start the channel into operation when asserted. It must remain true for the entire operation time. When this signal goes false, the channel will terminate. This signal must be synchronized to avoid interference with another device.
SAWRITE	This signal controls the direction of data transfer. When true, it signifies the device is writing some medium (reading memory). The timing is the same as that for CHANNEL START. The signal is -3 V when asserted.
CHANNEL BUSY	This signal comes from the channel and is asserted (-3 V) sometime after CHANNEL START is asserted from the device. The device must not put anything on the bus until this signal is asserted. When this signal goes false after having been true, the channel has terminated for one reason or another. CHANNEL START and CHANNEL BUSY must both be false for at least 400 ns prior to reassertion of CHANNEL START.

WRITE CONTROL WORD REQUEST	This negative 100 ns pulse from the device causes the channel to store the current contents of the data address register and control word address register into memory location IA + 1 where IA (an even number) is the channel initial control word address. The contents of the control word register go into bit positions 0-17 and the contents of the data address register into 18-35. Upon any channel termination, an automatic WRITE CONTROL WORD REQUEST is made.
CONTROL WORD WRITE COMPLETE	This pulse from the channel signals the completion of the operation requested above. This pulse does not occur on the automatic transfer caused by termination.
NO SUCH MEMORY	This pulse is sent from the channel as CHANNEL BUSY goes off and indicates that the memory addressed failed to respond within 100 μs.
CONTROL WORD PARITY ERROR	If a control word is fetched from the memory by the channel and this word has a parity error, CHANNEL BUSY goes off and this pulse is sent to the device from the channel.
DATA WORD PARITY ERROR	This pulse accompanies the data and the CHANNEL PULSE when a data word which was read from memory with a parity error is sent to the device.
CHANNEL RESET	This pulse forces the channel to its clear state. This signal is dangerous to use since it may hang memory if asserted at the wrong time. It should be used only in desperation.
WRITE EVEN PARITY	This level when asserted at the beginning of an operation will cause the channel to write even parity into memory on all data words received from the device. A control word written into memory will still have odd parity, however.

Control Word

The control word for the channel is loaded from the memory into the data address register and the word counter. The format is shown below.



For the sake of convenience, we will refer to the word counter as WC and the data address register as DA. DA is incremented by one prior to the first transfer.

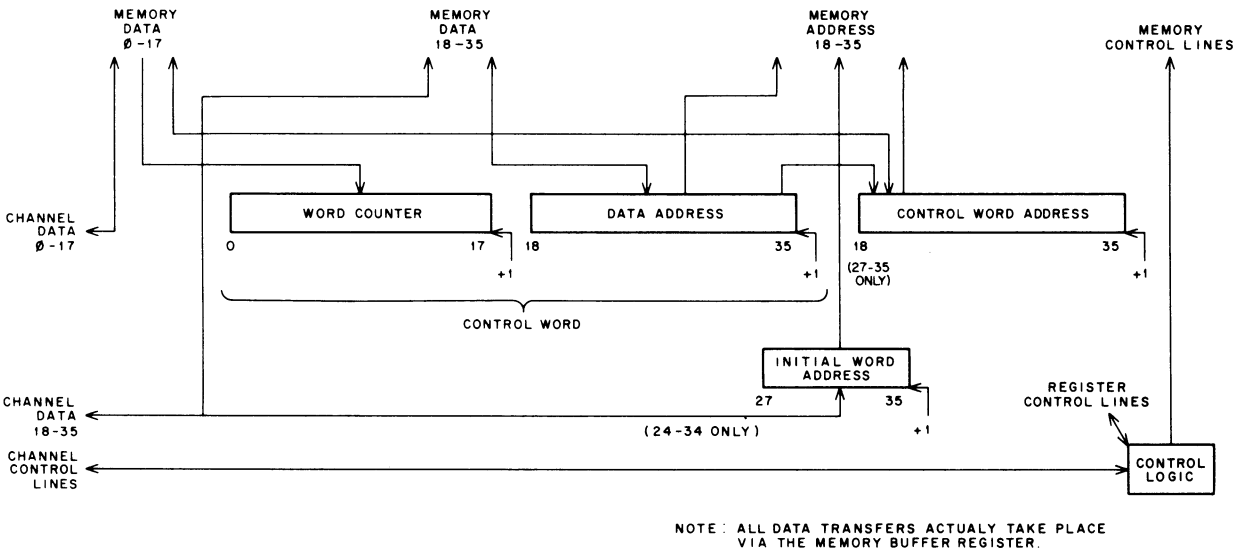


Figure 8-1 Channel Register Organization

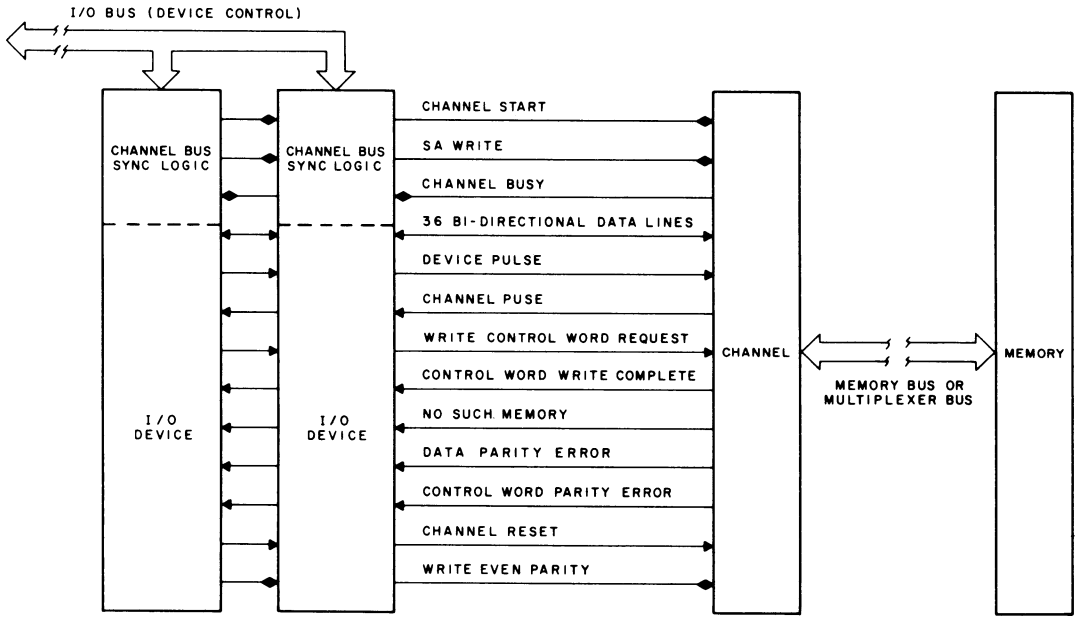


Figure 8-2 Channel Bus

Address 0 in the PDP-10 memory system has a special significance. Thus, in a newly fetched control word, WC = 0 and/or DA = 0 have the special meanings as shown below.

WC	DA	Action
=0	=0	Terminate the channel. Set CHANNEL BUSY false.
=0	≠0	DA is sent to the control word address register and a new control word is fetched from that location in memory.
≠0	=0	If SAWRITE is false (writing memory), the channel will receive the number of words specified by WC from the device, but will not put them into memory. This feature is useful for tape and disk applications. See examples.
≠0	≠0	Transfer the number of words indicated by WC. Transfer the first word into or from the address specified by DA + 1. After each transfer, increment the DA register by 1 and transfer the next word to or from the incremented address.

INITIAL CONTROL WORD ADDRESS

The control word initial address, IA, (an even number) is supplied by the device. Immediately upon receiving the CHANNEL BUSY signal from the channel, the device should send eight bits of initial address (bits 27 through 34) on the data bus and the DEVICE PULSE. There is no "latest time" for sending these signals. The channel will wait indefinitely to receive them. Bits 0 through 26 and 35 must be 0 to insure proper operation. Further, it is required that IA $\geq 20_8$ since the channel cannot access the fast accumulators when they are provided.

If a control word with WC=0 is stored in the memory location specified by IA, the channel will load DA into the control word address register and fetch another control word from there.

The control word address register is incremented by one after each control word fetch. Thus when the number of words specified by the word count of a particular control word has been transferred, a new control word is fetched from the address following the one from which the previous control word was taken.

TYPICAL PROGRAM EXAMPLES

All numbers are in octal representation.

Memory Location	Contents	
	WC	DA
IA	0	1000
1000	777700	1777
1001	0	0

If SAWRITE is not asserted by the device, the channel will accept up to 100 words from the device, and store them sequentially in memory locations 2000 through 2077. The channel will then clear the CHANNEL BUSY signal. Note that 1001 must contain 0 to stop the channel.

Memory Location	Contents	
	WC	DA
IA	776000	4777
IA +1	0	0

If SAWRITE is asserted the channel will deliver up to 2000 words to the device. The first word will come from 5000 and the others sequentially from there. The channel user should take care to understand that if the device sends the WRITE CONTROL WORD REQUEST pulse while the CHANNEL BUSY signal is asserted, the contents of IA+1 will change which may cause undesirable consequences.

Memory Location	Contents	
	WC	DA
IA	0	500
500	777700	777
501	777000	4777
502	777300	0
503	777000	5777
504	0	0

If SAWRITE is not asserted and this program runs to completion, the first 100 words delivered by the device (for instance a file header) will be in 1000 through 1077, the next 1000 words will be in 5000 through 5777, the next 500 words will be skipped and the next 1000 words will be in 6000 through 6777. In the case of disk and tape operations, skipping saves memory, and allows this type of transfer without having to reinitiate the device.

If SAWRITE had been asserted, the first 100 words delivered to the device would have come from 1000 through 1077, the next 1000 from 5000 through 5777, the next 500 from 0 through 477 (note that in a PDP-10 system with fast registers, 0 through 17 will not be otherwise available to the processor since to the processor these addresses are fast registers while to the channel they are core memory), and the next 1000 words from 6000 through 6777.

NORMAL OPERATING SEQUENCES

For a device to write the PDP-10 memory through the channel (device reading some medium and transmitting to memory) the following sequence holds for normal operation.

Device	Channel
1. CHANNEL START goes true SAWRITE goes false	
	2. Indefinite delay $\geq$ 50 ns CHANNEL BUSY goes true
3. Indefinite delay $\geq$ 0 DEVICE PULSE and Initial address pulses 27-34	
	4. Indefinite delay $\geq$ 500 ns CHANNEL PULSE
5. Indefinite delay $\geq$ 0 DEVICE PULSE and Data Pulses	
	6. Indefinite delay $\geq$ 200 ns CHANNEL PULSE
Indefinite delay $\geq$ 0 DEVICE PULSE Data Pulses	
	Indefinite delay $\geq$ 200 ns CHANNEL PULSE
etc.	

A normal termination can occur in two ways:

1. The channel fetches a zero control word and clears CHANNEL BUSY.
2. The device clears CHANNEL START. There is no timing restriction on doing this.

Abnormal terminations occur under the following conditions:

1. Control word parity error
2. Non-existent memory

Any termination will cause the current value of the control word address and the data address register to be stored in IA+1 ("Automatic Write Control Word Request").

For a device to read the PDP-10 memory through the channel (device writing some medium from the memory) the following sequence holds for normal operation.

Device	Channel
1. SAWRITE goes true CHANNEL START goes true	
	2. Indefinite delay $\geq$ 50 ns CHANNEL BUSY goes true

Device	Channel
3. Indefinite delay ≥ 0 DEVICE PULSE and initial address pulses Receipt of this pulse by the channel is taken by the channel to mean the device is now ready to receive data pulses. The delay indicated will elapse, however, since the channel must take 2 memory fetches before transmitting the first CHANNEL PULSE	
	4. Indefinite delay $\geq$ 500 ns CHANNEL PULSE and Data Pulses
5. Indefinite delay $\geq$ 100 ns* DEVICE PULSE give another word	
	6. Indefinite delay $\geq$ 60 ns CHANNEL PULSE Data Pulses
Indefinite delay $\geq$ 100 ns* DEVICE PULSE	
	Indefinite delay $\geq$ 60 ns CHANNEL PULSE Data Pulses
etc.	

*See text.

Normal and abnormal terminations are the same. The automatic WRITE CONTROL WORD REQUEST also occurs.

Delays are measured on the bus, at the unit (either channel or device), from leading edge of the incoming pulse to leading edge of the outgoing pulse. In the case of *delays, ten feet of channel bus cable is assumed. If the cable is shortened these delays must be increased by 3 ns for each foot the cable is shortened. If the cable is lengthened, these delays may be decreased, but this is not necessary.

The WRITE CONTROL WORD REQUEST pulse can be sent at any time to the channel. The transfer will take place, and the WRITE CONTROL WORD COMPLETE pulse will be sent, after the

next data word transfer which is not followed by a control word fetch. The contents of the control word address register will be in positions 0 through 17 of memory location IA+1 and the contents of DA will be in 18 through 35.

ELECTRICAL CHARACTERISTICS

Transmitters and receivers for pulses should be W102 cards. These produce 100 ns negative going pulses (ground to -3 V with no overshoot). The transmitter's output impedence is infinite when off.

The W102 receiver input is a diode input requiring 2 mA flowing inward at ground and no current at -3 V.

For levels, transmitters should be B683 cards. Receivers may be any of the B-series diode gates although 2 mA gates used in the PDP-10 system are recommended.

The cable must be terminated in 100 Ω at both ends.

CHANNEL BUS SYNCHRONIZATION

If a device is designed to operate on a channel bus along with other devices, it must be connected so that it relays CHANNEL START, CHANNEL BUSY, and SAWRITE only under certain conditions. Otherwise, two or more devices on the channel bus may attempt to use the bus simultaneously.

When a device is inactive, it must take CHANNEL START IN (from preceding devices) and send it toward the channel as CHANNEL START OUT (except immediately after a channel termination; see the example). Similarly, it must take SAWRITE IN (from preceding devices) and send it toward the channel as SAWRITE OUT when inactive. It must take CHANNEL BUSY IN (from the channel) and send it to the preceding devices as CHANNEL BUSY OUT when it is inactive.

When inactive, if CHANNEL START OUT or CHANNEL BUSY IN is true, the device must remain inactive.

The device may go active 400 ns after CHANNEL BUSY IN and CHANNEL START OUT both are false. When active, the device controls the state of the SAWRITE OUT signal and asserts CHANNEL START OUT. When CHANNEL BUSY IN becomes true, the device can send the initial control word address (and the DEVICE PULSE) and otherwise begin data transfer. The device must not assert CHANNEL BUSY OUT since it would cause other devices further down the bus to become active also.

When termination occurs (whether caused by the device or the channel) the device must keep CHANNEL START OUT and CHANNEL BUSY OUT false until 400 ns after CHANNEL BUSY IN and CHANNEL START OUT go false.

The synchronizing logic must be designed so that no glitches occur on CHANNEL START OUT or CHANNEL BUSY OUT. SAWRITE OUT is less critical as it is not used until the initial control word address transfer to the channel.

The device must not assert nor observe the state of any of the channel bus signals not mentioned above until the device is active and is asserting CHANNEL START OUT (not relaying it) and observes that CHANNEL BUSY IN is asserted.

Figure 8-3 shows one set of channel bus connections. All signals (including spares) should be wired from the "input" channel bus connectors (from preceding devices) to the output channel connectors (toward the channel) except CHANNEL START, CHANNEL BUSY, and SAWRITE. These three signals should go through logic as described above. CHANNEL START IN, SAWRITE IN, and CHANNEL BUSY OUT should appear in the "input" connectors; CHANNEL START OUT, SAWRITE OUT, and CHANNEL BUSY IN should appear in the "output" connectors. These six lines must be terminated with 100 Ω in each device. All channel bus lines must also be terminated at the end of the channel bus (farthest from the channel) in 100 Ω, using, for example, G700 and G703 terminating modules.

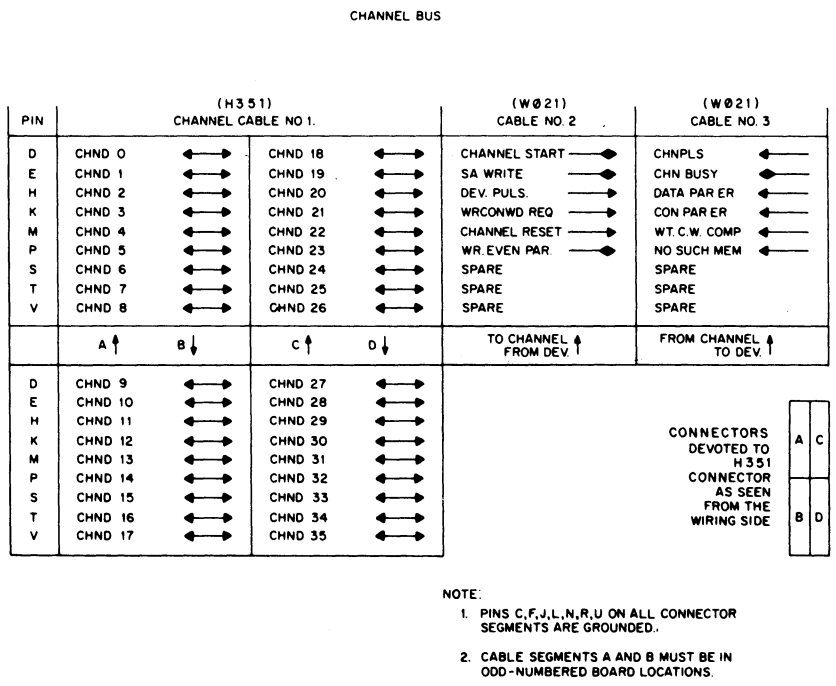


Figure 8-3 Channel Interconnections

Figure 8-4 shows a possible realization of the channel synchronizing logic required above. Figure 8-4 does not show necessary power clear logic and crobar connections.

The flip-flops and pulses generated to synchronize the channel bus are also useful to control the device itself.

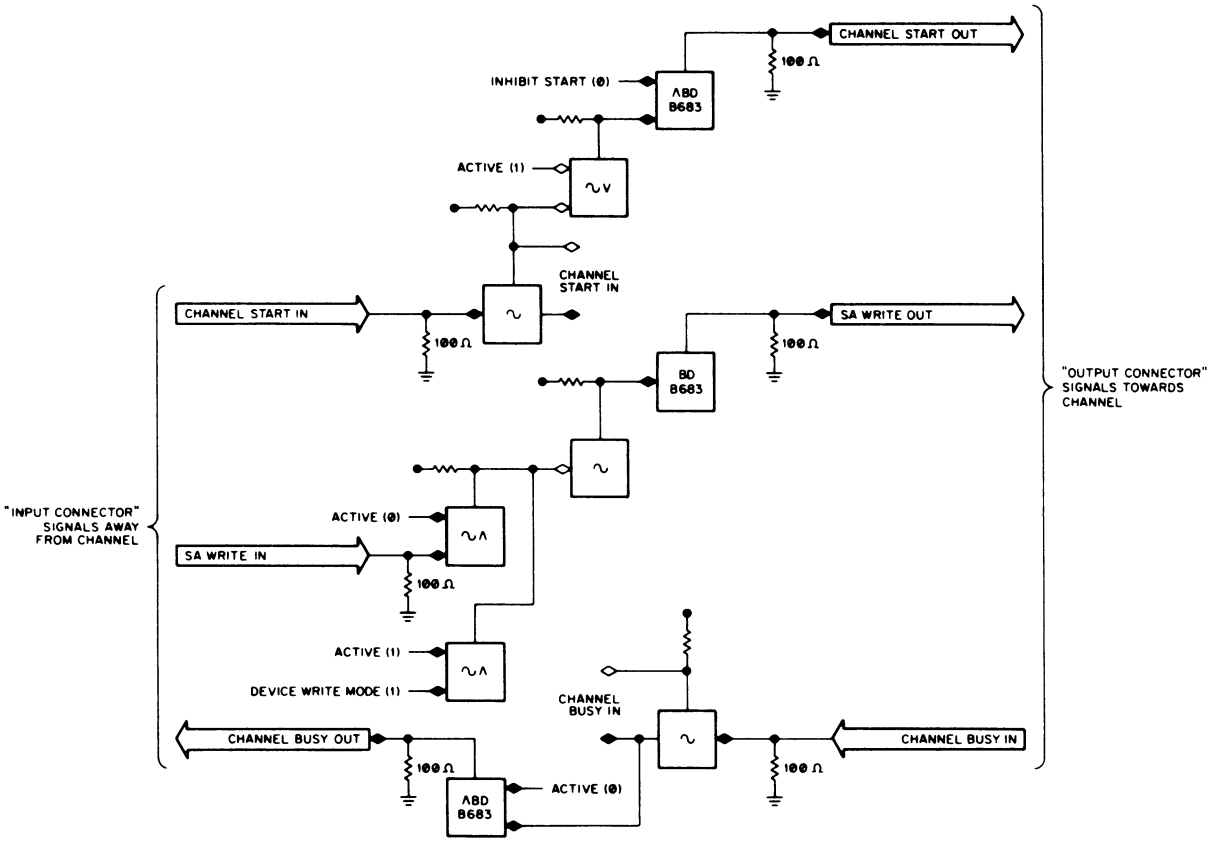


Figure 8-4 Channel Bus Synchronizing Logic

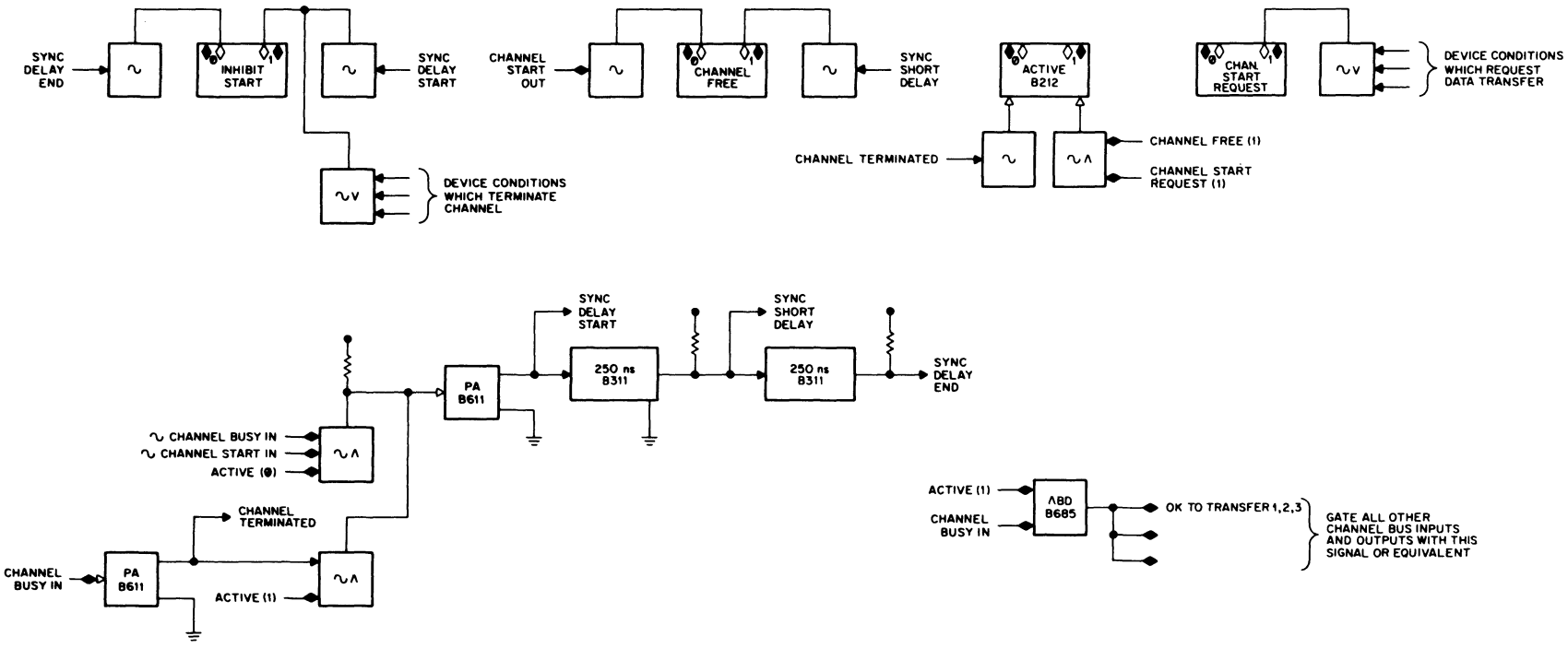


Figure 8-4 Channel Bus Synchronizing Logic (Cont)

CHAPTER 9
PDP-10 MARGIN CHECK BUS

Margin checking is a time-saving method of preventive and corrective maintenance, whereby the tolerance of a section of logic to a change in the nominal voltage gives an indication of the condition of the circuitry. A decreasing tolerance to voltage changes (that is, the logic fails at smaller deviations from nominal voltage) would indicate a degradation of circuit performance.

Margin checking in the PDP-10 system is generally done one logic row at a time. The method used for monitoring the margin voltage differs from previous DIGITAL margin check methods. Since the PDP-10 is a much larger system than previous ones, voltage drops in the margin lines are significant. For this reason, monitoring of the margin voltage is done as close to the logic as possible by means of meter return lines. Referring to Figure 9-1, which is a simplified schematic of the margining system, voltage drops between the variable power supply and the section of logic under test have no effect on the meter reading, and any drop between the logic and meter is negligible since the meter current is small.

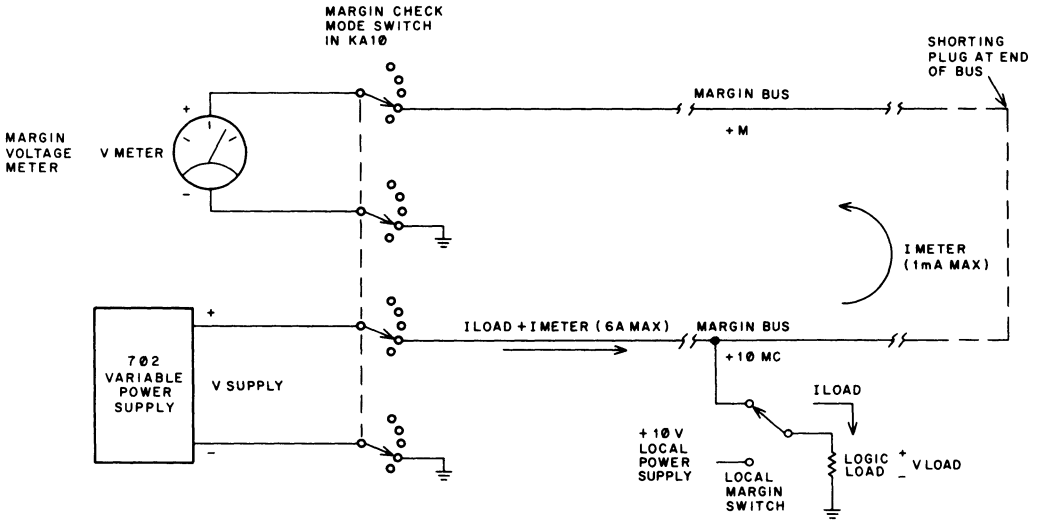


Figure 9-1 PDP-10 Margin Bus Voltage Drops

As shown in Figure 9-1, the margin voltage line and the meter return line are connected together at each end of the system; i.e., in the last cabinet at the left and right ends of the margin bus. Margining is done either to the "left" or "right", with the processor considered to the "left". As shown in Figure 9-2, "left" or "right" designates a physical direction. The maintenance control panel

margin switch indicates which direction is being margined and monitored: -15L, +10L, OFF, +10R, -15R. The "right" bus follows the I/O bus; the "left" bus follows the central processor memory bus.

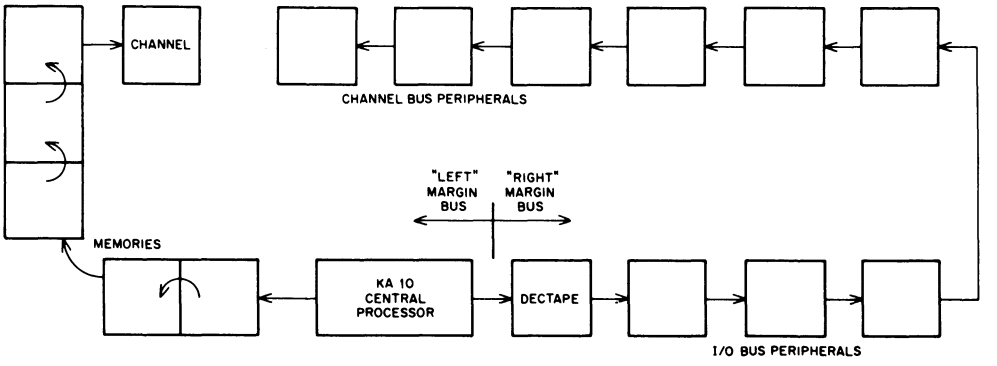


Figure 9-2 Margin Check Bus Layout

As shown in Figure 9-3, the voltage lines are common to both the left and right margin buses. Figure 9-3 is a simplified schematic of the maintenance control panel. A few points concerning the circuitry may be made:

1. The voltmeter is zero-left, and when the mode switch is OFF continually monitors the variable power supply output.

2. The variable supply (Type 702) has its output floating until a margin check is made. At this time the proper side of the supply is grounded.

3. The 702 Power Supply provides the variable dc voltage for margin checking. Up to 7A is available (at 20 V) from the margin check bus.

4. If a switch on a Margin Check Switch Panel is inadvertently left in the MC position while the maintenance panel switch is OFF or margining in another mode, the correct fixed voltage is supplied to the logic through a margin voltage line.

5. If this situation occurs, the following current is available: +10 V line, 4A; -15 V line, 5A. If both fixed voltages are used (again, through error), the currents are limited by $5I_{10} + 6I_{15} \leq 30A$. For example, 1.2A at +10 V and 4A at -15 V.

To allow compatible operation of PDP-6 devices arranged for -15 V remote turn-on, and to turn on the memory modules, a -15 V line is a part of the margin check bus.

The cable used to connect the margin bus everywhere in the system has a male connector (Cinch-Jones P306CCT) at one end and a female connector (S306CCT) at the other. The cable is designated as the BC10B margin check and remote control cable.

The power connector bracket used in MB10 memories and other peripherals having 19 in. cabinets is DEC part number 7005467.

When a Type 164 (PDP-6) memory or other PDP-6 peripheral is connected to the PDP-10 margin check system, the following changes must be made to the PDP-6 power connection bracket (DEC part number 7403950):

1. Rewire the margin bus connectors to agree with the wiring shown on drawing D-PW-164-0-PW revision B or later (Figure 2 on the drawing). That is, remove ground (black wire) from pin 4 of both connectors; bus pin 4 of each connector together (red); bus pin 5 of each connector together (blue); remove the blue wire between pin 6 of the connectors and the -15 V power supply bus if it has not already been removed.

2. Connect the PDP-6 device to the PDP-10 margin bus using a double-male margin check and remote control cable (DEC part number 7005256).

The margin shorting plug used in the last cabinet at each end of the system has pins 1 and 4 and 2 and 5 shorted together. It is a Cinch-Jones P306CCT:

Margin Check Shorting Plug
DEC part number 7005486

The six lines of the margin bus are wired to margin connectors throughout the system as follows:

PIN	1	+MC (positive variable voltage)
	2	-MC (negative variable voltage)
	3	GROUND
	4	+METER (positive return line to meter)
	5	-METER (negative return line to meter)
	6	REMOTE (-15 V for remote turn-on)

As indicated previously, the +METER and -METER lines are not electrically common to the left and right sides of the system (see Figure 9-3).

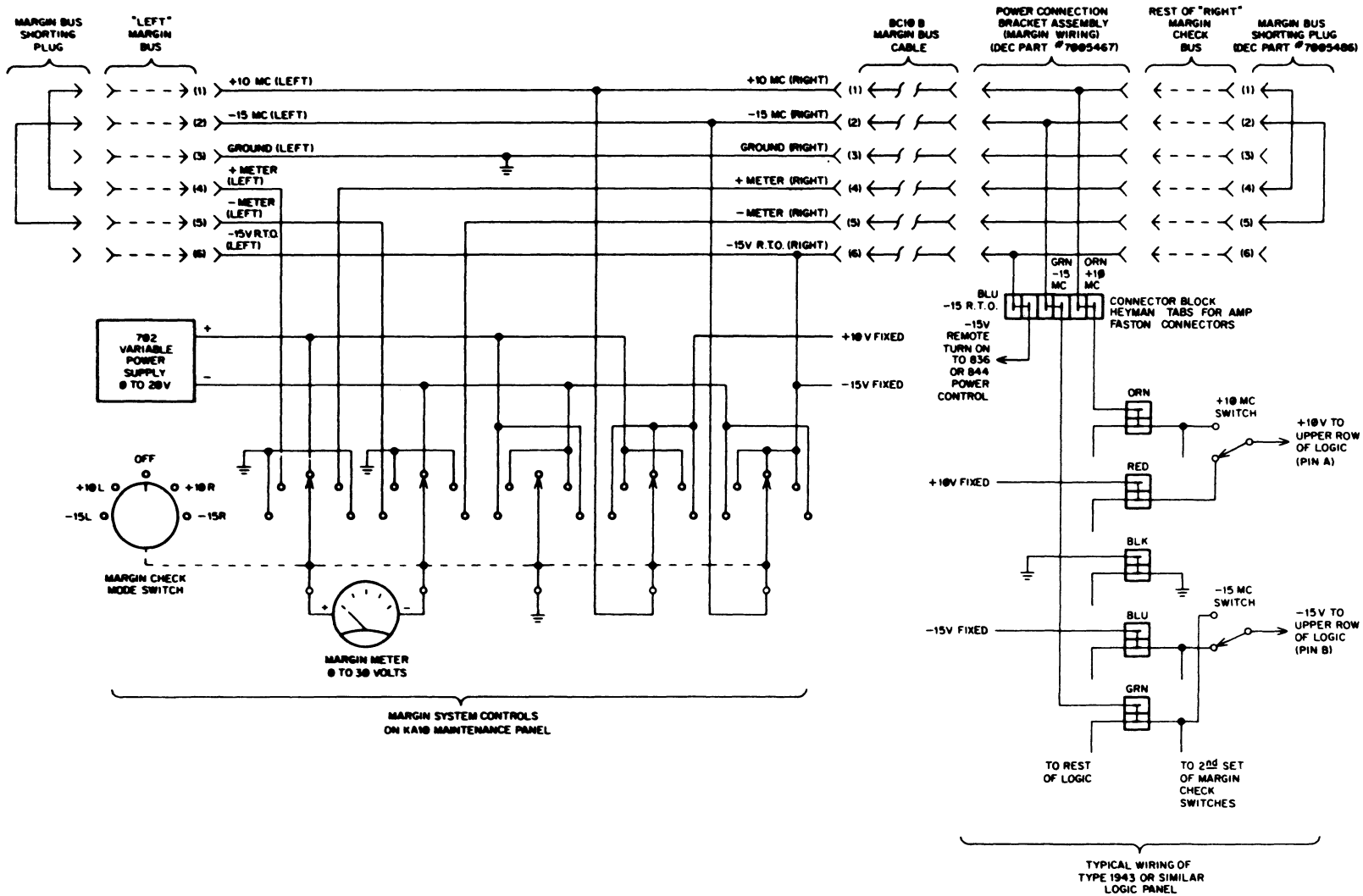


Figure 9-3 Margin Bus Circuit

CHAPTER 10
PDP-10 GROUND MESH SPECIFICATIONS

In order to keep electrical noise and differential potentials under control in the PDP-10 system the following ground system is recommended. Other schemes of grounding which a user might choose may provide adequate grounding. The serious consequences of an inadequate ground system should cause the user to consider carefully any alternate system he provides.

Each cabinet of the PDP-10 system is provided with ground lug terminals. These grounding connections should be tied together as shown in Figure 10-1 with #4 gage copper wire or equivalent. Ordinary stranded #4 gage wire is adequate for this purpose, although #4 gage welding cable (extra flexible stranding) may be preferred by some. DIGITAL supplies a standard grounding conductor with each I/O and memory cabinet. A Burndy QA4C-B solderless lug (or equivalent) is recommended for the cable, and is included on standard DIGITAL ground cables. Upon installation, the purchaser should supply a good earth ground connection to each central processor through #4 gage copper wire or equivalent. In general, an adequate earth ground is provided by a steel beam of a building frame or a reasonably large water pipe. The quality of the earth ground necessary depends somewhat on the use of the system. A system involving a digital-analog interface usually requires that the digital system ground be tied to the analog system ground at a single point, often at the analog-digital interface. Quite a good ground connection is usually required in these cases. In small systems where no analog interface is involved, the grounding provided by a large electrical conduit may be adequate, although electrical conduit systems often are connected together rather poorly in terms of a low resistance path to ground. In large systems, additional connections to earth ground may also be advisable. All of these ground connections are in addition to (not in place of) the ground leads carried along through the various signal buses (memory, I/O multiplexer and channel buses) and the ground conductors contained in the power (mains) cables. The green wire in the power (mains) cable must also be returned to ground, usually through the conduit of the electrical distribution system.

When two cabinets are joined together, they should be electrically bonded together by running a #4 gage conductor or several copper mesh straps between the two cabinets.

Auxiliary units such as the line printer and card reader should be grounded to their associated control cabinets with #4 gage copper wire. #6 wire can be used in this case if desired.

In general, ground conductors should follow the path of the data buses through the system (i.e., in parallel with the memory buses, the I/O bus, the channel bus, etc.).

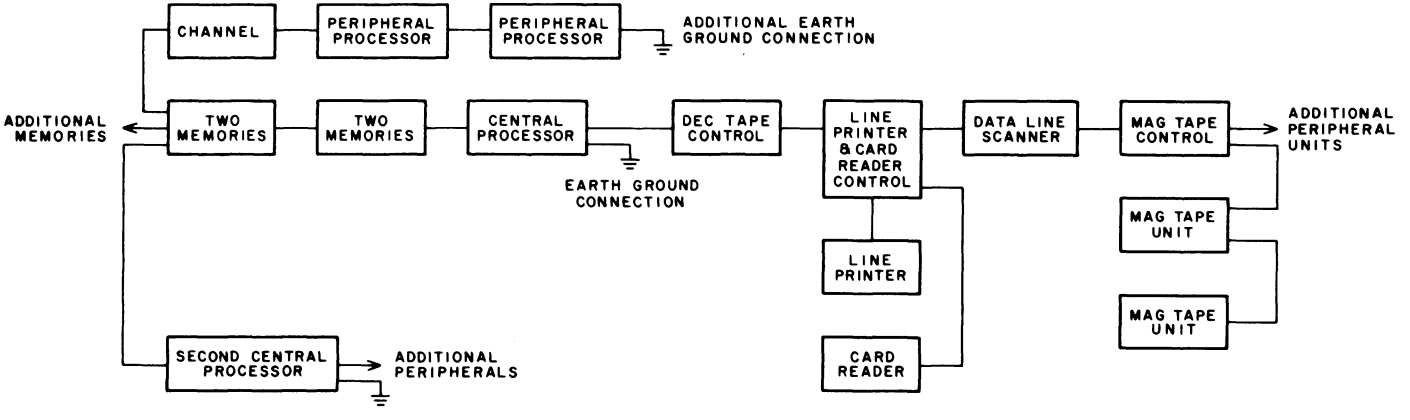


Figure 10-1 PDP-10 System

CHAPTER 11
PDP-10 GENERAL WIRING RULES AND SUGGESTIONS

In building a logic assembly of any but the smallest size, the wiring interconnecting the logic modules forms an important part of the logic. Improper wiring may lead to unreliable operation of the logic. DIGITAL logic will generate waveforms whose rising edges contain frequencies over 100 MHz. At these frequencies the inductance, mutual inductance, capacitance, and transmission line properties of the wiring become quite noticeable. To avoid potential problems the following rules or guidelines are provided.

The propagation delay of typical wiring is 1.5 ns/ft (4.5 ns/m). Although this delay is usually small in comparison with gate delays, it is often significant when overshoot and reflections are considered.

The current carrying capacity of a wire is only V/Z_0 until the wave (change) has propagated along the wire three times (4.5 ns/ft 13.5 ns/m). Typical wiring has a characteristic impedance (Z_0) in the neighborhood of 150 Ω so that the current available at the end of the wire for rising waveforms is only 20 mA until reflections propagate regardless of the source current available. Conversely, the initial voltage fall produced by a clamped load is IZo or 1.5 V for a 10 mA clamped load and 150 Ω characteristic impedance wiring.

The inductance and capacitance of the wiring combine to produce high frequency ringing on the transitions of waveforms. This ringing can be controlled by either resistively terminating the line with approximately 100 Ω if the circuit will drive it (B-series pulse amplifiers) or with the DIGITAL level terminator circuit incorporated into the G796, G704, B163, and other modules. This clamp circuit prevents the waveform from going more negative than -3.5 V and from going more positive than ground.

The mutual inductance and mutual capacitance of the wiring also causes high frequency cross-talk which may produce false operation of the logic. This can be reduced by minimizing the number of high frequency signal components through the substitution of slower R-series logic instead of B-series, by clipping or clamping high frequency ringing with a level terminator circuit, or by wiring with short wires and/or twisted pair, thereby reducing coupling.

A good ground system is essential to reliable logic operation. The following is recommended: (1) Bus the ground and power pins (pins A, B, and C) in each module row with Type 932 Horizontal Bussing Strip. (2) Tie the ground bus strips to chassis ground approximately every two inches (once per H800 module block) using solid wire and white spaghetti insulation. (3) Wirewrap all grounded pins together down each vertical module row (pins C and other ground pins). This ground mesh (see Figure 11-1) will form a good base for satisfactory logic performance.

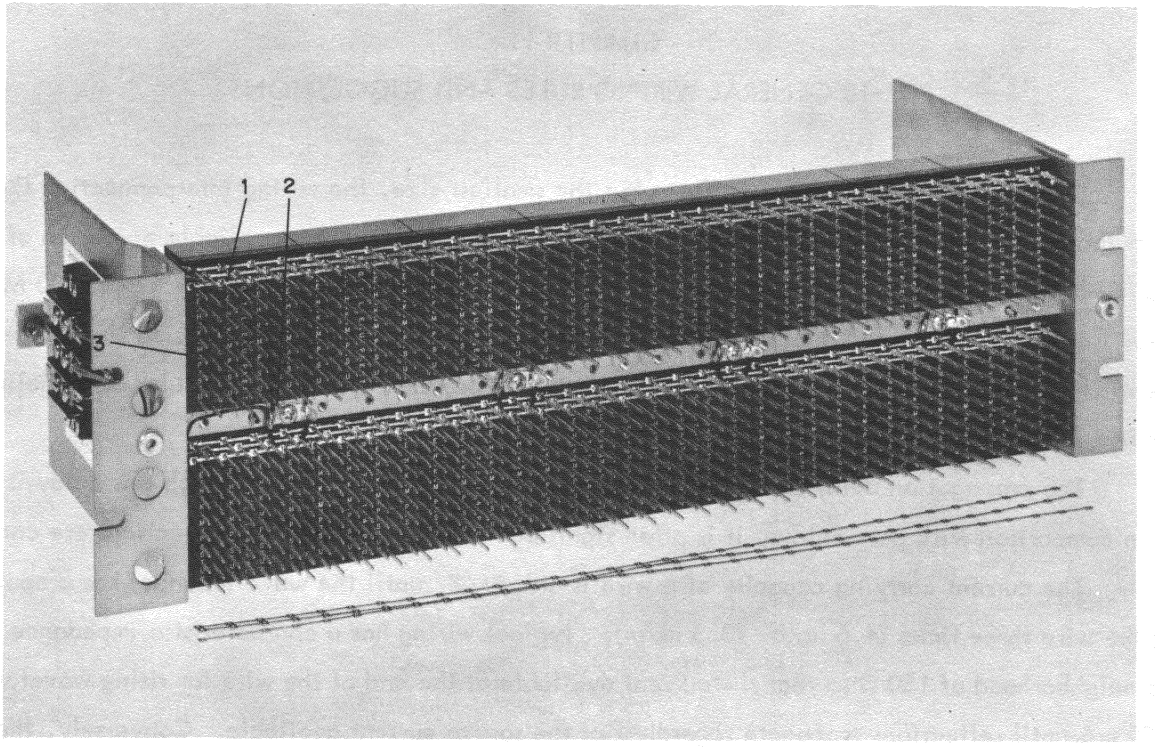


Figure 11-1 Ground Mesh

Signal Wiring Rules

The following signal wiring rules are to be taken as guidelines for the construction of reliable logic assemblies. They are engineering guidelines rather than hard and fast rules. Experience has shown that under some conditions limits may be exceeded somewhat and under other conditions the guidelines presented are not sufficiently restrictive to prevent trouble. The best test of adequate wiring design is the ability of the signal waveforms to meet the requirements of the following waveform requirements. The rules and waveform requirements do not apply to the I/O, memory, multiplexer, or channel busses which have their own rules. However, some details of interest for these busses are included.

These rules DO NOT APPLY to B-series transistor inverters such as the B104, B105, B123 or B124; to transistor inverter flip-flops such as the B200, B201 or B204; or to the input circuits of the B301, B310, B360 or B620. The use of these module types requires very careful design and considerable experience; thus the use of these modules is not recommended. Note that the R- and S-series pulses are to be treated as "levels", as the R- and S-series pulse amplifier output circuit is quite similar to an ordinary logic gate output circuit.

Level Wiring

The following rules on level wiring apply to B-Series levels and R- and S-series levels and pulses.

Levels entirely in one cabinet (not going through a cable): If less than 20 in. total run length and less than 4 loads, do not need to terminate; if less than 50 in. total run length and less than 4 loads and the level is ANDed with a pulse at the end of a run, do not need to terminate but should check that the pulse samples the level after ringing has settled down; short length run but more than 4 loads, terminate if waveform does not meet waveform requirements below; all other cases terminate level with a level terminator circuit.

Interbay Levels (levels which run through a cable): Use G796-G796 cable between bays (that is, for all level cables); if source to cable run is less than 20 in., do not need to terminate; if cable to load run is less than 20 in. and there are less than 4 loads, do not need to terminate; if cable to load run is less than 50 in. and there are less than 4 loads and the level is ANDed with a pulse at the end of the run, do not need to terminate; otherwise terminate with a level terminator circuit.

The standard level terminator is the G704 2 mA terminator circuit. It consists of a 2 mA clamped load which does not allow signal excursions below approximately -3.5 V and a clamp diode which does not allow signal excursions above approximately ground. The single inputs of the B163 (pin D, E, K, L, R, S) contain similar circuits which may be used in lieu of G704 terminators if convenient. The G796-G796 cable assembly contains a standard 2 mA terminator circuit at each end. The R-series DCD gate contains a diode clamp which prevents input excursions above ground on both the level and pulse inputs. The DCD gate clamping feature is also an adequate terminator in most cases. R001 and R002 diodes are usable as ground clamp terminators with the cathode tied to ground and the anode tied to the level run if no other terminator is available. A diode to ground should only be used if no other solution is practical. Additional clamped loads may have to be added to a long level line to maintain adequate fall time. For a terminator to be of any value it must be not more than 10 in. beyond the last load in the run.

Pulse Wiring (35 ns and 40 ns pulses): The following rules apply to B-series 35 ns and 40 ns pulses produced by pulse-transformer-output pulse amplifiers. They should also be applied to any other pulse-transformer-source signal source unless otherwise specified by the particular module data sheet. The pulse rules are divided into two parts: a set for areas of high pulse wiring density such as control circuits or timing chains and a set for areas of low pulse wiring density with good decoupling from level lines such as register loading pulses.

Control Area Pulses (high pulse wiring density): If less than 6 in. total run length, use single wire; if 6 to 20 in. total run length and less than 6 loads total, use single wire; all other cases use twisted pair; in any case, terminate the end of the run in a 100 Ω pulse terminator such as available on the G700.

Register Loading Pulses (low pulse wiring density): If distance from source to single load or to cable is less than 8 in., use single wire; if cable is used, cable length must not exceed 20 in., maximum vertical distance between cable connectors is 10.5 in., use G794-G794 or G799-G799 cables; if distance between load pins or between cable and load pin is less than 6 in., use single wire; if longer than 6 in. use twisted pair; all loads on a run must be located within an area 22 modules wide and 2 modules high; in any case, the end of the run must be terminated in a 100 Ω terminator as available in the G700.

Waveform Requirements

The following waveform requirements should be met by all levels and pulses.

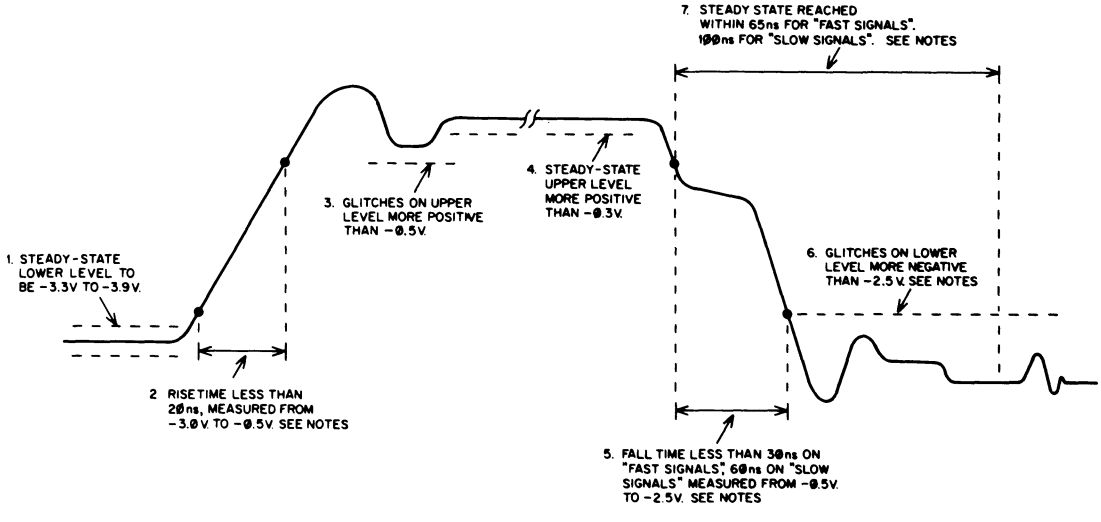
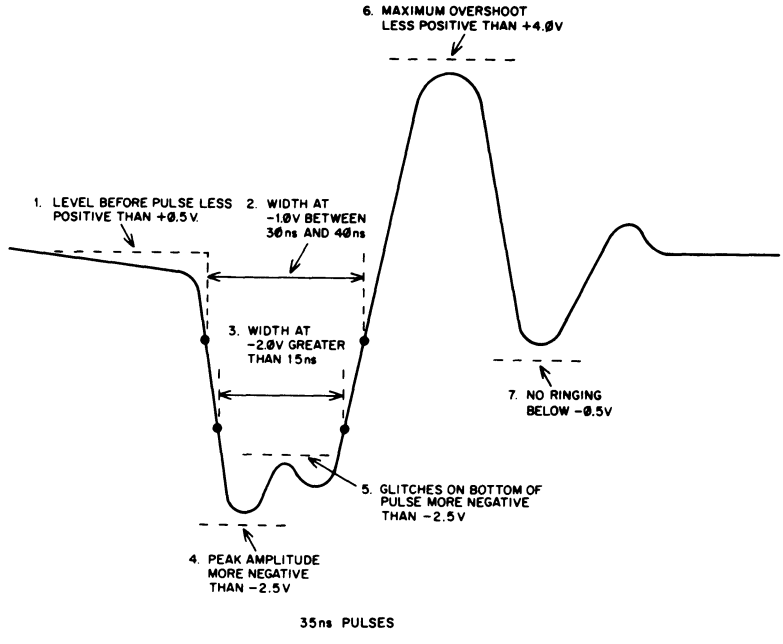


Figure 11-2 Waveform Requirements

If 2. is not met, the source is overloaded.
If 3. is not met, the level is inadequately terminated.
If 4. is not met, the source is overloaded.
If 5, 6, 7. is not met, more clamped loads are needed.



If 1. is not met, recovery time is not long enough.
If 2, 3, 4. is not met, load is too heavy or wire is too long.
If 5, 6, 7. is not met, termination resistors should be added along line.

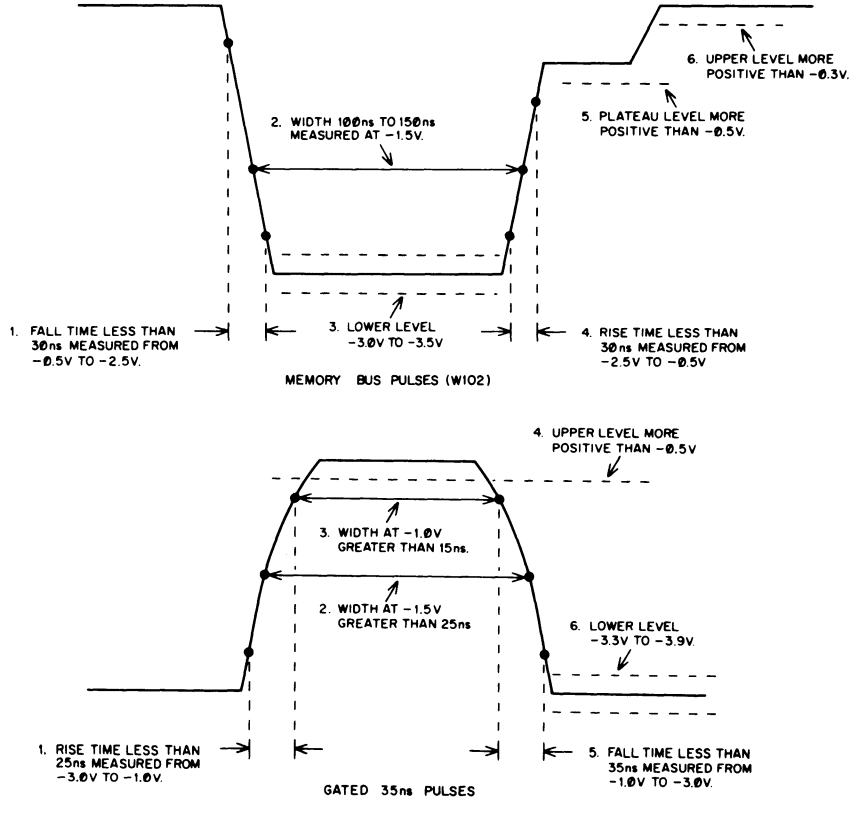


Figure 11-3 Pulses

NOTES: In general, R- and S-series modules will not meet the rise time or fall time specifications but should consistently meet reduced specifications of rise time 60 ns maximum, fall time 150 ns maximum. Due to wiring inductance, significant glitches may occur on output fall, particularly on heavily loaded lines. In many cases, these can be tolerated by providing adequate time before the level is used. Otherwise, additional clamped loads should be distributed along the line to make the entire run fall more uniformly. Certain types of gates (such as the R131 XOR gate) may glitch due to internal logic design; these cases are noted on the module description sheets and must be tolerated. The "cleanness" of fall necessary for proper operation is dependent upon what a level is being used for. A level which is sampled with a pulse need only be stable and settled during the pulse. A level which is used in a synchronizing circuit or to trigger a pulse amplifier must have an essentially smooth fall to -2.5 V.

APPENDIX A
LEVEL TERMINATOR OPERATION

It is initially amazing to most people that two-diode clamping circuits are adequate to terminate a transmission line such that little if any reflection occurs. This phenomenon is explained below.

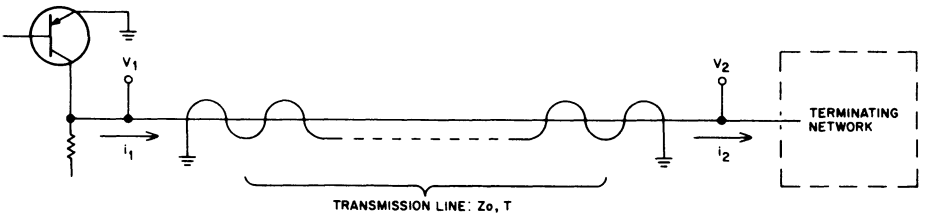


Figure A-1 Level Transmission Line

Consider the simplified example shown in Figure A-1. The transmission shown is a twisted pair, but any long signal line in a relatively uniform wiring network will act as a transmission line. Transmission lines will propagate independent forward (left-to-right) and backward (right-to-left) waves. These are described by the following incremental equations:

$$V_f(t,x) = V_{f0}\,(t - x/c)$$

forward wave

$$I_f(t,x) = \frac{Vf0\,(t - x/c)}{Z_0}$$

$$V_r(t,x) = V_{r0}\,(t + x/c)$$

backward wave

$$I_r(t,x) = -\frac{V_{f0}\,(t + x/c)}{Z_0}$$

Where Z_0 is the charactistic impedance of the transmission line and c is the velocity of propagation along the transmission line. (The line is assumed lossless and dispersionless.) The current in the line at any point is $I_f + I_r$ and the voltage at any point is $V_f + V_r$ where in both cases "dc" voltages and currents are ignored.

Consider the case where the transistor at the left end of the transmission line generates the voltage waveform shown in Figure A-2.

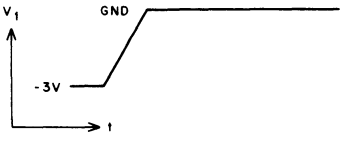


Figure A-2 Driving Waveform

At a time T later, this waveform traveling as a forward wave will reach the terminal end of the line and will interact with the terminating network possibly causing a reflected backward wave. The following equations must be satisfied at the terminal node:

$$V_f = I_f Z_0$$

$$V_r = - I_r Z_0$$

$$V_2 = I_2 Z \text{ term}$$

$$I_2 = I_f + I_r$$

$$V_2 = V_f + V_r$$

where Z Term is the (incremental) impedance of the terminating network (as a function of V_2 and I_2).

If Z Term is an open circuit (the signal is unterminated), then $I_2 = 0$ so $I_r = - I_f$ and $V_r = V_f$ (the signal is completely reflected). The voltage in the middle of the line will have a 100% overshoot (Figure A-3 (a)).

If Z Term = Z_0, then $I_2 = I_f$, $V_2 = V_f$ and I_r and $V_r = 0$ (there is no reflection). There will be no overshoot (Figure A-3 (b)). Unfortunately most logic circuits are unable to drive a load of Z_0 (typically 100 to 150 Ω).

If the terminating network is a short circuit, then $V_2 = 0$, so $V_r = -V_f$, $I_r = I_f$, and $I_2 = ZI_f$ (the signal is completely reflected and inverted). The voltage in the middle of the line will have a 100% undershoot.

If the terminating network is an ideal clamp diode connected to ground, the incremental reflected wave will be identical to the open circuit case until V_2 reaches ground. Then it will be identical to the incremental wave found in the short circuit case (Figure A-3 (d)). In this case the overshoot is only 50% and lasts only the duration of the risetime of the forward wave.

If the terminating network is a real diode connected to -0.7 V (to compensate for the forward voltage drop of the diode), the incremental terminating impedance will vary from an open circuit to a low impedance in a continuous fashion. The terminating impedance will be approximately equal to Z_0 over a significant part of the risetime. The overshoot in the middle of the line is now somewhat less than 50% but has a non-zero tail (Figure A-3 (e)).

The actual level terminating network has a positive going clamp at ground as discussed above and also a negative going clamp at -3.5 V. These clamp diodes in conjunction with the miscellaneous dissipative losses in the transmission line and the source provide signals throughout the length of the line which do not have excessive overshoot, undershoot, or ringing. A fairly typical waveform is pictured in Chapter 11, Figure 11-3.

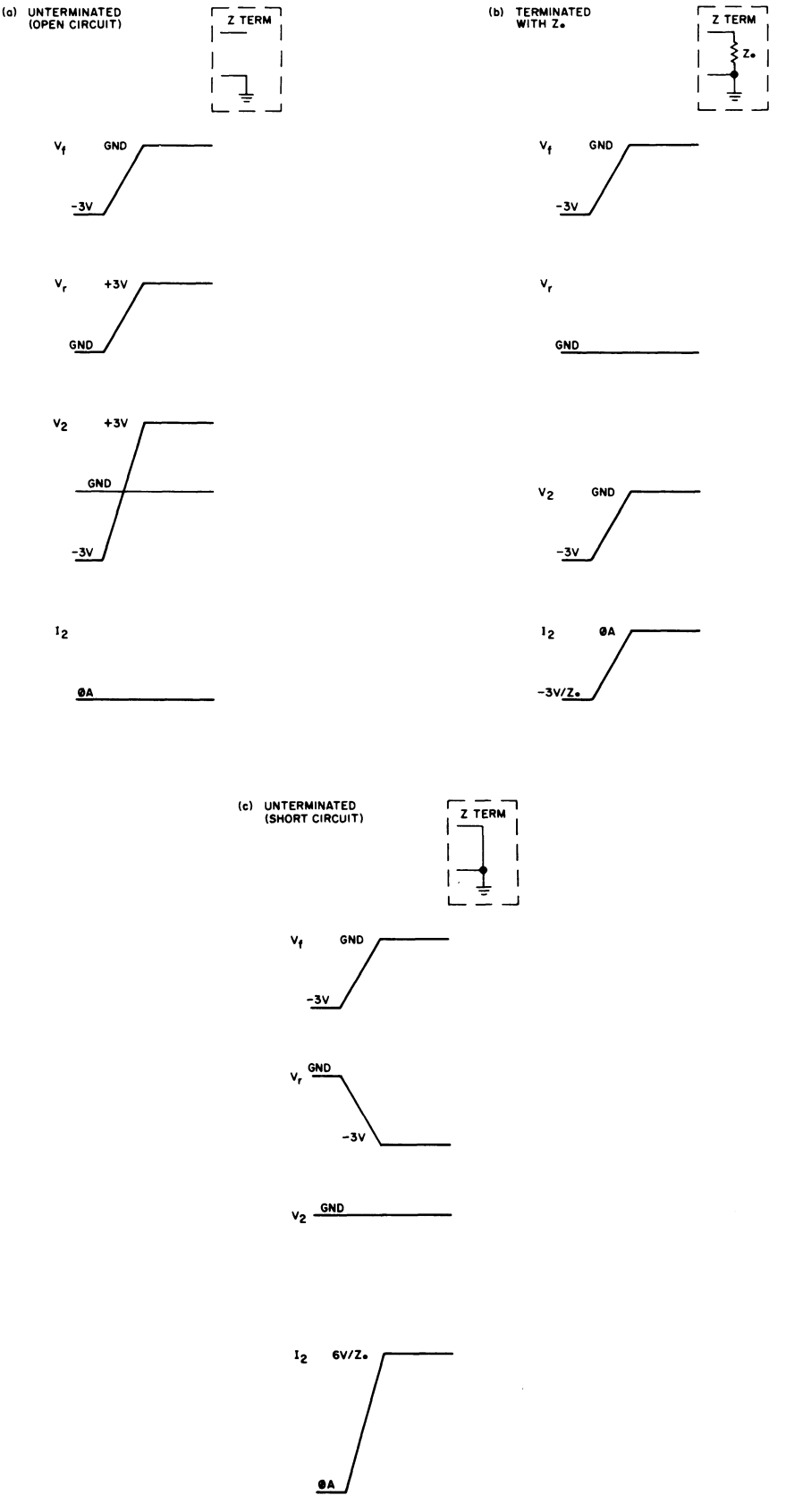


Figure A-3 Waveforms During Reflection

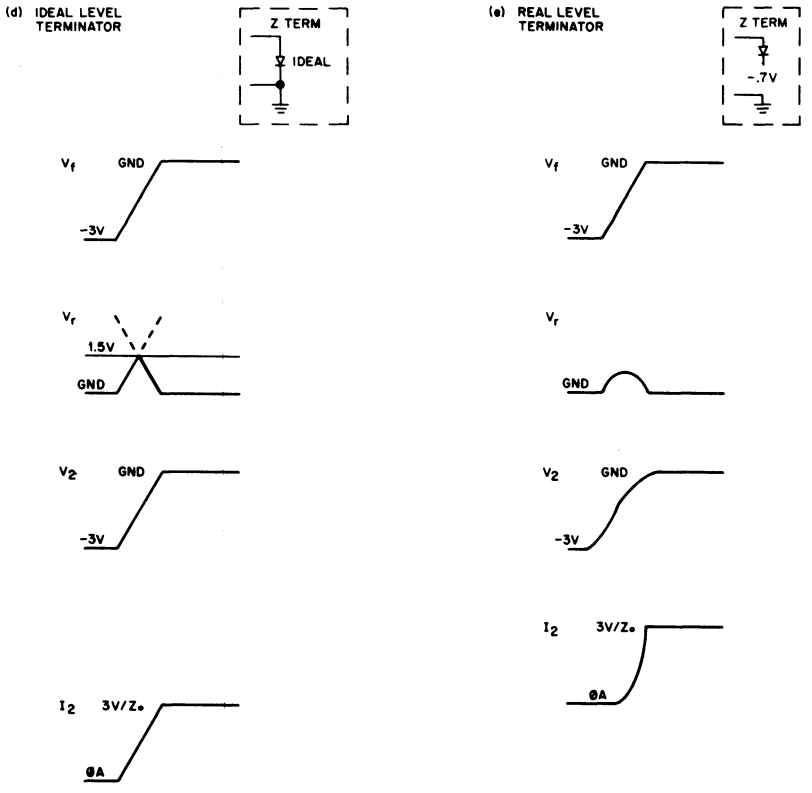


Figure A-3 Waveforms During Reflection (Cont)

APPENDIX B

MODULE AND COMPONENT PRICE LIST

Prices are subject to change without notice

B130	Three Bit Parity Circuit	$50.00
B133	Four two-input NAND	23.30
B134	Four two-input NOR	31.00
B135	Three three-input NAND	17.00
B137	Two six-input NAND	13.00
B141	Seven two-input NAND mixer	24.50
B152	Binary-to-Octal Decoder	34.00
B156	Half Binary-to-Octal Decoder	25.00
B163	Six two-input NAND	31.00
B165	Five Inverters	21.20
B166	Counting Gate	31.00
B167	Triple Two two-input NAND mixer with two Inverters	34.00
B168	Triple Three two-input NAND mixer	31.00
B169	Dual Four two-input NAND mixer	25.00
B172	Twelve-input NAND with Inverter	18.00
B211	Jam Flip-Flop with input mixer	43.00
B212	Two Set-Clear Flip-Flops with delay	42.00
B214	Four Flip-Flops	31.00
B311	Tapped Delay with two-input NAND	64.00
B312	Adjustable Delay with two-input NAND	65.00
B611	Two Pulse Amplifiers and two two-input NAND	42.00
B683	Three NAND Negative Bus Drivers	50.00
B684	Two Bus Drivers	52.00
B685	Two NAND Gate Drivers	27.00
G700	Nine 100 Ohm Terminators	8.00
G703	Dual Nine 100 Ohm Cable Terminator	9.50
G704	Fourteen 2 mA Level Terminators	30.20
H003	Single Width Connector Retaining Kit	5.20
H004	Double Width Connector Retaining Kit	11.00

MODULE AND COMPONENT PRICE LIST

H351	Level Terminated Bus Connector Kit	$75.00
H352	Unterminated Bus Connector Kit	30.00
R613	Three Pulse Amplifiers	42.00
W010	Fifteen 10 mA Clamped Loads	23.00
W102	Four Pulsed Bus Transceivers	58.50
W107	Seven Bus Receivers	36.00
BC10A-5	Single Bus Cable 5 feet	250.00
BC10A-7	Single Bus Cable 7 feet	270.00
BC10A-10	Single Bus Cable 10 feet	280.00
BC10A-15	Single Bus Cable 15 feet	310.00
BC10A-25	Single Bus Cable 25 feet	370.00
BC10A-35	Single Bus Cable 35 feet	430.00
BC10B	Margin Check Cable standard lengths	20.00
BS10A-5	Complete Bus Cable Set 5 feet	450.00
BS10A-7	Complete Bus Cable Set 7 feet	470.00
BS10A-10	Complete Bus Cable Set 10 feet	500.00
BS10A-15	Complete Bus Cable Set 15 feet	530.00
BS10A-25	Complete Bus Cable Set 25 feet	600.00
BS10A-35	Complete Bus Cable Set 35 feet	690.00
7005459	W012-W250 Indicator Cable Assembly	40.00
7005463	G799-G799 30 Ohm Pulse Cable Assembly	55.00
7005469	G796-G796 Level Terminated Cable Assembly	75.00
844	Power Control	365.40

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