KW11-L
line time clock
manual

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CHAPTER 1
INTRODUCTION

The KW11-L Line Time Clock is an option that provides the PDP-11 System with a method of accurately dividing time into intervals. The KW11-L consists of a single-height M787 Line Time Clock Module that generates a repetitive interrupt request to the processor. The rate of interrupt is the same as the line frequency, either 50 or 60 Hz.

This manual describes the manner in which the KW11-L functions and presents general and detailed descriptions of the KW11-L. It is assumed that the reader is familiar with basic digital theory.

Line time clock signals pass through the Unibus ⓉⓂ; it is beyond the scope of this manual to describe the operation of the Unibus. A detailed description of the Unibus is available in the *PDP-11 Unibus Interface Manual,* DEC-11-HIAB-D.

Installation of the KW11-L is accomplished by plugging the M787 Module into slot B12 of the KA11 or KC11 and removing the jumper wire from B12V2 to B12R2.

ⓉⓂ Unibus is a trademark of Digital Equipment Corporation.

CHAPTER 2
GENERAL DESCRIPTION

The KW11-L accurately divides time into intervals for more efficient use of PDP-11 computer time. The intervals are determined by the line frequency, either 50 or 60 Hz. The accuracy of the clock period is that of the frequency source.

The KW11-L includes an address selector, threshold detector, interrupt control, and a two-bit status register (see Figure 2-1). The address selector is permanently wired to respond to a single incoming address, 777546. Before the KW11-L begins to operate, the processor must send out that address, a master synchronization (MSYN) signal, and a gating control signal. MSYN indicates to the device that address and control information are present. The gating control signal determines the direction of the data transfer operation desired: DATI for transfer of data from slave to master, DATO for transfer from master to slave.

A valid combination of these three sets of signals controls data transfers between the two-bit status register of the KW11-L and the processor. These transfers determine whether the device is in the interrupt or the noninterrupt mode. In the interrupt mode, the KW11-L signals the processor for an interrupt each time it receives a pulse from the line frequency source. In the noninterrupt mode, the KW11-L acts as a program switch that the processor can examine or ignore.

When the KW11-L is in the interrupt mode, the interrupt control section of the device provides the circuits and logic required to make bus requests, gain bus control, and generate interrupts. When the threshold detector provides a pulse from the line frequency source, the interrupt control section initiates a bus request on priority level 6, which is the priority level of the KW11-L.

The priority arbitration logic in the processor recognizes the request and issues a bus grant signal, if this device is the highest priority device requesting an interrupt. The KW11-L responds with a selection acknowledge (SACK) signal. When the requirements for becoming bus master have been fulfilled, the KW11-L asserts bus busy (BBSY), an interrupt (INTR) signal, and an interrupt vector address of 100. The processor generates a slave synchronization (SSYN) signal, then responds to the interrupt with an interrupt service routine. The interrupt control section of the KW11-L then goes to a rest state until the next initialization.
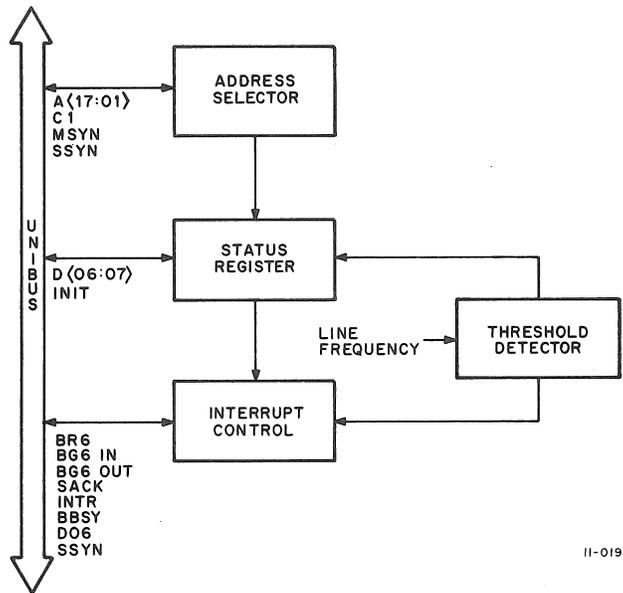
Figure 2-1   KW11-L Block Diagram

The two-bit status register of the KW11-L consists of bits 6 and 7 on the data bus line. When bit 6 is set, the device is in the interrupt mode; when it is clear, the device is in the noninterrupt mode. Bit 6 is set or cleared by a processor DATO to the KW11-L; it is also cleared by a processor INIT. Bit 7 is set by a line clock pulse from the threshold detector or by a processor INIT; it is cleared by any processor DATO to the KW11-L.

Bit 7 can be used by the processor to determine which device caused an interrupt. The interrupt service routine should include a DATI which reads the interrupt monitor bit (bit 7) to serve as a partial check on the origin of the interrupt vector. Thus, if bit 7 is clear, there is an indication to the processor that this device did not request the interrupt.

In the noninterrupt mode, the KW11-L performs a more passive function. The KW11-L acts as a program switch that the processor can examine or ignore. The interrupt control section is disabled so that the KW11-L cannot assert a bus request (BR6) and, therefore, cannot go into an interrupt sequence. A programmed DATO must be used to return the KW11-L to the interrupt mode; programmed DATIs must be used to examine the status of the device. In the noninterrupt mode, the KW11-L is controlled by programmed instruction from the processor.

A more detailed description of KW11-L operation is presented in Chapter 3. Chapter 4 contains programming information for both the interrupt and the noninterrupt modes.

KW11-L specifications are as follows:

Register	Two-bit status register; bits 6 and 7 on the data bus line
Address	Permanently wired to 777546
Vector Address	Permanently wired to 100_8
Function	Generates repetitive time interval indications to processor
Bit 6	Interrupt enable bit
Bit 7	Interrupt monitor bit
Rate	Same as line frequency; 50 or 60 Hz
Bus Cycles	DATO, DATI
Priority Level	Permanently wired to BR6
Modes	Interrupt and noninterrupt

CHAPTER 3
DETAILED DESCRIPTION

The KW11-L includes an address selector, threshold detector, interrupt control, and a two-bit status register. Each section is discussed with regard to its operation and interrelationship to the other sections of the device.

3.1 ADDRESS SELECTOR

The address selector section of the KW11-L is permanently wired to respond to incoming address 777546. Input signals enter on 17 address lines, A(17:01), one bus control line, C1, and a master synchronization (MSYN) line (see drawing D-BS-KW11-L-01). Address line A00 is not brought into the device because its only function is to select between bytes; the KW11-L deals only with complete words. The address format used to select the KW11-L is shown in Figure 3-1 and is decoded by the address selector. This decoded address, together with a 1 on MSYN, causes the output of gate E3 to go high (drawing D-BS-KW11-L-01), signalling that the device has been addressed.

3.2 THRESHOLD DETECTOR

The threshold detector section (Q2 and E11 on drawing D-BS-KW11-L-01) of the KW11-L detects a point on a waveform (LTC L) produced by the H720 Power Supply. A regulator circuit board in that power supply includes a circuit that provides a clipped waveform based on the input-line voltage.

Signal LTC L is inverted to cause a high pulse at the clock input of the flip-flop for bit 7 of the status register, setting that bit and, if bit 6 is set, the internal interrupt request flip-flop (E6).
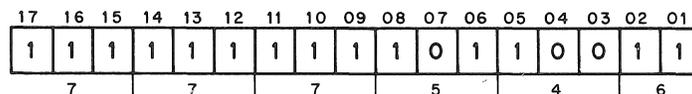
Figure 3-1   KW11-L Address Word

3.3 INTERRUPT CONTROL

The interrupt control section of the KW11-L provides the logic circuits to make bus requests, gain bus control, and generate interrupts. This section of the device uses three flip-flops: the interrupt request, FF1 and FF2 (see Figure 3-2). Table 3-1 lists the settings of these flip-flops in relation to the bus states and the signals asserted.
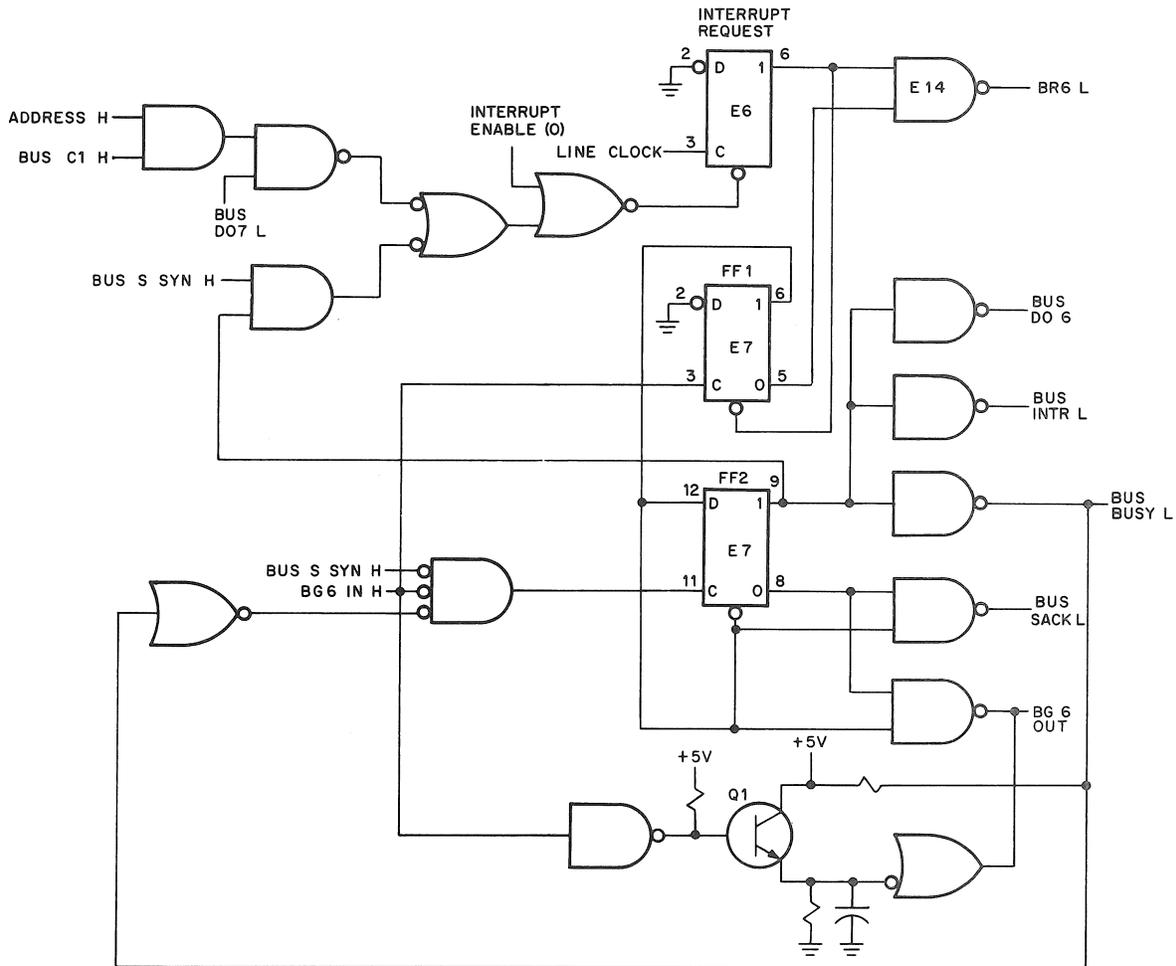

Figure 3-2 Interrupt Request Section, Simplified Logic Diagram

When the KW11-L is not requesting, all three flip-flops are in the 0 state, and no signals are asserted on the bus. The requesting state is entered when the interrupt request flip-flop is set by a line clock pulse. This setting of the flip-flop can occur only when the status bit 6 flip-flop (interrupt enable) is in the 1 state. Setting the interrupt request flip-flop generates a bus request priority level 6 (BR6).

The priority arbitration logic of the processor determines whether priority level 6 is the highest level requesting. If priority level 6 is the highest level requesting, the processor asserts a bus grant signal (BG6 IN high) that sets the FF1 flip-flop. Signal BG6 is blocked from being passed on to the next device and the assertion of the bus request (BR6) is dropped. With flip-flop FF1 a 1 and flip-flop FF2 a 0, the selection acknowledge signal (SACK) is asserted on the bus.

Table 3-1
Interrupt Control Flip-Flops

Interrupt Request	FF1	FF2	State	Signals
0	0	0	Not Requesting	None
1	0	0	Requesting	BR6
1	1	0	Granted	SACK, inhibit BG6 OUT
1	1	1	Master	BBSYN, INTR, D06 (Vector address)

On receiving the SACK signal, the processor drops BG6 IN, and flip-flop FF2 is set if SSYN and BBSY are unasserted. Signals BBSY and INTR are then asserted on the bus, as well as interrupt vector address 100 (D06).

The processor responds to these signals by asserting a slave synchronization signal (SSYN) that clears the interrupt request flip-flop. Flip-flops FF1 and FF2 are subsequently cleared; the interrupt control section of the KW11-L is returned to the not requesting state. At the same time the SSYN is asserted, the processor goes into the interrupt service routine at vector address 100.

3.4 STATUS REGISTER

The status register of the KW11-L contains the interrupt enable (D06) and the interrupt monitor (D07) flip-flops (see Figure 3-3). Operation of the status register circuits is controlled by INIT, the line clock pulse, DATO, and DATI.

Signal INIT is generated either by depressing the START switch on the console or by issuing a programmed RESET instruction. This signal clears D06 and sets D07 to initialize the status register for a new operation.

The line clock pulse is supplied by the threshold detector section of the KW11-L and is used to set D07. DATO and ADDRESS clear D07 when BUS D07 is 0, by applying a signal to the direct clear input.

For DATO and DATI to affect the circuits of the status register section, the address of the KW11-L and MSYN must be asserted on the bus to provide the ADDRESS H signal shown as an input on Figure 3-3. This ADDRESS signal is also used, after a delay, to assert a SSYN signal on the bus.

The combination of DATO and ADDRESS provide a signal to the clock input of D06. Depending on BUS D06, the flip-flop is either set or cleared. Thus, the processor can read a bit into this flip-flop by issuing a DATO and D06 = 1 for a 1, and DATO and D06 = 0 for a 0. The 0 side output of D06 controls the interrupt function of the KW11-L by holding the interrupt request flip-flop (in the interrupt control section of the KW11-L) in the cleared state when D06 is in the 0 state.

DATI and ADDRESS provide gating that reads the content of D06 onto bus line D06 and the content of D07 onto bus line D07.
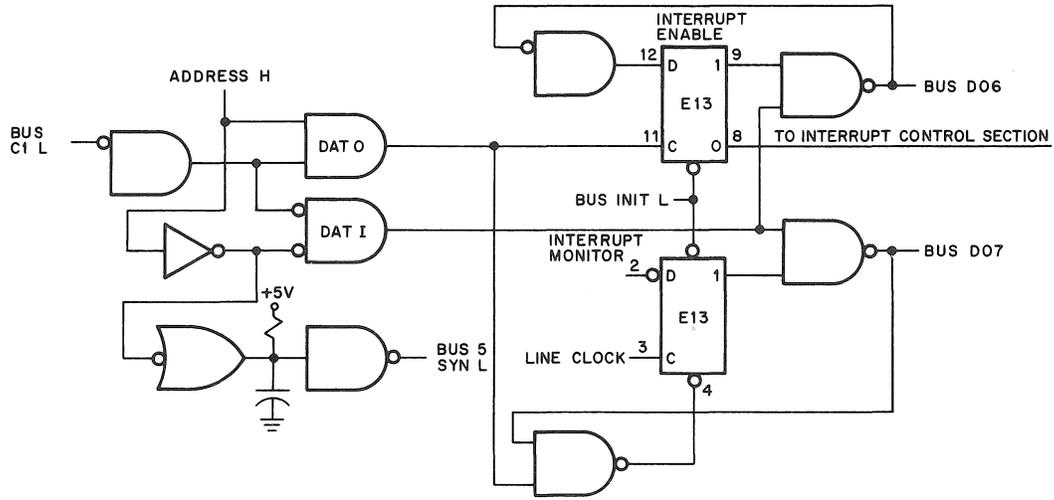
Figure 3-3   Status Register, Simplified Logic Diagram

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CHAPTER 4
PROGRAMMING INFORMATION

This chapter presents general programming information for software control of the KW11-L Line Time Clock. Although typical program examples for both the interrupt and noninterrupt modes of operation are included, it is beyond the scope of this manual to provide detailed programs. If more detailed programming information is desired, refer to the *PDP-11 Paper Tape Software Programming Handbook,* DEC-11-GGPA-D.

All software control of the KW11-L is performed by means of a two-bit status register, which has been assigned memory address 777546 and the mnemonic LKS. This register can be read or loaded by using any PDP-11 instruction that refers to its address.

4.1 INTERRUPT MODE

The following program is an example of one way the KW11-L can be used in the interrupt mode. The purpose of this program is to enter the routine TIME after every N interrupts. The mnemonic LKS represents the permanent memory address of the KW11-L, 777546; LKV represents the vector address, 100. When the main program is interrupted, it is directed to LKV, and then to LKV + 2, which is 102. The word in location 100 is the address of the first instruction in the interrupt service routine; this address is transferred into the program counter of the processor. The word in location 102 is the new status word, which is transferred into the status register of the processor. The new status word contains the number 300, which indicates a priority level of 6, with all five condition codes, T, Z, N, V, and C equal to 0.

```
          LKS  = 777546
          LKV = 100
MAIN:         MOV #N, CNTR
              MOV #100, LKS          ;ENB INTR
              .
              .
              .
LKV:          LKSERV
              300
LKSERV:       MOV #100, LKS          ;Clear bit 7.  This instruction is optional
              DEC CNTR
              BEQ TIME               ;If counter is zero, go to time.
                                     ;If counter is not
                                     ;zero, continue.
              RTI
TIME:         MOV #N, CNTR           ;Reset counter
              .
              .
              .
              RTI
```

4.2 NONINTERRUPT MODE

The following program is an example of one way the KW11-L can be used in the noninterrupt mode. In this example, it is assumed that an INIT or a previous DATO with D06 = 0 has placed the KW11-L in the noninterrupt mode. This program alternates between two program routines; each routine lasts for approximately the time period between line clock changes, which is either 16.67 ms or 20 ms. Each routine contains a program loop that lasts for a considerably shorter time than the period between line clock changes. The mnemonic LKS represents the permanent memory address of the KW11-L, 777546.

```
         LKS = 777546
START:      CLRB   LKS        ;Reset bit 7
SYNC:       TSTB   LKS        ;Wait until bit 7 is set,
            BPL    SYNC       ;Then reset it
            CLRB   LKS        ;Clear bit
ON:                .          ;Do first routine
                   .
                   .
            TSTB   LKS        ;Each time through loop test bit 7
            BPL    ON         ;When bit is set
            CLRB   LKS        ;Clear bit
OFF:               .          ;Do second routine
                   .
                   .
            TSTB   LKS        ;Test bit 7
            BPL    OFF        ;If not set, do loop again
            CLRB   LKS        ;If set, clear bit
            JMP    ON         ;Do first program again
```

CHAPTER 5
KW11-L ENGINEERING DRAWINGS

The engineering drawings for the KW11-L are contained in the print set that is shipped with the equipment. The drawings that relate to this manual are:

D-TD-KW11-L-02   Timing Diagram (KW11-L)
D-BS-KW11-L-01   Line Frequency Interval Clock

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