EY-DX056-SP-002/J6269-A/EY-DX052-SG-002

Small Systems Training PDP-11V23-/11T23 System Maintenance

Student Guide

digital

PDP-11V23/11T23 SYSTEM MAINTENANCE
EY-DX056-SP-002
J6269-A

STUDENT GUIDE
EY-DX052-SG-002

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PDP-11V23/11T23 SYSTEM MAINTENANCE

COURSE GUIDE

Course Guide

COURSE DESCRIPTION

The PDP-11V23/11T23 System Maintenance Course is a self-paced, lab-oriented course. It is designed to teach field service engineers the skills required to maintain the 11V23 and 11T23 systems in accordance with the prescribed maintenance philosophy. These skills include:

- Installation
- Loading and running diagnostics
- Interpreting diagnostic messages
- Configuring jumpers and switches
- Theory of operation
- Fault isolation

PREREQUISITES

The prerequisites for the PDP-11V23/11T23 System Maintenance Course are:

- RL01 Disk Drive SPI course

- RX02 Floppy Disk SPI course

- VT100 Video Terminal SPI course

- Introduction to PDP-11 Audio/Visual course

COURSE GOALS

After you complete this course you will be able to:

- Understand the physical relationships between all system elements.
- Identify the names and physical locations of switches, indicators, controls, and Field Replaceable Units (FRU).
- Operate the applicable device or system.
- Configure the switches and jumpers for particular applications or configurations.
- Using available maintenance and diagnostic aids, troubleshoot system malfunctions.
- Install an 11V23/11T23 system.

MAINTENANCE PHILOSOPHY

The PDP-11V23/11T23 will be maintained on-site by the field service engineer. Maintenance consists of removal and replacement of FRUs to the module or subassembly level. The microprocessor chip set is considered an FRU.

FRUs, when found to be defective, are replaced using maintenance and diagnostic aids. These aids consist of three groups of diagnostics and a PDP-11V23 Troubleshooting Guide.

The most basic diagnostic tool is the hardware on-line debugging technique (ODT). This is built into the computer processor and consists of a group of commands and routines for locating error conditions and for communicating with the computer in simple commands and responses. Use of ODT will be covered in the KDF11-AA Processor course module.

The next group of diagnostic programs is built into the computer hardware and is located on the BDV11 circuit card (M8Ø12-YA module) in the form of three small programs. One of these programs automatically checks non-memory-modifying processor instructions during the power-on sequence. The remaining two programs check memory-modifying processor instructions and system memory. Use of these diagnostics will be covered in the BDV11 Boot/Terminator course module.

The RYDP or RLDP diagnostic software system consists of a collection of diagnostic programs plus monitor and utility programs stored on floppy disks or disk pack. The RYDP and RLDP programs are designed to diagnose individual system components. The use of these individual diagnostics will be discussed in the various course modules training.

The PDP-11V23 Troubleshooting Guide is designed to detect problems that prevent the loading and execution of diagnostics. Use of this manual will be covered in the 11V23/11T23 System Laboratory course module.

COURSE OUTLINE

1 11V23/11T23 Introduction

A. PDP-11V23 System Overview
B. PDP-11T23 System Overview
C. PDP-11V23/11T23 Options

2 LSI-11/23 Bus Concepts

A. Bus Identification
B. Bus Basics
C. Bus Cycles
D. Data Transfers and Priority
E. Special Bus Functions

3 BA11-N Mounting Box

A. Overview
B. Physical/Functional Description
C. Configuring
D. Disassembly
E. Adjustments

4 KDF11-AA Processor

A. Overview
B. Physical/Functional Description
C. Theory of Operation
D. Configuring
E. Installation
F. Operation

5 MSV11-DD 32K Dynamic MOS Memory

A. Overview
B. Physical/Functional Description
C. Theory of Operation
D. Configuring
E. Installation

6 DLV11-J Serial Line Unit

A. Overview
B. Physical/Functional Description
C. Configuring
D. Installation
E. Programming
F. Troubleshooting

7 BDV11-AA Boot/Terminator

A. Overview
B. Physical/Functional Description
C. Programming
D. Configuring
E. Theory of Operation
E. Diagnostic

8 11V23/11T23 System Laboratory

A. Installation
B. Acceptance
C. Fault Isolation

COURSE ORIENTATION

The course material is presented in a series of modules (Figure 1). Related modules are grouped together. You will work through each module by reading and doing exercises with an 11V23 or 11T23 system in the lab. You are encouraged to work at your own speed, either alone or with another student. A Course Administrator will be present at all times to help you with any difficulties or questions.

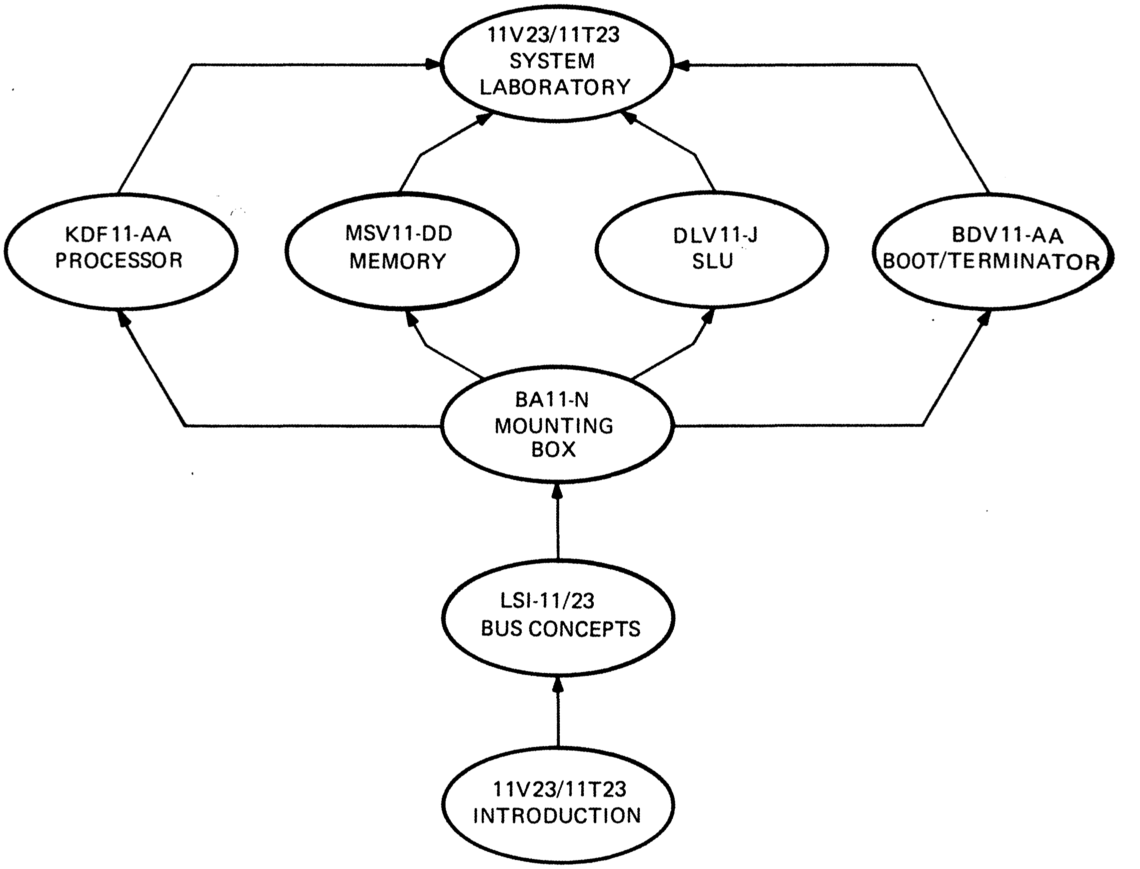


Figure 1. Course Map

Each module has at least one objective that states what you must be able to do to complete that module. To clarify these objectives, sample test items follow them. These show you the exact form in which you will be tested on the module's objectives.

There are at least four resources for each module: (1) the module itself, (2) other students, (3) the Course Administrator, and (4) additional resources. The additional resources may be the main source of information for the module or they may simply be additional suggested readings.

When borrowing an additional resource:

- Fill in the signout card or write your name on the Resource Signout Sheet.
- Cross out your name when you return the resource.
- Borrow only one resource at a time.
- Return all resources upon completion of the course.

Remember that you may request the help of the Course Administrator or another student (provided neither of you is working on a test) at any time.

The module text begins after the list of additional resources. The text presents information, directs you to additional resources, and instructs you to do related exercises. Work through this material at a comfortable speed, talking to your Course Administrator and the other students as necessary.

When you think that you can meet the module objectives, ask for the Module Test. This test covers only the material stated in the objectives and is similar in form to the sample test items.

For written tests:

- Use any reference material.
- There is no time limit.
- There is only one correct response.
- Work alone.

When you complete the test, submit it to the Course Administrator for evaluation (an 8Ø% performance level is considered successful completion). If you have fulfilled the objective, the Course Administrator will sign your Personal Progress Plotter and the Master Progress Plotter. At this point, you may go on to another module. There are no penalties for not answering 8Ø% of the questions correctly. You will simply be asked to review the test and exercise.

For performance/lab exercises:

- There is no time limit.
- Complete all steps.
- Observe safety precautions.
- Work alone.

If you think that you can meet the module objectives without reading its text or doing its performance/lab exercises, you may ask for the Module Test.

PERSONAL PROGRESS PLOTTER

Module Title	Date Achieved	Administrator Signoff
11V23/11T23 Introduction		
LS1-11/23 Bus Concepts		
BA11-N Mounting Box		
KDF11-AA Processor		
MSV11-DD Memory		
DLV11-J SLU		
BDV11-AA Boot/Terminator		
11V23/11T23 System Laboratory		

PDP-11V23/11T23 SYSTEM MAINTENANCE

11V23/11T23 INTRODUCTION

11V23/11T23 Introduction

INTRODUCTION

This module will give you an overview of the PDP-11V23 and PDP-11T23 system. You will learn about the systems' appearances, specifications, and component parts. Details of how these systems operate will be covered in later modules.

OBJECTIVE

Identify the major component locations, specifications, and system capabilities of the PDP-11V23 and PDP-11T23 systems.

SAMPLE TEST ITEM

The PDP-11V23, when used with a VT1ØØ video terminal, draws ________ watts from the ac power line.

a. 86Ø
b. 13ØØ
c. 96Ø
d. 9Ø5

PDP-11V23 SYSTEM OVERVIEW

The PDP-11V23 is a general-purpose microcomputer system used for developing and executing programs for a variety of applications. Optional hardware and software are available for such applications as high-level language program development, foreground/background real-time support, multiprogramming, and the capability to monitor and control equipment. The basic PDP-11V23 does not include a terminal. DIGITAL can provide either a LA120 DECwriter III, a LA34/LA38 DECwriter IV, or a VT100 terminal as optional equipment.

The PDP-11V23 (Figure 1) includes an operator's switch panel, a microcomputer with memory management functions, 64K word (128K byte) MOS memory (expandable to 128K word or 256K byte), a four channel serial line interface, and a dual floppy disk drive. Each disk drive provides 512K bytes of storage using double density format. Communication between user and microcomputer takes place via an optional system terminal (either a DECwriter or DECscope). A special bootstrap ROM terminator module initiates the system software when the system is turned on and can automatically test the system.

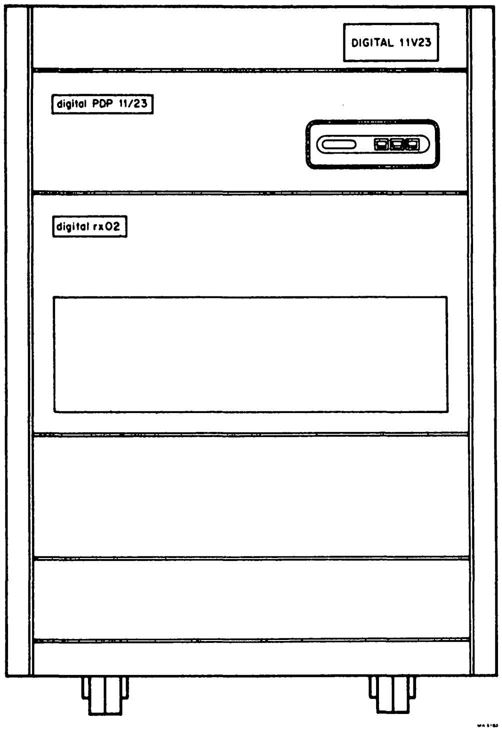


Figure 1. PDP-11V23 System

The cabinet for the 11V23 is divided into several major areas. On the top is the 11/23 microcomputer. It is mounted in a BA11-N mounting box with operator's console. Directly below the microcomputer is the RXØ2 dual floppy disk drive. Unit ZERO is on the left, while unit ONE is on the right. Below the RXØ2 there is usually a blank panel. In some systems this panel is replaced with a BA11-N expansion chassis. Behind the very bottom panel is the power controller. Figure 2 shows a rear view of the 11V23 system.

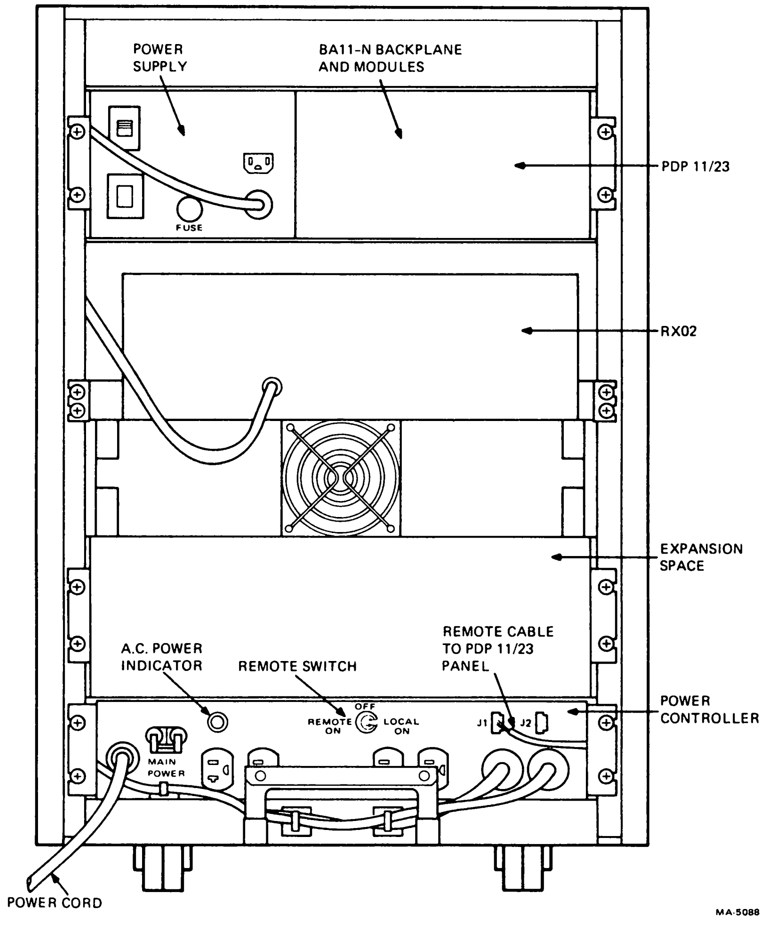


Figure 2. PDP-11V23 (Backpanel Removed)

As you view Figures 1 and 2 you will notice that there are a number of controls on the rear of the system as well as on the front. First, let's consider the front panel controls.

Operator's Console

Figure 3 shows the operator's console on the BA11-N. There are three switches and two indicators on the front panel. Table 1 explains the function of each one of these items.

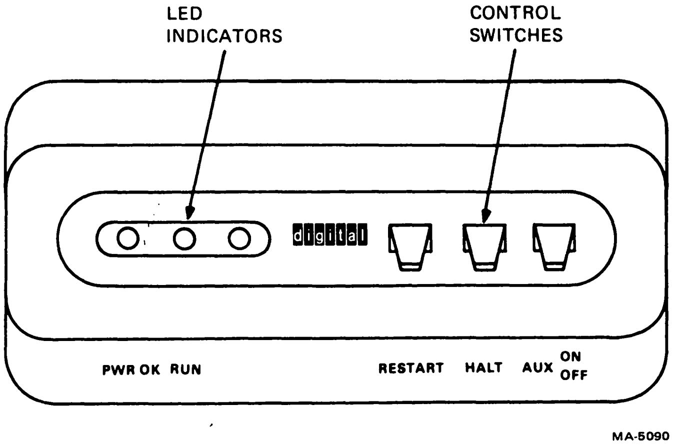


Figure 3. Front Panel Switches and Indicators

Table 1. Control Panel Functions

Switch/LED	Position	Function
AUX ON/OFF	OFF	In the normal factory configuration, the ac power is removed from the system.
	ON	In the normal factory configuration, the ac power is applied to the system. If the HALT switch is up, the system is automatically booted at this time.
HALT	Up (Enable)	The processor is enabled to run.
	Down (Halt)	The processor is halted and will respond to console ODT commands.
RESTART	RESTART (momentary switch)	When the Halt switch is up, the processor carries out a power-up sequence and displays the bootstrap dialogue
PWR OK		Illuminated when the proper dc output voltages are being generated by the microcomputer system.
RUN		Illuminated when the processor is operating and is turned OFF when the processor is not executing instructions.
(UNMARKED LED)		This is a spare indicator which serves no function unless modified by the customer.

Rear Panel Controls

Figure 4 shows a close-up of the rear of the BA11-N mounting box. The circuit breaker on the back of the box also serves as an ON/OFF switch. Primary ac power is supplied through the lower power connector. The upper power connector is usually unused in the 11V23 system. Figure 4 depicts a 115 volt version of the BA11-N.

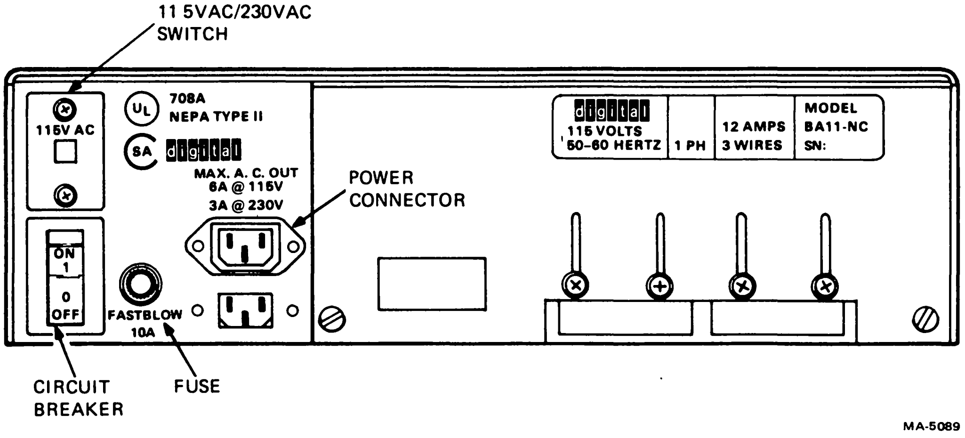


Figure 4. LSI-11/23 Microcomputer (Rear View)

Figure 5 shows the 871 power controller which is mounted at the bottom of the cabinet. The RXØ2 and BA11-N should have their ac power cable plugged into the switched outlet at the far right. The remote cable from the BA11-N should be plugged into J1. Since the ac power is being remotely controlled from the BA11-N, the remote power switch must be in the REMOTE ON position. Any devices, such as a terminal, which you want to power up or down along with the system should be plugged into one of the switched outlets.

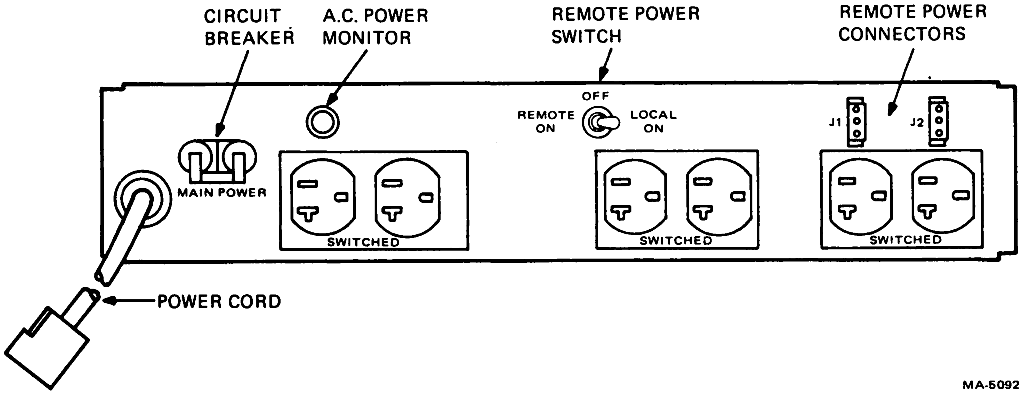


Figure 5. Power Controller (Rear View)

There are three model designations for the 11V23 system. These model numbers depend on power line voltage and frequency. Table 2 summarizes the model designations.

Table 2. PDP-11V23 System Model Designations

PDP-11V23	-AA	-AD	-AC
Input Voltage	115 Vac	230 Vac	115 Vac
Power Controller	871-A	871-B	871-A
Current Rating	12 A	8 A	12 A
Frequency	60 Hz	50 Hz	50 Hz

Inspection of the 11V23's specifications which follow shows that the system does not require a special environment. The system can be installed in any typical office or factory floor.

PDP-11V23 Specification Summary

Environmental Conditions	Specification
Altitude	2440 m (8000 ft) maximum
Operating temperature	15° to 32° C (59° to 90° F) nominal; reduce temperature 1.8° C/1000 m (1° F/1000 ft)
Max. wet bulb temperature	25° C (77° F)
Minimum dew point	2° C (36° F)
Storage temperature	-40° C (-40° F) to 60° C (140° F)
Temperature change rate	11° C (20° F) per hour
Relative humidity	10% to 80% (no condensation)
Maximum shock pulse	10 gravity peak (half-sine) and 10 ± 3 ms duration

Pitch and Roll	±5 maximum
Power Requirements	
PDP-11V23 System	86Ø W
Optional LA12Ø	44Ø W
Optional VT1ØØ	1ØØ W
Optional LA34/LA38	45 W

PDP-11T23 SYSTEM OVERVIEW

The 11T23 system is similar to the 11V23 with the exception of the fact that in place of the RXØ2 floppy disk drive there are two RLØ1 disk drives. Figure 6 shows a typical 11T23 system. From top to bottom, you will find RLØ1 drive Ø, the 11/23 processor, and RLØ1 drive 1. The disk pack is loaded into drive Ø through a hinged door in the top of the cabinet. To load the disk into drive 1 you must first slide out the disk drive and then place the pack into the top of the drive.

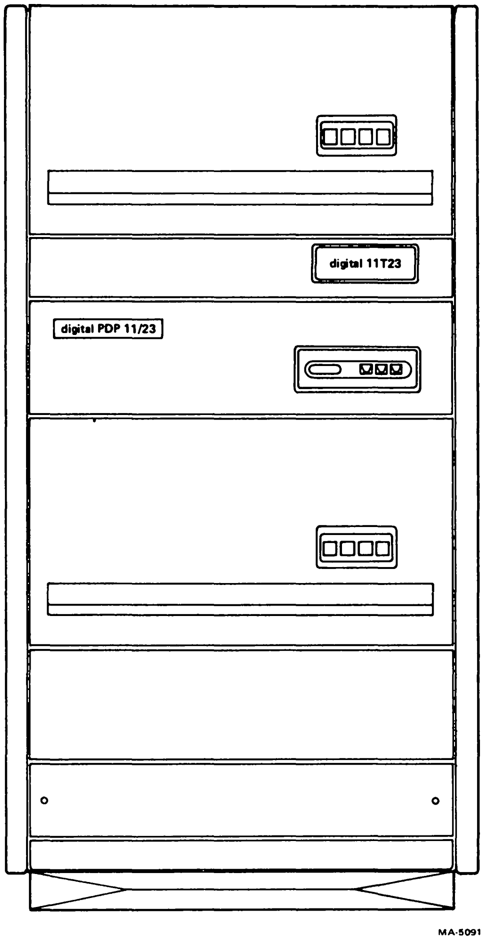


Figure 6. PDP-11T23 System

Figure 7 shows a rear view of the 11T23 system with the rear panel removed. Directly below drive 1 is empty space for a BA11-N expansion box. Below that is the 871 power controller.

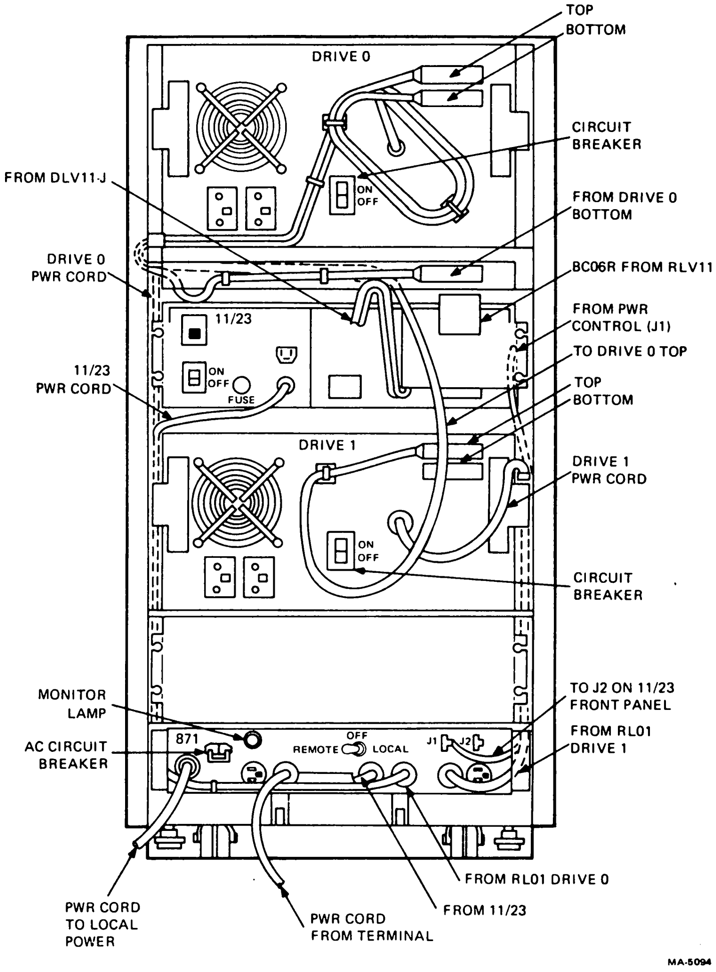


Figure 7. PDP-11T23 (Backpanel Removed)

RL01 Disk Drive

There are a number of controls and indicators on the front panel of the RLØ1 disk drive (Figure 8). Table 3 gives the function of each of these switches and indicators.

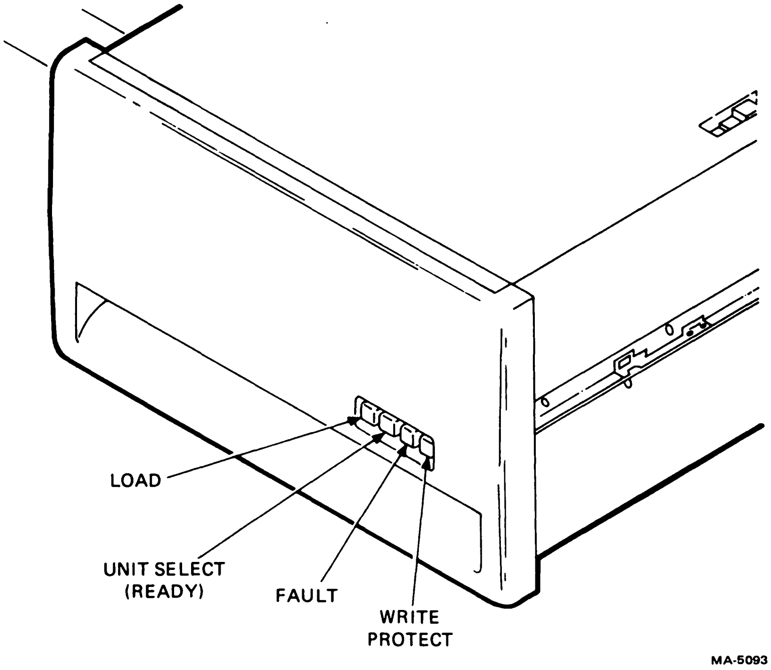


Figure 8.   RLØ1 Disk Drive (Front View)

Table 3.   RLØ1 Front Panel Operation

Indicator	Function
LOAD (push-button)	Lights to indicate that the spindle has stopped and a cartridge can be loaded.
UNIT SELECT (READY)	Lights to indicate that drive Ø or 1 is ready to read, write, or receive controller commands.
FAULT	Lights to indicate that a drive error condition exists.
WRITE PROT (push-button)	Lights to indicate that the cartridge currently mounted is protected from having data written on it.

PDP-11T23 Specification Summary

The specifications for the 11T23 system are as follows:

Environmental Conditions	Specifications
Altitude	2440 m (8000 ft) max
Operating temperature	10° to 40° C (50° to 105° F) nominal; reduce temperature 1.8° C/1000 m (1° F/1000 ft)
Maximum wet bulb temperature	28° C (82° F)
Minimum dew point	2° C (36° F)
Storage temperature	-40° C (-40° F) to 60° C (140° F)
Temperature change rate	16.6° C (30° F) per hour
Relative humidity	10% to 90% (no condensation)
Maximum shock pulse	10 gravity peak (half-sine) and 10 + 3 ms duration
Pitch and roll	+5 maximum

Power requirements	
PDP-11T23 system	860 W
Optional LA120	440 W
Optional VT100	100 W
Optional LA38	45 W

PDP-11V23/11T23 OPTIONS

There are many options available with the 11V23/11T23. The modules summarized below are part of a minimum system.

Processor

The KDF11-AA is a 16-bit, high-performance microprocessor contained on one dual-height multilayer module (M8186). Utilizing the latest MOS/LSI technology, the KDF11-AA brings the full PDP-11/34 functionality to a microprocessor that communicates along the LSI-11 bus. The KDF11-AA contains memory management as a standard feature and offers floating point as an option (KDF11-A).

The processor uses the LSI-11 bus with new four-level interrupt bus protocol and parity check features. The KDF11-AA is compatible with existing LSI-11 processors and devices.

MSV11-D Memory

The MSV11-D module has either 8K, 16K, or 32K by 16 bits of MOS memory. The MSV11-E is the same as the MSV11-D except that it has an 18-bit word that generates and detects byte parity for each word. The modules have on-board memory refresh and perform the necessary LSI-11 bus cycles. The memory addressing is selectable by the user by configuring switch settings. The module can use a battery backup system to preserve data when primary power is lost.

DLV11-J Serial Line Unit

The DLV11-J contains four independent asynchronous serial line channels used to interface peripheral devices to the LSI-11 bus. Each channel transmits and receives data from the peripheral device over EIA data leads (lines that do not use a control line). The module can be used with 2Ø mA current loop devices if a DUV11-KA adapter is used. The DLV11-J has jumper-selectable baud rates from 15Ø to 38.4K baud.

BDV11 Bootstrap/Terminator

The BDV11 module has 2K words of read-only memory (ROM) that contains diagnostic and bootstrap programs. These programs are user-selectable by setting dual in-line package (DIP) switches. The diagnostic programs will test the processor, the memory, and the user's console. The bootstrap programs can boot LSI-11 peripheral devices. The module also has 12Ø-ohm bus termination circuits.

The user can add up to 16K words of ROM and up to 2K words of erasable programmable ROM (EPROM) on the module. This 18K words of additional memory can be used with no increase in the amount of I/O address space.

RXV21 Dual Floppy Disk System

The RXV21 option consists of an interface module, cable assembly, and either a single or dual drive RXØ2 floppy disk. This option is a random access mass storage device that stores data in fixed-length blocks on a preformatted flexible diskette. Each diskette can store and retrieve up to 512K 8-bit bytes of data. The RXV21 system is rack-mountable in the standard 48.3 cm (19 in) cabinet.

This completes the course module for the 11V23/11T23 Introduction. Review the material covered and when you are ready, ask the Course Administrator for the module test.

PDP-11V23/11T23 SYSTEM MAINTENANCE

LSI-11/23 BUS CONCEPTS

LSI-11/23 Bus Concepts

INTRODUCTION

An LSI-11 computer is composed of many different units that operate together to form a complete computer system. These units could include the PDP-11/23 Central Processing Unit (CPU), a semiconductor memory, and any number of peripheral devices, such as a DECscope video terminal, an RX02 floppy disk drive, and DECprinter line printer. Operation of the computer system involves transferring addresses, data, and control information among these major system elements.

OBJECTIVES

1. Identify the major functions of:

   - a bus
   - an interface

2. Describe the fundamental concepts of the LSI-11 bus by answering test questions on:

   - Master/slave relationship
   - Dynamic bus control
   - Interlocked communication

3. Describe the principles of LSI-11 bus cycles by using bus cycle sequence diagrams to answer test questions about the DATI, DATO, DATOB, DATIO, and DATIOB bus cycles.

4. Describe the concepts of data transfers by answering test questions on:

   - Programmed data transfer
   - Interrupts
   - Direct Memory Access

   Identify the basic principles of LSI-11/23 bus priority by correctly answering questions.

5. Describe the principles of the special bus functions by answering test questions about:

   - Bus initialization
   - Halt mode
   - Power-up/power-down sequence

SAMPLE TEST ITEMS

1. Buses carry what type of information?

   a. data only
   b. addresses only
   c. control information only
   d. all the above

2. A floppy disk can assume the role of bus master and of bus slave.

   True
   False

3. On a DATI bus cycle, the signal BRPLYL is sent in response to:

   a. BDAL Ø-15
   b. BDINL
   c. BBS7L
   d. BSYNCL

You may use a bus sequence diagram to answer this question.

4. During an interrupt, the CPU sends BIAKOL to the interrupting device in response to what signal?

   a. BSYNCL
   b. BRPLYL
   c. BIRQL
   d. BBS7L

5. In the halt mode the CPU can still grant interrupts.

   True _______
   False ______

BUS IDENTIFICATION

Connections among the CPU, memory, and peripheral devices are made by electric conductors called buses. The conductors that form these buses can be electric cables, etches on a printed circuit board, or even the backplane into which the printed circuit boards are plugged. Buses carry address, data, and control information among the CPU, memory, and peripheral devices. The bus that we will be discussing during this module is the LSI-11 as it is used with the KDF11 processor. Figure 1 shows the LSI-11 bus connecting some typical peripheral devices with the microcomputer module.

Unfortunately, peripherals cannot be simply plugged into the CPU. Most peripherals are standard devices that have been designed for use with more than one series of computer. For example, the DECscope video terminal is intended to operate not only with the LSI-11 microcomputer but also with any of the PDP-11 minicomputers, the VAX 11/78Ø, and the much larger DECSYSTEM 2Ø. Because each of these computers has its own method of handling data, there must be some method of connecting a peripheral to a specific computer so that the two devices can operate properly. This connection is accomplished by using an interface. An interface may be thought of as a converter placed between a peripheral and a specific computer. All connections from the computer system to the peripheral are made through this interface. You can see in Figure 1 that the DECscope console terminal is connected to the LSI-11 bus by a serial line interface. This interface converts the serial data required by the terminal to a form which can be used by the LSI-11 bus.

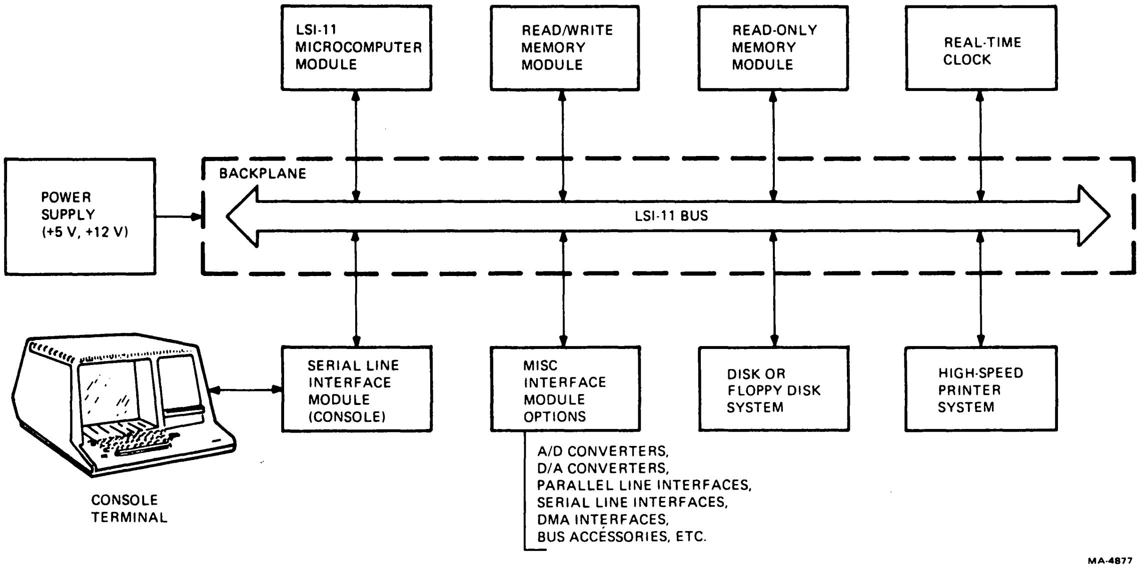

LSI-11 MICROCOMPUTER MODULE
READ/WRITE MEMORY MODULE
READ-ONLY MEMORY MODULE
REAL-TIME CLOCK
POWER SUPPLY (+5 V, +12 V)
BACKPLANE
LSI-11 BUS
SERIAL LINE INTERFACE MODULE (CONSOLE)
MISC INTERFACE MODULE OPTIONS
DISK OR FLOPPY DISK SYSTEM
HIGH-SPEED PRINTER SYSTEM
A/D CONVERTERS,
D/A CONVERTERS,
PARALLEL LINE INTERFACES,
SERIAL LINE INTERFACES,
DMA INTERFACES,
BUS ACCESSORIES, ETC.
CONSOLE TERMINAL
MA-4877

Figure 1. LSI-11 Bus Connections

EXERCISE

Circle the letter corresponding to the answer which best completes the given statement. You may use references. Check your answers with those given on the next page.

1. The conductors that make up a bus can be:

   a. electric cables
   b. etches on a printed circuit board
   c. part of a backplane
   d. all the above

2. An interface:

   a. converts serial data to parallel data

   b. converts parallel data to serial data

   c. converts data generated by a device, such as a DECscope, to a form which can be used by the LSI-11 bus

   d. is only required by larger systems such as the VAX 11/78Ø or the DECSYSTEM 2Ø

SOLUTIONS

1. d

2. c

BUS BASICS

Master/Slave Relationship

Whenever two devices use the LSI-11 bus to communicate, a master/slave relationship exists. Only two devices can communicate by means of the bus at any given time. When communicating, one device assumes the role of bus master while the other device becomes its bus slave (Figure 2).

Figure 2. Master and Slave

When a bus device becomes a master, its first job is to select the slave that it wants to communicate with. The master selects the slave by placing the address of the desired memory location or I/O device on the LSI-11 bus (Figure 3).

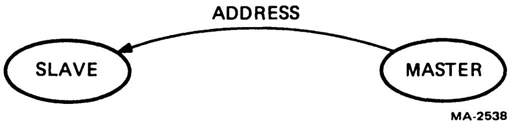


Figure 3. Master selects slave by sending address.

The next job of the master device is to specify the type of operation to be performed. This operation may involve some type of data transfer. By placing control information on the bus, the master specifies the type of operation (Figure 4).

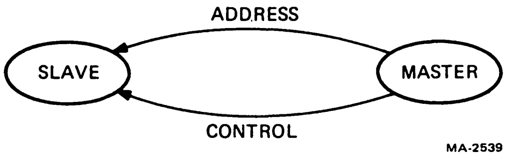


Figure 4. Master specifies type of transfer with control signals.

The master is now ready to initiate a data transfer. Suppose that data must be stored in the selected slave device. In this case the master places data on the bus so that it can be accepted by the slave for storage. Figure 5 shows a bus master sending data to a bus slave.

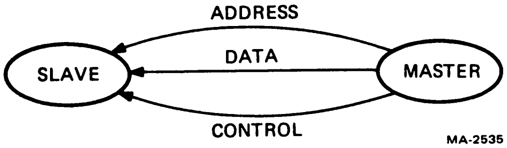


Figure 5. Master sends data to slave.

The master can also retrieve data from the slave as shown in Figure 6. Although it is now the slave that is putting the data on the bus, the transfer is still controlled by the master. It is the job of the bus master to select the location within the slave from which the data is to be transferred.

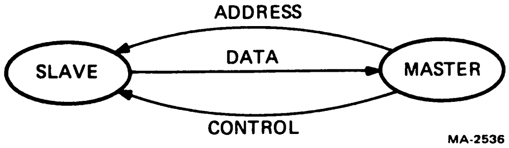


Figure 6. Master retrieves data from slave.

As an example, let us say that the CPU bus master wishes to read data from a memory location that is the bus slave. The CPU controls the transfer by addressing the memory and asking for data. The memory responds by sending data. Figures 5 and 6 show that regardless of the direction of the data transfer (master to slave or slave to master), the master always initiates the data transfer and always addresses the slave. A slave can never initiate a data transfer or address another device.

The program being executed by the CPU controls the master/slave relationship. For example, when an RLØ1 disk acts as bus master and transfers data to memory that is acting as a slave, the program has caused the data transfer to take place. The program has determined who will be master and who will be slave.

Dynamic Bus Control

When the program determines that data is to be transferred from the disk to memory, the CPU becomes master and commands the disk to send data. After receiving the command, the disk becomes bus master and sends data to memory, the slave.

Notice how the CPU and peripheral devices can change roles. This change of roles tells us that bus control is dynamic. Dynamic bus control simply means that once a bus master has completed its task, it can pass control of the LSI-11 bus over to another device which then assumes the role of master.

Memory is a slave. It cannot initiate a data transfer or address another device. As shown in Figure 7, the floppy disk system may address the read/write memory. However, the memory can never address the floppy.

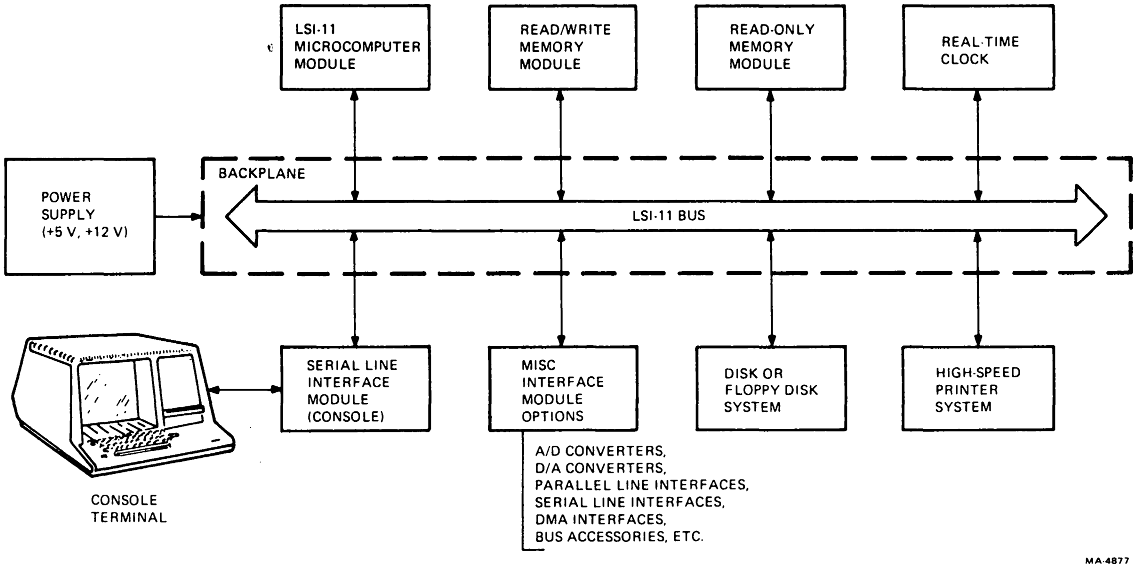

LSI-11 MICROCOMPUTER MODULE
READ/WRITE MEMORY MODULE
READ-ONLY MEMORY MODULE
REAL-TIME CLOCK
POWER SUPPLY (+5 V, +12 V)
BACKPLANE
LSI-11 BUS
SERIAL LINE INTERFACE MODULE (CONSOLE)
MISC INTERFACE MODULE OPTIONS
DISK OR FLOPPY DISK SYSTEM
HIGH-SPEED PRINTER SYSTEM
CONSOLE TERMINAL
A/D CONVERTERS,
D/A CONVERTERS,
PARALLEL LINE INTERFACES,
SERIAL LINE INTERFACES,
DMA INTERFACES,
BUS ACCESSORIES, ETC.
MA-4877

Figure 7. Typical LSI-11 System

Let's look at an example to illustrate what is meant by dynamic bus control and how bus mastership changes from one device to another. The system shown in Figure 8 consists of a CPU, a memory, and an RXØ2 floppy disk system. The CPU as master selects the floppy disk to function as slave. It then sends a command to the disk to transfer data to memory.

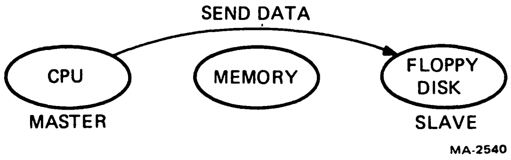


Figure 8. First the CPU is master.

The CPU gives up control of the bus to the floppy disk (Figure 9). At this point the floppy selects memory as its slave so that it can begin transferring data to memory. Note that the disk retains control of the bus only long enough to transfer its data. Then the disk relinquishes bus control to the CPU or to another device requesting the bus.

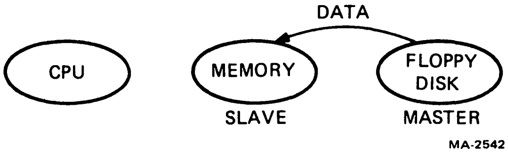


Figure 9. Next the floppy disk is master.

At this point, provided another device has not taken control of the bus, the floppy disk informs the CPU that the data transfer to memory is complete (Figure 1Ø). The CPU now becomes bus master, selects memory as its slave, and retrieves an instruction to determine what operation the CPU is to perform next (Figure 11).

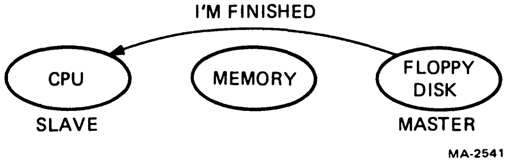


Figure 1Ø. The floppy disk tells the CPU that it is finished.

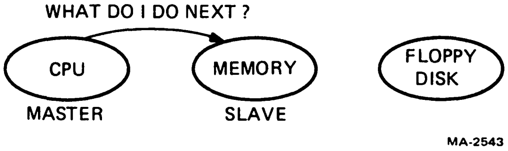


Figure 11. The CPU becomes master once again.

Notice how control of the bus in the example changes back and forth between the CPU and floppy disk. This is what dynamic (constantly changing) bus control means. Also notice that only the CPU and floppy disk assume roles as master since memory is always a slave.

Interlocked Communication

Communication between master and slave is interlocked, meaning that no data transfer occurs unless the slave issues a response signal for every control signal sent by the master. If we could listen to a typical dialogue between master and slave where the master wishes to retrieve data from memory, it might sound like this:

Master: Give me data.

Slave: Here it is.

Master: Thank you.

Slave: You are welcome.

Figure 12 is a sequence diagram showing the same dialogue in picture form. You will be referencing sequence diagrams in later chapters to illustrate the relationships among LSI-11 bus signals. For every statement made by the master there is a response from the slave. Now suppose that when the master says, "Give me data," there is no reply from the slave. In this case, all communication with the slave is broken off and the bus is now available for any other device to become master.

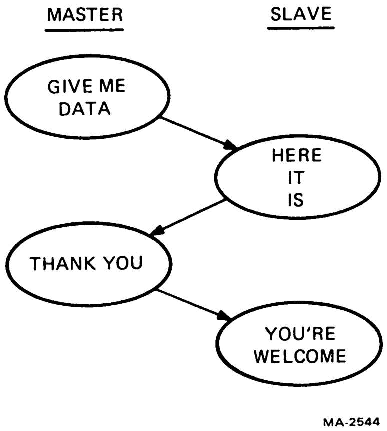


Figure 12. Dialogue Between Master and Slave

Because communication is interlocked, the LSI-11 bus is asynchronous. An asynchronous bus can handle devices with a wide range of operating speeds. Each device is allowed to transfer data at its own maximum speed. The DECscope video terminal and the RLØ1 disk both have very different operating speeds, yet the LSI-11 bus can handle both of them. Interlocked communication allows the LSI-11 bus to be asynchronous. The speed with which the slave replies to the master is unimportant as long as there is a reply.

Field service engineers sometimes refer to interlocked communication as "handshaking," indicating that two devices are present and interacting. The terms "interlocked communication" and "handshaking" have the same meaning and may be interchanged.

Summary

In this section we have covered three main points.

1. Two devices communicate by means of a master/slave relationship in which the master always controls the bus.

2. Bus control is dynamic. It can be passed from one device to another, allowing different devices to assume the role of master.

3. All dialogue between the master and slave is interlocked. When the master issues a control signal, the slave must produce a response signal or communication stops.

EXERCISE

Indicate whether the following statements are true or false by checking either column. You may use references. Check your answers with those given on the next page.

True False

1. Whenever two devices use the LSI-11 bus to communicate, a master/slave relationship exists. ____ ____

2. An RLØ1 can assume the role of bus master as well as that of bus slave. ____ ____

3. Memory may address another device and initiate a data transfer. ____ ____

4. Devices are not built to be bus masters or bus slaves. ____ ____

5. The CPU can never become a bus slave. ____ ____

6. Interlocked communication means that if the slave does not issue a response signal for every control signal sent by the master, the master will attempt to remedy the error. ____ ____

SOLUTIONS

1. True
2. True
3. False
4. True
5. False
6. False

BUS CYCLES

Types of Bus Cycles

In the Introduction you learned that the purpose of the LSI-11 bus is to carry address, data, and control information among the CPU, memory, and peripheral devices. The last section demonstrated how a device becomes bus master, selects a bus slave, and causes a data transfer to take place. Now we will look in detail at the process of data transfer.

There are five types of data transfers or bus cycles that can take place on the LSI-11 bus. In each of the descriptions that follow, the direction of the data transfer is always in relation to that of the bus master.

- DATI - During a Data In bus cycle a data word moves from the slave to the master.
- DATO - During a Data Out bus cycle a data word moves from the master to the slave.
- DATOB - A Data Out Byte bus cycle is similar to a Data Out bus cycle except that here only one byte of data moves from the master to the slave.
- DATIO - A Data In-Out bus cycle is a combination of a Data In and a Data Out bus cycle. First a data word moves from the slave to the master. Then another data word moves from the master to the slave.
- DATIOB - A Data In-Out Byte bus cycle is similar to a Data In-Out bus cycle except that after a data word is transferred from the slave to the master, only a byte of data is returned to the slave.

Before we continue, here are the correct pronounciations for the names of the bus cycles.

DATI is pronounced DATA EYE
DATO is pronounced DATA OH
DATOB is pronounced DATA OH BE
DATIO is pronounced DATA EYE OH
DATIOB is pronounced DATA EYE OH BE

At this point you are ready to study a bus cycle in detail. This study includes a description of what events take place on the bus as well as what bus signals cause these events to take place. All bus signal names are prefixed with the letter B. This letter simply stands for the word "bus." For example BDIN means "bus data in."

All LSI-11 bus signals, with the exception of two, have the letter L as a suffix. This letter stands for the word low and means that the signal is at the lower of two logic voltages when true (asserted) and at the higher of two logic voltages when false (not asserted). For example BDINL tells us that the signal BDIN is low when asserted. The two exceptions mentioned earlier are BDCOK H and BPOK H. These two signals are high when asserted.

The DATI Bus Cycle

Figure 13 shows a simplified sequence diagram of the events that must take place during a DATI bus cycle. In following the diagram in Figure 13 from top to bottom, notice that the master selects the slave with which it will communicate by broadcasting the address of the slave to every device on the bus. Only the addressed slave recognizes its address and the slave remembers or stores the fact that it has been selected.

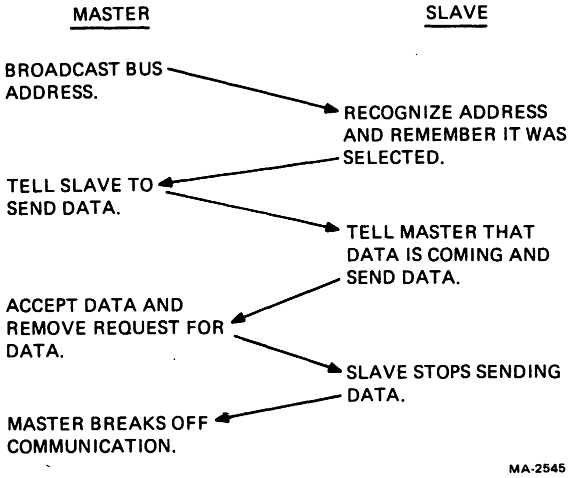

MASTER
SLAVE
BROADCAST BUS ADDRESS.
RECOGNIZE ADDRESS AND REMEMBER IT WAS SELECTED.
TELL SLAVE TO SEND DATA.
TELL MASTER THAT DATA IS COMING AND SEND DATA.
ACCEPT DATA AND REMOVE REQUEST FOR DATA.
SLAVE STOPS SENDING DATA.
MASTER BREAKS OFF COMMUNICATION.
MA-2545

Figure 13. Simplified Diagram of DATI Bus Cycle

The master then tells the slave to send data. The slave warns the master that data is coming and then sends a single data word. The master accepts the data word and removes the request for data. When the slave sees that there is no longer a request for data, it stops sending. At this point the master breaks off communication with the slave. The sequence diagram shows not only what events take place but also the order and cause.

Before looking at a sequence diagram showing the actual bus signals for a DATI bus cycle you must know something about the LSI-11 memory organization. Without memory management the LSI-11 is capable of addressing bus locations from zero all the way up to 32K (32 thousand). Only the first 28K locations can be used for memory. The last 4K locations, 28K to 32K, are reserved for peripheral device interfaces. In short, to address a peripheral device, the bus address must be between 28K and 32K. To address a memory location the bus address must be below 28K. Figure 14 shows memory organization. With memory management the processor is capable of addressing memory up to 124K and a peripheral device address space from 124K to 128K. Memory management will be discussed in detail later in this module.

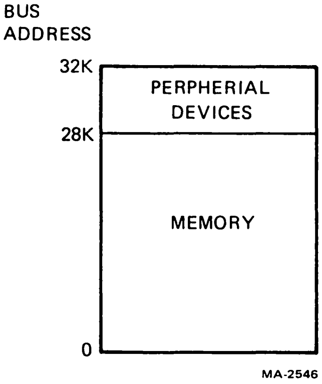


Figure 14. LSI-11 Memory Organization

The actual sequence diagram shown in Figure 15 recalls the fact that the first thing the master must do is select the slave with which it will communicate by broadcasting the slave's address on the bus.

NOTE

Throughout the discussion on bus cycles memory management will not be covered.

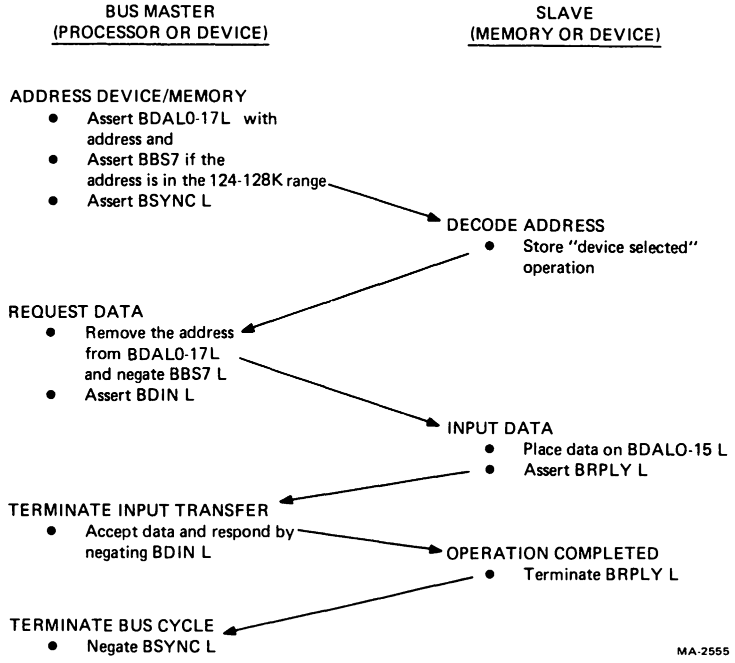


Figure 15. DATI Bus Cycle

This broadcasting is accomplished on 18 lines referred to as BDALØL through BDAL17L. Remember that the B stands for bus and the L stands for low asserted. The remaining letters, DAL, stand for data and address lines. Thus the 18 lines, BDALØL through BDAL17L, serve two purposes. They can carry an 18 bit bus address or they can carry a 16 bit data word. Without memory management the largest address sent is 16 bits. These lines are also bidirectional, that is, they can carry data or addresses in either direction along the bus.

If a peripheral device is being addressed, that is, if the bus address is between 28K and 32K, the signal BBS7L (bus bank select 7 low) must also be asserted. If we are addressing memory, which has a bus address of less than 28K, then BBS7L is not asserted.

Finally, the master asserts BSYNCL (bus sync low) to inform all devices that an address has been placed on the BDAL lines. BSYNCL remains asserted throughout the bus cycle. The bus master has just completed selection of the slave.

Follow the arrow in Figure 15 to the right. Notice that the selected slave recognizes its address and stores "device selected." Moving back to the left, we can see that the master is now ready to request data. But first it removes the address from DBALØL through BDAL15L and negates (removes) BBS7L. The master now says, "Give me data," by asserting BDINL (bus data in low). The slave, in turn, places the 16 bit data word on lines BDALØL through BDAL15L and says, "Here it is," by asserting BRPLY (bus reply low).

The master accepts the data and signals to the slave that it has the data by negating BDINL. The slave then removes the data from BDALØ-15 and negates BRPLYL. Finally, the master ends the bus cycle by negating BSYNCL.

The sequence diagram we have just looked at assumes normal operation. But, what if the addressed slave is malfunctioning and does not answer? The bus master is looking at the address lines (BDALØ-15L) and at the reply line (BRPLYL). When an address is placed on the bus and there is no reply within 1Ø microseconds (1Ø millionths of one second), the CPU ends the bus cycle and begins to execute a program that tries to clear up the problem. If a device other than the CPU is master and there is no reply within 1Ø microseconds, the device interrupts the operation of the CPU and inform it that an error has taken place.

So far we have looked at 2Ø of the LSI-11 bus lines:

- BDALØL through BDAL15L
- BBS7L
- BSYNCL
- BDINL
- BRPLYL

Before continuing with this section, look up each of these bus signals in Appendix A and read the corresponding entry. Then return to this point and continue.

The DATO and DATOB Bus Cycles

The DATO and DATOB bus cycles (Figure 16) are identical to each other with one exception. The DATO moves a 16 bit data word from the master to the slave, while a DATOB moves an eight bit byte from the master to the slave.

If we look at the top of Figure 16, we can see that the bus cycle starts off in the same way as the DATI bus cycle.

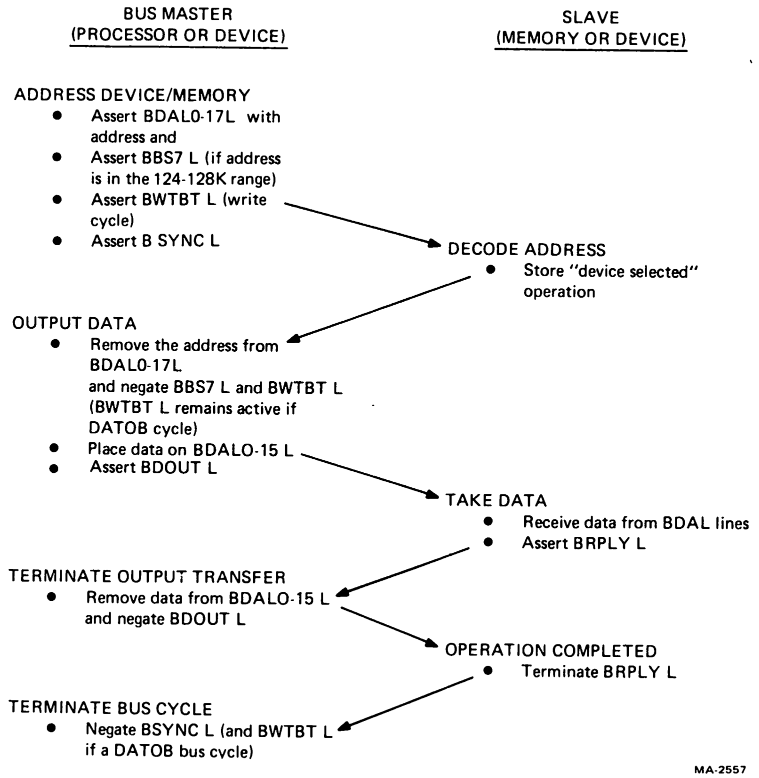

BUS MASTER
(PROCESSOR OR DEVICE)
SLAVE
(MEMORY OR DEVICE)
ADDRESS DEVICE/MEMORY
● Assert BDAL0-17L with address and
● Assert BBS7 L (if address is in the 124-128K range)
● Assert BWTBT L (write cycle)
● Assert B SYNC L
DECODE ADDRESS
● Store "device selected" operation
OUTPUT DATA
● Remove the address from BDAL0-17L and negate BBS7 L and BWTBT L (BWTBT L remains active if DATOB cycle)
● Place data on BDAL0-15 L
● Assert BDOUT L
TAKE DATA
● Receive data from BDAL lines
● Assert BRPLY L
TERMINATE OUTPUT TRANSFER
● Remove data from BDAL0-15 L and negate BDOUT L
OPERATION COMPLETED
● Terminate BRPLY L
TERMINATE BUS CYCLE
● Negate BSYNC L (and BWTBT L if a DATOB bus cycle)
MA-2557

Figure 16.   DATO or DATOB Bus Cycle

However, in this case, the master not only selects the slave but also asserts a signal called BWTBTL (bus write byte low). It asserts this signal during the first portion of the bus cycle to tell the peripheral device that we are going to write data. If BWTBTL remains asserted during the last portion of the bus cycle, a byte transfer takes place (DATOB). On the other hand, if BWTBTL is negated during the last portion of the bus cycle, word transfer takes place (DATO).

In the sequence diagram, when the slave recognizes its bus address, it stores "device selected." At this point, the master removes the address from BDALØ-15 and negates BBS7L if it has been asserted. If this is a DATOB bus cycle, then BWTBTL remains active; otherwise, it is negated. Also the master places the data on BDALØ-15 and warns the slave that data is there by asserting BDOUTL (bus data out low).

The slave accepts the data from BDAL0-15 and tells the master it has done so by asserting BRPLYL. When the master sees BRPLYL, it knows that the data has been accepted. It now removes the data from BDAL0-15 and negates BDOUTL.

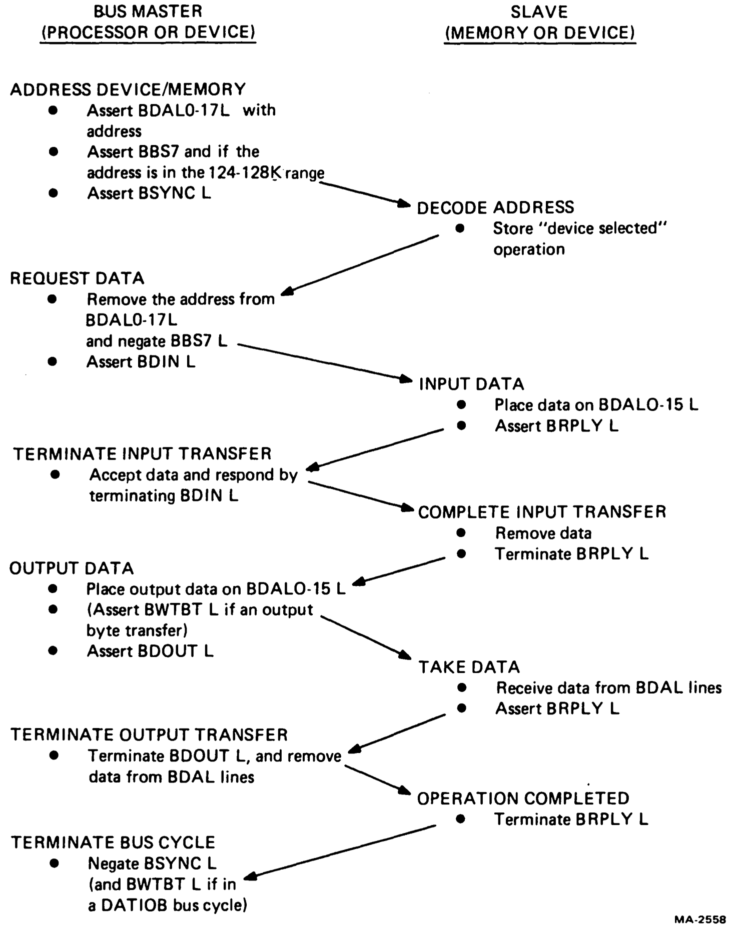
The slave negates BRPLYL and the master, in turn, negates BSYNCL. The master negates BWTBTL if this is a DATOB bus cycle. In the DATO/DATOB bus cycle, just as in the DATI bus cycle, if BRPLYL is not returned within 10 microseconds from the time an address is placed on BDAL0-15L, the master steps in and ends the bus cycle.

We have just discussed two new signals: BWTBTL and BDOUTL. Before continuing with this section, look up each of these bus signals in Appendix A (p. BC-51) and read the corresponding entry. Then return to this point and continue reading.

The DATIO and DATIOB Bus Cycle

DATIO and DATIOB bus cycles can be considered read/modify/write operations. Read/modify/write operations are used whenever data is written back to the same location that it was read from. It takes less time to do a DATIO bus cycle than to do a DATI followed by a DATO bus cycle. First the master reads a data word from the slave (DATI). The master then writes back either a data word (DATO) or a data byte (DATOB) to the slave.

In looking at Figure 17 you can see that the top half of the sequence diagram is identical to the DATI bus cycle. Locate the third entry down under the column headed "Slave." It says "complete input transfer: remove data; terminate BRPLYL." We would expect that the master would now negate BSYNCL, but it does not. Rather, the master begins a DATO or a DATOB bus cycle. Note that the master does not have to put the device address on the bus a second time. It simply goes ahead and places the data on the BDAL lines and sends BDOUTL. Also notice that the signal BWTBTL is only used for the DATIOB bus cycle and not used at all for the DATIO bus cycle.



BUS MASTER
(PROCESSOR OR DEVICE)

SLAVE
(MEMORY OR DEVICE)

ADDRESS DEVICE/MEMORY
- Assert BDAL0-17L with address
- Assert BBS7 and if the address is in the 124-128K range
- Assert BSYNC L

DECODE ADDRESS
- Store "device selected" operation

REQUEST DATA
- Remove the address from BDAL0-17L and negate BBS7 L
- Assert BDIN L

INPUT DATA
- Place data on BDALO-15 L
- Assert BRPLY L

TERMINATE INPUT TRANSFER
- Accept data and respond by terminating BDIN L

COMPLETE INPUT TRANSFER
- Remove data
- Terminate BRPLY L

OUTPUT DATA
- Place output data on BDALO-15 L
- (Assert BWTBT L if an output byte transfer)
- Assert BDOUT L

TAKE DATA
- Receive data from BDAL lines
- Assert BRPLY L

TERMINATE OUTPUT TRANSFER
- Terminate BDOUT L, and remove data from BDAL lines

OPERATION COMPLETED
- Terminate BRPLY L

TERMINATE BUS CYCLE
- Negate BSYNC L (and BWTBT L if in a DATIOB bus cycle)

Figure 17. DATIO or DATIOB Bus Cycle

Summary

You have just learned about the five types of bus cycles and how they are used to transfer data between the master and slave.

- DATI
- DATO
- DATOB
- DATIO
- DATIOB

We have also looked at the following bus signals and how they are used on the LSI-11 bus.

- BDALØ-17
- BBS7L
- BSYNCL
- BDINL
- BRPLYL
- BDOUTL
- BWTBTL

EXERCISE

Listed below are events that take place during a DATI bus cycle. Put them in order by writing the letter of the event next to the correct number. You may use references. Check your answers with those given on the following page.

1. ____ a. Tell master that data is coming and send data.

2. ____ b. Broadcast bus address.

3. ____ c. Slave removes data from bus.

4. ____ d. Accept data and remove request for data.

5. ____ e. Master breaks off communication.

6. ____ f. Tell slave to send data.

SOLUTIONS

1. b
2. f
3. a
4. d
5. c
6. e

DATA TRANSFERS AND PRIORITY

Methods of Data Transfers

You have learned that the function of the LSI-11 bus is to carry data, addresses, and control information between master and slave devices. Also you have seen that the master uses one of five basic bus cycles to communicate with the slave. In an actual data transfer between a peripheral device and the CPU, the bus master may select one of three methods in which to use these bus cycles to transfer data. They are:

- Programmed data transfer
- Interrupt initiated programmed data transfer
- Direct Memory Access (DMA)

The program being executed by the CPU determines which of the three methods will be used. We will discuss the simplest method first: the programmed data transfer.

Programmed Data Transfer

To demonstrate programmed data transfer, let's consider a situation where the CPU is to move data from one location to another. This transfer is part of normal program execution of a MOVE instruction.

Figure 18 illustrates the LSI-11 memory. The CPU moves data from the source location to the destination location. First the CPU becomes bus master and reads the data in the source location by doing a DATI bus cycle. At the completion of this bus cycle the data has moved to the CPU. Then, as shown in Figure 19, the CPU addresses the destination location and writes the data to memory with a DATO bus cycle.

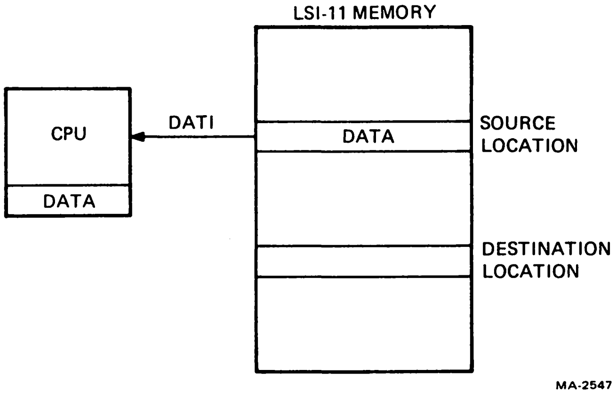


Figure 18. First the CPU does a DATI bus cycle.

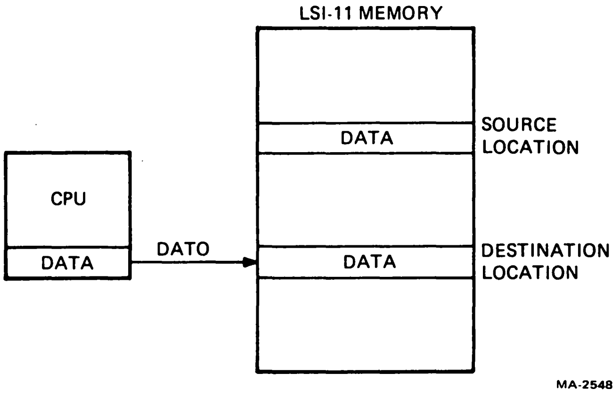


Figure 19. Next the CPU does a DATO bus cycle.

Have you noticed that in this case the CPU has to do two bus cycles to execute the instruction? This instruction cycle requires two bus cycles. If the processor is sending data to a peripheral device, the process is exactly the same. Figure 20 shows the CPU writing data to the RX01 floppy disk memory data buffer.

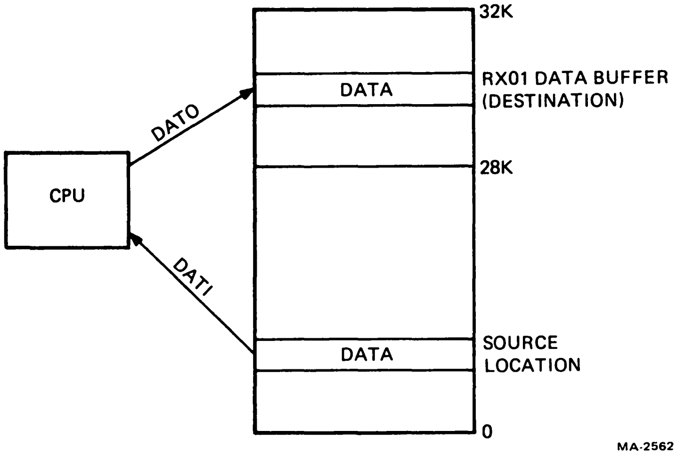


Figure 2Ø. With a single MOVE instruction, the CPU performs two bus cycles and sends data to the RX01 memory data buffer.

First the CPU retrieves the data by addressing the source location and does a DATI bus cycle. Next the processor sends this data to the RXØ1 by addressing its data buffer and doing a DATO bus cycle. The only difference between this example and the one shown in Figure 19 is that here the bus address of the destination location is in the top 4K of the address range. Remember that bus addresses between 124K and 128K are reserved for peripheral devices and are not part of memory. These two examples clarify what programmed data transfer involves. When the processor is executing a program and some of the instructions in the program move data to peripheral devices, the CPU is performing a programmed data transfer.

Let's look at some of the features of a programmed data transfer. First, it can only be performed by the CPU because only the CPU can execute instructions. Secondly, a programmed data transfer requires no special bus signals. The CPU simply addresses the device and does a bus cycle. Finally, the addressed device must be ready to transfer data. If it is not ready, the transfer is very slow. In Figure 2Ø, if the RXØ1 is not ready to accept the data word, the CPU has to stop and wait until the data can be accepted.

Interrupt Initiated Programmed Data Transfer

Interrupts allow the CPU to execute a program without being tied up waiting for a device to become ready to transfer data. When the device becomes ready, it interrupts the CPU and says, "I am ready for data." Then the CPU stops executing its program and begins a programmed data transfer between itself and the interrupting device. Figure 21 is a simplified sequence diagram showing the basic events that take place during an interrupt.

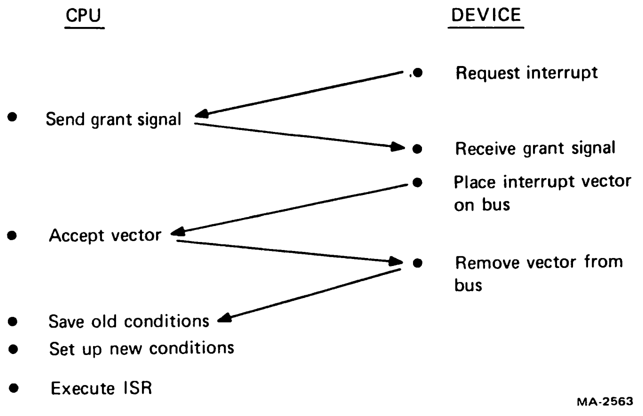


Figure 21. A Simplified Interrupt Sequence Diagram

Initially, the device requests an interrupt. The CPU, upon receiving the interrupt request, sends out an interrupt grant signal. Without this signal the interrupting device cannot continue.

The device places a vector address on the bus just as soon as it receives the grant. A vector (or pointer) address tells the CPU where in memory it can find the address of first instruction of a program. The program that this vector is pointing to is called an Interrupt Service Routine (ISR).

Contrary to what some people think, CPUs are not intelligent. When a device interrupts, the CPU has no idea of what to do. So the interrupting device sends over a vector address. This address points to the address of first instruction in the ISR. Once it begins to execute, this program must do two things. First it must find out what the device wants; then it must perform the operation indicated by the interrupting device.

So in our sequence diagram, the device has just put its interrupt vector on the bus. After the CPU accepts this vector the device will remove the address from the bus. As the final operation in servicing the interrupt, the CPU must store the old processor conditions so that it knows where to continue after the interrupt. It loads the new processor conditions so that it knows where to start the ISR. And finally it begins to execute the ISR.

What happens now depends upon the device that is interrupting as well as the reason why it is interrupting. After the ISR determines what the interrupting device wants, it will usually perform one of the five basic bus cycles discussed in the last lesson. Let's say, for example, that the CPU does a DATO and transfers a single word to the device. The operation for which the device interrupted the CPU is now over. The CPU gives up control of the bus and continues with the program it was executing before the interrupt took place.

The important thing to remember about an interrupt is that it is a method of attracting the attention of the CPU. Once the processor's attention has been attracted a programmed data transfer takes place. Figure 22 shows an actual interrupt sequence diagram. This diagram contains some new bus signals. You will encounter some signals that have already been discussed, only this time they are used differently.

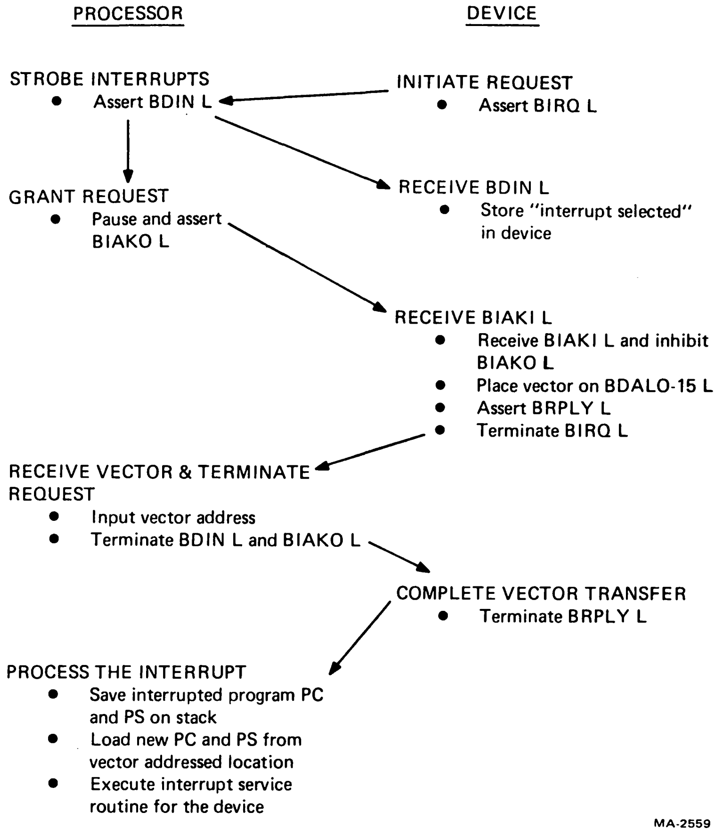

PROCESSOR
DEVICE
STROBE INTERRUPTS
● Assert BDIN L
INITIATE REQUEST
● Assert BIRQ L
RECEIVE BDIN L
● Store "interrupt selected" in device
GRANT REQUEST
● Pause and assert BIAKO L
RECEIVE BIAKI L
● Receive BIAKI L and inhibit BIAKO L
● Place vector on BDALO-15 L
● Assert BRPLY L
● Terminate BIRQ L
RECEIVE VECTOR & TERMINATE REQUEST
● Input vector address
● Terminate BDIN L and BIAKO L
COMPLETE VECTOR TRANSFER
● Terminate BRPLY L
PROCESS THE INTERRUPT
● Save interrupted program PC and PS on stack
● Load new PC and PS from vector addressed location
● Execute interrupt service routine for the device
MA-2559

Figure 22. Interrupt Request/Acknowledge Sequence

Now we will follow the sequence of events as a DECscope video terminal interrupts the processor to send a single data byte. The sequence begins with the DECscope controller requesting an interrupt by asserting BIRQL (bus interrupt request low). The CPU then sends BDINL and the interrupt grant signal BIAKOL (bus interrupt acknowledge out low). The DECscope controller receives the grant signal as BIAKIL (bus interrupt acknowledge in low) and replies by placing the vector address on BDALØ-17L and asserting BRPLYL. (BIAKOL and BIAKIL are two names for the same signal. We will discuss this signal in detail when you learn about bus priority.)

BIRQL can now be negated. The processor accepts the vector address and indicates this acceptance by negating BDINL and BIAKOL. Next the DECscope controller removes the vector address from the bus and negates BRPLYL. Finally the CPU executes the ISR, services the controller, and ultimately returns to its original program.

One question remains about interrupts. When can one take place? An interrupt can only take place after the end of an instruction cycle. This is because the CPU must stop executing its program in order to do the ISR. An instruction in the standard instruction set must always be completed before a new one is started.

You have learned about two new signals from the previous example: BIRQL and BIAKOL/BIAKIL. You have also seen that BDINL is used differently here than it has been in other examples. Before continuing, look up these signals in the table in Appendix A (p. BC-51) and read the corresponding entries. Then return to this point and continue reading.

Direct Memory Access

The Direct Memory Access (DMA) is the fastest type of data transfer. During a DMA, a high speed peripheral device, usually a disk, reads or writes data directly to memory without disturbing the processor. Memory is always the slave while the high-speed device is the master.

Before a DMA can take place, there are two registers which must be set up under program control. These are the Word Count Register and the Memory Address Register. When the program being executed by the CPU determines that it is time to transfer data to or from a high speed device, the CPU places the number of words to be transferred in the Word Count Register. Also the address of the first memory location from which data is read from or written to is placed in the Memory Address Register.

Circuits on the CPU module are used to arbitrate the DMA, that is to decide who will be allowed to do a DMA and when a DMA can be done. The CPU can arbitrate DMAs at the same time it is executing a program. First, this means that the DMA can be arbitrated, or set up, while the bus is still being used by another master/slave pair. At the completion of the present bus cycle, the peripheral breaks in and transfers data. Upon completion of the transfer, bus mastership is given up. Secondly, at the completion of the bus cycle, the CPU immediately resumes executing its program. Since the CPU has not been disturbed during the DMA, there is no need to restore the contents of any registers as was required after an interrupt. As you look at the simplified DMA sequence diagram shown in Figure 23, notice that the first two steps can take place even if another master/slave pair is using the bus.

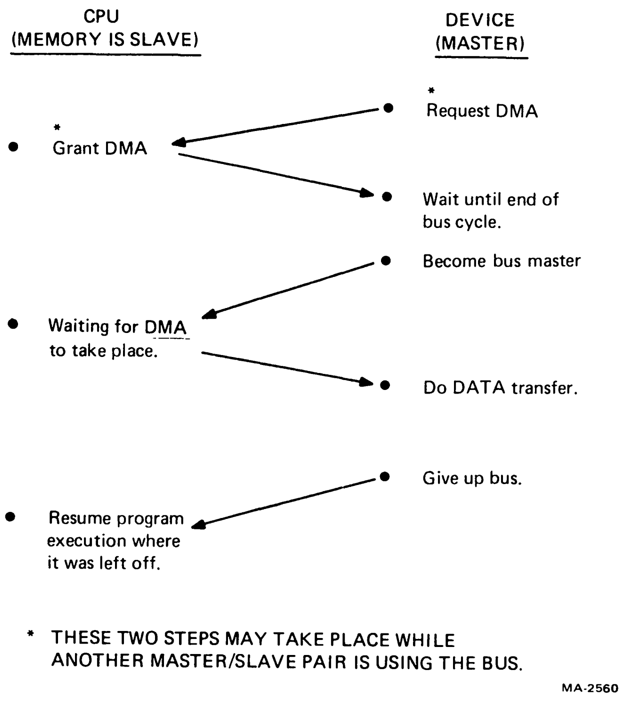


Figure 23. Simplified DMA Sequence Diagram

The device requests a DMA and the CPU grants it. Nothing more happens until the bus is free. At the end of the next bus cycle the device becomes bus master. The CPU waits for the DMA to take place. The device can now do any one of the five basic bus cycles and then give up the bus. In the last step the CPU simply resumes operation. Figure 24 shows the actual DMA sequence and the bus lines that are involved in the requesting and granting of the bus.

A device requests the bus by asserting BDMRL (bus DMA request low). The processor responds by sending BDMGOL (bus DMA grant out low), thus allowing the device to become bus master. This signal also stops further processor generation of BSYNCL, preventing the processor from starting a new bus cycle. The device receives the grant signal as BDMGIL (bus DMA grant in low). As soon as the bus is idle (BSYNCL and BRPLYL are both negated), the device takes over as bus master by asserting BSACKL (bus selection acknowledge low). At the same time the device negates BDMRL. (BDMGOL and BDMGIL are two names for the same signal. This signal will be discussed in detail when you learn about bus priority.) The CPU now negates BDMGOL and waits for the DMA to take place. The device does any one of the five basic bus cycles and then gives up the bus by negating BSACKL. Finally the CPU resumes its normal operation.

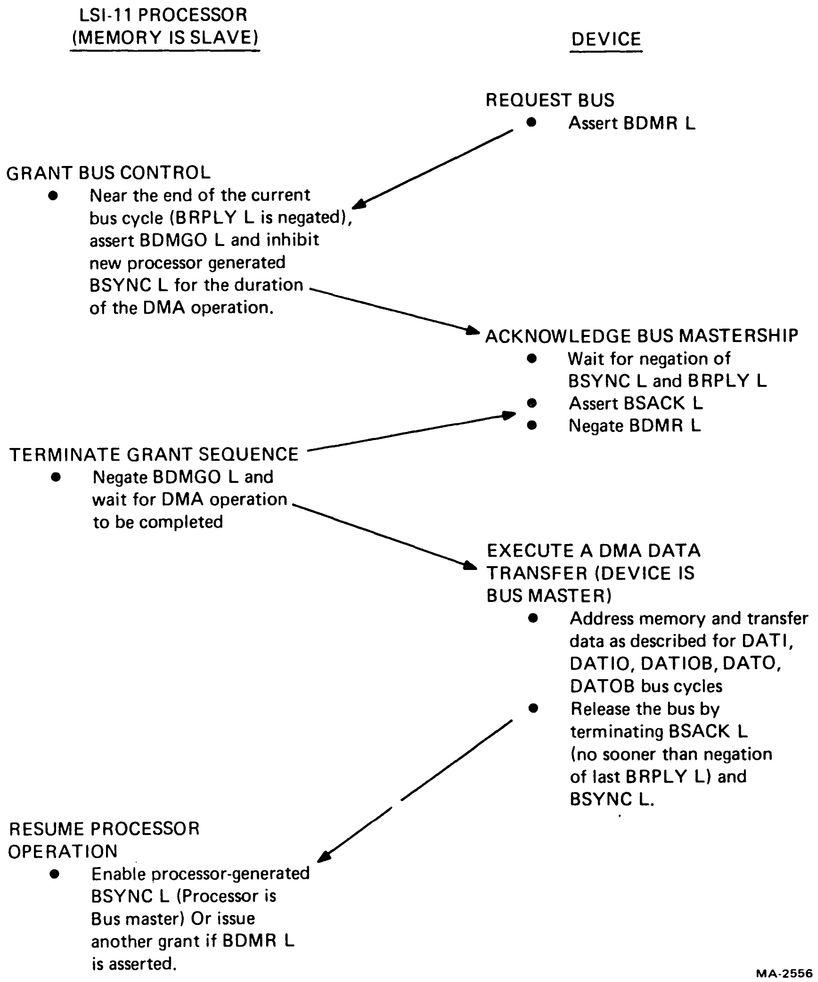

LSI-11 PROCESSOR
(MEMORY IS SLAVE)
DEVICE
REQUEST BUS
• Assert BDMR L
GRANT BUS CONTROL
• Near the end of the current bus cycle (BRPLY L is negated), assert BDMGO L and inhibit new processor generated BSYNC L for the duration of the DMA operation.
ACKNOWLEDGE BUS MASTERSHIP
• Wait for negation of BSYNC L and BRPLY L
• Assert BSACK L
• Negate BDMR L
TERMINATE GRANT SEQUENCE
• Negate BDMGO L and wait for DMA operation to be completed
EXECUTE A DMA DATA TRANSFER (DEVICE IS BUS MASTER)
• Address memory and transfer data as described for DATI, DATIO, DATIOB, DATO, DATOB bus cycles
• Release the bus by terminating BSACK L (no sooner than negation of last BRPLY L) and BSYNC L.
RESUME PROCESSOR OPERATION
• Enable processor-generated BSYNC L (Processor is Bus master) Or issue another grant if BDMR L is asserted.
MA-2556

Figure 24. DMA Request/Grant Sequence

The most important feature of DMA is that when the CPU arbitrates the request, it does not have to stop executing its program. For this reason, a DMA can be performed between any two bus cycles, even if this means that the DMA falls in the middle of an instruction cycle. Additionally, a DMA can still be arbitrated when the processor is halted. Since the ability to execute a program has nothing to do with the DMA process, the CPU can still service the DMA when halted.

You have learned three new signals: BDMRL, BDMGOL/BDMGIL, and BSACKL. Before reading on, look these signals up in the table in Appendix A and read the corresponding entries. Then return to this point and continue reading.

LSI-11 Bus Priority

In our discussion of interrupts and DMAs, every time a device requested the bus, the request was always granted. This is because we assumed that the device requesting bus mastership was the only device on the bus. In a real system, this is not the case. A small system may include an LA36 teleprinter, a DECscope video terminal, and an RXØ2 floppy disk. While the CPU module is performing programmed data transfers, the peripherals are attempting to take over bus mastership through interrupts and DMAs.

The CPU must be able to arbitrate these requests for the bus. Through arbitration, the CPU decides which device gets control of the bus. This is done by assigning each device a specific priority. If two or more devices ever request the bus at the same time, the device with the highest priority will always gain control. The KDF11 processor is capable of two methods of bus priority. One method uses a serial priority scheme which is totally compatible with the older 11/Ø3 systems. The second method employs a multi-level priority scheme which is not presently supported by DIGITAL software. The multi-level scheme will be explained here because it may be used on future DIGITAL systems.

Serial Priority

With the exception of priority grant signals, all signals are passed along the LSI-11 bus so that they are received by all devices at the same time. (There actually is a very small delay along the bus, but it can be neglected in a well-designed system.) The priority grant signals are daisy-chained, or transmitted serially along the bus as shown in Figure 25.

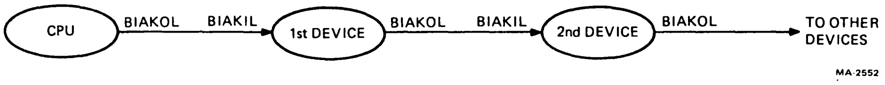


Figure 25. The interrupt grant signal is daisy-chained along the LSI-11 bus.

Here we can see that the CPU generates the interrupt grant signal BIAKOL. This signal is serial in the sense that it has to pass through the internal circuits of each device controller before it leaves the other side. Notice how the name of the signal changes as it gets passed from device to device. If the signal is leaving a module, such as the CPU or device controller, it is called BIAKOL (bus interrupt acknowledge OUT low). If the SAME signal is about to enter a module, it is called BIAKIL (bus interrupt acknowledge IN low).

Let's set up some rules for this grant signal. First, if a device requests an interrupt, it must receive BIAKIL asserted to continue with the interrupt. Secondly, if a device requesting an interrupt receives BIAKIL asserted, it will NOT pass the signal on to the next device. Only if the device is not requesting an interrupt will it pass BIAKOL on to the next device. Lastly, a device raises an interrupt by asserting BIRQ4L.

Figure 26 shows a system with three devices on the bus. The LA36, which is requesting the interrupt, captures the grant signal. It has received BIAKIL asserted but does not pass it on to the next device. Note that the floppy disk which is not interrupting passes BIAKIL to the next device.

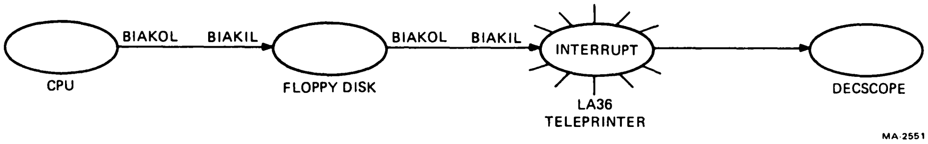


Figure 26. The LA36 teleprinter captures the grant signal.

What if two devices interrupt at the same time? In looking at Figure 27, we can see that both the floppy disk and the LA36 teleprinter are interrupting. Since the floppy disk has captured the grant signal, the LA36 cannot continue with its interrupt. However, the floppy disk can continue, and when it is finished transferring data, it will pass on the BIAKOL grant signal the next time it is raised. In Figure 28, the LA36 receives BIAKOL and proceeds with its interrupt.

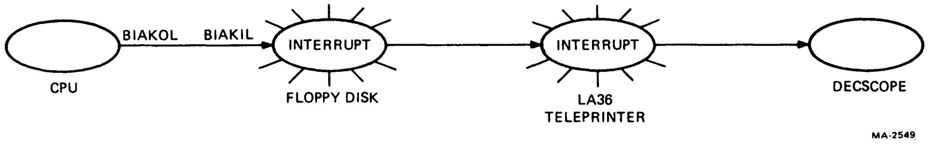


Figure 27. Two devices raise an interrupt at the same time.

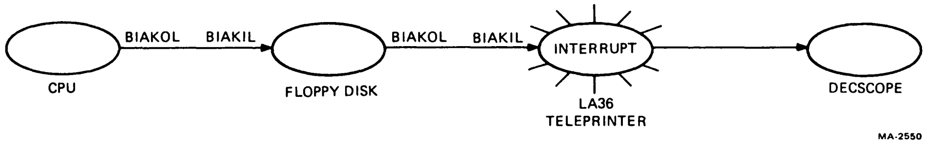


Figure 28. The LA36 continues with its interrupt.

Figure 28 demonstrates a very important principle of serial priority. The device closest to the CPU along the LSI-11V23 bus has the highest priority. In other words, if more than one device interrupts at the same time, the device closest to the CPU will always be serviced first.

DMA priority is handled in exactly the same way. Every device that is capable of performing a DMA has the signal BDMGOL/BDMGIL daisy-chained through it. Also a device requests a DMA by asserting the signal BDMRL. Therefore the device closest to the CPU will be granted DMAs before any other device.

Four-Level Interrupt Scheme

The KDF11 is capable of using a four-level interrupt scheme.

NOTE

The four-level interrupt scheme is not supported by DIGITAL software.

There are four interrupt request lines on the LSI-11 bus. They are designated BIRQ4L through BIRQ7L. When the KDF11 sees a request on one of these lines it will acknowledge it according to the following rules.

BIRQ7L is considered the highest priority request level, while BIRQ4L is the lowest priority level. This means, for example, that if requests were raised by BIRQ4L and BIRQ6L at the same time, the processor would acknowledge the level 6 request first.

On the other hand, the device interfaces must follow certain rules for asserting and monitoring the request lines. These rules are shown in Table 1.

NOTE

Presently DIGITAL manufactured interfaces only assert BIRQ4L and do not monitor any request lines.

Table 1. Device Interface Request Levels

Interrupt Level	Request Lines Asserted	Request Lines Monitored
Level 4	BIRQ4L	BIRQ5L BIRQ6L
Level 5	BIRQ4L BIRQ5L	BIRQ6L
Level 6	BIRQ4L BIRQ6L	BIRQ7L
Level 7	BIRQ4L BIRQ6L BIRQ7L	(None)

Lets look at two examples to see how this table is used.

Example 1:

If a level 7 device requested an interrupt, the following would take place:

1. Level 6 devices will not interrupt because they are monitoring level 7.
2. Level 5 devices will not interrupt because they are monitoring level 6.
3. Level 4 devices will not interrupt because they are monitoring level 6.

Example 2:

If a level 6 device requested an interrupt, the following would take place:

1. A level 7 device could still interrupt because it does not monitor request lines.

2. Level 4 and 5 devices will not interrupt because they both are monitoring level 6.

This complex system is used for two reasons. It enables older software which only recognizes interrupt level 4 to be used. Also this scheme uses the least amount of ICs on the processor module.

There are two ways to use these request levels. There is a position independent configuration and a position dependent configuration. Figure 29 shows the position dependent configuration. This configuration is similar to the older serial method in that the module closest to the processor has the highest priority. As shown in Figure 29, the device in option location 1 has a higher priority than the device in location 2. This priority level continues all the way down the bus. The position dependent configuration does not limit you to four devices. It is possible to place more than one device on the same request line. Suppose two devices request an interrupt at the same time on level 6.

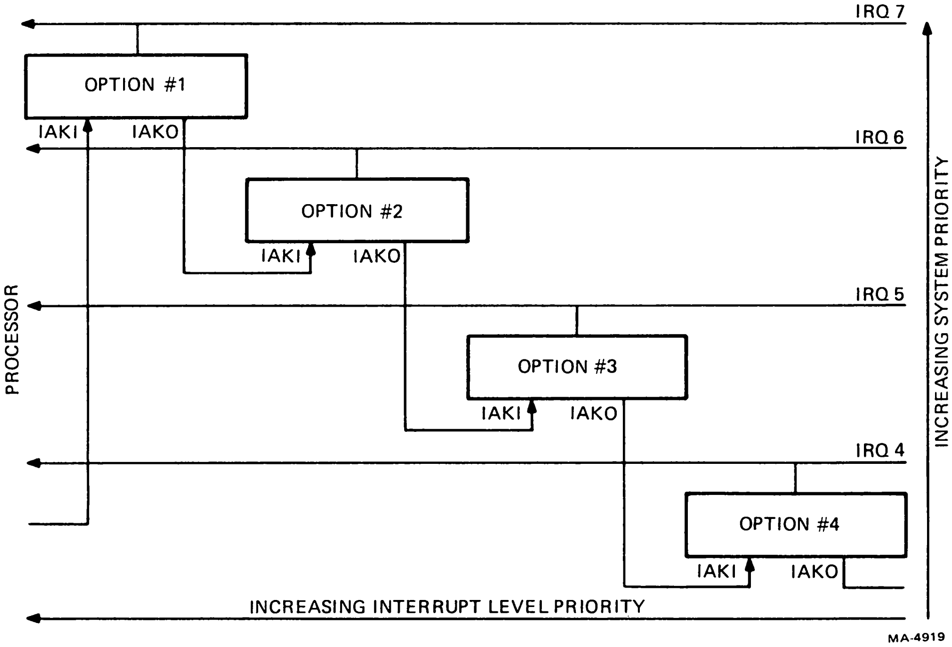


Figure 29. LSI-11/23 Position Dependent Modules

The device that is physically closer to the processor still has the highest priority. This is because the interrupt acknowledge signal is still daisy-chained through each device.

A typical example of a position independent configuration is shown in Figure 3Ø. In this particular example the device in option location 1 (closest to the processor) has the lowest priority because it is connected to request level 4. In this figure the order of priority from highest to lowest is:

- Option 2
- Option 4
- Option 3
- Option 1

As in the previous example, more than one device can be attached to a request level.

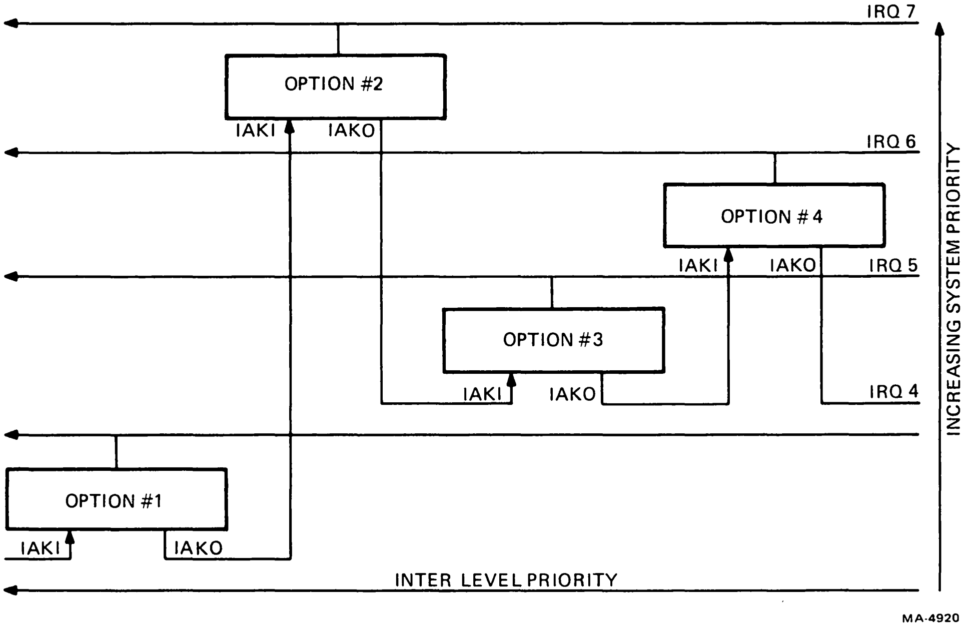


Figure 3Ø. LSI-11/23 Position Independent Modules

Summary

In this section we have discussed three types of data transfers: programmed data transfers, interrupts, and direct memory accesses. These items are compared in Table 2. We have also looked at the LSI-11 bus priority scheme which gives devices closest to the CPU the highest priority.

Table 2. Data Transfers

	Programmed Data Transfer	Interrupt	DMA
Speed	slowest	faster	fastest
Who can perform transfer	CPU only	most devices (except memory)	any DMA (high speed) device
When can transfer be done	when CPU becomes master	between instructions	between bus cycles
If CPU is halted	can not be done	can not be honored	can still be arbitrated

EXERCISE

Circle the letter corresponding to the correct response for each question/statement. You may use references. Check your answers with those given on the next page.

1. During programmed data transfer how many bus cycles can an instruction cycle have?

   a. one
   b. two
   c. more than two
   d. all the above

2. When an interrupt request is received by the CPU: the CPU will:

   a. send a grant signal
   b. send a vector address
   c. accept a vector address
   d. execute the ISR

3. When the bus master is performing a bus cycle during a DMA, the CPU will:

   a. send a grant signal
   b. wait for the DMA to complete
   c. execute an ISR
   d. continue executing its program

4. An interrupting device must wait for the grant signal before continuing with the interrupt.

   True ____
   False ____

5. For interrupts, the device closest to the CPU has the highest priority, while for DMAs the device furthest from the CPU has the highest priority.

   True ____
   False ____

SOLUTIONS

1. d

2. a

3. b

4. True

5. False

SPECIAL BUS FUNCTIONS

Special Functions

You will now learn about operations that take place on the LSI-11 bus, but are not used for data transfer. These operations are bus initialization, power-up/power-down sequence, and the processor halt mode. You will also learn about the remaining bus lines.

Bus Initialization

The bus can be initialized in one of two ways: by the CPU executing a RESET instruction or by going through a power-up or power-down sequence. The CPU initializes the bus by asserting the signal BINITL (bus initialize low) for 1Ø microseconds. This signal is used by devices along the bus to clear registers, reset circuits, and, in some cases, to initiate self test diagnostic programs.

Halt Mode

If the bus halt line, BHALTL, is asserted the CPU goes into the halt mode. Even though the CPU cannot execute a program in this mode, it still arbitrates DMAs and executes the microcode ODT. ODT (On-Line Debugging Technique) is the LSI-11's microcode console emulator.

BHALTL can be asserted by the console Halt switch. The BHALTL line can also be asserted by depressing the BREAK key on the console teleprinter, provided the proper jumpers are in place on the serial line unit.

Power-Up/Power-Down Sequence

The bus power-up sequence (Figure 31) allows for the automatic starting of a user's program when power is applied to the computer system. The power-down sequence (Figure 32) allows the CPU to execute a program which saves important data in the three milliseconds between the time the power failure is sensed and power supply voltages are lost.

In order to take advantage of the power-up/power-down sequence, the system must include some Read Only Memory (ROM), core memory, or MOS memory with battery backup. If none of these options are present all programs and data stored in memory are lost when power is removed.

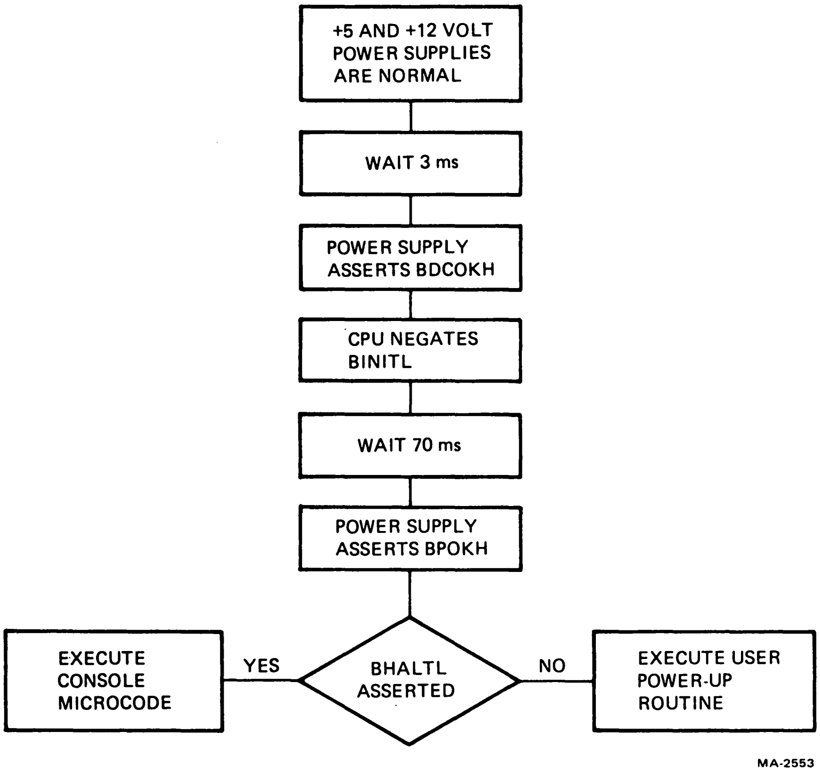

+5 AND +12 VOLT POWER SUPPLIES ARE NORMAL
WAIT 3 ms
POWER SUPPLY ASSERTS BDCOKH
CPU NEGATES BINITL
WAIT 70 ms
POWER SUPPLY ASSERTS BPOKH
BHALTL ASSERTED
YES
NO
EXECUTE CONSOLE MICROCODE
EXECUTE USER POWER-UP ROUTINE
MA-2553

Figure 31. The Power-Up Sequence Flowchart

As Figure 31 shows, when power supply voltages become normal, a three millisecond delay begins. At the end of this delay the power supply asserts BDCOKH (bus DC is OK high). The CPU responds by negating BINITL, which until now was held asserted from the time that power was applied. There is now a second time delay, lasting for 7Ø milliseconds, at the end of which the power supply asserts BPOKH (bus power OK high). The CPU now examines the BHALTL line. If it is asserted, the CPU executes the ODT microcode. If it is not asserted, a user-supplied power-up routine is started.

When the power supply senses a failure of the ac power, it negates BPOKH. This signals the CPU to execute a user-supplied power-down routine. Three milliseconds after BPOKH is negated, the CPU completes the sequence by asserting BINITL to initialize the bus (Figure 32).

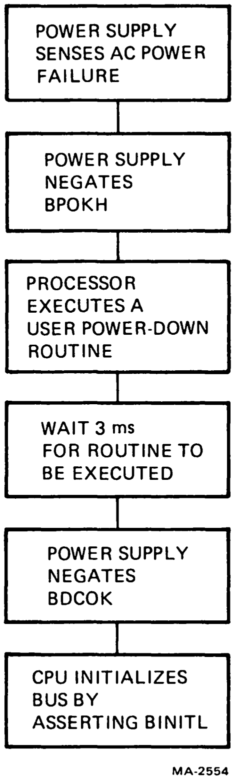

POWER SUPPLY SENSES AC POWER FAILURE
POWER SUPPLY NEGATES BPOKH
PROCESSOR EXECUTES A USER POWER-DOWN ROUTINE
WAIT 3 ms FOR ROUTINE TO BE EXECUTED
POWER SUPPLY NEGATES BDCOK
CPU INITIALIZES BUS BY ASSERTING BINITL
MA-2554

Figure 32. The Power-Down Sequence Flowchart

Miscellaneous Bus Lines

There are still two signals that have not been explained. The first is BREFL (bus refresh low). Semiconductor memories that are used with the LSI-11 must be periodically refreshed. Older-style memories had to be refreshed by an external device or by the CPU. BREFL is asserted to start the refresh process. Newer-style memories can perform an internal refresh and no longer use this line. The topic of Memory Refresh will be included in your Systems Course when you learn about semiconductor memories.

The second signal is BEVNTL (bus event low). This signal is used to note the occurrence of a selected event. When BEVNTL is asserted, the processor automatically services this interrupt request through a vector address found in location 1ØØ (octal). No vector address is transferred as happens in the normal interrupt. This line is usually used for the line time clock option which uses the power line frequency (5Ø or 6Ø Hz) to measure time intervals.

EXERCISE

Indicate whether the following statements are true or false by checking either column. You may use references. Check your answers with those given on the next page.

True **False**

1. Every time a RESET instruction is executed, an initialization pulse is sent down the LSI-11 bus. ____ ____

2. After BHALTL is asserted, the CPU can still arbitrate DMAs. ____ ____

3. During a power-up and power-down sequence, the user must supply the routine that is executed. ____ ____

4. The signals BPOKH and BDCOKH are the only two high asserted signals on the LSI-11 bus. ____ ____

5. The signal BEVNTL is used to refresh semiconductor memories. ____ ____

SOLUTIONS

1. True

2. True

3. True

4. True

5. False

This completes the course module for the LSI-11/23 bus concepts. Review the material covered and when you are ready, ask the Course Administrator for the module test.

APPENDIX A

SIMPLIFIED LIST OF LSI-11 BUS SIGNALS

Signal	Name	Function
BDALØL thru BDAL17L	Data and Address Lines	These 16 lines carry addresses and data during a portion of the bus cycle.
BBS7L	Bank 7 Select	The address that is currently on the address lines is between 124K and 128K(11/23)
BSYNCL	Synchronize	Asserted by the bus master to indicate it has put an address on the bus.
BDINL	Data In	1. During a bus cycle, it tells the slave to send data. 2. During an interrupt, it signals to all bus devices that an interrupt is taking place.
BRPLYL	Reply	Asserted by the slave to indicate that it has accepted data or placed data on the bus.
BDOUTL	Data Out	When asserted, tells the slave that data is on the bus.
BWTBT	Write Byte	When asserted, indicates that a write or a byte bus cycle is taking place.
BIRQ4L thru BIRQ7L	Interrupt Request	When asserted, indicates that some device on the bus wishes to interrupt.
BIAKIL/ BIAKOL	Interrupt Acknowledge In/Interrupt Acknowledge Out	Interrupt grant signal. Must be captured by interrupting device.
BDMRL	DMA Request	Indicates that some device on the bus wishes to do a DMA.

Signal	Name	Function
BDMGIL/ BDMGOL	DMA Grant In/ DMA Grant Out	DMA grant signal. Must be captured by device doing DMA.
BSACKL	Selection Acknowledge	During DMA, sent by device to indicate that it is bus master.
BDCOKH	Direct Current OK	Asserted only when dc power is OK.
BPOKH	Power OK	Asserted only when ac power is OK.
BHALTL	Halt	When asserted, CPU halts. Interrupts are ignored while DMAs are still arbitrated.
BINITL	Initialize	A 1Ø-microsecond pulse that resets I/O devices.
BEVNTL	External event Interrupt	Causes an automatic interrupt to location 1ØØ.
BREFL	Refresh	Used to refresh semiconductor memories.

PDP-11V23/11T23 SYSTEM MAINTENANCE

BA11-N MOUNTING BOX

BA11-N Mounting Box

INTRODUCTION

The BA11-N is a mounting box enclosure. It can house a PDP-11/23 CPU or be used as an expansion box. This course module will provide you with the information needed to:

- Remove and replace FRUs contained in the BA11-N.

- Make electrical adjustments to the power supply FRU.

- Properly configure a system containing one, two or three mounting boxes in accordance with prescribed DMA and interrupt grant priority schemes.

OBJECTIVES

1. Using a terminal tool kit and written procedures, remove and replace the logic assembly, ac input box and/or the power supply assembly.

2. Identify the basic variations of the BA11-N.

3. Adjust the H786 power supply voltages to within specifications using a voltmeter.

4. From a list of LSI-11 bus option circuit cards, indicate their proper placement in the BA11-N backplane according to a prescribed DMA and interrupt grant priority scheme.

SAMPLE TEST ITEMS

1. The required input voltage for the BA11-ND/NF is:

   a. 23Ø Vac
   b. +5 Vdc
   c. +12 Vdc
   d. 115 Vac

2. The H786 power supply's +5 Vdc output has a tolerance of ________ .

3. Remove and replace the H4Ø3-A ac input box to the satisfaction of the Course Administrator.

4. Of the following option modules, which should occupy the first slot in the BA11-N backplane?

   a. KD11-F
   b. MSV11-CD
   c. BDV11-AA
   d. DLV11-F

RESOURCES

BA11-N Mounting Box Technical Manual   EK-BA11N-TM-ØØ1

OVERVIEW

The BA11-N mounting box can be installed in a standard 48.3 cm (19 in) equipment rack. It contains cooling fans, ac input unit, power supply, and a 9-slot backplane that accept double-height and quad-height modules. The BA11-NE and NF have a blank front panel. The BA11-NC and ND have a bezel that is equipped with operating switches and status indicators. Figures 1 and 2 show the BA11-N with a bezel and a blank panel, respectively.

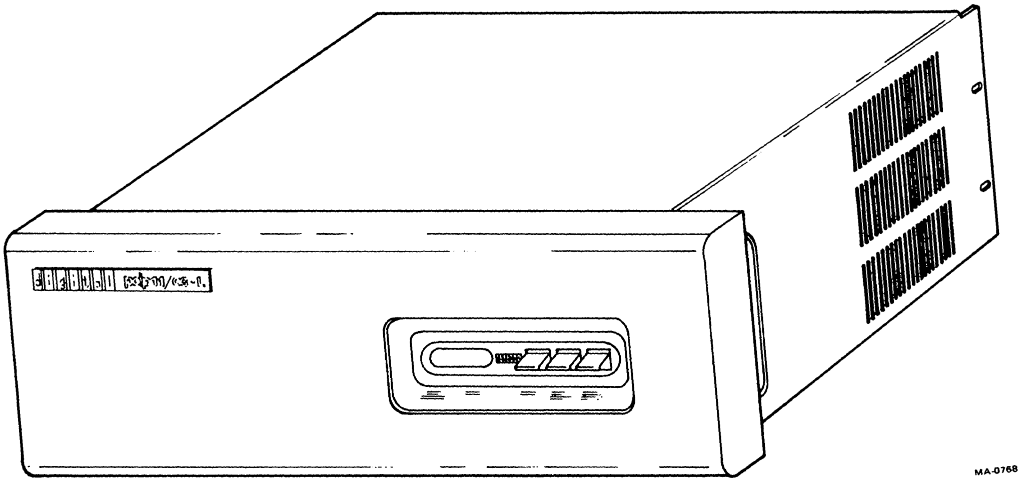


Figure 1. BA11-N with Front Bezel

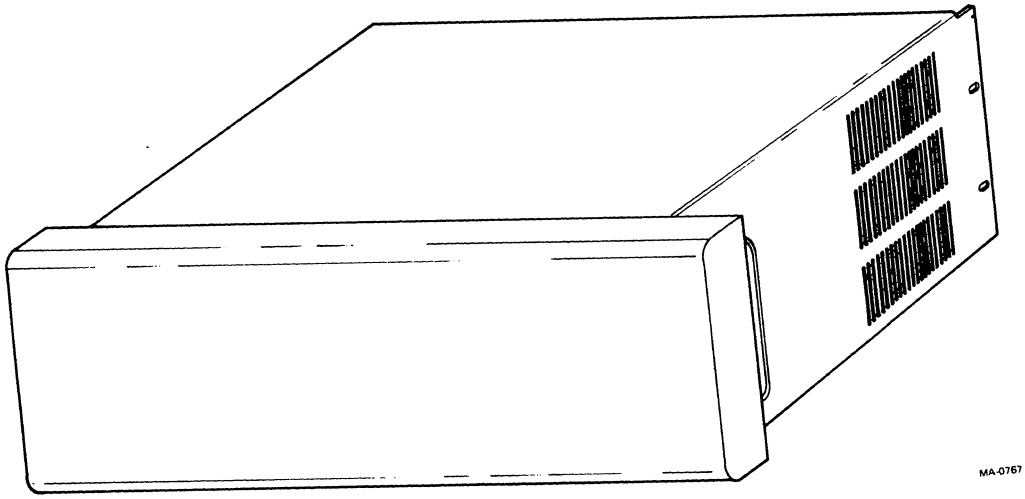


Figure 2. BA11-N with Blank Front Panel

The mounting box is available for both 115 V and 230 V systems. Because a choice of front panels is also provided, the user can select any of the following BA11-N models.

Model	**Primary Power/Front Panel**
BA11-NC	115 V/bezel panel
BA11-ND	230 V/bezel panel
BA11-NE	115 V/blank panel
BA11-NF	230 V/blank panel

Figure 3 shows the BA11-N with the logic box cover removed. The ac input box, power supply, and H9273 logic assembly (which includes the fans and the backplane) are attached to the logic box base; the bezel is attached to the power supply. The power supply assembly is hinged to the base and can be swung open to expose the internal components. Modules are inserted in the backplane from the rear of the box through an access door. This door is equipped with strain reliefs for the cables (Figure 4).

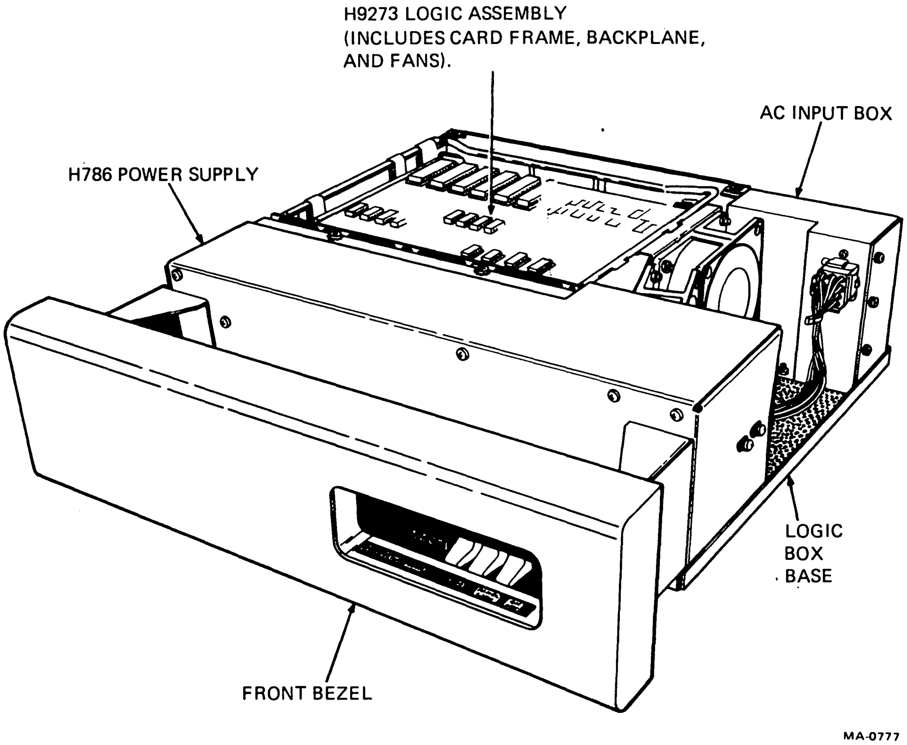


Figure 3. BA11-N, Logic Box Cover Removed

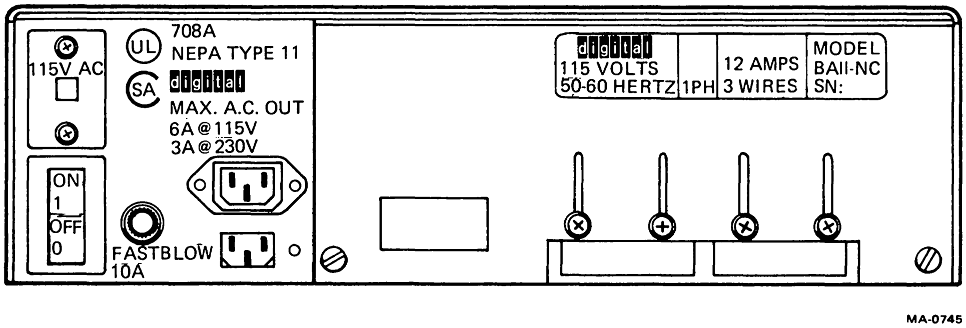


Figure 4. BA11-N, Rear View

When the unit is to be rack mounted, the logic box cover is attached to the rack with mounting hardware. The base of the logic box slides into the cover. Then a spring-button assembly engages, preventing the base from being pulled out of the cover accidentally.

Tables 1 and 2 list significant BA11-N mounting box specifications.

Table 1. BA11-N Specifications

Item	Specification
Dimensions (including bezel)	
Width	48.3 cm (19 in.)
Height	13.2 cm (5.19 in.)
Depth (without mounting brackets)	57.8 cm (22.75 in.)
Depth (with mounting brackets)	67.96 cm (26.75 in.)
Weight (without modules)	2Ø kg (44 lb)
Operating Temperature	5° C-5Ø° C (41° F-122° F)
Input Voltage	115 Vac (BA11-NC/NE), 23Ø Vac (BA11-ND/NF)
Input Current	12 A, Max (BA11-NC/NE), 6 A, Max (BA11-ND/NF)
Circuit Breaker Rating	15 A @ 115 Vac or @ 23Ø Vac

Table 2. BA11-N Power Supply Specifications

(H786 Power Supply)

Item	Specification
Current Rating	5.5 A @ 115 Vrms 2.7 A @ 230 Vrms
Inrush Current	100 A, peak, for 1/2 cycle at 128 Vrms or 256 Vrms
Apparent Power	630 VA
Power Factor	The ratio of input power to apparent power shall be greater than 0.6 at full load and low input voltage.
Output Power	+5 Vdc ± 250 mV @ 22A (A minimum of 2A of +5 Vdc power must be drawn to ensure that the +12 Vdc supply regulates properly; however, the +12 Vdc output will not go above 12.6 Vdc no matter what +5 Vdc current is drawn). +12 Vdc ± 600 mV @ 11 A
Power Up/Power Down Characteristics	
Static Performance	
Power Up	BDCOK H goes high: @ 75 Vac BPOK H goes high: @ 90 Vac
Power Down	BPOK H goes low: @ 80 Vac BDCOK H goes low: @ 75 Vac

EXERCISE

Select the answer which best completes the given statement by circling the corresponding letter. Check your answers with those given on the next page.

1. Which of the following statements best describes the Model BA11-NE mounting box?

    a. 115 Vac/bezel panel
    b. 230 Vac/bezel panel
    c. 115 Vac/blank panel
    d. 230 Vac/blank panel

2. The BA11-N's power supply provides which of the following output voltages?

    a. +5 Vdc and -12 Vdc
    b. ±5 Vdc and ±12 Vdc
    c. -5 Vdc and +12 Vdc
    d. +5 Vdc and +12 Vdc

SOLUTIONS

1. c

2. d

PHYSICAL/FUNCTIONAL DESCRIPTION

The BA11-N system comprises an ac input box (H4Ø3-A), a power supply (H786), a backplane, a bezel assembly with switches and indicators (a blank bezel is available), and two fans that provide air circulation around the printed circuit boards. Figure 5, which shows the BA11-N with its cover removed, locates the major components. The backplane and fans, as well as the card frame assembly, are part of the H9273 logic assembly. Figure 6 is a block diagram of the BA11-N electronics.

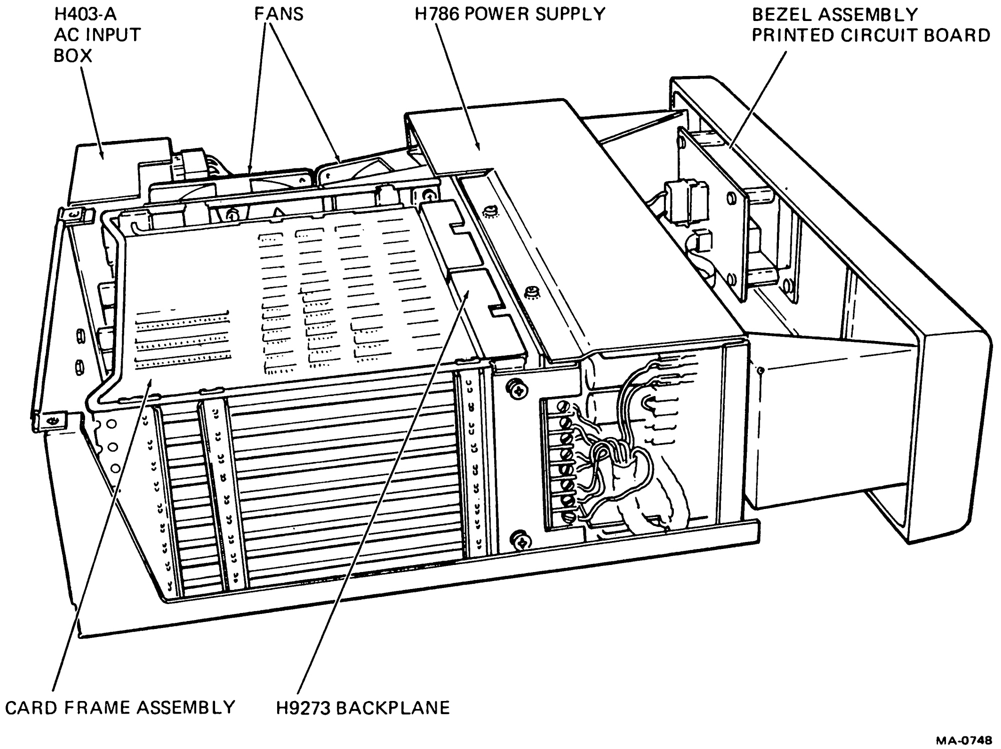


Figure 5. BA11-N Major Assemblies

AC Input Box (H4Ø3-A)

The ac input box is mounted in the rear of the logic box base and is bolted to both the logic box base and the door assembly. Power is supplied to the box from the power source by either a 115 V line cord or a 23Ø V line cord.

The box contains ac input and output receptacles, a circuit breaker, a line fuse, a line filter, and a switch for changing from 115 Vac to 23Ø Vac line voltages.

The output of the box is taken to the fans and the power supply by an ac power harness.

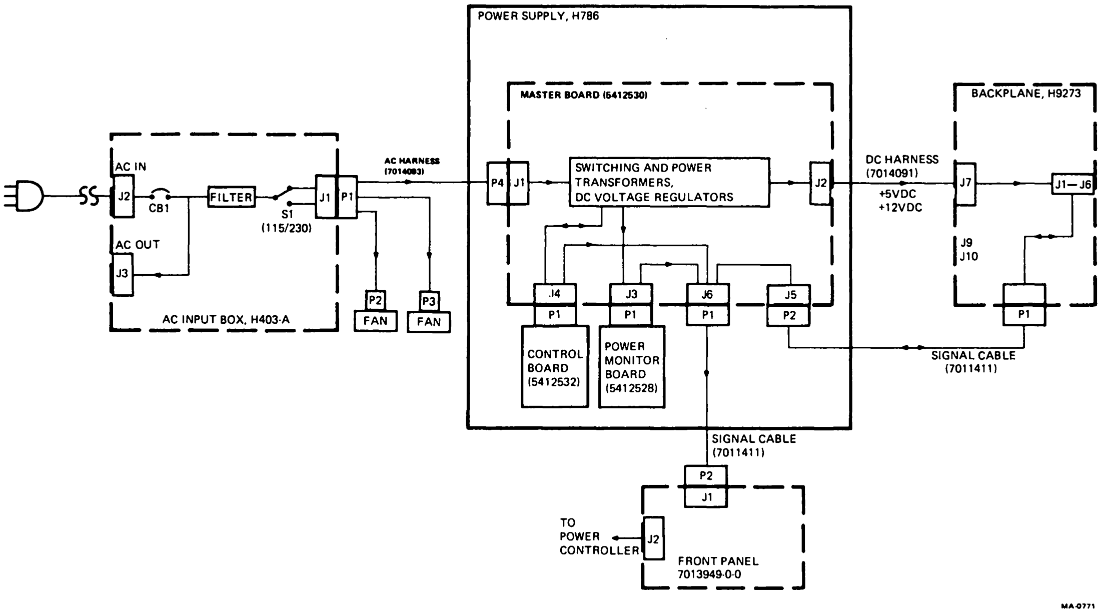


Figure 6. BA11-N Functional Block Diagram

H786 Power Supply

The power supply is mounted on the front of the logic box base. It is fastened to the logic assembly with two screws and held to the logic box base by two hinges. When the two screws are removed from the logic assembly, the entire assembly can be swung open on the hinges, exposing the printed circuit boards mounted within. The assembly can be removed easily by unscrewing the screws, unfastening the hinges, and disconnecting a maximum of four cables (three, if a blank front panel is used).

Three printed circuit boards contain all of the power supply components. The control board and the power monitor board are inserted in connectors that are mounted on the master board. The regulated dc voltages generated on the master board are applied to the H9273 backplane by a dc harness connected at both ends with screw terminals. The signals generated on the control board are carried to the backplane and front panel by two different signal cables.

Front Bezel

The BA11-N expander box is supplied with a blank bezel. The BA11-N mounting box is equipped with the operator control panel shown in Figure 7. The switches permit an operator to turn the power on and off, to restart the CPU, and to halt program execution. The indicators, when lighted, tell the operator that the power supply voltages are adequate for operation and the CPU is running. The front panel is connected to the power supply master board by a signal cable and, if applicable, to a power controller by a twisted-pair cable that can be supplied. Table 3 lists their functions.

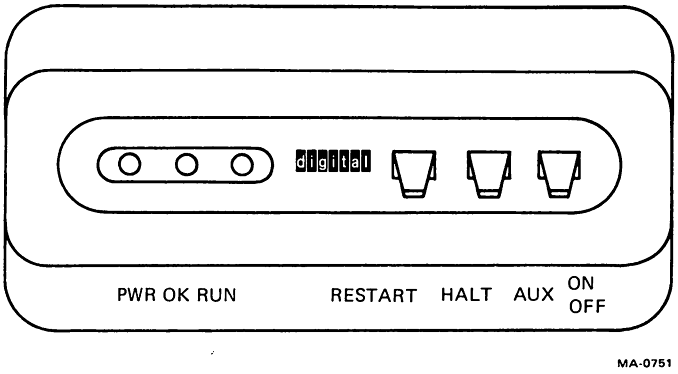


Figure 7. Front Panel Switches and Indicators

Table 3. BA11-N Front Panel Switches and Indicators

Switch	Indicator	Function
Aux On/Off		Can be used for any desired function (switch is rated at 48 V, 1 A dc). Two specific functions are: If the BA11-N is wired to control system power, the Aux switch turns the power on and off; if the BA11-N is not wired to control system power, the switch can control the LTC signal, disabling the signal when the switch is in the OFF position.
Halt		In the down position, the Halt switch forces the cpu to suspend normal program execution, enables console odt microcode operation, and permits single-instruction execution. to resume program execution, return the Halt switch to the up position and enter a P command from the console terminal (ODT microcode will be covered in a later course module). In an expander box, the Halt switch can be used to light the RUN indicator.
Restart		When the momentary Restart switch is activated, the CPU automatically carries out a power-up sequence; thus, the CPU can be rebooted at any time from the front panel.
	PWR OK	The PWR OK indicator lights when the power supply dc voltages are present.
	RUN	The RUN indicator lights when the CPU is executing programs.

H9273 Backplane

The BA11-N backplane is an H9273 four section by 9 slot backplane that accepts both double-height and quad-height modules. The backplane provides two distinct buses, the LSI-11 bus and the CD bus. The locations of these two buses are shown in Figure 8. Modules are inserted in rows 1 through 9 of the backplane. The LSI-11 bus signals appear on slots A and B; the CD bus signals appear on slots C and D.

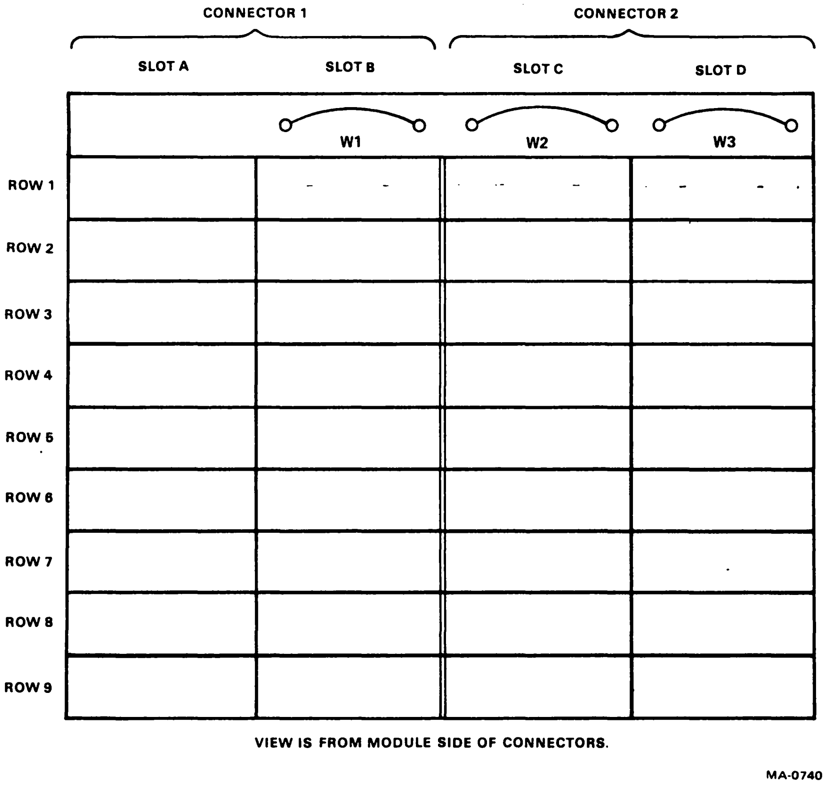
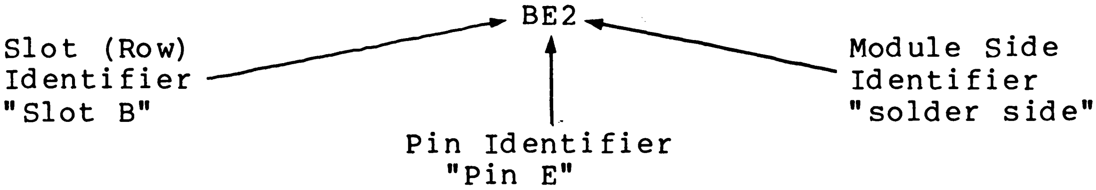


Figure 8. H9273 Backplane Connectors

Before continuing the discussion of the LSI-11 and CD buses, a look at module contact pin assignments is in order.

All modules intended for use with the BA11-N use the standard DIGITAL PDP-11 contact finger (pin) identification system. The LSI-11 bus is based on the use of double-height modules. These modules plug into the A and B connectors of the backplane. Each connector contains 36 lines, 18 on the component side of the circuit board and 18 on the solder side. Most quad-height modules use only slots A and B for interface purposes.

Slots, shown as ROW A and ROW B in Figure 9, include a numeric identifier for the side of the module. The component side is designated side "1" and the solder side is designated side "2." Letters ranging from A through V, excluding G, I, O, and Q, identify a particular pin on a side of a slot. A typical pin is designated as:


BE2

Slot (Row)
Identifier
"Slot B"

Module Side
Identifier
"solder side"

Pin Identifier
"Pin E"

Note that the positioning notch between the two rows of pins mates with a protrusion on the connector block for correct module positioning.

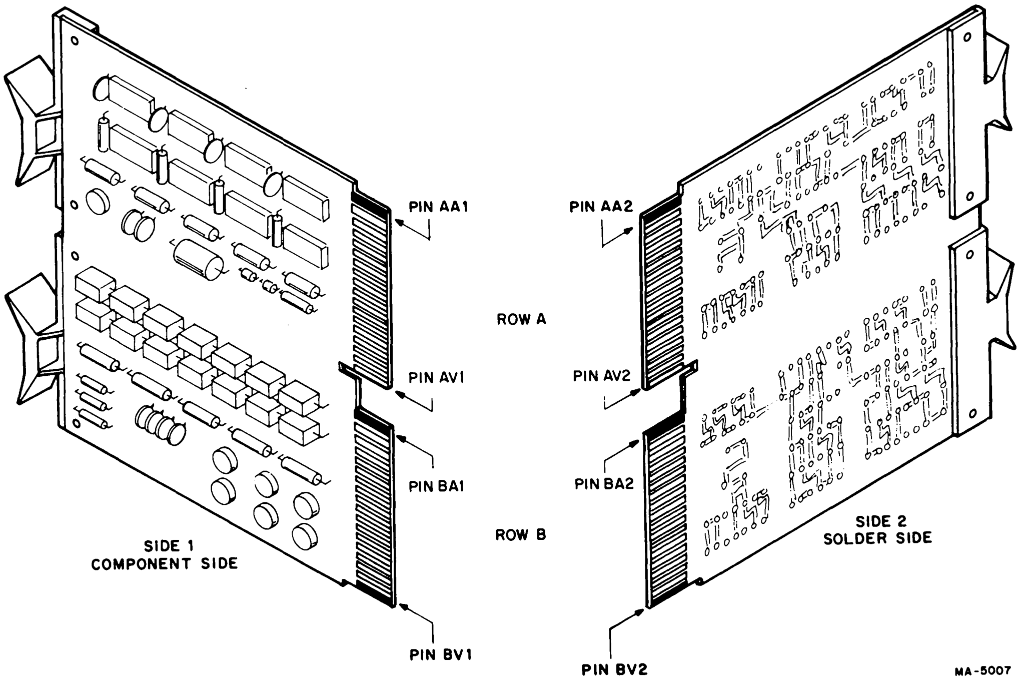


Figure 9. Double-Height Module Contact Finger Identification

Quad-height modules are numbered in the same way as double-height modules (Figure 1Ø).

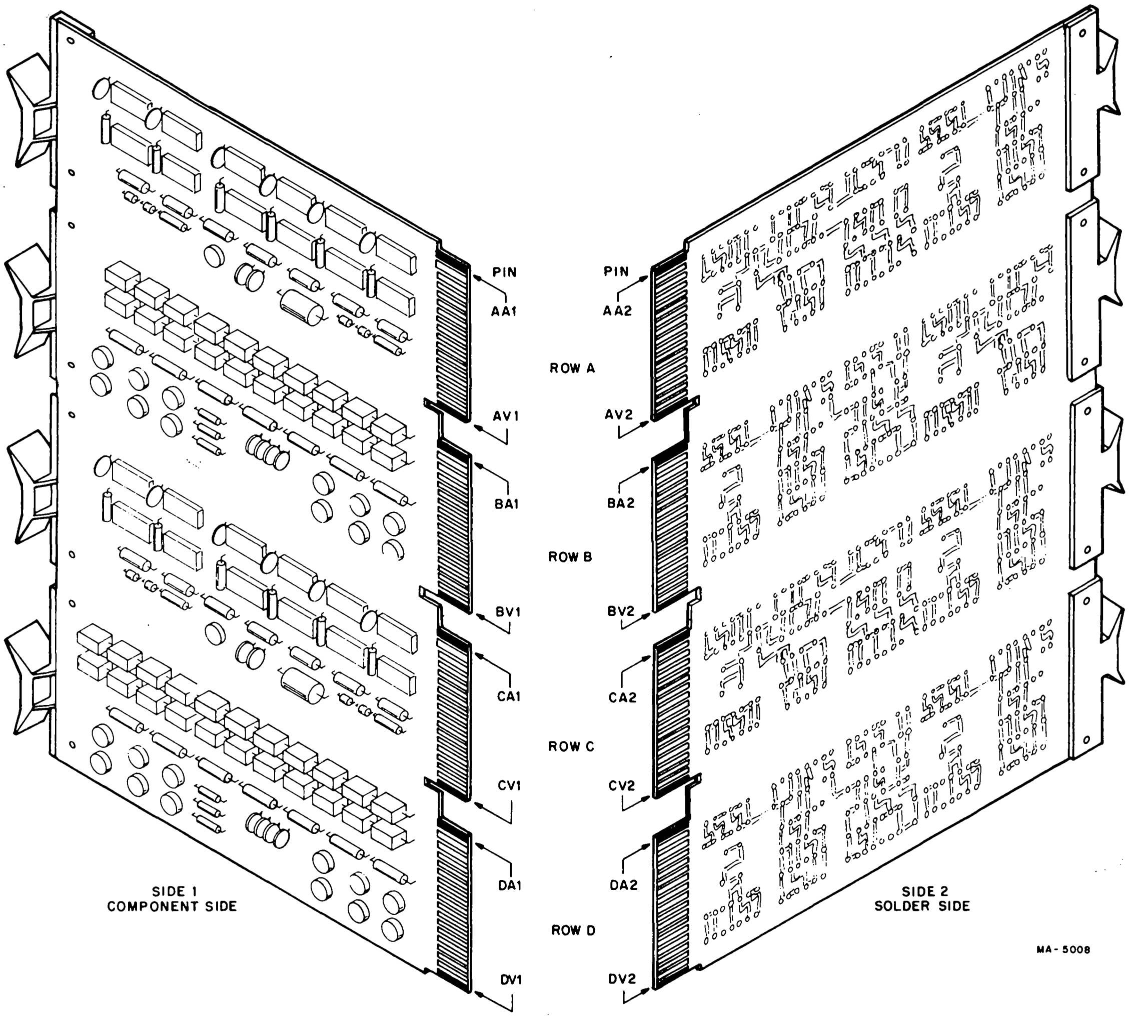


Figure 1Ø. Quad Module Contact Finger Identification

LSI-11 Bus Signals

The LSI-11 bus signals in the H9273 backplane are supplied by slots A and B. Most of these signals are bused to the same pin in all nine rows of the backplane. Certain designated spare pins are not bused. Likewise, interrupt acknowledge and bus grant signals (BIAKO L, BIAKI L, BDMGO L, and BDMGI L) are not bused. They are connected, instead, as shown in Figure 11. The interrupt acknowledge and bus grant signals are passed from module to module by etch jumpers that connect pin M2 to pin N2 and pin R2 to pin S2 on connector A of the module; hence, there can be no empty module positions between the CPU (which occupies row 1) and an I/O device option that uses these signals.

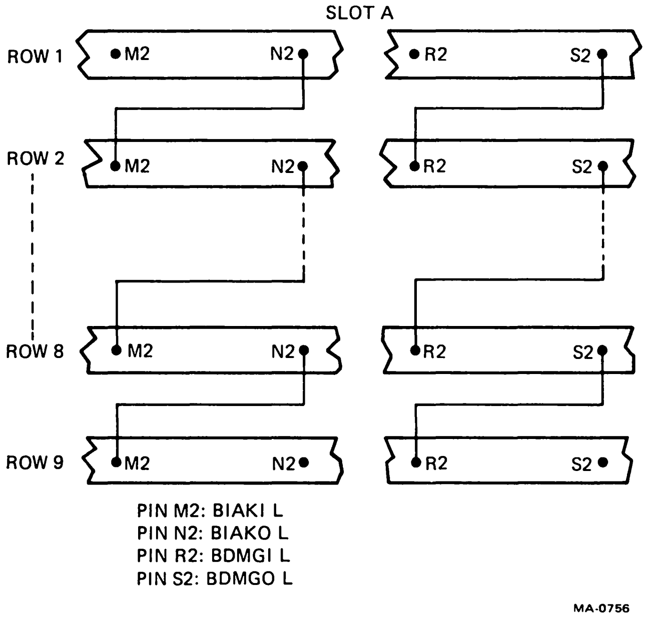
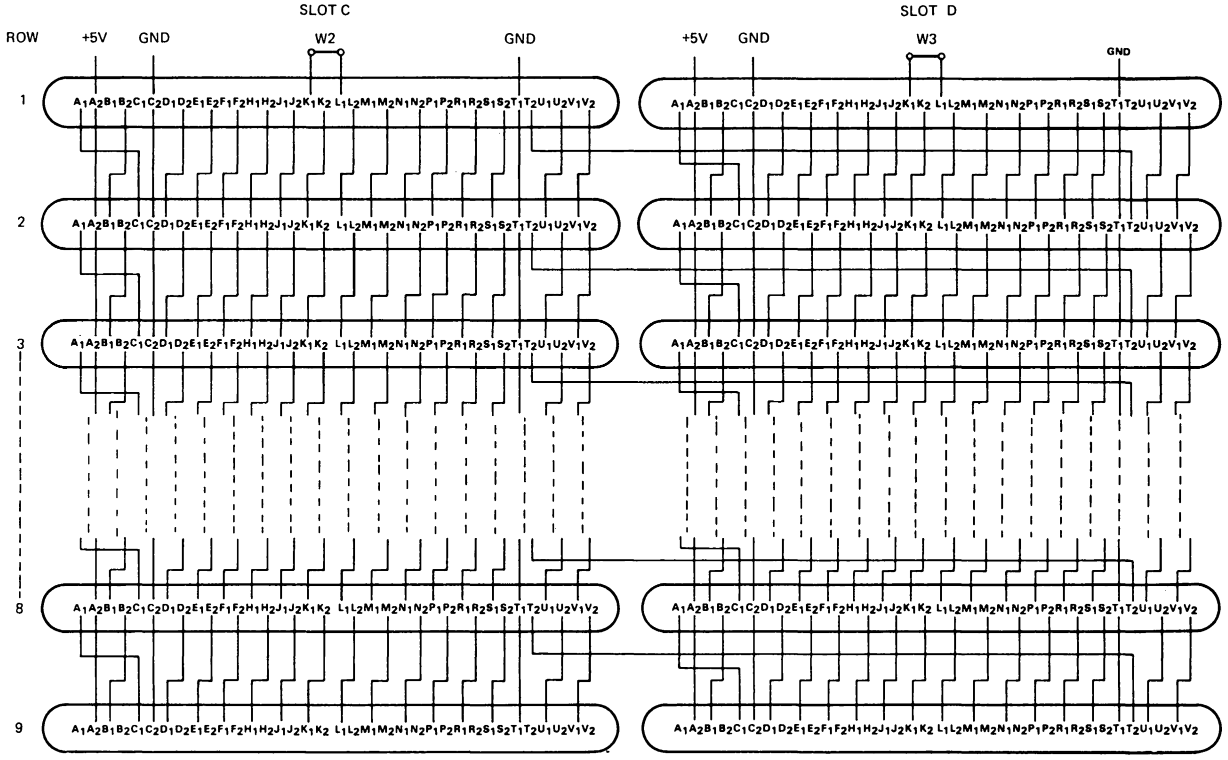


Figure 11. Interrupt/Acknowledge and Bus Grant Signal Interconnection, H9273 Backplane

If the LSI-11 bus is to be continued to a second backplane, a cable must connect slot A and B of row 9 in the first backplane to slot A and B of row 1 in the second backplane. Multiple backplane configurations will be discussed later in this module. A bus terminator module must be inserted in row 9 of the last backplane.

CD Bus Signals

The CD bus connections are shown in Figure 12. The +5 V supply voltage is bused to all rows on pin A2 of slots C and D (Example, pins CA2 and DA2). Ground connections on pins CC2, CT1, DC2 and DT1 are bused to all rows (Figure 12).


SLOT C
SLOT D
ROW
+5V
GND
W2
GND
+5V
GND
W3
GND
1
2
3
8
9
A1A2B1B2C1C2D1D2E1E2F1F2H1H2J1J2K1K2 L1L2M1M2N1N2P1P2R1R2S1S2T1T2U1U2V1V2
MA-0769

NOTE:
W2 AND W3 ENABLE THE LSI-11 CPU TO OPERATE IN ROW 1. IF THE BACKPLANE IS BEING USED AS AN EXTENDED BUS, REMOVE THE JUMPERS (THE CPU MUST BE PLACE IN ROW 1 OF THE MAIN BOX, ONLY).

Figure 12. CD Bus Interconnection

SOLUTIONS

1. b

2. d

3. b

All other pins connect only to an adjacent row. That is, all pins on the solder side of the board in Row 1 connect to corresponding pins on the component side of the board in Row 2. The solder side pins of the Row 2 board connect to corresponding pins of the component side of the board in Row 3 and so forth. For example, pin CF2 of any row connects only to pin CF1 of the adjacent higher numbered board. This scheme holds true with several exceptions. The first exception is the +5 V and ground lines which were discussed earlier. Two other exceptions are:

1. Pin CT2 connects to pin DT2 of the adjacent higher numbered row.

2. Pin CA1 connects to pin CC1 of the adjacent higher numbered row. (Refer to Figure 12.)

At this time, only the RLV11 RLØ1 Disk Drive Controller interface modules use the CD bus. The RLV11 option consists of two quad height boards (M8Ø13 and M8Ø14). The A and B slot connectors of both boards interface with the LSI-11 bus. The C and D slot connectors of the two boards use the CD bus for inter-board communications.

At this time, one quad height module cannot be used in this backplane. This module is the MMV11-A 4K by 16-bit core memory option. The module is limited to use in backplanes that contain the LSI-11 bus in both the A/B and the C/D slots.

NOTE

There are several LSI-11 bus modules which are not compatible with the 11/23 processor. This is due to software and addressing problems and not to the BA11-N backplane.

EXERCISE

Select the answer which best completes the statement. You will find the answers on the next page. You may use references.

1. The ________ is not a major assembly in the BA11-N Mounting Box.

   a. H786 power supply
   b. card frame
   c. bezel
   d. H4Ø3-A ac input box

2. In which slots of an H9273 backplane can the LSI-11 bus signals be found.

   a. A and C
   b. B and C
   c. D and A
   d. A and B

3. Which of the following is bused in the CD bus.

   a. BIAKI L
   b. +5 V
   c. +12 V
   d. BDMGO L

CONFIGURING

When configuring an 11/23 system using a BA11-N box, there are several items which must be taken into consideration. These are:

- Module placement
- Multiple BA11-N systems
- Power connections
- BA11-N jumper placement

Module Placement

When placing modules in the BA11-N, keep in mind that there is a definite scheme to be followed. A few general rules and guidelines are listed here. You should keep in mind that if your product line has any specific requirements other than those listed here, use them. The guidelines listed here will, however, usually be sufficient.

As you have learned earlier, the LSI-11 bus travels only down the A and B slots of the BA11-N. This means that any double-height modules which are placed in the BA11-N backplane will have to be placed in the A and B slots only. No double height modules can be placed in the C and D slots.

The CPU always goes in the very top location. Since the 11/23 processor is a double-height module, it will always be placed in the very top location, in the A and B slots.

Memory modules are always placed in the next available locations after the processor. If you are using memories such as the MSV11-D 32K word MOS memory which is mounted on a double-height board, this memory board will always be placed in the A and B slots.

The "interrupt" type devices should be placed in the locations immediately following the memories. Examples of interrupt type devices are the DLV11 series serial line units, the RXV11, RXØ1 interface, and the LAV11, LA18Ø interface. One thing that you should keep in mind while configuring your system is that the DLV11 which is controlling the console terminal should be placed in the first available location immediately after the memory.

Immediately after the interrupt devices, the "DMA" or high speed devices should be placed. Examples of DMA interfaces are the RXV21, RXØ2 interface, the RLV11, RLØ1 interface, and the RKV11, RKØ5 interface.

The very last slot in the backplane should hold the BDV11 bootstrap/terminator module. This module is ALWAYS placed in the last slot even if there are empty locations between the last occupied option location and the bootstrap/terminator board.

If you have more than one BA11-N box in your system, this will only slightly modify the method that you will use to place the module into the box. This information will be found in the next paragraph.

Multiple BA11-N Systems

Now that you are familiar with the general rules of module placement within the BA11-N mounting box, you are ready to determine exactly what hardware options are required to interconnect multiple backplane systems. LSI-11/23 systems can come with one, two, or three backplanes. Three backplanes is the largest DEC-approved system available. Figure 13 shows a three backplane system.

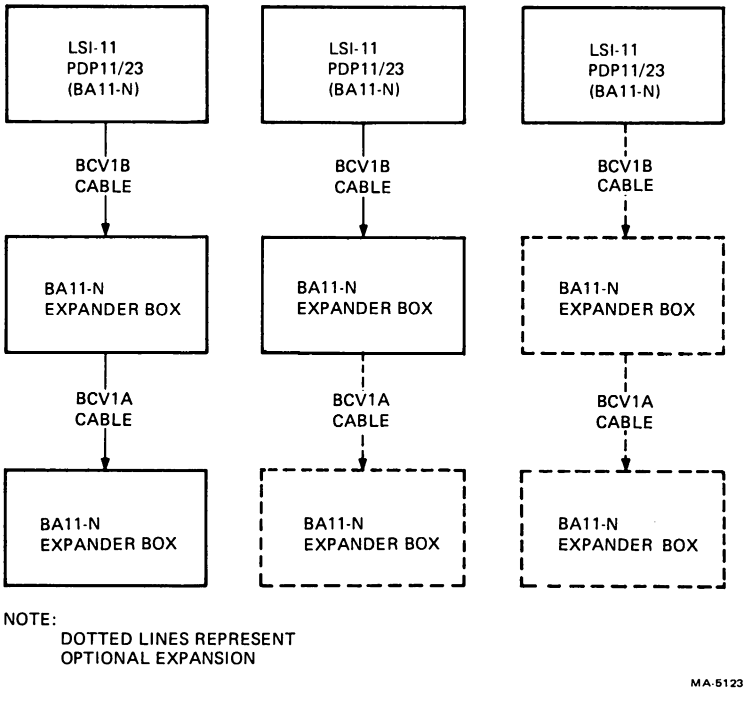


Figure 13. BA11-N System Application

In any multiple backplane system the first backplane will always be a BA11-NC or BA11-ND while the second and third backplane, if any, will be a BA11-NE or BA11-NF.

Two Backplane System

To connect a two backplane system a BCV1B-XX option is required. Figure 14 shows that the BCV1B-XX is composed of three parts, an M9400-YE bus terminator/connector module, two BC05L-XX cables, and an M9401 connector module. The XX in the option and cable designations refers to the length of the BC05L-XX cable. For example, if you are ordering a BCV1B with six feet of cable the designation becomes BCV1B-06. Figure 15 shows how to install the BCV1B.

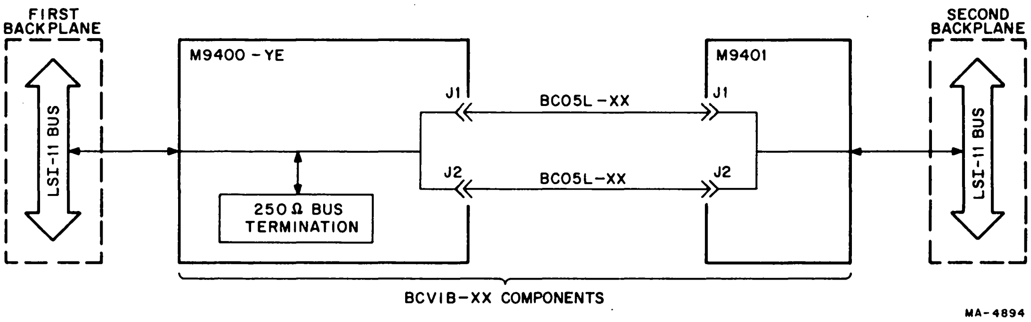


Figure 14. BCV1B-XX

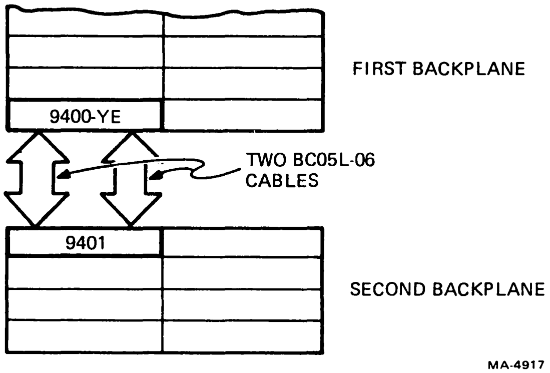


Figure 15. BCV1B Installation

Because of the bus grant priority scheme, the M9400-YE is inserted in the location usually reserved for the last option in the first backplane. The M9401 connector module is inserted into the highest priority position of the second backplane. The BCV1B is always used between the first and second backplane.

Three Backplane System

Configuring a three backplane system is similar to configuring a two backplane system. Chassis one and two are still connected by a BCV1B. Chassis two and three are connected by a BCV1A-XX.

Figure 16 shows that the BCV1A consists of an M94ØØ-YD connector module, two BCØ5L-XX cables, and an M94Ø1 connector module. Just as before, the XX represents the length of the BCØ5L cable. A BCV1A is always used between the second and third backplane.

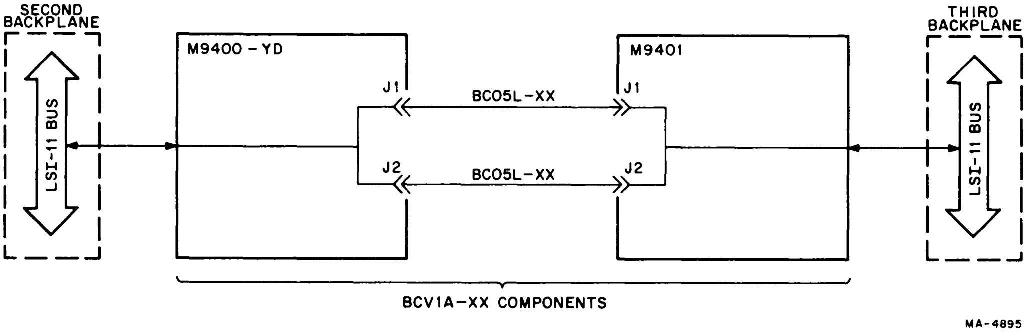


Figure 16. BCV1A-XX

Figure 17 shows the BCV1A connecting the last option position in chassis two with the first option position of chassis three.

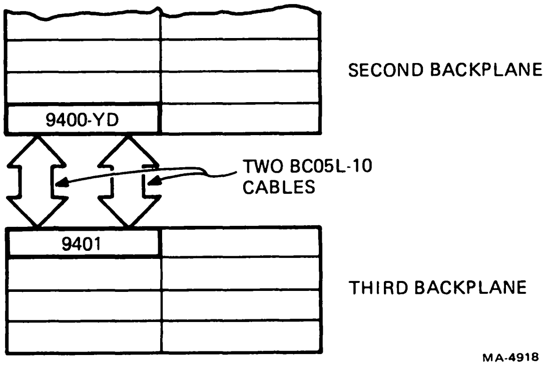


Figure 17. BCV1A Installation

On standard multiple backplane systems the cables used to connect the first backplane to the second backplane are BC05L-06 cables. The cables used to connect the second backplane to the third backplane are BC05L-10 cables. If you must use non-standard cables in your system, you should make sure that there is always a four-foot difference in the length of the cables between the first and second backplane and the second and third backplane. This is done to prevent the generation of undesired signals along the LSI-11 bus.

Power Connections

There are several different ways of connecting the BA11-N to a source of primary ac power as shown in Figure 18. Figure 18A shows a system where no power controller is used. This connection also uses a minimum number of line cords. Referring back to Figure 6, J2 is connected to J3 through a circuit breaker. Because of the current rating of the ac input box no more than two BA11-Ns may be operated from a single linecord.

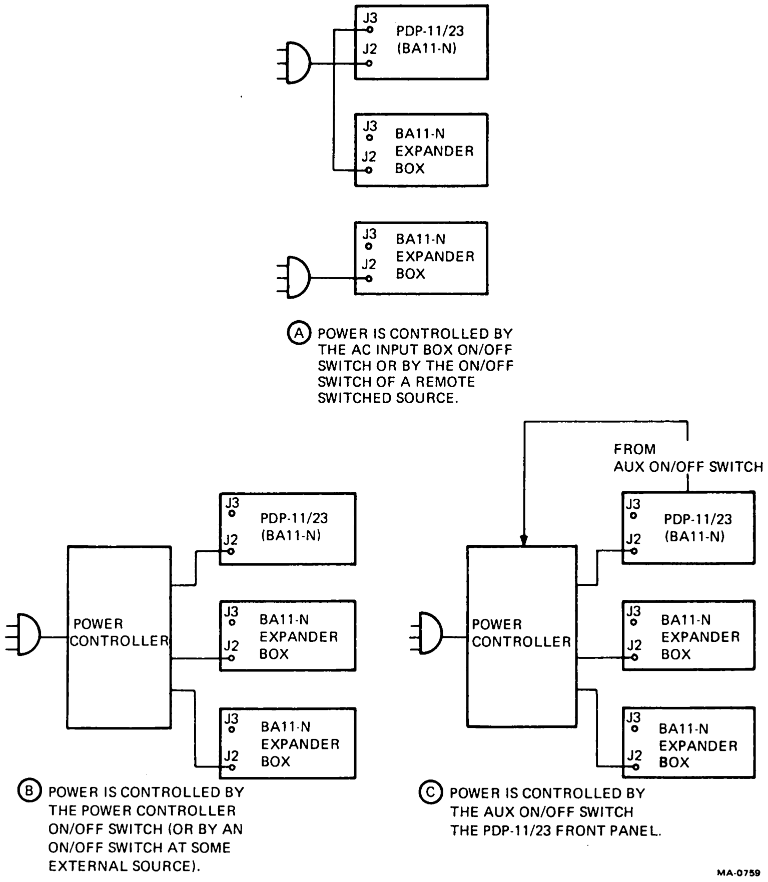

J3
J2
PDP-11/23 (BA11-N)
BA11-N EXPANDER BOX
BA11-N EXPANDER BOX
(A) POWER IS CONTROLLED BY THE AC INPUT BOX ON/OFF SWITCH OR BY THE ON/OFF SWITCH OF A REMOTE SWITCHED SOURCE.
POWER CONTROLLER
(B) POWER IS CONTROLLED BY THE POWER CONTROLLER ON/OFF SWITCH (OR BY AN ON/OFF SWITCH AT SOME EXTERNAL SOURCE).
FROM AUX ON/OFF SWITCH
(C) POWER IS CONTROLLED BY THE AUX ON/OFF SWITCH THE PDP-11/23 FRONT PANEL.
MA-0759

Figure 18. Power Connections, 11/23 Systems

When installing a system designed for 240 volts, 50 Hz, be sure that you order the proper linecords. The linecords that connect to the ac outlet are of the European type, while the linecord that connects the two BA11-N mounting boxes are still of the American type.

Figure 18B shows a system where three BA11-N mounting boxes get their ac supply from a power controller. Power is turned on and off by operating the power switch on the ac power controller. Figure 18C shows a similar connection. The only difference here is that the ac power is controlled by the Auxiliary On/Off switch on the bezel of the first BA11-N.

Figure 19 shows a typical 11V23 system. In this system power is turned on and off by operating the Auxiliary On/Off switch on the BA11-N mounting box. The remote power cable is connected to J1 of the power controller. Also the Remote On/Off switch is left in the Remote On position.

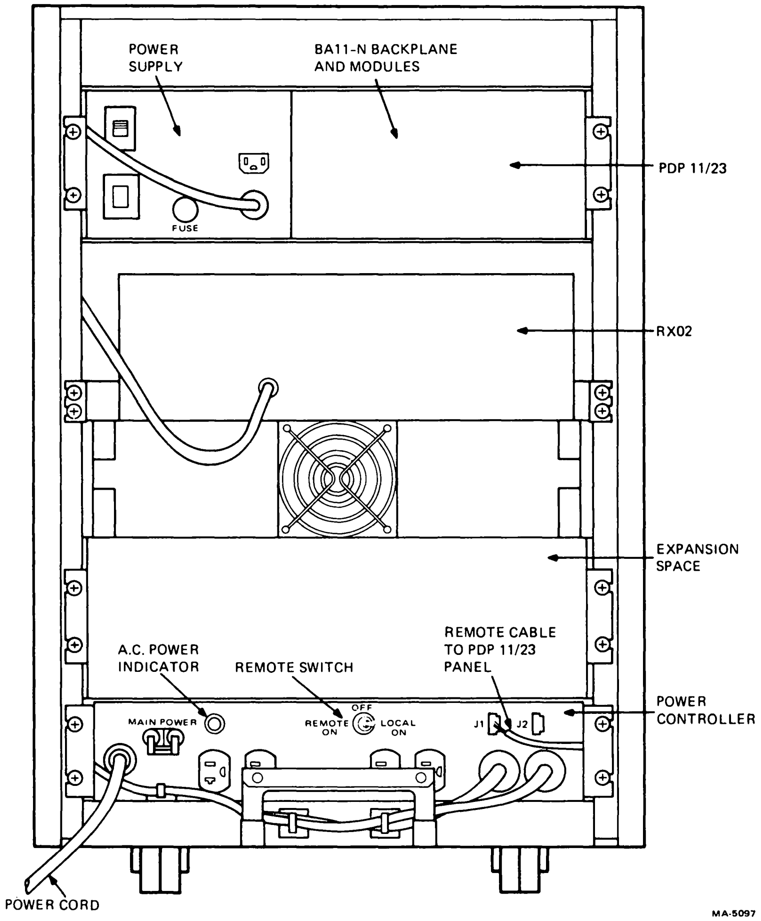


Figure 19. PDP-11V23 with Backpanel Removed

BA11-N Jumper Placement

There are seven jumpers located on the BA11-N mounting box. Three of them are located on the H9273 backplane; the remaining four jumpers are found on the printed circuit board directly behind the bezel.

Backplane Jumper Positions

The three jumpers located on the H9273 backplane are numbered W1, W2, and W3. Figure 2Ø shows the location of these jumpers. When the backplane is manufactured, all three of these jumpers are installed. Table 4 gives the function of each of these jumpers. Table 5 indicates when these jumpers should be installed and when they should be removed.

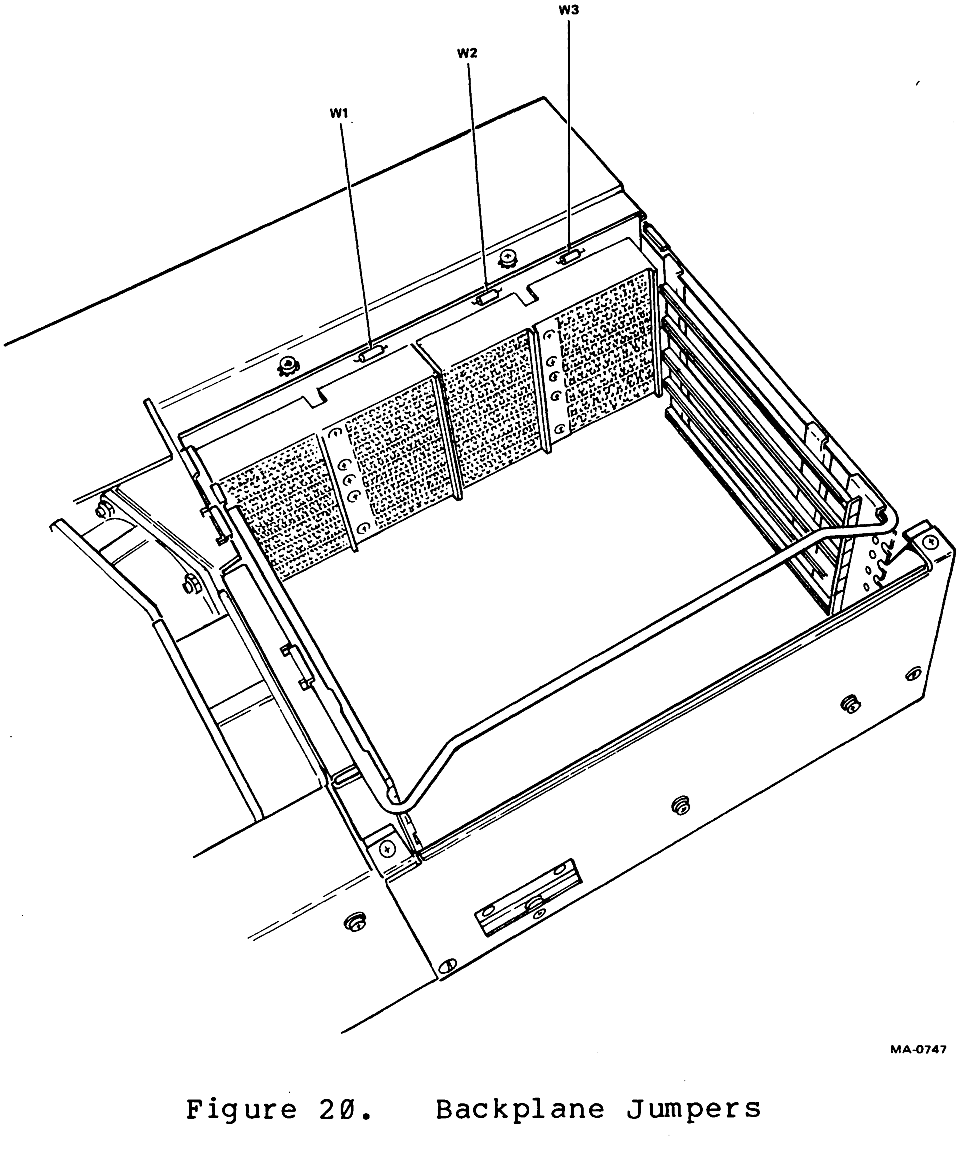


Figure 2Ø. Backplane Jumpers

Table 4. Backplane Jumpers

Jumper Position	Jumper(s) In	Jumper(s) Out
W1	When the H786 power supply generated LTC signal is used to assert the LSI-11 bus BEVNT L signal.	When it is not desired to have line time clock (LTC) sourcing BEVNT L, such as when an external source is used instead.
W2, W3	When a quad KDF11 CPU is inserted in row 1 of the backplane.	When any other module is installed in row 1, i.e., when the backplane is part of an expander box.

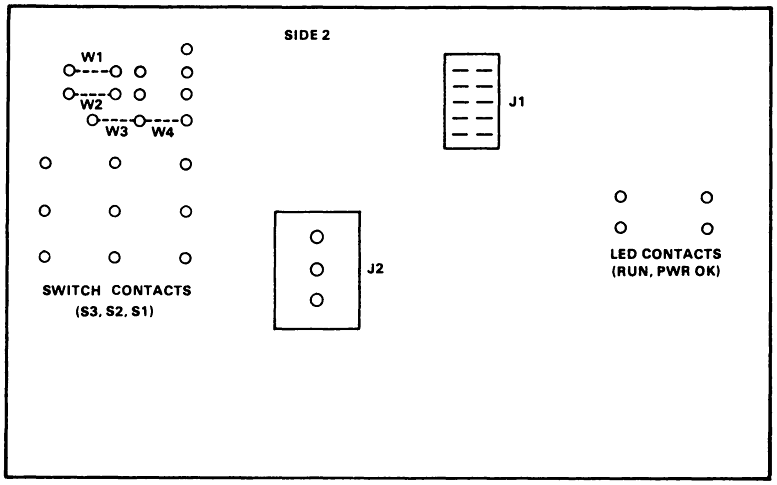
Table 5. Backplane Jumper Positions

BA11-N used as	W1	W2	W3
Mounting box	I	I	I
Expander box	I	R	R

I = Inserted
R = Removed

Bezel Assembly Jumper Positions

There are four jumper positions W1, W2, W3, and W4 on the printed circuit board behind the bezel assembly. The physical location of these jumpers is shown in Figure 21. When the printed circuit board is manufactured W1, W2, and W4 are in place, W3 is left blank. Table 6 lists the function of each of these jumpers. Table 7 indicates when these jumpers should be installed or removed.



NOTES:
1. VIEW IS FROM THE REAR OF THE BEZEL WHEN THE BOARD IS MOUNTED ON THE BEZEL.
2. JUMPERS ARE MOUNTED ON SIDE 1.

MA-0737

Figure 21. Bezel Printed Circuit Board

Table 6. Bezel Assembly Jumpers

Jumper Position	Jumper In	Jumper Out
W1, W2	When the bezel Aux On/Off switch is used to control the power supply generated LTC signal (when the switch is in the Aux On position, LTC-initiated interrupts are possible).	When the bezel Aux On/Off switch is used to turn the system power controller on and off.
W3	When the bezel is to be mounted on an expander box (W3 permits the Halt switch to light the RUN indicator).	When the bezel is part of the main box, i.e., the CPU is mounted in this bezel's backplane.
W4	When the bezel is part of the main box (W4 enables the S RUN L signal to light the RUN indicator).	When the bezel is mounted on an expander box.

Table 7. Bezel Assembly Jumper Positions

BA11-N used as	W1	W2	W3	W4
Mounting box	I	I	R	I
Expander box	I	I	I	R

EXERCISE

Select the answer which best completes the statement. You will find the answers on the next page. You may use references.

1. An LSI-11 system can include as many as ____ backplanes.

   a. 3
   b. 4
   c. 5
   d. 6

2. In a H9273 backplane, there are ________ jumpers.

   a. 2
   b. 3
   c. 5
   d. 7

3. In a properly configured LSI-11 system, which module should always occupy the top slot?

   a. Memory
   b. DMA interface
   c. Console interface
   d. Processor

SOLUTIONS

a. a

b. b

c. d

DISASSEMBLY

The BA11-N is made up of four major assemblies: the bezel assembly, the power supply assembly, the ac input box, and the H9273 backplane. These assemblies are designed to be quickly and easily removed.

Ask your Administrator for a tool kit and a BA11-N mounting box. Then perform the following exercise.

EXERCISE

All figures and paragraphs referenced in this exercise can be found in the BA11-N Mounting Box Technical Manual (EK-BA11N-TM-ØØ1). Clean off an area on your desk or workbench large enough to accommodate a BA11-N mounting box. Carefully perform the following procedures.

NOTE

While disassembling and/or reassembling the BA11-N follow these guidelines.

1. USE THE PROPER TOOL FOR THE JOB.
2. DO NOT DISCONNECT PLUGS BY YANKING ON CABLES.
3. FORCE NOTHING. If something does not come apart or go back together easily, DO NOT use force. Ask your Course Administrator for assistance.
4. USE COMMON SENSE.

Check off each step as it is performed.

READ

Read Paragraph 4.3 of the BA11-N Tech Manual.

___ 1. Remove the logic box base from the cabinet and place it on your work surface. Follow the procedures in Paragraph 4.3.1 of the Tech Manual.

NOTE

> Step 2 of Paragraph 4.3.1 warns that the twisted-pair cable can snag while you are pulling the base out. PDP-11V23 and PDP-11T23 are shipped with the cable attached to the base with a tie wrap. If you encounter such a system, cut the tie wrap off and don't replace it. Once the base is out, don't cut any more of the tie wraps.

___ 2. Remove the bezel assembly and power supply as a unit following the procedures in Paragraph 4.3.4 of the Tech Manual. When you have the unit removed, notice that the bezel assembly is held to the power supply by four screws at the mounting brackets. Do not bother disassembling the two assemblies. Just note how they are held together and set the unit out of the way while you continue disassembly.

___ 3. Remove the ac input box following the procedures in Paragraph 4.3.5 of the Tech Manual. When you have removed the unit, set it aside.

___ 4. Remove the H9273 logic assembly following the procedures in Paragraph 4.3.6 of the Tech Manual.

___ 5. Now that you have the BA11-N apart in front of you, put it back together again following the preceding procedures in reverse order.

All of the cable plugs are keyed and cannot be inserted backwards. DO NOT FORCE any connectors. Be especially careful when reinstalling the plugs on the ac fans. The pins are easily bent.

___ 6. Have your Course Administrator give the box a visual inspection prior to proceeding to the next section.

ADJUSTMENTS

There are two electrical adjustments in the BA11-N Mounting Box. One adjusts the +5 Vdc output voltage. The other adjusts the +12 Vdc output voltage.

EXERCISE

Ask your Course Administrator for a terminal tool kit and a PDP-11V23 or PDP-11T23 system.

READ

Proceed to Paragraph 4.2 of the BA11-N Mounting Box Technical Manual (EK-BA11N-TM-ØØ1).

Adjust the H786 +5 Vdc and +12 Vdc output voltage following the procedures in Paragraph 4.2. Measure the voltages at the tip jacks on the back edge of the M8Ø12 (BDV11-A) module.

You have now completed this course module. Ask your Course Administrator for the BA11-N Module Test.

PDP-11V23/11T23 SYSTEM MAINTENANCE

KDF11-AA PROCESSOR

KDF11-AA Processor

INTRODUCTION

The KDF11 processor module is the heart of both the 11V23 floppy-based system and the 11T23 hard-disk system. For you to effectively maintain any LSI-based system, it is not only necessary to know how to configure this module properly but also how to use the microcode ODT.

OBJECTIVES

1. Select from a list the major features of a KDF11.

2. Select from a list those functions of the processor module which can be altered by jumper selections.

3. Match the functions of the processor module with the jumpers that control those functions.

4. Describe the theory of operation of the KDF11 by recalling the principles of operation of:

   - Data chip
   - Control chip
   - Memory Management Unit (MMU) Chip
   - Data-Address Lines (DAL)
   - Micro Instruction Bus (MIB)
   - DMA control
   - Chip reset logic
   - Floating point processor (KEF11-A)

5. Examine a processor module and list the jumper settings for:

   - Event line enable
   - Power-up mode
   - Halt/trap option
   - Bootstrap starting address enable
   - Bootstrap starting address select

6. Remove and replace the MMU chip.

7. Using microcode ODT, load and run a program supplied by the Course Administrator.

8. Examine and modify the contents of memory and general purpose registers using microcode ODT.

SAMPLE TEST ITEMS

1. The hybrid ICs used in the KDF11 have ________ chips per package.

   a. one
   b. two
   c. three
   d. four

2. Which of the following features are jumper-selectable?

   a. power-up mode
   b. refresh enable
   c. reply to refresh
   d. ODT enable

3. Which statement about the control chip is true?

   a. It has 522 locations for microcode storage.
   b. It contains the ALU.
   c. It contains the general purpose registers.
   d. It holds the processor status word.

4. Ask your Administrator for a KDF11 processor module. Examine the jumpers and list the settings for:

   - Event line enable
   - Power-up mode
   - Halt/trap option
   - Bootstrap starting address enable
   - Bootstrap starting address select

5. Remove and replace the MMU chip.

6. Using microcode ODT, load and run a program supplied by the Course Administrator.

7. Enter the value 177777 into general purpose register 3.

OVERVIEW

The KDF11-AA microcomputer (Figure 1) is contained on one double-height board. The designation for this module is M8186. It contains eight high-speed, general-purpose registers which can be used as accumulators, address pointers, index registers, and for other specialized functions. The KDF11 controls an enhanced version of the LSI-11 bus. The new LSI-11 bus is compatible with the PDP-11/23's bus and has greatly increased interrupt handling and parity checking capabilities. The later feature is due to the ability of the new bus to communicate with an external parity controller.

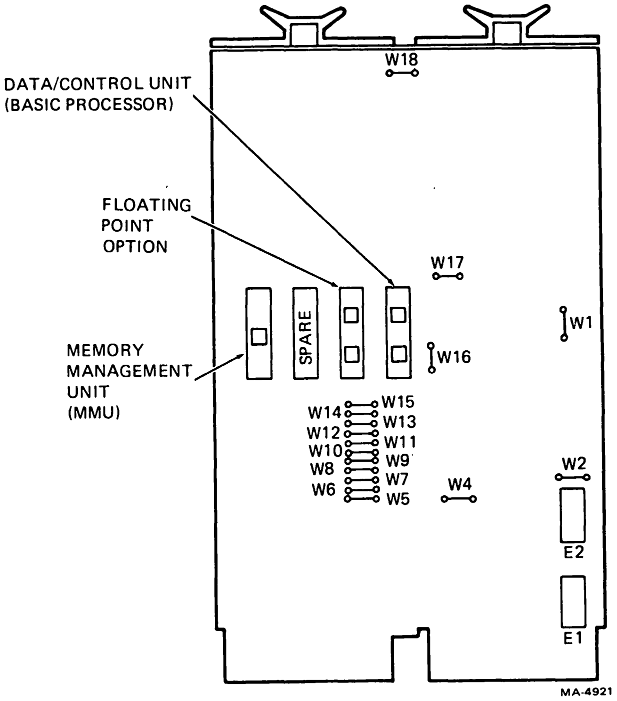


Figure 1. KDF11-AA Processor Module (M8186) with Optional Floating Point

The KDF11 is implemented using hybrid ICs (integrated circuits). A hybrid IC has more than one IC per package. The basic processor hybrid (Figure 1) consists of a data chip and a control chip mounted in a single 40-pin dual in-line package (DIP). The data chip contains the arithmetic and logic unit (ALU) and the general purpose registers, while the control chip contains the microcode ROM and the PDP-11 instruction decode logic.

The Memory Management Unit (MMU), shown on the far left side of Figure 1, allows memory to be extended to 124K, 16 bit words. With memory management, the I/O page occupies the addresses from 124K to 128K.

Using the optional floating point hybrid (Figure 1), the instruction set is expanded to include the same floating point instructions used by the PDP-11/34, 11/60, and 11/70.

There are three variations of the KDF11 processor:

- KDF11-AA processor with MMU
- KDF11-AB processor with MMU and floating point option (KEF11-A).
- KDF11-AC processor without MMU or KEF11-A.

A KDF11-AA or -AB module along with memory and a mounting box is called an LSI-11/23. An LSI-11/23 and RX02 disk is called an 11V23 system, while an LSI-11/23 and RL01 is called an 11T23 system.

The specifications for the KDF11 are listed in Table 1.

Table 1. KDF11 Specifications

Identification	M8186
Size	Double
Dimensions	13.34 cm X 21.59 cm (5.25 in X 8.5 in)
Power Requirements	+5 V ± 5%, 2.0 A +12 V ± 5%, 0.2 A
Bus Loads	ac 2 unit loads dc 1 unit load
Environmental	
Storage	40° C to 65° C (104° F to 149° F) 10% to 90% relative humidity, non-condensing
Operating	5° C to 60° C, (41° F to 140° F) Maximum outlet temperature rise of 5° C (9° F) above 60° C (140° F) Derate maximum temperature by 1° C (1.8° F) for each 305 m (1000 ft) above 2440 m (8000 ft). 10% to 90% relative humidity, non-condensing
Timing (Based on 3000 ns CPU microcycle time)	
Interrupt Latency (based on MSV11-D without parity, add 500 ns worst case with parity)	
Worst Case	55.7 microseconds (for infrequently used instructions) 10.8 microseconds (for more frequently used group)
Typical	6.0 microseconds
Interrupt Service Time	8.2 microseconds
DMA Latency	3.49 microseconds (worst case)

EXERCISE

Indicate the correct answer by circling the corresponding letter for each question. You may use references. Check your answers with those given on the Solutions page.

1. The LSI-11 bus which is controlled by the KDF11:

   a. is compatible with the PDP-11/23's bus.

   b. has increased interrupt handling capabilities.

   c. is capable of communicating with an external parity controller.

   d. all of the above

2. The hybrid ICs used in the KDF11 have __________ chips per package.

   a. one
   b. two
   c. three
   d. four

3. The memory management unit allows the KDF11 a usable address space of:

   a. Ø to 124K
   b. Ø to 128K
   c. Ø to 28K
   d. Ø to 32K

4. An M8186 board with a KEF11-A and an MMU is called a:

   a. KDF11-AA
   b. KDF11-AB
   c. KDF11-AC
   d. KDF11-BA

SOLUTIONS

1. d

2. b

3. a

4. b

PHYSICAL/FUNCTIONAL DESCRIPTION

Many of the functions performed by the processor module can be altered by inserting or removing jumpers. In this section you will learn what these functions are and where the jumpers are located. Specifically, the functions which are jumper-alterable are:

- Event line enable
- Power-up mode
- Halt/trap option
- Bootstrap 173000 starting address enable
- Bootstrap starting address select

Use Figure 2 to locate jumpers on the KDF11 for the following discussion.

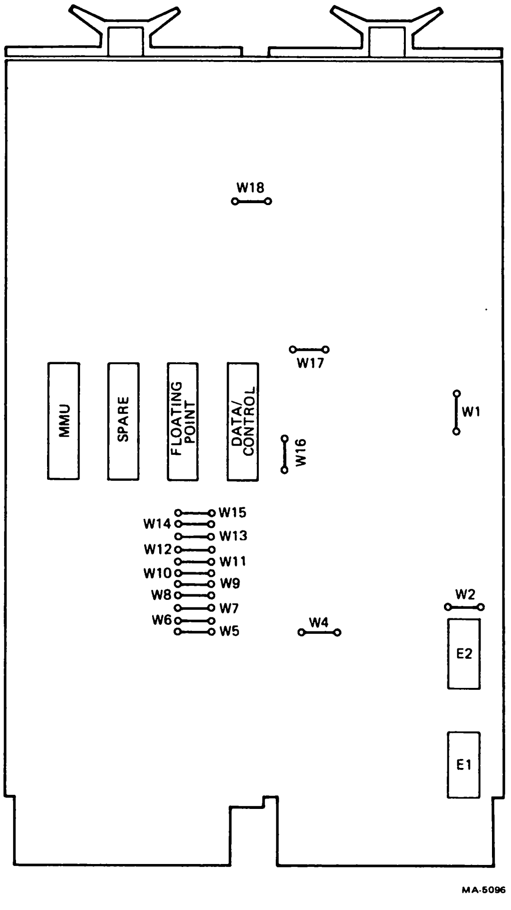


Figure 2. KDF11 Jumper Locations

NOTE

For specific jumper settings, see the Configuring section of this course module.

Event Line Enable

When B EVENT L is asserted on the LSI-11 bus, the processor will trap to location 1ØØ. However, if a multi-level interrupt scheme is used, an interrupt of level five or higher must not be pending. The event line enable, W4, is used to enable or disable the trap to location 1ØØ. Usually this feature is used by the line time clock (LTC).

Power-Up Mode Selection

Four power-up modes are available through the manipulation of W5 and W6. Only the power-up mode is affected, not the power-down sequence. The following paragraphs describe the sequence of events after executing a powerup. The state of bus signal BHALT L is significant in power-up mode operation.

Power-Up Mode Ø

This mode causes the microcode to fetch the contents of memory location 24 and load its contents into the Program Counter (PC). The microcode then examines BHALT L. If BHALT L is asserted, the processor enters console ODT mode. If BHALT L is not asserted, the processor begins program execution by fetching an instruction from the location pointed to by the PC. This mode is useful when power fail/auto restart capability is desired.

Power-Up Mode 1

This mode causes the processor to enter console ODT mode immediately after power-up regardless of the state of the BHALT L line.

Power-Up Mode 2

Depending on the state of jumper W8, the CPU will begin to execute a program at 173ØØØ or some other jumper-selectable address. Unless your system is designed for some special purpose, the CPU should always powerup and execute a bootstrap loader starting at 173ØØØ.

Power-Up Mode 3

Power-up mode 3 is for future use and presently should not be used.

Halt/Trap Option

Depending on the state of W7, when the processor is in the kernel mode (when the operating system is in control of the processor) and encounters a halt instruction, it will either halt or trap to location 1Ø. When in the user mode, the processor will always trap to location 1Ø.

Bootstrap Starting Address Enable

The state of W8 determines whether the processor begins program execution at location 173ØØØ or at some other starting address. Location 173ØØØ is the standard starting address for DIGITAL systems.

Bootstrap Starting Address Selection

When starting execution at any location other than 173ØØØ, jumpers W9 through W15 determine the starting address.

Reserved Jumpers

Jumper Wl is for manufacturing use only and should not be removed. Likewise jumpers W2, W16, W17, and W18 are reserved for future use and should not be removed.

EXERCISE

Part I

In column II check either "Yes" or "No" if the item in column I is jumper-selectable. You may use references.

	Column I	Column II	
		Yes	No
1.	Power-up mode	_____	_____
2.	Processor DMA priority	_____	_____
3.	Memory refresh	_____	_____
4.	Halt trap option	_____	_____
5.	Reply to refresh	_____	_____
6.	Bootstrap starting address enable	_____	_____
7.	Floating point enable	_____	_____
8.	Event line enable	_____	_____
9.	Bootstrap starting address select	_____	_____
1Ø.	ODT enable	_____	_____

Part II

Match the given jumper(s) with their jumper-selectable functions by writing the correct letter next to each jumper. Keep in mind that some of the functions are not jumper-selectable.

11. ____________ W4 a. Power-up mode

12. ____________ W5, W6 b. Processor DMA priority

13. ____________ W7 c. Memory refresh

14. ____________ W8 d. Halt trap option

15. ____________ W9-W15 e. Reply to refresh

f. Bootstrap starting address enable

g. Floating point enable

h. Event line enable

i. Bootstrap starting address select

j. ODT enable

SOLUTIONS

1. Yes
2. No
3. No
4. Yes
5. No
6. Yes
7. No
8. Yes
9. Yes
1Ø. No

11. h
12. a
13. d
14. f
15. i

THEORY OF OPERATION

At first glance the operation of the M8186 processor seems to be very complex because of the many functions it performs. However, you will notice that in the block diagram (Figure 3) each function is performed by an individual block. The functions (or blocks) that you will be studying in this section are the:

- Data chip
- Control chip
- Memory Management Unit (MMU) chip
- Data-Address Lines (DAL)
- Micro Instruction Bus (MIB)
- DMA control
- Chip reset logic
- Floating point processor (KDF11-A)

Before you read any further locate each of these items on the block diagram (KDF11-A is not shown).

Broad arrows represent buses. Two of the buses shown are, for example, the data and address bus (DAL) and the microinstruction bus (MIB). Thin arrows represent individual signals. The squares along the right side of the diagram represent terminals where the signals may leave the processor board. If the square has a letter B, this indicates that the signal becomes part of the LSI-11 bus.

The heart of the processor is contained on three MOS/LSI chips. They are the data chip, the control chip, and the MMU. The data and control chips are combined in a single 4Ø-pin package. The MMU is packaged as one 4Ø-pin chip.

The MOS chips communicate over two internal buses: the MIB and the DAL. The MIB is used for communication and control among the three MOS chips and for controlling the logic circuitry on the processor board. The DALs are used for transferring data between the MOS chips and to and from the processor and the LSI-11 bus.

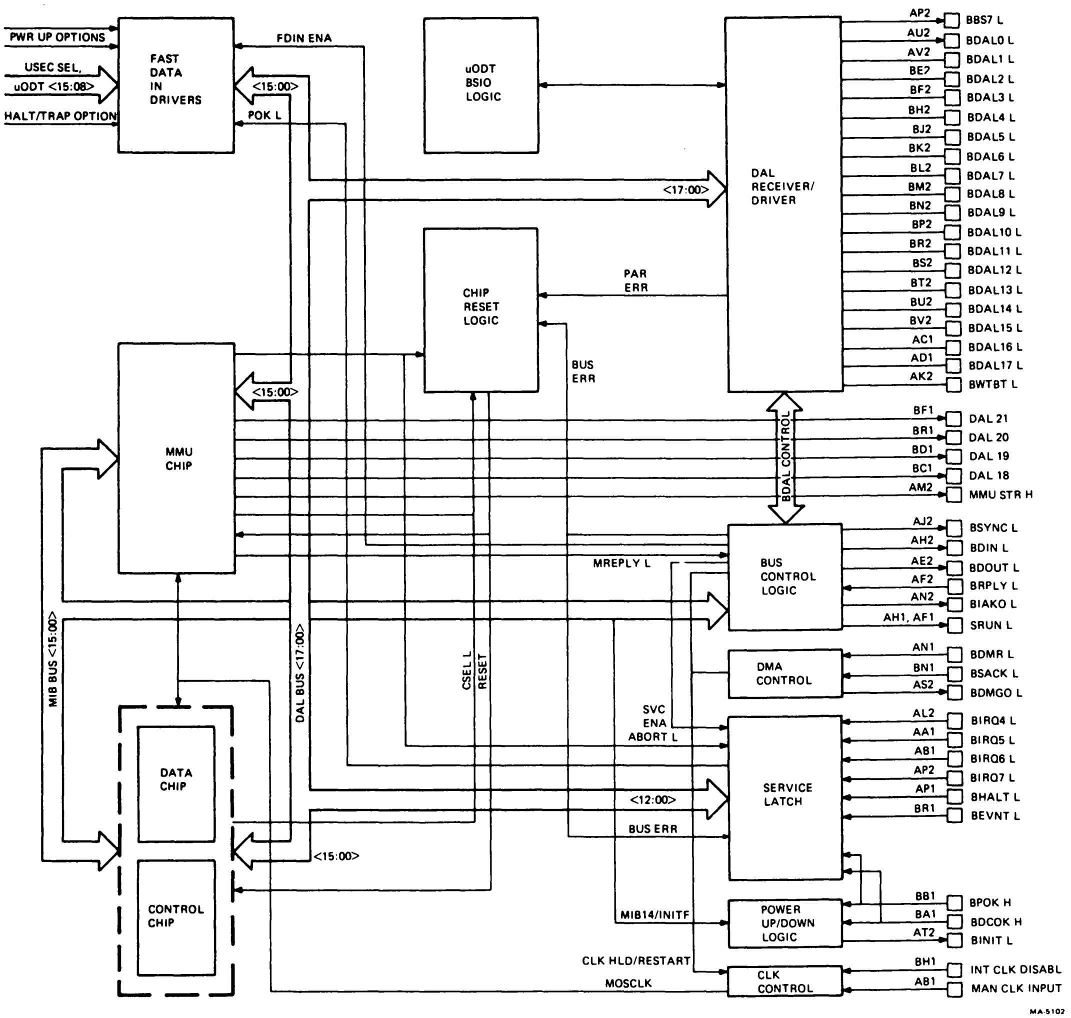


Figure 3. KDF11 Processor Block Diagram

Data Chip

The data chip contains the PDP-11 general registers, the PS, several working registers, ALU, and conditional branching logic. The data chip:

1. Performs all arithmetic and logical functions.

2. Handles all data and address transfers with the LSI-11 bus (except relocation which is handled by the MMU).

3. Generates most of the signals used for interchip communication and external system control.

A typical microinstruction cycle starts when the data chip receives a 16-bit microinstruction from the control chip on the time-multiplexed, bidirectional MIB. During the first half of the cycle the register file is addressed and the selected register(s) are read and sent partially through the ALU chain. Also during the first half of the cycle, control information is decoded from the microinstruction and is output on the MIB for use by other chips and external logic. During the second half of the cycle ALU operation is completed and the result is written back into the appropriate register.

Output operations occur during the first half of the cycle when the contents of the selected source register are bused around the ALU logic directly to the output buffers. Input data is strobed into the data chip during the first half of the cycle, although it is not written into the register file until the second half of the cycle.

Control Chip

The control chip contains the microprogram sequence logic and 552 words of microprogram storage in programmable logic arrays (PLA) and ROM arrays.

During the course of a normal microinstruction cycle, the control chip accesses the appropriate microinstruction in the PLA or ROM, sends it along the MIB to the data and MMU chips for execution, and then generates the address for the next microinstruction to be accessed. The next address is constructed from either a next address field associated with the current microinstruction or, if a microprogrammed branch is to be executed, the target address contained within the microinstruction itself. The control chip operation is pipelined for better performance so that the next microinstruction is being accessed while the current one is being executed. This next address is then used in conjunction with various internal status and external service inputs to determine the microprogram sequence. The control chip accesses only its local storage. Multiple chips (up to 32) can be cascaded with external buffering to provide additional microstore.

Chip Select (CSEL)

CSEL is routed to all MOS chips on the board except the MMU. The active control chip holds the line low. If a nonexistent control chip is selected by the microcode, the line is pulled high. This causes a control chip error and a trap to location 1Ø.

MMU Chip

The MMU chip serves two purposes.

1. It provides the memory management function.

2. It provides storage for the FP11 floating point accumulators and status registers.

This chip provides dual mode (user and kernel) address relocation of 18 bits. Sixteen-bit virtual addresses are received from the data chip via the DAL, relocated to the appropriate 18-bit physical address, and then sent on the DAL to replace the original virtual address for transmission to the external system bus. The MMU chip contains the status registers and active page registers (PAR/PDR register pairs), as well as access protection and error detection capability. The MMU chip also provides the thirty-six 16-bit registers needed for operand storage, scratchpad areas, and status information storage during floating point operations.

The MMU chip is controlled by information received on the MIB from both the data chip and the control chip, and by several discrete control inputs.

The KDF11-AA can operate without the MMU chip; however, the memory would be limited to 32K words and the floating point registers would not be available.

Data-Address Lines (DAL)

The DAL bus is routed between all the MOS chips, along the processor board, and to the LSI-11 bus transceivers. The 16-bit DAL bus is time-multiplexed. During clock-high time, the DAL bus transfers data from the data chip to the other MOS chips or between the processor board and the MOS chips. During clock-low time, the DAL bus transfers service data (external and internal interrupt requests) from the board to the control chip. (The control chip receives service information and determines whether to interrupt or fetch the next instruction.)

Microinstruction Bus (MIB)

The 16-bit MIB is common to all data and control chips. A subset of the MIB is routed to the MMU because it does not need access to all MIB control signals. A different subset of the MIB controls the processor board logic.

The MIB is time-multiplexed and is used for different functions during clock high and low times. During clock-high time, the MIB transfers control information from the data chip to all control chips, the MMU, and the board logic. During clock-low time, the MIB transfers microinstructions from the active control chip to other control chips and the data chip.

Direct Memory Access (DMA)

DMA on the KDF11 board allows peripherals to gain control of the LSI-11 bus from the processor and to transfer data directly between a peripheral and memory. In this way, data transfers can occur at the full memory speed rather than having the processor transfer data words one at a time between the peripheral and memory. A speed gain of about 12 to 1 over regular programmed transfers is gained by this technique.

The signals required for the DMA logic are listed below.

1. BDMR L - This is the DMA request signal. A peripheral device asserts this line when it is ready to use the bus for a DMA transfer. This line is common to all peripheral devices.

2. BDMGO L - This DMA grant signal is issued by the processor in response to a DMA request. By asserting this line, the processor indicates that it will halt processing as soon as the current bus cycle is completed. The processor will also disable all bus control lines and data-address lines (BDAL) so that the peripheral device can use them to control the bus. The BDMR line is common to all peripheral devices. BDMGO L is a daisy-chained signal. Any memory or peripheral device that does not want to use the bus simply passes the signal on. The first (physically closest to the processor) device on the bus desiring to use the bus "takes the grant;" i.e., blocks the signal from being passed on. Therefore, the peripheral closest to the processor requesting the bus at the time the grant is issued gets to use the bus. In order to prevent overuse of the bus by peripheral devices nearest the processor, DMA transfer time must be as short as possible.

3. BSACK L - This DMA acknowledge signal is issued by the peripheral device taking control of the bus. This signal completes the "handshake" between the processor and the peripheral device and indicates to the processor that a device has taken the bus.

4. No SACK Timeout - In LSI-11 bus systems there is a possibility that a device can request use of the bus and then not take the DMA grant signal. The no SACK timeout feature clears the DMA grant signal and returns bus mastership to the processor if no peripheral device has issued BSACK L within 18 microseconds after the processor has issued a grant. This prevents a potential bus lockup problem in which the processor has given up the bus but no one has taken the grant.

Chip Reset Logic

The reset logic is shown in Figure 4. RESET is routed to all MOS chips except the MMU. If an interrupt requiring immediate attention occurs, the line is asserted high. The following five interrupts require immediate attention.

1. Control error - Nonexistent control chip selected by the microcode. A trap to location 1Ø occurs.

2. Bus error - Nonexistent memory location accessed. A trap to location 4 occurs.

3. Parity error - A parity error detected on a current read from memory. A trap to location 114 occurs.

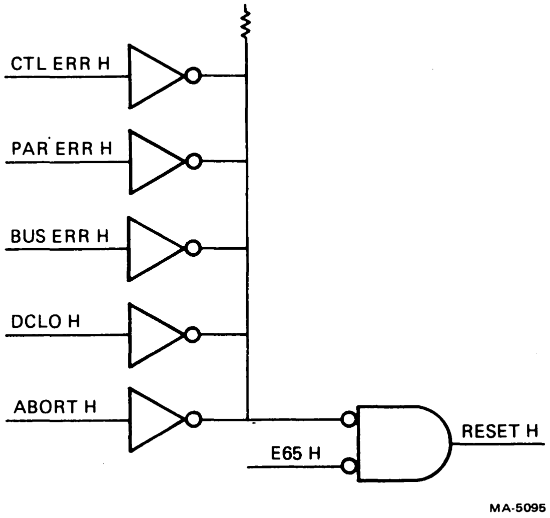


Figure 4. Chip Reset Logic

4. MMU abort - The MMU has aborted a mapped reference. A trap to location 25Ø occurs for any of the following reasons.

   - The memory location referenced is not present in the current user's protected address space.

   - An attempt is made to modify a write-protected location.

   - The user is exceeding his allotted page boundary.

5. DC powerup - Upon powerup the processor forces two sequential RESETS to the chip set to initialize all internal chip registers. The dc power-up line then clears and is not activated again while dc power is on.

Floating Point Processor (KEF11-A)

The floating point processor (FPP) is a microcode option (KEF11-A for use with the KDF11-AA). The KEF11-A FPP is completely software-compatible with the FP11-A used on the PDP-11/34, the FP11-E used on the PDP-11/6Ø, and the FP11-C used on the PDP-11/7Ø. Both single and double precision floating point capability are available together with other features including floating-to-integer and integer-to-floating conversion.

The FPP microcode resides in two MOS/LSI chips contained in one 4Ø-pin package. The FPP requires the MMU chip, in addition to the base MOS/LSI chips, because all the floating point accumulators and status registers reside in the MMU.

EXERCISE

Indicate the correct answer by circling the corresponding letter. You may use references. Check your answers with those given on the Solutions page.

1. Which statement about the control chip is true?

   a. It contains the ALU.

   b. It has 522 locations for microcode storage.

   c. It contains the general purpose registers.

   d. It holds the processor status word.

2. Which internal buses are time multiplexed?

   a. DAL only

   b. MIB only

   c. Both DAL and MIB

   d. None of the above

3. The DMA logic allows data transfers to take place _______ times faster than programmed data transfers.

   a. 2
   b. 4
   c. 6
   d. 12

4. If a nonexistent memory location is addressed, a trap to location ________ occurs.

   a. 1Ø
   b. 4
   c. 114
   d. 25Ø

5. Which statement is true about the KEF11-A?

   a. Is compatible with the floating point processor in the 11/7Ø.

   b. Is located in a single 4Ø pin package.

   c. Requires an MMU chip to be mounted on the processor board.

   d. All the above

SOLUTIONS

1. b

2. c

3. d

4. b

5. d

CONFIGURING

You have already learned that many functions of the KDF11 are jumper-selectable. These features are:

- Event line enable
- Power-up mode
- Halt/trap option
- Bootstrap starting address enable
- Bootstrap starting address select.

In this section you will learn how to configure the jumpers for specific systems. Also, since the maintenance philosophy considers the processor chip set (Data/Control, MMU, and KEF11) to be FRUs, you will have to know something about chip set compatibility and module upgrading. Figure 5 shows the location of the jumpers referred to in the text.

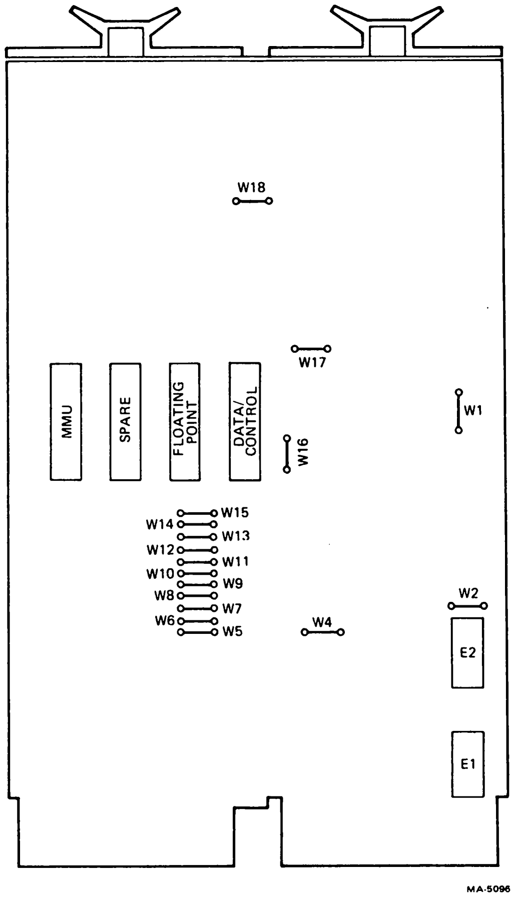


Figure 5. KDF11 Jumper Locations

Event Line Enable - W4

This jumper should be removed (enable) if a line time clock is present. If a programmable real time clock is present, this jumper should be installed (disable).

Power-Up Mode - W5 and W6

The four possible power-up modes are determined by the combinations of W5 and W6 (Table 2). The usual power-up mode is 2.

Table 2. Power-Up Modes

Mode	Function	W6*	W5*
Ø	PC = 24	R	R
1	Console ODT	R	I
2	Bootstrap	I	R
3	Not yet implemented	I	I

*I = Inserted; R = Removed

Halt/Trap Option - W7

If the processor is to halt after executing a HALT instruction while in the kernel mode, W7 should be removed. A trap to location 1Ø will occur if W7 is installed.

Bootstrap Starting Address Enable - W8

The usual condition for this jumper is to be inserted. Installing W8 causes the processor to power up to the DIGITAL standard bootstrap starting address (1730ØØ). Power-up mode 2 must be selected to use this feature. If W8 is removed, the processor will power up to the address selected by W9 through W15.

Bootstrap Starting Address Select - W9 through W15

If W8 is removed, W9 through W15 will specify the bootstrap starting address. Jumpers W9 through W15 correspond to address bits 9 through 15. A logic one is generated by inserting (I) jumpers, while a logic zero is generated by removing (R) jumpers. As an example, to have a bootstrap starting address of 165000, the jumper configuration in Table 3 would be used. All other jumpers (W1, W2, W16, W17, W18) should be inserted. Table 4 gives a summary of jumper functions.

Table 3. Example Jumper Configuration

Bit	Jumper	Logic State	Inserted/ Removed
15	W15	1	I
14	W14	1	I
13	W13	1	I
12	W12	0	R
11	W11	1	I
10	W10	0	R
9	W9	1	I

Chip sets used for different revisions of the KDF11 (M8186) processor module are not identical. Early versions of the processor will not support the KEF11 floating point option. This means that you cannot install the KEF11 option on early versions. Modules which cannot accept the KEF11 chip set can easily be identified by the numbers printed on the IC package. The numbers for the various chip set combinations are given in Table 5.

NOTE

The DAT and CTL chip are mounted on a single hybrid package.

Table 4. Jumper Functions

Jumper	Name	In	Out
W1	Master clock	Enable internal master clock	Do not remove manufacturing use only
W2	Reserved for DIGITAL use	Factory-installed	Do not remove
W4	Event line enable	Disabled	Enabled
W5,W6	Power-up mode selector	See text	See text
W7	Halt/trap option	Trap to 1Ø on halt	Enter console ODT on halt
W8	Conventional bootstrap start address; enable if power-up mode 2 is selected	Power-up to bootstrap address 173ØØØ	Power-up to bootstrap address select by jumpers W9-W15
W9-W15	User-selectable bootstrap starting address for power-up mode 2	Generates logic one	Generates logic zero
W16	Reserved for DIGITAL use	Must be installed	Do not remove
W17	Reserved for DIGITAL use	Must be installed	Do not remove
W18	Reserved for DIGITAL use	Must be installed	Do not remove

Table 5. Chip Set Combinations

Chip	Combination	Model Number	Chip Part Number	Hybrid Part Number
CTL:	#1	DEC 3Ø3-C	23-ØØ1C7-AA	57-ØØØØØ-ØØ
DAT:		DEC 3Ø2-E	21-15541-AA	
MMU:		DEC 3Ø4-C	21-15542-ØØ	
CTL:	#2	DEC 3Ø3-D	23-ØØ1C7-AA	57-ØØØØØ-ØØ
DAT:		DEC 3Ø2-E	21-15541-AA	
MMU:		DEC 3Ø4-C	21-15542-ØØ	
CTL:	#3	DEC 3Ø3-D	23-ØØ1C7-AA	57-ØØØØØ-Ø1
DAT:		DEC 3Ø2-F	21-15541-AB	
MMU:		DEC 3Ø4-C	21-15542-ØØ	

EXERCISE

Ask your Administrator for a KDF11 module. List the jumper settings for:

1. Event Line Enable

   a. Enable
   b. Disable

2. Power-Up Mode

   a. Ø
   b. 1
   c. 2
   d. 3

3. Halt/Trap Option

   After executing a HALT instruction while in the kernel mode the processor will:

   a. Halt
   b. Trap to location 1Ø

4. Bootstrap Starting Address Enable

   a. Enable
   b. Disable

5. Bootstrap Starting Address
   (Only if selected)

   Address _______________

INSTALLATION

At the time this course was written the method for packaging the LSI chip set had not yet been determined. In the future an update will be supplied covering removal and replacement of the LSI chip set.

OPERATION

Whenever the CPU halts, it automatically executes a program called On-Line Debugging Technique (ODT). ODT is used as an aid in modifying or correcting programs. It can examine or deposit data in any memory location or general purpose register (GPR). ODT can also start programs, halt the processor, and perform a number of other functions that will be explained later. The reason for using ODT is to replace the lights and switches of the programmer's console found on the larger PDP-11 computers.

The ODT program is not located in memory. It is implemented as part of the microcomputer chip set. Since ODT is located in a ROM it will always be there when the CPU is powered up.

The Halt Mode

Console ODT commands are executed by the KDF11 processor only when the processor is in the halt mode. When in this mode, the processor responds to commands and information entered via the console terminal, and all processor response is controlled by the processor's microcode.

> NOTE
>
> **For console ODT communication, the DLV11-J must be configured for console bus addresses 17756Ø through 177566. These addresses are included in the KDF11 processor's microcode and cannot be changed.**

Console ODT Operation

The processor's microcode operates the serial line interface in the half-duplex mode. Programmed I/O data transfer is used rather than interrupts. When the console ODT microcode is busy printing characters using the transmit side of the interface, the microcode is not monitoring the receive side for incoming characters. Any characters coming in at this time are lost. The interface may set overrun errors, but the microcode does not check for any error bit in the interface. Therefore, you should not type ahead to ODT because those characters will be lost.

Console ODT Entry Conditions

ODT may be entered as follows.

1. Execution of a HALT instruction in kernel mode, provided the HALT TRAP jumper is not installed.

2. Assertion of the BHALT L signal on the LSI-11 bus. BHALT L is a level, not edge-triggered. The signal must be asserted long enough so that it is seen at the end of a macroinstruction by the service state in the processor.

3. If power-up mode 1 has been selected, ODT is entered upon power-up.

Console ODT Commands

There are only nine commands in the console ODT command set. In the following paragraphs you will find an explanation of these commands along with an example of how each one is used.

> **NOTE**
>
> In the examples the response from the processor is underlined, while the user's entry is not.

/(ASCII Ø57) Slash. This command is used to open an LSI-11 bus address, processor register, or processor status word and is normally preceded by other characters which specify a location. In response to /, console ODT prints the contents of the location (i.e., six characters) and then a space (ASCII 4Ø). After printing is complete, console ODT waits for either new data for that location or a valid close command. The space character is issued so that the location's contents and possible new contents entered by the user are legible on the terminal.

Example: @ØØ1ØØØ/Ø125<SPACE>

where:

@ = console ODT prompt character

ØØ1ØØØ = octal location in the LSI-11 bus address space desired by the user (leading Øs not required).

/ = command to open and print contents of location

Ø12525 = contents of octal location 1ØØØ

<SPACE> = space character generated by console ODT

The / command can be used without a location specifier to verify the data just entered into a previously opened location. The / is recognized only if it is entered immediately after a prompt character. A / issued immediately after the processor enters ODT mode causes a ?<CR><LF> to be printed because a location has not been opened.

```
Example:  @1ØØØ/Ø12525<SPACE> 1234 <CR><CR><LF>
          @/ØØ1234<SPACE>
```

where:

first line = new data of 1234 entered into location 1ØØØ and location closed with <CR>

second line = a / entered without a location specifier and previous location opened to reveal that the new contents were correctly entered into memory

<CR> (ASCII 15) Carriage Return. This command is used to close an open location. If a location's contents are to be changed, the user should precede the <CR> with the new data. If no change is desired, <CR> closes the location without altering its contents.

```
Example: @R1/ØØ4321<SPACE> <CR> <CR><LF>
         @
```

Processor register R1 was opened and no change was desired, so the user issued <CR>. In response to the <CR>, console ODT printed <CR><LF>@.

```
Example: @R1/ØØ4321<SPACE> 1234 <CR> <CR><LF>
```

In this case the user desired to change R1, so new data, 1234, was entered before issuing the <CR>. Console ODT deposited the new data in the open location and then printed <CR><LF>@. Console ODT echoes the <CR> entered by the user and then prints an additional <CR>, followed by a <LF>, and @.

<LF> (ASCII 12) Line Feed. This command is used to close an open location, and then to open the next contiguous location. LSI-11 bus addresses and processor registers are incremented by 2 and 1 respectively. If the PS is open when a <LF> is issued, it is closed and a <CR><LF>@ is printed; no new location is opened. If the open location's contents are to be changed, the new data should precede the <LF>. If no data is entered, the location is closed without being altered.

```
Example: @R2/123456<SPACE> <LF> <CR><LF>
         @R3/Ø54321<SPACE>
```

In this case, the user entered <LF> with no data preceding it. In response, console ODT closed R2 and then opened R3. When a user has the last register, R7, open and issues <LF>, console ODT opens the beginning register, RØ. When the user has the last LSI-11 bus address open of a 32K word segment and issues <LF>, console ODT opens the first location of that same segment. If the user wishes to cross the 32K word boundary, he/she must reenter the address for the desired 32K word segment (e.g., console ODT is modulo 32K word). This operation is the same as that found on all other PDP-11 consoles.

```
Example: @R7/ØØØØØØ<SPACE> <LF> <CR><LF>
         @RØ/123456<SPACE>

         or

         @577776/ØØØØØ1<SPACE> <LF> <CR><LF>
         @477776/125252<SPACE>
```

Unlike other commands, console ODT does not echo the <LF>. Instead it prints <CR>, then <LF> so that terminal printers operate properly. In order to make this easier to decode, console ODT does not echo ASCII Ø, 2, or 1Ø, but responds to these three characters with ?<CR><LF>@.

$ (ASCII Ø44) or R (ASCII 122) Internal Register Designator. Either character when followed by a register number, Ø to 7, or PS designator, S, will open that specific processor register. The $ character is recognized to be compatible with ODT-11. The R character was introduced for the convenience of one key stroke and because it is representative of what it does.

```
Example: @$Ø/ØØØ123<SPACE>

         or

         @R7/ØØØ123<SPACE> <LF>
         @RØ/Ø54321<SPACE>
```

If more than one character is typed (digit or S) after the R or $, console ODT uses the last character as the register designator. However, there is one exception. If the last three digits equal Ø77 or 477, ODT opens the PS rather than R7.

S (ASCII 123) Processor Status Word. This designator is for opening the PS and must be employed after the user has entered an R or $ register designator.

```
Example: @RS/1ØØ377<SPACE> Ø <CR> <CR><LF>
         @/ØØØØ1Ø<SPACE>
```

Note that the trace bit (bit 4) of the PS cannot be modified by the user. This safeguards the PDP-11 program debug utilities (e.g., ODT-11) which use the T bit for single-stepping so that they are not accidentally harmed by the user.

If the user issues a <LF> while the PS is open, the PS is closed and ODT prints a <CR><LF>@. No new location is opened in this case.

G (ASCII 1Ø7) Go. This command is used to start program execution at a location entered immediately before the G. This function is equivalent to the load address and start switch sequence on other PDP-11 consoles.

```
Example: @ 2ØØ <NULL><NULL>
```

The console ODT sequence for a G, after echoing the command character, is as follows.

1. Print two nulls (ASCII 0) so the LSI-11 bus initialize that follows does not flush the G character from the double-buffered Universal Asynchronous Receive/Transmit (UART) chip in the DLV11 serial line interface.

2. Load R7 (PC) with the entered data. If no data is entered, 0 is used. (In the above example, R7 is equal to 200 and that is where program execution begins.)

3. The PS and floating point status register (if the MMU is present) are cleared to 0.

4. The LSI-11 bus is initialized by the processor that is asserting BINIT L for 12.6 microseconds (at 300 ns microcycle), thus negating BINIT L and then waiting for 110 microseconds (at 300 ns microcycle).

5. The service state is entered by the processor. If there is anything to be serviced, it is processed. If the BHALT L bus signal is asserted, the processor re-enters the console ODT state. This feature is used to initialize a system without starting a program (R7 is altered). If the user wants to single-step his program, he issues a G and then successive P commands - all done with the BHALT L bus signal asserted.

P (ASCII 120) Proceed. This command is used to resume execution of a program and corresponds to the Continue switch on other PDP-11 consoles. No programmer-visible machine state is altered using this command.

Example: @ P

Program execution resumes at the address pointed to by R7. After the P is echoed, the console ODT state is left and the processor immediately enters the state to fetch the next instruction. If the BHALT L bus signal is asserted, it is recognized at the end of the instruction (during the service state) and the processor enters the console ODT state. Upon entry, the content of the PC (R7) is printed. In this fashion, a user can single-instruction step through a program and get a PC trace displayed on his terminal.

Control-Shift-S (ASCII 23) Binary Dump. This command is used for manufacturing test purposes and is not a normal user command. It is described here to explain the machine's response if it is accidentally invoked. It is intended to display more efficiently a portion of memory compared to using the / and <LF> commands. The protocol is as follows.

1. After a prompt character, console ODT receives a control-shift-S command and echoes it.

2. The host system at the other end of the serial line must send two 8-bit bytes which console ODT interprets as a starting address. These two bytes are not echoed. The first byte specifies starting address <15:08> and the second byte specifies starting address <07:00>. Bus address bits <17:16> are always forced to be 0; the dump command is restricted to the first 32K words of address space.

3. After the second address byte has been received, console ODT outputs 12 octal bytes to the serial line starting at the address previously specified. When the output is finished, console ODT prints <CR><LF>@. If a user accidentally enters this command, it is recommended, in order to exit from the command, that two @ characters (ASCII 100) be entered as a starting address. After the binary dump, an @ prompt character is printed.

Reserved Commands

An ASCII H is reserved for future DIGITAL use. If it is accidentally typed, console ODT will echo the H and print a prompt character rather than a "?" which is the invalid character response. No other operation is performed.

Table 6 gives a summary of the console ODT commands.

Table 6. Console ODT Commands

Command	Symbol	Use
Slash	/	Prints the contents of a specified location.
Carriage Return	<CR>	Closes an open location.
Line Feed	<LF>	Closes an open location and then opens the next contiguous location.
Internal Register Designator	$ or R	Opens a specific processor register.
Processor Status Word Designator	S	Opens the PS: must follow an $ or R command.
Go	G	Starts program execution.
Proceed	P	Resumes execution of a program.
Binary Dump	Control-Shift-S	Manufacturing use only.
	H	Reserved for DIGITAL use.

EXERCISE

Obtain an operational 11/23 system from your Course Administrator and perform the following Exercise. Check off each item in the Exercise as it is performed.

____ 1. Power up system.

____ 2. Move the Halt/Enable switch to the Halt position and then return it to the Enable position.

____ 3. Type "1ØØØ/". You have just opened location 1ØØØ. The CPU will respond by displaying the contents of location 1ØØØ.

____ 4. Type "123456 <CR>". Remember that <CR> means carriage return. The < > indicates that the carriage return is not printed. You have just deposited 123456 into location 1ØØØ and closed the location with a <CR>.

____ 5. Type "1ØØØ/" again. The data that you have deposited should still be there.

____ 6. Type "<LF>" (remember that <LF> means line feed). Location 1ØØ2 should be displayed.

____ 7. Type <CR>.

____ 8. You are now going to enter a short program that will continuously send characters to the console device. Enter the program below:

```
@ 1ØØØ/XXXXXX 1Ø5737<LF>
ØØ1ØØ2 XXXXXX 177564<LF>
ØØ1ØØ4 XXXXXX 1ØØ375<LF>
ØØ1ØØ6 XXXXXX 11ØØ37<LF>
ØØ1Ø1Ø XXXXXX 177566<LF>
ØØ1Ø12 XXXXXX 52ØØ<LF>
ØØ1Ø14 XXXXXX 137<LF>
ØØ1Ø16 XXXXXX 1ØØØ<CR>
```

NOTE

Leading zeros do not have to be typed when entering addresses or data. The XXXXXX indicates unknown data contents.

After you have entered the program, recheck locations 1ØØØ through 1Ø16.

____ 9. Start the program at location 1ØØØ by typing "1ØØØG". The terminal should now be displaying characters.

____ 1Ø. Stop the program by depressing the BREAK key. The CPU will display the PC contents and the prompt "@".

____ 11. Restart the program by typing "P".

____ 12. Halt the program by putting the Halt switch in the down (halt) position. You will now single-step through the program. Since the Halt switch has been thrown, typing "P" will cause the CPU to execute a single instruction and to halt. Type "P" at least seven times and note how the PC loops through the same addresses.

____ 13. Examine RØ by typing "RØ/".
RØ = __________

____ 14. Using the <LF> key examine R1 through R7.
R1 = __________
R2 = __________
R3 = __________
R4 = __________
R5 = __________
R6 = __________
R7 = __________

____ 15. Deposit 123456 into R5 by typing "R5/XXXXXX 123456".

____ 16. Examine R5 again. The data should still be there.

____ 17. Type "RS/" to examine the processor status word (PSW).
PSW = __________

This completes the course module for the KDF11-AA Processor. Review the material covered and when you are ready, ask the Course Administrator for the module test.

PDP-11V23/11T23 SYSTEM MAINTENANCE

MSV11-DD 32K DYNAMIC MOS MEMORY

MSV11-DD 32K Dynamic MOS Memory

INTRODUCTION

The MSV11-DD MOS memory is capable of storing 32K of 16-bit words. Since the 11V23 system can use up to four of these modules, each module must be configured on an individual basis to operate properly. The modules are shipped with a certain factory configuration. You must be aware of the necessary re-configuration that must be done to the module before it can operate in the system. This course module will provide you with the knowledge necessary to properly configure and install the MSV11-DD into an 11V23 system.

OBJECTIVES

1. Identify major features of the MSV11-DD MOS memory through the use of multiple-choice questions.

2. Select from a list those functions of an MSV11-DD that can be changed by jumper selections and switch settings.

3. Match the functions of the MSV11-DD with the jumpers and switches that control those functions.

4. Describe the theory of operation principles of the MSV11-DD through multiple-choice questions about the following:

   - Memory array
   - Addressing logic
   - Refresh logic
   - Timing and control logic
   - Charge pump circuit

5. Examine an MSV11-DD MOS memory module and list the jumper and switch settings for:

   - Starting address
   - Battery backup
   - Parity select
   - Memory size
   - Bank 7 selection

6. Remove and replace an MSV11-DD module.

SAMPLE TEST ITEMS

1. An MSV11-DD memory module would have which of the following characteristics?

   a. 4K
   b. 8K
   c. 16K
   d. 32K

2. Which of the following features of the MSV11-DD is selected by switches?

   a. Starting address
   b. Parity
   c. Memory size
   d. Battery backup mode

3. Which jumpers allow parity selection?

   a. Pins 5, 6, and 7
   b. W2 and W3
   c. Pins 1, 2 and 3
   d. Pins 15, 16 and 17

4. The purpose of the charge pump circuit is to generate:

   a. +5 volts
   b. +12 volts
   c. -5 volts
   d. -25 volts

5. Ask your Administrator for an MSV11-DD module. Examine the jumpers and switches. List the settings for:

   - Starting address
   - Battery backup
   - Bank 7 selection
   - Memory size
   - Type of parity

6. Remove and replace an MSV11-DD module.

OVERVIEW

The MSV11-DD is a 32K 16-bit word MOS memory located on a double-height module. The designation for this module is M8Ø44-D. This MOS memory will interface with any LSI-11 bus and observes standard DATI, DATO, DATOB, DATIO and DATAIOB bus cycles according to LSI-11 bus protocol.

The first letter of the DD designation means that this is a memory without byte parity. Each word is 16 bits long. If it were an E, then byte parity would exist, making each word 18 bits in size. The second letter designates the memory size with D = 32K. An A is 4K, B is 8K, and C is 16K.

When operating power is removed from any semi-conductor (MOS) memory, the stored data is lost. This is known as volatile memory. However, memory contents can be protected during system power failure by supplying battery back-up power. Jumpers allow the user to implement battery back-up power.

The basic storage element in the MOS memory is a capacitor for each bit. Information is stored as charge or no charge in the capacitor. Since this charge will deteriorate due to leakage, however, it becomes necessary to refresh a given charge every two milliseconds. Earlier models of MOS memory required the refreshing function to be located on a separate module, but the MSV11-DD module contains its own refreshing circuits. This eliminates the need to tie up the LSI-11 bus with refresh sequence signals.

Some of the memory integrated circuits require -5 volts dc which is not available on the backplane. A charge pump circuit located on the MSV11-DD module produces the -5 volts from the +12 volts dc available from the backplane.

The system memory address space to which the module will respond is user-configured by switches contained on the module. An address space can start at any 4K bank boundary ranging through the Ø-128K address range.

Since Bank 7, the upper 4K system address space, is normally reserved for peripheral device addressing, access to this space is disabled when Bank 7 is addressed (when bus signal BBS7 L is asserted). However, some systems only use 2K of address space for peripheral device addressing. The lower 2K of Bank 7 can be enabled for normal addressing by a user-installed jumper.

The specifications for the MSV11-DD are given in Table 1.

Table 1. MSV11-DD Specifications

Identification	M8044-DD
Size	Double

Power

Supply Voltage	Typical Operating Power	Typical Standby Power
+5 V system power	1.7 A	1.7 A
+5 V battery backup	0.7 A	0.7 A
+12 V system power or battery backup	0.37 A	0.08 A

Bus Loading

AC	2
DC	1

Operating (Typical)

Bus Cycle	Access Time (ns)		Cycle Time (ns)	
(Type)	(Typical	Maximum)	(Typical	Maximum)
DATI	210	225	500	520
DATO(B)	100	110	545	565
DATIO(B)	630	650	1075	1100

NOTE:

All operating speeds are based on memory not being busy and no refresh arbitration. Refresh arbitration adds 100 ns typical to access and cycle times (120 ns maximum). Refresh conflicts add 575 ns typical to access and cycle times (600 ns maximum).

EXERCISE

Indicate the correct response for each question by circling the corresponding letter. You may use any references. Check your answers with those given on the Solutions page.

An MSV11-DD memory module would have which of the following characteristics? Choose one from each group.

1. a. 4K
   b. 8K
   c. 16K
   d. 32K

2. a. Non-volatile
   b. Volatile
   c. Liquid
   d. Flammable

3. a. Parity
   b. Non-parity
   c. 18-bit word
   d. Magnetized cores

4. a. Does not require refresh mode.
   b. Relies on refresh circuits of another module.
   c. Has its own refresh circuits.
   d. Does not use capacitor charge to store bits.

5. a. Always used with 2K of space devoted to peripheral addresses.
   b. Can be jumpered to allow use of 2K for peripheral addresses.
   c. Has no space allotted for peripheral addresses.
   d. Bank 1 space is allotted for peripheral addresses.

SOLUTIONS

1. d

2. b

3. b

4. c

5. b

PHYSICAL/FUNCTIONAL DESCRIPTION

The MSV11-DD memory has a wide range of functions. Most of these functions are selected by use of jumpers or switches. In this section you will learn what these functions are and where the jumpers and switches are physically located. The items that are either jumper- or switch-selectable are:

- Starting address of memory
- Memory size
- Battery back-up mode
- Bank 7, lower 2K use
- Parity mode

The jumpers and switches that you will need to locate are shown in Figure 1. This is a drawing of the component side of the MSV11-DD printed circuit board.

> NOTE
>
> For particular switch settings and jumper conditions, see the Configuring section of this course module.

Memory Starting Address

The MSV11-DD memory has a range of 32K words. The usual starting address of the first memory module is ØØØØØØ. If a second memory module is used, its starting address would have to be 2ØØØØØ.

The starting address of a MSV11-DD memory module can actually begin at any 4K bank boundary. This would then be the beginning of a contiguous portion of memory on the module. Normally the starting address is the beginning address of a 32K section of memory.

The switches used to determine the starting memory address are shown in Figure 1, labelled as S1-1 through S1-5. They are physically located in a dual in-line package, more commonly known as a DIP switch.

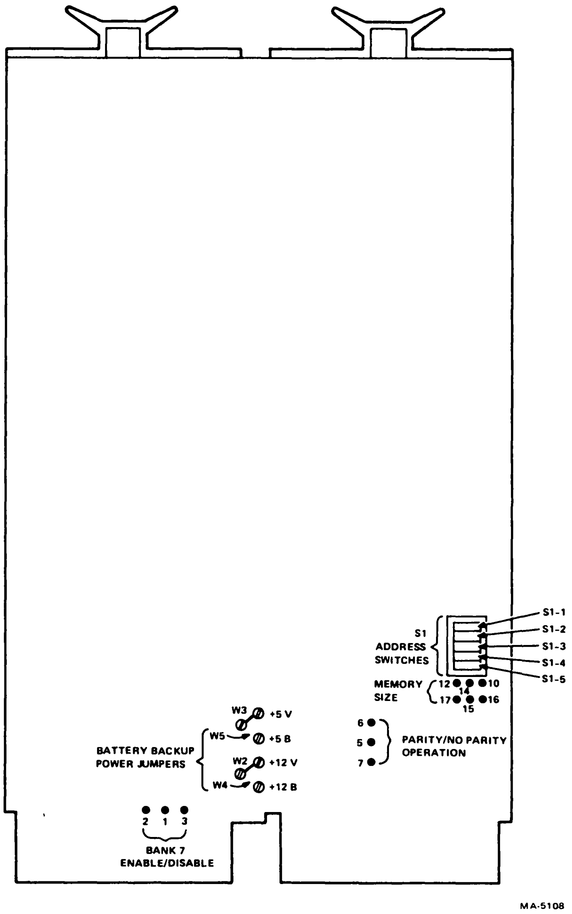


Figure 1. MSV11-DD Switches and Jumpers

Memory Size

Each MSV11-DD module contains two factory-installed wirewrap jumpers next to the Starting Memory Address switches. These are used to indicate the size of memory on the module. These are set to indicate 32K of memory and normally should not be changed. The pins used are shown in Figure 1 and are labelled pins 1Ø, 12, 14, 15, 16, and 17.

Battery Back-up Mode

The MSV11-DD module is factory-configured with the power jumpers installed for normal system power. In this configuration, the memory and refresh logic are powered from the normal bus backplane power. The jumpers are provided to allow the user to disconnect the memory and the refresh logic from the normal bus power and connect it to a separate battery source. These jumpers are located just above the center notch on the connector end of the module and are labelled W2, W3, W4 and W5.

Bank 7, Lower 2K

Modules come from the factory in a configuration that does not allow the memory to respond to any Bank 7 addresses. However, in some special applications, the lower 2K of addresses in Bank 7, 760000-767776, can be used as normal memory address space. By changing the jumper configuration, this mode of operation is made possible. Pins 1, 2 and 3 (Figure 1) are used for this purpose.

Parity

One jumper is factory-installed for non-parity on the MSV11-DD module. DO NOT reconfigure this jumper. The pins labelled 5, 6 and 7 (Figure 1) are used for this purpose.

EXERCISE

Indicate the correct answer to each question by circling the corresponding letter. You may use any references. Check your answers with those given on the Solutions page.

1. Which of the following features of the MSV11-DD is selected by switches?

    a. Starting address
    b. Parity
    c. Memory size
    d. Battery back-up mode

2. Which of the following features is not selected by the use of jumpers on the MSV11-DD module?

    a. Memory size
    b. Bank 7, lower 2K use
    c. Battery back-up mode
    d. Refresh mode

Match the following functions with the switch or jumper numbers. There are some extra functions listed which will not be matched to items in the left column.

Switches and Jumpers

3. ___(S1-1 -- S1-5)

4. ___(Pins 1, 2, 3)

5. ___(Pins 1Ø,12,14, 15, 16, 17)

6. ___(Pins 5, 6, 7)

7. ___(W2,W3,W4,W5)

Functions

a. Battery backup

b. Parity mode

c. Bank 7, lower 2K

d. Memory size

e. Refresh time delay

f. Starting memory address

g. Charge pump osc. freq.

h. Refresh mode

SOLUTIONS

1. a

2. d

3. f

4. c

5. d

6. b

7. a

THEORY OF OPERATION

The basic logic functions and circuits that comprise the MSV11-DD are shown in Figure 2. The memory array is the main function contained on the module. Timing and control circuits along with addressing circuits make up almost all of the remaining logic functions. The refresh logic and charge pump circuit complete the basic function diagram.

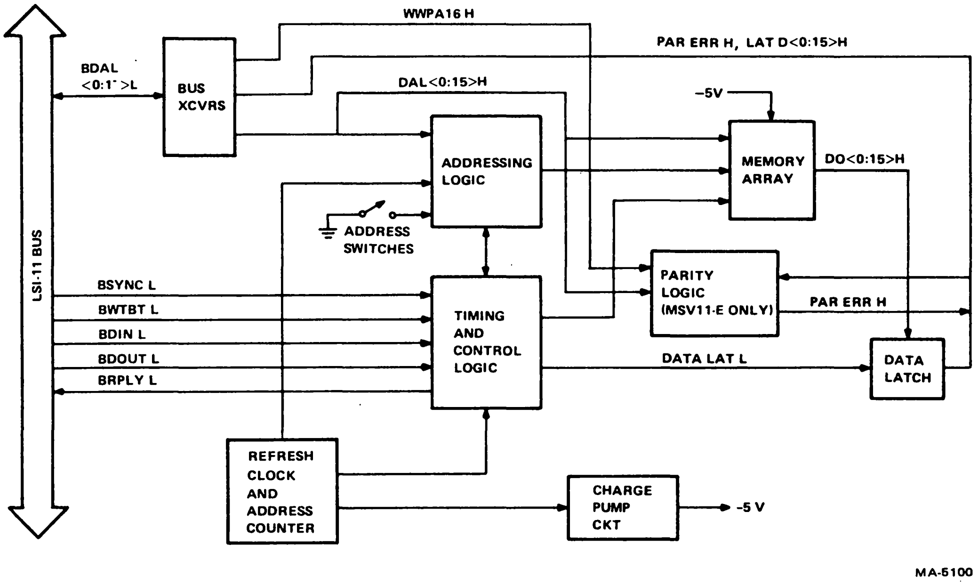


Figure 2. MSV11-DD Block Diagram

Memory Array

A single MOS dynamic Random Access Memory (RAM) IC array contains 16,384 addressable bits. This is designated as a 16K X 1-bit array. Sixteen of these arrays would make up a 16K memory of 16-bit words. Therefore, it takes 32 of the arrays to make up a 32K memory of 16-bit words.

A single 16K X 1-bit array is shown in Figure 3. There are 16 pins on each array chip. An individual bit is addressed through a row and column matrix arrangement. The row address and column address data are brought into the array over seven address lines. The two addresses appear on the address lines in sequence and are strobed into the proper logic functions by a row address strobe followed by a column address strobe. This time-sequencing of data on the address lines is known as multiplexing. Address decoding logic circuits on the array chip will select the addressed bit so it can be read from or written to. A read/write input, WTBT, is used to control the read and write function. A signal line carries data into the array during a write function, and another signal line brings data out during a read function. The power and ground signals make up the rest of the required signals.

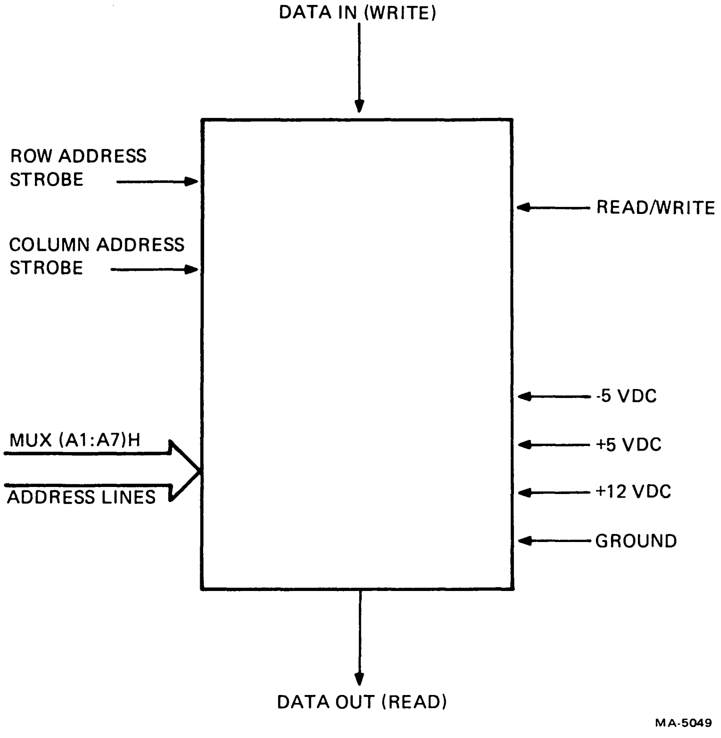


Figure 3. Basic MOS Memory Integrated Circuit

The total memory array on the MSV11-DD module is organized as shown in Figure 4. As mentioned before, this total array is made up of 32 RAM ICs. The circuits are organized into low and high byte groups in a low address range (16K), and another similiar set of byte groups in the high address range (second 16K).

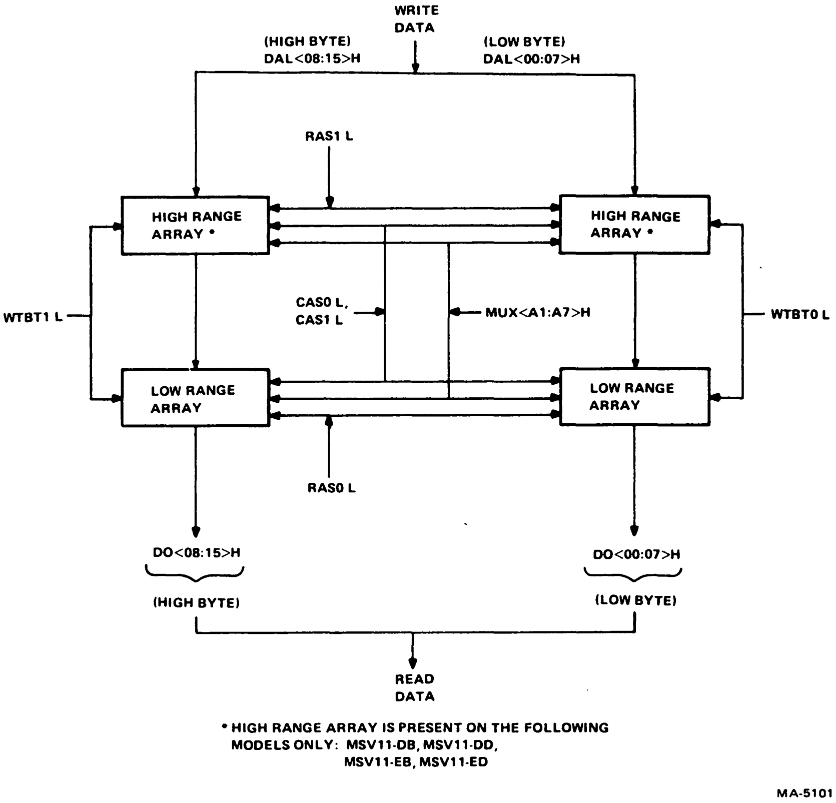


Figure 4. MSV11-DD Memory Array

Row address strobe (RASØ L and RAS1 L) control signals produced by the addressing logic select the appropriate low- or high-range array. Write byte (WTBT1 L and WTBTØ L) control signals are produced by the addressing logic during a memory write operation to select the addressed byte (DATOB bus cycle); during a word write operation (DATO bus cycle), WTBT L is high and selects both bytes.

Fourteen address bits are multiplexed over 7 address lines [MUX(A1:A7) H] to all RAM ICs in the memory array. Addressing is controlled by column address strobe (CASØ L and CAS1 L) and row address strobe (RASØ L and RAS1 L) signals.

Addressing Logic

Addressing logic (Figure 5) receives addresses from the LSI-11 bus and produces address bits and control signals when the received address is for a memory location on the MSV11-DD module.

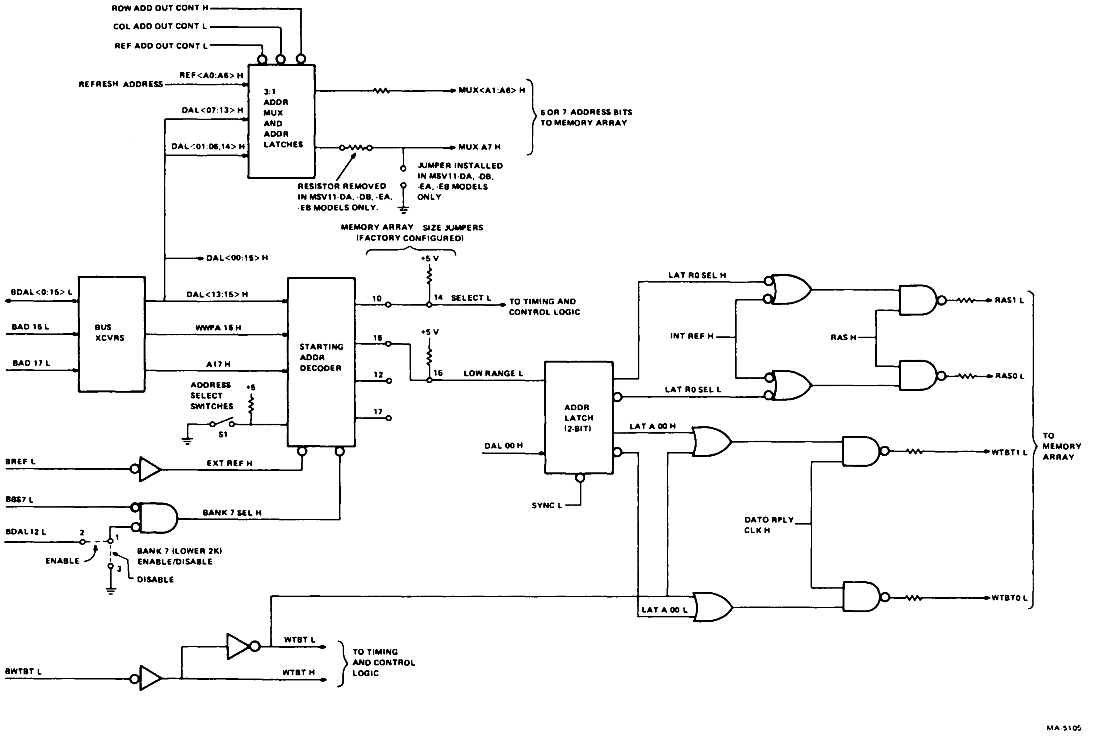


Figure 5. MSV11-DD Addressing Logic

The user configures a starting address that defines the lowest address in the module's range. When an address is received that resides in the module's user-configured range, SELECT L goes active. This signal is produced by decoding address bits DAL (13:15) H and the starting address configured by switches S1-1 thru S1-5. Memory array size jumpers select the appropriate SELECT L and LOW RANGE L decoder ROM outputs. These jumpers are factory-configured and normally should not be changed. SELECT L initiates the memory cycle in the timing and control logic. LOW RANGE L controls selection of RASØ L or RAS1 L signals that select the low-range array or the high-range array.

The upper 4K address space in all systems is normally reserved for peripheral device addresses. However, the user can enable the use of the lower 2K portion of Bank 7 by installing a jumper. When Bank 7 is not enabled, BBS7 L is inverted by a bus receiver producing BANK 7 SEL H. This high signal inhibits the starting address decoder ROM, and no active outputs are produced. When the lower 2K portion of Bank 7 is enabled, a jumper on the input of the BBS7 L bus receiver is reconfigured to inhibit the bus receiver when BDAL 12 L is high (the lower 2K portion). Thus, BANK 7 SEL H will go high only when an address resides in the upper 2K portion of Bank 7 and inhibits memory address decoding.

Memory Refresh

Dynamic MOS memory integrated circuits require periodic refreshing to retain stored data. This is accomplished by forcing a memory read operation on each of the 128 row addresses. Each row address must be refreshed in this manner once every 2 ms (maximum).

The memory refresh logic is shown in Figure 6. A 14.5 μs refresh clock operates the refresh request time to allow completion of 128 refresh cycles during any two ms period. A refresh address counter increments once on each refresh cycle, producing the current refresh row address. Sequential row addresses are thus refreshed, completing all 128 rows within 2 ms for 16K by 1-bit RAM ICs.

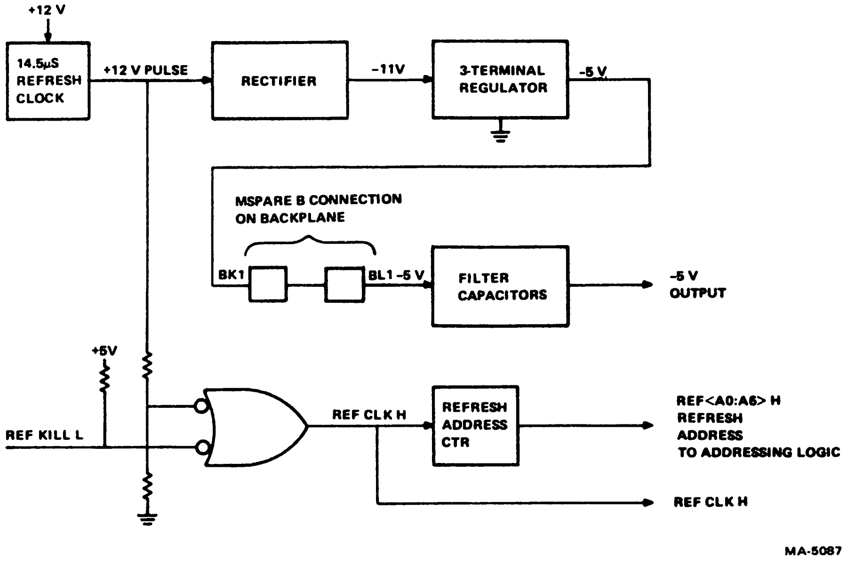


Figure 6. Refresh and Charge Pump Circuits

Charge Pump Circuit

The charge pump circuit (Figure 6) produces -5 Vdc for the memory array. Input power is obtained from the +12 V system via the refresh clock. The resulting 12 V, 14.5 μs refresh clock pulse is applied to a rectifier circuit which produces a -11 Vdc output. A 3-terminal regulator then produces the regulated -5 Vdc.

Timing And Control Logic

Circuits that make up the timing and control logic are shown in Figure 7. The major portions of timing and control functions are contained in timing and refresh arbitration logic. Basic timing for any memory cycle is produced by a tapped delay line and appropriate gating logic. Additional logic functions arbitrate refresh cycles, produce control signals for the memory array addressing logic, and generate appropriate BRPLY L signals during any memory access operation. A memory cycle (other than refresh) is initiated by the active SELECT L signal produced by addressing logic.

If a refresh cycle is in progress when the DATI, DATO(B), or DATIO(B) cycle is initiated, the refresh operation is first completed before continuing the memory access operation. LOCKOUT L goes active during any cycle timing sequence and inhibits the new request from starting another cycle until the present cycle has been completed. However, if a memory access cycle is initiated (addressing portion completed) and a refresh cycle request occurs, refresh arbitration logic delays the start of the memory access cycle approximately 1ØØ ns. If a refresh conflict occurs (refresh wins), the refresh cycle will be first completed and will add about 575 ns to the DATI or DATO(B) cycle time. If memory has been accessed (LOCKOUT L goes passive), a refresh cycle can be initiated although the bus cycle "handshaking" may not have been completed.

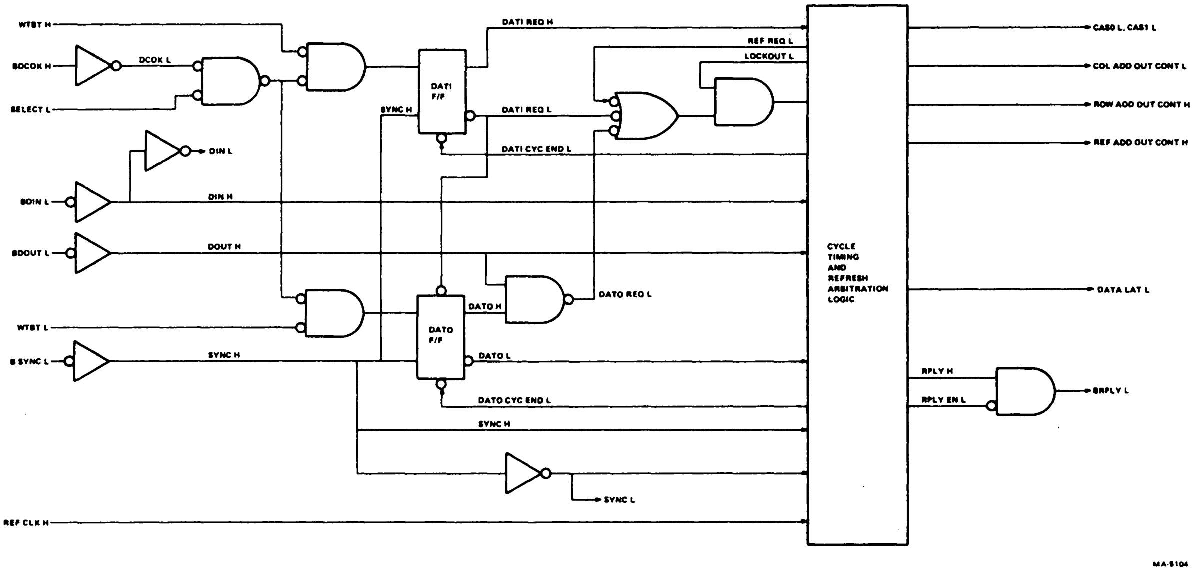


Figure 7. Timing and Control Logic

EXERCISE

Circle the letter that corresponds to the correct response for each question. You may use any references. Check your answers with those given on the Solutions page.

1. The purpose of the charge pump circuit is to generate:

   a. +5 Vdc
   b. +12 Vdc
   c. -5 Vdc
   d. -12 Vdc

2. There are ______ MOS memory integrated chips located on the MSV11-DD module.

   a. 8
   b. 16
   c. 32
   d. 64

3. A refresh cycle is required for the MOS-type memory arrays because:

   a. of the discharging of the storage capacitors.
   b. destructive readout characteristic of the memory.
   c. the addressing logic will fail to operate properly if it is not refreshed.
   d. the writing cycle wears out the storage elements.

4. The memory refresh cycle is used in the array on a(n) ______ basis.

   a. bit-by-bit
   b. row-by-row
   c. column-by-column
   d. array-by-array

5. The __________ signal is used to start all memory cycles except for the refresh cycle.

   a. BRPLY L
   b. LOCKOUT L
   c. DAL 12 H
   d. SELECT L

6. A storage element in the MOS memory array must be refreshed at least every _____.

   a. 14.5 μs
   b. 1ØØ ns
   c. 2 ms
   d. 575 ns

7. Which bit of the LSI-11 bus address determines if the lower 2K of Bank 7 is selected?

   a. BDAL 2 L
   b. BDAL 1Ø L
   c. BDAL 12 L
   d. BDAL 16 L

SOLUTIONS

1. c

2. c

3. a

4. b

5. d

6. c

7. c

CONFIGURING

When you install an MSV11-DD module, you will often find it necessary to change some of the factory-configured jumpers and switches. In this section you will learn how to:

- Set the memory starting address switches
- Select the battery back-up mode
- Enable/disable lower 2K, Bank 7
- Check the memory size jumpers
- Check the parity mode jumper

Memory Starting Address

The MSV11-DD memory starting address can be set at any 4K boundary address. Switches labelled S1-1 through S1-5 in Figure 8 are used to select the starting address.

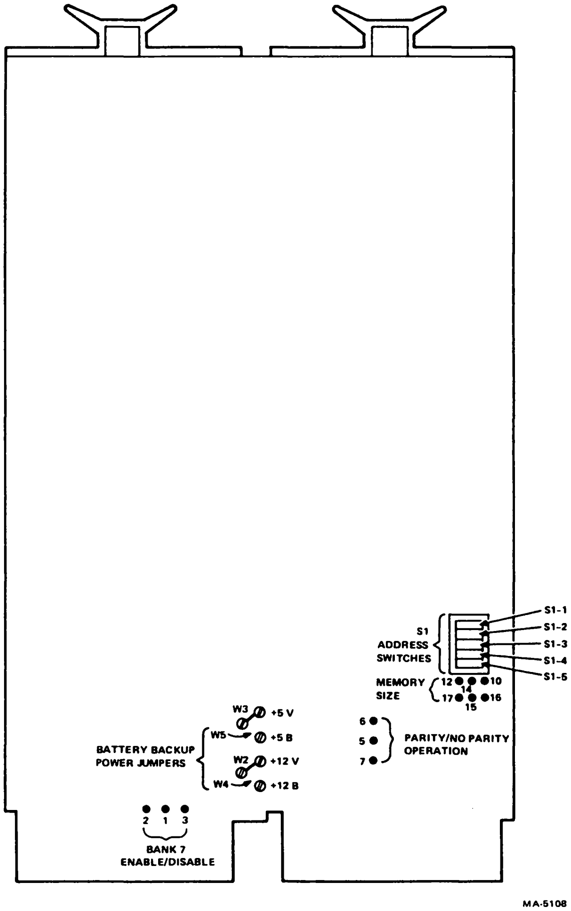


Figure 8. MSV11-DD Switches and Jumpers

The switches are set by pressing them on the red dot in the ON side and reset by pressing them on the red dot located in the OFF side. When the red dot is visible, it appears that the switch is in a complementary state. In other words, when a switch is set to a "1" position, the red dot in the "Ø" column appears, and vice-versa. Table 2 shows the starting addresses possible in the 11V23 system.

Table 2. MSV11-DD Starting Addresses

Starting		Switch Settings			
Addresses	S1-1	S1-2	S1-3	S1-4	S1-5
ØØØØØØ	ON	ON	ON	ON	ON
2ØØØØØ	ON	OFF	ON	ON	ON
4ØØØØØ	OFF	ON	ON	ON	ON
6ØØØØØ	OFF	OFF	ON	ON	OFF

Battery Backup Selection

The MSV11-DD module is factory-configured with the power jumpers installed for normal system power. The module is designed so that during a battery back-up period a minimum of dc power is required. The jumpers provided allow you to disconnect the memory and refresh logic from the normal bus power and connect it to a separate battery source. You can configure the jumpers (Figure 8) as follows.

- W2, W3 Remove to separate the module from the bus-powered backplane.
- W4, W5 Insert to connect the battery power to the memory and refresh logic.

The battery must be capable of supplying:

- +5 Vdc ±3% Ø.7 A
- +12 Vdc +5% Ø.37 A

Lower 2K, Bank 7 Enable/Disable

The lower 2K of Bank 7 (760000-767776) can be enabled for use as normal memory space by removing the jumper from wirewrap pins 1 and 3 and connecting a new jumper from pins 1 and 2. The location of these pins is shown in Figure 8. The factory configuration will disable the lower 2K of memory space which allows it to be used for peripheral device address purposes.

Memory Size

Two jumpers are factory-installed to configure the addressing logic for memory size. Do not change these jumpers. On the MSV11-DD, the correct jumper locations are from pin 15 to 16 and from pin 10 to 14. The location of the pins is shown in Figure 8.

Parity Mode

One jumper is factory-installed for non-parity operation on the MSV11-DD. Do not change this jumper. This jumper should always be installed from pin 5 to pin 7 for the MSV11-DD module.

EXERCISE

Ask your Adminstrator for an MSV11-DD memory module. Examine the jumpers and switch settings. List the configurations selected in each case.

Starting Address = ________________________

Battery Backup _____________________________

Parity Mode Selected = _____________________

Lower 2K , Bank 7 Is _______________________

Memory Size Jumpers From Pins __ To __ And

Pins __ To __.

INSTALLATION

The MSV11-DD module can be inserted into any LSI-11 backplane. Since it is a dual-height module, it is placed into connectors A and B of the backplane. Connector A on the module is the rightmost connector when viewing the component side of the module with the connector fingers pointing down. When inserting or removing the module, the power is to be turned off.

To remove the module, grasp the module firmly and gently pull out of the backplane connectors. Take care when removing the module from the backplane area so that components of the module are not damaged by striking other modules.

> CAUTION
>
> **THE MODULE AND/OR THE BACKPLANE ASSEMBLY MIGHT BE DAMAGED IF THE MODULE IS INSERTED OR REMOVED WITH THE POWER ON OR IF THE MODULE IS INSERTED UPSIDE DOWN.**

EXERCISE

Remove and replace the MSV11-DD module.

This completes the course module for the MSV11-DD 32K Dynamic MOS Memory. Review the material covered and when you are ready, ask the Course Administrator for the module test.

PDP-11V23/11T23 SYSTEM MAINTENANCE

DLV11-J SLU

DLV11-J SLU

INTRODUCTION

The purpose of this course module is to present information which will allow you to configure, install, and program the DLV11-J module. The DLV11-J module is LSI-11 bus compatible and contains four asynchronous serial line unit (SLU) channels. Normally one of the SLU channels is used to communicate with a console terminal device in an LSI-11 system.

The remaining three SLU channels can be used with any devices that use asynchronous serial type communication. The three channels can be configured to operate in three independent modes and speeds. You must understand the configuration procedures for the DLV11-J module because it may not be configured for your system use when you receive it from the factory. It will also be useful to know the bit assignments of the Control/Status Registers associated with this module. This course module assumes that you have some background in serial communication.

OBJECTIVES

1. Find the location of module jumpers on a DLV11-J module illustration by matching each to its proper area.

2. Identify the function of the blocks on the DLV11-J block diagram by matching them to their descriptions.

3. Identify which jumpers must be used for given parameters and modes of operation through the use of a DLV11-J drawing which shows certain jumpers installed.

4. Identify the Control/Status and Buffer Registers with their respective addresses. Also identify the various bits with their functions.

5. Choose the best troubleshooting step to verify or correct a given symptom or diagnostic result for the DLV11-J module.

SAMPLE TEST ITEMS

1. Area "E" on the drawing (Figure 1) is the location for the:

   a. Channel Ø UART
   b. Channel Ø connector
   c. Channel Ø word format jumpers
   d. Channel Ø signal mode jumpers
   e. Baud rate selection jumpers

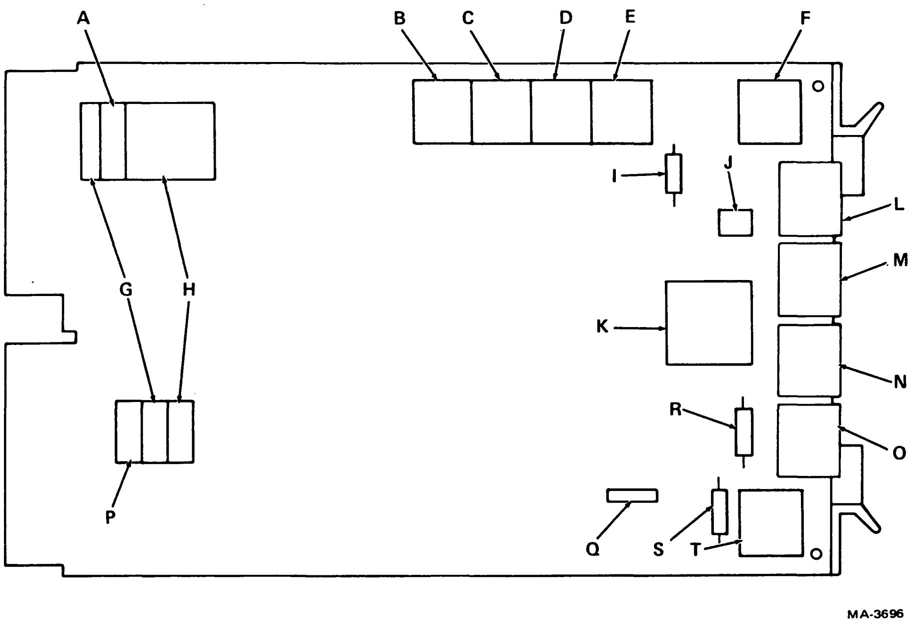


Figure 1. Sample Test Item DLV11-J

2. Identify the function of a selected block from the DLV11-J block diagram by matching it to its function.

   The function of block B is:

   a. UART SLU channel 1
   b. Bus interface
   c. Baud rate generator
   d. UART SLU channel 3
   e. SLU3 transmit

3. To set up the SLU3 channel for an 8-bit character, which posts must be jumpered in the SLU3 word format area?

   a. P X TO Ø
   b. D X TO Ø
   c. E X TO 1
   d. D X TO 1
   e. P X TO 1

4. An address of 177562 on the bus is used to access the:

   a. Channel Ø RBUF Register
   b. Console RBUF Register
   c. Channel 2 XBUF Register
   d. Console XBUF Register
   e. Console RCSR

5. Problem: There is no communication between the CPU and the console terminal when a spare DLV11-J is tried. The console was operating properly with the previous DLV11-J, and when power is applied there is no indication of trouble in the console terminal. You would most likely check which of the following items first?

   a. Jumpers CØ and C1
   b. SLU channel 3 P jumper
   c. SLU channel 3 S jumper
   d. SLU channel Ø D jumper
   e. SLU channel Ø P jumper

RESOURCES

Equipment

1. LSI-based system with DLV11-J module
2. Video terminal
3. Diagnostic diskette (XXDP) with VDLA?? diagnostic
4. Small screwdriver

OVERVIEW

The DLV11-J module is a double-height module which is designed to function in LSI-11 systems. It contains four independent serial line channels, each with its own device and vector address assignments. Each channel can be configured to operate at its own speed and mode of operation. All channels will transmit and receive data simultaneously (duplex mode). If a console termination device is used, it will use channel 3, which uses the normal device and vector addresses assigned to the console termination device.

The specifications for DLV11-J are listed in Table 1.

Table 1. DLV11-J Specifications

Identification M8043	
Electrical	
Power Requirements	+5 Vdc, 1 A typical (1.25 A max.) +12 Vdc, .15 A typical(.2 A max.)
Bus Loading	ac loading = 1 unit load dc loading = 1 unit load
Environmental	
Operating	5 to 60° C (41 to 140° F) with relative humidity of 5% to 95% (Non-condensing) Max. temperature with max. airflow is 60° C. (140° F)
Storage	-40 to 80° C (-40 to 176° F) with relative humidity of 5% to 95% (Non-condensing)
Physical	
Height	13.2 cm (5.2 in) typical
Width	1.27 cm (0.5 in) typical
Length	22.8 cm (8.9 in) typical (includes handles)
Weight	0.23 kg (8.0 oz) typical

PHYSICAL/FUNCTIONAL DESCRIPTION

Four 1Ø-pin connectors labelled JØ-J3 (Figure 2) are provided on the DLV11-J module (one for each channel). The connector pin layout is shown in Figure 3. Table 2 lists the pin assignments.

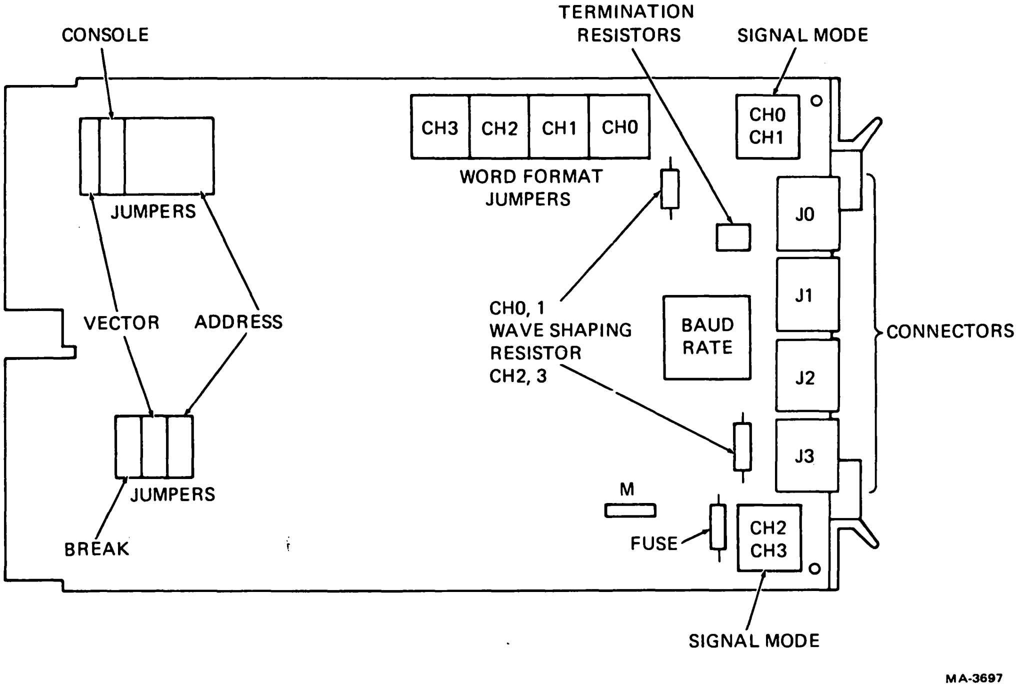


Figure 2. Configuration and Connector Areas on the DLV11-J Module

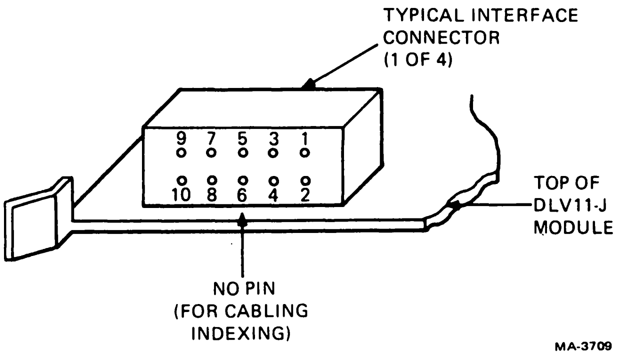

TYPICAL INTERFACE CONNECTOR (1 OF 4)
9 7 5 3 1
10 8 6 4 2
TOP OF DLV11-J MODULE
NO PIN (FOR CABLING INDEXING)
MA-3709

Figure 3. Connector Pin Layout

Table 2. DLV11-J Connector Pins

Pin	Signal/Function
1	UART Clock in or out (16 x baud rate)
2	Signal Ground
3	Transmitted Data (EIA RS-232C;RS-423;2Ø mA) Transmitted Data (+) (EIA RS-422)
4	Signal Ground (EIA RS-232C;RS-423) Transmitted Data (-) (EIA RS-422) RDR Run (2Ø mA option)
5	Signal Ground
6	Index Keying (No pin)
7	Received Data (-)
8	Received Data (+)
9	Signal Ground
1Ø	Fused +12 Vdc

Each channel can be configured to transmit and receive at one of the following baud rates: 15Ø, 3ØØ, 6ØØ, 12ØØ, 24ØØ, 48ØØ, 96ØØ, 192ØØ, or 384ØØ bits per second. The area for installing jumpers to select the baud rates is shown in Figure 2, just to the left of the connectors.

Each channel uses four device registers, two for the transmit function and two for the receive function. A total of 16 device registers on the module can be individually addressed by the computer program. The address of SLUØ channel's first register is used as a base address. It is this address which is configured on the module's wirewrap posts (Figure 2). The remaining SLU addresses are logically derived from this base address.

If SLU3 is used to interface with the console terminal, it must respond to the normal console terminal device addresses and not follow the normal sequential address pattern. A pair of jumpers used to indicate this is located between the upper vector and address jumpers (Figure 2).

Each of the SLU channels must be provided with two interrupt vectors, one for receive and one for transmit. The same method used in the address scheme is used for the vector addresses. The SLUØ receive vector address is used as a base address. It is configured at the jumper wirewrap posts (Figure 2).

It is also necessary to configure the word format to be used by each channel. This is necessary whether seven or eight data bits are used, one or two stop bits, and if parity is used, whether it is odd or even. Figure 2 shows the location of these jumper wirewrap posts for the word formats.

When SLU3 is used for a console terminal and the BREAK key is depressed, a jumper chooses the system response (Figure 2).

Each SLU channel can be independently configured for signal line compatibility with EIA RS-422, RS-423, RS-232C, or 2Ø mA current loop devices. It may be necessary to install termination or waveshaping resistors depending upon the mode chosen. The location of the signal mode jumpers and resistors is shown in Figure 2.

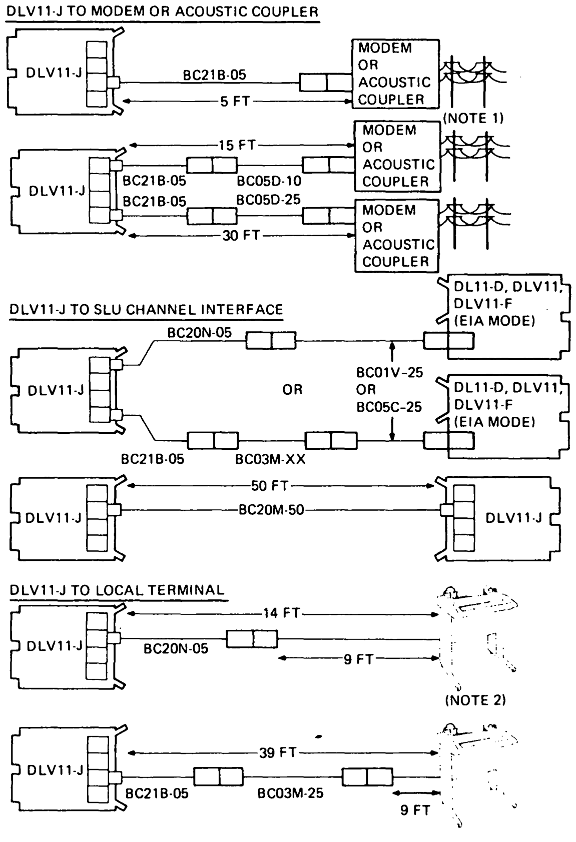
The DLV11-J module can be used for 2Ø mA current loop operation when it is connected to the DLV11-KA option. An on-board fuse is installed for this application (Figure 2).

Jumper M is removed only for factory checkout. It should <u>not</u> be removed in the field.

Options

The DLV11-J will work with several peripheral device cables and options. Figure 4 illustrates the possible cables and options used as well as the primary application of each.

The 2Ø mA current loop option, DLV11-KA, consists of a DLV11-KB EIA to 2Ø mA current loop converter and a BC21A-Ø3 interface cable. The cables and devices which can be used with this option are shown in Figure 5.

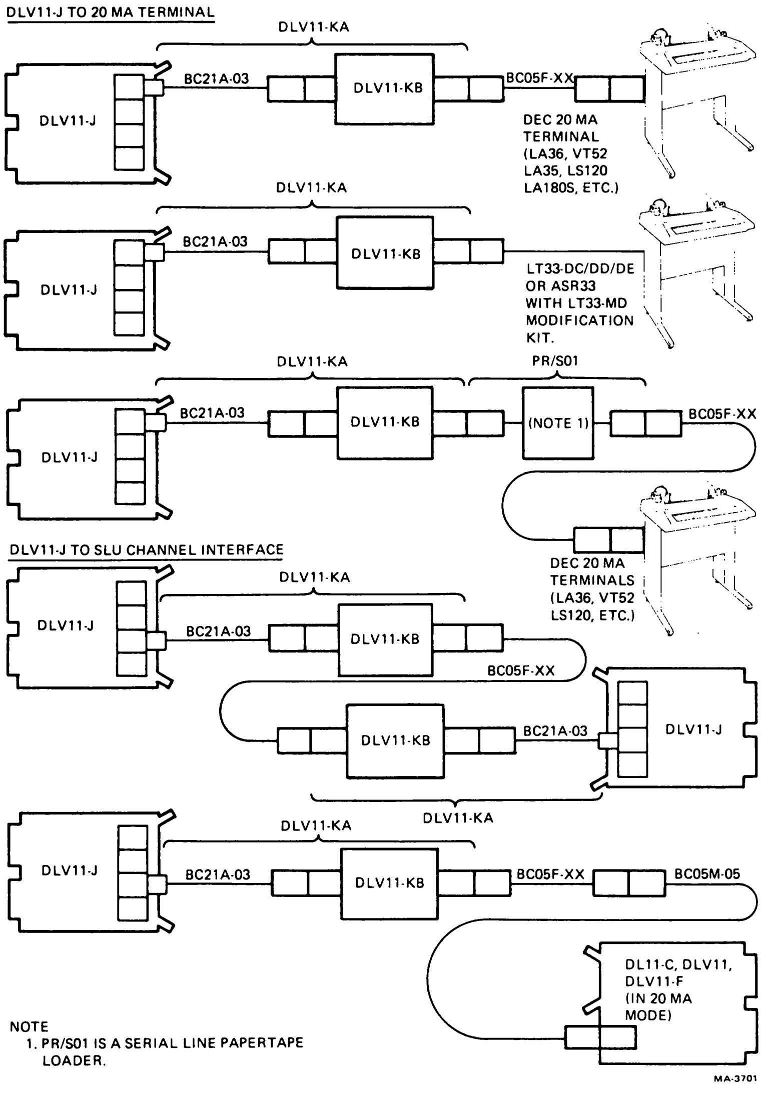

DLV11-J TO MODEM OR ACOUSTIC COUPLER
DLV11-J
BC21B-05
5 FT
MODEM OR ACOUSTIC COUPLER
(NOTE 1)
15 FT
DLV11-J
BC21B-05
BC05D-10
BC21B-05
BC05D-25
30 FT
MODEM OR ACOUSTIC COUPLER
MODEM OR ACOUSTIC COUPLER
DLV11-J TO SLU CHANNEL INTERFACE
DL11-D, DLV11, DLV11-F (EIA MODE)
BC20N-05
DLV11-J
OR
BC01V-25 OR BC05C-25
DL11-D, DLV11, DLV11-F (EIA MODE)
BC21B-05
BC03M-XX
50 FT
DLV11-J
BC20M-50
DLV11-J
DLV11-J TO LOCAL TERMINAL
14 FT
DLV11-J
BC20N-05
9 FT
(NOTE 2)
39 FT
DLV11-J
BC21B-05
BC03M-25
9 FT

NOTES:

1. MODEM USED IS A "MANUAL TYPE" SUCH AS BELL 103A WITH 804B.
2. DEC EIA RS-232C TERMINALS (VT52, LA36, LS120, ETC.) COME EQUIPPED WITH A 9 FT CABLE. NON-DEC EIA RS-232C TERMINALS ARE CONNECTED SIMILARLY EXCEPT 9 FT OF LENGTH MUST BE DEDUCTED FROM THE TOTAL CABLE LENGTH.

MA-3702

Figure 4. Cabling Summary


DLV11-J TO 20 MA TERMINAL
DLV11-KA
DLV11-J
BC21A-03
DLV11-KB
BC05F-XX
DEC 20 MA TERMINAL (LA36, VT52 LA35, LS120 LA180S, ETC.)
DLV11-KA
DLV11-J
BC21A-03
DLV11-KB
LT33-DC/DD/DE OR ASR33 WITH LT33-MD MODIFICATION KIT.
DLV11-KA
PR/S01
DLV11-J
BC21A-03
DLV11-KB
(NOTE 1)
BC05F-XX
DEC 20 MA TERMINALS (LA36, VT52 LS120, ETC.)
DLV11-J TO SLU CHANNEL INTERFACE
DLV11-J
DLV11-KA
BC21A-03
DLV11-KB
BC05F-XX
DLV11-KB
BC21A-03
DLV11-J
DLV11-KA
DLV11-J
DLV11-KA
BC21A-03
DLV11-KB
BC05F-XX
BC05M-05
DL11-C, DLV11, DLV11-F (IN 20 MA MODE)
MA-3701

NOTE
1. PR/S01 IS A SERIAL LINE PAPERTAPE LOADER.

Figure 5. 2Ø mA Option Cabling Summary

EXERCISE

Complete the following exercise using Figure 6 and any material as reference. Circle the letter of the correct response. Check your answers with those given on the Solutions page.

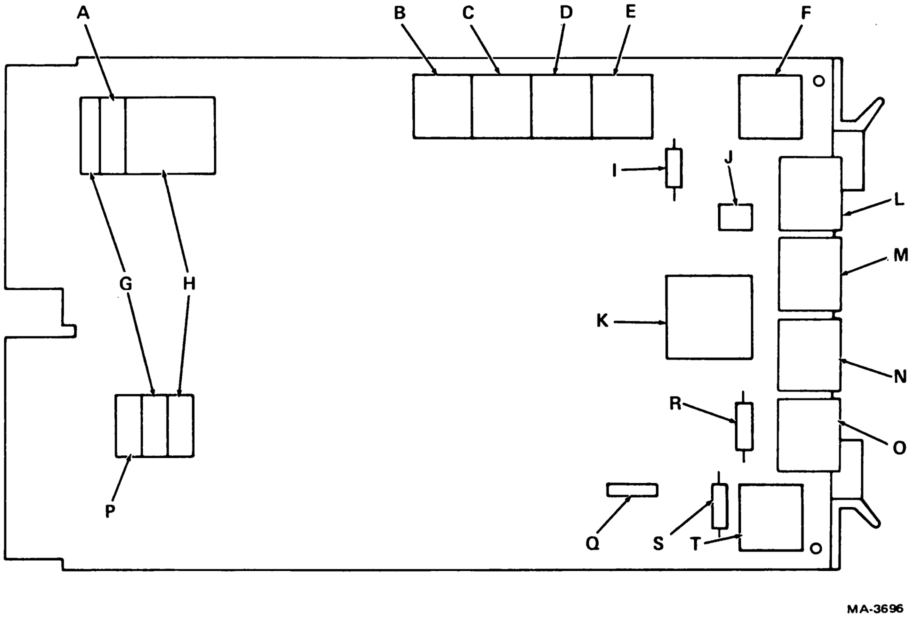


Figure 6. Physical/Functional Exercise DLV11-J

1. Arrow E indicates the:

   a. Channel Ø UART
   b. Channel Ø connector
   c. Channel Ø format jumpers
   d. Channel Ø signal mode jumpers
   e. Baud selection jumper

2. Arrow H indicates the:

   a. Vector address jumpers
   b. Device base address jumpers
   c. Break selection jumper
   d. Baud selection jumpers
   e. Channel Ø, 1 signal mode jumpers

3. Arrow P indicates the:

   a. Baud selection jumpers
   b. Console terminal jumpers
   c. Vector address jumpers
   d. Device base address jumpers
   e. break selection jumper

4. Arrow O indicates the:

   a. Channel Ø connector
   b. Console terminal connector
   c. Channel 1 connector
   d. Channel 2, 3 signal mode jumpers
   e. Channel 2 connector

5. Arrow A indicates the:

   a. Console termination jumpers
   b. Baud selection jumpers
   c. Vector address jumpers
   d. Device base address jumpers
   e. Break selection jumper

6. Arrow J indicates the:

   a. Channel Ø connector
   b. Channel termination resistors
   c. Baud rate selection jumpers
   d. Channel Ø, 1 signal mode jumpers
   e. Channel Ø format jumpers

7. Arrow G indicates the:

   a. Vector address jumpers
   b. Device base address jumpers
   c. Break selection jumper
   d. Console termination jumpers
   e. None of the above

SOLUTIONS

1. c

2. b

3. e

4. b

5. a

6. b

7. a

Block Diagram Description

The following functional description of the DLV11-J module is based on the simplified block diagram in Figure 7.

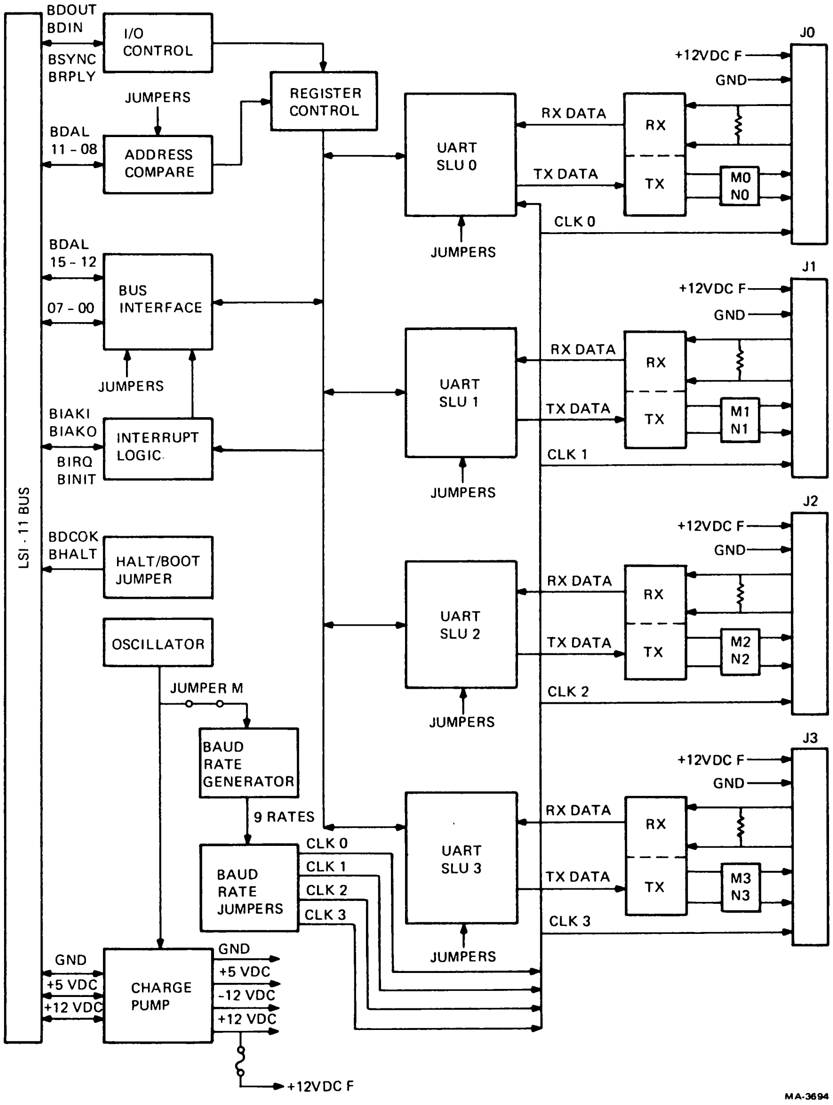


Figure 7. DLV11-J Block Diagram

The DLV11-J receives data on the LSI bus and converts it to the format required by the peripheral device, including the data format, timing, and proper signal levels. The data is received from the bus in parallel format and changed to a serial data stream for transmission to the device. In the receive mode, the serial data stream from the device must be changed to parallel format for transmission to the processor.

The I/O control logic controls the overall operation of the DLV11-J module by directing data transactions between the processor and the DLV11-J. The I/O control logic also monitors the LSI-11 bus lines to recognize if the data transaction is word or byte, input or output, and status or character data. It controls the four device registers of each SLU to write or read processor information.

The desired channel is selected by the processor by placing its address on the LSI bus, along with timing and control signals. The bus interface and address compare functions will be used to match the address on the bus with the address set up by the address jumpers. When a match occurs, the channel and register are also selected. Through the register control function, the data presented on the bus will be placed into the proper register, either the Control/Status or Data Buffer Register, of the selected channel.

If the Control/Status Register is used, the processor may be beginning a receive or transmit operation, or it may be checking for errors from the previous operation. If the bus data lines carry a character to be transmitted, the parallel data is passed into the respective UART for conversion to the serial bit stream with proper format and timing for the peripheral device. The bit stream passes through the TX (Transmit) interface logic to be made compatible with the signal level required by the device, as determined by the jumpers configured on the DLV11-J module. The processor can be notified that the character has been transmitted and thus must send the next character by use of the interrupt logic. The DLV11-J module sends an interrupt vector address for the processor to use to locate the service routine it must execute in order to find and send the next character.

When data is being received from peripheral devices, it enters the RX (Receive) interface logic. Here it is converted to TTL signal levels which are applied to the UART receive section. At this point the serial bit stream is converted to parallel data and checked for parity errors and timing errors. When the character is ready for transmission to the processor, an interrupt routine is entered by the DLV11-J, request is made to use the bus, and the interrupt vector address is sent to the processor. A service routine is used to read the character and store it in memory.

Each channel can operate independently at its own baud rate as selected by the jumpers. An oscillator produces a master clock signal, and the baud rate generator is used to divide the rate to the required rates. These are made available at posts where they can be connected by jumpers (baud rate jumpers) to each channel.

It is necessary to provide -12 Vdc to the EIA driver chips. This voltage is not available on the LSI-11 bus, so it is produced on the DLV11-J module by the charge pump circuitry.

EXERCISE

Complete the following exercise while referring to Figure 8 and any resource material. Circle the letter of the correct response. Check your answers with those given on the Solutions page.

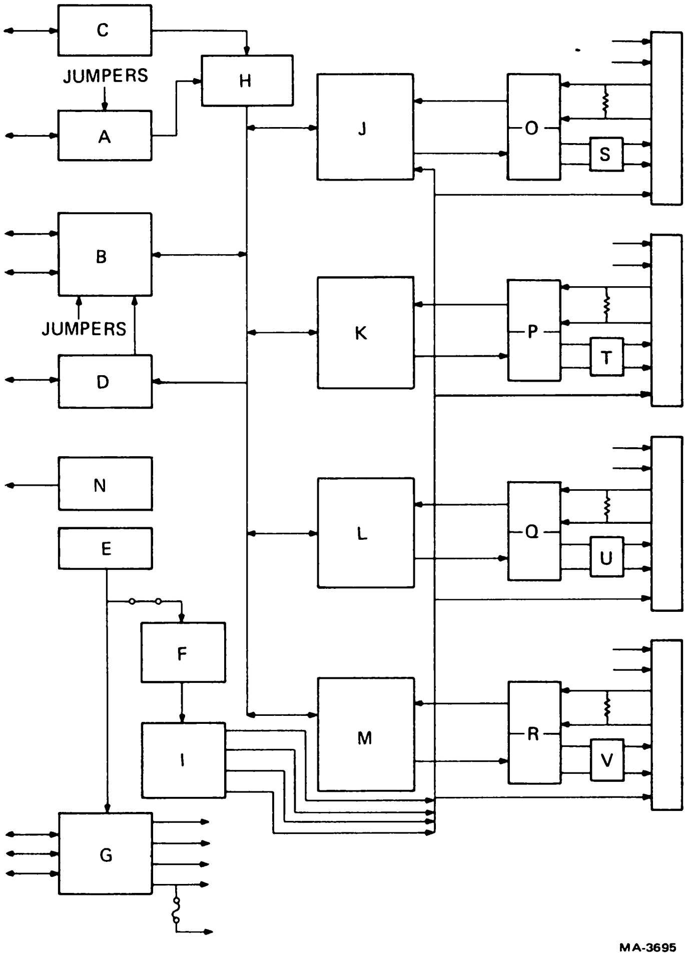


Figure 8. DLV11-J Block Diagram Exercise

1. The block B function is:

   a. UART channel 1
   b. Bus interface
   c. Baud rate generator
   d. UART channel 3
   e. SLU3 receive/transmit

2. The block F function is:

   a. UART channel 1
   b. Bus interface
   c. Baud rate generator
   d. UART channel 3
   e. SLU3 receive/transmit

3. The block R function is:

   a. UART channel 1
   b. Bus interface
   c. Baud rate generator
   d. UART channel 3
   e. SLU3 receive/transmit

4. The block H function is:

   a. I/O control
   b. Address compare
   c. UART channel Ø
   d. Register control
   e. Bus interface

5. The interrupt function is block:

   a. A
   b. B
   c. C
   d. D
   e. E

6. The line signal mode jumpers for SLUØ are in block:

   a. O
   b. P
   c. Q
   d. S
   e. T

SOLUTIONS

1. b

2. c

3. e

4. d

5. d

6. d

CONFIGURING

Since the DLV11-J module is shipped in a factory configuration, it will be necessary for you to reconfigure the module for your particular system and application. This part of the course module will discuss the various parameters and configuration modes which must be checked before installation. A wirewrap tool will be needed to change the jumpers.

> NOTE
>
> **When jumpers need to be changed for only a few of the parameters and modes, refer to the preceding pages for the configuration instructions.**

Bus Addresses

Even though the DLV11-J module contains 16 device registers that can be individually addressed, it is necessary to configure the module only for the first or base address of the series. This is the address for the SLUØ Receiver Control/Status Register. The factory-assigned base address is 1765ØØ, and SLU3 is selected by factory-installed jumpers to be used with the console termination device. Table 3 shows the resulting address pattern.

Table 3. DLV11-J Address Pattern

Address	Register	
1765ØØ	RCSR	SLUØ
1765Ø2	RBUF	
1765Ø4	XCSR	
1765Ø6	XBUF	
176510	RCSR	SLU1
176512	RBUF	
176514	XCSR	
176516	XBUF	
17652Ø	RCSR	SLU2
176522	RBUF	
176524	XCSR	
176526	XBUF	
17756Ø	RCSR	CONSOLE (SLU3)
177562	RBUF	
177564	XCSR	
177566	XBUF	

R = RECEIVE
X = TRANSMIT

Bits 17-13 are not connected by jumpers on the module (Figure 9). These bits are set automatically when an upper address is accessed by the Bank 7 select (BBS7 L) bus signal. Bits 12-Ø5 are used for jumper configuration while the remaining bits are not. Bits 4 and 3 are used by the program to select the channel SLU and bits 2 and 1 are used by the register.

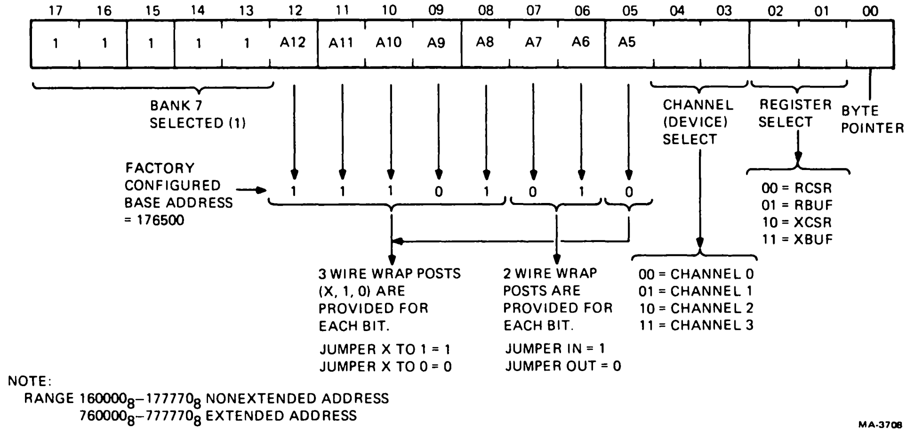


Figure 9. DLV11-J Address Format

For bits 12-Ø8, the three wirewrap posts X, 1, and Ø are available (Figure 1Ø). The X post is connected to the 1 for a bit equal to 1, and to the Ø for a bit equal to Ø, for each address bit position. Bits Ø7-Ø6 have only two posts provided for each bit, with the jumper installed for a bit equal to 1, and the jumper removed for a bit equal to Ø.

To select SLU3 as a console termination interface, the two C jumpers, located just below the address bits 12-Ø8 posts, must be installed. C1 and C2 must be jumpered from X to 1 (Figure 1Ø).

NOTE

If SLU3 is used as the console termination interface, the base address of the DLV11-J module is restricted to 1765ØØ, 17654Ø, or 1775ØØ.

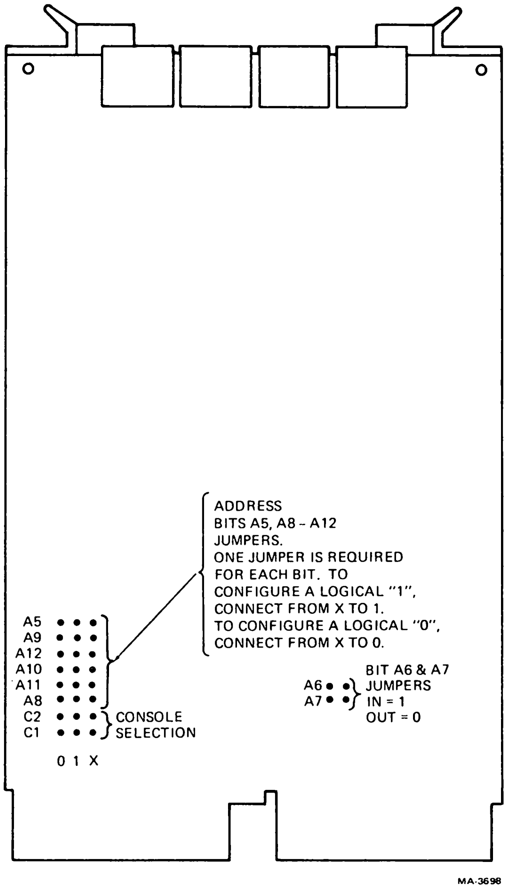
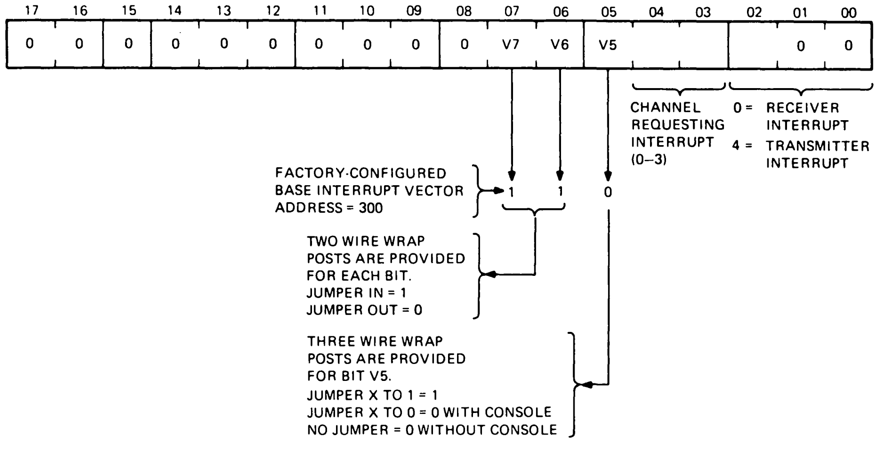


Figure 1Ø. DLV11-J Address Jumper Locations

Vectors

Each of the SLU channels is provided with two interrupt vectors, one for the receive and one for transmit function. Figure 11 illustrates the interrupt vector format.

Only bits Ø7, Ø6, and Ø5 are used for jumper configuration. For bits Ø7 and Ø6, two wirewrap posts are provided, where the jumper is installed if the bit equals a 1. No jumper is installed if the bit equals a Ø. Bit Ø5 position uses three jumper posts, the X, 1, and Ø. A jumper is installed from X to 1 when the bit is a 1, and X to Ø for a bit equal to Ø when the console termination is used. If no console termination is used, no jumper is used at this position. The vectors used by the channels are set at the factory as listed in Table 4.


17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
0 0 0 0 0 0 0 0 0 0 V7 V6 V5 0 0
CHANNEL REQUESTING INTERRUPT (0–3)
0 = RECEIVER INTERRUPT
4 = TRANSMITTER INTERRUPT
FACTORY-CONFIGURED BASE INTERRUPT VECTOR ADDRESS = 300
1 1 0
TWO WIRE WRAP POSTS ARE PROVIDED FOR EACH BIT. JUMPER IN = 1 JUMPER OUT = 0
THREE WIRE WRAP POSTS ARE PROVIDED FOR BIT V5. JUMPER X TO 1 = 1 JUMPER X TO 0 = 0 WITH CONSOLE NO JUMPER = 0 WITHOUT CONSOLE
MA-3707

NOTE:
RANGE 0–377_8 (040_8 NOT ALLOWED IN CONSOLE MODE)

Figure 11. Interrupt Vector Format

Table 4. Factory Vector Settings

Vector	Function
3ØØ	RX SLUØ
3Ø4	TX SLUØ
31Ø	RX SLU1
314	TX SLU1
32Ø	RX SLU2
324	TX SLU2
6Ø	RX CONSOLE (SLU3)
64	TX CONSOLE

If the SLU3 channel is not used for a console termination, the vectors and device addresses are a normal continuation of the other addresses. The vector jumper posts are shown in Figure 12.

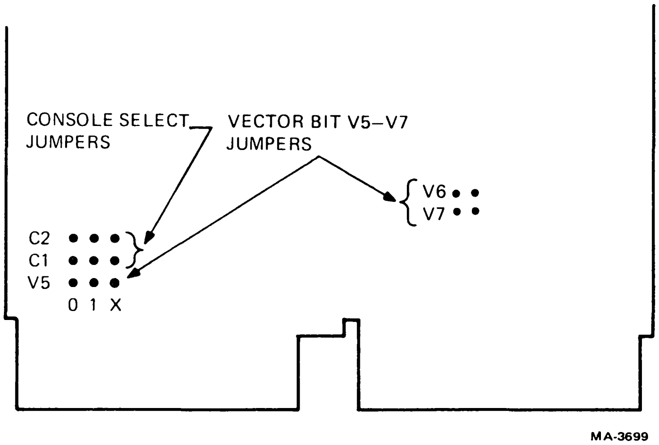


Figure 12. DLV11-J Vector Jumpers

Word Formats

Each of the SLU channels can be configured individually for a word format. This word format includes the number of data bits (7 or 8), number of stop bits (1 or 2), even, odd or no parity (Figure 13). Each channel has its own set of jumper posts which are in the pattern of X, 1, or Ø in columns (Figure 14). Four rows of posts are provided for each channel for even or odd parity (E), number of data bits (D), number of stop bits (S), and for whether parity is inhibited or not (P). Table 5 provides a summary of these configurations.

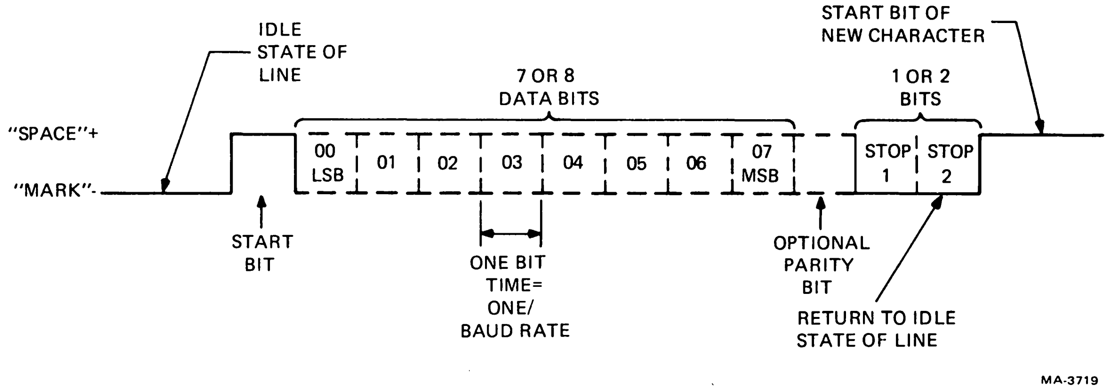


Figure 13. DLV11-J Serial Character Format

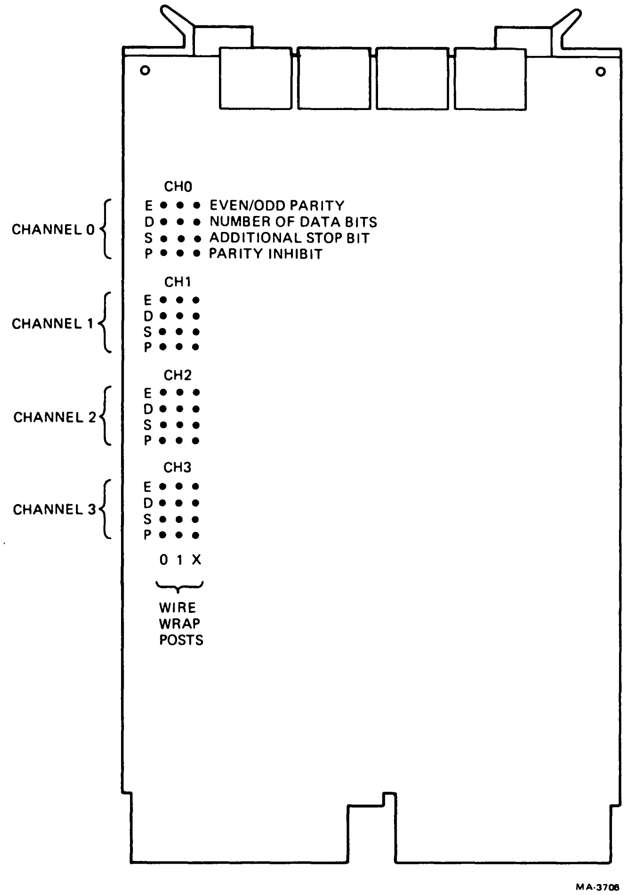


Figure 14. DLV11-J Word Format Jumpers

Table 5. SLU Channel Configuration

Label	Parameter	X To Ø	X To 1
E	Parity	Odd	Even
D	Data Bits	7 Bits	8 Bits
S	Stop Bits	1 Bit	2 Bits
P	Parity (Yes or No)	Yes	No

NOTE

The E jumper must be connected to 1 or Ø, even if parity (P) is disabled.

Baud Rates

Each SLU channel can be configured to any one of the available baud rates. One wirewrap pin is provided for each channel. All the baud rates are available at individual posts (Figure 15). Both the receive and transmit functions of a given channel will operate at the same baud rate. It is not possible to split the baud rate for a channel.

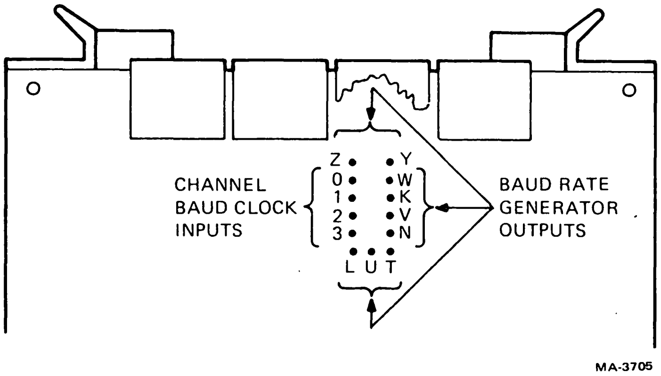


Figure 15. DLV11-J Baud Rate Jumpers

Install a jumper for each channel to the desired baud rate. All channels can use the same baud rate, if necessary. Table 6 shows the posts and baud rates available.

NOTE

If 11Ø baud is required for a 2Ø mA option device, the 11Ø baud is provided by the DLV11-KA 2Ø mA module through its interface connector.

Table 6. Posts and Baud Rates

Wirewrap Post	Baud Rate
U	15Ø
T	3ØØ
V	6ØØ
W	12ØØ
Y	24ØØ
L	48ØØ
N	96ØØ
K	192ØØ
Z	384ØØ

Channel 3 Break Response

The response to pressing the BREAK key on the terminal keyboard depends on which jumper is installed below the V7 jumper posts (Figure 16).

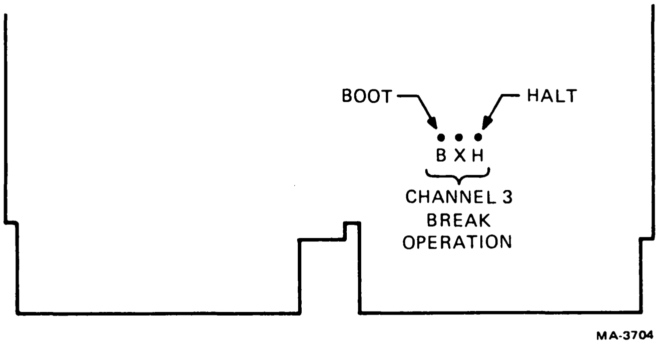


Figure 16. DLV11-J Break Jumpers

When the X post is connected to the B post, the boot function is selected. When BREAK is pressed, the restart operation in the processor can execute the bootstrap program of location 173ØØØ if the processor module is also configured to power-up mode 2.

When the X post is connected to the H post, the halt function occurs, regardless of the power-up mode of the processor. Whenever the processor is halted, the ODT is entered. If no operation is desired, no jumper is installed.

EIA Signal Levels

The area used to configure the signal levels for each channel is shown in Figure 17. Table 7 shows the various configurations and resistors required. Table 8 shows the correspondence between baud rates and resistor values.

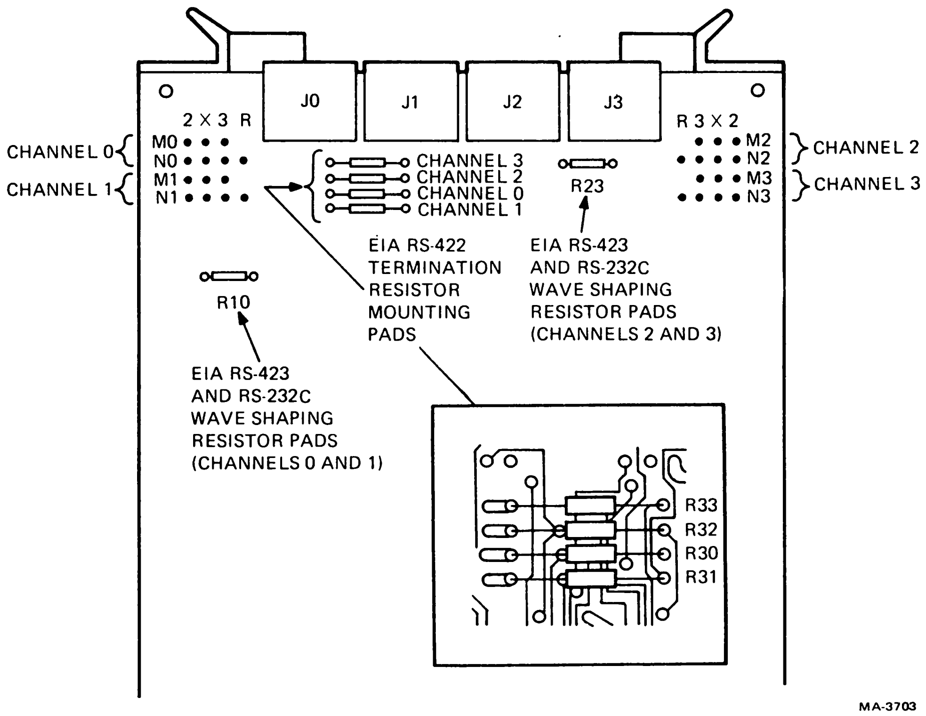

J0
J1
J2
J3
2 X 3 R
R 3 X 2
CHANNEL 0
CHANNEL 1
M0
N0
M1
N1
M2
N2
M3
N3
CHANNEL 2
CHANNEL 3
CHANNEL 3
CHANNEL 2
CHANNEL 0
CHANNEL 1
R23
EIA RS-422 TERMINATION RESISTOR MOUNTING PADS
EIA RS-423 AND RS-232C WAVE SHAPING RESISTOR PADS (CHANNELS 2 AND 3)
R10
EIA RS-423 AND RS-232C WAVE SHAPING RESISTOR PADS (CHANNELS 0 AND 1)
R33
R32
R30
R31
MA-3703

Figure 17. DLV11-J EIA Signal Level Jumpers

Table 7. SLU Signal Level Compatibility Configurations

SLU Channel Modifiers	EIA RS-422	EIA RS-232C and RS-423	2Ø mA Loop (DLV11-KA Option)
M Jumpers	X to 2	X to 3	X to 3
N Jumpers	X to 2	X to 3	X to R for reader capability
Termination Resistor	1ØØ ohm 1/4 W non-wirewound fusible	none	none
Wave-Shaping Resistor (1 for SLUØ and SLU1, and 1 for SLU2 and SLU3)	None	Select from Table 9 1/4 non-wirewound	Select from Table 9 1/4 non-wirewound

Table 8. Baud Rate/Resistor Value Chart

Baud Rate	Resistor Value
38400	22K
19200	51K
9600	120K
4800	200K
2400	430K
1200	820K
600	1 M
300	1 M
150	1 M
110	1 M

INSTALLATION

The DLV11-J module plugs into a two-slot bus connector. Each slot contains 36 lines (18 lines on each side of the module board).

CAUTION

DC POWER MUST BE SHUT OFF WHEN REMOVING OR INSERTING THE MODULE.

ENSURE THAT THE COMPONENT SIDE OF THE MODULE FACES THE SAME DIRECTION AS OTHER LSI-11 SYSTEM MODULES WHEN INSERTING IT INTO THE BACKPLANE.

The interrupt priority of the DLV11-J is determined by its electrical position in the LSI-11 backplane. Be sure to follow the system configuration when inserting the DLV11-J into the backplane. Within the DLV11-J module, the interrupt priority is fixed. The SLU0 receive function has the highest priority. SLU3 receive has the fourth highest priority. The SLU0 transmit function has the fifth highest priority. SLU3 transmit has the lowest priority.

Factory Configuration

The DLV11-J is factory-configured for the following operation:

```
Base Address = 176500
Base Vector Address = 300
SLU3 = Console Device
SLU3 = Halt On Break
Baud Rates:
        SLU0,1, and 2 = 9600
        SLU3 = 300
All Channels:
        Data Bits = 8
        Stop Bits = 1
        Parity = none
        EIA RS-232C/RS-423
        R10,R23 = 22K (2 us)
```

Cabling Considerations

The applications, lengths of cabling, and options available for the DLV11-J module are shown in Figure 18. The definitions of the various cables used are listed in Table 9.

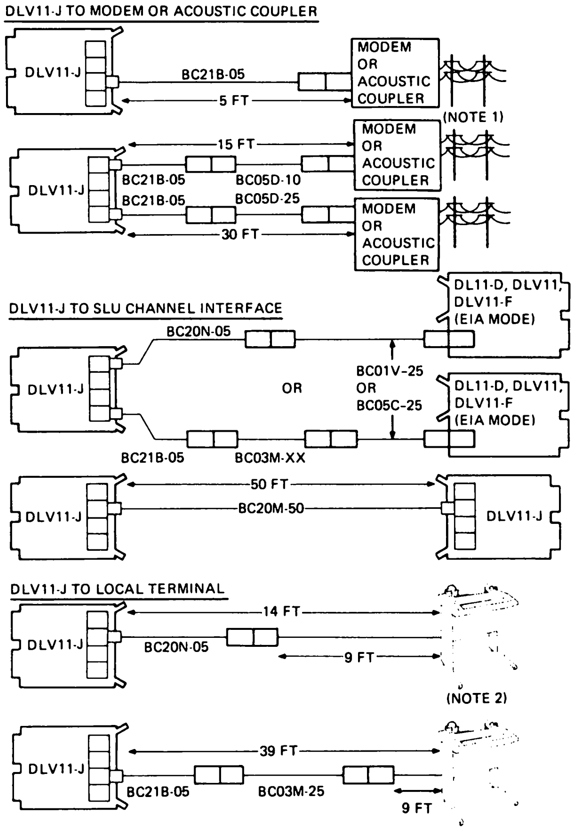
NOTE

"Strapped" (configured) logic levels are provided on data terminal ready (DTR) and request to send (RTS) to allow operation of modems with manual provisions (such as Bell 103A data set with 804B auxiliary set).

When the equipment being interconnected has compatible but different EIA standards, the performance of the channel is limited by the least efficient EIA specifications. Thus, EIA RS-232C/RS-423 interconnections are limited to RS-232C performance capabilities and EIA RS-423/RS-422 interconnections are limited to EIA RS-423 performance capabilities. The relationship between baud rates vs. cabling lengths for EIA RS-422 and RS-423 specifications is shown in Figure 19.

NOTE

When connecting equipment that adheres to RS-232C specifications, the baud rate is limited to 20K with a maximum cable length of 50 feet.


DLV11-J TO MODEM OR ACOUSTIC COUPLER
DLV11-J
BC21B-05
5 FT
MODEM OR ACOUSTIC COUPLER
(NOTE 1)
15 FT
DLV11-J
BC21B-05
BC05D-10
MODEM OR ACOUSTIC COUPLER
BC21B-05
BC05D-25
MODEM OR ACOUSTIC COUPLER
30 FT
DLV11-J TO SLU CHANNEL INTERFACE
DL11-D, DLV11, DLV11-F (EIA MODE)
BC20N-05
DLV11-J
OR
BC01V-25 OR BC05C-25
DL11-D, DLV11, DLV11-F (EIA MODE)
BC21B-05
BC03M-XX
DLV11-J
50 FT
BC20M-50
DLV11-J
DLV11-J TO LOCAL TERMINAL
14 FT
DLV11-J
BC20N-05
9 FT
(NOTE 2)
DLV11-J
39 FT
BC21B-05
BC03M-25
9 FT

NOTES:

1. MODEM USED IS A "MANUAL TYPE" SUCH AS BELL 103A WITH 804B.
2. DEC EIA RS-232C TERMINALS (VT52, LA36, LS120, ETC.) COME EQUIPPED WITH A 9 FT CABLE. NON-DEC EIA RS-232C TERMINALS ARE CONNECTED SIMILARLY EXCEPT 9 FT OF LENGTH MUST BE DEDUCTED FROM THE TOTAL CABLE LENGTH.

MA-3702

Figure 18. DLV11-J Cabling Summary

Table 9. Definitions of Cables

Cable	Application	Length
BC21B-Ø5	Modem or acoustic coupler operation	1.5 m (5 ft)
BCØ5D-1Ø	Extension cable used with BC21B-Ø5	3 m (1Ø ft)
BCØ1V-25	Modem or acoustic coupler operation	7.6 m (25 ft)
BCØ5D-25	Extension cable used with BC21B-Ø5	7.6 m (25 ft)
BCØ5C-25	Modem or acoustic coupler operation	7.6 m (25 ft)
BCØ3M-25	Null modem extension cable used with BC21B-Ø5	7.6 m (25 ft)
BC2ØN-Ø5	Null modem cable for local terminal connection	1.5 m (5 ft)
BC2ØM-5Ø	DLV11-J to DLV11-J operation	15 m (5Ø ft)
H327Ø-A	Four DLV11-J diagnostic loopback plugs, one plug required for each channel. Four required per DLV11-J module to run diagnostic.	

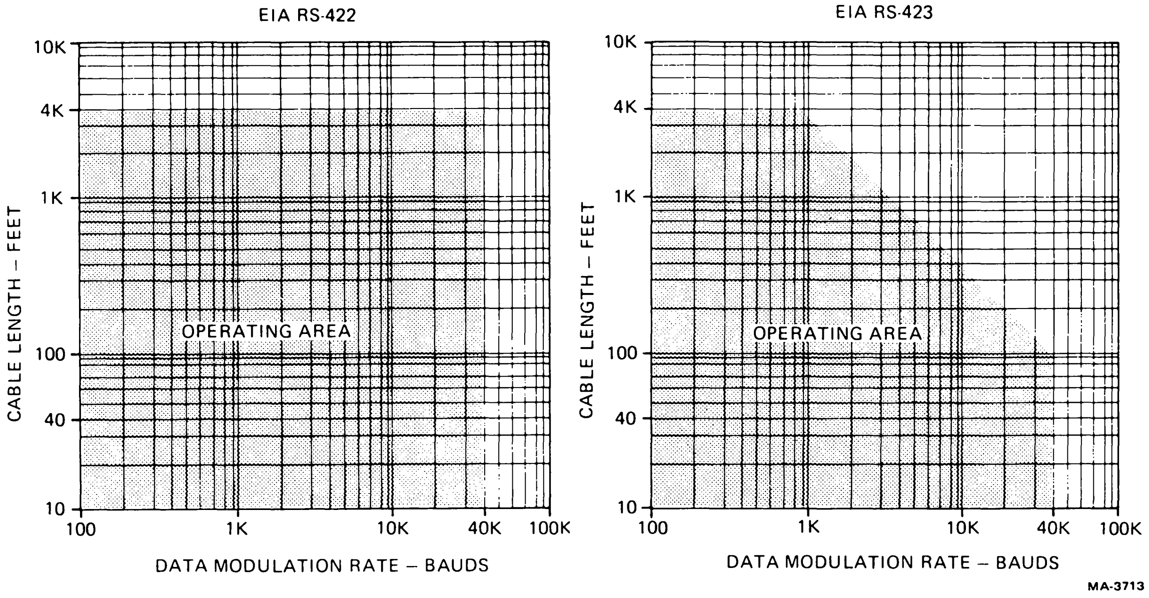


Figure 19. Baud Rate vs. Cable Length

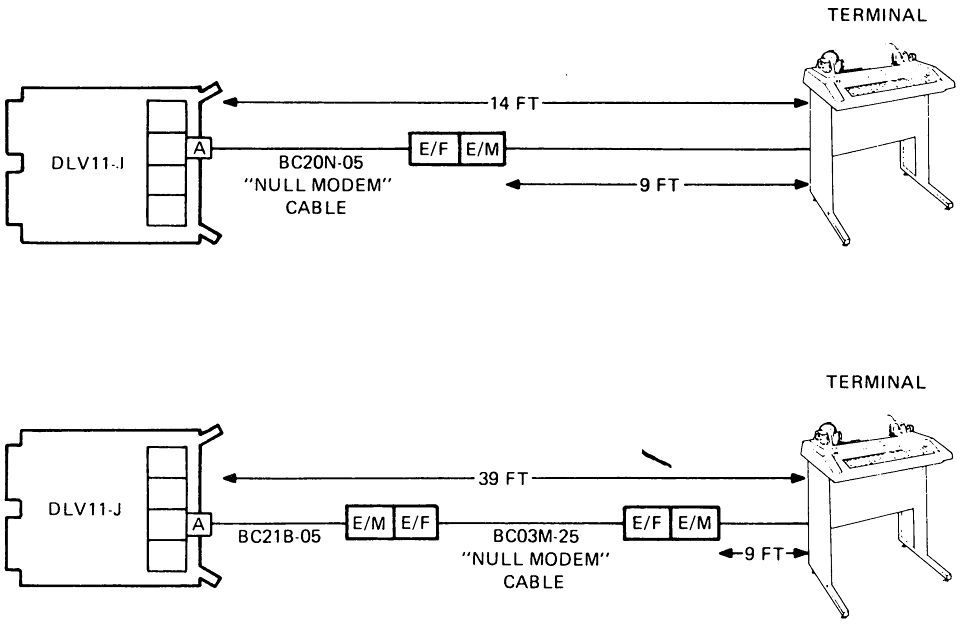
When configuring the channels for slew rate for EIA RS-232C and RS-423, the value of the resistors for two channels may be changed to meet specifications. These are channel Ø and 1 pair, and channel 2 and 3 pair. The highest baud rate of the channel pair limits the cable length of both channels. The factory configuration of the DLV11-J uses a 22K resistor; this allows operation at all baud rates, but limits the cable length to 1ØØ feet.

Local Terminal Cabling

Two methods may be used to connect the DLV11-J to local terminals (Figure 2Ø).

Modem Operation Cabling

The DLV11-J does not monitor EIA control lines from modems. It supplies the modem with a continuous true logic level on both the RTS and DTR control lines. This allows the DLV11-J to operate with modems equipped with manual operation provisions (e.g., Bell 1Ø3A data set with 8Ø4 auxiliary set). Connections to a modem or acoustic coupler device are shown in Figure 21.



NOTES

TERMINALS SHOWN ARE DEC EIA RS-232C TERMINALS (SUCH AS VT52, LA36, LS120, ETC.)

DEC TERMINALS ARE CONSTRUCTED WITH 9 FOOT CABLES, WHEN USING NON-DEC EIA RS-232C TERMINALS DEDUCT 9 FEET FROM THE TOTAL CABLE LENGTH.

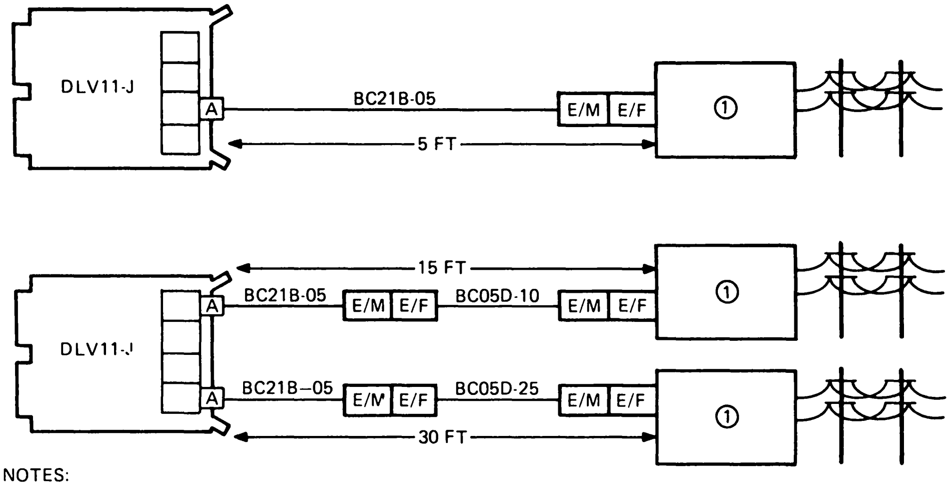
A = 2 X 5 PIN AMP NO 87133-5 CONNECTORS

E/M = EIA RS-232C 25 PIN MALE CONNECTORS

E/F = EIA RS-232C 25 PIN FEMALE CONNECTORS

MA-3700

Figure 2Ø. Local Terminal Cabling



NOTES:

① MODEM OR ACOUSTIC COUPLER. MODEMS SHOWN ARE "MANUAL" MODEMS SUCH AS BELL 103A DATA SETS WITH 804B AUXILIARY SET.

A = 2 X 5 PIN AMP NO 87133-5 CONNECTORS

E/M = EIA RS-232C 25 PIN MALE CONNECTORS

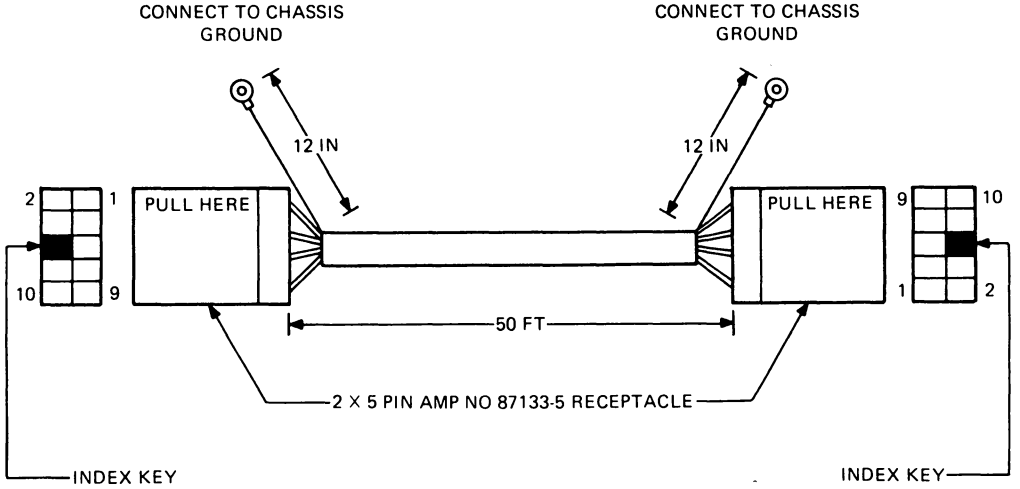
E/F = EIA RS-232C 25 PIN FEMALE CONNECTORS

MA-3712

Figure 21. DLV11-J to Modem or Acoustic Coupler

DLV11-J To DLV11-J Operation Cabling

The BC2ØM-5Ø cable (Figure 22) is used for DLV11-J to DLV11-J connections.


CONNECT TO CHASSIS GROUND
CONNECT TO CHASSIS GROUND
12 IN
12 IN
2
1
10
9
PULL HERE
PULL HERE
9
10
1
2
50 FT
2 X 5 PIN AMP NO 87133-5 RECEPTACLE
INDEX KEY
INDEX KEY

NOTE
BOTH CONNECTORS HAVE THE SAME CABLE RETENTION MECHANISM. CABLE RETENTION IS PROVIDED BY "LOCKING PINS". PULL ON RECEPTACLE TO RELEASE.

MA-3710

Figure 22. BC2ØM-5Ø Cable

DLV11-J To SLU Module Cabling

Serial line units are EIA compatible (DL11-D, DLV11, DLV11-F, etc.) and may be connected to the DLV11-J (Figure 23).

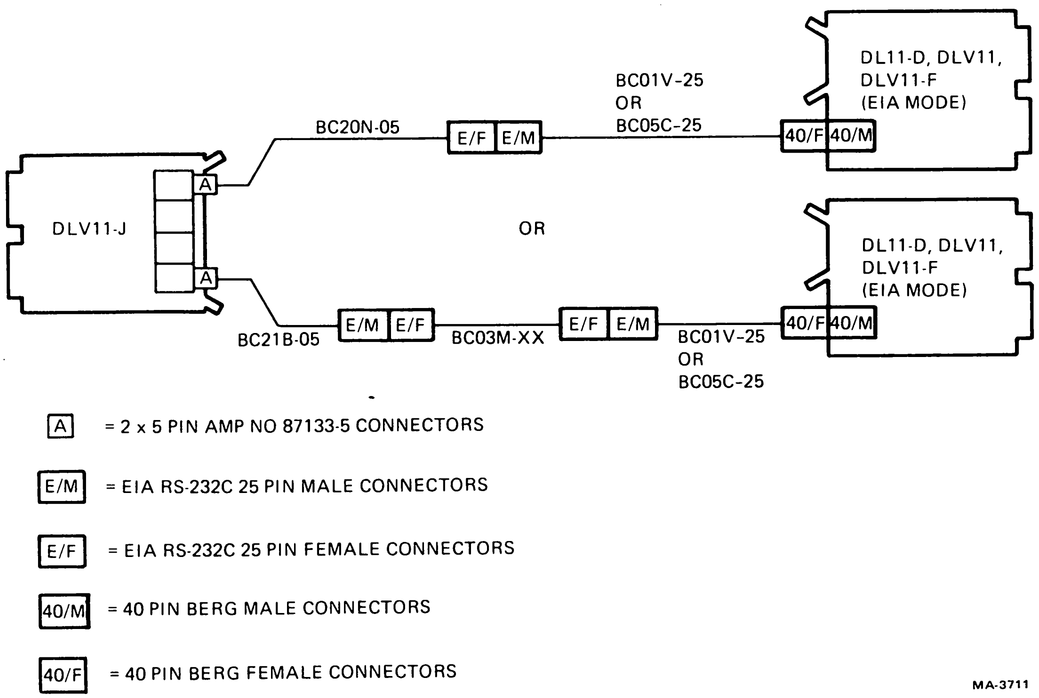

DL11-D, DLV11,
DLV11-F
(EIA MODE)
BC01V-25
OR
BC05C-25
BC20N-05
E/F
E/M
40/F
40/M
A
DLV11-J
OR
A
DL11-D, DLV11,
DLV11-F
(EIA MODE)
E/M
E/F
E/F
E/M
40/F
40/M
BC21B-05
BC03M-XX
BC01V-25
OR
BC05C-25
A = 2 x 5 PIN AMP NO 87133-5 CONNECTORS
E/M = EIA RS-232C 25 PIN MALE CONNECTORS
E/F = EIA RS-232C 25 PIN FEMALE CONNECTORS
40/M = 40 PIN BERG MALE CONNECTORS
40/F = 40 PIN BERG FEMALE CONNECTORS
MA-3711

Figure 23. DLV11-J to SLU Module Cabling

Diagnostics

A diagnostic program is available to verify proper operation of the DLV11-J module. Any LSI-11 based system with at least 4K of memory will support the diagnostic. Loopback plugs must be inserted into the three device connectors so that data loopback tests can be performed with the console terminal connected to the fourth, SLU3.

CAUTION

DC POWER MUST BE OFF WHEN INSERTING THE 327Ø-A LOOPBACK PLUGS.

The diagnostic has two sections. The first section tests the channels individually by the use of register bit tests. The second section tests the four channels for interaction, that is, correct interrupt contention and correct buffer loading. The buffers are checked to ensure that no channel interaction occurs during data transfers. A detailed description of the diagnostic is presented in the section on Troubleshooting.

EXERCISE

Circle the letter of the correct response. You may use any references. Refer to Figure 24 to solve questions 2 through 5. Check your answers with those provided on the Solutions page.

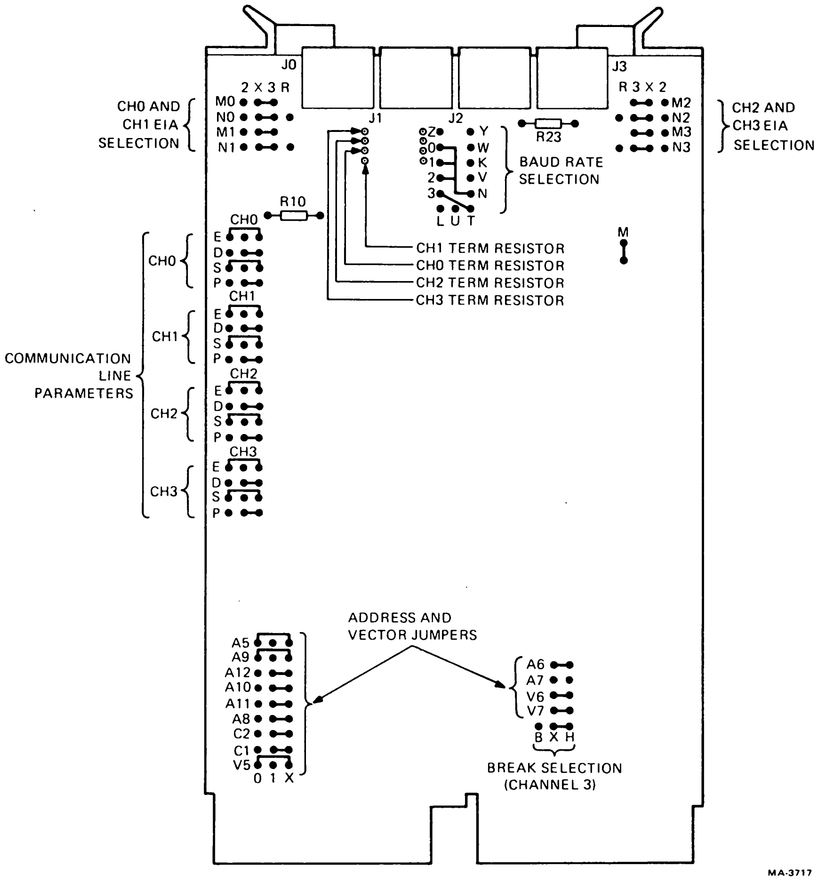


Figure 24. DLV11-J Module with Jumpers (Exercise)

1. To set up the character format for 8-bits for SLU3 channel, which posts are jumpered in the SLU3 section?

   a. P X to Ø
   b. D X to Ø
   c. E X to 1
   d. D X to 1
   e. P X to 1

2. The base address configured is:

   a. 1775ØØ
   b. 17756Ø
   c. 17654Ø
   d. 1765ØØ
   e. 17751Ø

3. The vector address configured is:

   a. 3ØØ
   b. 31Ø
   c. Ø6Ø
   d. Ø64
   e. 32Ø

4. SLU3 will be used as the console termination channel.

   a. True
   b. False

5. Pressing the BREAK key on the console keyboard will cause the CPU to boot from location 173ØØØ.

   a. True
   b. False

SOLUTIONS

1. d

2. d

3. a

4. a

5. b

PROGRAMMING

This section explains the programming aspects of the DLV11-J module. Understanding the bit assignments of the control/status registers and how the data buffer registers operate will enable you to write short maintenance routines to check out the DLV11-J or devices connected to it. When the diagnostic programs print out error messages, they often contain the actual register contents and the expected contents.

There are four registers associated with each channel. Two of them function in the receive operation and two of them in the transmit operation. In each case, it is necessary to control the operation, to allow the processor to obtain the status at the end of an operation, and to transfer characters to and from the device.

The register used to control the operation and also have status information available for the processor is called the Control/Status Register (CSR). The register used to temporarily store the character is called the Data Buffer (BUF). The two registers associated with the receive function are abbreviated as RCSR and RBUF, and those with the transmit function as XCSR and XBUF.

Register Addresses

Although the registers of the individual channels will have different bus addresses, the last octal digit will always be the same for the same register function:

Address	Register	Function
XXXXXØ	RCSR	Receive Control/Status
XXXXX2	RBUF	Receive Data Buffer
XXXXX4	XCSR	Transmit Control/Status
XXXXX6	XBUF	Transmit Data Buffer

When the base address is configured with the jumpers on the DLV11-J module, the 16 registers of the four channels are in sequence. Thus, if the SLUØ base address is 1765ØØ, the first SLU1 address is 17651Ø, SLU2 is 17652Ø, and SLU3 is 17653Ø. The SLU2 XCSR address is 176524.

The vector address for SLUØ is 3ØØ for the receive function and 3Ø4 for the transmit function. These addresses will also continue in sequence for the other SLUs.

When SLU3 is jumpered to act as the console terminal interface, its registers will be assigned the normal console interface addresses. These addresses are:

Address	Register
17756Ø	RCSR
177562	RBUF
177564	XCSR
177566	XBUF

The vector addresses for console interface are 60 and 62 for the receive function and 64 and 66 for the transmit function.

Receive Control/Status Register (RCSR)

The bit assignments for the RCSR are shown in Figure 25. As you can see, only three bits are used. Bit Ø is only used with the 2Ø mA current loop option; it is used to advance paper tape one character at a time on the LT33 terminal.

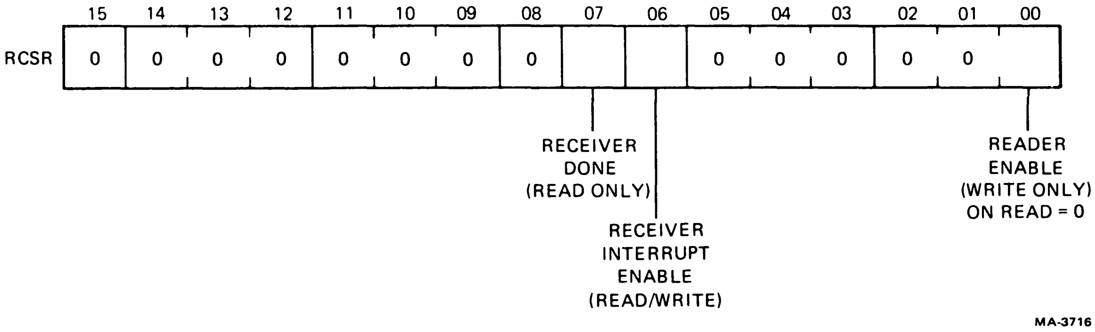

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
RCSR
0 0 0 0 0 0 0 0 0 0 0 0 0
RECEIVER DONE (READ ONLY)
RECEIVER INTERRUPT ENABLE (READ/WRITE)
READER ENABLE (WRITE ONLY) ON READ = 0
MA-3716

Figure 25. Receive Control/Status Register (RCSR) Bit Assignments

Bit 7 is assigned the Receive Done function. It is set by the DLV11-J when an entire character has been received and is ready for input to the CPU. It is automatically cleared when the RBUF is read, when BINIT L goes true (low), or when bit Ø is set.

Bit 6 is the Receive Interrupt Enable bit. When it is set by the program, the DLV11-J is allowed to interrupt the CPU when a character is ready for input to the CPU (bit 7 becomes set). Bit 6 can be cleared by the program or by the BINIT signal.

Receive Data Buffer Register (RBUF)

The bit assignments for the RBUF are shown in Figure 26. This register contains the character and error information from the UART. The lower byte (bits Ø7-ØØ) contains the 7- or 8-bit character, right-justified. Bits 11-Ø8 are not used. Bit 12 is the parity error bit, with a set condition indicating a parity error. If no parity is used, it is always a Ø. Bit 13 is the framing error bit, which means that no valid stop bit was received. Bit 14 is the overrun error bit. When set, it indicates that the last character received was not read by the CPU before the new character was received. Error bits are cleared by the BINIT signal, and are updated with each new character received.

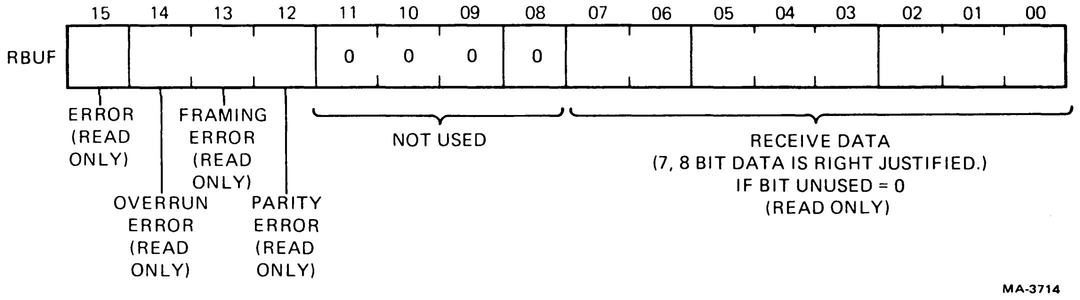

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
RBUF
0 0 0 0
ERROR (READ ONLY)
FRAMING ERROR (READ ONLY)
OVERRUN ERROR (READ ONLY)
PARITY ERROR (READ ONLY)
NOT USED
RECEIVE DATA (7, 8 BIT DATA IS RIGHT JUSTIFIED.) IF BIT UNUSED = 0 (READ ONLY)
MA-3714

Figure 26. Receive Data Buffer Register (RBUF) Bit Assignments

Transmit Control/Status Register (XCSR)

The transmit registers are shown in Figure 27. The XCSR uses only three bits, 7, 6, and Ø.

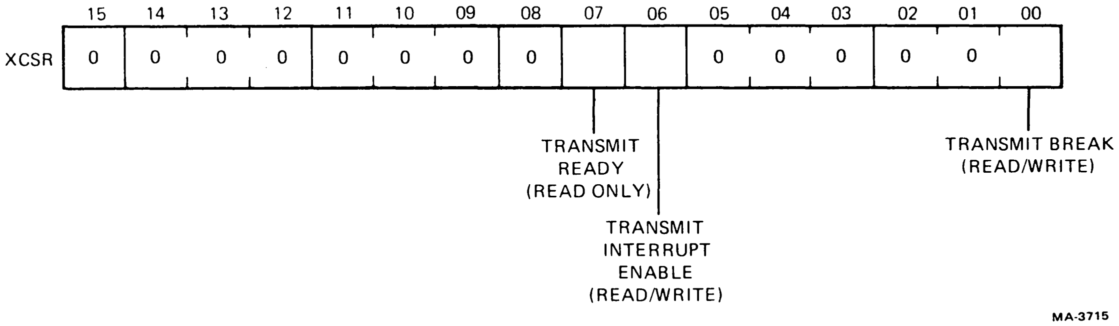

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
XCSR
0 0 0 0 0 0 0 0 0 0 0 0 0
TRANSMIT READY (READ ONLY)
TRANSMIT INTERRUPT ENABLE (READ/WRITE)
TRANSMIT BREAK (READ/WRITE)
MA-3715

Figure 27. Transmit Control/Status Register (XCSR) Bit Assignments

Bit 7 is the Transmit Ready bit. When set, bit 7 indicates the XBUF is empty and can accept another character for transmission. It is also set by BINIT.

Bit 6 is the Transmit Interrupt Enable bit. It is set under program control when the DLV11-J is allowed to interrupt the CPU whenever bit 7 is set. The bit is cleared by the CPU or the BINIT signal.

Bit Ø is the Transmit Break bit, and it is set and cleared by program control. When set, a continuous space level is transmitted, which is the same as a break condition in the transmit lines. However, transmit done and interrupt enable can still operate, so that the break is software-controlled. When it is not set, normal character transmission will take place. It is also cleared by the BINIT signal.

Transmit Data Buffer Register (XBUF)

The XBUF register uses only the lower byte, bits Ø7-ØØ, which will contain the 7 or 8 data bits, right-justified, of the character to be transmitted.

EXERCISE

Circle the letter of the correct response. You may use any references. Check your answers with those provided on the Solutions page.

1. An address of 177562 on the bus is used to access the:

   a. Channel Ø RBUF
   b. Console RBUF
   c. Channel 2 XBUF
   d. Console XBUF
   e. Console RCSR

2. Bit 6 of the register accessed by address 177564 functions as the:

   a. Receive Done bit
   b. Receive Interrupt Enable bit
   c. Transmit Ready bit
   d. Transmit Interrupt Enable bit
   e. Receive Framing Error

3. An address of 176544 on the bus would access the:

   a. Channel 3 XCSR
   b. Channel 2 XCSR
   c. Channel 1 XCSR
   d. Channel Ø XCSR
   e. Console XCSR

4. If address 177562 is read, and its contents are 11Ø315:
   a. An overrun error has occurred.
   b. No error has occurred.
   c. A framing error has occurred.
   d. A parity error has occurred.
   e. The character M was transmitted.

5. Which of the following statements indicates that the channel 1 Transmit Ready bit being set can cause an interrupt in the CPU?

   a. Address 17651Ø contains ØØØØ1ØØ.
   b. Address 176514 contains ØØØØ1ØØ.
   c. Address 177564 contains ØØØØ3ØØ.
   d. Address 1765Ø4 contains ØØØØ1ØØ.
   e. Address 176514 contains ØØØØ2ØØ.

6. The octal word ØØØØ1ØØ is written into address 17653Ø. Which statement is true?

   a. Console channel can interrupt when it is ready to transmit next character.

   b. SLU3 channel can interrupt when it is ready to transmit next character.

   c. SLU3 channel can interrupt when it is ready to send CPU next character.

   d. Console channel can interrupt when it is ready to send CPU next character.

   e. SLU3 channel cannot interrupt the CPU.

SOLUTIONS

1. b

2. d

3. d

4. d

5. b

6. c

TROUBLESHOOTING

Any malfunctions that point to the DLV11-J module, when it is first tried in a system, could indicate either cable connection problems or improper jumper configurations. If nothing is found, run the diagnostic.

Physical Problems

Cable connections should be checked by looking for bent pins or broken wires at the connectors. Jumper configurations should be checked against a system listing for the DLV11-J jumpers required. The DLV11-J module is always received in a factory-configured mode.

Diagnostics Program

As described in the Installation section, a diagnostic program is available to verify proper operation of the DLV11-J module. It will run on any LSI-11 based system which contains at least 4K of memory. If the data loopback tests are to be performed, an H327Ø-A diagnostic loopback plug must be inserted into the device connectors, with the exception of the console connector. The system should be powered down when the device cable connectors are removed and the loopback plugs are inserted.

The following program specifics apply:

PROGRAM TITLE - CVDLA?? DLV11-J TEST
DOCUMENT LISTING NUMBER - AC-E188A-MC
MICROFICHE LISTING NUMBER - AH-E189A-MC
PAPER TAPE - AK-E19ØA-MC

The diagnostic consists of two phases:

1. All selected channels are tested individually.

2. All selected channels are tested for channel interaction to the logic level (not chip level).

The diagnostic can test up to two DLV11-J modules when they are configured for consecutive addresses. Unless otherwise specified, the diagnostic will do auto-sizing and test all channels. The operator can select the modules and channels to be tested, in which case the program will bypass the auto-sizing mode and test only those channels selected.

The default addresses and vectors are:

177560 - Console interface address

1765ØØ - SLU channel Ø address (first of up to eight consecutive devices)

6Ø - Vector address for console interface

3ØØ - Vector address for SLU channel Ø (first of up to eight devices)

Before running this diagnostic the CPU, memory, and bus must be fully operational.

After the diagnostic has been loaded into memory, two word locations can be initialized. The first is the Software Switch Register (SWREG) with the following options:

Bit Set	**Octal**	**Function**
15	1ØØØØØ	Halt on Error
14	4ØØØØ	Loop on Test (Used in Progress)
13	2ØØØØ	Inhibit Error Typeouts
12	1ØØØØ	Enable Performance Reports
11	4ØØØ	Inhibit Iterations
1Ø	2ØØØ	Bell on Errors
9	1ØØØ	Loop on Errors
8	4ØØ	Loop on Test in SWREG <7:Ø>
7:Ø		Number of Test to Loop On (Used with Bit 8). All tests preceding the selected one are executed once only.

The Software Switch Register contents will be displayed as soon as the diagnostic program execution begins. If no change is desired, press <CR> (Carriage Return). If a change is desired, enter the octal numbers by following the above options. When <CR> is pressed, the contents of the register will reflect your choice. If a mistake is made, a question mark is printed or displayed, followed by a carriage return and line feed. The location of the Switch Register is 176. This location can be opened by using ODT methods (after @, enter "176/", and the contents will be displayed). An easier way to display the Switch Register is to use Control G (press CTRL and G at the same time). This is covered in the upcoming Lab Exercise.

$DEVM (Location 1252)

The $DEVM location contains a bit map which can be used to select which module and channels should be tested during the diagnostic. The change in the bit pattern should be made before the program is started, or all channels will be tested. Figure 28 shows the assignments in the bit map.

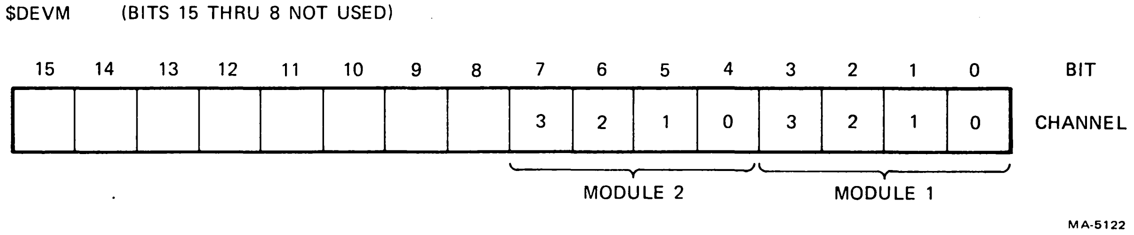


Figure 28. $DEVM Bit Assignments

If the $DEVM is changed, the program must be restarted at 2ØØ. Otherwise the contents of $DEVM will be ignored and complete testing of all channels will take place.

Power Fail

Auto start from power fail is not implemented in this program.

Error Information

The error format output is as follows:

TEST #___ERROR#___PC=___ADDRESS=___VECTOR=___

All values are in octal. Address and vector refer to the failing channel. The test number, error number, and PC values are used to direct you to the proper place in the diagnostic listing.

The setting of bits 15, 13, 1Ø, and 9 of the SWREG determines what will happen when an error is detected:

15 - Diagnostic will halt in error routine. Program can be continued from where it halted.

13 - Disables printing of error message.

1Ø - Causes bell to ring on error or "beep" in video terminal.

Ø9 - Causes diagnostic to loop from beginning of test to error.

The Control G function will work during the error routine. This allows you to stop the diagnostic and change the contents of the SWREG.

Performance Reports

When bit 12 is set in the SWREG, the performance report mode is entered. As each channel completes one pass of the diagnostic, the report is displayed or printed. After all channels and modules have been tested successfully, an end pass statement is typed. Figure 29 shows the display for one DLV11-J module. Table 1Ø summarizes the tests performed in the DLV11-J diagnostic.

```
CVDLAA1 DLV11-J TEST

SWREG= ØØØØØØ   NEW= 1ØØØØ <CR> (ENABLES REPORTS)

WILL TEST:

MODULE 1        CHANNEL Ø  1  2  3

                ** PHASE 1 SUMMARY **

CSR:  17650Ø, VECTOR: ØØØ3ØØ, ERRORS:  Ø
CSR:  17651Ø, VECTOR: ØØØ31Ø, ERRORS:  Ø
CSR:  17652Ø, VECTOR: ØØØ32Ø, ERRORS:  Ø
CSR:  17756Ø, VECTOR: ØØØØ6Ø, ERRORS:  Ø

                ** PHASE 2 SUMMARY **

CSR:  1765ØØ, VECTOR: ØØØ3ØØ, ERRORS:  Ø

END PASS  #   1
```

Figure 29. Performance Reports

Table 10. DLV11-J Diagnostic Tests

Phase 1 Tests	
Test 1	Addressability: This test verifies that all four registers in a channel respond to their addresses.
	The next three tests will test all read/write bits.
TEST 2	BREAK TCSR0 SET, CLEAR, RESET
TEST 3	XMITIE TCSR6 SET, CLEAR, RESET
TEST 4	RCVRIE RCSR6 SET, CLEAR, RESET
TEST 5	XMIT RDY TCSR7 IS SET BY INIT
TEST 6	XMIT RDY TCSR7 CLEARS WHEN XMIT BUFFER IS LOADED AND THAT IT SETS WITHIN A REASONABLE AMOUNT OF TIME
TEST 7	RCVRDONE RCSR7 (REQUIRES WRAPAROUND) OUTPUTTING A CHARACTER FROM XMIT BUFFER RESULTS IN RCSR7 SETTING WITHIN A REASONABLE AMOUNT OF TIME, AND RESET CLEARS THE BIT
TEST 10	RCSR7 IS CLEARED BY SETTING RCSR0
TEST 11	RCSR7 IS CLEARED BY READING RBUF
TEST 12	RBUF14 AND 15 OVERRUN AND ERROR BIT
TEST 13	XMIT INTERRUPT LOGIC TEST (4 TESTS) 1. DOES XMIT INTERRUPT LOGIC WORK? 2. AT PRIORITY OF 0? 3. AND ONLY ONCE? 4. BUT NOT WITH INTERRUPT ENABLE CLEAR
TEST 14	RECEIVE INTERRUPT LOGIC TEST
TEST 15	TEST DATA WRAPAROUND (FLAG MODE)
TEST 16	TEST DATA WRAPAROUND (INTERRUPT MODE)
TEST 17	TEST BREAK GENERATION LOGIC BY XMITTING A KNOWN CHARACTER 1. XMIT CHARACTER WITH BREAK SET AND COMPARE RECEIVED WITH 0 2. TEST FOR FRAMING ERROR ON BREAK 3. IF PARITY ENABLED AND ODD IS SELECTED, CHECK TO SEE THAT ERROR WAS GENERATED 4) IF PARITY ENABLED AND EVEN SELECTED, CHECK TO SEE THAT NO ERROR OCCURRED.
TEST 20	NOT A DIAGNOSTIC TEST, SEND BACK TO LOOP

Phase 2 Tests	
TEST 21	CHECK FOR CHANNELS INTERRUPTING AT THEIR ASSIGNED PRIORITY
TEST 22	TEST DATA TRANSFERS WITH ALL ACTIVE LINES INTERRUPTING

EXERCISE

Circle the letter of the correct response. You may use any references. Check your answers with those given on the Solutions page.

1. Problem: There is no communication between the CPU and the console terminal when a spare DLV11-J is tried. The console has been working properly. Power has been applied and indications show no power problem. Which of the following steps should be taken first?

   a. Check jumpers CØ and C1.
   b. Check the channel 3 P jumper.
   c. Check the channel 3 S jumper.
   d. Check the channel Ø D jumper.
   e. Check the channel Ø P jumper.

2. If the Switch Register (SWREG) contains 12ØØØ when the diagnostic program begins, which of the following will occur?

   a. Halt on error and inhibit error typeouts
   b. Enable reports and ring bell on error
   c. Loop on Test #2
   d. Inhibit error typeouts
   e. None of the above

3. If you write 12 into location 1252 after loading in the DLV11-J diagnostic, what will occur when you run the diagnostic?

   a. Test #12 will be repeated indefinitely.
   b. Only channel 1 and 2 of module 2 will be tested.
   c. Only channel 1 and 2 of module 1 will be tested.
   d. Halt on error and inhibit error typeouts.
   e. Only the console channel and channel 1 of module 1 will be tested.

4. Which of the following entries into SWR will cause halt on error, inhibit error typeouts, enable performance reports, and beep on errors?

   a. Ø23ØØØ
   b. 1Ø3ØØØ
   c. ØØ3ØØØ
   d. 132ØØØ
   e. 123ØØØ

EXERCISE (Cont)

5. Which of the following problems is the most likely cause of the error printout shown?

```
TEST #7 ERROR  #11 PC=ØØ456Ø  ADDRESS=1765ØØ  VECTOR=3ØØ
```

   a. Console not connected to DLV11-J
   b. Wraparound plug missing on SLUØ connector
   c. Wraparound plug missing on SLU1 connector
   d. Failure in SLU2 transmit logic
   e. None of the above

6. The simplest method to use for looking at the SWR contents and changing them is to:

   a. Depress CTRL and C at the same time.
   b. Depress BREAK and open location 1252.
   c. Power system down and reboot XXDP monitor.
   d. Depress CTRL and S at the same time.
   e. Depress CTRL and G at the same time.

SOLUTIONS

1. a

2. b

3. e

4. d

5. b

6. e

LAB EXERCISE

To do this Lab Exercise on the system, you will need an XXDP diskette, DLV11-J installed with console, and three wraparound plugs connected on SLUØ, 1, and 2.

Check off each step as you complete it. Write in answers or results when requested. Check your answers with those given on the Solutions page.

___ 1. Boot the system with XXDP diskette.

___ 2. Display directory by entering D <CR> after the dot, which is called the XXDP monitor prompt character. The program is ready for an operator entry.

___ 3. Load and run the DLV11-J diagnostic by entering R VDLA?? <CR> after the dot. The question marks allow use of all revisions of the diagnostic program.

___ 4. When SWR=ØØØØØØ NEW= is displayed, default (no entry) by pressing <CR>. This will keep SWR=ØØØØØØ, or cause no change in contents. Program should now begin execution.

___ 5. What is being tested according to the auto-sizing routine display? ______________________________

___ 6. After END PASS #2 is displayed, stop the diagnostic by pressing BREAK.

___ 7. Look at location 1252, by entering 1252/ after the @ prompt character of the ODT. This location contains the bits of the $DEVR which determine what channels are to be tested. What are its contents?

____

This was entered by the auto-sizing routine.

Which channels and module are to be tested?

____

___ 8. Begin the diagnostic again by entering 2ØØG after the @ symbol. Were you given the chance to change the SWR? ______________________

___ 9. Stop diagnostic be pressing BREAK.

___ 1Ø. After @, enter XXDP monitor restart address of 152262, followed by G (for GO). What is the result? ____________________

LAB EXERCISE (Cont)

___ 11. After the dot, you must again enter R VDLA?? <CR> to load and run the diagnostic.

___ 12. Set bit 12 in SWR by entering 10000 <CR>. What is the function of bit 12? ______________________

___ 13. Note display. After END PASS #1 is displayed, keep pressing CTRL and G together until the program accepts it. What is the result?

____

___ 14. Remove the SLU0 wraparound plug and change the contents of SWR to all 0s, which restarts program execution.

___ 15. What is the result? ______________________

___ 16. Press BREAK and enter the XXDP monitor restart address of 152262G and load in the diagnostic again.

___ 17. When the chance to change SWR is offered, press BREAK.

___ 18. Now open location 1252 by typing in 1252/. The contents of 1252 are now displayed. Write in new contents by typing 14<CR>. What channels are now selected? ________________

___ 19. Enter 200G to start the diagnostic. What channels were selected? ______________________

___ 20. After END PASS #1 is displayed, press BREAK.

___ 21. Change location 1252 to 40. What module and channel did you just select? ________________

___ 22. Enter 200G to start the diagnostic. Notice the result. Why did the error result?

____

___ 23. What is displayed on the bottom two lines?

The CPU halted with 10 in the PC, which means it executed a HALT instruction at location 06 where it was sent by the instruction at location 04. The CPU ended up at location 4 (trapped to 4) because of a bus time out.

___ 24. Change location 1252 to all 0s.

LAB EXERCISE (Cont)

____ 25. Enter 2ØØG and then immediately press CTRL and G.

____ 26. Set the bits in SWR to halt and ring bell on error. What octal entry must be made?

____

____ 27. What is the result? Did terminal "beep" on the error? _______ In what test did the program halt? ________ What channel has the fault? _______ Why?

____

____ 28. Replace wraparound plug and check DLV11-J for proper operation by running the diagnostic, starting at 2ØØG.

____ 29. After program runs, press BREAK and look at location 176 (SWR). What is the result?

____

____ 3Ø. Write all Øs to this location.

____ 31. Run program again by entering 2ØØG. You should now observe diagnostic being executed as in Step 4.

____ 32. Press BREAK to stop diagnostic. Power down system and power up again to re-boot XXDP monitor.

____ 33. Load and run the DLV11-J diagnostic in normal default mode to refresh yourself in the normal routine. After END PASS #2 is displayed, press BREAK to stop the program. Power down and remove the diskette.

SOLUTIONS

5. Module 1 - SLU Ø, 1, 2, 3

7. ØØØØ17

   Module 1 - SLU Ø, 1, 2, 3

8. No.

1Ø. Prompt character "." displayed.

12. Enable performance reports.

13. SWR = Ø1ØØQP`ØØ displayed. You now have the opportunity to change the SWR contents.

15. Test error numbers 14 and 15 with other data displayed. Entered ODT mode, since we see @ is displayed.

18. Module 1, SLU 2 and 3.

19. Module 1, SLU 2 and 3.

21. Module 2, SLU channel 1.

22. No module 2 in the system.

23. ØØØØ1Ø

    @

    The CPU halted with 1Ø in the PC which means it executed a HALT instruction at location Ø6. It was sent here from location Ø4. The CPU ended up at location Ø4 (trapped to Ø4) because of a bus time out. A nonexistent device was addressed.

26. 1Ø2ØØØ

27. Yes

    Test #25

    SLUØ

    Wraparound plug is still out.

29. Read out 1Ø2ØØØ which is the SWR contents.

See the Course Administrator when you finish the Lab Exercise. He or she will give you the Module Test for this module.

PDP-11V23/11T23 SYSTEM MAINTENANCE

BDV11-AA BOOT/TERMINATOR

BDV11-AA Boot/Terminator

INTRODUCTION

The purpose of the Overview section in this course module is to acquaint you with the BDV11-AA. For many of you, this may be the first time you have even heard of this device. We will familiarize you with the BDV11-AA and some of its uses.

The Operation section will give you an idea of how the device operates by providing you with a functional description.

The Programming section will familiarize you with the hardware registers and their bus addresses as well as with the function performed by the individual bits within the registers.

The Configuration section will familiarize you with each switch and jumper function.

Finally, the Theory of Operation section will give you some additional details on material covered in previous areas. Other subjects to be covered include diagnostics, interpretation of diagnostic light displays and diagnostic printouts, and loading of user ROMS/EPROMS.

OBJECTIVES

1. Identify BDV11-AA characteristics and functions by completing statements concerning them.

2. Identify the BDV11-AA ROM locations by matching a list of the ROMs to a line drawing of the BDV11-AA.

3. Identify the major functions of the BDV11-AA ROMs by matching the ROM socket identifier to the ROM function.

4. Locate and identify the switches, tip jacks, lights and indicators on the BDV11-AA by matching a list of those items to a line drawing of the BDV11-AA.

5. Identify the function of the switches, tip jacks, lights, and indicators on the BDV11-AA by matching each item to a list of its functions.

6. Identify the characteristics and functions of the BDV11-AA hardware registers by matching items on lists of characteristics and functions to the correct registers.

7. Select the ROM socket number when given the bus address and page number.

8. Demonstrate an understanding of the methods used to configure the BDV11-AA specific function performance by matching the function to the switch and jumper configurations.

9. Using statements about BDV11-AA diagnostic operation and interpretation, select the correct definition for each.

SAMPLE TEST ITEMS

1. The BDV11-AA has _____ words of memory space.

   a. 4K
   b. 8K
   c. 16K
   d. 22K

2. Check the letter given in the figure that identifies a pair of the BDV11-AA system ROMs.

   a. _____
   b. _____
   c. _____
   d. _____

3. Match the ROM functions to the ROM sockets used for those functions.

	ROM Sockets		ROM Functions
_____	XE53/XE48	a.	2K system ROM
_____	XE52/XE36	b.	2K diagnostic/bootstrap (reserved for DEC use)
_____	XE58/XE44	c.	1K EPROM
_____	XE43/XE46	d.	2K diagnostic/bootstrap (reserved for future use by DEC)

4. Write into the space provided, the letter from the figure that matches the part names listed.

   _____ DIP switch E21
   _____ Halt/Enable switch
   _____ Diagnostic light display
   _____ Restart switch
   _____ DIP switch E15
   _____ Tip jack test points

5. The switch that causes the CPU to automatically carry out a power-up sequence is:

   a. the BEVNT L switch
   b. the Restart switch
   c. the Halt/Enable Switch
   d. E15-A3
   e. E21-B5

6. The Display Register contains:

   a. 1 bit
   b. 4 bits
   c. 12 bits
   d. 16 bits

7. To load the PCR for ROM pages 264 and 265, what octal value would you use?

   a. 264265
   b. 265264
   c. 132664
   d. 130660

8. What switch must be turned on to execute the memory test on powerup or restart?

   a. A1
   b. A2
   c. A3
   d. A4

9. When booting up the BDV11-AA diagnostics on XXDP media, you would type ________ on the console terminal.

   a. 000200
   b. START
   c. 177550L
   d. 173000G

RESOURCES

Optional

BDV11 Bus Terminator, Bootstrap and Diagnostic ROM Technical Manual, EK-BDV11-TM-001

Equipment

1. XXDP diagnostic monitor
2. VM8A.BIC diagnostic

OVERVIEW

The BDV11-AA is a quad-height LSI-11 bus compatible option. Its logic components are mounted on a quad-height printed circuit board. The BDV11-AA is known as a Bootstrap/Terminator/Diagnostic module.

As a bootstrap the BDV11-AA contains the firmware necessary to load initial programs off a preselected group of peripherals. As a terminator, it provides 12Ø ohm termination for the LSI-11 bus signal lines. As a diagnostic tool, the BDV11-AA provides the firmware diagnostics programs necessary to do a preliminary verification of the CPU, memory, serial line unit and the bootstrapped peripheral. These firmware programs are stored in ROM memory. The diagnostic programs are optionally run when the system is booted. The BDV11-AA also provides a program-controlled line clock. Figure 1 shows the overall component side of the BDV11-AA module, including the 24 sockets for ROM DIPs.

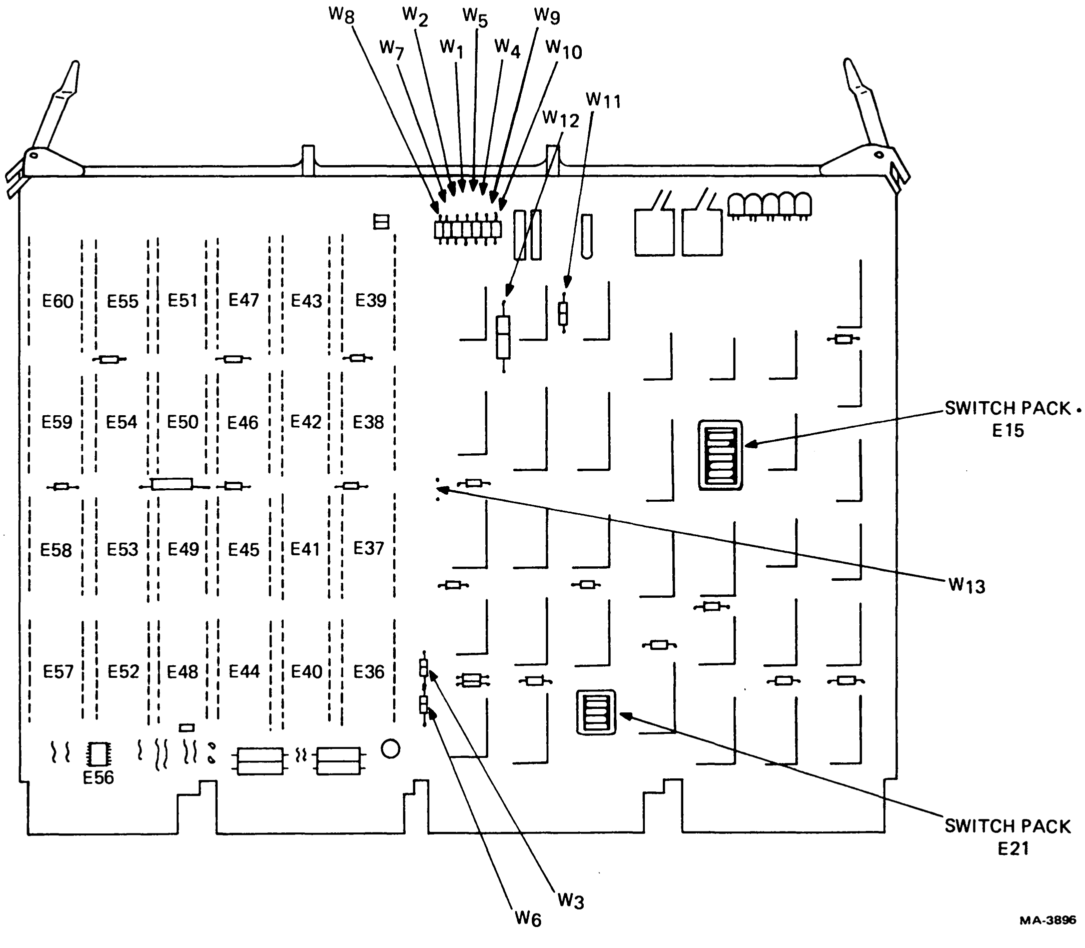


Figure 1. BDV11-AA Component Side

PHYSICAL/FUNCTIONAL DESCRIPTION

The BDV11-AA is one variation of the BDV11. This course module describes the BDV11 module in general and the BDV11-AA in particular. Other variations of the BDV11, such as BDV11-AB, might be offered by DIGITAL at some later date. The only difference between BDV11-AA and other variations would be in the contents of 2K ROM diagnostic/bootstrap programs. Additionally, DEC has reserved an extra 2K space for adding future bootstrap capability.

Memory Space

The total ROM/EPROM memory space on BDV11 is 22K words. A ROM space of 4K words is reserved for DEC use. The remaining 18K is available for customer use, of which 2K words are for EPROM and 16K words are for either ROM or EPROM. Table 1 summarizes the ROM/EPROM chips used on the module.

Table 1. ROM/EPROM Chips

No of ROMs	Use	ROM Function
2	DIGITAL Diagnostics	2K Diagnostic/Bootstrap
2	Reserved by DIGITAL	2K Diagnostic/Bootstrap (Reserved for DEC use)
4	Customer	2K EPROM (Note 1)
16	Customer	16K ROM/EPROM (Note 2)

NOTES:

1. 2K EPROM space can be divided in half for 1K use.

2. 16K ROM customer area can be divided into eight 2K sections.

The 18K user ROM/EPROM can be executed directly or loaded into RAM for automatic execution upon completion of diagnostic programs. The user selects the diagnostic and/or bootstrap options by setting various switches on the BDV11 module. When power is applied to the system (or when the system is rebooted), the selected option is executed.

Memory Mapping

The 22K words of ROM/EPROM on the BDV11-AA are mapped into a 256-word address space in the I/O page. This space occupies the DIGITAL bootstrap from bus address 173000_8 to address 173776_8 (Figure 2).

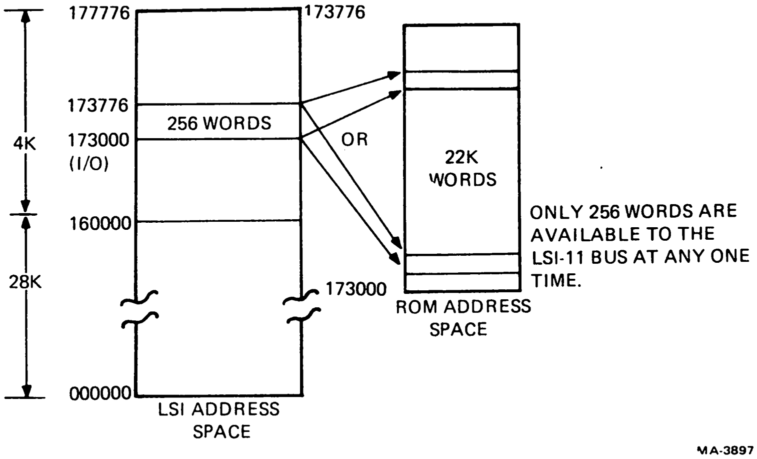


Figure 2. BDV11-AA Memory Mapping

The diagnostic/bootstrap programs are automatically executed by the CPU when power is applied to the system or when the system is rebooted. If any error occurs during the execution of diagnostics/bootstrap, the CPU halts and a diagnostic light display on the module indicates the specific area of the failure. When the CPU halts in this manner, it enters the halt mode and the address of the error is printed at the operator's console. The system now responds to the ODT commands. This is helpful in further diagnosing and troubleshooting.

The ROM sockets on the BDV11-AA are assigned to particular ROMs that perform various functions (Table 2). Figure 1 shows the ROM locations on the BDV11-AA module.

Switches, Indicators, and Tip Jacks

The BDV11-AA is equipped with several switches, indicators, and tip jacks (Figure 3). The two DIP switches, E15 and E21, allow selection of various diagnostics and bootstraps on powerup or restart. As an example, contact 5 of switch E21 permits program control of the LSI-11 line-time clock (LTC) function.

Table 2. Functions and Socket Assignments

Sockets	ROM Function
XE53/XE48	2K Diagnostic/Bootstrap
XE58/XE44	2K Diagnostic/Bootstrap (reserved for DEC)
XE57/XE4Ø	1K EPROM
XE52/XE36	1K EPROM
XE39/XE5Ø	2K System ROM
XE43/XE46	2K System ROM
XE47/XE42	2K System ROM
XE51/XE38	2K System ROM
XE55/XE37	2K System ROM
XE6Ø/XE41	2K System ROM
XE59/XE45	2K System ROM
XE54/XE49	2K System ROM

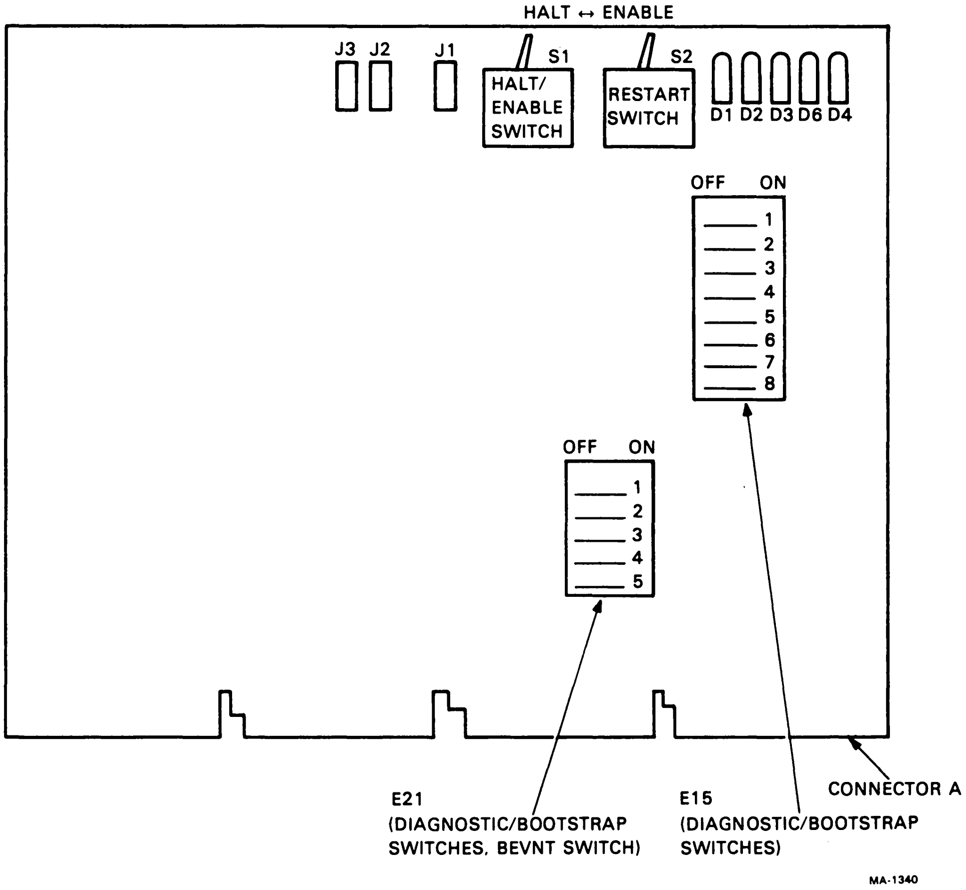


Figure 3. BDV11-AA Switches, Indicators, and Tip Jacks

A green Light-Emitting Diode (LED, D6) located in the upper right corner of the BDV11-AA indicates the condition of the dc power. Four other LEDs (D1, D2, D3, D4) display diagnostic information.

There are two test points (tip jacks) provided to monitor the +5 Vdc (J2, red) and the +12 Vdc (J3, purple) voltage outputs from the power supply. A third tip jack (J1, black) is the ground terminal.

Two switches, mounted between the LEDs and the tip jacks, are used to control certain functions of the CPU. Switch S1 is the Halt/Enable switch. It allows you to force the CPU into the halt mode. The second switch, S2, is the Restart switch that allows you to reboot the system. Figure 4 presents another view of the diagnostic LEDs, showing you how the power indicator, D6, is used as an octal separation point for the diagnostic light display.

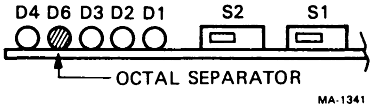


Figure 4. Diagnostic Light Display

Power OK LED

The green Power OK LED (D6) is lighted when the +12 Vdc voltage is greater than +1Ø V and the +5 Vdc supply voltage is greater than +4 V. These voltages can be measured on the tip jacks.

Jack	Color	Voltage
J1	Black	Ground
J2	Red	+5 Vdc
J3	Purple	+12 Vdc

The Power OK LED has a second function. It is used to separate the octal digits of the diagnostic light display, with LEDs D1, D2, and D3 on one side, and D4 on the other (Figure 4).

Halt/Enable Switch

When the Halt/Enable switch is in the enable position (towards the diagnostic lights), the LSI-11 CPU can operate under program control. If the switch is placed in the halt position (away from the diagnostic lights), the CPU enters the halt mode and responds to console ODT commands.

Restart Switch

When the Restart switch is cycled or switched away from the diagnostic lights and back again, the CPU automatically carries out a power-up sequence. Thus the system can be rebooted at any time.

BEVNT L Switch

Contact 5 of DIP switch E21 is the BEVNT L switch. The signal BEVNT L is used by the LSI-11 to control a LTC. If the BEVNT L signal is asserted, an interrupt will occur on the program sequence of the LSI to vector 1ØØ every 16.7 ms at a line frequency of 6Ø Hz or 2Ø.Ø ms at 5Ø Hz. When contact 5 of the switch is off (open) the LSI-11 bus BEVNT L signal cannot be controlled by the BDV11. It allows the LSI-11 power supply to control the LTC function. When the switch is on (closed), the LTC function is program-controlled.

Diagnostic/Bootstrap Switches

The DIP switches, E15 and E21, are used with each variation of the BDV11. The switches, except switch 5 of E21, allow the user to select diagnostic programs and/or a bootstrap program that runs automatically when power is turned on or when the system is rebooted. The 12 individual switches comprise the Option Select Register which can be read at bus address 177524_8. (The Option Select Register will be described in more detail later in this module.)

Some things to remember when using the BEVNT feature in the BDV11-AA are:

- Configure the power supply to disable the LTC features.

- Configure the CPU module to recognize the BEVNT signal.

The DIP switches on E15 and E21 are referred to in the following way:

- DIP switch E15
  A1, A2, A3, A4, A5, A6, A7, A8

- DIP switch E21
  B1, B2, B3, B4, B5

Diagnostic Light Display

The interpretation of the diagnostic light display will vary depending on the version of BDV11 with which you are working. The display will indicate a failure of a diagnostic or the bootstrap by providing an octal error display. An interpretation chart is included in the Theory of Operation portion of this module.

EXERCISE

Circle the letter of the correct response for each question. Check your answers with those given on the Solutions page.

1. The BDV11-AA has ____ words of memory space.

   a. 4K
   b. 8K
   c. 16K
   d. 22K

2. How much memory space in the BDV11-AA is reserved for customer use?

   a. 4K
   b. 8K
   c. 18K
   d. 22K

3. The I/O address range on the LSI bus that is reserved for the BDV11-A is:

   a. ØØØØØØ - 177776
   b. 16ØØØØ _ 173ØØØ
   c. 173ØØØ - 177776
   d. 173ØØØ - 173776

For questions 4 through 7, match the ROM functions to the ROM sockets used for those functions.

ROM Sockets — **ROM Functions**

4. ____ XE53/XE48 — a. 2K system ROM

5. ____ XE52/XE36 — b. 2K diagnostic/bootstrap

6. ____ XE58/XE44 — c. 1K EPROM

7. ____ XE43/XE46 — d. 2K diagnostic/bootstrap (reversed for future use by DEC)

SOLUTIONS

1. d
2. c
3. d
4. b
5. c
6. d
7. a

PROGRAMMING

There are several hardware registers in the BDV11-AA that perform control and diagnostic functions.

- Page Control Register (PCR)
- Read/Write Register
- Switch Register
- Display Register
- BEVNT Register

Page Control Register (PCR)

The bus address of the PCR (Figure 5) is 17752Ø$_{8}$. It is a 16-bit register that can be read or written. The PCR controls the mapping of the ROM pages into physical ROM addresses. It can be cleared during power up or when the Restart switch is activated.

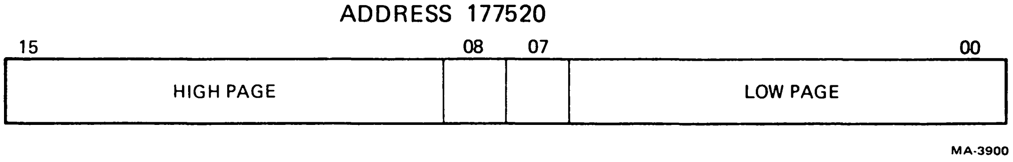


Figure 5. Page Control Register (PCR) Format

As mentioned earlier, the BDV11-AA ROM is mapped into a 256 address space on the LSI bus. When the low byte of the PCR is equal to page Ø, then LSI bus addresses 173ØØØ to 173376 will access the 128 ROM locations in the ØØØØ-Ø177 block or low byte of the diagnostic/bootstrap ROM. If the LSI bus address is in the range of 1734ØØ to 173776, the high byte of the PCR is used to point to another 128 ROM locations. The PCR contents normally would point to two consecutive ROM pages.

Read/Write Register

The Read/Write Register is a 16-bit maintenance register used for diagnostics. Its address is 177522 and, as its name implies, it can be read or written. The Read/Write Register is cleared when power is turned on or when the Restart switch is activated.

Switch Register

The Switch Register (Figure 6) is a 12-bit, read-only register with an address of 177524. It is used for maintenance and system configuration by selecting diagnostic and/or bootstrap programs for execution.

Bits Ø-11 of the register (corresponding to E15-1 through E15-8 and E21-1 through E21-4 respectively) are associated with BADL <Ø:11> L respectively; when an individual switch of the register is closed (on), the corresponding BDAL signal is low (1).

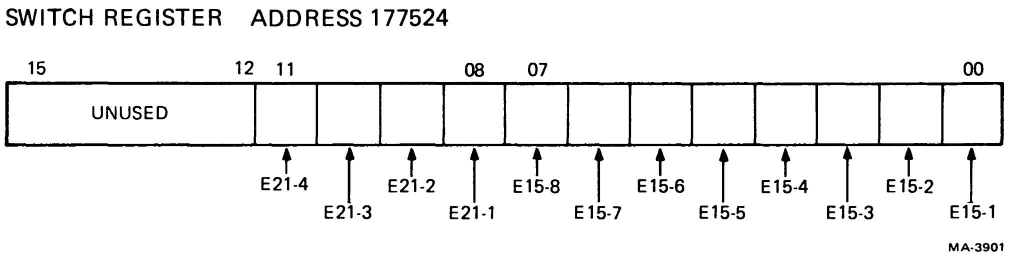


Figure 6. Switch Register Format

Display Register

The Display Register (Figure 7) is a 4-bit, write-only register at address 177524. You will notice that it is the same address as the Switch Register. If you read address 177524, you will get the contents of the Switch Register, and if you write to address 177524, you will write to the Display Register.

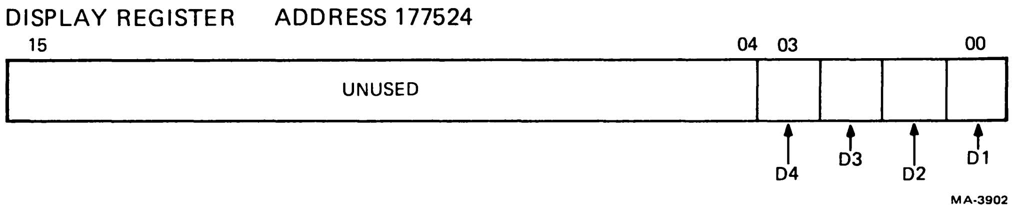


Figure 7. Display Register Format

Bits Ø-3 of the Display Register control LEDs D1-D4, respectively. When a bit is set, the corresponding LED is off. The Display Register is cleared (all lights on) when power is turned on or when the Restart switch is activated.

BEVNT Register

Finally, we have the BEVNT Register (Figure 8), a 1-bit, write-only register at address 177546. When cleared, this register clamps the BEVNT signal low (if the BEVNT switch is closed). This action permits program control of the LSI-11 LTC function. The BEVNT Register is cleared when power is turned on or when the Restart switch is activated.

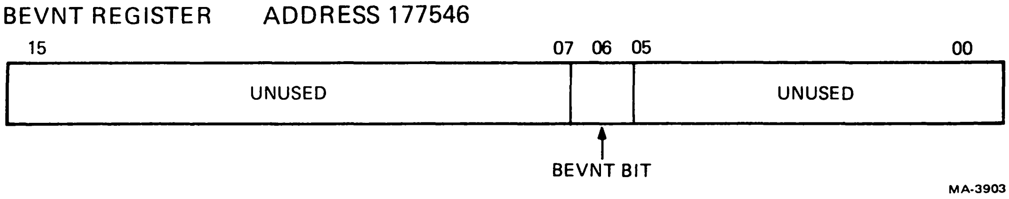


Figure 8. BEVNT Register Format

ROM Page Format Summary

All ROMs are accessed in a paged format of 128-word pages.

- 173000 to 173377 - Low Page
- 173400 to 173777 - High Page

The standard 256-word boot address space from 173000 to 173776 is broken into two 128 word "windows," and the ROMs are manipulated as a series of 128 word "pages." The mapping of pages into windows is controlled by a register at 177520 (PCR). The content of the low byte of the PCR is the binary number of the page mapped into the window from 173000 to 173776. The PCR is word- or byte-addressable, allowing operation on the PCR to map both windows individually or together. The PCR is cleared by the negation of BDCOK.

EXERCISE

Circle the letter of the correct response. Check your answers with those given on the Solutions page.

1. Diagnostic information is provided on the BDV11-AA by the:

   a. Diagnostic light display
   b. Diagnostic/Bootstrap switches
   c. BEVNT L switch
   d. 2K EPROM

2. The BEVNT Register contains:

   a. 1 bit
   b. 4 bits
   c. 12 bits
   d. 16 bits

3. The Display Register contains:

   a. 1 bit
   b. 4 bits
   c. 12 bits
   d. 16 bits

Match the registers listed to the LSI bus addresses for questions 4 through 8.

		Register	Address
4.	______	Page Control Register	a. 173000
5.	______	Read/Write Register	b. 177520
6.	______	Switch Register	c. 177522
7.	______	Display Register	d. 177524
8.	______	BEVNT Register	e. 177546

SOLUTIONS

1. a
2. a
3. b
4. b
5. c
6. d
7. d
8. e

CONFIGURING

The BDV11-AA has thirteen (13) jumper wires and two switch packs with thirteen (13) switches. The jumpers are used to select ROM sockets and memory chip types. The switches determine which of the programs stored in the ROMs will be selected.

BDV11-AA Jumpers

The BDV11-AA has sockets for diagnostic/bootstrap ROMs, EPROMs and system or user ROMs. Also the user is allowed to insert different types of ROM/EPROM chips in the sockets. Eight of the thirteen jumpers are used for socket selection. The remaining five are used for chip selection. Jumpers W1 through W4 and W9 through W12 control the socket selection logic. They can be configured seven different ways. You will almost always see the standard factory configuration. The alternate configurations allow the user to choose where program execution begins. The standard configuration is:

W1	W2	W3	W4	W9	W1Ø	W11	W12
R	I	I	R	I	R	R	I

where: I = Installed; R = Removed

The system ROM sockets can hold either 2K or 1K ROMs. The five-system ROM jumpers control the selection signals and allow either size ROMs to be used.

Diagnostic/Bootstrap Switches

The DIP switches, E15 and E21, allow the user to select diagnostic programs and/or a bootstrap program. The switches are designated A1 through A8, representing switches 1-8 of E15, and B1 through B4, representing switches 1-4 of E21. These 12 switches comprise the Switch Register that can be read at address 177524. Switches A1 through A4 are defined in Table 3.

DECnet boot arguments are presented in Table 4. All boots other than the above DECnet boots are controlled by the bit patterns in switches A5 through A8 and B1 (Table 5) or, if the console test is selected, by the mneumonic and unit number. The console test prompts with:

```
xx
START?
```

where xx is the amount of memory.

Table 3. Switch Functions

Switch	Setting	Function
A1	ON	Executes CPU test upon power up or restart.
A2	ON	Executes memory test upon power up or restart.
A3	ON	DECnet boot - A4, 5, 6 and 7 are arguments.
A4	ON	Console test and dialogue (A3 OFF).
A4	OFF	Turnkey boot dispatched by switch setting (A3 OFF).

Table 4. DECnet Boot Arguments

BOOT	A4	A5	A6	A7
DUV11	ON	OFF	OFF	OFF
DLV11-E	OFF	ON	OFF	OFF
DLV11-F	OFF	ON	OFF	ON

NOTE:
DLV11-E CSR = 17561Ø; DLV11-F CSR = 1765ØØ; DUV11 CSR = 16ØØ4Ø if no devices from 16ØØ1Ø to 16ØØ36.

You may respond with a two-character mnemonic with a one-digit octal unit number or one of two special single-character mnemonics. The response must be followed by a RETURN. The special single-character mnemonics are:

- Y Use switch settings to determine boot device.

- N Halt - Enter microcode ODT.

The features we have just seen allow the user to implement additional features or boots in additional ROMs without changing the base ROMs.

Table 5. Other Boots

Mnemonic	A5	A6	A7	A8	B1	Program Selected
	Ø	Ø	Ø	Ø	1	Loop on test
DKNN<8	Ø	Ø	Ø	1	Ø	RKV11 Boot
DLnn<4	Ø	Ø	1	Ø	Ø	RLV11 Boot
DXnn<2	Ø	1	Ø	Ø	Ø	RXV11 Boot
DYnn<2	Ø	1	1	Ø	Ø	RXV21 Boot
	1	Ø	Ø	Ø	Ø	ROM Boot[2]

NOTES:

1. All unused patterns (not shown) or mnemonics will default to ROM boot if switch B2, B3 or B4 is on.

2. The ROM boot uses switches B2, B3 and B4 to dispatch as follows:

B2	B3	B4	ROM
1	X	X	Extended diagnostic
Ø	1	1	27Ø8
Ø	Ø	1	System ROM

where X = 1 or Ø.

BEVNT L Switch (B5)

Switch 5 of E21 is used to allow program control of the LSI-11 bus LTC. When switch B5 is OFF, the BEVNT L signal is controlled by the LTC signal generated in the bus power supply. When the switch is ON, BEVNT L is controlled by the contents of the BEVNNT Register at address 177546. When bit 6 of this register is set and switch B5 ON, the BEVNT L signal on the LSI-11 bus is clamped low.

Halt/Enable Switch

The Halt/Enable switch on the BDV11-AA is used to control the LSI-11 CPU. When this switch is in the enable position, the processor can operate under program control. If the switch is placed in the halt position, the CPU enters the halt mode and responds to console ODT commands. While in this mode, the CPU can execute single instructions, allowing you to single step through a program.

Program control is re-established by returning the switch to the enable position and entering a "P" command at the console terminal providing that the contents of the PC (R7) are not changed.

Restart Switch

When the Restart switch is cycled or moved from side from side, the processor automatically carries out a power-up sequence. Using this switch, you can reboot the system at any time.

EXERCISE

Answer the following questions. Check your answers with those given on the Solutions page.

1. How are the BDV11-AA ROM socket selection jumpers configured when shipped with the standard configuration? (I = Inserted, R = Removed, X = I or R).

		W1	W2	W3	W4	W9	W1Ø	W11	W12
a.	___	R	I	I	R	I	R	R	I
b.	___	I	R	I	R	X	X	X	X
c.	___	X	X	X	X	R	I	R	I
d.	___	I	R	R	I	R	I	I	R

2. What switch must be turned on to execute the memory test on power up or restart?

   a. A1
   b. A2
   c. A3
   d. A4

3. If switches A3 and A4 are ON, the system will boot from:

   a. RXØ1
   b. RLØ1
   c. DLV11-E
   d. DUV11

4. Which of the following switches allows the BDV11-AA to control a LTC?

   a. The BEVNT L switch
   b. The Restart switch
   c. The Halt/Enable switch
   d. E15-A3
   e. E21-B1

5. The switch that allows the CPU to operate under program control is the:

   a. BEVNT L switch
   b. Restart switch
   c. Halt/Enable switch
   d. E15-A3
   e. E21-B1

SOLUTIONS

1. a

2. b

3. d

4. a

5. c

THEORY OF OPERATION

Since the maintenance philosophy of LSI systems is module replacement and the BDV11-AA is a module, it is not necessary to know all the minor details of how it works. For those who would like to understand better why or how the BDV11-AA might fail, however, this course module presents information on how the device works.

Figure 9 shows a block diagram of the BDV11 logic. The DC005 transceivers monitor the LSI-11 bus BDAL lines. When an address in the upper 4K bank of bus addresses is placed on the BDAL lines, the transceivers gate the address information onto the BDV11 DAL lines. If the address is one of those assigned to the BDV11 (173000-173777, 177520, 177522, 177524, 177546), the transceivers generate address match signals. These signals cause the control logic to decode the bus address and to respond to the protocol signals that effect bus data transfers.

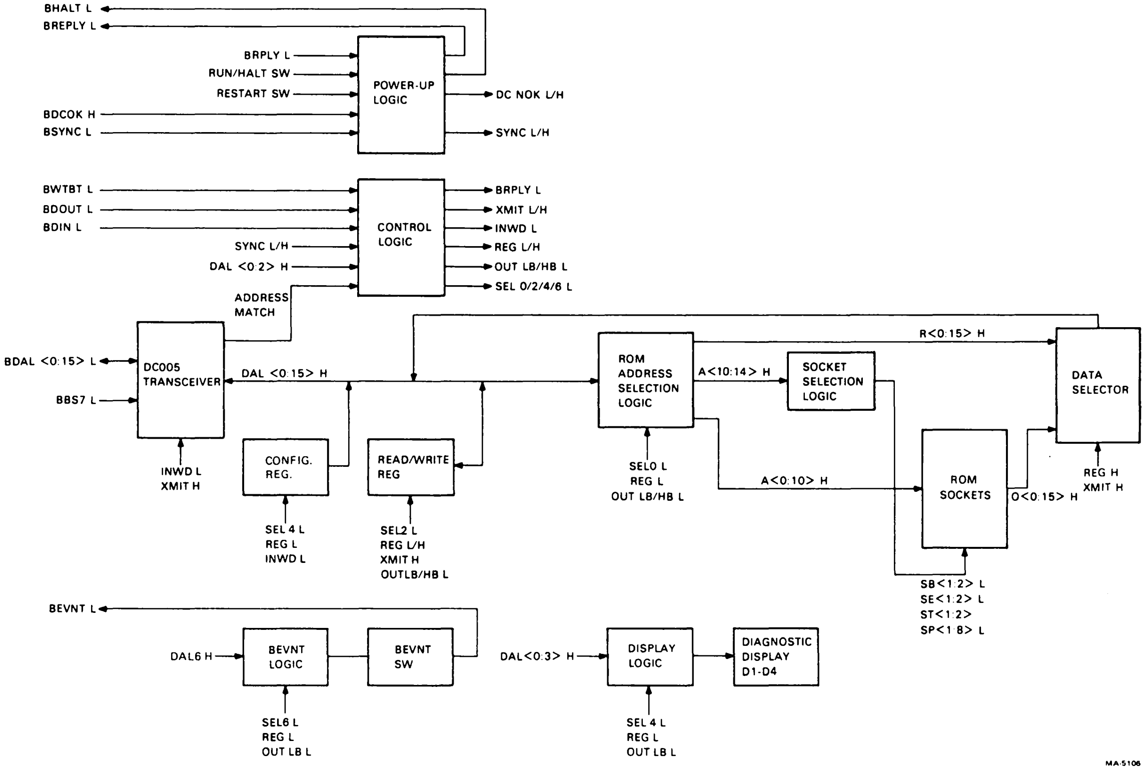


Figure 9. BDV11 Block Diagram

The bus address placed on the BDAL lines can be the address of one of the BDV11 registers, or the address of a ROM location. If one of the registers has been addressed, the control logic asserts those signals that are necessary to carry out the operation directed by the protocol signals that follow. For example, if the 16-bit Read/Write Register is addressed, the control logic asserts the signals that permit the register to be either read or written. When the actual transfer of data takes place, the information is gated to or from the register on the DAL lines in response to the protocol signals.

If the bus address is that of a ROM location, the address is loaded into the ROM address selection logic. This logic includes the PCR, which contains page information previously loaded by a writing operation. The address selection logic decodes the address and asserts relative address signals (AØ H - A1Ø H) that are applied to all the ROM sockets. Other address signals (A1Ø H - A14 H) are applied to the socket selection logic; this logic generates signals that select the particular ROM identified by the PCR page information. This ROM responds to the relative address signals and places the data in the addressed location on the O<Ø:15>H lines. The data is then gated onto the DAL lines by the data selector and placed on the BDAL lines in response to the protocol signals.

The data selector is also used when the PCR is read. When this operation is executed, the PCR page information carried on the R<Ø:15>L lines is gated onto the DAL lines and from those lines to the bus.

For more detailed information concerning BDV11-AA operation, refer to the BDV11 Technical Manual listed as an optional resource for this module.

PCR Pages

Table 6 lists the PCR pages used to select the various diagnostics and bootstraps in the BDV11-AA diagnostic ROMs.

Error Halts

Table 7 lists the error halts you may encounter when running the ROM diagnostics.

Table 6. PCR Pages

Page	PCR Contents	Function
Ø	ØØØ4ØØ	Pre-test, switch check, loop test
2	ØØ14Ø2	Memory test and CPU test
4	ØØ24Ø4	CPU test
6	ØØ34Ø6	Console terminal test
1Ø	ØØ41Ø	Power fail restart, RLVØ1 boot, RKV boot
12	ØØ5412	Floppy (RXØ1-RXØ2) bootstrap
14	ØØ6414	SLU bootstraps
16	ØØ7416	ROM bootstraps
2Ø	Ø2Ø	ROM address for diagnostic ROM 2
4Ø	Ø4Ø	ROM address for EPROM
2ØØ	2ØØ	Address for system ROM

Table 7. Error Halt Listing

PC Contents	ROM	PCR	Page	Cause of Error
173Ø22	B	14Ø2	2,3	Memory error 1. Write address into itself.
173Ø4Ø	G	6414	14,15	SLU switch selection incorrect: error in switches.
173Ø46	G	6414	14,15	SLU error, CSR address for selected device. Check CSR for selected device in floating CSR address area.
173Ø5Ø	A	4ØØ	Ø,1	CP1 error; RØ contains address of error.

Table 7. Error Halt Listing (Cont)

PC Contents	ROM	PCR	Page	Cause of Error
173Ø52	B	14Ø2	2,3	Memory error 2. Data test failed.
1731Ø6	B	14Ø2	2,3	Memory error 3. Write and read bytes failed.
1732Ø2	H	7416	16,17	ROM loader error. Checksum on data block.
17324Ø	D	34Ø6	6,7	CP4 error; RØ contains address of error.
173366	H	7416	16,17	ROM loader error. Checksum on address block.
1734Ø2	H	7416	16,17	ROM loader error. Jump address is odd.
173532	E	441Ø	1Ø,11	RL device error.
173634	C	24Ø4	4,5	CPU error 3. RØ points to cause of error.
173642	D	34Ø6	6,7	In console terminal test, "NO" typed.
173656	E	441Ø	1Ø,11	RK device error.
173656	A	4ØØ	Ø,1	Switch mode halt match was not made with switches.
17367Ø	D	34Ø6	6,7	Console terminal test. No done flag.
1737Ø6	B	14Ø2	2,3	CPU error 2. RØ points to cause of error.
173712	F	5412	12,13	RX device error.

LED Error Display

Table 8 provides you with the meaning of the LED display as viewed from the edge of the BDV11-AA. The diagnostics make use of the LEDs to give you an indication of what caused the diagnostic to fail while you were testing the device.

Table 8. LED Indications

Display Contents	Failing Function
All off	+12 Vdc or +5 Vdc bad.
All on	System hung, Halt switch on, or power-up mode wrong.
1	CPU fault or configuration error.
2	Memory error; R1 points to bad location.
3	Console CLU will not transmit.
4	Waiting for response from operator.
5	Load device fault.
6	Bootstrap incorrect (location Ø not = to NOP).
7	DECnet, waiting for response from host.
1Ø	DECnet, received done flag set.
11	DECnet, message received.
12	ROM boot error.
13	Power fail/restart.
14 - 16	Reserved for future use.

DIAGNOSTIC

The BDV11-AA diagnostic (CVM8A??) is used to check that the module is functioning properly. It does a checksum verification of the diagnostic ROMs and any additional ROM or EPROM. In addition, it will verify that the proper diagnostic ROMs are inserted in the module by comparing the actual checkwords in the ROMs to those specified in the diagnostic program. It will also accept checkwords from an operator for use in testing any additional ROM/EPROM. The diagnostic will also test the programmable registers and exercise the LEDs for operator inspection.

The minimum amount of hardware required to run the BDV11-AA diagnostic is:

- LSI-11 processor
- 16K words of memory
- Console terminal
- Diagnostic program load device

The diagnostic assumes that the CPU is running properly. It also assumes that the jumpers are configured properly and that all the memory chips are installed in the correct sockets.

Diagnostic Operation

Figure 1Ø is a sample of what a dialogue between you and the system might look like. Operator responses may vary from these, depending on system configuration and diagnostic revision level. The starting point for this dialogue is after XXDP is booted. The underlined items are operator responses to system questions. The time required to run a single error-free pass is less than three seconds.

```
.R VM8ABØ<CR>                (Load & run BDV11 Diagnostic.)
L_CLK (L) N ? Y<CR>          (Yes, I have a line clock.)
5Ø Hz (L) N ? <CR>           (No, it's a 6Ø Hz machine.)
LSI (L) N ? Y<CR>            (Yes, it's an LSI processor.)
LPT (L) N ? <CR>             (No line printer.)
MEM (K) (D) 16 ? <CR>        (Yes, I have at least 16K.)

DS-B>START/PASS:3<CR>
# UNITS (D) ? 1              (How many BDV11s?)
UNIT NUMBER (Ø) Ø ? <CR> (Unit number Ø)
INTERRUPT VECTOR ADDRESS (Ø) 1ØØ ? <CR>
INTERRUPT LEVEL (Ø) 7 ? <CR>
ROCKET SWITCH SETTINGS (Ø) 7777 ? 143<CR>
CHANGE SW (L) ? N<CR>       (Change ROM checkwords?)

BDV11-AA BOOTSTRAP DIAGNOSTIC PROGRAM

SWITCHES ON: ØØØ143: A1,A2,A6,A7,
STANDARD JUMPERS (L) Y ? <CR>
ANY ADDITIONAL MEMORY (L) N ? <CR>

(End of pass)  (Pass number)
CVM8AB   EOP    1BDV11-AA BOOTSTRAP DIAGNOSTIC PROGRAM
SWITCHES ON:    ØØØ143: A1,A2,A6,A7,

CVM8AB   EOP    2BDV11-AA BOOTSTRAP DIAGNOSTIC PROGRAM
SWITCHES ON:    ØØØ143: A1,A2,A6,A7,

CVM8AB   EOP    3

DS-B>
```

Figure 1Ø.   Operator/System Dialogue

Switch Check

The steps below give the recommended procedure to be followed when checking the switches on the BDV11-AA.

1. Power down the unit under test.

2. Remove the BDV11 (M8Ø12).

3. Set the switches E15-1 and E15-2 to the desired position.

E15-1	ON	CPU test enabled
	OFF	CPU test disabled
E15-2	ON	Memory test enabled
	OFF	Memory test disabled

4. Set switch E15-3 to the desired position.

E15-3	ON	DECnet boot enabled
	OFF	Not DECnet

If a DECnet boot was chosen, go to step 5. Otherwise go to step 6.

5. Set switches E15-4 through E15-7 to the desired position.

DECnet Boot Device	E15-4	E15-5	E15-6	E15-7
DUV11	ON	OFF	OFF	OFF
DLV11-E	OFF	ON	OFF	OFF
DLV11-F	OFF	ON	OFF	ON

a. If a programmable line clock is desired turn on switch E21-5.

b. Replace the BDV11.

c. Power up the unit under test.

6. Set switch E15-4 to the desired position.

E15-4	ON	Console test and dialog boot
	OFF	Turnkey boot

7. Set switches E15-5, -6, -7, -8, and E21-1 to the desired position for turnkey boot device or default dialogue boot.

Device	E15-5	E15-6	E15-7	E15-8	E21-1
RKØ5	OFF	OFF	OFF	ON	OFF
RLØ1	OFF	OFF	ON	OFF	OFF
RXØ1	OFF	ON	OFF	OFF	OFF
RXØ2	OFF	ON	ON	OFF	OFF

8. Only if a ROM boot is desired, set switches E15-5, E21-2, E21-3, and E21-4 to the desired position.

Boot Device	E15-5	E21-2	E21-3	E21-4
Extended diagnostic	ON	ON	OFF	OFF
27Ø8 type ROM	ON	OFF	ON	OFF
Program ROM	ON	OFF	OFF	ON

9. If a programmable line clock is desired, turn on switch E21-5.

1Ø. Replace the BDV11.

11. Power up the unit under test.

EXERCISE

Circle the letter of the correct response. Check your answers with those given on the Solutions page.

1. After loading XXDP, the command used to load and start the BDV11-AA is:

   a. LOAD VM8ABØ <CR>
   b. START VM8ABØ <CR>
   c. RUN VM8ABØ <CR>
   d. BEGIN VM8ABØ <CR>

2. The command used to start test number 1 of VM8ABØ and run it three times, ready to halt on an error is:

   a. START <CR>
   b. START/TEST:1/FLAG:LOE <CR>
   c. START/TEST:3/PASS:1/FLAG:HOE <CR>
   d. START/TEST:1/PASS:3/FLAG:HOE <CR>

SOLUTIONS

1. c

2. d

Now that you have completed this module, review the material you have covered. When you are ready, ask your Course Administrator for a copy of the Module Test. When you have completed the Module Test, return it to the Administrator for evaluation.

PDP-11V23/11T23 SYSTEM MAINTENANCE

11V23/11T23 SYSTEM LABORATORY

11V23/11T23 System Laboratory

INTRODUCTION

This is the last module in the PDP-11V23/11T23 System Maintenance course. The purpose of this module is to tie together all the ideas presented in previous modules. In addition to performing an acceptance test, you will learn how to load and run diagnostics. Emphasis is placed on setting the Software Switch Register and interpreting error messages. This module will show you how a properly functioning system operates, and how to locate faults in a defective system.

OBJECTIVES

1. Perform an acceptance test on an 11V23 system.
2. Load and run diagnostics, modify the Software Switch Register, and interpret error messages.
3. Isolate faults on an 11V23 system.

SAMPLE TEST ITEMS

1. Perform an acceptance test on an 11V23 system.
2. Load DZKMA, put 1Ø,ØØØ into the Software Switch Register, and interpret the error message.
3. Ask your Administrator for an 11V23 system with a fault in it. Isolate the fault and fill out a troubleshooting report.

RESOURCES

LSI-11/23 Troubleshooting Guide
(No number assigned)

INSTALLATION

Unpacking the System

The first step in any installation is to unpack the system. When unpacking the system you will find two major components: the computer cabinet and the terminal.

As you are unpacking the system, look for obvious mechanical damage such as dents, cracks, or any other breakage. Also be sure to listen for any loose parts rolling around inside the cabinets.

Powering Up the System

At this point you are ready to apply power to the system. In order to ensure an orderly and predictable power-up sequence, follow the power-up procedure given in Chapter 2 of the LSI-11/23 Troubleshooting Guide. This power-up procedure should always be used the first time power is applied to the system.

> READ
>
> Read Chapter 2 of the LSI-11/23 Troubleshooting Guide.

In an actual installation, if you did not get the required responses as described in the LSI-11/23 Troubleshooting procedure, you would continue troubleshooting. Since this is a training situation, however, and your system is working, you can now go into loading and running diagnostics.

Loading and Handling the Diskette

Insert the diskette into drive Ø (left drive) of the RXØ2. Refer to Figure 1 to load the diskette and to Figure 2 to remove it. When handling the diskette, observe the following precautions.

1. Do not write on the envelope containing the diskette. Write any information on a label prior to affixing it to the diskette.

2. Paper clips should not be used on the diskette.

3. Do not use writing instruments that leave flakes, such as lead or grease pencils, to label the envelope.

4. Do not touch the disk surface exposed in the diskette slot or index hole.

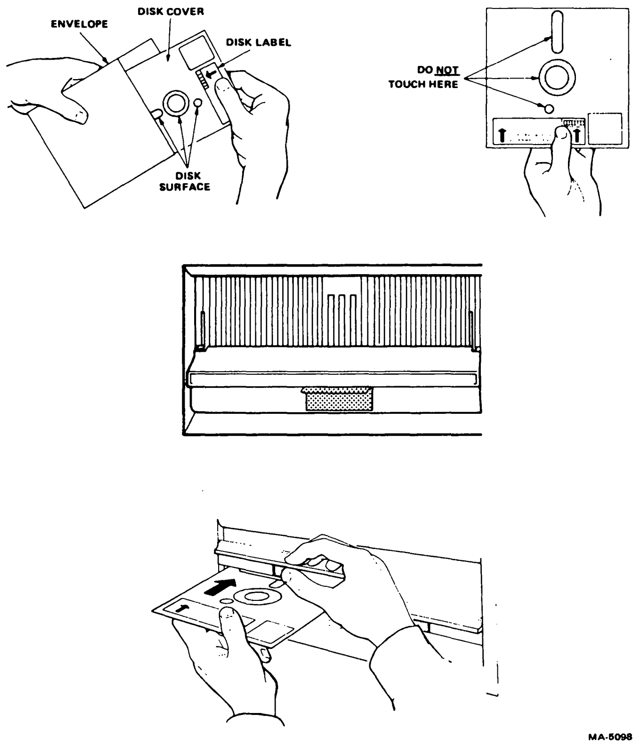


Figure 1. Loading the Diskette

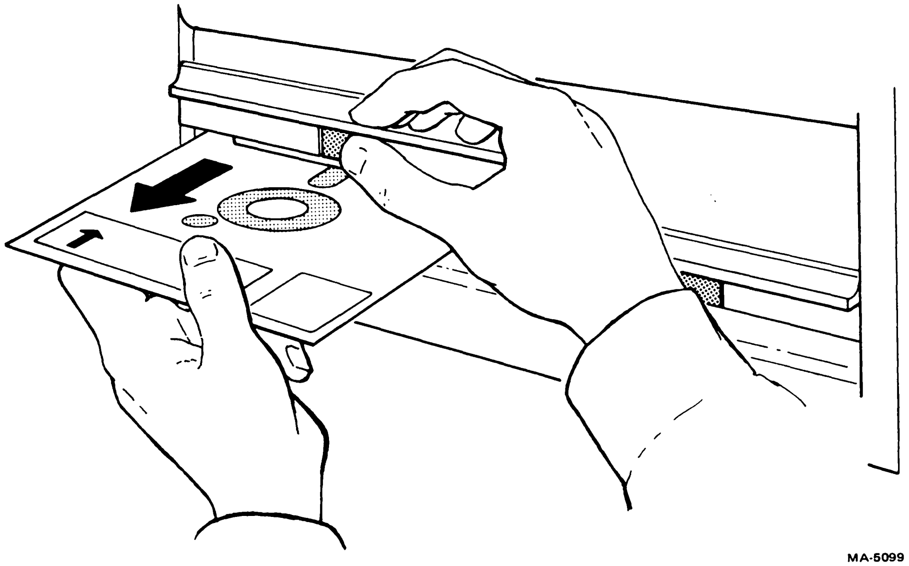


Figure 2. Removing the Diskette

5. Do not attempt to clean the disk in any manner.

6. Keep the diskette away from magnets or tools that may have become magnetized. A diskette exposed to a magnetic field may lose information.

7. Do not expose the diskette to a heat source or prolonged sunlight.

8. Always return the diskette to the envelope supplied with it to protect it from dust and dirt. Diskettes not being used should be stored in a file box, if possible.

9. When the diskette is in use, protect the empty envelope from liquids, dust, and metallic materials.

1Ø. Do not place heavy items on the diskette.

11. Do not store diskettes on top of computer cabinets or in places where dirt can be blown by fans into the diskette interior. Store diskettes in their envelopes in horizontal stacks of ten diskettes or less. If vertical storage is necessary, the diskettes should be supported so that they do not lean or sag, but should not be subjected to compression. Permanent deformation may result from improper storage.

12. If a diskette has been exposed to temperatures outside the range of the operating environment, allow five minutes for thermal stabilization before use. (The diskette must be removed from the envelope during this time.)

Booting the System

Before you can load any programs into memory you must first boot the system. This means that you will have to execute a program which is used for loading larger programs into memory. In the 11V23 system the bootstrap program is located in the BDV11 Bootstrap/Terminator option.

NOTE

This laboratory guide has been prepared for an 11V23 system. If you have an 11T23 system make the following substitutions:

1. RLDP for RYDP
2. DL FOR DY
3. Disk pack for floppy diskette

LAB EXERCISE 1

Booting the System and Loading RYDP

1. Power up the system according to Chapter 2 of the Troubleshooting Guide.

2. Obtain a diagnostic floppy diskette from your Course Administrator. Place the diskette in drive zero.

3. Enter the following command: DY <CR>

4. What type of message appeared on the terminal?

   ____

5. Is there a new prompt symbol? ____________________

6. You have just loaded RXDP from drive zero. Suppose drive zero is defective. You would now have to load RXDP from drive one. Do this by moving the diskette to drive one and entering: DY1 <CR>

7. Are the results in step 6 the same as those in steps 4 and 5? _______________

8. Return the diskette to drive zero and load RXDP one more time.

9. Finally you will run UPD2. This utility program helps you modify, load, and start diagnostic programs.

   Enter: R UPD3 <CR>

10. Enter today's date followed by a RETURN. Example: 17-AUG-79 <CR>.

11. Record the UPD3 restart address. ________________

After halting a diagnostic, if you wish to restart UPD3 you may do so by entering the restart address followed by a G.

Loading and Running Diagnostics

As part of the installation procedure, it is necessary for you to run a series of diagnostic programs. But before proceeding with the acceptance test, we will take time out and look at two diagnostic programs in particular. You will use these programs as examples of how to load and run diagnostics as well as how to interpret error messages. At the end of this module in Appendix A, you will find a technical summary of the diagnostics to be run on the 11V23 system. Use this Appendix for answering questions about the diagnostic programs.

LAB EXERCISE 2

Loading and Running Diagnostics

1. Load RYDP and UPD3 as described in the previous exercise. Record restart address. ________________

2. Obtain a directory of drive zero by entering:

   DIR DYØ: <CR>

3. Is VDLA BØ present? ________________

4. What option module is this diagnostic for? ________

   ____

5. Load the diagnostic by entering:
   LOAD DYØ: VDLABØ.BIC <CR>

6. Without any wraparound connectors installed, run the diagnostic for at least one pass. Enter:
   START 2ØØ <CR>

   When the diagnostic asks for the new contents of the Switch Register enter a <CR>.

7. Is an error message displayed? ___________
   This error indicates that wraparound connectors are required to successfully run this diagnostic. If you do not have wraparound connectors, go to step 11.

8. Install wraparound connectors in the three unused ports of the console DLV11-J.

9. Start the diagnostic at location 2ØØ and run it for at least one pass.

1Ø. Did the diagnostic run successfully? ___________

11. If you do not have any wraparound connectors, perform the following two-step procedure:

    a. Change location 122Ø from 1Ø31 to 1Ø11. This causes the diagnostic to skip the wraparound tests. Run the diagnostic for at least one pass.

    b. Restore location 122Ø to 1Ø31 and change location 1252 to a 1Ø. This causes the diagnostic to test only the console terminal (channel 3) for all tests including wraparound.

LAB EXERCISE 2 (Cont)

12. Restore location 1252 to 17 only if you have wraparound connectors.

13. What location is used as the Switch Register for this diagnostic? ______________

14. Set bit 12 in the Switch Register by entering 10000. This enables performance reporting. Run the diagnostic for several passes. What is the difference in the display?

    ____

15. Stop the CPU by pressing the BREAK key. Restart UPD3 by entering the restart address followed by a G. The restart address was recorded in step 1.

16. Using the same procedure described in step 5, load DZKMA.BIC. Start the diagnostic at location 200. Let the diagnostic run until at least one "END PASS" message is printed. This will take at least 10 minutes.

    DZKMA is a memory diagnostic. It checks memory by doing the following:

    a. Determines how large memory is.
    b. Checks memory above the diagnostic.
    c. Relocates and checks the memory locations that it was previously loaded in.

    As a result of this procedure, any program previously loaded in memory is lost.

17. After the first "END PASS" message, halt the processor using the BREAK key.

18. Examine the pass count location and error code location.

    Pass count __________

    Error code __________

19. The Switch Register location for this diagnostic is ________________________.

20. Look up the Switch Register settings. Enter 4000 into the Switch Register. This tells the diagnostic that you have the parity checking option. Since you do not have the parity option this will cause an error.

21. Start the diagnostic at location 2ØØ.

22. What is the error code displayed?

23. Look up this code and state the problem.

    ____

    ____

24. Restart UPD2 at the restart location. Will it start? ___________

25. Examine the restart location and several of the next sequential locations. What happened to UPD2?

    ____

    Why? ____

    ____

26. Reboot the system.

27. Run the BDV11 diagnostic (VM8ABØ).

28. Enter the following responses during the diagnostic dialogue.

    a. L-CLK (L) N? Y <CR>
    b. 5Ø Hz (L) N? <CR>
    c. LSI (L) N? Y <CR>
    d. LPT (L) N? <CR>
    e. MEM (K) (D) 16? <CR>

29. What is the prompt displayed?

    ____

30. Run the diagnostic for five passes by entering: START/PASS: 5 <CR>

31. There is one unit to be tested.

32. The unit number is Ø.

33. The interrupt vector is 1ØØ.

34. The interrupt level is 7.

35. When the diagnostic asks for the Rocker switch settings, if you do not know them, do the following.

    a. Default by entering a <CR>.

    b. Answer the next question. The diagnostic will now begin to run. It will print the correct switch settings and wait for more input.

    c. Write down the correct switch settings and reboot the system.

    d. Go back to step 27 and begin again.

36. The jumpers are standard.

37. No additional memory.

38. Did the diagnostic run for 5 passes? ___________

ACCEPTANCE

You have already learned how to unpack and power up the 11V23 system. To complete the installation it is necessary to run a series of diagnostics that will check out all the options. In the next Lab Exercise you will find out which diagnostics should be run in order to ensure that the system is running properly.

Installation and Acceptance Procedure

The normal sequence for the Installation and Acceptance procedure is given below.

1. Unpack all equipment
2. Visual inspection
3. Connect terminal
4. Power up equipment
5. Run diagnostics

Table 1 lists features normally found on the 11V23 system. Next to these features are listed the diagnostic programs that have to be run to check those features.

Table 1. 11V23 Features and Diagnostic Programs

Feature		Diagnostic Program
M8186	Processor	CJKDBA-A CJKDA-A
M8Ø44	MSV11-D/Memory	DZKMA
M8Ø43	DLV11-J SLU	CVDLAB
M8Ø12	BDV11 Boot/Terminator	DVM8ABØ
	RXV21 (RXØ2)	DZRXD

LAB EXERCISE 3

Acceptance Test

Run at least two passes of each of the following diagnostics.

1. CJKDBA-A, CPU diagnostic

2. CJKDA-A, MMU diagnostic

3. CVDLAB, DLV11-J diagnostic

4. DVM8ABØ, BDV11 diagnostic

5. DZKMA, Memory diagnostic

6. DZRXD, RXØ2 diagnostic

LAB EXERCISE 4

Configuring A System

You arrive at the local office of the American Widget Company expecting to install an 11T23 system. To your surprise you find several crates, which you are told contain their new custom-designed accounting system. To your further surprise when you unpack everything you find the following items:

1. Cabinet containing:

   a. Two RLØ1 disks
   b. One BA11-NC
   c. One BA11-NE

2. Four VT1ØØs. One to be used as a console terminal, the remaining three to be used as user terminals. Each VT1ØØ is set up for EIA-RS232, 96ØØ baud, eight data bits, no parity.

3. Two LA18Ø printers.

4. Two LPV11 (M8Ø27) printer interfaces. This is an interrupt type device.

5. Four MSV11-DD (M8Ø44) memories.

6. One DLV11-J (M8Ø43) four channel serial line unit.

7. One 11/23 (M8186) CPU with memory management and no floating point processor.

8. One RLV11 (M8Ø13, M8Ø14) RLØ1 interface. This interface consists of two quad-height logic boards and communicates by DMA. The boards are always placed in adjacent slots with the M8Ø13 above the M8Ø14.

9. One BDV11 (M8Ø12) boot/terminator board.

1Ø. One BCV1B consisting of an M94ØØ-YE, an M94Ø1 connector module, and two BCØ5L-Ø6 cables.

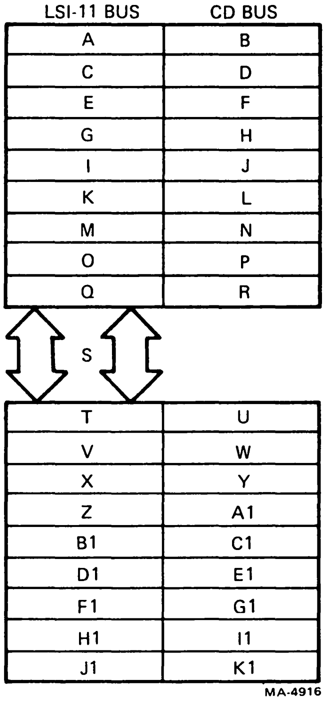
After smiling at the customer and assuring him/her that the system will be assembled shortly, you may begin to plan the system configuration on the worksheet that is provided.

Part I

Configure a system using the previously mentioned components. Remember that an 11/23 system may have no more than 124K words of memory. The last 4K word are used for the I/O page.

Look at the diagram of the two-backplane BA11-N system (Figure 3). Next to the option number, write the letter or letters which correspond with the location(s) where you would place the module into the backplane. Keep in mind that there will be many empty locations. You may use references. Most of the configuring information can be found in the BA11-N module.

1. M94ØØ-YE ____________________
2. M94Ø1 ____________________
3. Two BCØ5L-Ø6 cables ____________________
4. 1st M8Ø44 ____________________
5. 2nd M8Ø44 ____________________
6. 3rd M8Ø44 ____________________
7. 4th M8Ø44 ____________________
8. M8186 ____________________
9. M8Ø13 ____________________
1Ø. M8Ø14 ____________________
11. M8Ø43 ____________________
12. M8Ø12 ____________________
13. 1st 8Ø27 ____________________
14. 2nd 8Ø27 ____________________



LSI-11 BUS	CD BUS
A	B
C	D
E	F
G	H
I	J
K	L
M	N
O	P
Q	R

T	U
V	W
X	Y
Z	A1
B1	C1
D1	E1
F1	G1
H1	I1
J1	K1

Figure 3. Two-Backplane BA11-N System

LAB EXERCISE 4 (Cont)

Part II

For each module listed below, indicate whether jumpers are inserted or removed by writing an I or R next to the jumper number. If the position of the jumper makes no difference use an X. For switches use 1 for ON and Ø for OFF. Assume that the RLV11 and LPV11s are properly configured. Jumper numbers and functions will be found in the appropriate training module.

M8Ø44

1. S1-1 ________ 2. S1-2 ________ 3. S1-3 ________

4. S1-4 ________ 5. S1-5 ________ 6. W2 ________

7. W3 ________ 8. W4 ________ 9. W5 ________

1Ø. Pin 1 connected to pin ________.

11. S1-1 ________ 12. S1-2 ________ 13. S1-3 ________

14. S1-4 ________ 15. S1-5 ________ 16. W2 ________

17. W3 ________ 18. W4 ________ 19. W5 ________

2Ø. Pin 1 connected to pin ________

M8186

21. W4 ________ 22. W5 ________ 23. W6 ________

24. W8 ________ 25. W9 ________ 26. W1Ø ________

27. W11 ________ 28. W12 ________ 29. W13 ________

3Ø. W14 ________ 31. W15 ________

M8Ø43

32. A5 Connect pin X to pin ________

33. A6 ________

34. A7 ________

35. A8 Connect pin X to pin ________

36. A9 Connect pin X to pin ________

37. A1Ø Connect pin X to pin ________

38. A11 Connect pin X to pin ________

LAB EXERCISE 4 (Cont)

39. A12 Connect pin X to pin __________

4Ø. C1 Connect pin X to pin __________

41. C2 Connect pin X to pin __________

42. V5 Connect pin X to pin __________

43. V6 __________

44. V7 __________

45. E Connect pin X to pin __________

46. D Connect pin X to pin __________ all channels

47. S Connect pin X to pin __________

48. P Connect pin X to pin __________

49. Ø Connected to __________

5Ø. 1 Connected to __________

51. 2 Connected to __________ Baud rate

52. 3 Connected to __________

53. MØ Connect pin X to ________________

54. NØ Connect pin X to ________________

M8Ø12

55. A1 __________ 56. A2 __________ 57. A3 __________

58. A4 __________ 59. A5 __________ 6Ø. A6 __________

61. A7 __________ 62. A8 __________ 63. B1 __________

FAULT ISOLATION

Now that you have seen how a properly functioning system responds, you are going to have a chance to isolate some faults in a defective system.

There are three causes for problems in a small computer system. First of all, there are problems that are caused by shipping. These include breakage, loose logic boards, and loose cables. There are also problems that are caused by incorrect configuration. This includes incorrect jumper installation or empty slots in the backplane. Finally, there are problems caused by faulty FRUs.

With the last two types of problems, if diagnostics will run, it is a simple matter to run the diagnostic programs described in Exercise 3. The diagnostics will call out the faulty FRU.

If diagnostic programs will not run, you can use the LSI-11/23 Troubleshooting Guide. Chapter 1 of this guide explains how to use it; Figure 1 shows the procedure organization.

READ

Read Chapter 1 in the LSI-11/23 Troubleshooting Guide.

Remember, whenever you use this Guide, always start at Chapter 2, Verify Procedure.

LAB EXERCISE 5

Fault Isolation

Inform the Course Administrator that you are ready for the Fault Isolation exercise. He will place a fault in your PDP-11V23 system which you will have to isolate. As you are locating the problem, fill out the following Troubleshooting Report.

Troubleshooting Report

Name ____________________________ Badge No. ___________

Date __________System Type ______ Serial No. _________

Fault No. _____________

Visual inspection:

Will diagnostics run? ____________________

Failing diagnostic: ____________________

Error callout (if any): ________________________________

____

If diagnostics will not run, begin at Chapter 2 of the Troubleshooting Guide and follow the sequence until you find the fault.

Step no. in Guide which called out problem: __________

What is the fault?

Is this a configuration problem or must the FRU be replaced?

Administrator Signoff: ______________________________

Troubleshooting Report

Name ______________________________ Badge No. ____________

Date ___________System Type ______ Serial No. _________

Fault No. ______________

Visual inspection:

Will diagnostics run? ______________________

Failing diagnostic: ______________________

Error Callout (if any) ___________________________________

____

If diagnostics will not run, begin at Chapter 2 of the Troubleshooting Guide and follow the sequence until you find the fault.

Step no. in Guide which called out problem:

What is the fault?

Is this a configuration problem or must the FRU be replaced?

Administrator Signoff: ____

Troubleshooting Report

Name ______________________________ Badge No. ____________

Date ___________System Type ______ Serial No. __________

Fault No. ______________

Visual inspection:

Will diagnostics run? ______________________

Failing diagnostic: ______________________

Error callout (if any): ___________________________________

____

If diagnostics will not run, begin at Chapter 2 of the Troubleshooting Guide and follow the sequence until you find the fault.

Step no. in Guide which called out problem: ___________

What is the fault?

Is this a configuration problem or must the FRU be replaced?

Administrator Signoff: ____

Troubleshooting Report

Name ______________________________ Badge No. ____________

Date ___________System Type ______ Serial No. _________

Fault No. ______________

Visual inspection:

Will diagnostics run? ______________________

Failing diagnostic: ______________________

Error callout (if any): ____________________________________

____

If diagnostics will not run, begin at Chapter 2 of the Troubleshooting Guide and follow the sequence until you find the fault.

Step no. in Guide which called out problem:

What is the fault?

Is this a configuration problem or must the FRU be replaced?

Administrator Signoff: ____

Troubleshooting Report

Name ______________________________ Badge No. ____________

Date ___________System Type ______ Serial No. __________

Fault No. ______________

Visual inspection:

Will diagnostics run? ____________________

Failing diagnostic: ____________________

Error callout (if any): ________________________________

____

If diagnostics will not run, begin at Chapter 2 of the Troubleshooting Guide and follow the sequence until you find the fault.

Step no. in guide which called out problem: ___________

What is the fault?

Is this a configuration problem or must the FRU be replaced?

Administrator Signoff: _____________________________________

APPENDIX A

DIAGNOSTIC PROGRAM

SUMMARIES

Diagnostic Name:
CJKDBA-A
Use JKDBA?.BIC for XXDP

Diagnostic Title:
F-11 CPU Diagnostic

Diagnostic Function:
Part I - Checks basic instruction set in every addressing mode.
Part II - Checks all operations that cause traps
Part III - Checks the extended instruction set (EIS)

Starting Addresses:
Normal 2ØØ
Restart 1Ø24

Switch Register Settings:
Location 176
Bit 15 = 1 halt on error
Bit 13 = 1 inhibit error printout

Error Reporting:
Part I and II halt on error
Part III prints error message

Execution Time:
1 second

End of Pass Indication:
Prints END PASS after first pass. This message is repeated about every 15 seconds.

Diagnostic Name:
CJKDA-A
Use JKDA?.BIC for XXDP

Diagnostic Title:
F-11 MMU Diagnostic

Diagnostic Function:
Checks memory management unit (MMU) logic.

Starting Address:
Normal 200
Restart none

Switch Register Settings:
Location 176

Bit 15 = 1	Halt on error
Bit 14 = 1	Loop on test
Bit 13 = 1	Inhibit error printouts
Bit 12 = 1	Inhibit trace trap
Bit 11 = 1	Inhibit subtest iterations
Bit 10 = 1	Bell on error
Bit 9 = 1	Loop on error
Bit 8 = 1	Loop on test indicated by bits 7:0.

Error Reporting:
The diagnostic gives the following information:

1) address of failing register in MMU
2) written data in octal
3) read data in octal
4) read data in binary
5) test number
6) PC of error

Execution Time:
Approximately 30 seconds.

End of Pass Indication:
After every pass the diagnostic prints:

End of pass #(number) total errors since last report (number)

NOTE

The CPU diagnostic (CJKDBA-A) should be run before this diagnostic.

Diagnostic Name:
CVDLAB
Use CVDLA? for XXDP

Diagnostic Title:
DLV11-J test

Diagnostic Function:

1. Tests each channel of the DLV11-J individually.

2. Tests all four channels for interaction.

Starting Addresses:
Normal
Restart

Switch Register Settings
Location 176

Bit 15 SET	=	100000	=	HALT ON ERROR
BIT 14 SET	=	40000	=	LOOP ON TEST (TO BE USED ONLY WHILE TESTING IN PROGRESS)
BIT 13 SET	=	20000	=	INHIBIT ERROR TYPEOUTS
BIT 12 SET	=	10000	=	ENABLE PERFORMANCE REPORTS
BIT 11 SET	=	4000	=	INHIBIT ITERATIONS
BIT 10 SET	=	2000	=	BELL ON ERROR
BIT 9 SET	=	1000	=	LOOP ON ERROR
BIT 8 SET	=	400	=	LOOP ON TEST IN SWR<7:0>
7:0	=			NUMBER OF TEST TO LOOP ON (USED WITH BIT 8) (ALL TESTS PREVIOUS TO THE SELECTED TEST ARE EXECUTED FIRST WITH ONE ITERATION ONLY)

Error Reporting:
When a failure occurs the diagnostic reports the following:

1. Test number
2. Error number
3. Failing PC
4. DLV11-J address
5. DLV11-J vector

Execution Time:
30 second for first pass
90 second for each additional pass

End of Pass Indication:
Print "End Pass" #(pass number)
If Bit 12 in Switch Register is set a complete performance report will be printed.

NOTE

See lab guide for additional information on this diagnostic.

Diagnostic Name:
DZKMA.BIC
Use ZKMA??.BIC for XXDP

Diagnostic Title:
MOS/Core Ø-124K exerciser.

Diagnostic Function:
Tests memory in any PDP-11 series computer. The execution of this diagnostic causes any programs in memory, such as XXDP and Update, to be lost.

Starting Address:
Normal 2ØØ
Restart 25Ø

Switch Register Settings:
Location 176

BIT15 (1ØØØØØ)	HALT ON ERROR
BIT14 (Ø4ØØØØ)	LOOP IN SUBTEST DEFINED BY BITS <3:Ø>
BIT13 (Ø2ØØØØ)	INHIBIT ERROR PRINTOUTS
BIT12 (Ø1ØØØØ)	ENABLE TESTING ABOVE 28K (MEMORY MANAGEMENT)
BIT11 (ØØ4ØØØ)	ENABLE PARITY TESTING
BIT1Ø (ØØ2ØØØ)	HALT AFTER EACH SUBTEST
BITØ9 (ØØ1ØØØ)	INHIBIT PROGRAM RELOCATION
BITØ8 (ØØØ4ØØ)	TYPE FIRST FAILING BIT ERROR PER 4K.
BITØ7 (ØØØ2ØØ)	ENABLE LONG GALLOPING TEST
BITØ6 (ØØØ1ØØ)	INHIBIT MEMORY SIZING
BITØ5 (ØØØØ4Ø)	INHIBIT "END PASS #XX" PRINTOUTS
BITØ4 (ØØØØ2Ø)	INHIBIT PRINTOUTS
BITØ3 -BITØØ	BEGINNING TEST NUMBER.

No special settings required.

Special Locations:
Location 4Ø6 is the octal pass count
Location 4Ø4 is the octal test number
Location 4Ø2 is the octal error code.

Error Reporting:

THE ERROR PRINTOUT CONSISTS OF SIX OCTAL WORDS IN THE FOLLOWING FORMAT:

"LOCATION   GOOD   BAD   PC   ERROR PASFLG"

"ADR ERR" WILL BE PRINTED PRIOR IF AN ADDRESSING ERROR IS SUSPECTED.
"PAR ERR" WILL BE PRINTED PRIOR IF A PARITY ERROR TRAP OCCURRED!
CAUTION! IF PARITY ERROR THE GOOD DATA PRINTOUT IS THE PARITY MODULE UNIBUS ADDRESS THAT FAILED.

WHERE:

LOCATION	=	FAILING MEMORY LOCATION
GOOD	=	GOOD DATA [DATA THAT WAS EXPECTED]
BAD	=	BAD DATA [DATA THAT WAS FOUND]
PC	=	PROGRAM COUNTER AT ERROR CALL.
ERROR	=	FAILING ERROR NO. (SEE SEC 6.2 - ERROR DICTIONARY)
PASFLG	=	CONTENTS OF LOCATION PASFLG. THIS MAY NOT BE RELEVANT. (SEE SEC. 6-2 - ERROR DICTIONARY)

THE TEST WILL CONTINUE AFTER THE ERROR PRINTOUT.
"NO MNG" WILL BE TYPED IF TESTING ABOVE 28K SELECTED AND NO MEMORY MANAGEMENT IS FOUND.

"NO PAR" WILL BE TYPED IF PARITY OPTION SELECTED AND NO PARITY MODULES WERE FOUND.

(FATAL ERRORS)

"ERROR #XXXXXX" WILL BE TYPED WHERE "XXXXXX" IS THE ERROR NUMBER. THE DIAGNOSTIC WILL USUALLY HALT ON THIS TYPE OF ERROR. SEE ERROR CODE DICTIONARY FOR DESCRIPTIONS OF THE ERROR.

Error Code Dictionary

This is a list of error numbers printed and possible causes for errors.

ERROR # Ø

[BUSER] BUS ERROR TRAP TO LOC. 4 OCCURRED THIS ERROR IS NOT PRINTED AND IS FOR "APT" USE.

ERROR # 1

[TSTTRP]FATAL DATA ERROR
LOCATIONS ØØØØ-43Ø FAILED 1'S + Ø'S TEST.
RØ = GOOD DATA
R1 = ADDRESS OF FAILING LOCATION.

ERROR # 2

[APTSIZ] APT FATAL ERROR
APT MEMORY TABLES NOT SETUP CORRECTLY.
CHECK LOCATIONS $MAMS1 [43Ø] TO $MADR4 [446] FOR CORRECT MEMORY SIZE DATA.

ERROR # 3

[TSTSIZ] OPERATOR FATAL ERROR
SELECTED MEMORY SIZE GREATER THAN 28K, BUT SR BIT12 (1ØØØØ) NOT SET. SET BIT12 AND RESTART AT 2ØØ.

ERROR # 4

[TSTSIZ] OPERATOR FATAL ERROR LOWEST SELECTED TEST LIMIT IS HIGHER THAN HIGHEST TEST LIMIT. SET LOCATIONS "LOWTWO"[322]TO "HIGHADD" [33Ø] CORRECTLY AND RESTART AT 2ØØ.

ERROR # 5

[TSTØ] TEST SEQUENCE ERROR
TSTØ HAS BEEN ENTERED OUT OF SEQUENCE
TESTN SHOULD = ØØ
THE DIAGNOSTIC HAS BEEN CORRUPTED.
IF POSSIBLE SELECT ANOTHER 4K BANK BANK Ø AND RERUN THE TEST ON THE FAILING MEMORY.

ERROR # 6

[TSTØ] DUAL ADDRESSING ERROR
FOR THIS ERROR THE GOOD DATA PRINTED IS AN ADDRESS. THIS IS THE ADDRESS SELECTED WHEN THE SAME DATA WAS WRITTEN INTO THE FAILING LOCATION. CHECK BANK SELECT CIRCUITRY.

ERROR # 7

[TSTØ] ADDRESS AND DATA ERROR
IDENTICAL TO PREVIOUS ERROR EXCEPT THE DATA WRITTEN INTO THE FAILING LOCATION WAS IN ERROR ALSO.

ERROR # 8

[TSTØ] DATA ERROR
IF BAD DATA = ØØØØ COULD BE AN ADDRESSING ERROR, ELSE COMPARE GOOD AND BAD DATA FOR FAILING BITS.

ERROR # 11 [TSTØ] ADDRESSING ERROR
THE FAILING ADDRESS RESPONDED BUT IS NON-EXISTENT. MAY BE A DUAL ADDRESSING PROBLEM.

ERROR # 12 [TST1] TEST SEQUENCE ERROR
$TEST [4Ø4] SHOULD = Ø1
THE DIAGNOSTIC HAS BEEN CORRUPTED.

ERROR # 13 [TST1] DATA ERROR
COMPARE GOOD AND BAD PRINTED DATA, FAILING DATA BITS MAY BE SHORTED OR SWAPPED.

ERROR # 14 [TST2] TEST SEQUENCE ERROR
$TESTN [4Ø4] SHOULD = Ø2
THE DIAGNOSTIC HAS BEEN CORRUPTED.

ERROR # 15 [TST2] ADDRESS OR DATA ERROR
IF "ADR ERR" NOT PRINTED THEN THE BYTE SELECT CIRCUITRY PROBABLY FAILED.

ERROR # 16 [TST3] TEST SEQUENCE ERROR
$TESTN [4Ø4] SHOULD = Ø3
THE DIAGNOSTIC HAS BEEN CORRUPTED.

ERROR # 17 [TST3] DUAL ADDRESSING ERROR
DUAL ADDRESSING PROBLEM FOR BITS THAT DIFFER IN GOOD AND BAD DATA PRINTOUT.

ERROR # 2Ø [TST3] DUAL ADDRESSING ERROR
FOR THIS ERROR THE DATA PRINTED IS AN ADDRESS.
THIS IS THE ADDRESS THAT WAS SELECTED WHEN THE SAME DATA WAS WRITTEN INTO THE FAILING LOCATION.

ERROR # 21 [TST3] DUAL ADDRESSING ERROR
SAME AS ERROR #2Ø EXCEPT DIFFERENT DATA (SWAPPED BAKPAT) WAS WRITTEN.

ERROR # 22 [TST4] TEST SEQUENCE ERROR
$TESTN [4Ø4] SHOULD = Ø4.
THE DIAGNOSTIC HAS BEEN CORRUPTED.

ERROR # 23 [TST4] DUAL ADDRESSING ERROR
IF PASFLG = Ø THEN THE FAILING LOCATION AND FAILING DATA ARE DUAL ADDRESSES.

ERROR # 24 [TST5] TEST SEQUENCE ERROR
$TESTN [4Ø4] SHOULD = Ø5 THE DIAGNOSTIC HAS BEEN CORRUPTED.

ERROR # 25 [TST5] DATA ERROR
DATA WRITE OR READ ERROR.

ERROR # 26 [TST5] MARCHING 1'S AND Ø'S DATA ERROR
IF PASFLG = Ø FAILED MARCHING 1'S + Ø'S IN MAX TO MIN DIRECTION.
IF PASFLG = 1 FAILED MARCHING 1'S + Ø'S IN MIN TO MAX DIRECTION.
IF PASFLG = 3 FAILED MARCHING Ø'S + 1'S IN MAX TO MIN DIRECTION.

ERROR # 27 [TST5] MARCHING 1'S AND Ø'S DATA ERROR
IDENTICAL TO PREVIOUS ERROR EXCEPT THE DATA IS CHECKED IMMEDIATELY AFTER BEING WRITTEN.

ERROR # 3Ø [TST6] TEST SEQUENCE ERROR
$TESTN SHOULD = Ø6
THE DIAGNOSTIC HAS BEEN CORRUPTED.

ERROR # 31 [TST6] VOLATILITY/REFRESH TEST ERROR
IF PASFLG = Ø BAKPAT AT WRITE OR READ ERROR.
IF PASFLG = 1 THE FAILING LOCATION CHANGED WHILE ANOTHER LOCATION WAS WRITTEN FOR 2 MS. THE OTHER LOCATION IS SAVED IN SAVLOC [353]
IF PASFLG = 2 SWAPPED BAKPAT (774ØØ OR 77ØØØ) WRITE OR READ ERROR.
IF PASFLG = 3 SAME AS IF PASFLG = 2 EXCEPT THE DATA IS SWAPPED BAKPAT.

ERROR # 32 [TST7] TEST SEQUENCE ERROR
$TESTN SHOULD = Ø7
THE DIAGNOSTIC HAS BEEN CORRUPTED.

ERROR # 33 [TST7] SHIFTING DIAGONAL DATA ERROR
IF PASFLG = Ø BAKPAT WRITE OR READ ERROR.
IF PASFLG = 1 BAKPAT READ CHECK ERROR
IF PASFLG = GREATER THAN 1 BUT EVEN VALUE THEN:
THE FAILING LOCATION COULD NOT BE WRITTEN INTO.
IF PASFLG = GREATER THAN 1 BUT ODD VALUE THEN:
THE FAILING LOCATION WAS WRITTEN CORRECTLY BUT LOST THE DATA.

ERROR # 34 [TST1Ø] TEST SEQUENCE ERROR
$TESTN SHOULD = 1Ø
THE DIAGNOSTIC HAS BEEN CORRUPTED.

ERROR # 35 [TST1Ø] BAKPAT DATA ERROR
BAKPAT WRITE OR READ ERROR INTO THE FAILING LOCATION.

ERROR # 36 [TST1Ø] READ RECOVERY DATA ERROR

THIS ERROR CAN BE REPORTED BY TST1Ø AND TST11. (THEY SHARE CODE). SEE $TESTN [4Ø4] FOR WHICH TEST FAILED.

FOR BOTH TESTS COMPARE THE GOOD AND BAD DATA AT THE FAILING LOCATION TO SEE WHICH BITS FAILED.

ERROR # 37 [TST1Ø] READ RECOVERY DATA ERROR

IDENTICAL TO THE PREVIOUS ERROR EXCEPT SWAPPED BAKPAT IS USED AS WRITE AND READ DATA.

ERROR # 4Ø [TST11] TEST SEQUENCE ERROR

$TESTN SHOULD = 11

THE DIAGNOSTIC HAS BEEN CORRUPTED.

ERROR # 41 [TST12] TEST SEQUENCE ERROR

$TESTN SHOULD = 12

THE DIAGNOSTIC HAS BEEN CORRUPTED.

ERROR # 42 [TST12] WORST CASE CORE TEST DATA ERROR

IF PASFLG = 1 COMPARE GOOD AND BAD DATA FOR FAILING BITS.

IF PASFLG = 2 THE FAILING LOCATION WAS WRITTEN AND READ WITH GOOD DATA, BUT FAILED READ CHECK READING IN THE MIN. TO MAX DIRECTION.

IF PASFLG = 3 SAME CONDITIONS AS PASFLG = 2 EXCEPT FAILED DOING THE READ CHECK FROM MAX TO MIN DIRECTION.

ERROR # 43 [TST12] WORST CASE CORE TEST DATA ERROR

IDENTICAL TO PREVIOUS ERROR EXCEPT THE DATA WRITTEN AND READ IS COMPLEMENTED.

ERROR # 44 [TST13] TEST SEQUENCE ERROR

$TESTN SHOULD = 13

THE DIAGNOSTIC HAS BEEN CORRUPTED.

ERROR # 45 [TST13] WRITE RECOVERY TEST DATA ERROR

IF PASFLG = Ø COMPARE GOOD AND BAD DATA FOR FAILING BITS.

IF PASFLG = 774ØØ DATA ERROR FOUND WHILE DOING A SECOND READ CHECK. IF PASFLG = 774Ø2 DATA ERROR FOUND IN FAILING LOCATION AFTER SMALL TEST PROGRAM RUN IN FAILING BANK.

ERROR # 46 [TST13] WRITE RECOVERY TEST DATA ERROR

DATA ERROR FOUND JUST BEFORE THE SMALL TEST WAS TO BE RUN IN THE FAILING BANK. TO AVOID "BLOWING" UP WHEN THE SMALL TEST IS RUN TST13 IS ABORTED.

ERROR # 47 [TST13] WRITE RECOVERY TEST DATA ERROR
IDENTICAL TO ERROR $XXX EXCEPT THE DATA WRITTEN AND READ IS DIFFERENT. (177667).
177667 IS THE COMPLEMENT OF "JMP (RØ)" (11Ø) WHICH IS THE ESCAPE FROM THE SMALL TEST PROGRAM RUN IN THE BANK UNDER TEST.

ERROR # 5Ø [PARERR] PARITY TRAP ERROR
PARITY TRAP TO 114 OCCURRED.
FOR THIS ERROR PRINTOUT THE "GOOD DATA" IS ACTUALLY THE FAILING PARITY MODULE UNIBUS ADDRESS.
SAVLOC [352] CONTAINS THE PC WHERE THE TRAP OCCURRED.

ERROR # 51 [PARITY] PARITY TRAP FATAL ERROR
A PARITY TRAP TO 114 OCCURRED, BUT NO PARITY MODULES COULD BE FOUND WITH AN ERROR BIT (BIT15) SET.

ERROR # 52 [NOMM] OPERATOR FATAL ERROR
TESTING ABOVE 28K WAS SELECTED, BUT NO MEMORY MANAGEMENT OPTION WAS FOUND.
RESET SWITCH OPTIONS AND RESTART AT 2ØØ.

ERROR # 53 [PARITY] OPERATOR FATAL ERROR
PARITY TESTING WAS SELECTED BUT NO PARITY MODULES WERE FOUND.
RESET SWITCH OPTIONS AND START AT 2ØØ.

Execution Time:
About 12 minutes with 16K of memory

End of Pass Indication:
Types out "END PASS (number)" after every pass

NOTE

Since this diagnostic wipes out memory, it should be the last diagnostic run.

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